VOLUME 2 OF 2

ADDENDUM TO

FINAL REPORT

FOR

NIMBUS DESIGN STUDY

CONTRACT NO. NAS 5-3787

Prepared by

RADIATION INCORPORATED

MELBOURNE, FLORIDA

For

GODDARD SPACE FLIGHT CENTER

GREENBELT, MARYLAND

FACILITY FORM 602

N67-24621
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(CATEGORY)

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Approved By:

Project Manager

APPENDIX I

DRAWINGS

APPENDIX I

DRAWINGS

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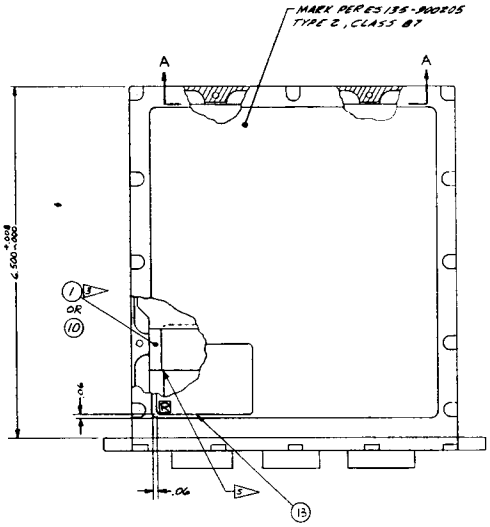
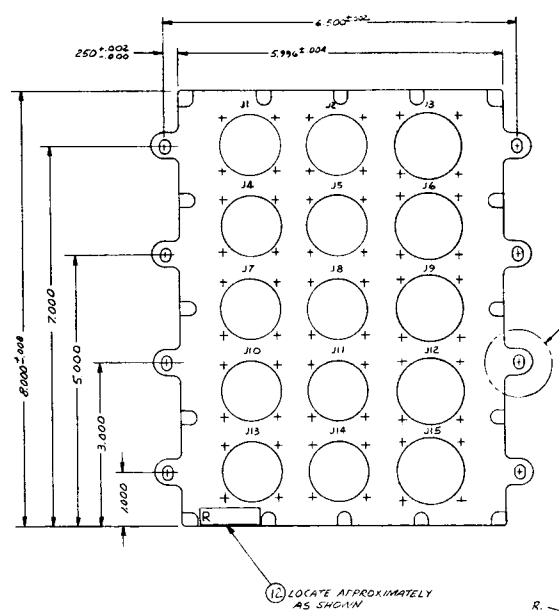
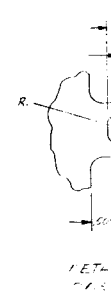
This appendix contains all detailed drawings referenced in the main body of the addendum to the Final Report for Nimbus Design Study.

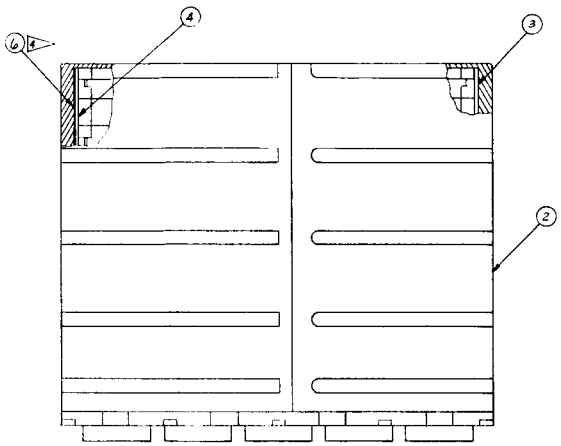

MARK PER ES 135-900205
TYPE 2, CLASS B7
A
A
6.500 +.008 -.000
1
OR
10
.06
.06
13

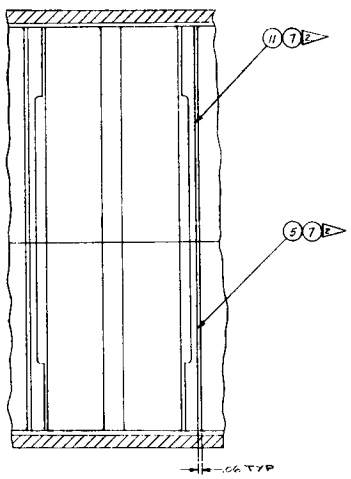

6.500 ±.002
250 +.002 -.000
5.996 ±.004
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
J13
J14
J15
8.000 ±.008
7.000
5.000
3.000
1.000
R
12 LOCATE APPROXIMATELY AS SHOWN


R.

NOTES:

1. FOR PROCUREMENT OR PART NUMBER, SEE SPEC OR SOURCE CONTROL DRAWING.
2. BOND ITEM 5 & 7 TO ITEM 2 USING ITEM 7.
3. ASSEMBLE ITEM 1 OR 10 IN ITEM 2 PER ITEM 8.
4. INSTALL SHIMS 409762-1 THRU -4 ONLY AS REQUIRED TO BRING COMPRESSIVE PRELOAD FORCE TO 300 ± 50 LB.
5. REMOVE POTTING MATERIAL AS NECESSARY TO INSURE LOADING PLATE OF ITEM 2 LOADING AGAINST PRINTED CIRCUIT BOARDS.
6. ITEM 14 TO BE APPLIED TO THREADS OF SCREWS (ITEMS 6 & 7 OF DWG 604815) PRIOR TO FINAL ASSEMBLY





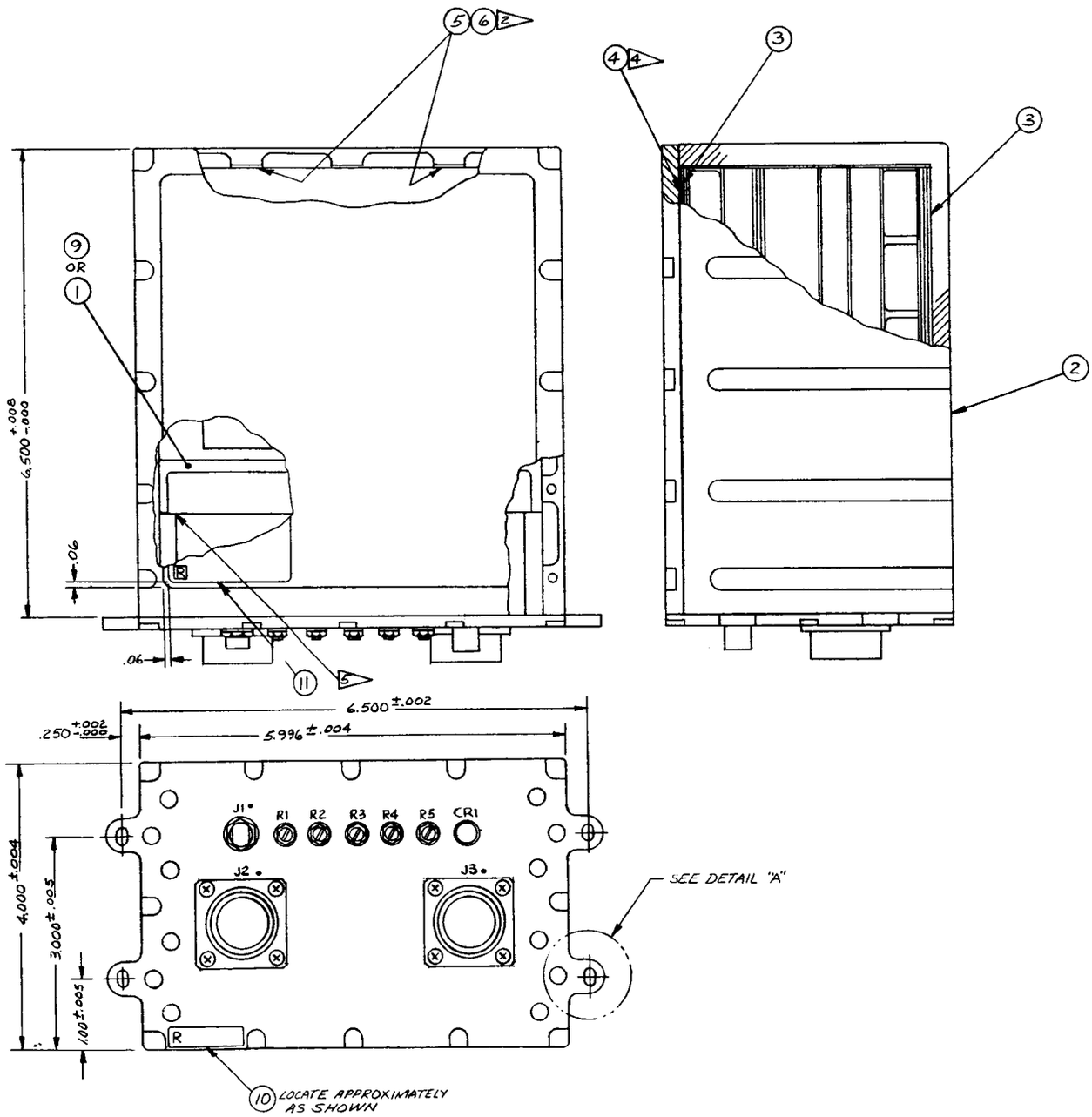
SECTION A-A

	REF	REF	15	606517	DRAWING TREE
1	AR	AR	14	100891-002	SEALANT

	1	1	13	409904-1	PLATE, IDENTIFICATION
	1	1	12	304156-1	PLATE, IDENTIFICATION
	2	2	11	304319-2	SPACER, RUBBER
	1	–	10	605430G2	ELECTRICAL ASSY PCM
	REF	REF	9	513659	BLOCK DIAGRAM
3	REF	REF	8	112664	PROCEDURE, COMPRESSIVE LOADING
2	AR	AR	7	101978-001	ADHESIVE
4	AR	AR	6	409762	SHIM, EPOXY
	2	2	5	304319-1	RUBBER, SPACER
	1	1	4	409053-3	SHIM, SILICONE
	1	1	3	409053-1	SHIM, SILICONE
	1	1	2	604815G1	HOUSING, COMPONENT
	–	1	1	605430G1	ELECTRICAL ASSEMBLY PCM
	G2	G1	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION (CODE IDENT)

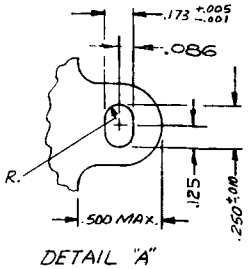
QUANTITY REQUIRED — LIST OF MATERIALS OR PARTS LIST — D605364-B

Figure 1-1. PCM Unit, Assembly Drawing


5 6 Z
4 4
3
3
2
9 R
1
6.500 +.008 -.000
.06
R
.06
11 5
6.500 ±.002
.250 +.002 -.000
5.996 ±.004
J1
R1
R2
R3
R4
R5
CR1
J2
J3
SEE DETAIL "A"
4.000 ±.004
3.000 ±.005
1.00 ±.005
R
10 LOCATE APPROXIMATELY AS SHOWN

NOTES:

1. FOR PROCUREMENT OR PART NUMBER, SEE SPEC OR SOURCE CONTROL DRAWING.
2. BOND ITEM 5 TO ITEM 2 USING ITEM 6
3. ASSEMBLE ITEM 10 OR 9 IN ITEM 2 PER ITEM 7.
4. INSTALL SHIMS 409762-1 THRU -4 ONLY AS REQUIRED TO BRING COMPRESSIVE PRELOAD FORCE TO 300± 50LB.
5. REMOVE POTTING MATERIAL AS NECESSARY TO INSURE LOADING PLATE OF ITEM 2, LOADING AGAINST PRINTED CIRCUIT BOARD.
6. ITEM 12 TO BE APPLIED TO THREADS OF SCREWS (ITEM 7 OF DWG 605732) PRIOR TO FINAL ASSY.

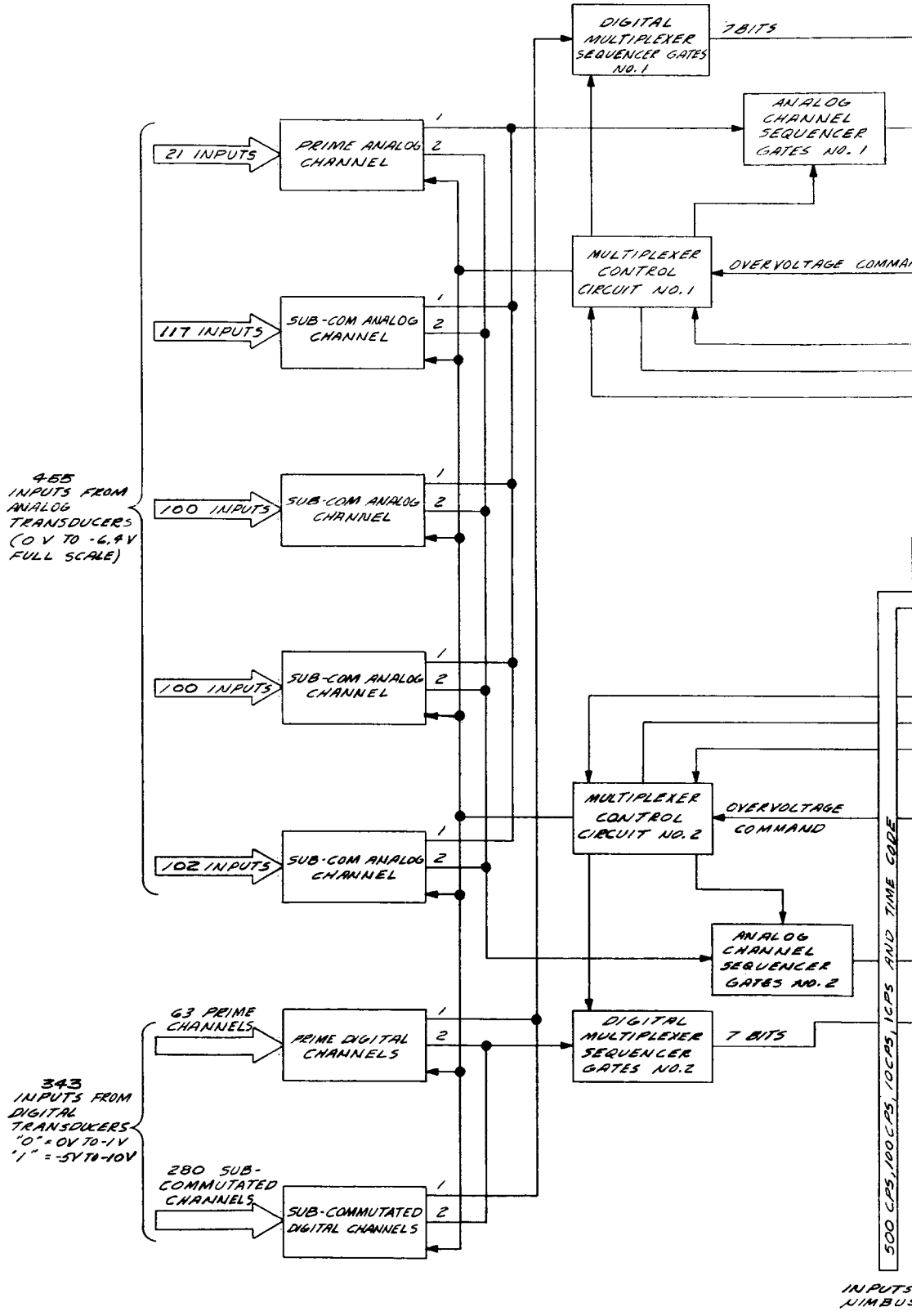


DETAIL "A"
SCALE: 2/1

	G2	G1	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT
	REF	REF	13	516483	DRAWING TREE	
1	AR	AR	12	100891-002	SEALANT	
	1	1	11	409904-2	PLATE IDENTIFICATION	
	1	1	10	304156-1	PLATE IDENTIFICATION	
	1	–	9	514027G2	ELECTRICAL ASSEMBLY TME	
	REF	REF	8	514023	BLOCK, DIAGRAM	
3	REF	REF	7	109347	PROCEDURE, COMPRESSIVE LOADING	
1	AR	AR	6	101978-001	ADHESIVE	
	2	2	5	303881-1	RUBBER, SPACER	
4	AR	AR	4	409762	SHIM, EPOXY	
	2	2	3	409053-1	SHIM, SILICONE	
	1	1	2	605732G1	HOUSING, COMPONENT	
	–	1	1	514027G1	ELECTRICAL ASSEMBLY TME	

LIST OF MATERIALS OR PARTS LIST D513929-B

Figure I-2. TME Unit, Assembly Drawing


DIGITAL MULTIPLEXER SEQUENCER GATES NO. 1
7 BITS
ANALOG CHANNEL SEQUENCER GATES NO. 1
21 INPUTS
PRIME ANALOG CHANNEL
MULTIPLEXER CONTROL CIRCUIT NO. 1
OVERVOLTAGE COMMAN
117 INPUTS
SUB-COM ANALOG CHANNEL
465 INPUTS FROM ANALOG TRANSDUCERS (0 V TO -6.4 V FULL SCALE)
100 INPUTS
SUB-COM ANALOG CHANNEL
100 INPUTS
SUB-COM ANALOG CHANNEL
MULTIPLEXER CONTROL CIRCUIT NO. 2
OVERVOLTAGE COMMAND
102 INPUTS
SUB-COM ANALOG CHANNEL
ANALOG CHANNEL SEQUENCER GATES NO. 2
63 PRIME CHANNELS
PRIME DIGITAL CHANNELS
DIGITAL MULTIPLEXER SEQUENCER GATES NO. 2
7 BITS
343 INPUTS FROM DIGITAL TRANSDUCERS "0" = 0V TO -1V "1" = -5V TO -10V
280 SUB-COMMUTATED CHANNELS
SUB-COMMUTATED DIGITAL CHANNELS
500 CPS, 100 CPS, 10 CPS, 1 CPS AND TIME CODE
INPUTS
NIMBUS

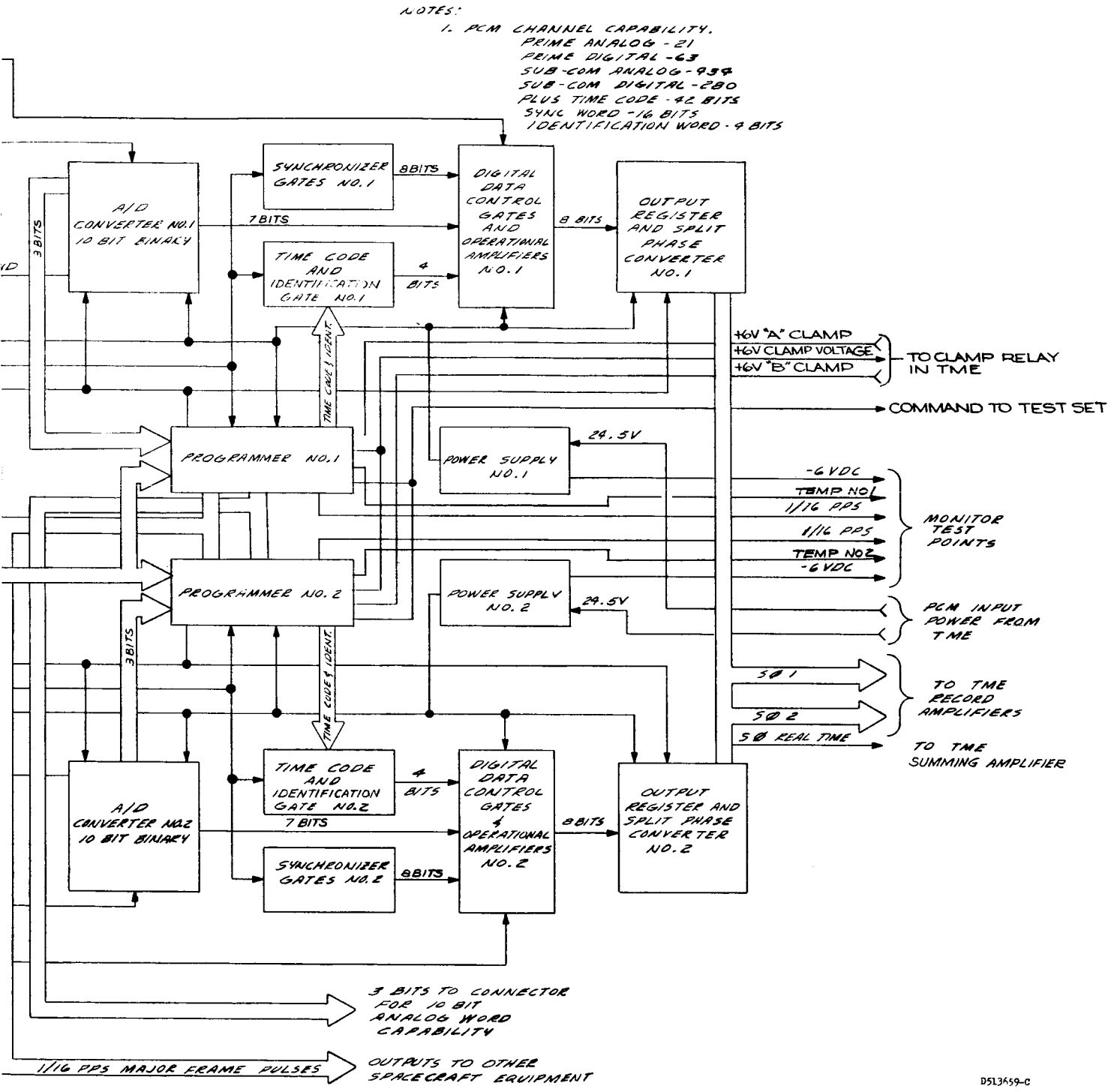
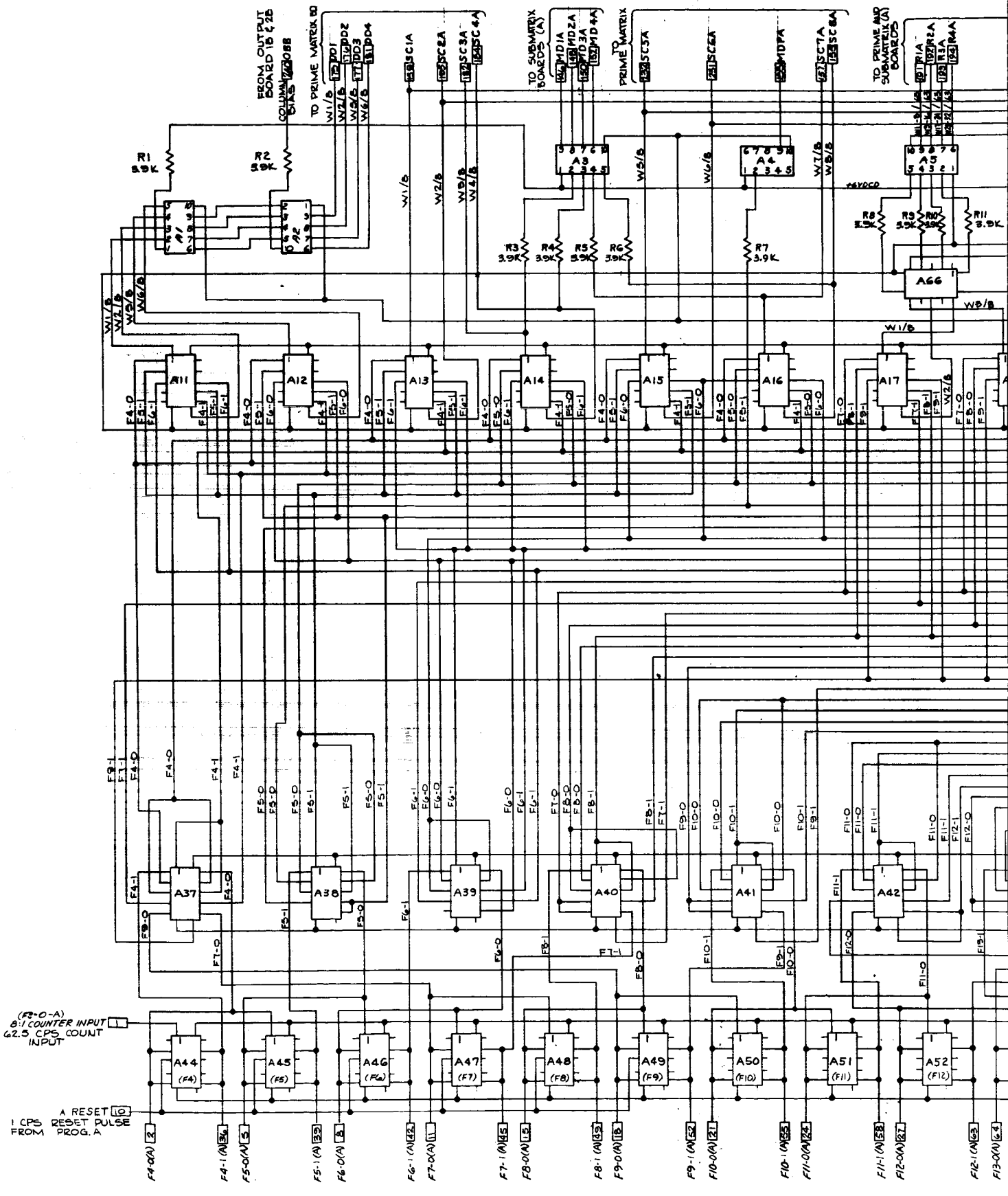
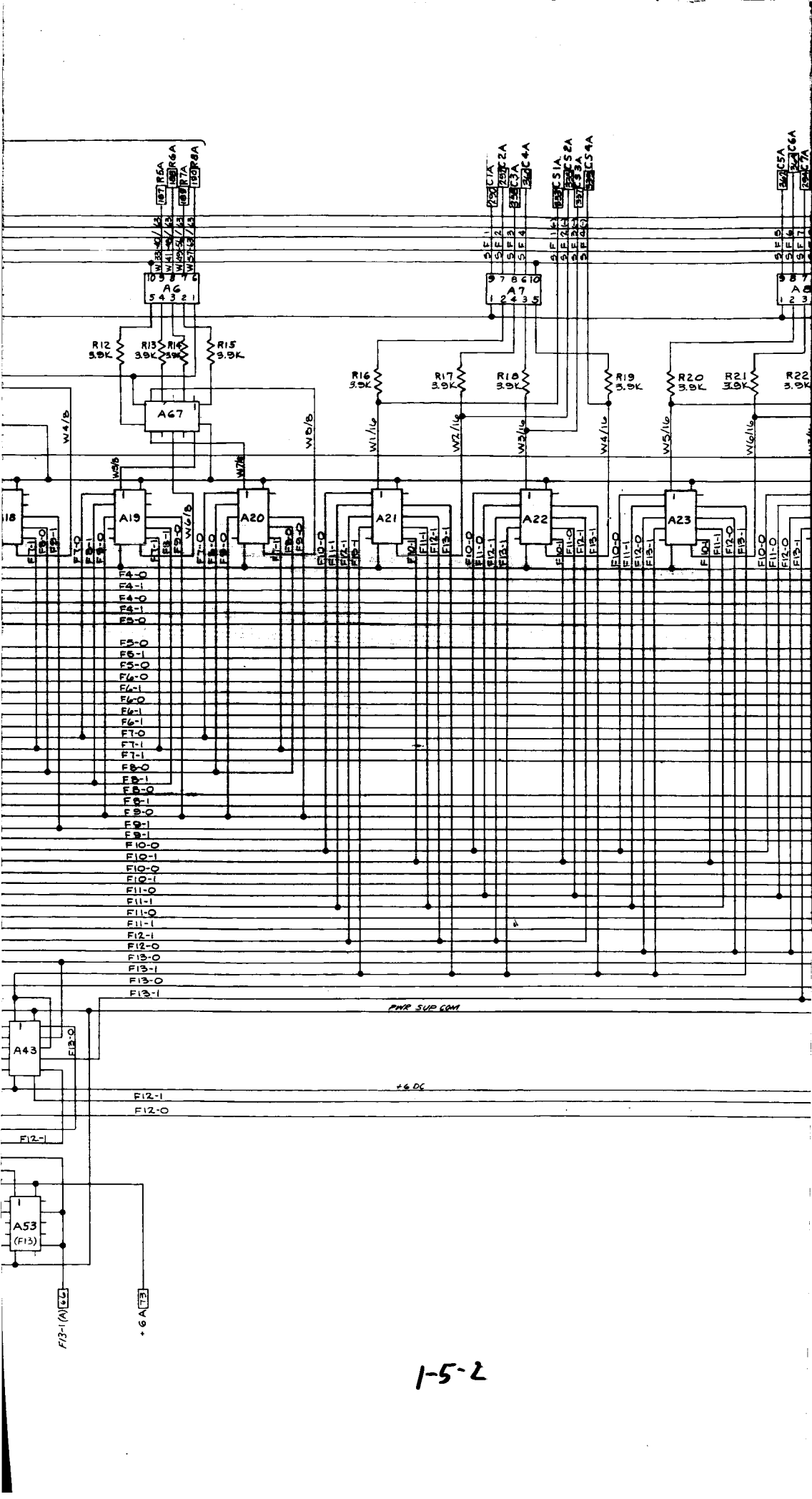
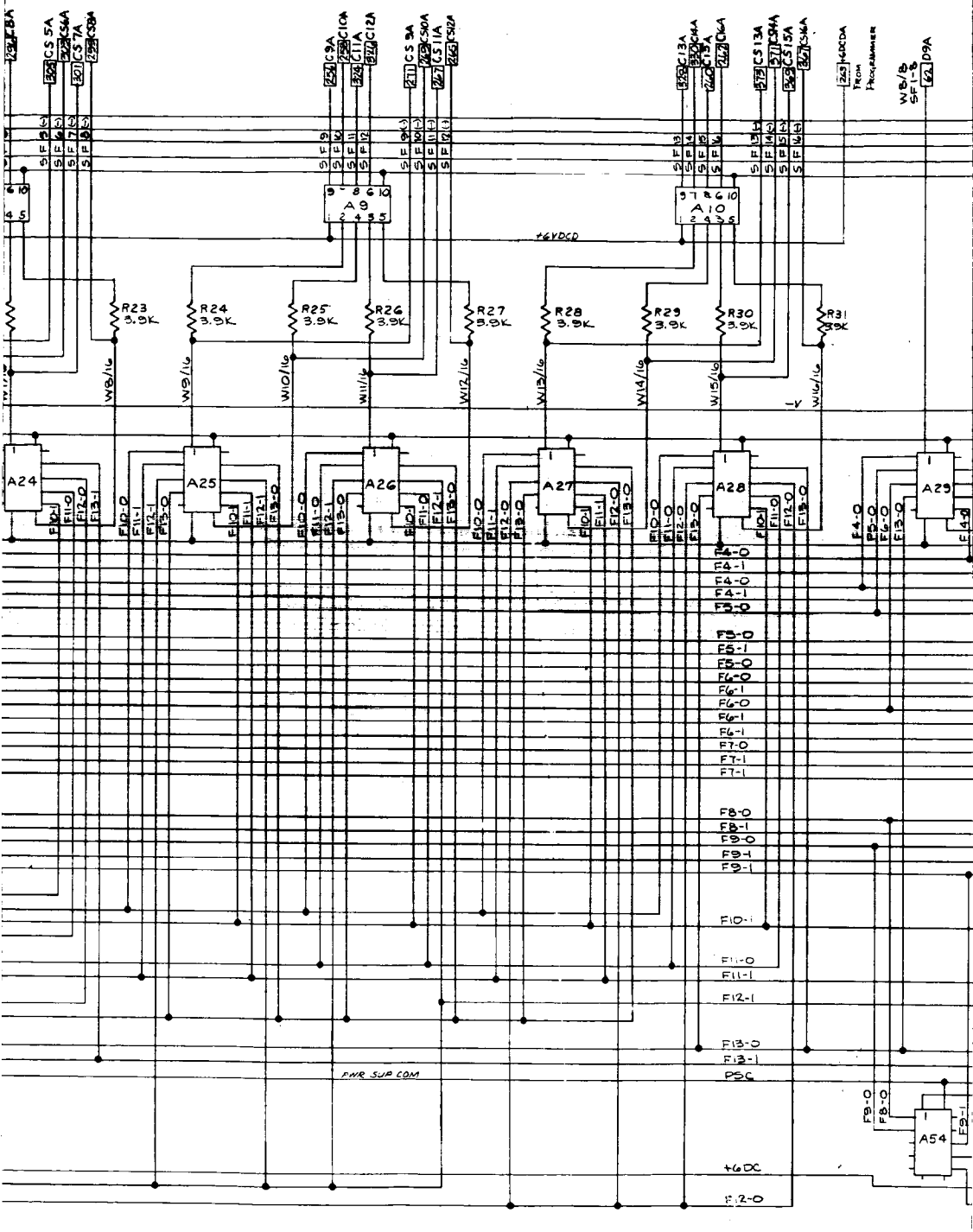


Figure I-3. PCM Unit, Block Diagram


FROM OUTPUT BOARD 1B & 2B
COLUMN BIAS
TO PRIME MATRIX BD
TO SUBMATRIX BOARDS (A)
TO PRIME MATRIX
TO PRIME AND SUBMATRIX (A) BOARDS
R1 3.9K
R2 3.9K
R3 3.9K
R4 3.9K
R5 3.9K
R6 3.9K
R7 3.9K
R8 3.9K
R9 3.9K
R10 3.9K
R11 3.9K
+6VDCD
A1
A2
A3
A4
A5
A66
A11
A12
A13
A14
A15
A16
A17
A37
A38
A39
A40
A41
A42
A44 (F4)
A45 (F5)
A46 (F6)
A47 (F7)
A48 (F8)
A49 (F9)
A50 (F10)
A51 (F11)
A52 (F12)
(F8-0-A) 8:1 COUNTER INPUT 62.5 CPS COUNT INPUT
A RESET
1 CPS RESET PULSE FROM PROG. A


A6
A7
A8
A67
A19
A20
A21
A22
A23
A43
A53
(F13)
R12 3.9K
R13 3.9K
R14 3.9K
R15 3.9K
R16 3.9K
R17 3.9K
R18 3.9K
R19 3.9K
R20 3.9K
R21 3.9K
R22 3.9K
PWR SUP COM
+6 DC
F13-1 (A)
+6 A

1-5-2

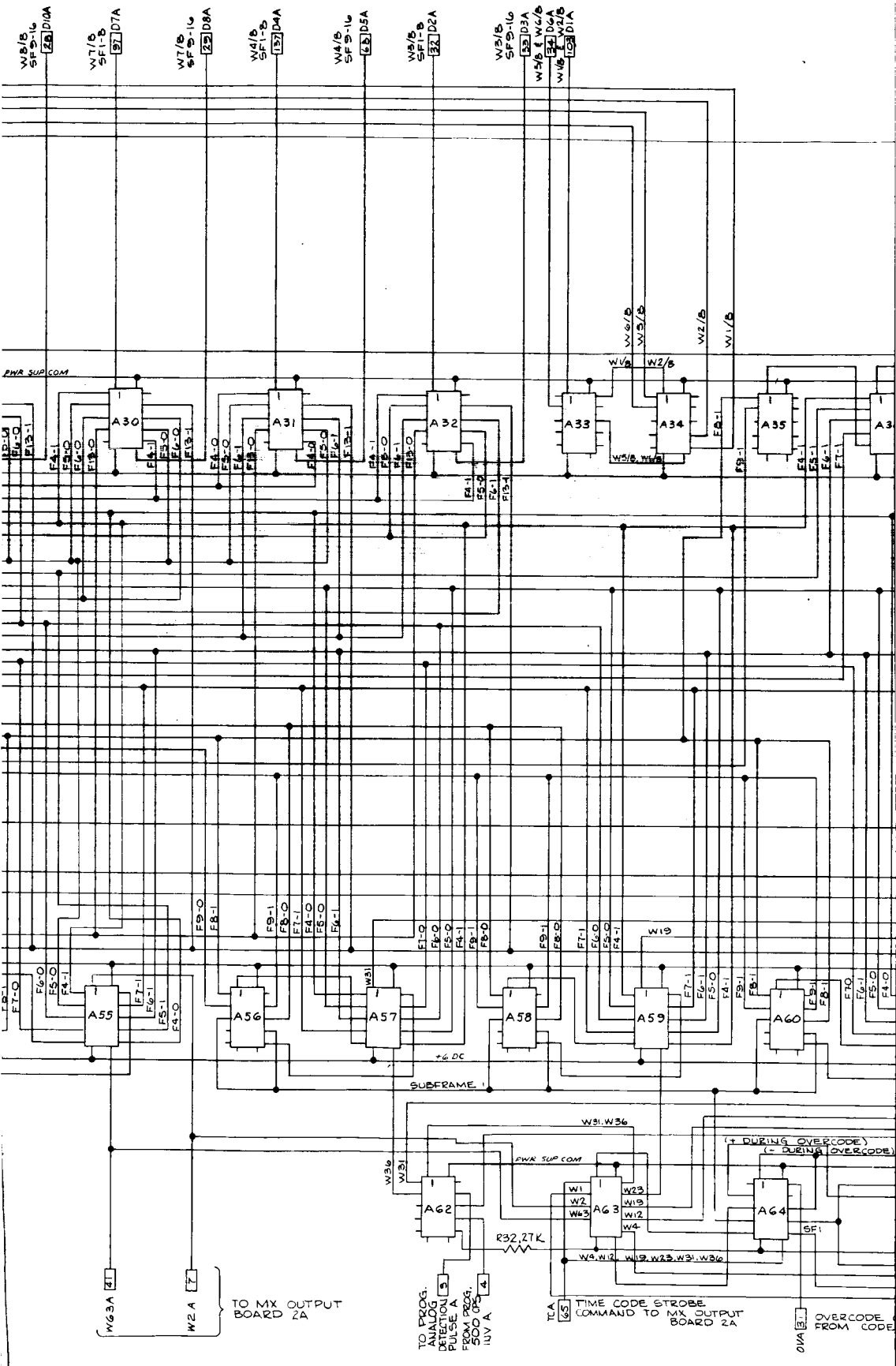


FC 274 FAULT CLAMP 70

239 ANALO A 69

306 ANALOG OUTPUT B 35

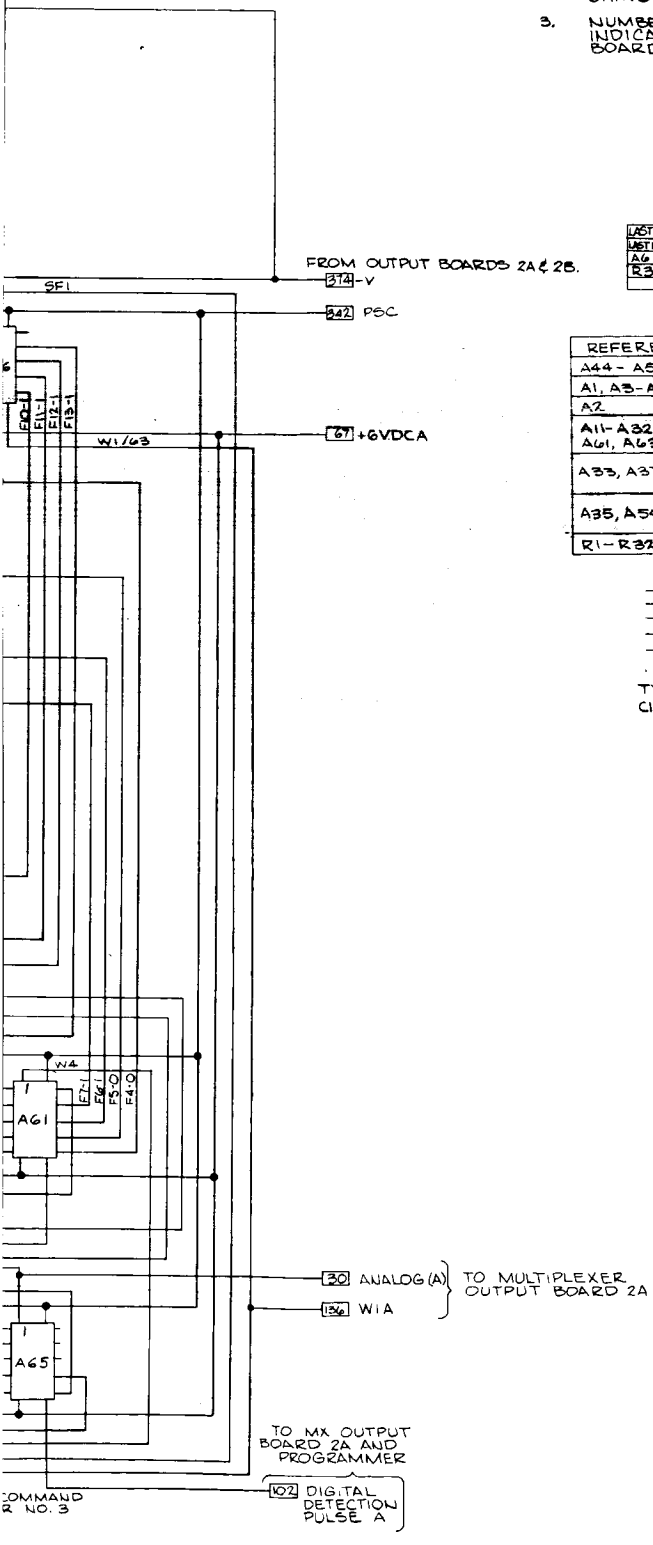
1-5-3



W8/8 SF9-16 28 D10A
W7/8 SF1-8 97 D7A
W7/8 SF9-16 29 D8A
W4/8 SF1-8 137 D4A
W4/8 SF9-16 68 D5A
W3/8 SF1-8 32 D2A
W3/8 SF9-16 33 D3A
W5/8 & W6/8 34 D6A
W1/8 & W2/8 103 D1A
W6/8
W5/8
W2/8
W1/8
PWR SUP COM
A30
A31
A32
A33
A34
A35
A55
A56
A57
A58
A59
A60
A62
A63
A64
W19
W31
+6 DC
SUBFRAME 1
W31, W36
(+ DURING OVERCODE)
(- DURING OVERCODE)
W36
W31
W1
W2
W63
W23
W19
W12
W4
SF1
R32, 27K
W4, W12, W19, W23, W31, W36
W63A 41
W2A 7
TO MX OUTPUT BOARD 2A
TO PROG. ANALOG DETECTION PULSE A 5
FROM PROG. 500 CPS 1UV A 4
TCA 65
TIME CODE STROBE COMMAND TO MX OUTPUT BOARD 2A
OVA 31
OVERCODE FROM CODE

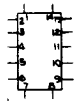
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: PREFIX WITH UNIT NO. OR SUBASSEMBLY DESIGNATION OR BOTH FOR COMPLETE DESIGNATION.
2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS ±5%, ⅛W.
3. NUMBERS IN RECTANGLES INDICATE PRINTED CIRCUIT BOARD TERMINATIONS.



LAST NO. CHART	
LAST NO.	UNUSED
A6	
R32	

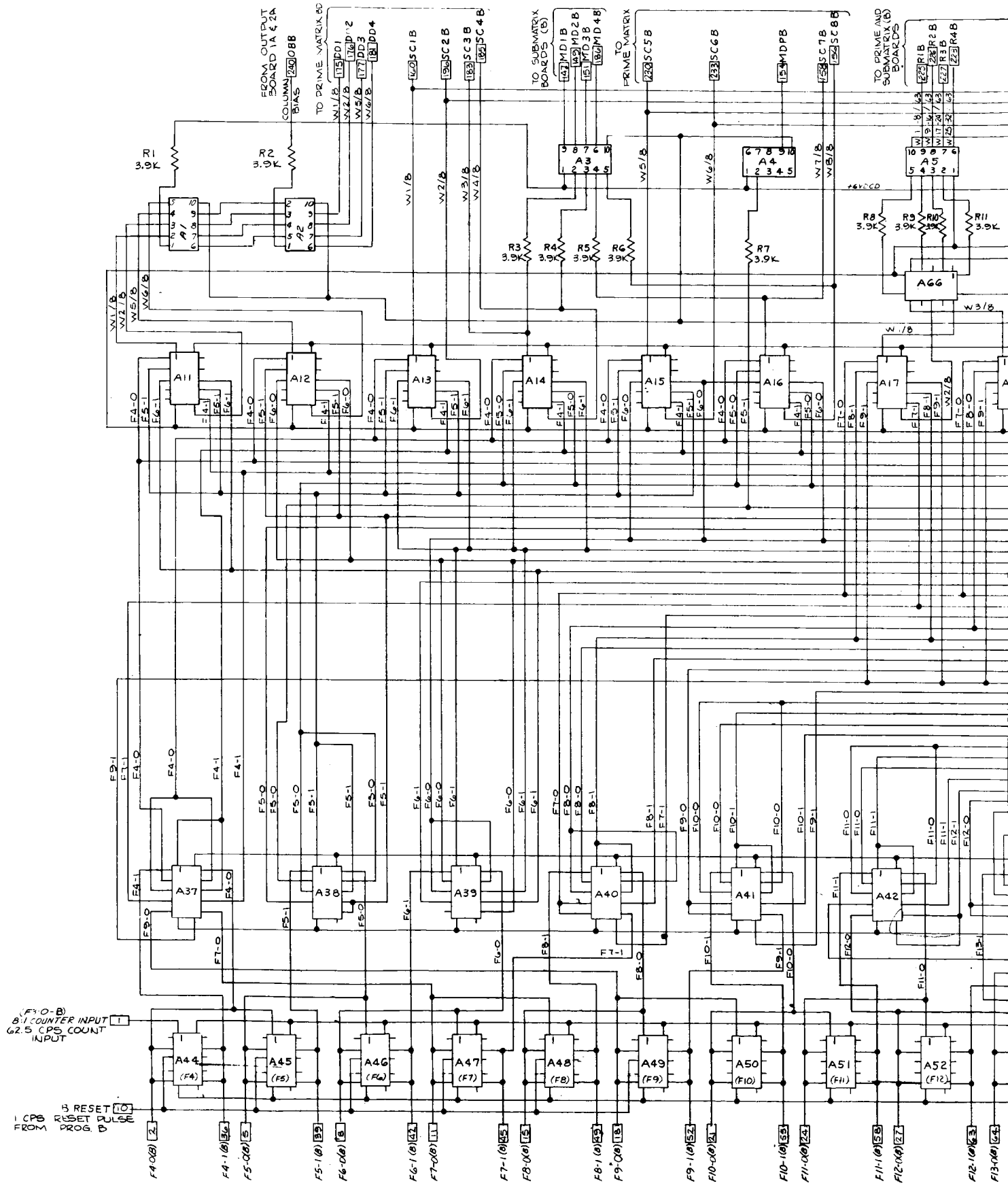
REFERENCE DESIGNATION	PART NO.	TYPE
A44 - A53	110430	MC1133
A1, A3-A10	110261-1	PNP
A2	110260-2	NPN-2
A11-A32, A34, A36, A55, A57, A59, A61, A63, A65	110426	WM261
A33, A37-A43, A64, A66, A67	110425	WM296
A35, A54, A56, A58, A60, A62	110427	WM217
R1-R32	110291	

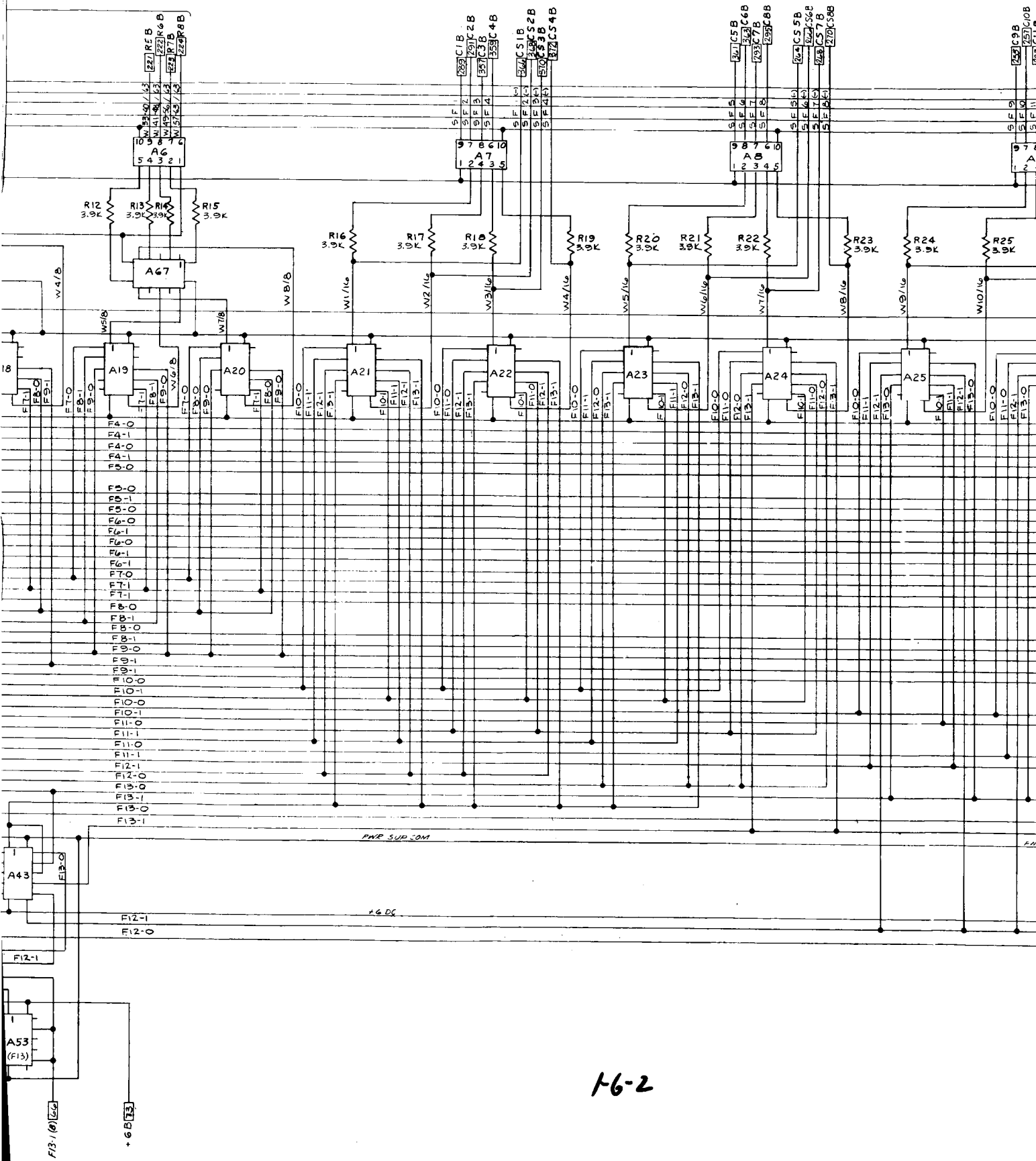


TYP INTEGRATED CIRCUIT NO.

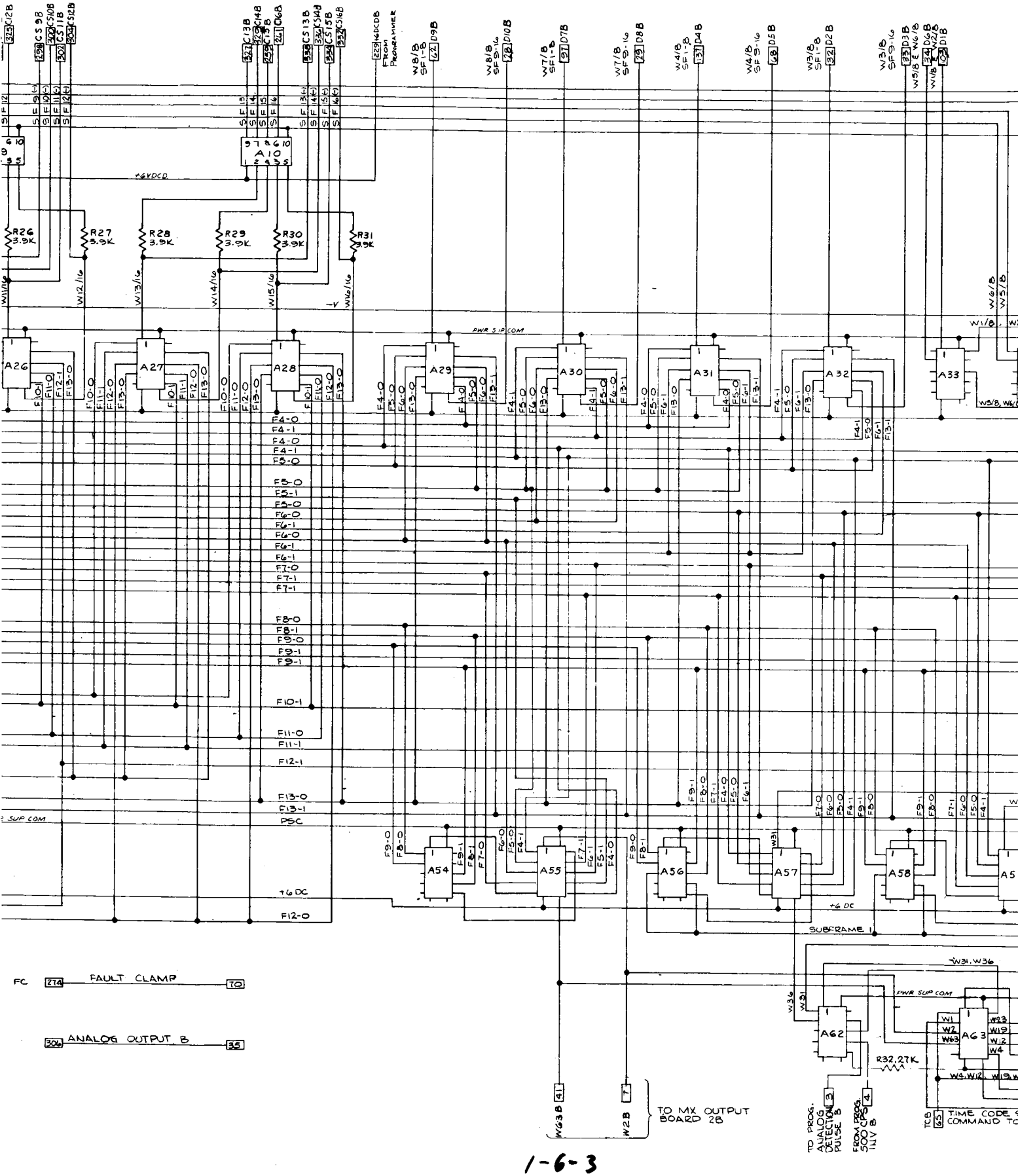
605488

Figure I-4 . Output Board I-A, Schematic Diagram


FROM OUTPUT BOARD 1A & 2A
COLUMN BIAS
TO PRIME MATRIX BD
TO SUBMATRIX BOARDS (B)
TO PRIME MATRIX
TO PRIME AND SUBMATRIX (B) BOARDS
R1 3.9K
R2 3.9K
R3 3.9K
R4 3.9K
R5 3.9K
R6 3.9K
R7 3.9K
R8 3.9K
R9 3.9K
R10 3.9K
R11 3.9K
A1
A2
A3
A4
A5
A66
A11
A12
A13
A14
A15
A16
A17
A37
A38
A39
A40
A41
A42
A44 (F4)
A45 (F5)
A46 (F6)
A47 (F7)
A48 (F8)
A49 (F9)
A50 (F10)
A51 (F11)
A52 (F12)
(F3-0-B) 8:1 COUNTER INPUT 62.5 CPS COUNT INPUT
B RESET 1 CPS RESET PULSE FROM PROG. B


A6
A7
A8
A67
A19
A20
A21
A22
A23
A24
A25
A43
A53
(F13)
R12 3.9K
R13 3.9K
R14 3.9K
R15 3.9K
R16 3.9K
R17 3.9K
R18 3.9K
R19 3.9K
R20 3.9K
R21 3.9K
R22 3.9K
R23 3.9K
R24 3.9K
R25 3.9K
PWR SUP COM
+6 DC
F13-1 (8)
+6B

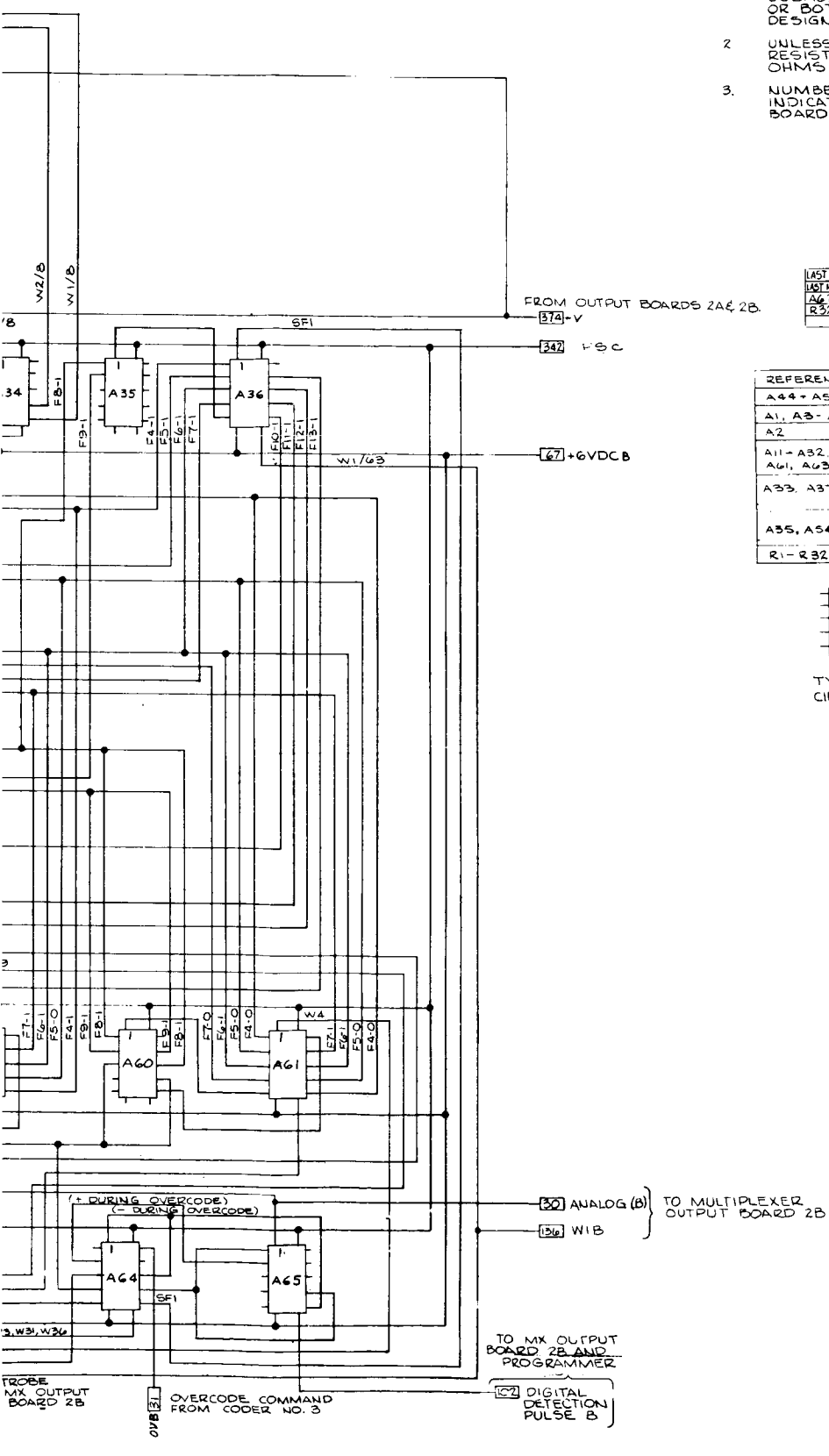
1-6-2



FC 274 FAULT CLAMP 70
306 ANALOG OUTPUT B 35
TO MX OUTPUT BOARD 2B
TO PROG. ANALOG DETECTION PULSE B
FROM PROG. 500 CPS INV B
TIME CODE
COMMAND
SUBFRAME 1
PWR SUP COM
+6VDCD
+6 DC
PSC

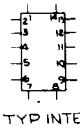
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: PREFIX WITH UNIT NO. OR SUBASSEMBLY DESIGNATION OR BOTH FOR COMPLETE DESIGNATION.
2. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS ± 5%, ⅛ W.
3. NUMBERS IN RECTANGLES INDICATE PRINTED CIRCUIT BOARD TERMINATIONS.



LAST NO. CHART	
LAST NO.	UNUSED
A67	
R32	

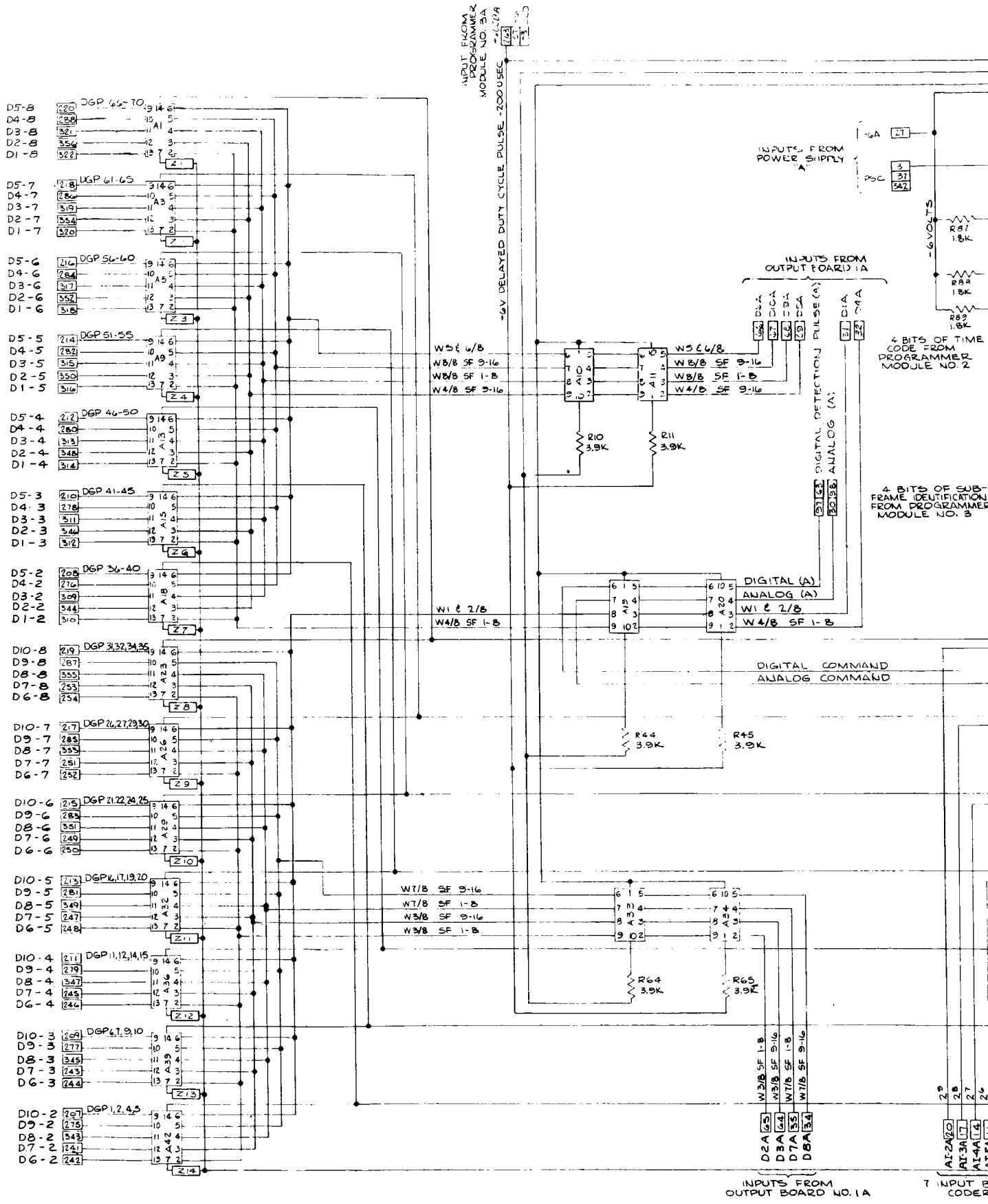
REFERENCE DESIGNATION	PART NO.	TYPE
A44 - A53	110430	MC1133
A1, A3 - A10	110261-1	PNP
A2	110260-2	NPN-2
A11 - A32, A34, A36, A55, A57, A59, A61, A63, A65	110426	WM261
A33, A37 - A43, A64, A66, A67	110425	WM236
A35, A54, A56, A58, A60, A62	110427	WM217
R1 - R32	110291	

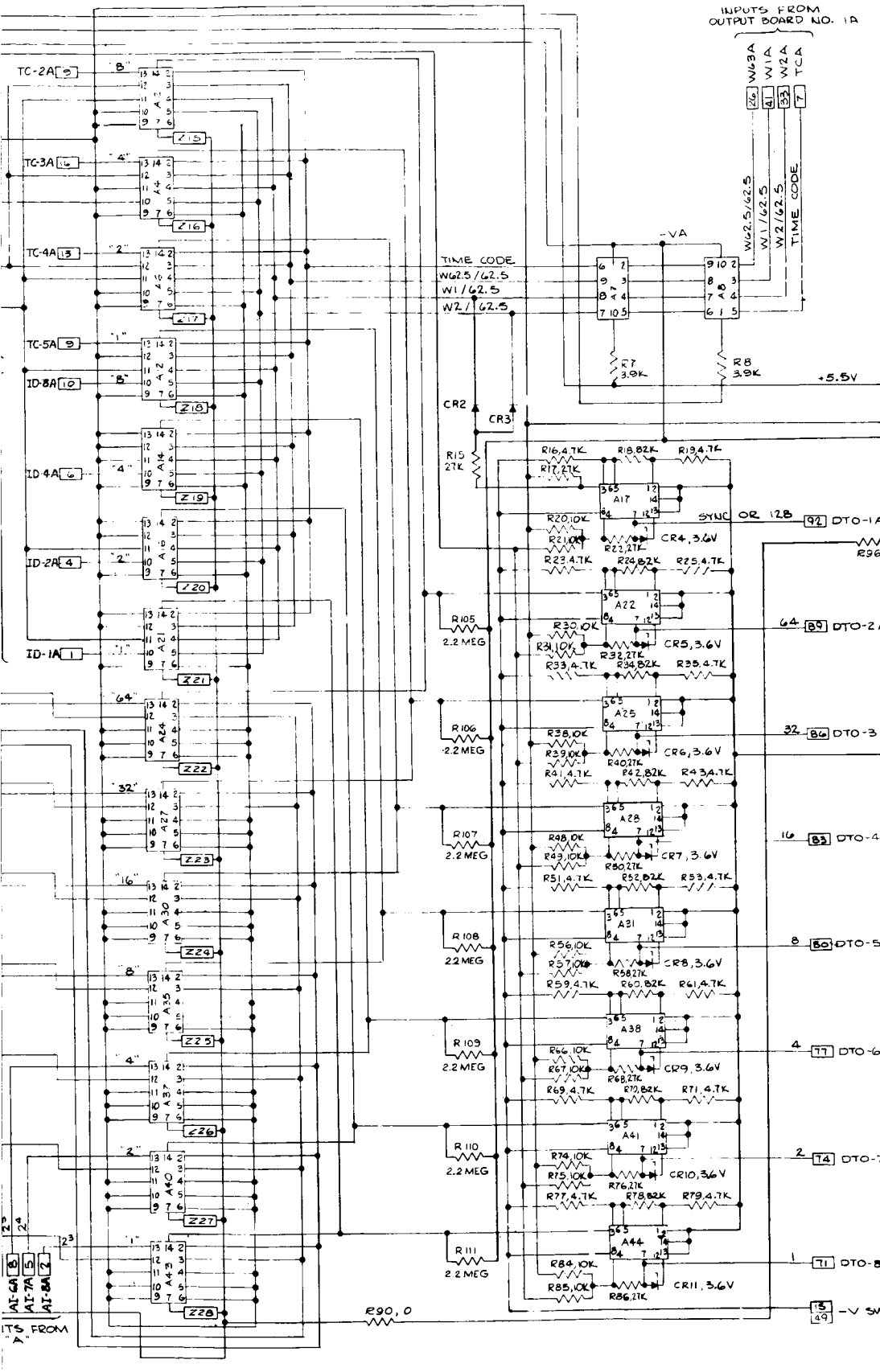


TYP INTEGRATED CIRCUIT NO.

605439

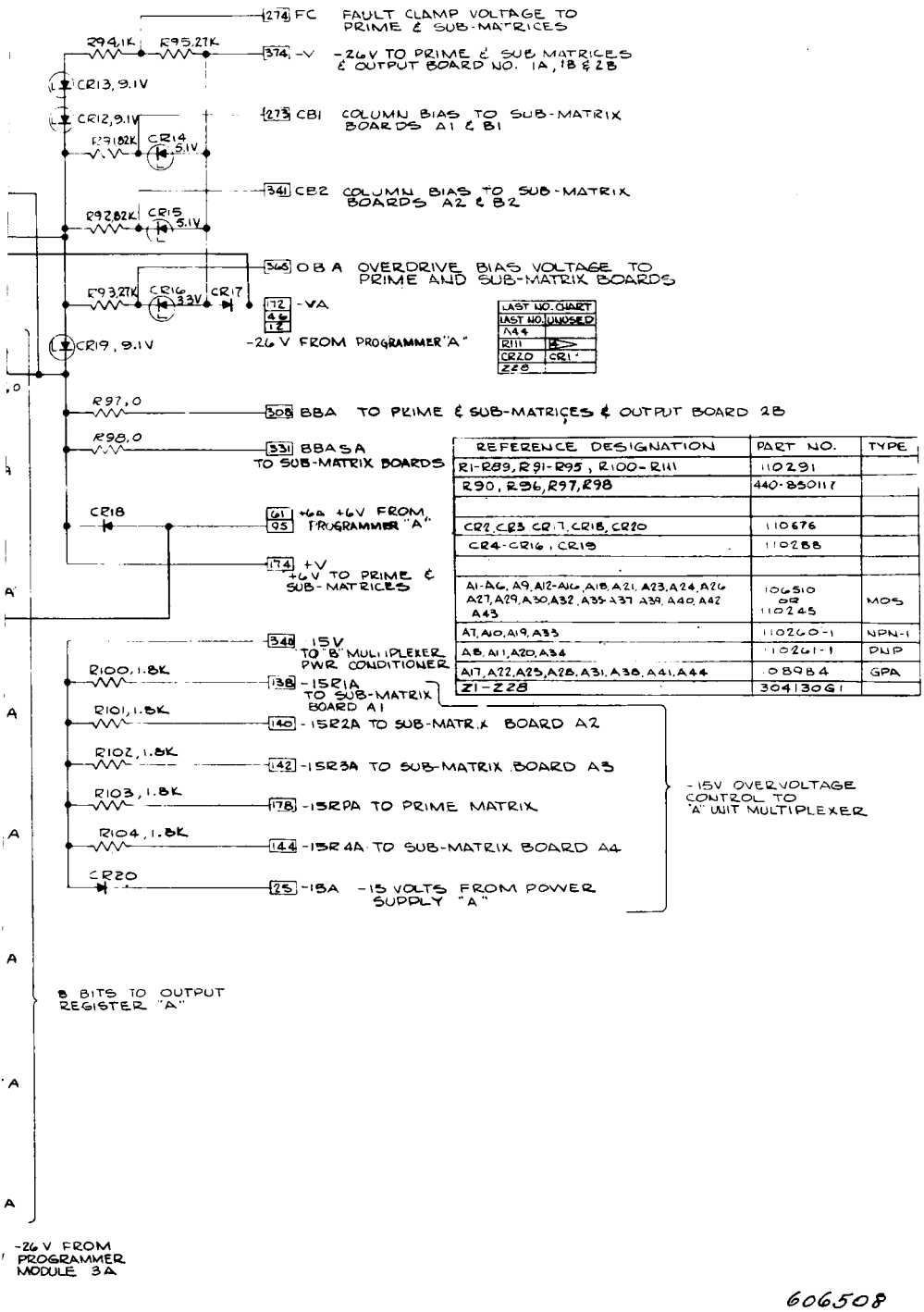
Figure 1-5 . Output Board 1-B, Schematic Diagram


INPUT FROM PROGRAMMER MODULE NO. 3A
-6V DELAYED DUTY CYCLE PULSE -200 USEC
INPUTS FROM POWER SUPPLY "A"
-6A
PSC
-6 VOLTS
R87 1.8K
R88 1.8K
R89 1.8K
INPUTS FROM OUTPUT BOARD 1A
DIGITAL DETECTION PULSE (A)
ANALOG (A)
4 BITS OF TIME CODE FROM PROGRAMMER MODULE NO. 2
4 BITS OF SUB-FRAME IDENTIFICATION FROM PROGRAMMER MODULE NO. 3
DIGITAL (A)
ANALOG (A)
W1 & 2/8
W4/8 SF 1-8
DIGITAL COMMAND
ANALOG COMMAND
R10 3.9K
R11 3.9K
R44 3.9K
R45 3.9K
R64 3.9K
R65 3.9K
W5 & 6/8
W8/8 SF 9-16
W8/8 SF 1-8
W4/8 SF 9-16
W7/8 SF 9-16
W7/8 SF 1-8
W3/8 SF 9-16
W3/8 SF 1-8
D2A
D3A
D7A
D8A
INPUTS FROM OUTPUT BOARD NO. 1A
AI-2A
AI-3A
AI-4A
7 INPUT B
CODER
DGP 66-70
DGP 61-65
DGP 56-60
DGP 51-55
DGP 46-50
DGP 41-45
DGP 36-40
DGP 31,32,34,35
DGP 26,27,29,30
DGP 21,22,24,25
DGP 16,17,19,20
DGP 11,12,14,15
DGP 6,7,9,10
DGP 1,2,4,5


INPUTS FROM OUTPUT BOARD NO. 1A
W1-3A
W1A
W2A
TCA
W62.5/62.5
W1/62.5
W2/62.5
TIME CODE
-VA
+5.5V
TC-2A
TC-3A
TC-4A
TC-5A
ID-8A
ID-4A
ID-2A
ID-1A
CR2
CR3
R7 3.9K
R8 3.9K
R15 27K
R105 2.2 MEG
R106 2.2 MEG
R107 2.2 MEG
R108 2.2 MEG
R109 2.2 MEG
R110 2.2 MEG
R111 2.2 MEG
SYNC OR 128
DTO-1A
DTO-2A
DTO-3
DTO-4
DTO-5
DTO-6
DTO-7
DTO-8
-V SW
R90, 0
AI-6A
AI-7A
AI-8A

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: PREFIX WITH UNIT NO. OR SUBASSEMBLY DESIGNATION OR BOTH FOR COMPLETE DESIGNATION.
2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS ±5% TOL., ¼ W., CAPACITANCE IN PF ±10%, 100V., DIODES ARE TI-251.
3. NUMBERS IN RECTANGLES INDICATE PRINTED CIRCUIT BOARD TERMINATIONS.
4. FOLLOWING RES NO NOT USED-R39, R1, R3, R5, R9, R13, R26, R28, R36, R46, R54, R62, R72, R80, R82, R2, R4, R6, R12, R14, R27, R29, R37, R47, R55, R63, R73, R81, R83



LAST NO. CHART	
LAST NO.	UNUSED
A44	
R111	
CR20	CR1
Z28	

REFERENCE DESIGNATION	PART NO.	TYPE
R1-R89, R91-R95, R100-R111	110291	
R90, R96, R97, R98	440-850117	
CR2, CR3, CR17, CR18, CR20	110676	
CR4-CR16, CR19	110288	
A1-A6, A9, A12-A16, A18, A21, A23, A24, A26, A27, A29, A30, A32, A35-A37, A39, A40, A42, A43	106510 OR 110245	MOS
A7, A10, A19, A33	110260-1	NPN-1
A8, A11, A20, A34	110261-1	PNP
A17, A22, A25, A28, A31, A38, A41, A44	08984	GPA
Z1-Z28	304130G1	

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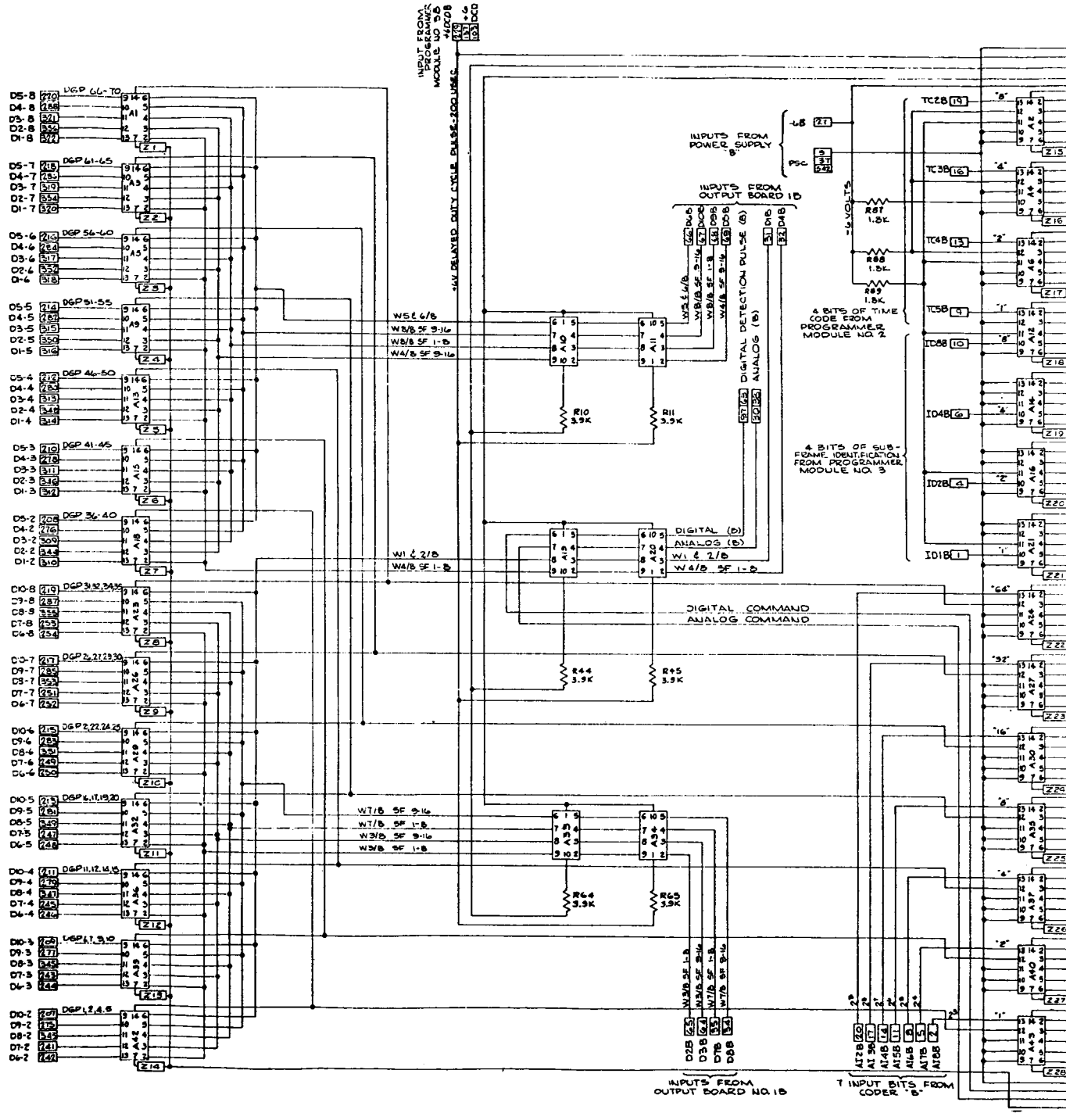
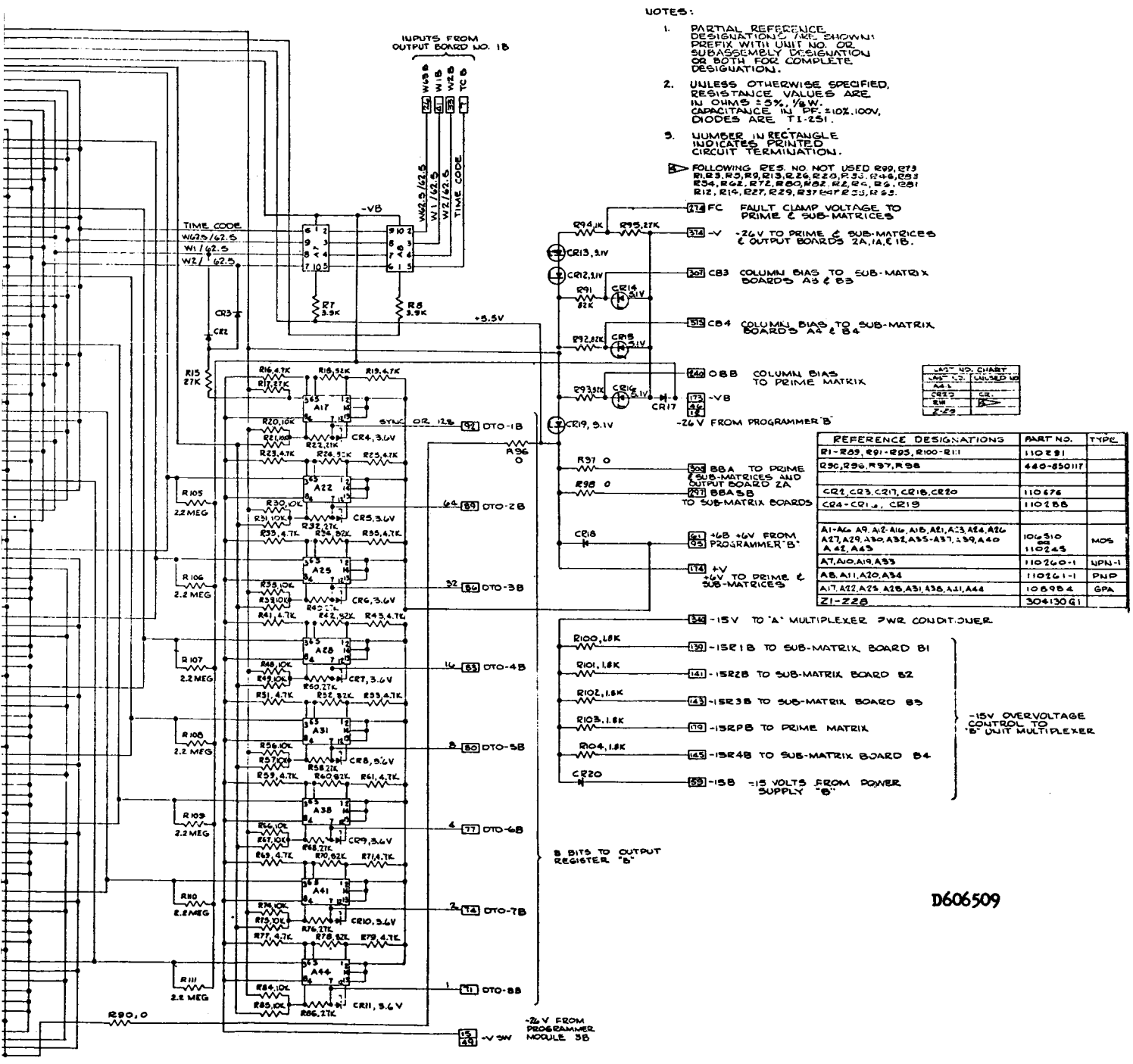
Figure 1-6 . Output board 11-A, Schematic Diagram

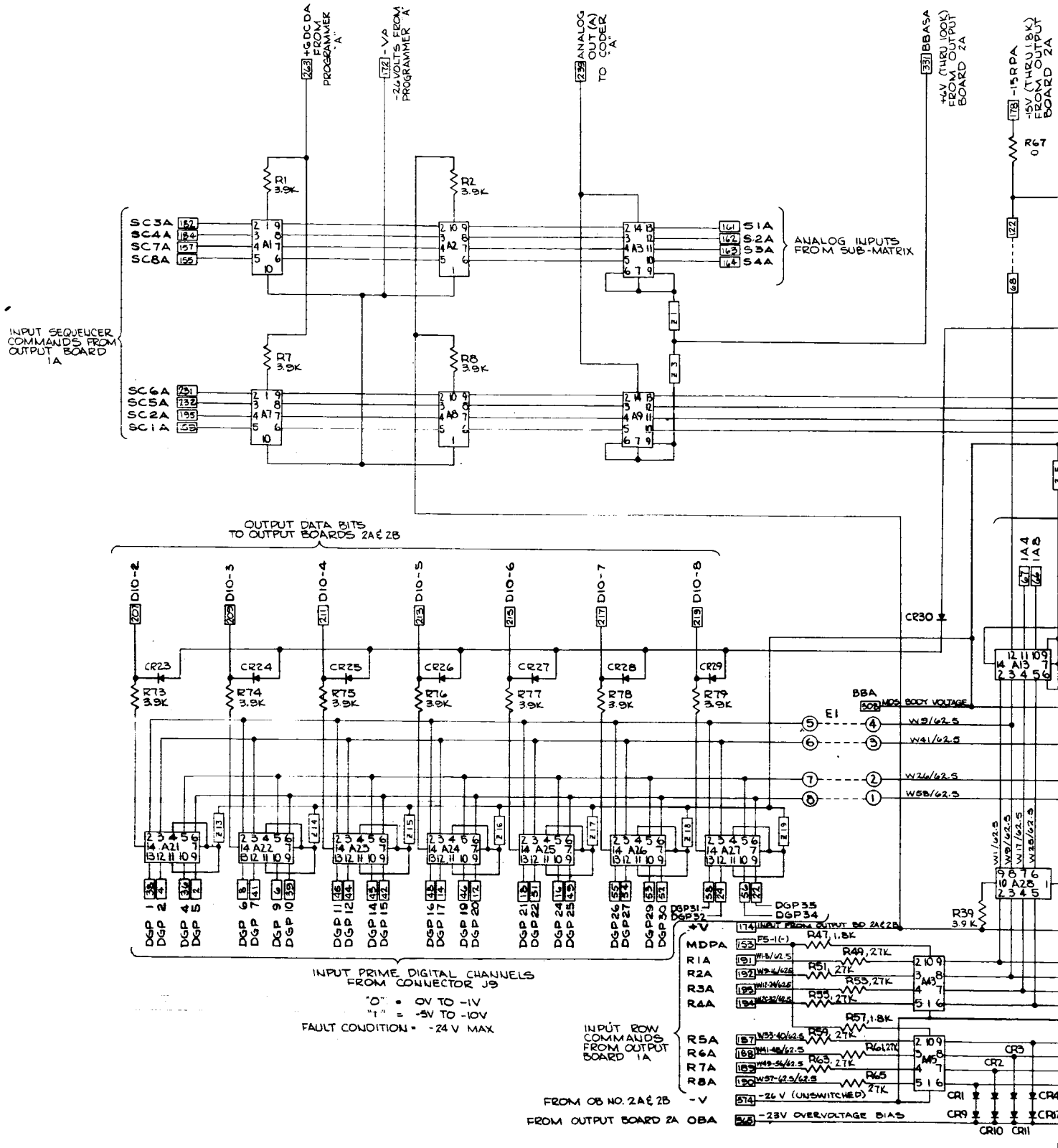

INPUT FROM PROGRAMMER MODULE NO 3B
+6V DELAYED DUTY CYCLE PULSE-200 USEC.
INPUTS FROM POWER SUPPLY "B"
INPUTS FROM OUTPUT BOARD 1B
DIGITAL DETECTION PULSE (B)
ANALOG (B)
DIGITAL (B)
ANALOG (B)
DIGITAL COMMAND
ANALOG COMMAND
4 BITS OF TIME CODE FROM PROGRAMMER MODULE NO 2
4 BITS OF SUB-FRAME IDENTIFICATION FROM PROGRAMMER MODULE NO 3
INPUTS FROM OUTPUT BOARD NO 1B
T INPUT BITS FROM CODER "B"

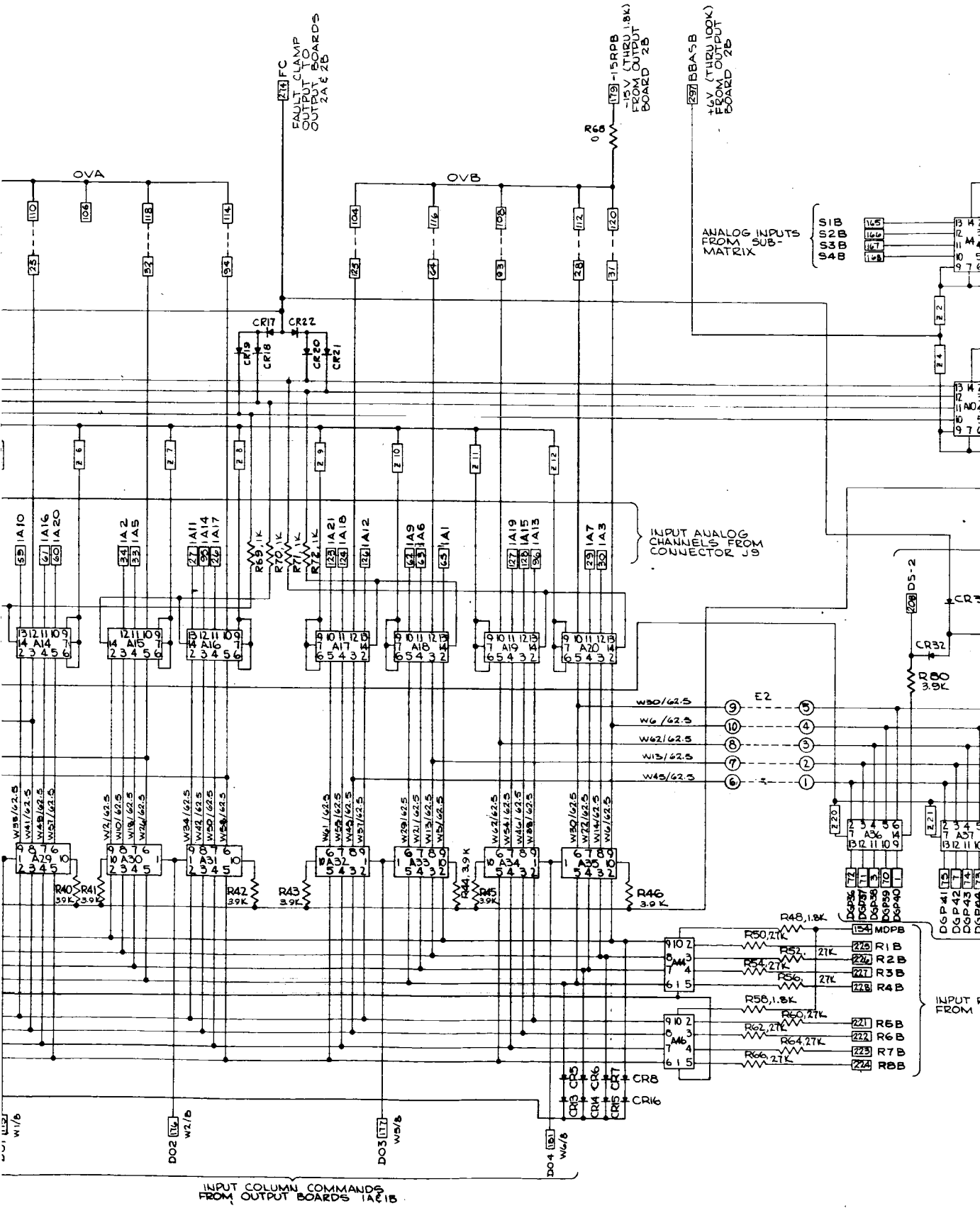
1-8-1

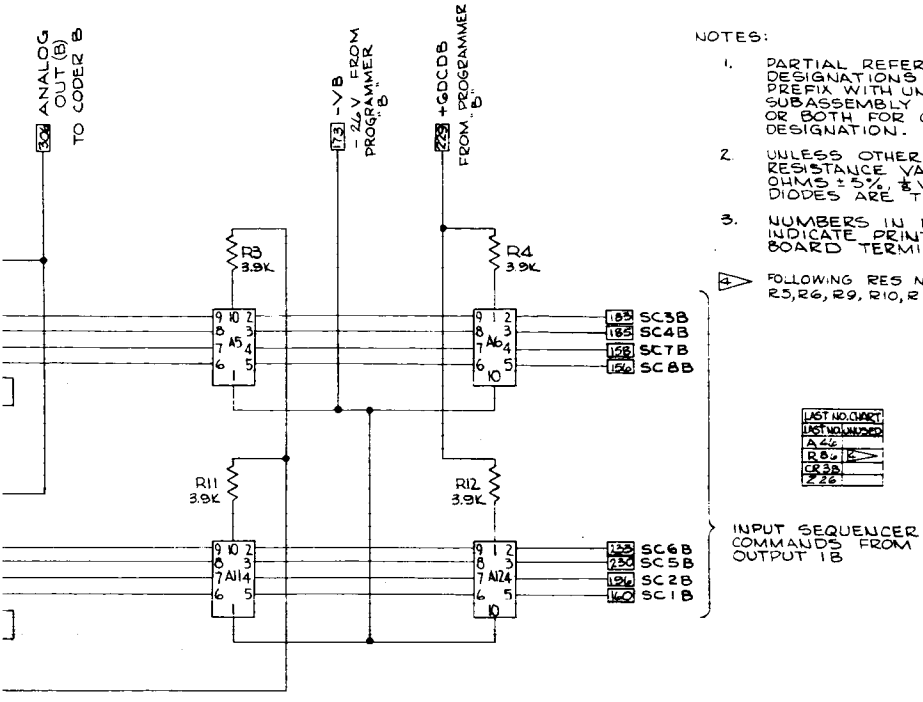


REFERENCE DESIGNATIONS	PART NO.	TYPE
R1-R89, R91-R95, R100-R111	110291	
R90, R96, R97, R98	440-850117	
CR2, CR3, CR17, CR18, CR20	110676	
CR4-CR16, CR19	110288	
A1-A6, A9, A12-A16, A18, A21, A23, A24, A26, A27, A29, A30, A32, A35-A37, A39, A40, A42, A43	106510 or 110245	MOS
A7, A10, A19, A33	110260-1	UPN-1
A8, A11, A20, A34	110261-1	PNP
A17, A22, A25, A28, A31, A38, A41, A44	108984	GPA
Z1-Z28	304130G1	

Figure 1-7. Output Board 11-B, Schematic Diagram


+6DCDA FROM PROGRAMMER "A"
-VA -26 VOLTS FROM PROGRAMMER "A"
ANALOG OUT (A) TO CODER "A"
BBASA
+6V (THRU 100K) FROM OUTPUT BOARD 2A
-15RPA -15V (THRU 1.8K) FROM OUTPUT BOARD 2A
R67 0
R1 3.9K
R2 3.9K
R7 3.9K
R8 3.9K
SC3A
SC4A
SC7A
SC8A
SC6A
SC5A
SC2A
SC1A
S1A
S2A
S3A
S4A
ANALOG INPUTS FROM SUB-MATRIX
INPUT SEQUEUCER COMMANDS FROM OUTPUT BOARD 1A
OUTPUT DATA BITS TO OUTPUT BOARDS 2A & 2B
DIO-2
DIO-3
DIO-4
DIO-5
DIO-6
DIO-7
DIO-8
CR23
CR24
CR25
CR26
CR27
CR28
CR29
R73 3.9K
R74 3.9K
R75 3.9K
R76 3.9K
R77 3.9K
R78 3.9K
R79 3.9K
CR30
BBA
MDS BODY VOLTAGE
E1
W19/62.5
W41/62.5
W26/62.5
W58/62.5
W1/62.5
W9/62.5
W17/62.5
W25/62.5
DGP35
DGP34
DGP31
DGP32
R39 3.9K
INPUT PRIME DIGITAL CHANNELS FROM CONNECTOR J9
"0" = 0V TO -1V
"1" = -5V TO -10V
FAULT CONDITION = -24 V MAX
+V
MDPA
R1A
R2A
R3A
R4A
R5A
R6A
R7A
R8A
INPUT FROM OUTPUT BD 2A&2B
R47, 1.8K
R49, 27K
R51, 27K
R53, 27K
R55, 27K
R57, 1.8K
R59, 27K
R61, 27K
R63, 27K
R65, 27K
INPUT ROW COMMANDS FROM OUTPUT BOARD 1A
FROM OB NO. 2A & 2B -V
-26 V (UNSWITCHED)
FROM OUTPUT BOARD 2A OBA
-23V OVERVOLTAGE BIAS
CR1
CR2
CR3
CR4
CR9
CR10
CR11
CR12

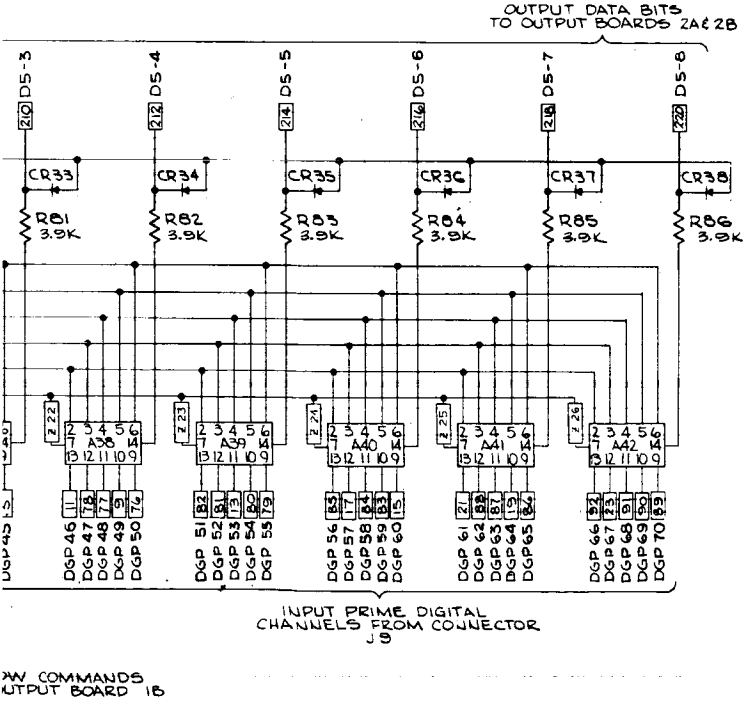

FAULT CLAMP OUTPUT TO OUTPUT BOARDS 2A & 2B
-15RPB -15V (THRU 1.8K) FROM OUTPUT BOARD 2B
BBA-5B +6V (THRU 100K) FROM OUTPUT BOARD 2B
OVA
OVB
ANALOG INPUTS FROM SUB-MATRIX
S1B
S2B
S3B
S4B
INPUT ANALOG CHANNELS FROM CONNECTOR J9
INPUT FROM
INPUT COLUMN COMMANDS FROM OUTPUT BOARDS 1A & 1B



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: PREFIX WITH UNIT NO. OR SUBASSEMBLY DESIGNATION OR BOTH FOR COMPLETE DESIGNATION.
2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS ± 5%, ½ W. DIODES ARE TI-251.
3. NUMBERS IN RECTANGLES INDICATE PRINTED CIRCUIT BOARD TERMINATIONS.
4. FOLLOWING RES NO. NOT USED R5, R6, R9, R10, R13 THRU R38

LAST NO. CHART	
LAST NO. UNUSED	
A46	
R86	4
CR38	
Z26	



REFERENCE DESIGNATION	PART NO.	TYPE
R67, R68	440-850117	
R1-R4, R7, R8, R11, R12, R39-R66, R87-R86	110291	
CR1-CR38	110676	
A3, A4, A9, A10, A13-A27, A36-A42	106510 OR 110245	MOS
A1, A6, A7, A12	110261-	PNP
A2, A5, A8, A11, A28-A35	110260-1	NPN-1
A43-A46	110260-2	NPN-2
Z THRU Z-26	304130G1	

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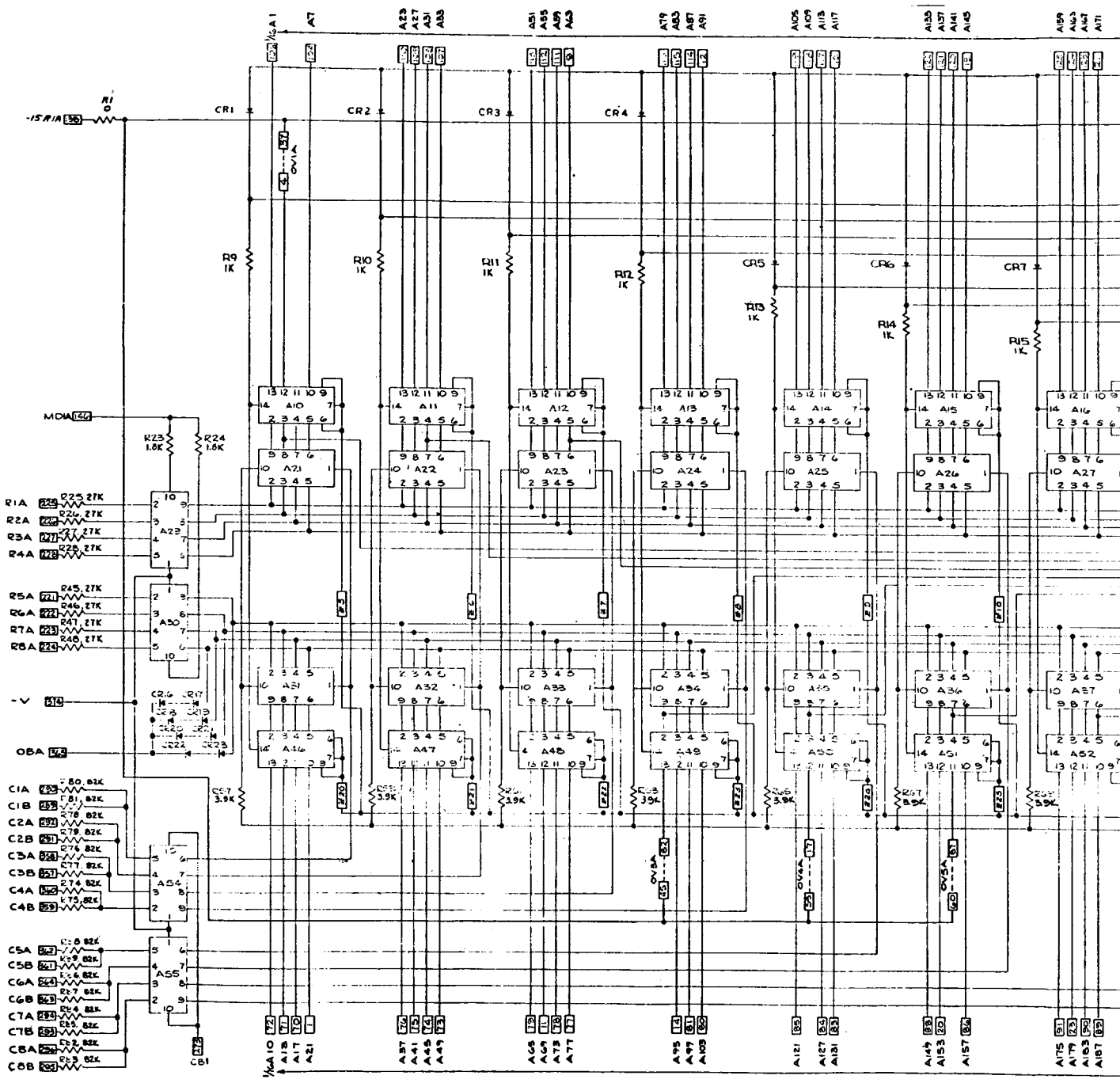
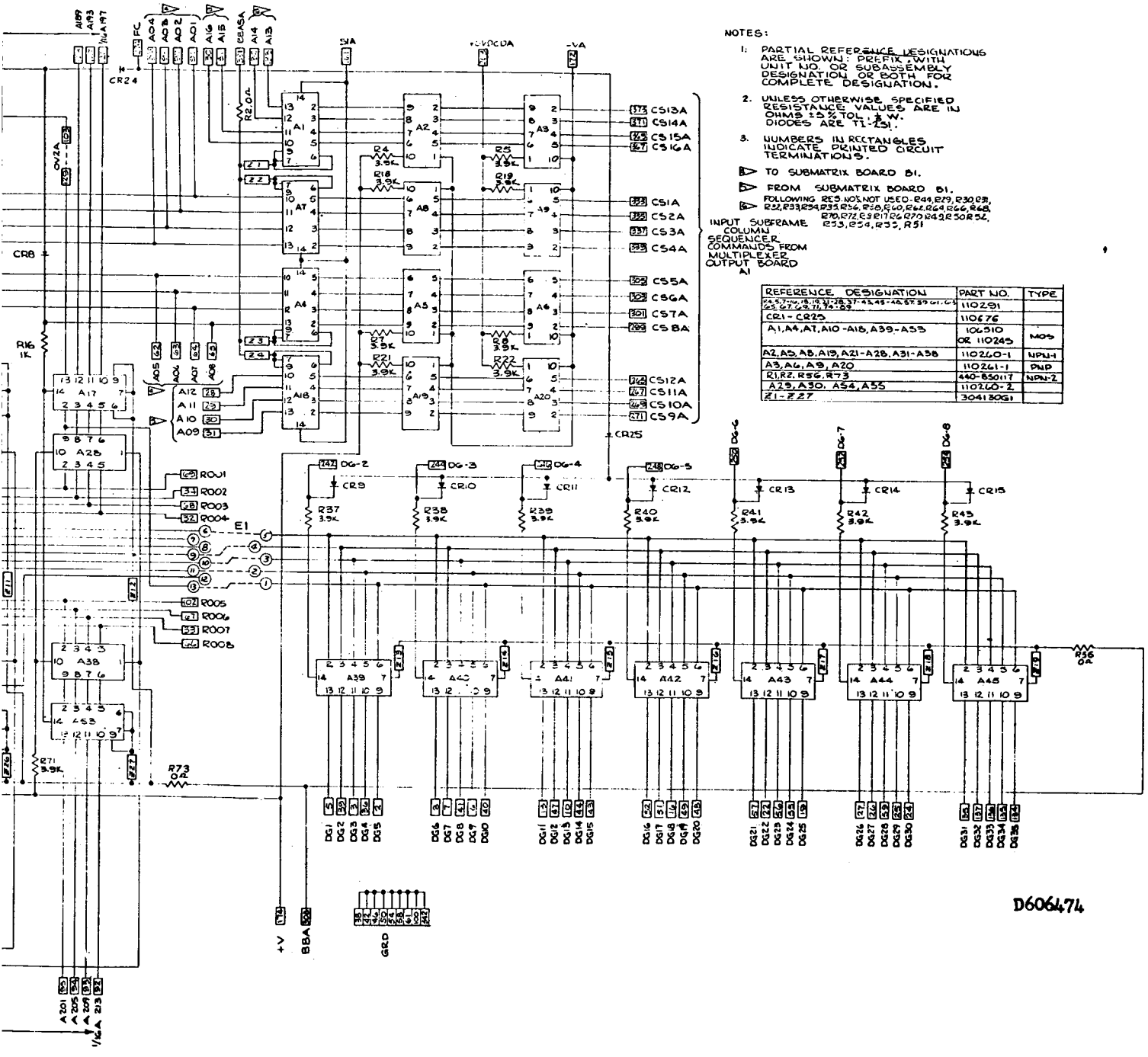
Figure 1-8 . Prime Matrix Board, Schematic Diagram

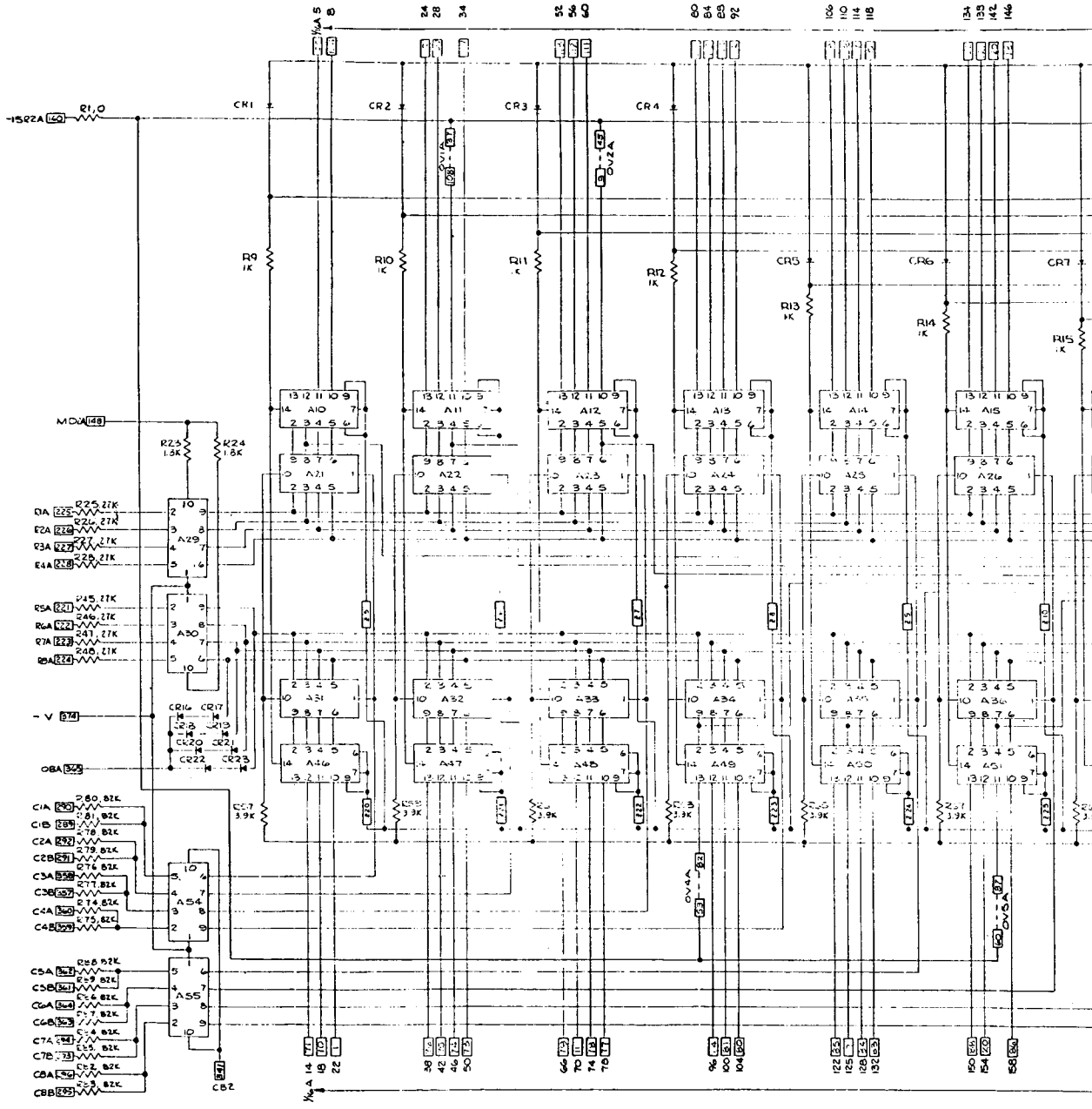

-15R1A
R1
CR1
CR2
CR3
CR4
CR5
CR6
CR7
R9 1K
R10 1K
R11 1K
R12 1K
R13 1K
R14 1K
R15 1K
MDIA
R23 1.8K
R24 1.8K
R1A
R2A
R3A
R4A
R5A
R6A
R7A
R8A
-V
OBA
C1A
C1B
C2A
C2B
C3A
C3B
C4A
C4B
C5A
C5B
C6A
C6B
C7A
C7B
C8A
C8B
CB1

1-10-1



REFERENCE DESIGNATION	PART NO.	TYPE
[illegible]	1102291	
CR1 - CR25	110676	
A1, A4, A7, A10 - A18, A39 - A53	106510 OR 110245	MOS
A2, A5, A8, A19, A21 - A28, A31 - A38	110260-1	NPN-1
A3, A6, A9, A20	110261-1	PNP
R1, R2, R56, R73	440-850117	NPN-2
A29, A30, A54, A55	110260-2	
Z1 - Z27	3041806-1	

Figure 1-9. Submatrix Board A1, Schematic Diagram



-15R2A
R1,0
CR1
CR2
CR3
CR4
CR5
CR6
CR7
R9 1K
R10 1K
R11 1K
R12 1K
R13 1K
R14 1K
R15 1K
MDA
R23 1.5K
R24 1.8K
R1A
R2A
R3A
R4A
R5A
R6A
R7A
R8A
A29
A30
-V
OBA
C1A
C1B
C2A
C2B
C3A
C3B
C4A
C4B
C5A
C5B
C6A
C6B
C7A
C7B
C8A
C8B
A54
A55
CB2
A10
A11
A12
A13
A14
A15
A21
A22
A23
A24
A25
A26
A31
A32
A33
A34
A35
A36
A46
A47
A48
A49
A50
A51

F11-1

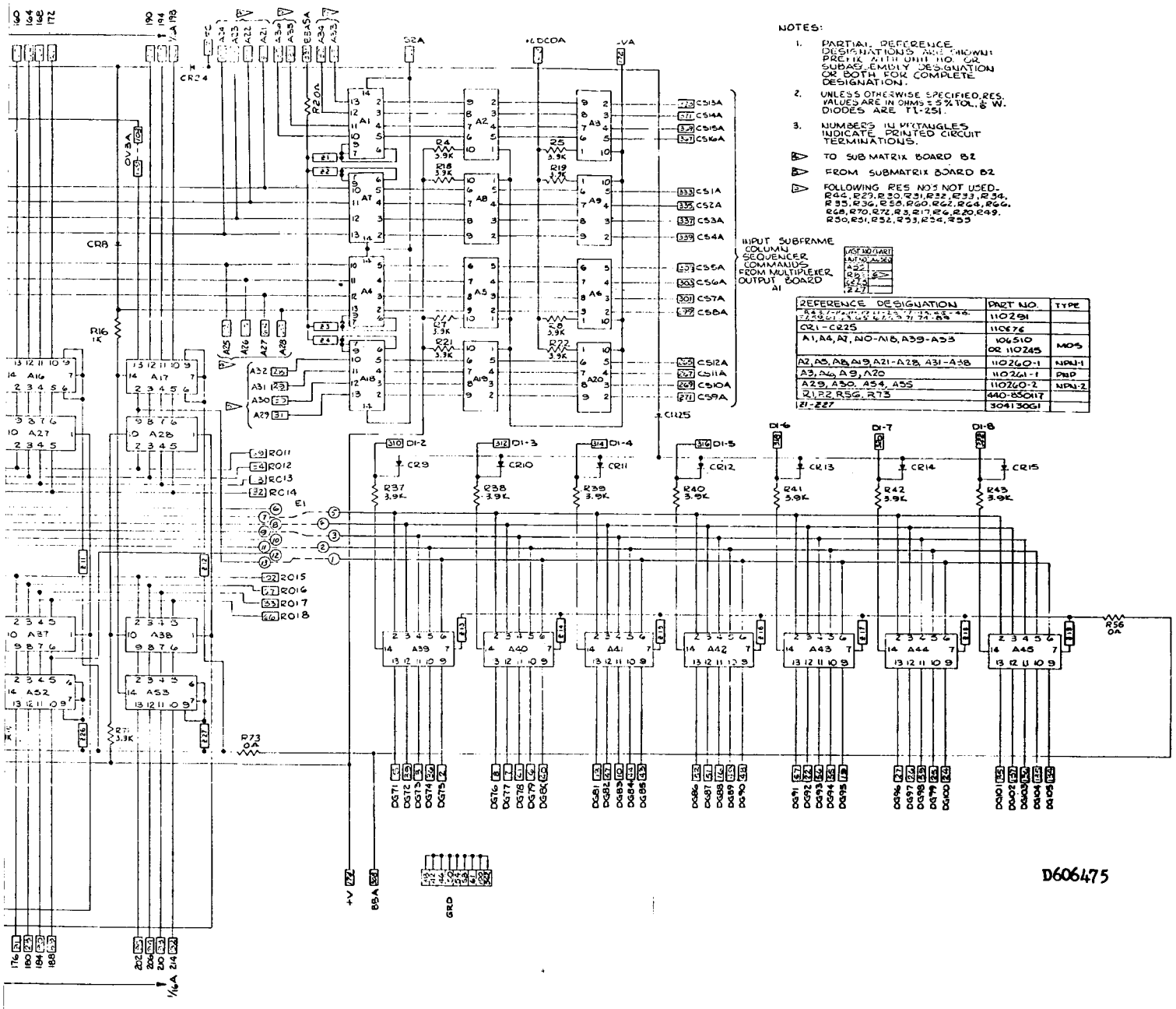
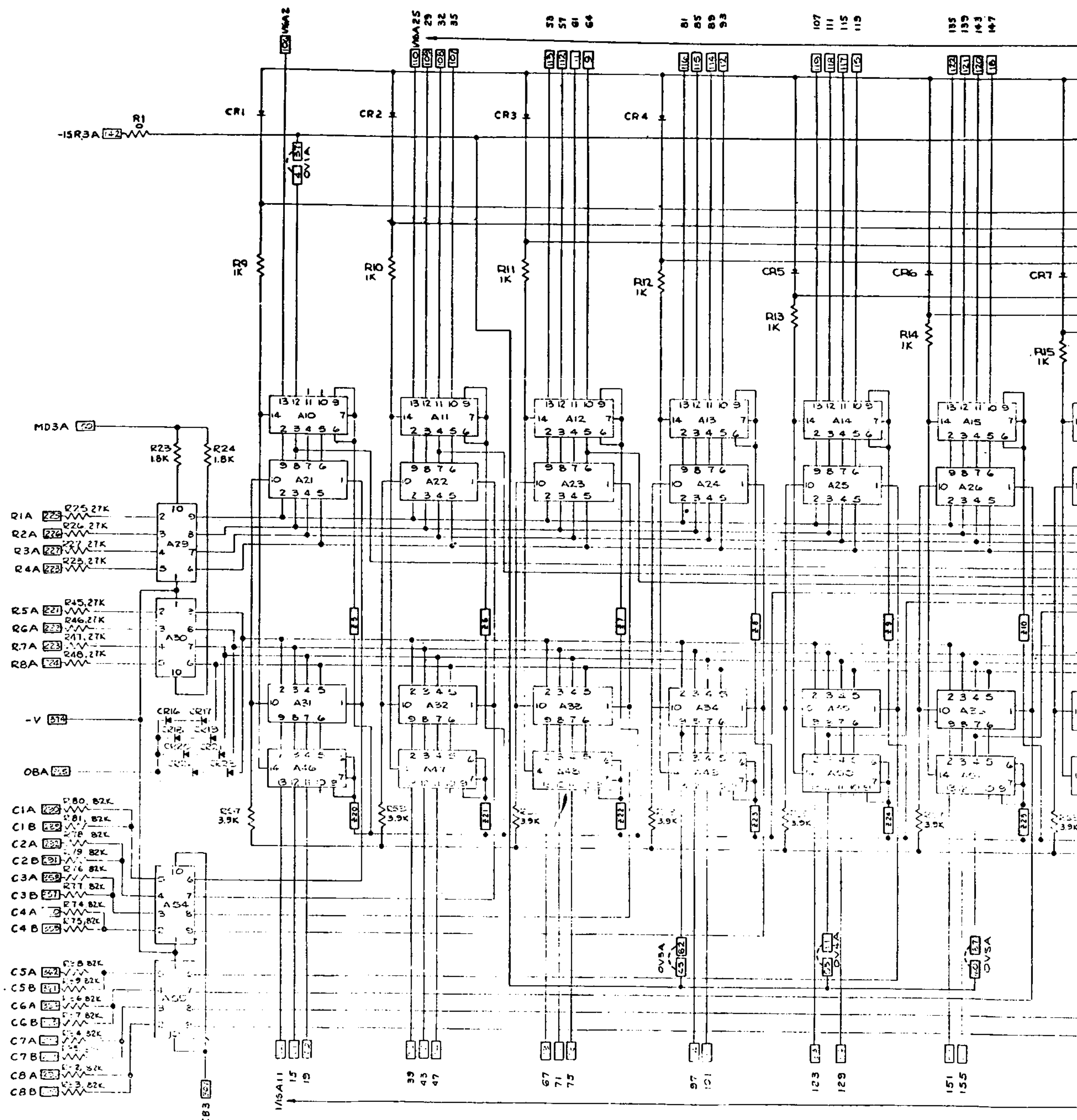


Figure I-10. Submatrix Board A2, Schematic Diagram


-15R3A
R1
CR1
CR2
CR3
CR4
CR5
CR6
CR7
R9 1K
R10 1K
R11 1K
R12 1K
R13 1K
R14 1K
R15 1K
MD3A
R23 1.8K
R24 1.8K
A10
A11
A12
A13
A14
A15
A21
A22
A23
A24
A25
A26
A29
A30
A31
A32
A33
A34
A46
A54
A55
R1A
R2A
R3A
R4A
R5A
R6A
R7A
R8A
-V
OBA
C1A
C1B
C2A
C2B
C3A
C3B
C4A
C4B
C5A
C5B
C6A
C6B
C7A
C7B
C8A
C8B
CB3
3.9K
OV5A
1/15A11

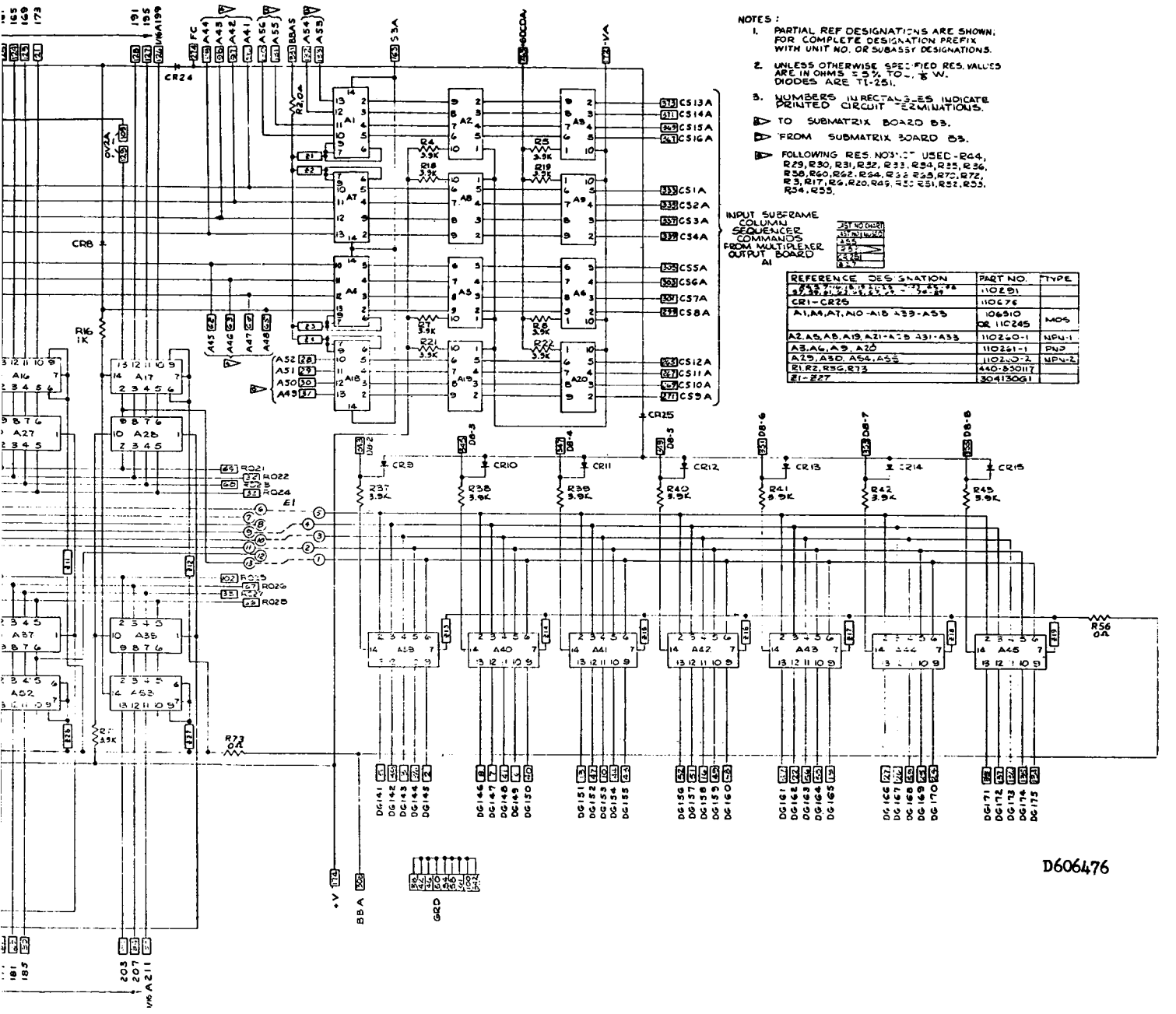
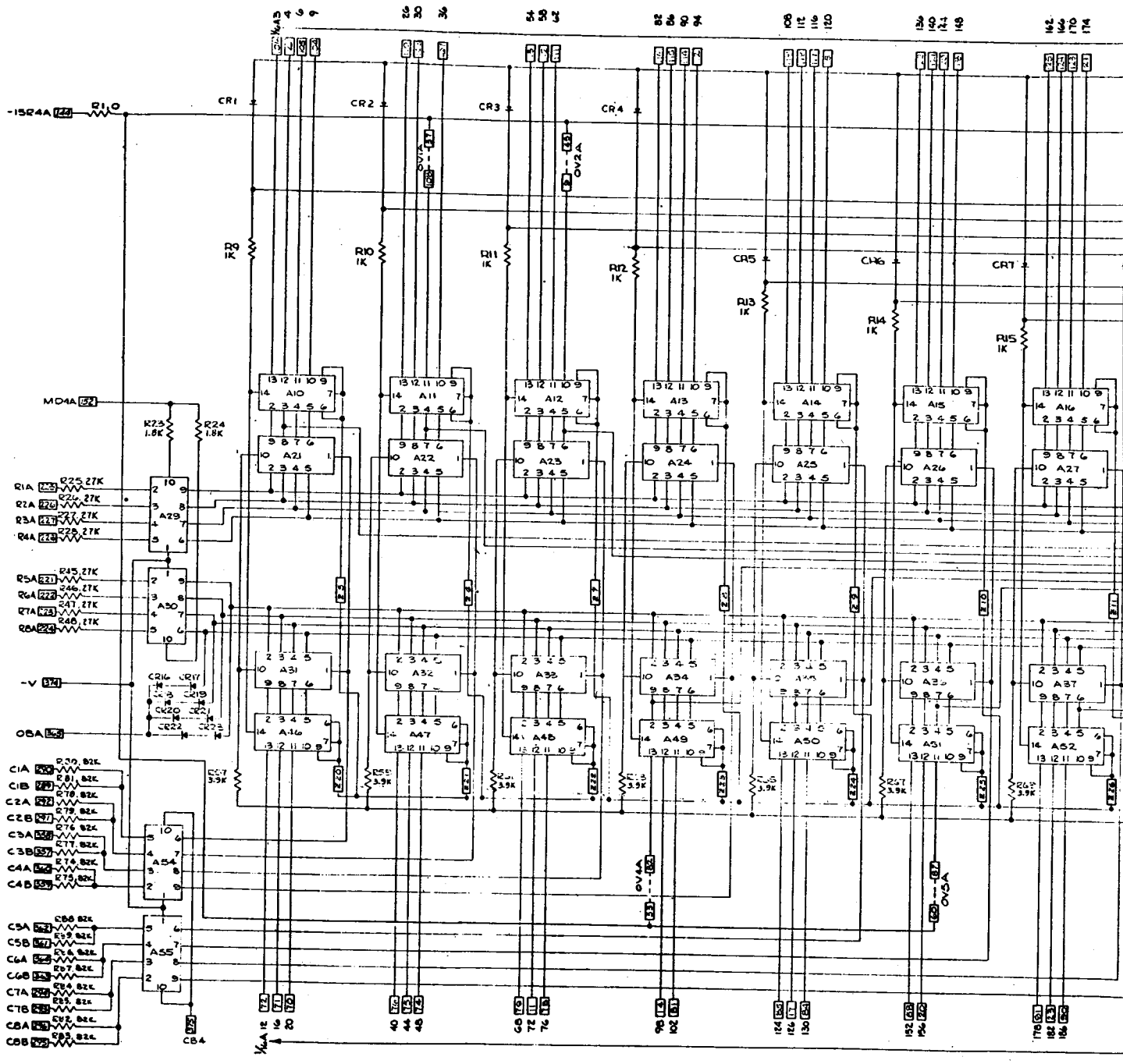


Figure I-11. Submatrix Board A3, Schematic Diagram


-15R4A
R1.0
CR1
CR2
CR3
CR4
CR5
CR6
CR7
R9 1K
R10 1K
R11 1K
R12 1K
R13 1K
R14 1K
R15 1K
MD4A
R23 1.8K
R24 1.8K
R1A
R2A
R3A
R4A
R5A
R6A
R7A
R8A
-V
OBA
C1A
C1B
C2A
C2B
C3A
C3B
C4A
C4B
C5A
C5B
C6A
C6B
C7A
C7B
C8A
C8B
CB4
A10
A11
A12
A13
A14
A15
A16
A21
A22
A23
A24
A25
A26
A27
A29
A30
A31
A32
A33
A34
A35
A36
A37
A46
A47
A48
A49
A50
A51
A52
A54
A55
0V1A
0V2A
0V4A
0V5A

1-13-1

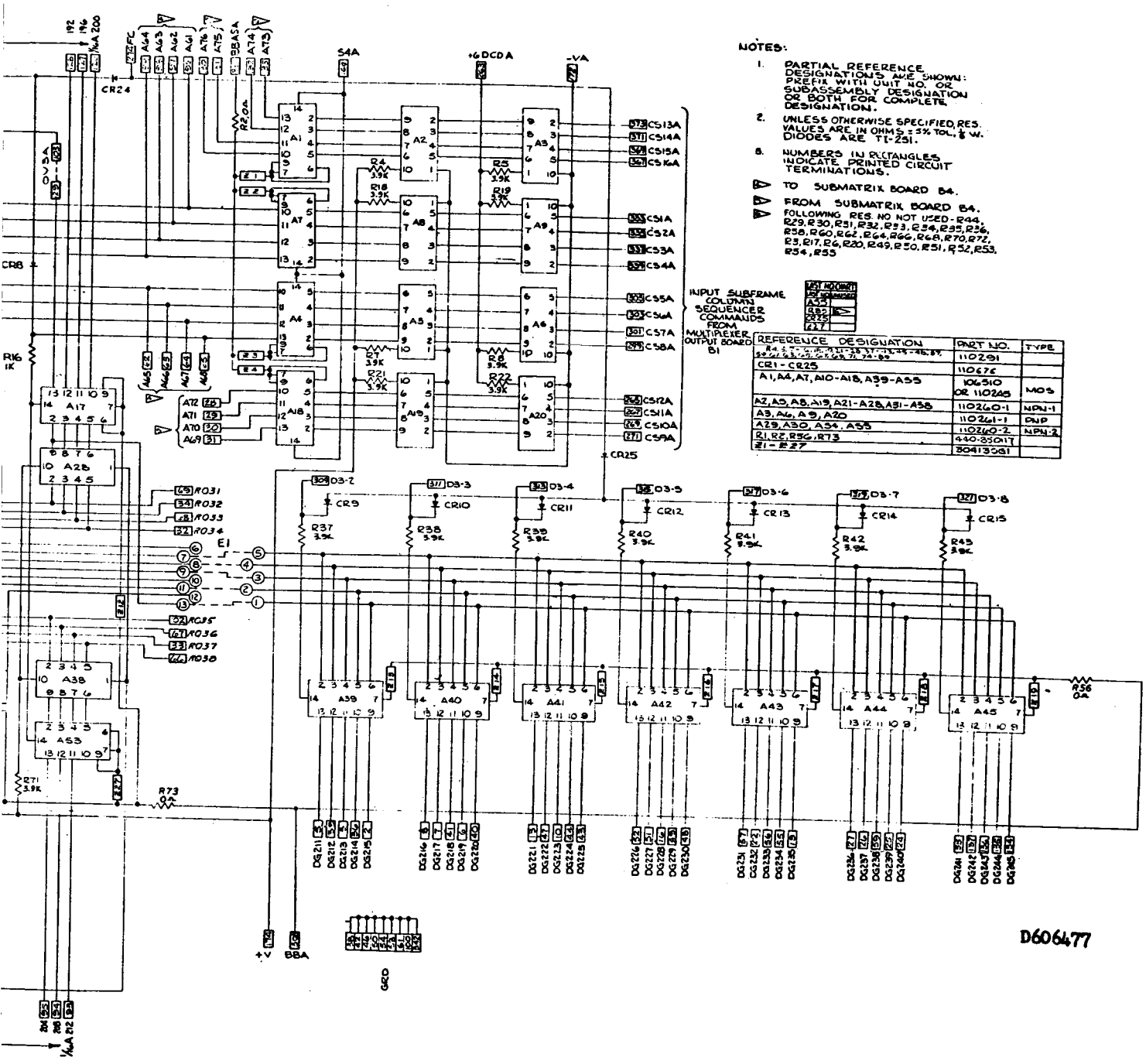
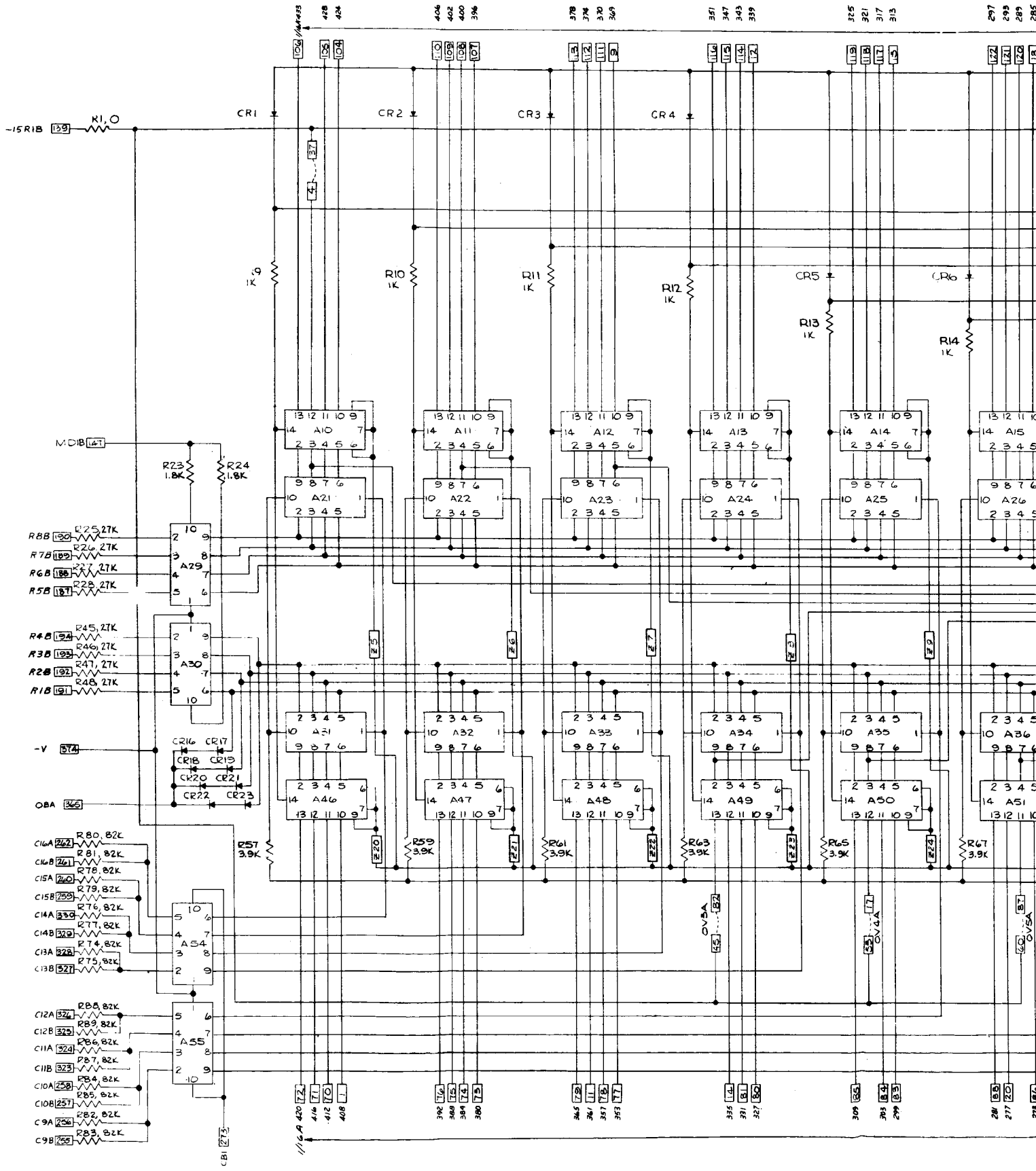
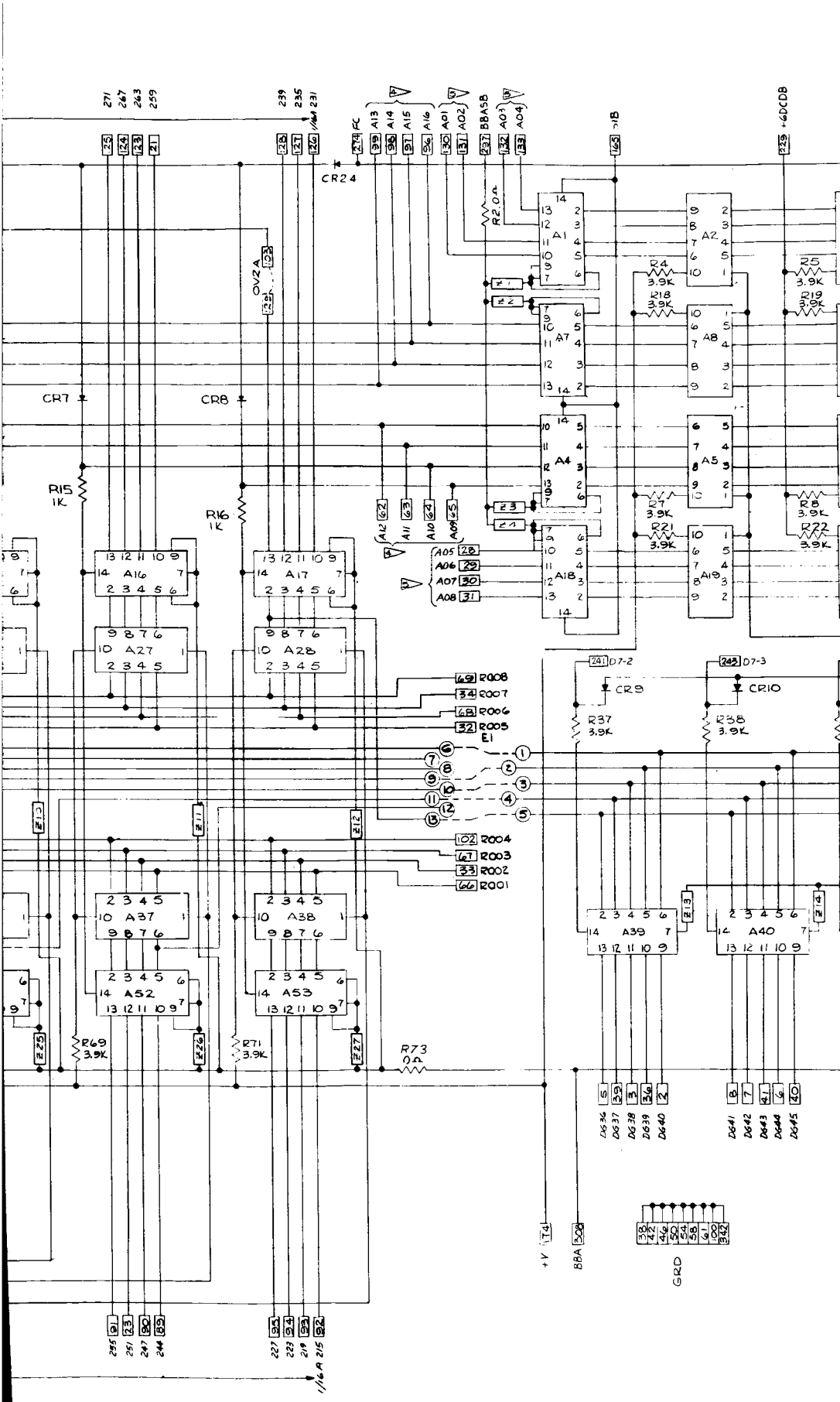


Figure I-12. Submatrix Board A4, Schematic Diagram


-15R1B
R1, 0
CR1
CR2
CR3
CR4
CR5
CR6
R9 1K
R10 1K
R11 1K
R12 1K
R13 1K
R14 1K
M DIB
R23 1.8K
R24 1.8K
R8B
R7B
R6B
R5B
R4B
R3B
R2B
R1B
-V
OBA
C16A
C16B
C15A
C15B
C14A
C14B
C13A
C13B
C12A
C12B
C11A
C11B
C10A
C10B
C9A
C9B
R57 3.9K
R59 3.9K
R61 3.9K
R63 3.9K
R65 3.9K
R67 3.9K
0V5A
0V4A
CBI



CR24
CR7
CR8
CR9
CR10
R15 1K
R16 1K
R2.0Ω
R4 3.9K
R5 3.9K
R7 3.9K
R8 3.9K
R21 3.9K
R22 3.9K
R37 3.9K
R38 3.9K
R69 3.9K
R71 3.9K
R73 0Ω
R008
R007
R006
R005
R004
R003
R002
R001
E1
A1
A2
A4
A5
A7
A8
A16
A17
A18
A19
A27
A28
A37
A38
A39
A40
A52
A53
+6DCDB
+V
BBA
GRD

1-14-2

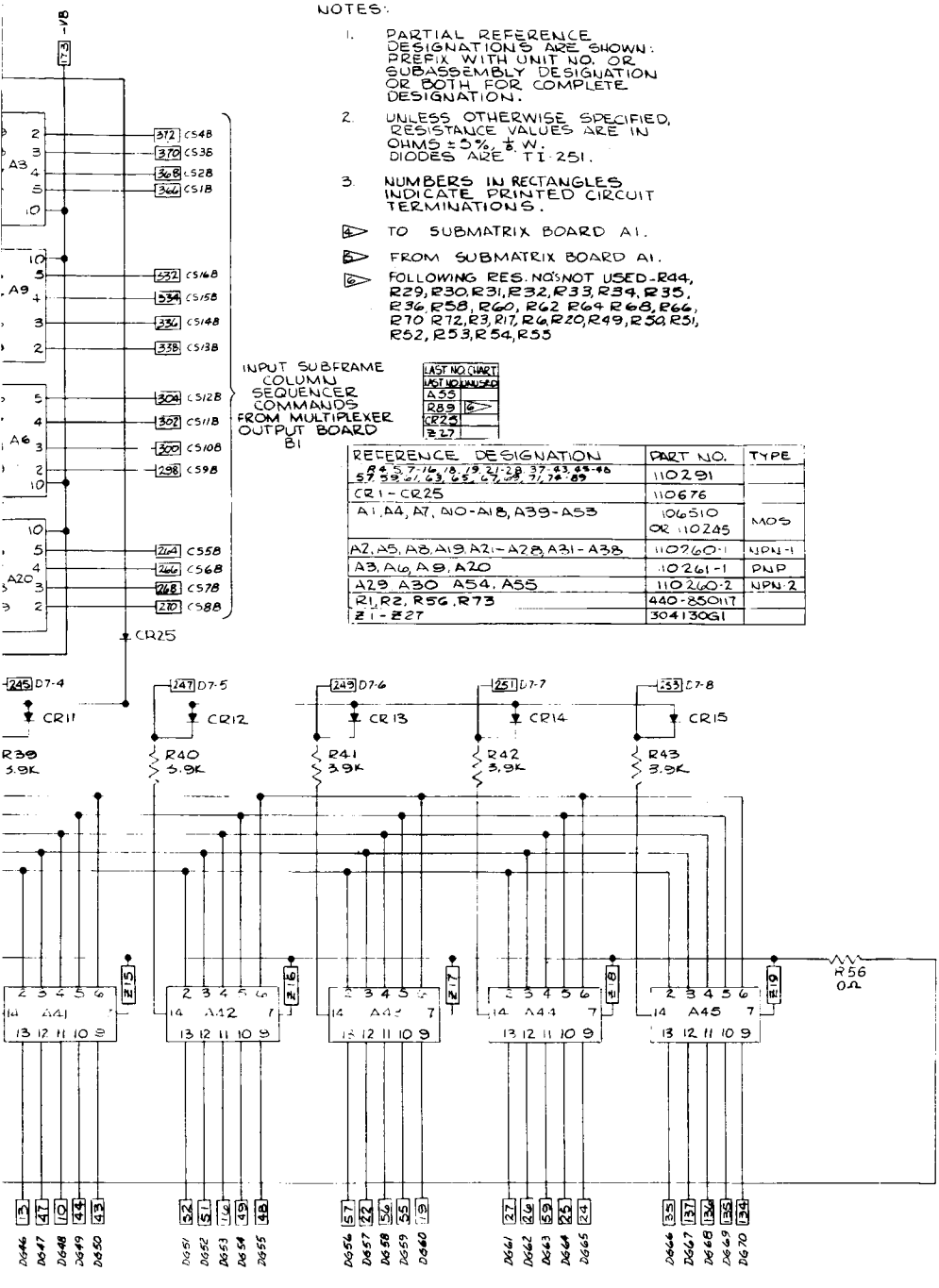
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: PREFIX WITH UNIT NO. OR SUBASSEMBLY DESIGNATION OR BOTH FOR COMPLETE DESIGNATION.
2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS ± 5%, ¼ W. DIODES ARE TI-251.
3. NUMBERS IN RECTANGLES INDICATE PRINTED CIRCUIT TERMINATIONS.

4 TO SUBMATRIX BOARD A1.

5 FROM SUBMATRIX BOARD A1.

6 FOLLOWING RES. NO'S NOT USED - R44, R29, R30, R31, R32, R33, R34, R35, R36, R58, R60, R62, R64, R68, R66, R70, R72, R3, R17, R6, R20, R49, R50, R51, R52, R53, R54, R55



LAST NO. CHART	
LAST NO. UNUSED	
A55	
R89	6
CR25	
Z27	

REFERENCE DESIGNATION	PART NO.	TYPE
R4, 5, 7-16, 18, 19, 21-28, 37-43, 45-48, 57, 59, 61, 63, 65, 67, 68, 71, 74-89	110291	
CR1 - CR25	110676	
A1, A4, A7, A10-A18, A39-A53	106510 OR 110245	MOS
A2, A5, A8, A19, A21-A28, A31-A38	110260-1	NPN-1
A3, A6, A9, A20	110261-1	PNP
A29 A30 A54, A55	110260-2	NPN-2
R1, R2, R56, R73	440-850117	
Z1 - Z27	304130G1	

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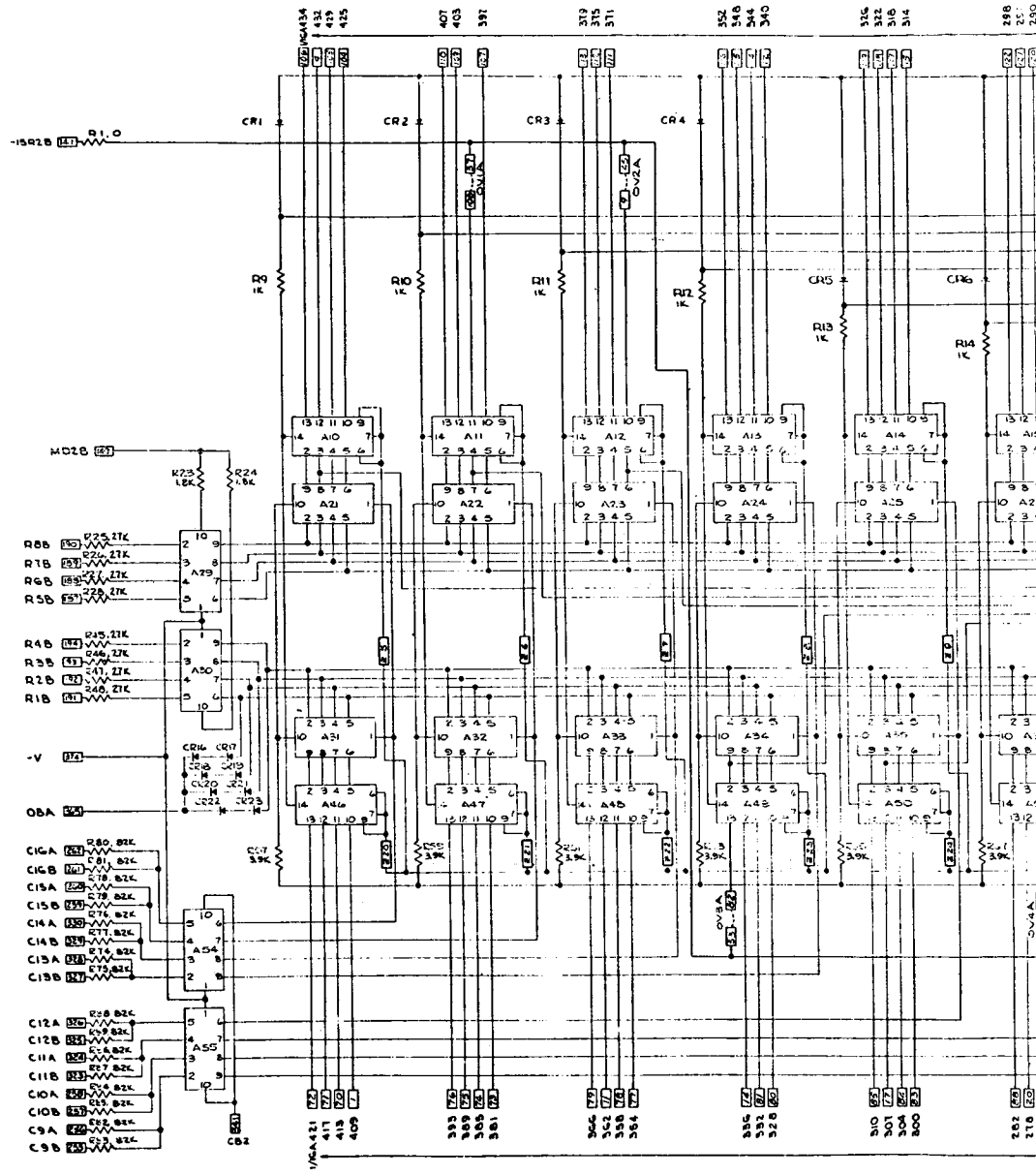
Figure 1-13. Submatrix Board B1, Schematic Diagram



CR1
CR2
CR3
CR4
CR5
CR6
R9 1K
R10 1K
R11 1K
R12 1K
R13 1K
R14 1K
MD2B
R8B
R7B
R6B
R5B
R4B
R3B
R2B
R1B
-V
OBA
C16A
C16B
C15A
C15B
C14A
C14B
C13A
C13B
C12A
C12B
C11A
C11B
C10A
C10B
C9A
C9B
CB2

1-15-1

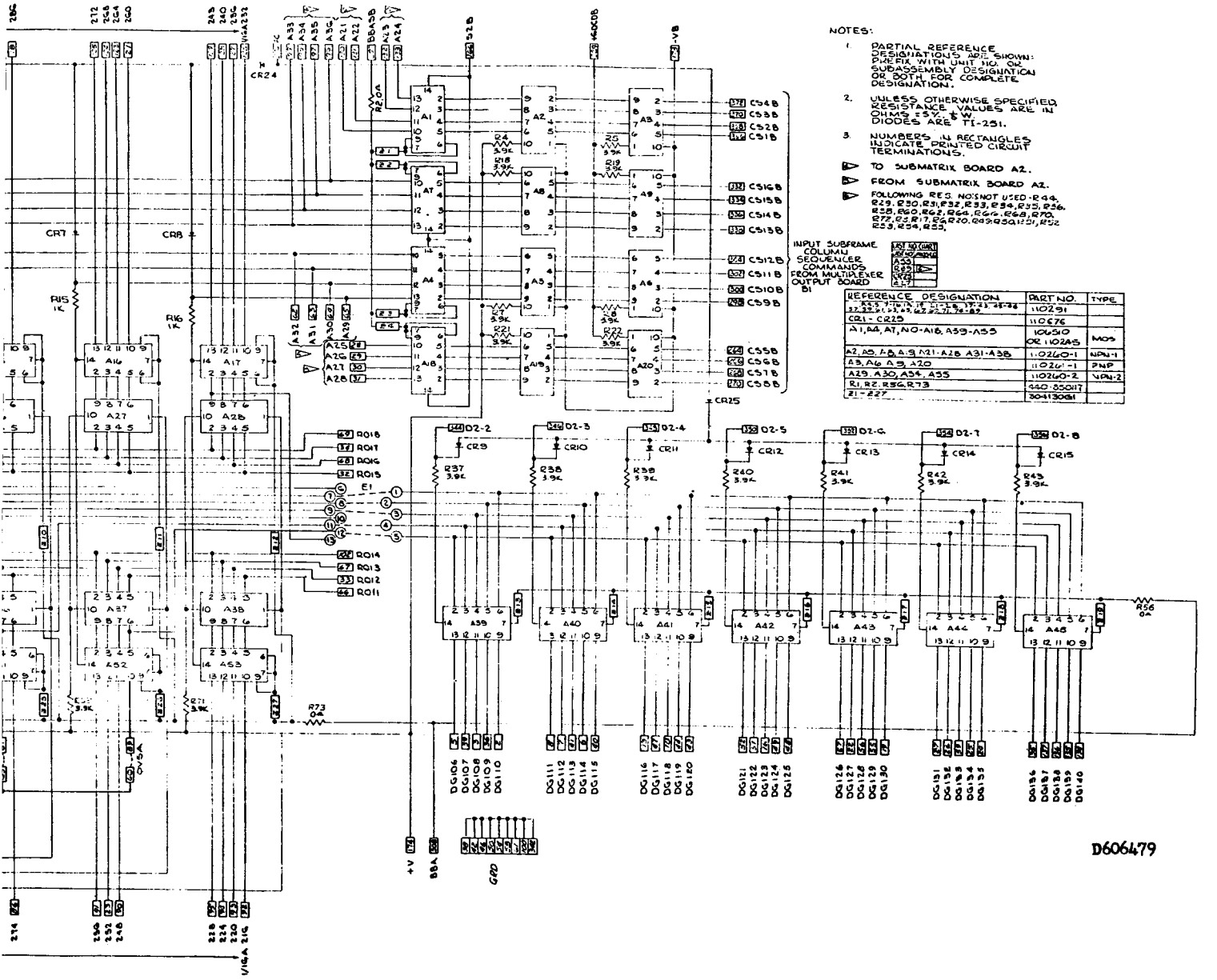
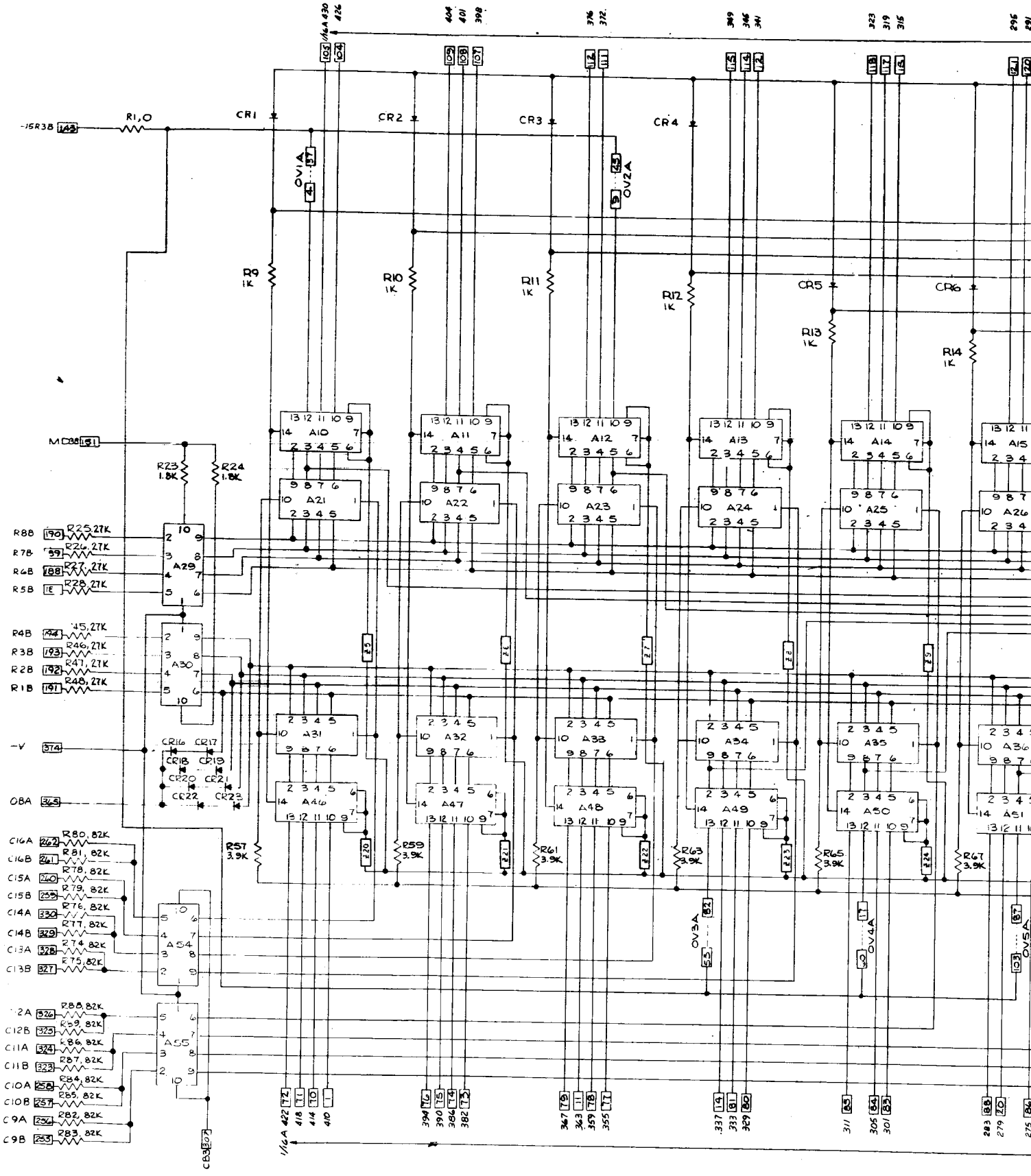
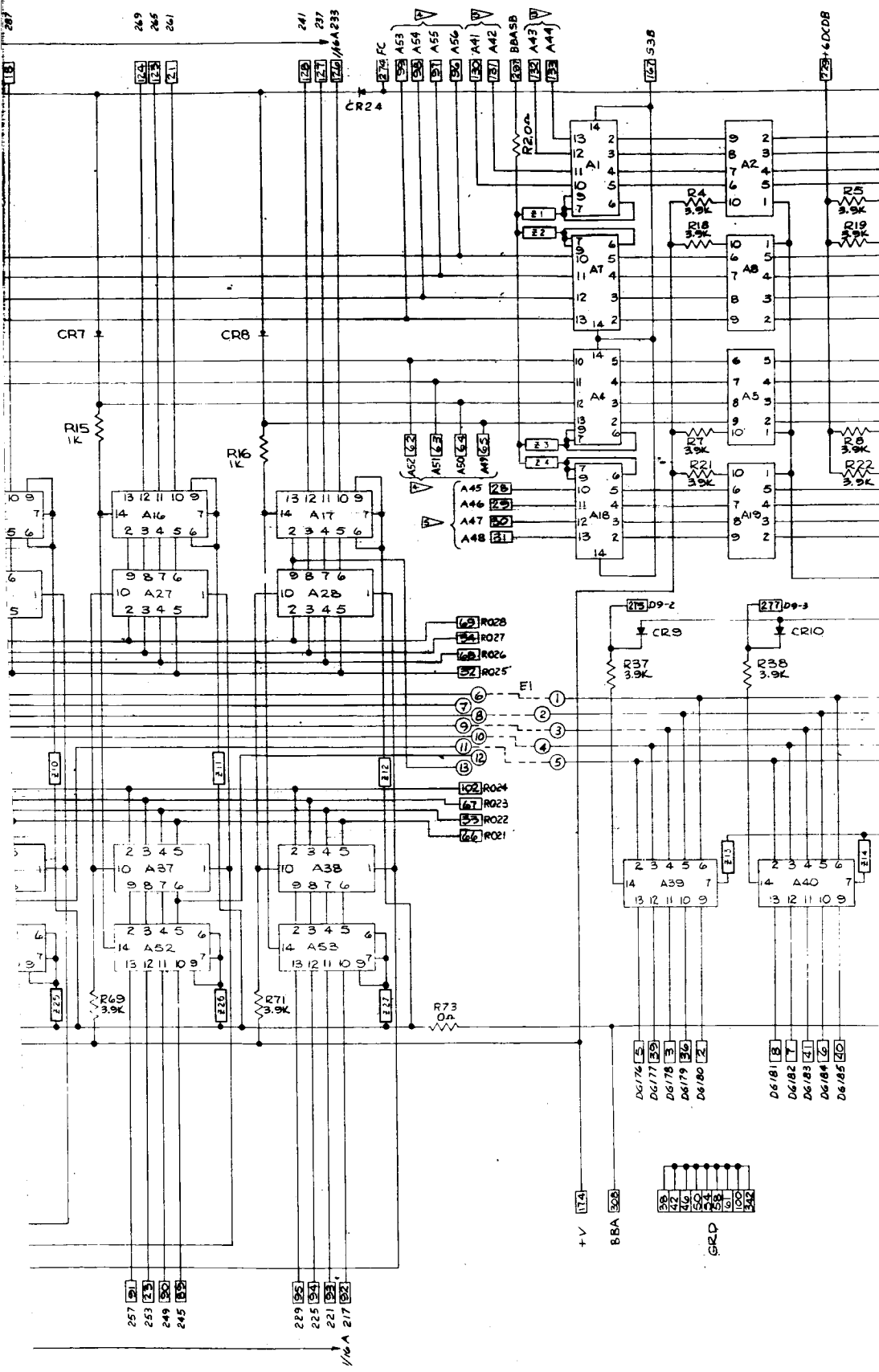


Figure I-14. Submatrix Board B2, Schematic Diagram


-15R38
R1,0
CR1
CR2
CR3
CR4
CR5
CR6
OV1A
OV2A
OV3A
OV4A
OV5A
R9 1K
R10 1K
R11 1K
R12 1K
R13 1K
R14 1K
MC88
R23 1.8K
R24 1.8K
R88
R78
R68
R58
R48
R38
R28
R18
-V
OBA
C16A
C16B
C15A
C15B
C14A
C14B
C13A
C13B
C12A
C12B
C11A
C11B
C10A
C10B
C9A
C9B
R25 27K
R26 27K
R27 27K
R28 27K
R45 27K
R46 27K
R47 27K
R48 27K
R80 82K
R81 82K
R78 82K
R79 82K
R76 82K
R77 82K
R74 82K
R75 82K
R88 82K
R89 82K
R86 82K
R87 82K
R84 82K
R85 82K
R82 82K
R83 82K
A10
A11
A12
A13
A14
A15
A21
A22
A23
A24
A25
A26
A29
A30
A31
A32
A33
A34
A35
A36
A40
A47
A48
A49
A50
A51
A54
A55
R57 3.9K
R59 3.9K
R61 3.9K
R63 3.9K
R65 3.9K
R67 3.9K
CR16
CR17
CR18
CR19
CR20
CR21
CR22
CR23
CB3

1-16-1


CR24
R20Ω
A1
A2
A7
A8
A4
A5
A18
A19
R4 3.9K
R5 3.9K
R18 3.9K
R19 3.9K
CR7
CR8
R15 1K
R16 1K
A16
A17
A27
A28
R7 3.9K
R8 3.9K
R21 3.9K
R22 3.9K
R028
R027
R026
R025
E1
CR9
CR10
R37 3.9K
R38 3.9K
R024
R023
R022
R021
A37
A38
A52
A53
A39
A40
R69 3.9K
R71 3.9K
R73 0Ω
+V
BBA
GRD

1-16-2

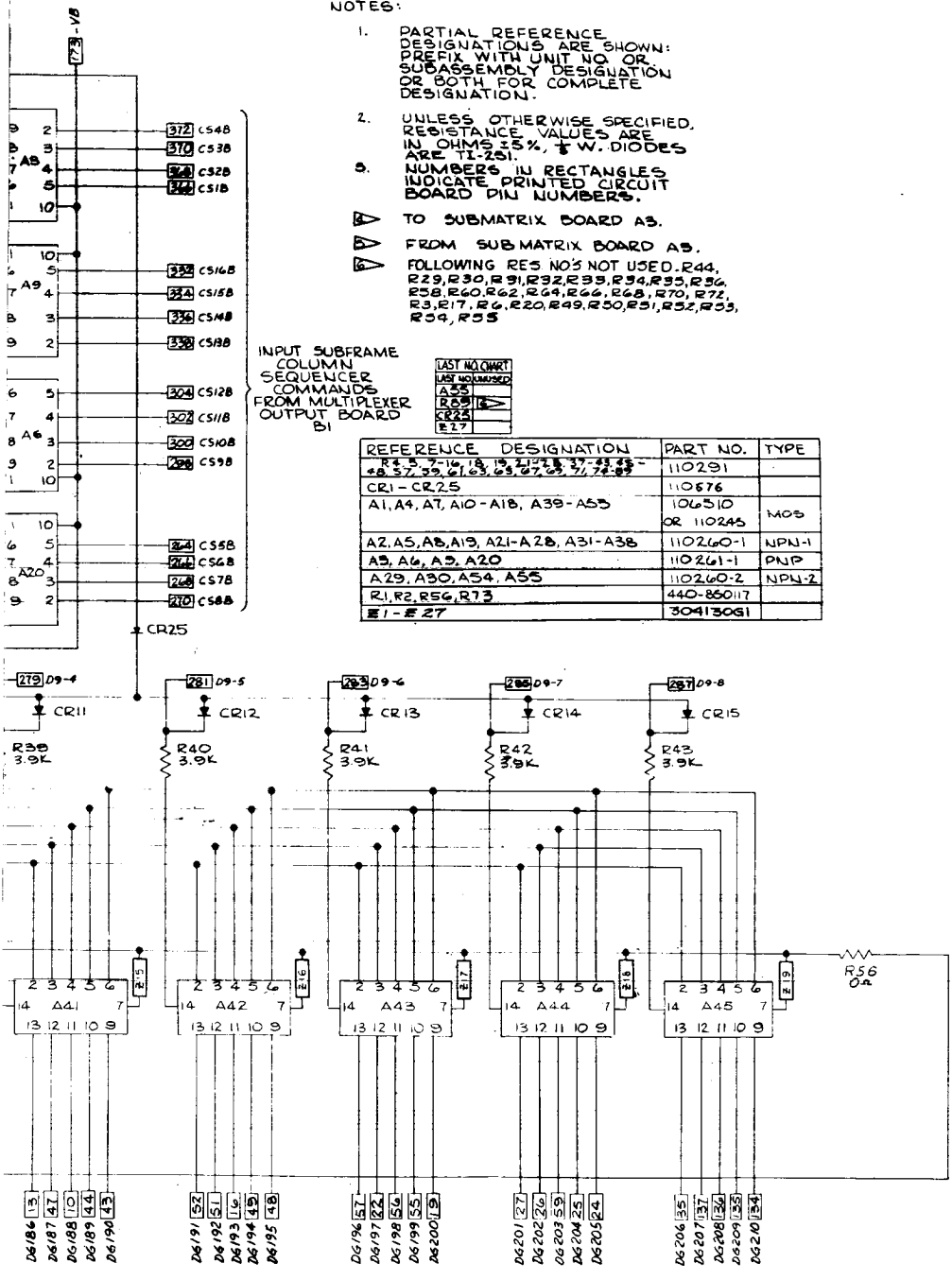
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: PREFIX WITH UNIT NO. OR SUBASSEMBLY DESIGNATION OR BOTH FOR COMPLETE DESIGNATION.
2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS ±5%, ½ W. DIODES ARE TI-251.
3. NUMBERS IN RECTANGLES INDICATE PRINTED CIRCUIT BOARD PIN NUMBERS.

TO SUBMATRIX BOARD A3.

FROM SUBMATRIX BOARD A3.

FOLLOWING RES NO'S NOT USED. R44, R29, R30, R31, R32, R33, R34, R35, R36, R58, R60, R62, R64, R66, R68, R70, R72, R3, R17, R6, R20, R49, R50, R51, R52, R53, R54, R55

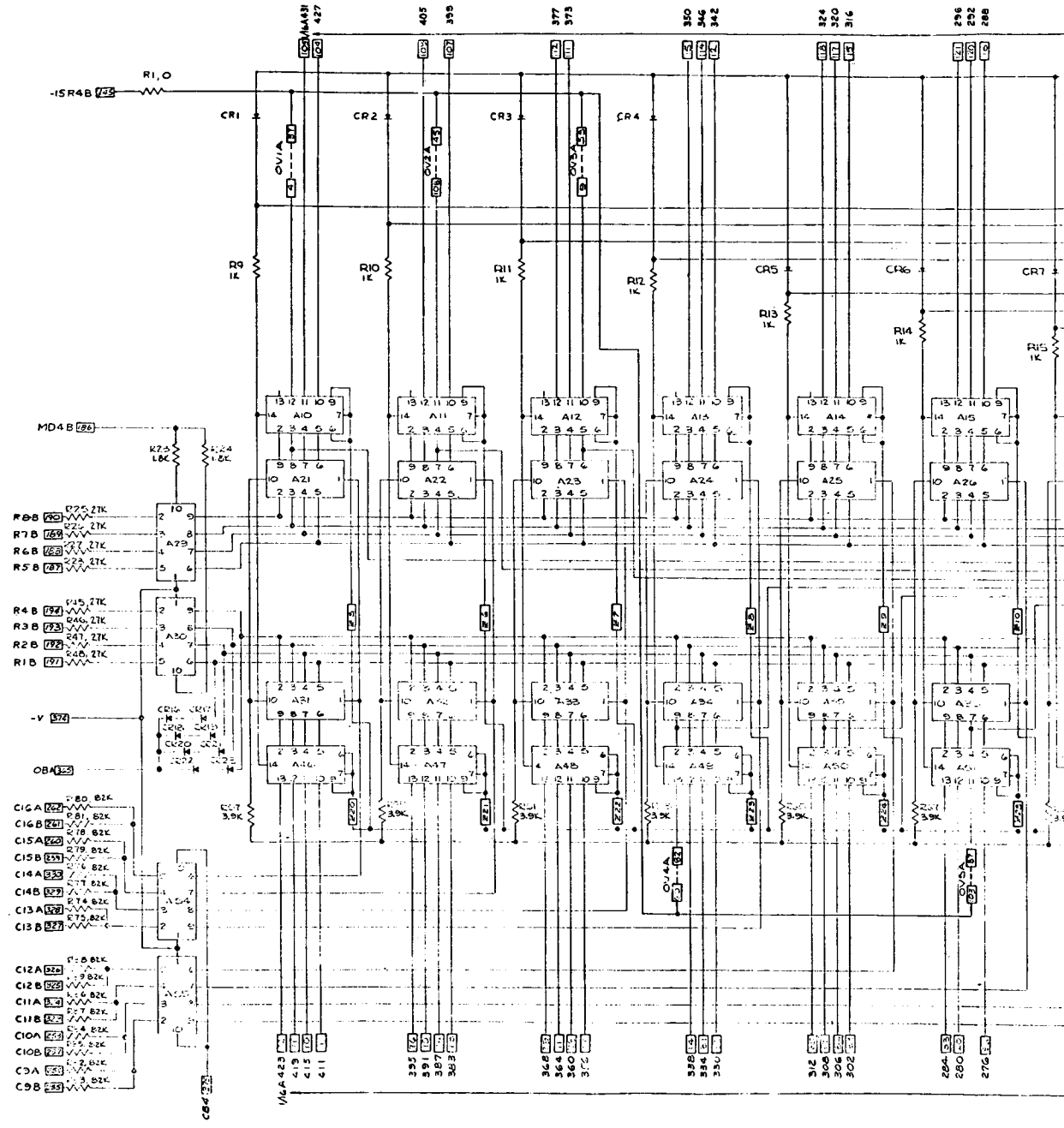


LAST NO. CHART	
LAST NO. USED	
A55	
R69	
CR25	
E27	

REFERENCE DESIGNATION	PART NO.	TYPE
R3, 5, 7-16, 18, 19, 21-27, 33-43, 45-48, 57, 59, 61, 63, 65, 67, 69, 71, 74-89	110291	
CR1 - CR25	110676	
A1, A4, A7, A10 - A18, A39 - A55	106510 OR 110245	MOS
A2, A5, A8, A19, A21 - A28, A31 - A38	110260-1	NPN-1
A3, A6, A9, A20	110261-1	PNP
A29, A30, A54, A55	110260-2	NPN-2
R1, R2, R56, R73	440-860117	
E1 - E27	304130G1	

606480

Figure 1-15. Submatrix Board B3, Schematic Diagram


-15R4B
R1,0
CR1
CR2
CR3
CR4
CR5
CR6
CR7
R9 1K
R10 1K
R11 1K
R12 1K
R13 1K
R14 1K
R15 1K
MD4B
R8B
R7B
R6B
R5B
R4B
R3B
R2B
R1B
-V
OBA
C16A
C16B
C15A
C15B
C14A
C14B
C13A
C13B
C12A
C12B
C11A
C11B
C10A
C10B
C9A
C9B
C84

1-17-1

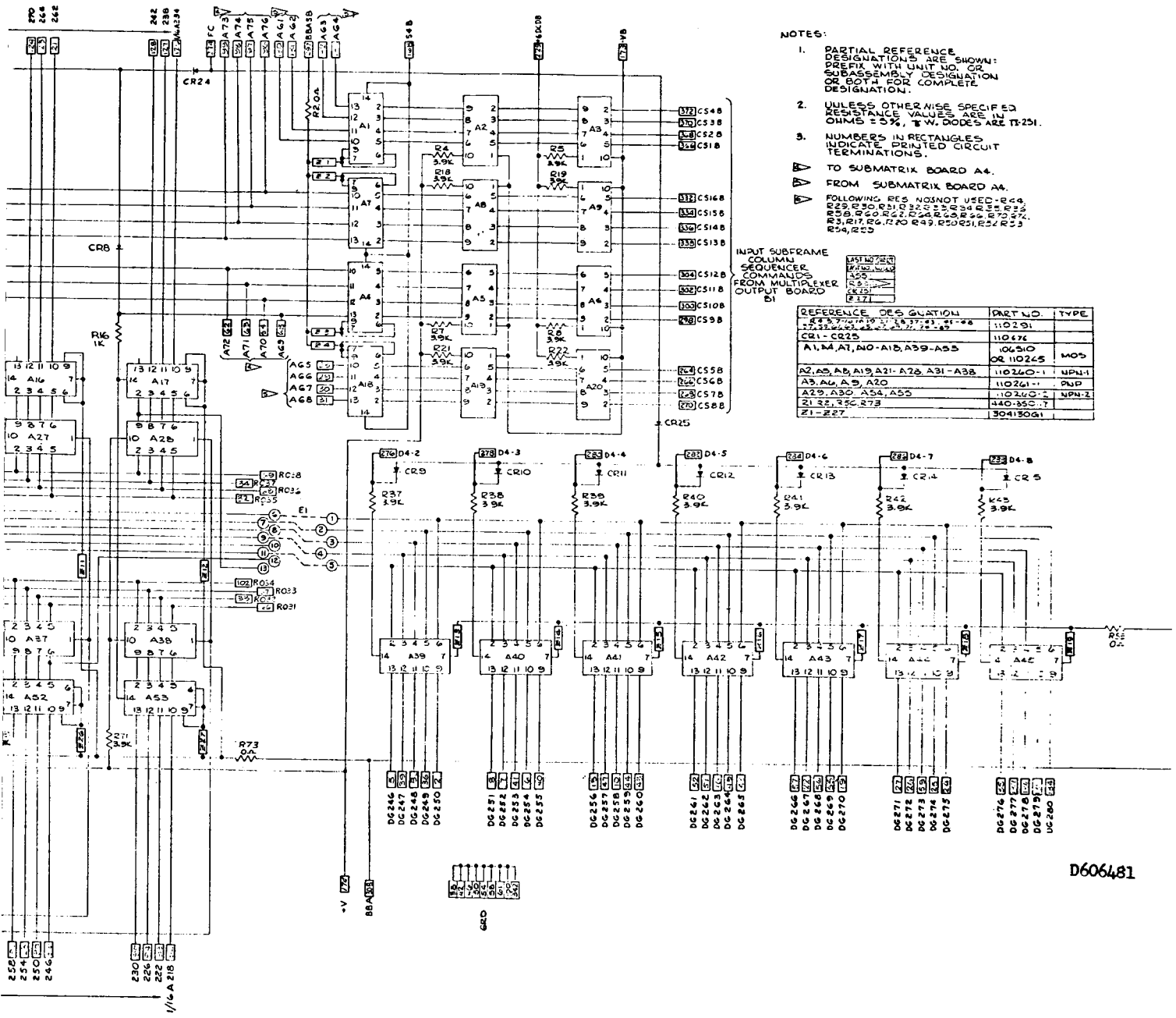
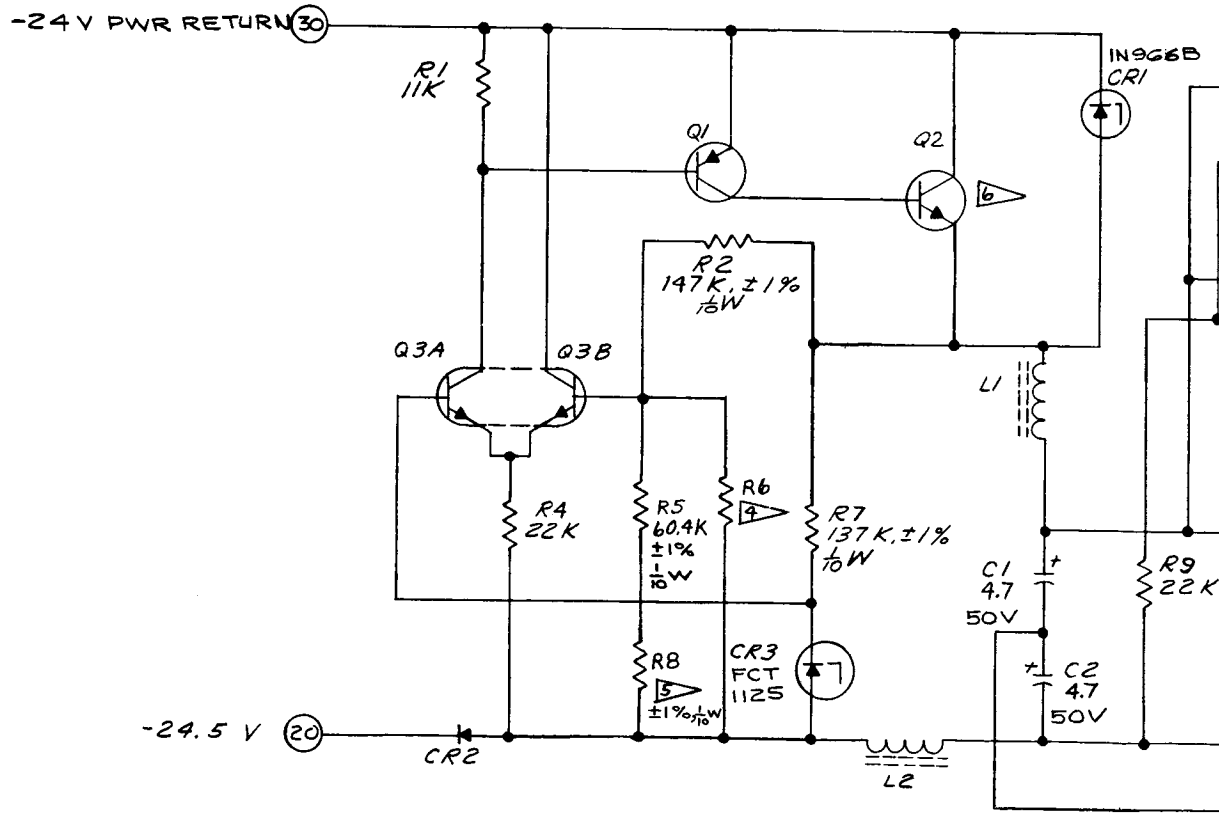


Figure I-16. Submatrix Board B4, Schematic Diagram

REF DESIGNATION	PART NO.
Q1, Q4, Q5	106941
Q2,	110153
Q3	106940
CR1	110173
CR3	106936
CR2, CR4 THRU CR19	110286
C1 THRU C9	100851
R1, R4, R6, R9 THRU R14	104115
R2, R5, R7 R8	104602
L1 & L2	112010
T1	112009
CR20	106933



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS ±5%, 1/8W CAPACITANCE VALUES ARE IN MICROFARADS ±10%, 35V. DIODES ARE 1N3600
2. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION (S).
3. NUMBERS IN CIRCLES INDICATES ASSY PIN NUMBERS.
4. R6 SAT RANGE 3.3 MEG, 5.6 MEG, 10 MEG OR OPEN
5. R8 SAT RANGE 0, 1.33K, 3.32K, 5.11K, 6.98K, 8.87K, 11K, 13K, 14K
6. TSTR Q2 TO BE MOUNTED TO HEAT SINK 30409961

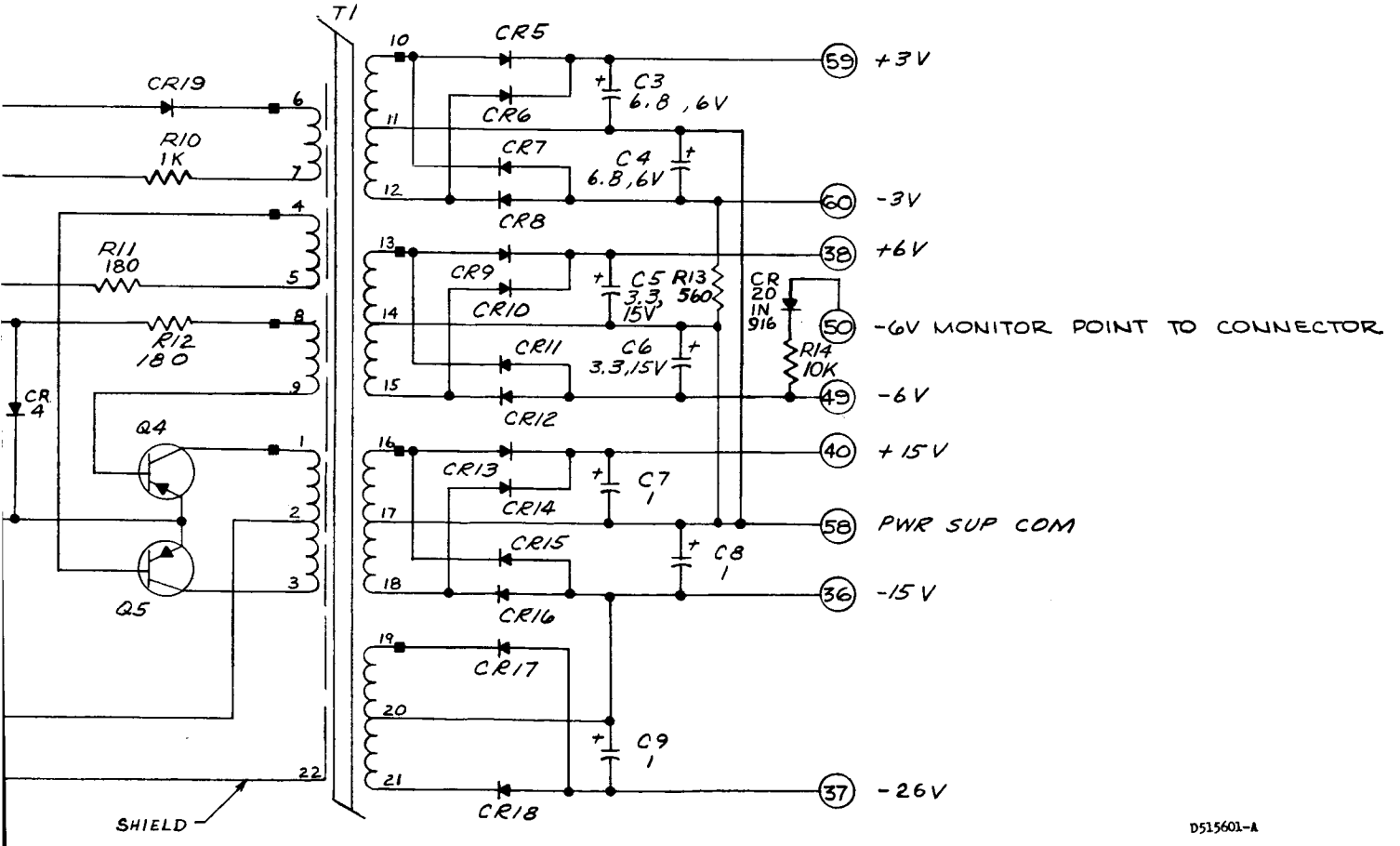
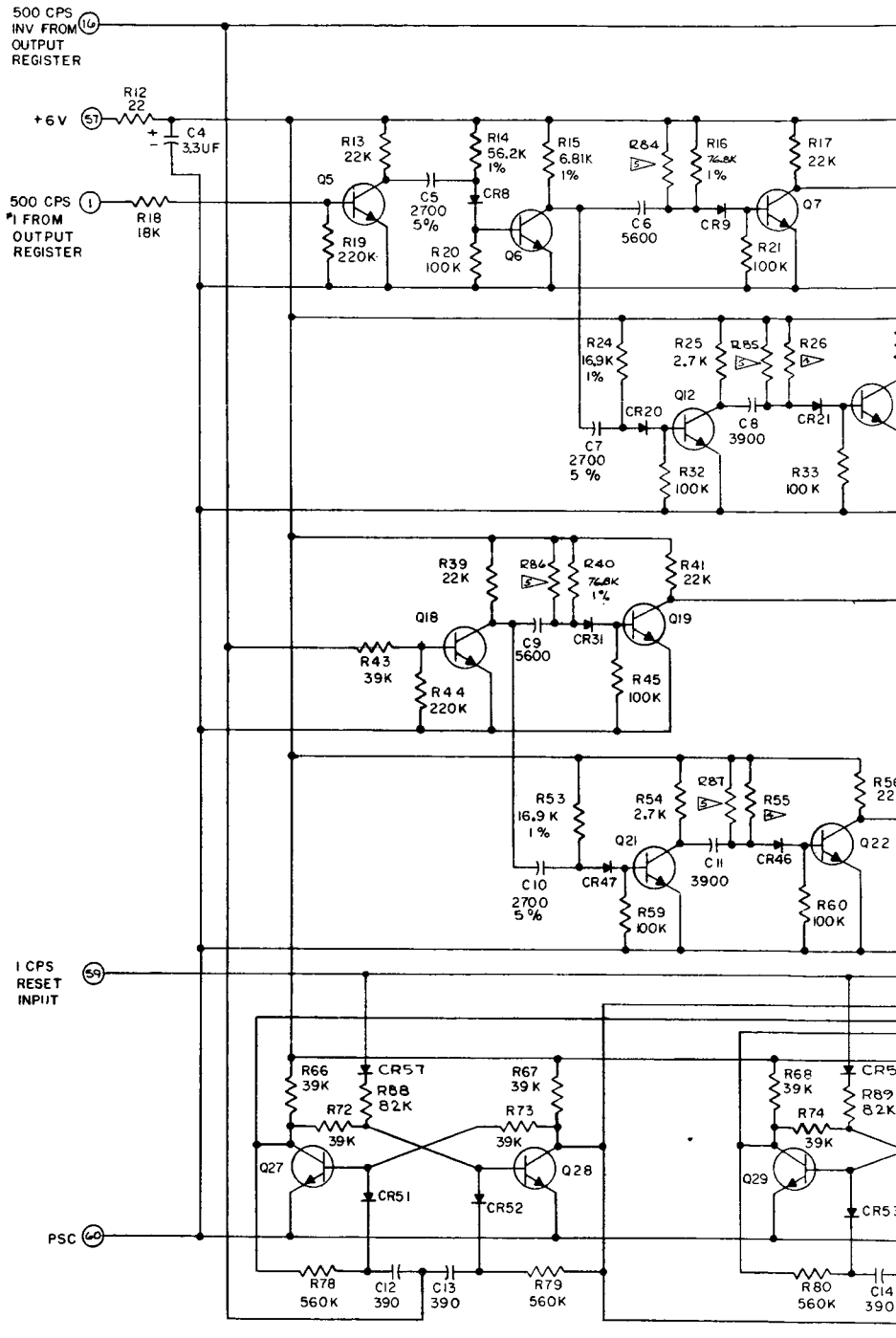


Figure 1-17. Power Supply, Schematic Diagram

REF DESIGNATION	PART NO.
CR1 – CR58	106933
Q1-Q22, Q25 - Q32	106943
Q23 & Q24	102618
C1 & C4	100851
C2, C5, C10, C7	104202
R1, R2, R4, R6, R7 – R13, R17 - R23, R25, R27 - R52, R54, R56 - R89	104115
R3, R5, R14, R15, R16, R24, R26, R40, R53, R55	106780
C8 - C17, C6, C3	104238

NOTES:
1. PARTIAL REF
FOR COMPLE
UNIT NO. OR
2. NUMBER IN
3. UNLESS OTI
RESISTANC
CAPACITAN
DIODES A
TRANSISTO



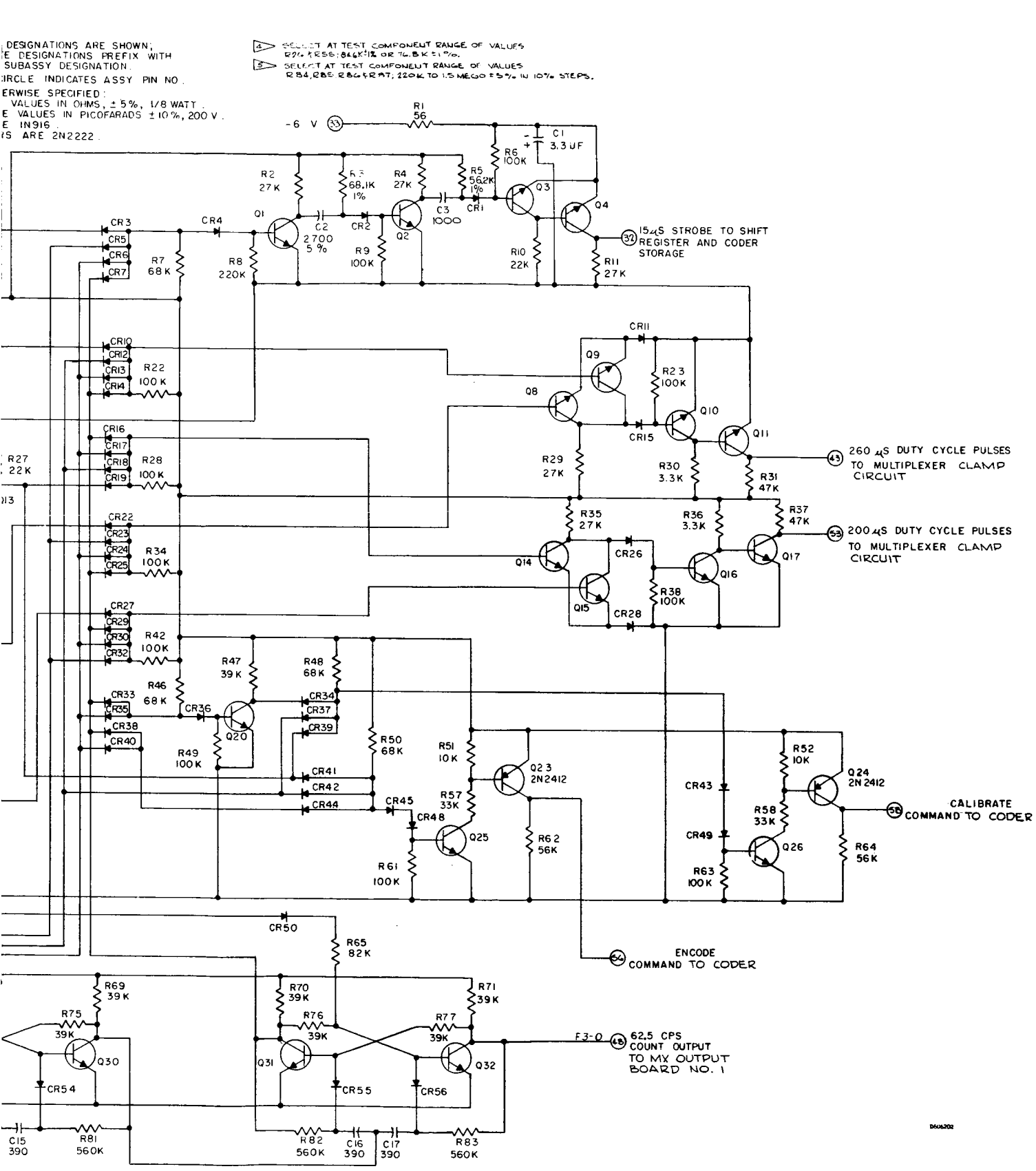
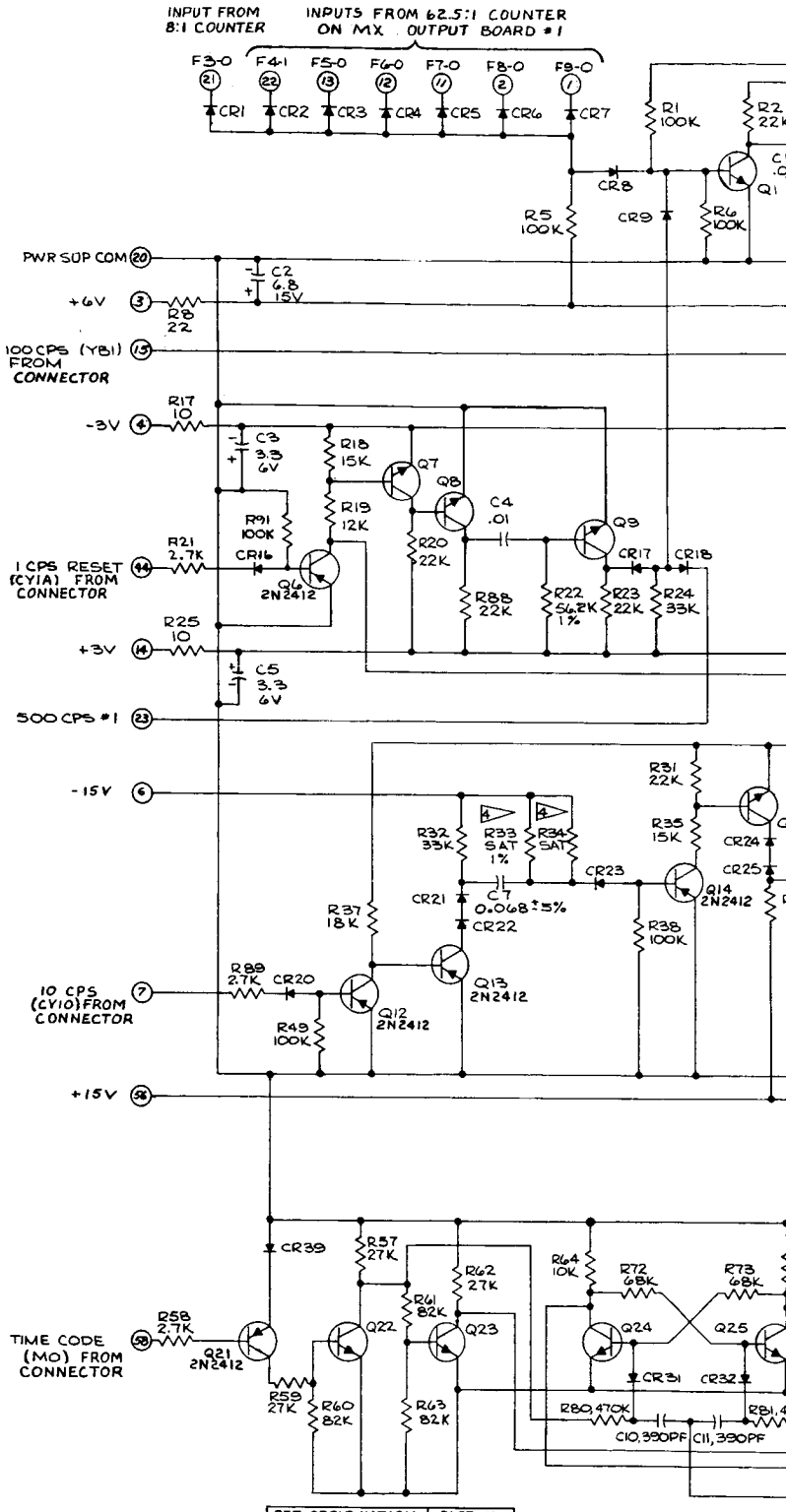


Figure I-18. Programmer Module No. 1, Schematic Diagram



REF DESIGNATION	PART NO.
CR1 - CR40	106933
Q6, Q12-Q14, Q20, Q21	102618
Q1-Q5, Q7-Q11, Q15-Q19 Q22-Q31	106943
R3, R43, R72	106780
R1, R2, R4-R21, R23-R32, R35-R39 R41, R42, R44-R92, R34	104115
C1, C4, C6, C9-C17	104238
C2, C3, C5, C18	100851
R33, R40	104608

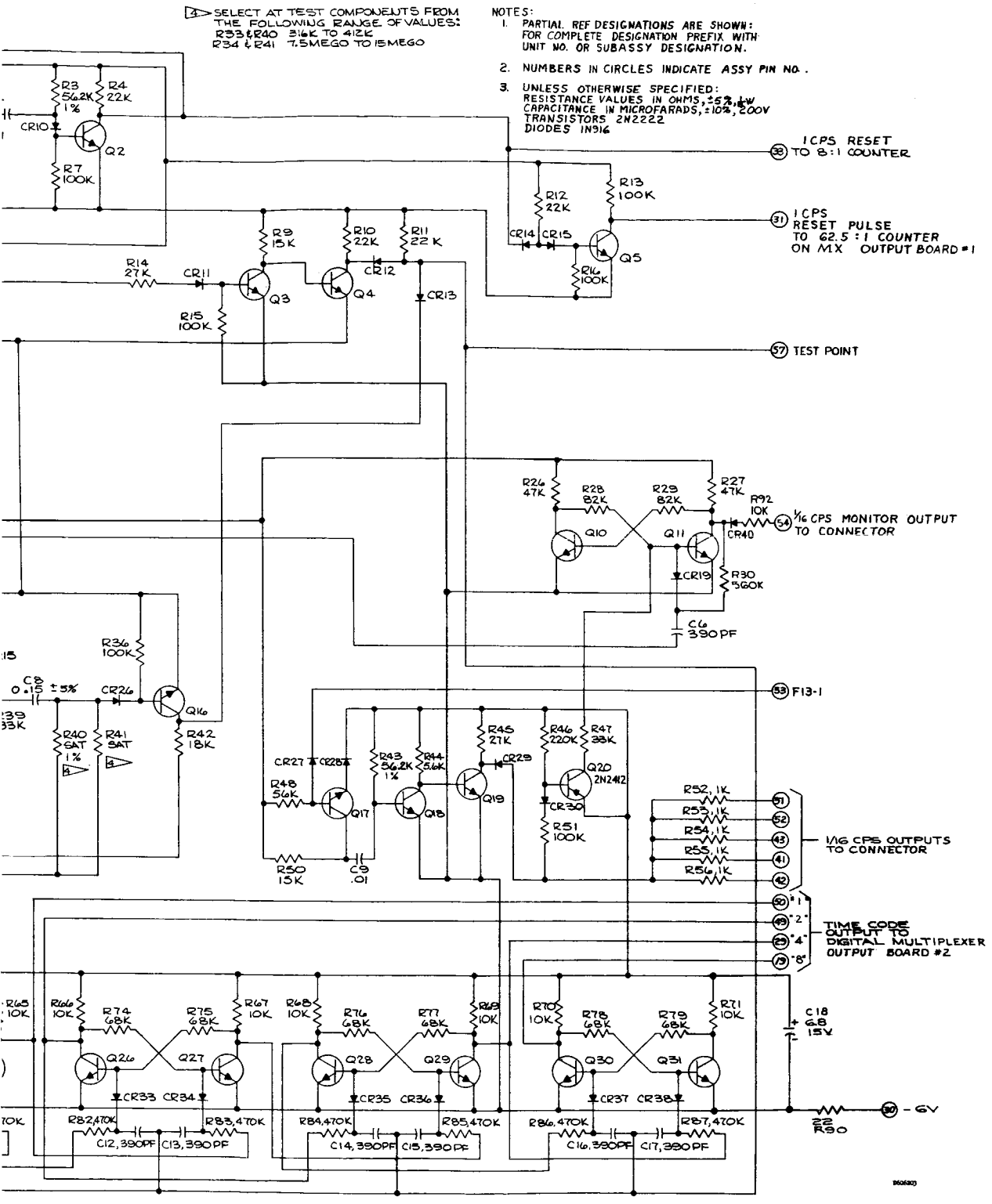
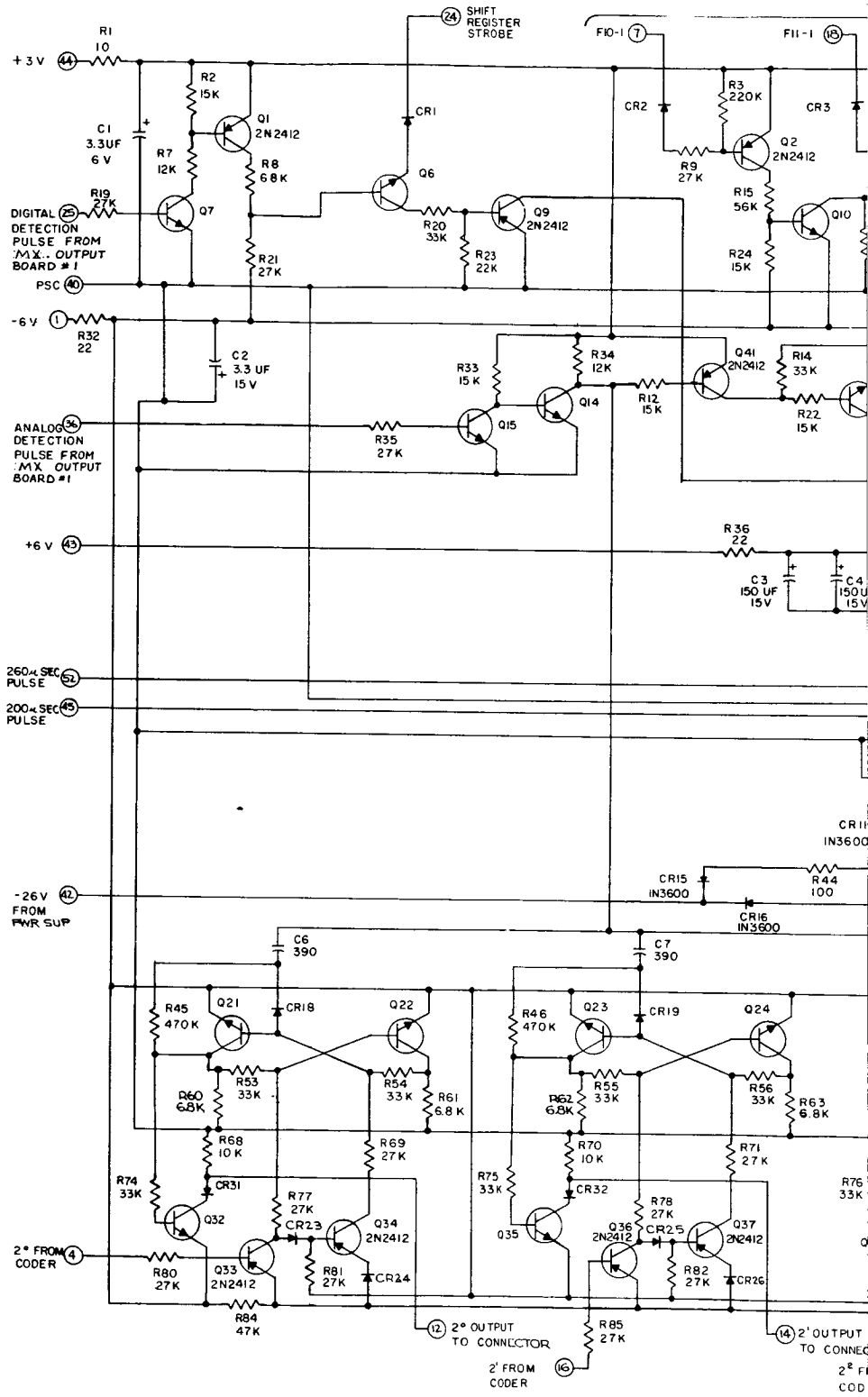


Figure 1-19. Programmer Module No. 2, Schematic Diagram

REF DESIGNATION	PART NO.
CR1-CR7, CR17-CR29 CR31-CR33	106933
CR8-CR16	110286
CR30	106934
C6, C7, C8	104238
Q16-Q19, Q28, Q31	106941
C34	106299

REF DESIGNATION	PART NO.
C2-C5, C1, C9	100851
Q1-Q5, Q9, Q34, Q39, Q40, Q41	102618
Q6-Q8, Q10-Q15, Q20-Q27, Q29-30, Q32, Q35, Q38	106943
RT1	110398
Q36, Q37, Q33	102618

REF DESI
R1 - R 87
R88
R89



GNATION	PART NO.
',R90,R91,R92	104115
	104608
	104602

NOTES:
1. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.
2. NUMBER IN CIRCLE INDICATES ASSY PIN NO.
3. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES IN OHMS, ±5%, 1/8WATT
   CAPACITANCE IN PICOFARADS ±10%, 200V
   DIODES ARE IN916
   TRANSISTORS 2N2222

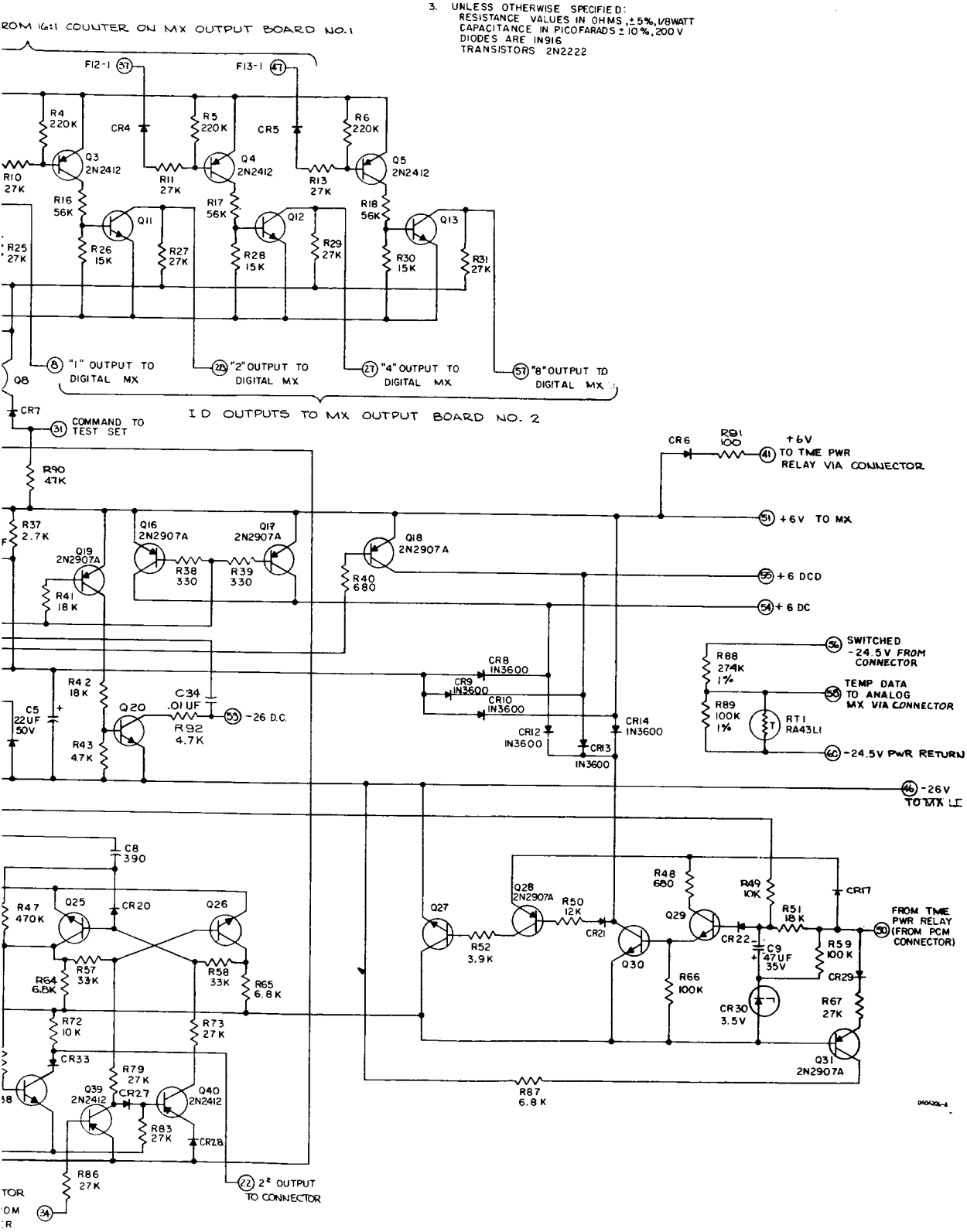
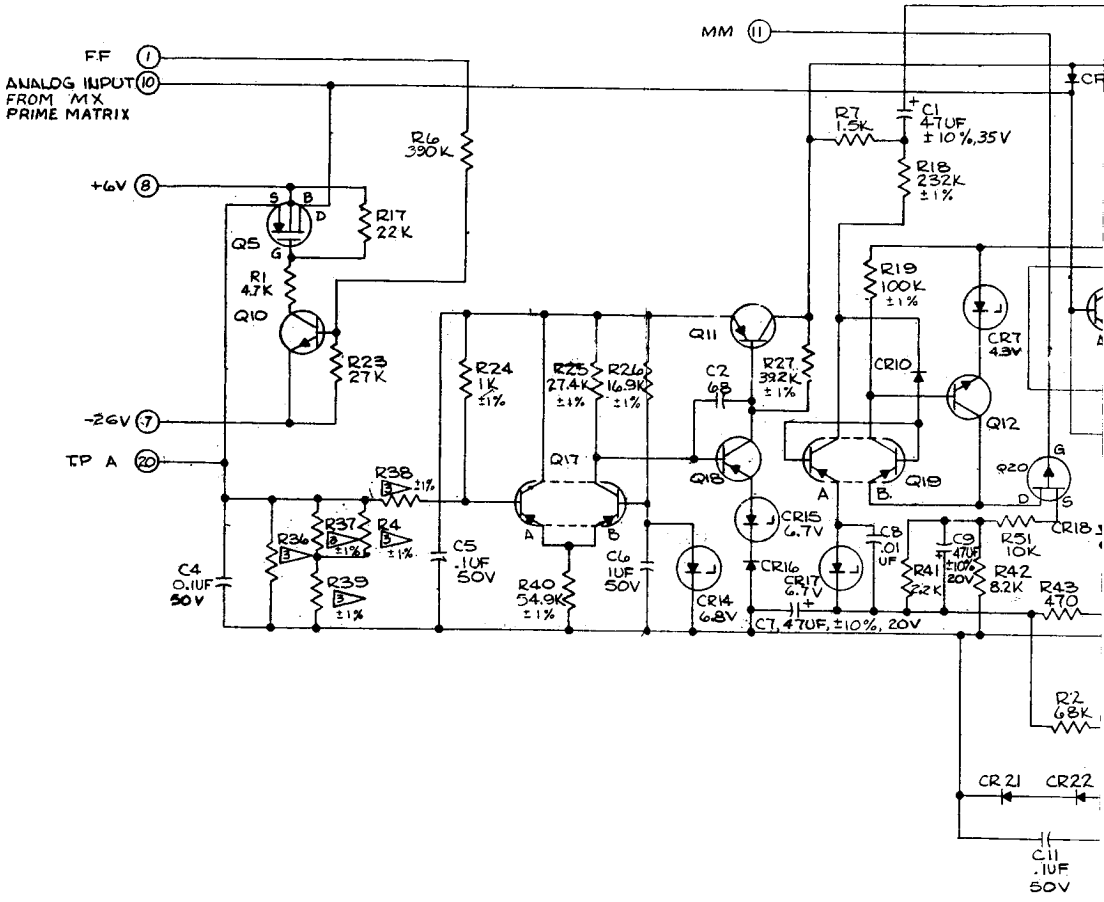


Figure 1-20. Programmer Module No. 3, Schematic Diagram


F.F
ANALOG INPUT FROM MX PRIME MATRIX
+6V
-26V
TP A
MM
R6 390K
R17 22K
Q5
R1 4.7K
Q10
R23 27K
R24 1K ±1%
R25 27.4K ±1%
R26 16.9K ±1%
R38 ±1%
R37 ±1%
R4 ±1%
R36
R39 ±1%
C4 0.1UF 50V
C5 .1UF 50V
Q17
R40 54.9K ±1%
C6 1UF 50V
Q11
C2 68
Q18
CR14 6.8V
R27 392K ±1%
CR15 6.7V
CR16
CR17 6.7V
CT, 47UF, ±10%, 20V
R7 1.5K
C1 47UF ±10%, 35V
R18 232K ±1%
R19 100K ±1%
CR10
Q19
CR7 4.3V
Q12
Q20
CR18
R51 10K
CB .01 UF
C9 47UF ±10% 20V
R41 2.2K
R42 8.2K
R43 470
R2 68K
CR21
CR22
C11 .1UF 50V

NOTES:

1. PARTIAL REF DES ARE SHOWN; FOR COMPLETE DES, PREFIX WITH UNIT NO. OR SUB-ASSY DES.

2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ⅛ W ±5% TOL; CAPACITANCE VALUES ARE IN PICOFARADS ±10% TOL, 200V

3. SELECT AT TEST COMPONENTS
RANGE OF VALUES:
R36 VALUES IN MEGO— 1, 1.5, 2, 2.4, 2.7, 3, 3.3, 3.6, 3.9, 4.3, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1, 10.
R32 - 10Ω THRU 220Ω
R28 - 10, 6, 7, 8, 10, 18.2K, 20K, 22.1K, 24.3K, 27.4K, 10, 4, 11.5, 33K, 39K, 47K, 62K, 91K, 120K, 150K, 270K.
R4, R37 - 5.23 K, 5.36K, 5.49K, 5.62K, 5.76K, 5.90K, 6.04K, 6.19K, 6.34K, 6.49K, 6.65K, 6.81K.
R39 - 49.9, 63.4, 90.9, 121, 143, 169, 187, 205 OHMS.
R38 - 221, 232, 243 OHMS

4. NUMBERS IN CIRCLES INDICATE ASSY PIN NO.

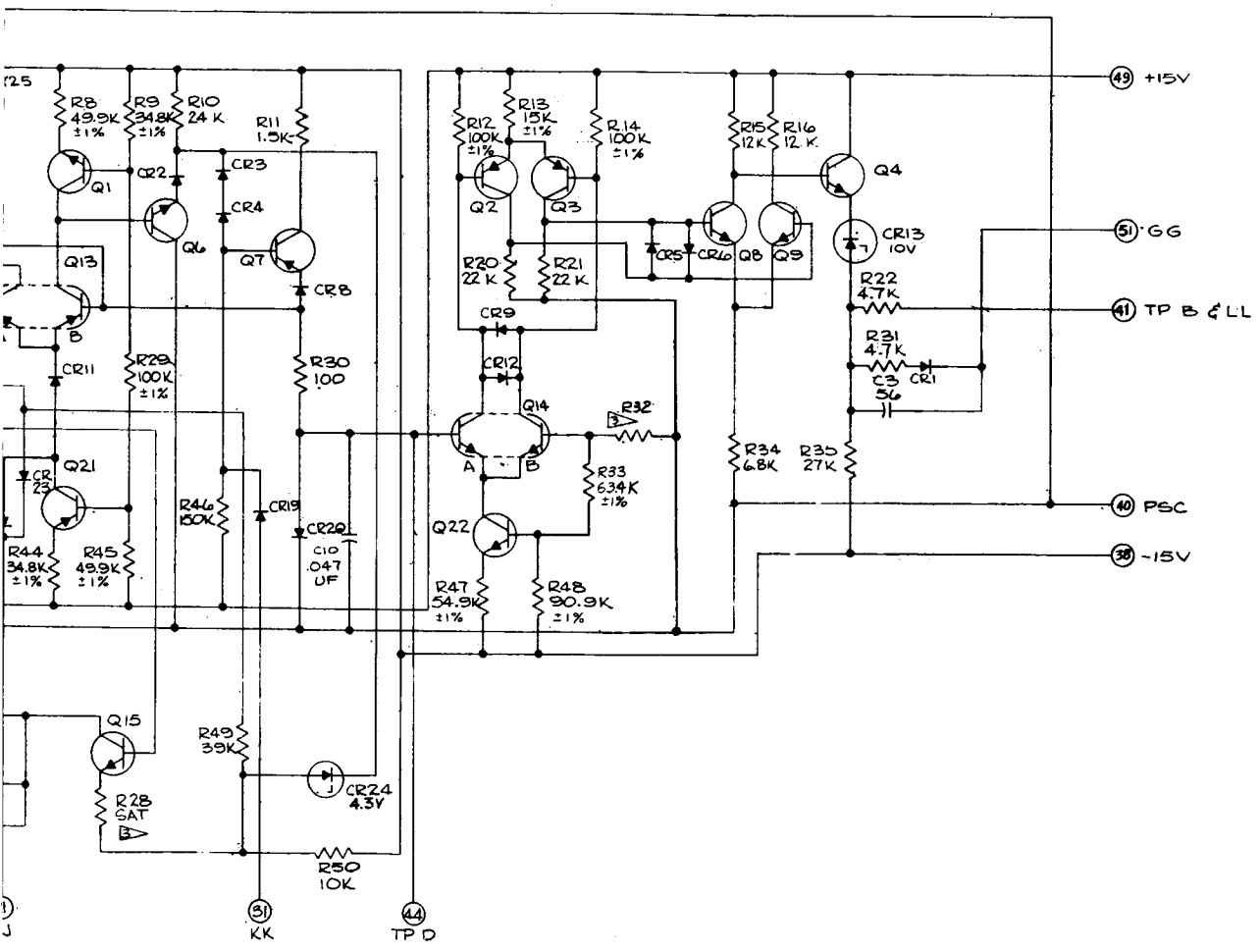
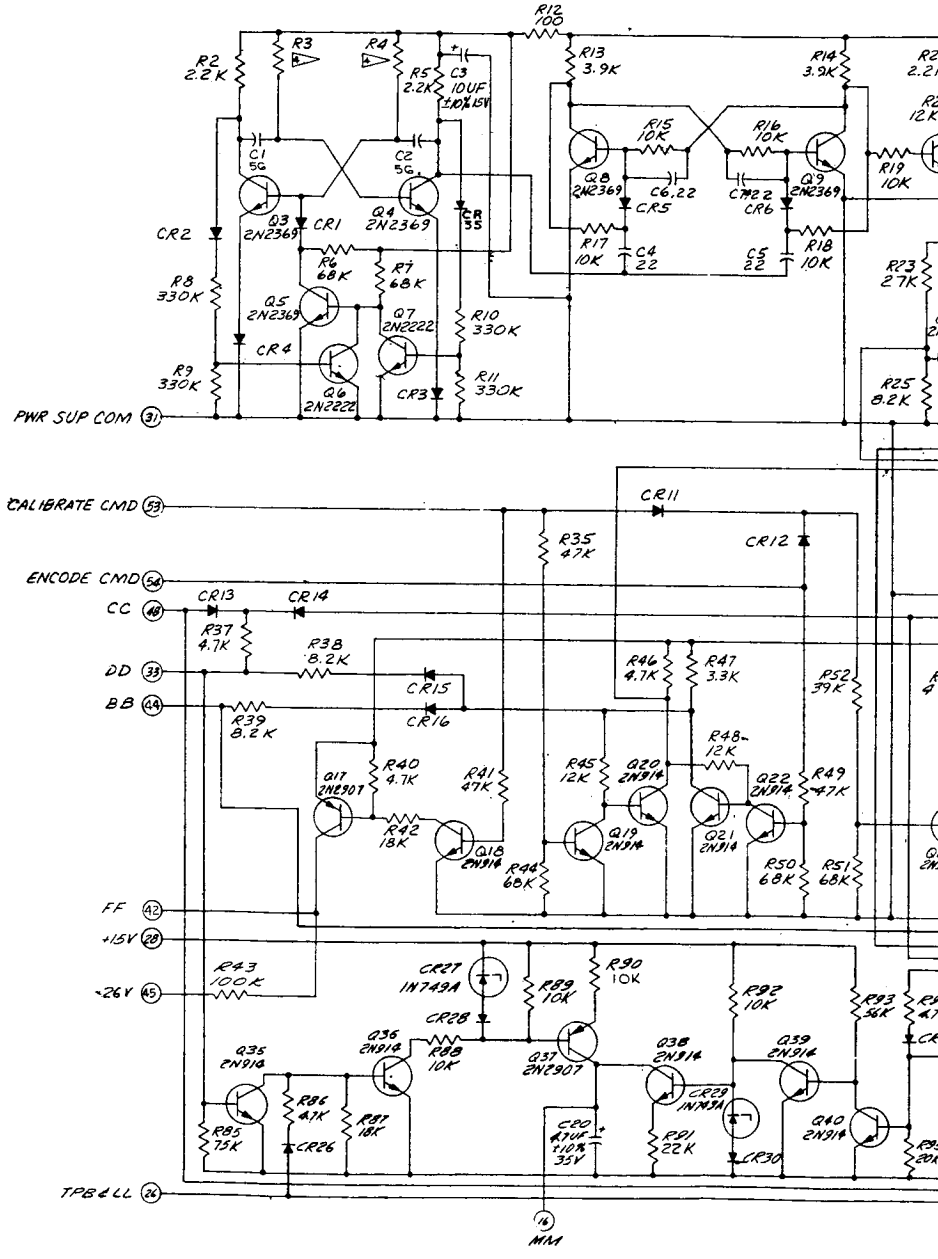


Figure I-21. Coder Module No. 1, Schematic Diagram


R12 100
R2 2.2K
R3
R4
R5 2.2K
C3 10UF ±10% 15V
R13 3.9K
R14 3.9K
R15 10K
R16 10K
C1 5G
C2 5G
Q3 2N2369
Q4 2N2369
CR1
CR2
CR35
Q8 2N2369
Q9 2N2369
C6 22
C7 22
CR5
CR6
R17 10K
C4 22
C5 22
R18 10K
R19 10K
R6 68K
R7 68K
R8 330K
Q5 2N2369
Q7 2N2222
R10 330K
CR4
R9 330K
Q6 2N2222
CR3
R11 330K
R23 27K
R25 8.2K
PWR SUP COM 31
CALIBRATE CMD 53
CR11
R35 47K
CR12
ENCODE CMD 54
CC 48
CR13
CR14
R37 4.7K
R38 8.2K
DD 33
BB 44
CR15
CR16
R39 8.2K
R46 4.7K
R47 3.3K
R52 39K
R40 4.7K
Q17 2N2907
R41 47K
R45 12K
Q20 2N914
R48 12K
Q22 2N914
R49 47K
R42 18K
Q18 2N914
Q19 2N914
Q21 2N914
R44 68K
R50 68K
R51 68K
FF 42
+15V 28
-26V 45
R43 100K
CR27 1N749A
R89 10K
R90 10K
R92 10K
R93 56K
CR28
Q35 2N914
Q36 2N914
R88 10K
Q37 2N2907
Q38 2N914
Q39 2N914
CR29 1N749A
R85 75K
R86 47K
R87 10K
CR26
C20 470K ±10% 35V
R91 22K
CR30
Q40 2N914
TPB&LL 26
16 MM

1-23-1

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ±5% TOL, 1/8 WATT, CAPACITANCE VALUES ARE IN PICOFARADS, ± 10%, 200 VOLTS, DIODES ARE IN916.
2. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION(S).
3. NUMBERS IN CIRCLES INDICATES ASSY PIN NUMBERS.

SELECT AT TEST COMPONENTS RANGE OF VALUES, R3, R4, 10.5K, 11.3K, 12.1K, 13.7K.

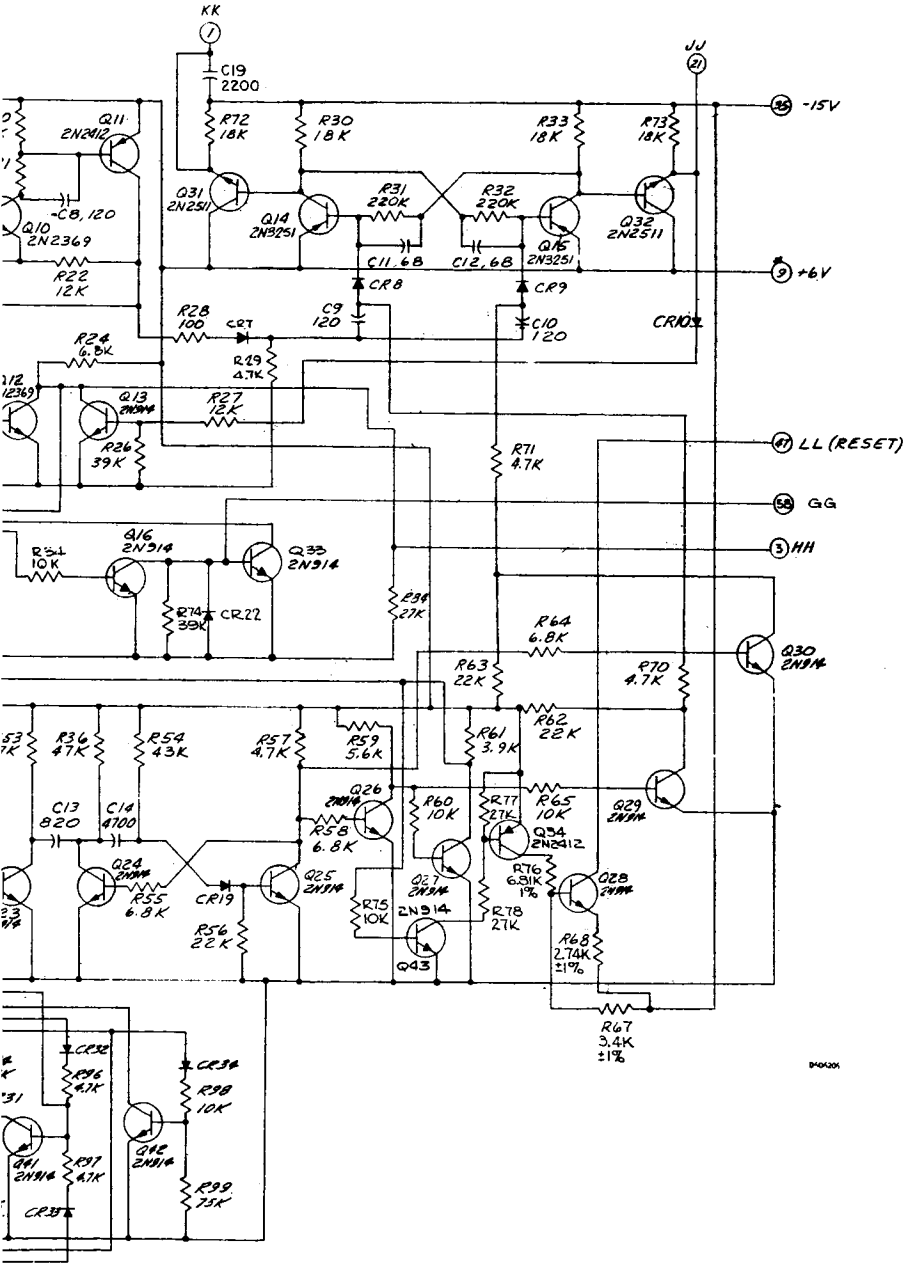
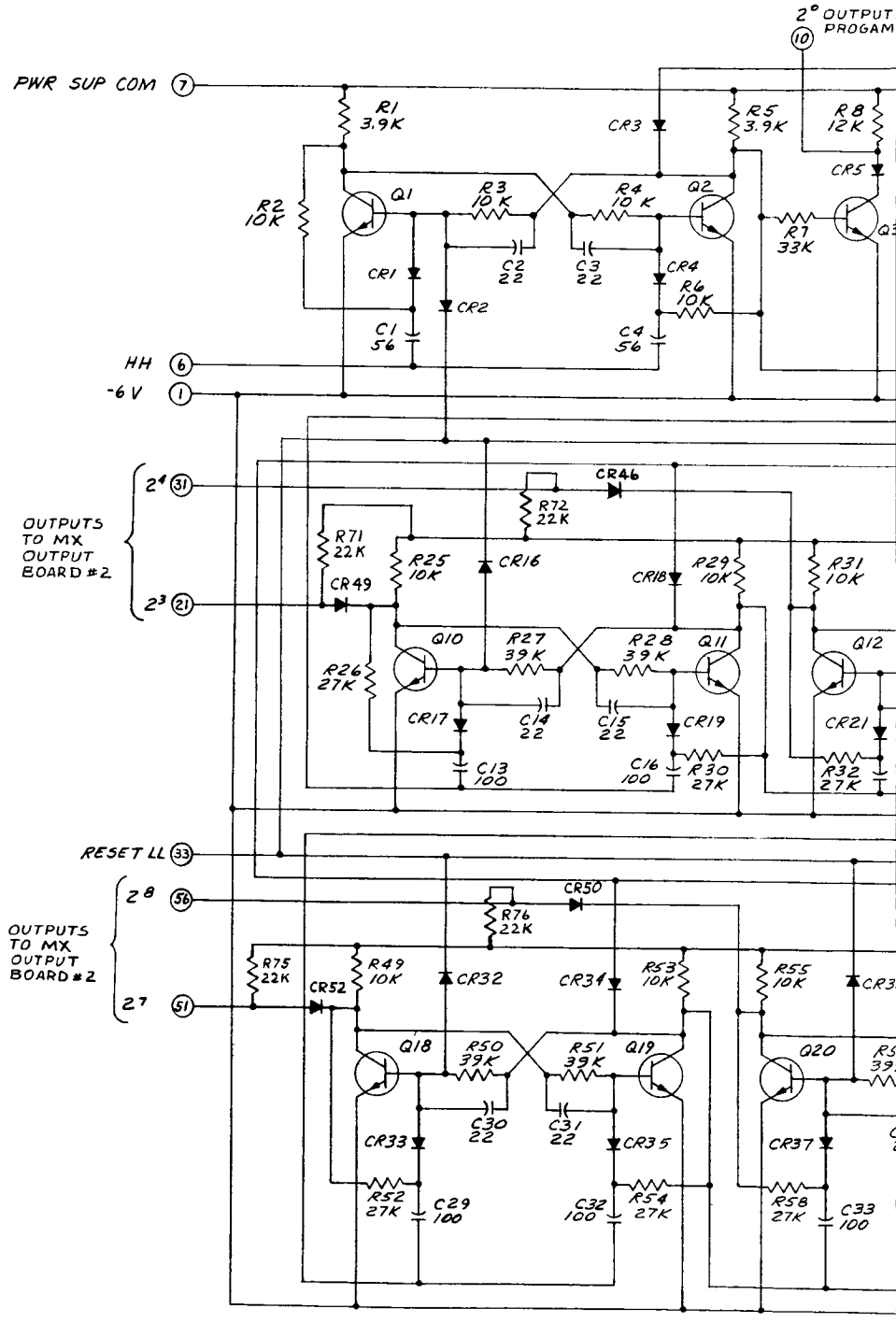


Figure 1-22. Coder Module No. 2, Schematic Diagram

REF DESIGNATION	PART NO.
Q1 THRU Q9	101936
CR1 THRU 44, 46-52	106933
CR 45	106934
R1 THRU R77	104115
C1 THRU C40	104238
Q10 THRU Q25	106943



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ±5% TOLERANCE, ⅛ WATT; CAPACITANCE VALUES ARE IN PICOFARADS, ±10% TOLERANCE, 200 VOLTS.
2. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION(S).
3. NUMBERS IN CIRCLES INDICATES ASSY PIN NUMBERS.

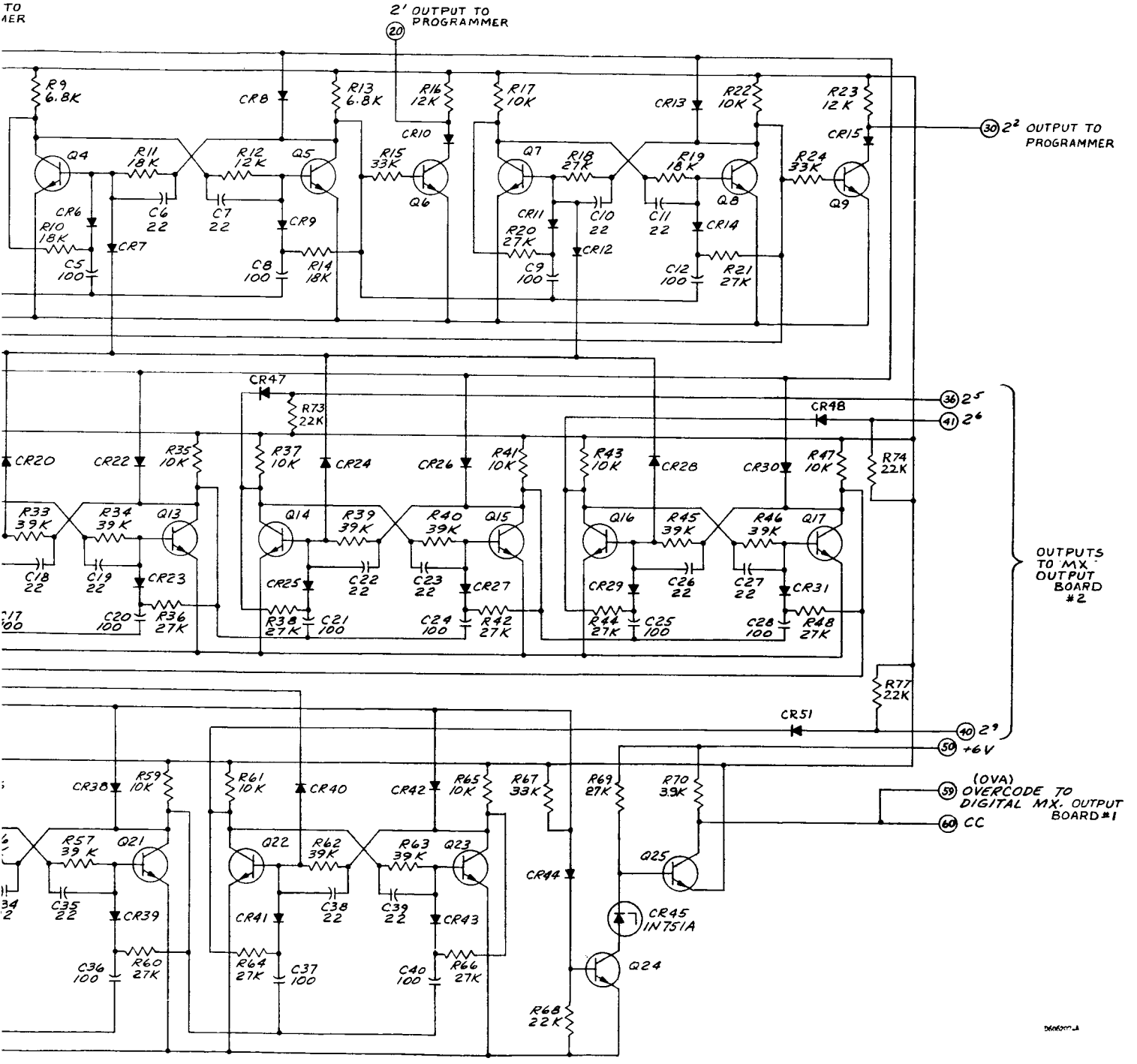
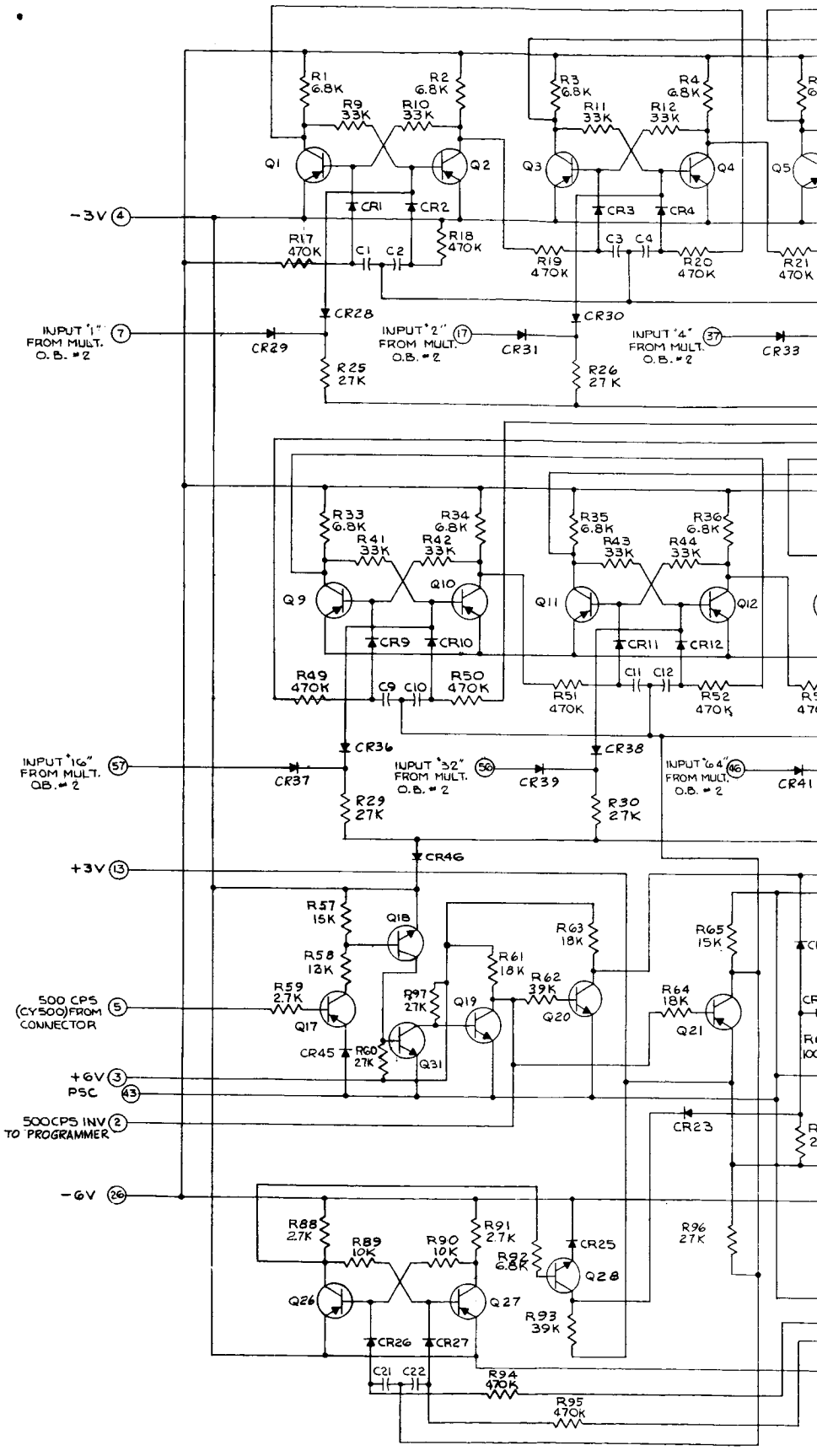


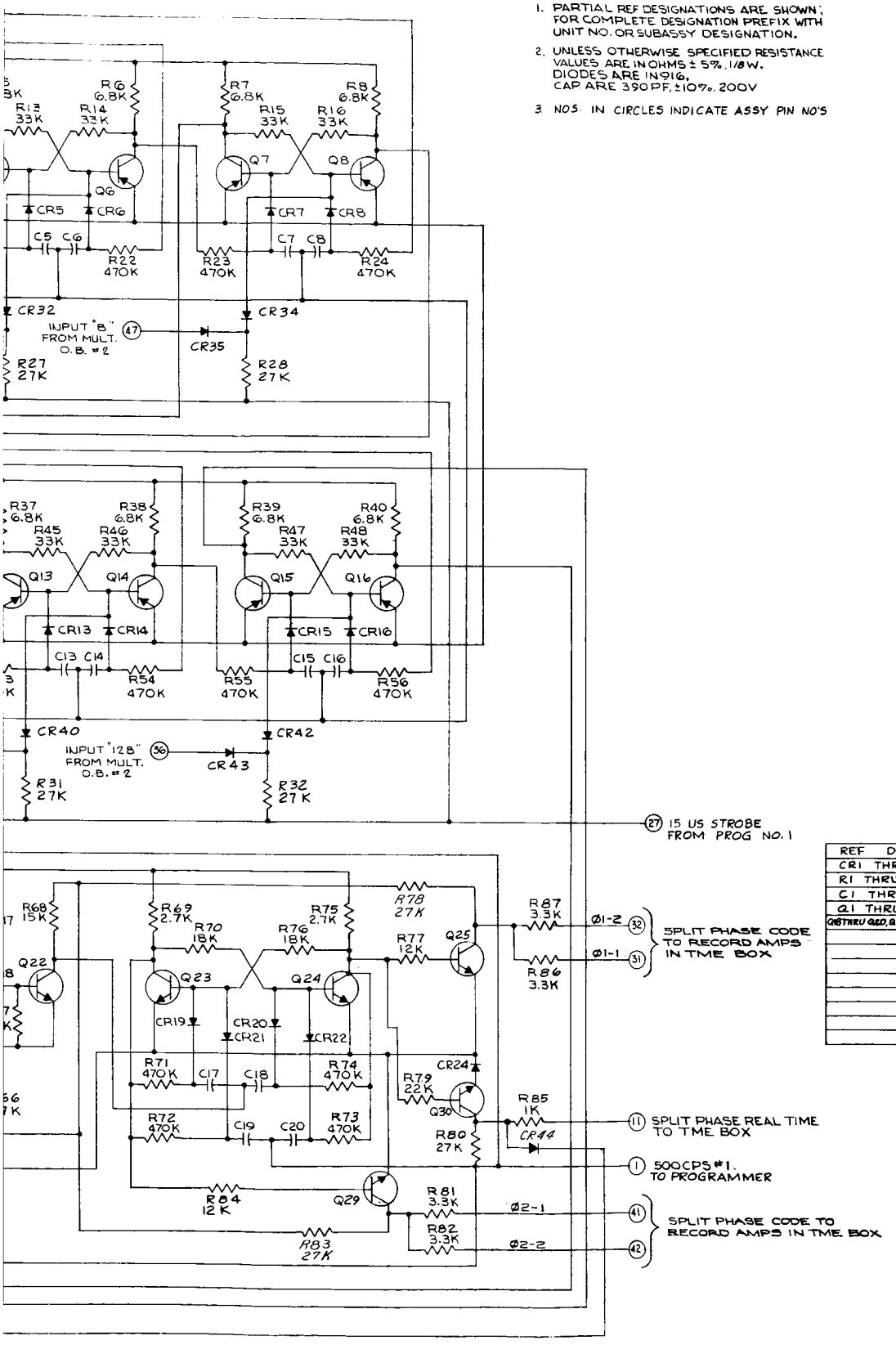
Figure I-23. Coder Module No. 3, Schematic Diagram


R1 6.8K
R2 6.8K
R9 33K
R10 33K
Q1
Q2
CR1
CR2
R17 470K
C1
C2
R18 470K
R3 6.8K
R4 6.8K
R11 33K
R12 33K
Q3
Q4
CR3
CR4
C3
C4
R19 470K
R20 470K
Q5
R21 470K
-3V 4
INPUT "1" FROM MULT. O.B. #2 7
CR29
CR28
R25 27K
INPUT "2" FROM MULT. O.B. #2 17
CR31
CR30
R26 27K
INPUT "4" FROM MULT. O.B. #2 37
CR33
R33 6.8K
R34 6.8K
R41 33K
R42 33K
Q9
Q10
CR9
CR10
R49 470K
C9
C10
R50 470K
R35 6.8K
R36 6.8K
R43 33K
R44 33K
Q11
Q12
CR11
CR12
C11
C12
R51 470K
R52 470K
INPUT "16" FROM MULT. OB. #2 57
CR37
CR36
R29 27K
INPUT "32" FROM MULT. O.B. #2 56
CR39
CR38
R30 27K
INPUT "64" FROM MULT. O.B. #2 46
CR41
+3V 13
CR46
R57 15K
Q18
R58 12K
R59 2.7K
Q17
500 CPS (CY500) FROM CONNECTOR 5
R61 18K
R63 18K
R62 39K
Q19
Q20
R97 2.7K
CR45
R60 2.7K
Q31
R65 15K
R64 18K
Q21
+6V 3
PSC 43
500CPS INV 2 TO PROGRAMMER
CR23
-6V 26
R88 2.7K
R89 10K
R90 10K
R91 2.7K
R92 6.8K
CR25
Q28
Q26
Q27
R93 39K
CR26
CR27
C21
C22
R94 470K
R95 470K
R96 27K

1-25-1

NOTES:

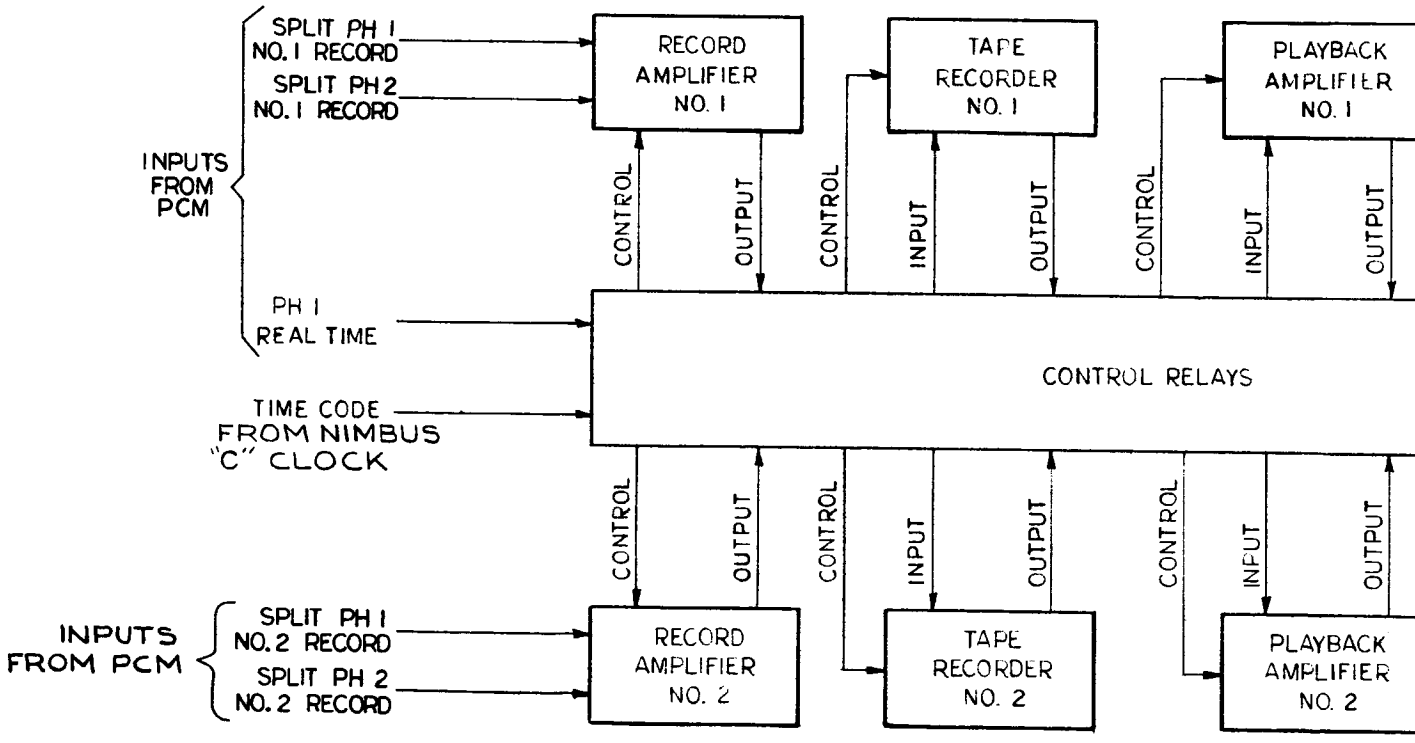
1. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.
2. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS ± 5%, 1/8W. DIODES ARE IN916, CAP. ARE 390PF, ±10%, 200V
3. NOS. IN CIRCLES INDICATE ASSY PIN NO'S



REF DESIGNATION	PART NO.
CR1 THRU CR46	106933
R1 THRU R97	104115
C1 THRU C22	104238
Q1 THRU Q17, Q21, Q26, Q27	102618
Q18 THRU Q20, Q22 THRU Q25, Q28, 29, 30, 31	106943

Figure 1-24. Output Register and Split-Phase Converter, Schematic Diagram

SATELLITE TEMP
SENSOR - 2



NOTES:

1. THIS MONITOR POINT MUST BE CONNECTED INTO AN ANALOG CHANNEL IF USED.
2. THESE MONITOR POINTS MUST BE CONNECTED INTO A DIGITAL CHANNEL IF USED

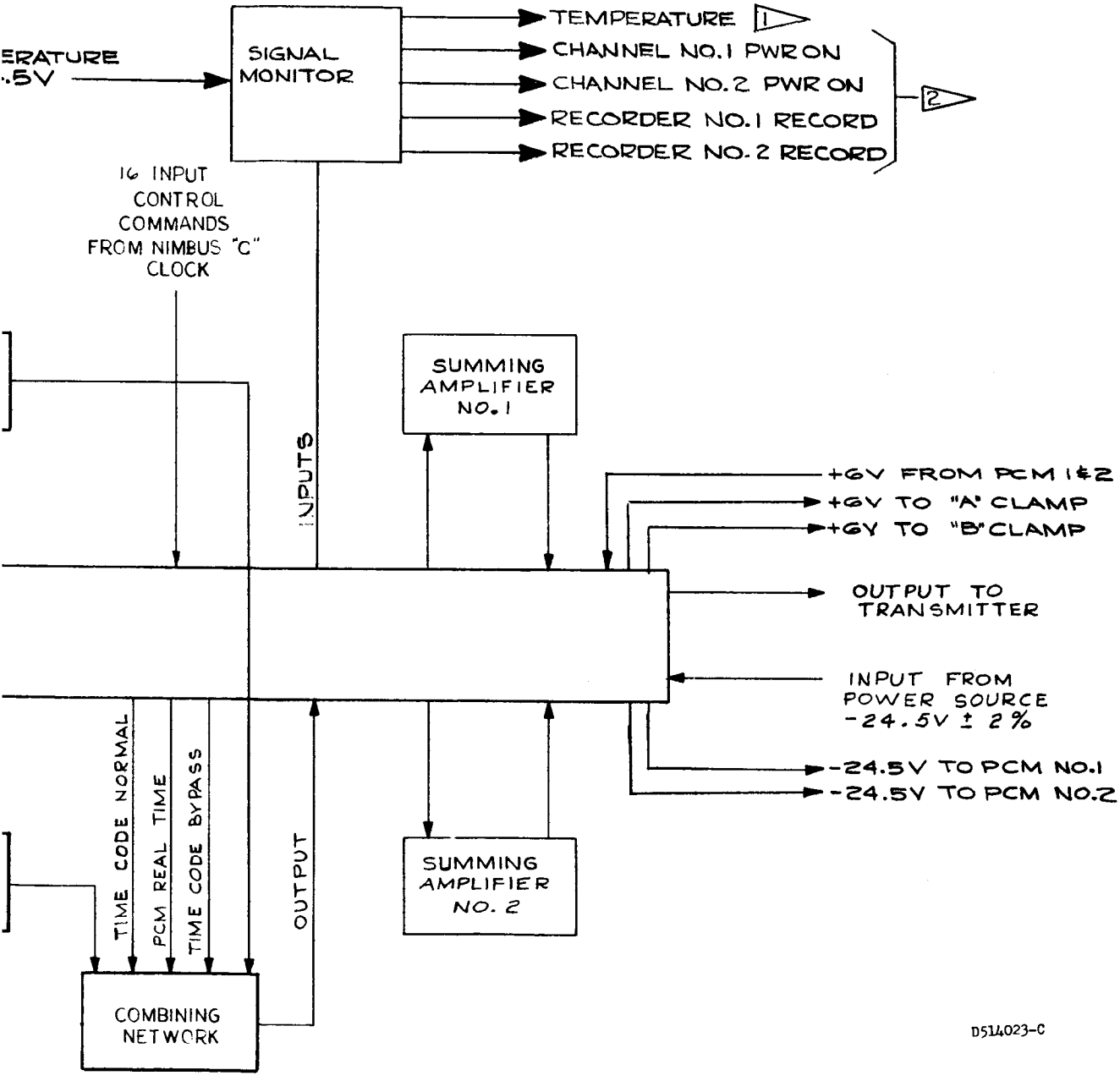
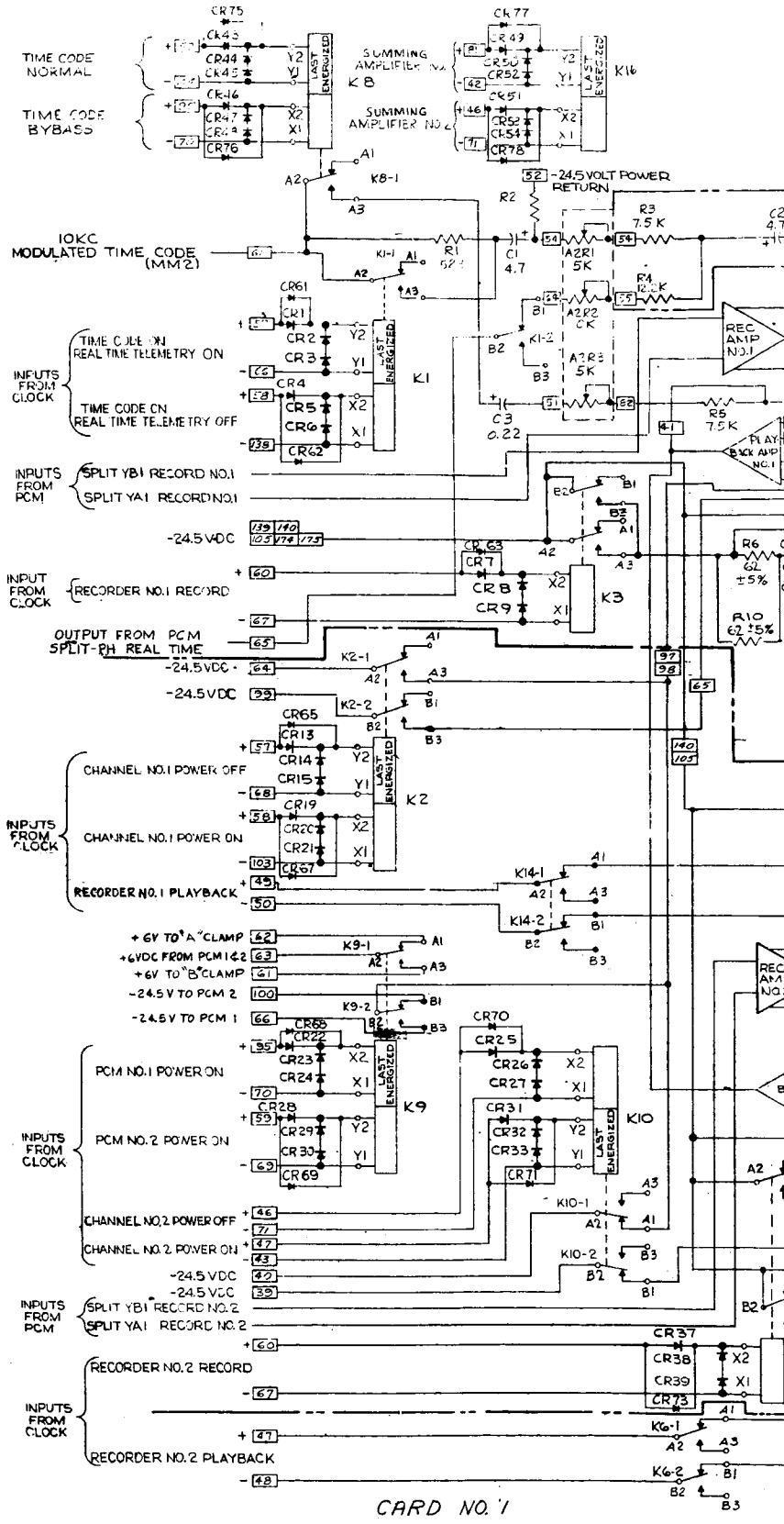


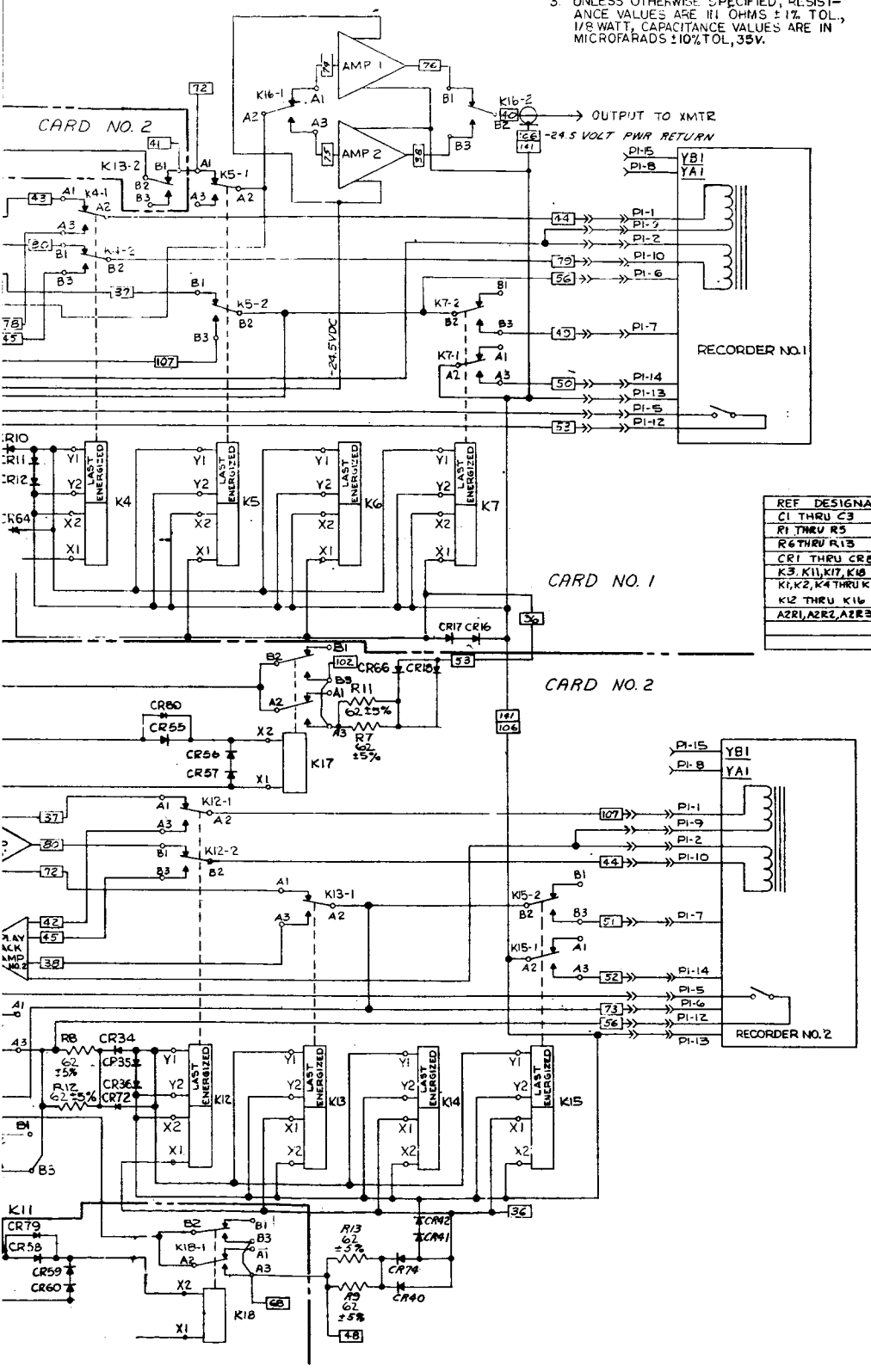
Figure 1-25. TME Unit, Block Diagram


TIME CODE NORMAL
TIME CODE BYBASS
SUMMING AMPLIFIER NO.1
SUMMING AMPLIFIER NO.2
K8
K16
-24.5 VOLT POWER RETURN
10KC MODULATED TIME CODE (MM'2)
INPUTS FROM CLOCK
TIME CODE ON REAL TIME TELEMETRY ON
TIME CODE ON REAL TIME TELEMETRY OFF
K1
INPUTS FROM PCM
SPLIT YB1 RECORD NO.1
SPLIT YA1 RECORD NO.1
-24.5 VDC
INPUT FROM CLOCK
RECORDER NO.1 RECORD
K3
OUTPUT FROM PCM SPLIT-PH REAL TIME
-24.5 VDC
CHANNEL NO.1 POWER OFF
CHANNEL NO.1 POWER ON
RECORDER NO.1 PLAYBACK
K2
+6V TO "A" CLAMP
+6VDC FROM PCM 1&2
+6V TO "B" CLAMP
-24.5 V TO PCM 2
-24.5 V TO PCM 1
PCM NO.1 POWER ON
PCM NO.2 POWER ON
K9
K10
CHANNEL NO.2 POWER OFF
CHANNEL NO.2 POWER ON
SPLIT YB1 RECORD NO.2
SPLIT YA1 RECORD NO.2
RECORDER NO.2 RECORD
RECORDER NO.2 PLAYBACK
K6
REC AMP NO.1
PLAY BACK AMP NO.1
LAST ENERGIZED

CARD NO. 1

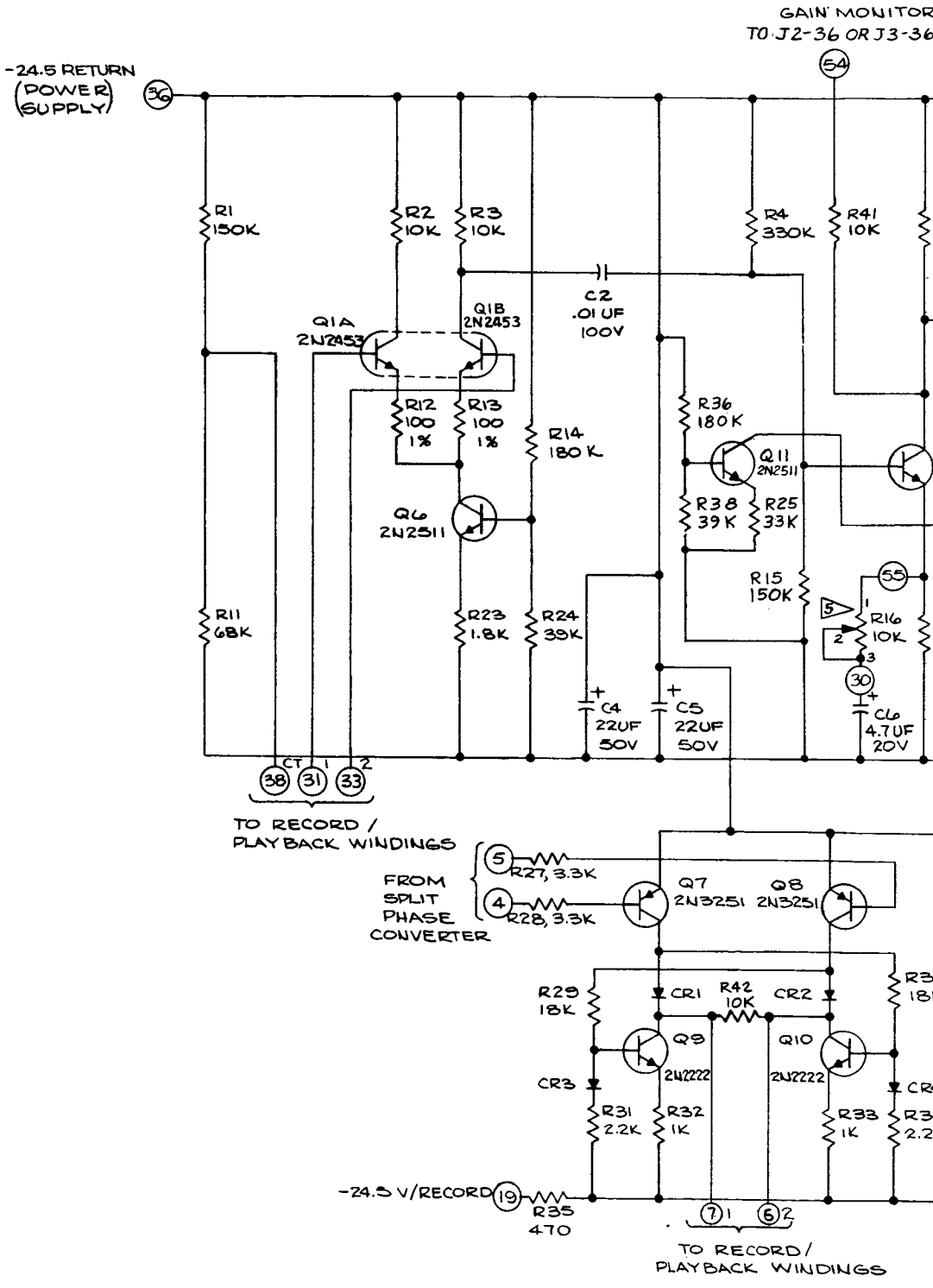
NOTES:

1. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.
2. NUMBERS IN RECTANGLES REPRESENT PRINTED CIRCUIT BOARD TERMINATIONS
3. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS ±1% TOL., 1/8 WATT, CAPACITANCE VALUES ARE IN MICROFARADS ±10% TOL, 35V.



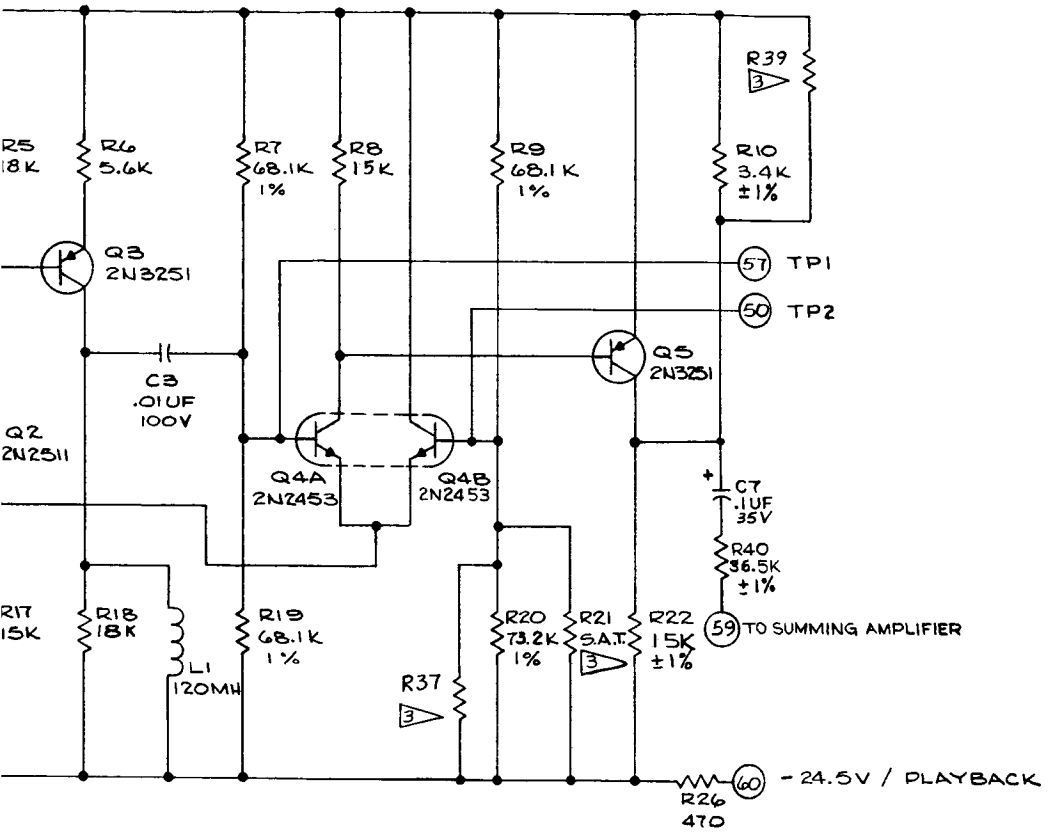
REF DESIGNATION	PART NO.
C1 THRU C3	100851
R1 THRU R5	106780
R6 THRU R13	104115
CR1 THRU CR80	106933
K3, K11, K17, K18	110428
K1, K2, K4 THRU K10, K12 THRU K16	110429
A2R1, A2R2, A2R3	110289

Figure 1-26. TME Unit, Schematic Diagram


GAIN MONITOR
TO J2-36 OR J3-36
54
-24.5 RETURN
(POWER SUPPLY)
36
R1
150K
R2
10K
R3
10K
R4
330K
R41
10K
C2
.01 UF
100V
Q1A
2N2453
Q1B
2N2453
R12
100
1%
R13
100
1%
R14
180 K
R36
180 K
Q11
2N2511
R38
39 K
R25
33K
Q6
2N2511
R15
150K
55
R16
10K
30
C6
4.7UF
20V
R11
68K
R23
1.8K
R24
39K
C4
22UF
50V
C5
22UF
50V
38
31
33
CT
1
2
TO RECORD /
PLAYBACK WINDINGS
FROM
SPLIT
PHASE
CONVERTER
5
4
R27, 3.3K
R28, 3.3K
Q7
2N3251
Q8
2N3251
R29
18K
CR1
R42
10K
CR2
Q9
2N2222
Q10
2N2222
CR3
R31
2.2K
R32
1K
R33
1K
-24.5 V/RECORD
19
R35
470
7
6
TO RECORD/
PLAYBACK WINDINGS

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ±5% TOLERANCE, $\frac{1}{8}$ WATT. TOLERANCE ON CAPACITORS IS ±10%.
2. UNLESS OTHERWISE SPECIFIED, DIODES ARE IN916.
3. SELECT AT TEST COMPONENTS RANGE OF VALUES R21, 560K TO 10 M, R37, 10MEG TO 22 M, R39, 10K TO 100K.
4. PARTIAL REF DESIGNATIONS ARE SHOWN, FOR COMPLETE DES PREFIX WITH UNIT NO., OR SUBASSY DESIGNATION.
5. R16 IS ACTUALLY ON FRONT PANEL AS A2R4 FOR CHANNEL #1 AND A2R5 FOR CHANNEL #2

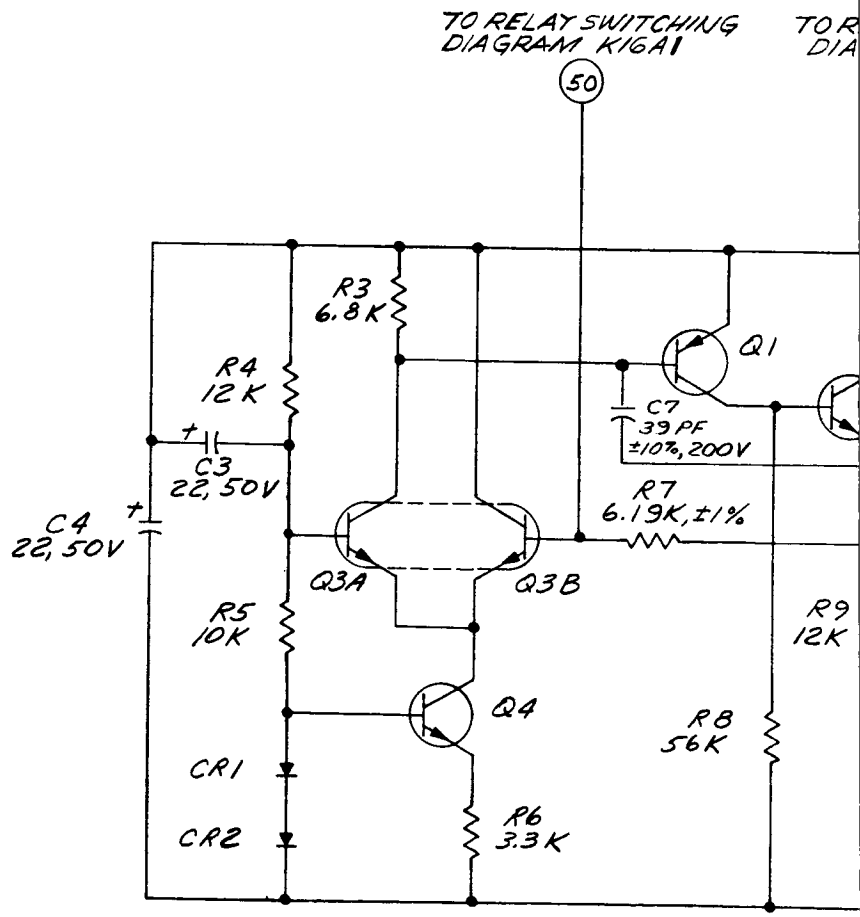


REF DESIGNATION	PART NO.
R1 THRU R6, R8, R42, R11, R14, R15 R17, R18, R21, R23 THRU R39, 41	104115
R7, R9, R12, R10, R13, R19, R20, R22, 40	106780
C2 & C3	104238
C1, C4, C5, C6 & C7	100851
CR1 THRU CR4	106933
Q1 & Q4	106940
Q2, Q6 & Q11	106942
Q3, Q5, Q7 & Q8	110121
Q9 & Q10	106943
R16	110289-010
L1	110290-001

D515612-A

Figure 1-27. Record and Playback Amplifiers, Schematic Diagram

REF DESIGNATION	PART NO.
Q1, Q5	110121
Q2, Q4, Q6, Q8	106942
Q3, Q7	106940
CR1 THRU CR4	106933
C3 THRU C6	100851
R7, R14	106780
R3-6, R8-13, R15-18	104115
C7, C8	104238



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHM'S, ±5% TOL., 1/8 WATT, CAPACITANCE VALUES ARE IN MICROFARADS, ±10% TOL.
2. NO'S. IN CIRCLES INDICATES ASSY PIN NO'S.
3. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION(S).

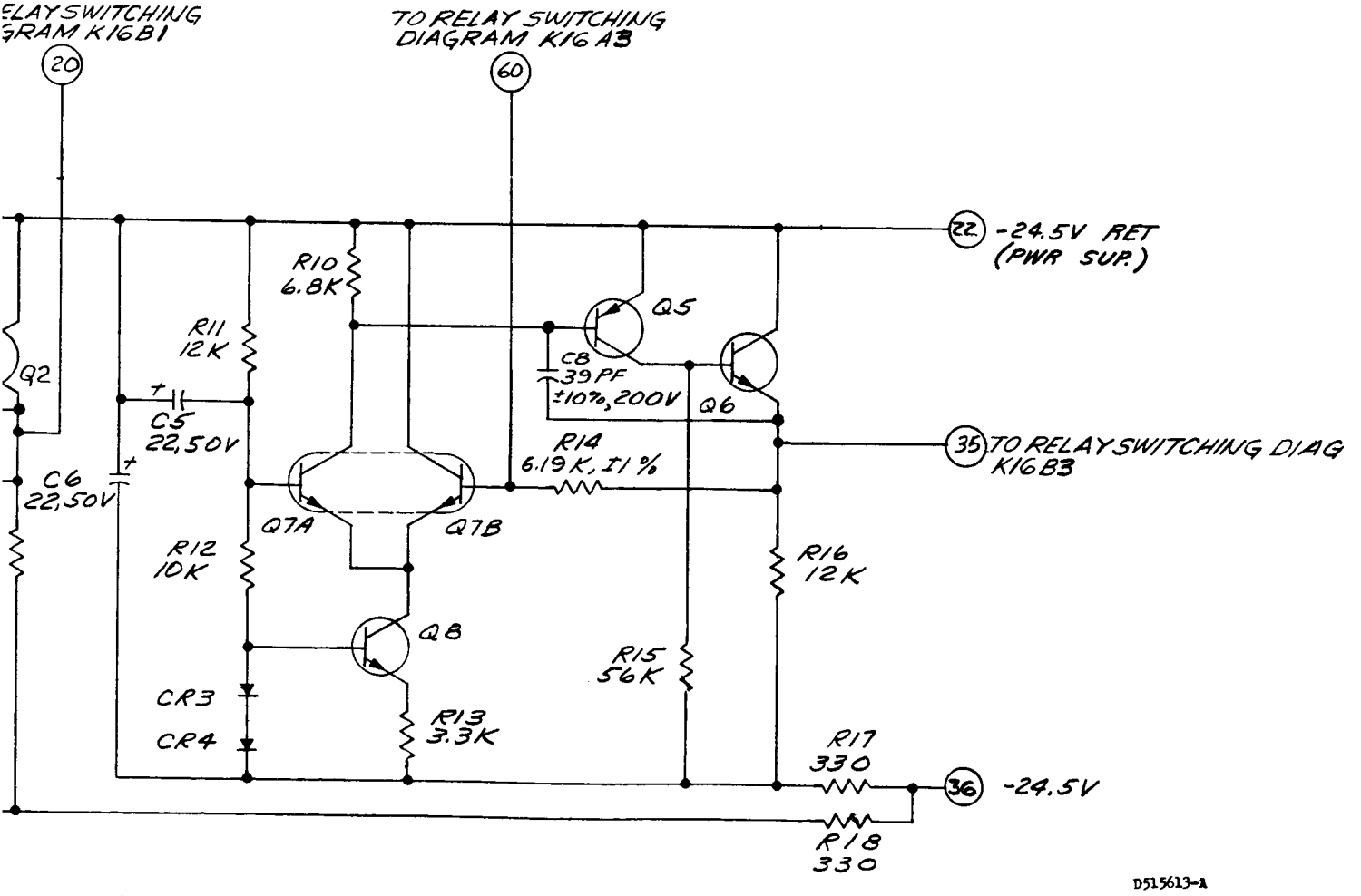


Figure 1-28. Summing Amplifier, Schematic Diagram

REF DESIGNATION	PART NO.
R3-R10	104115
RT1	110398
R1	104608
R2	104602

NOTES:

1. PARTIAL REF DES ARE SHOWN; FOR COMPLETE DES. PREFIX WITH UNIT NO. OR SUB-ASSY DES.
2. NUMBER IN CIRCLE INDICATES ASSY PIN NO.
3. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES IN OHMS, ±5%
   1/8 WATT.

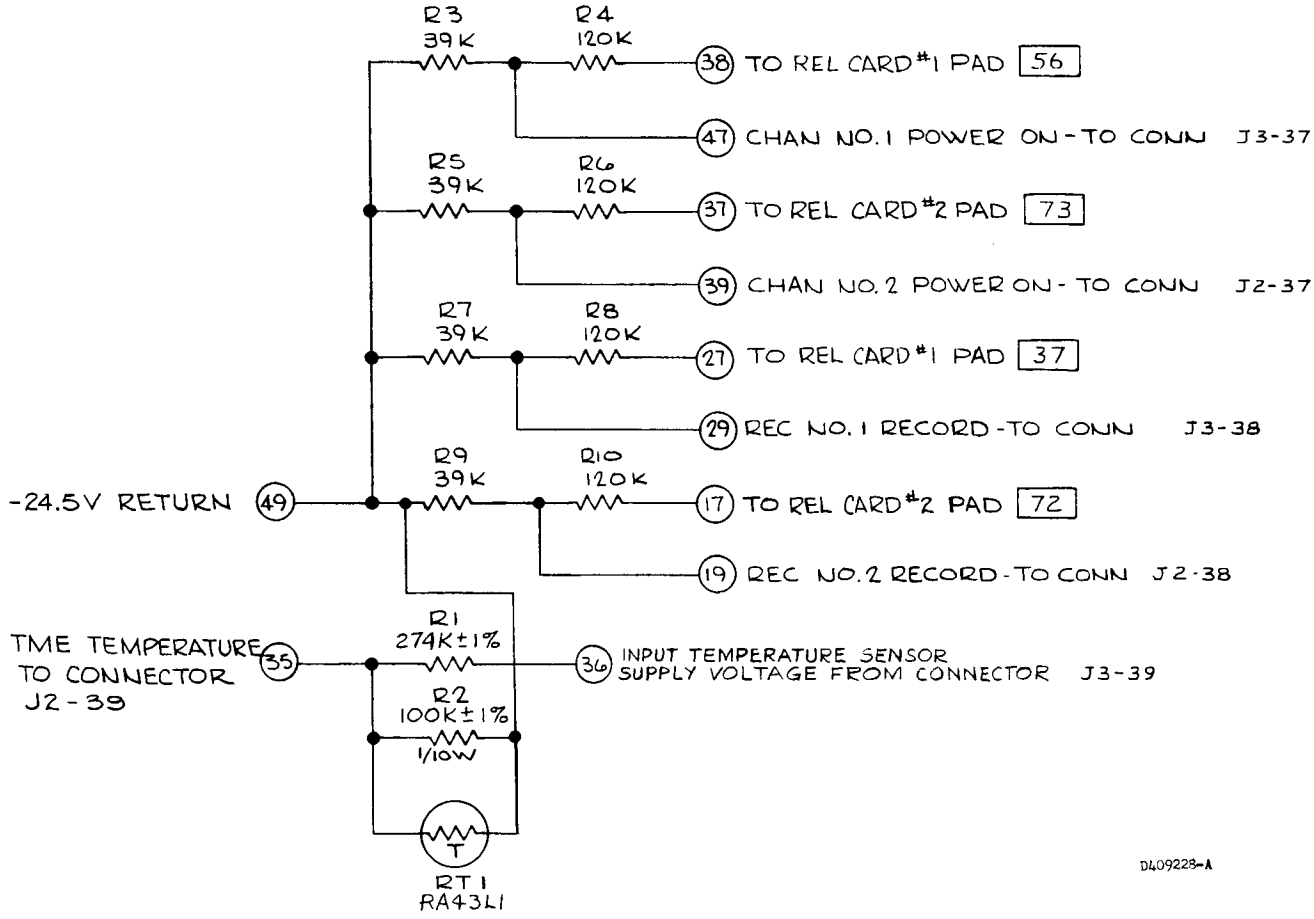
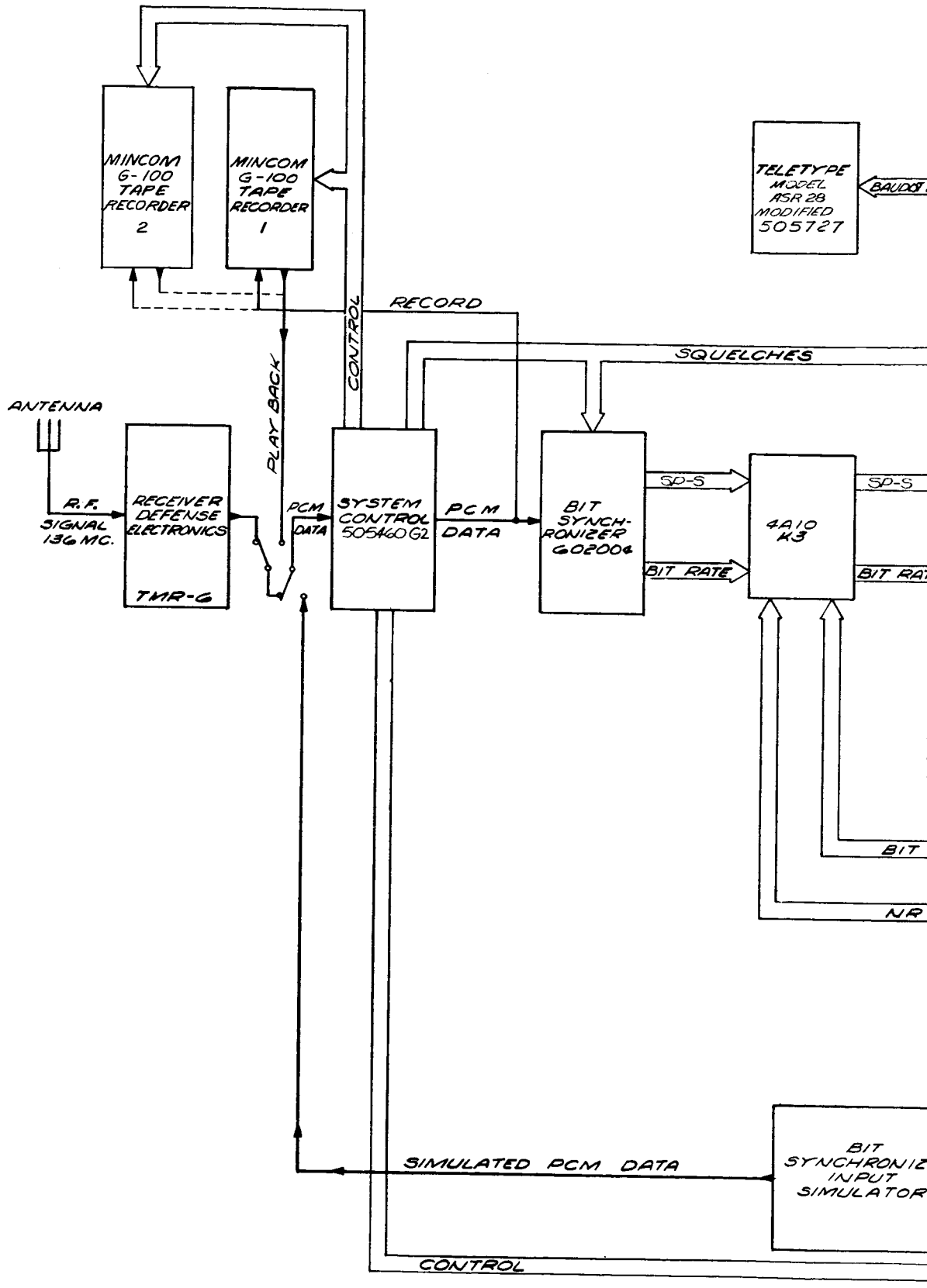


Figure I-29. Monitor, Schematic Diagram


MINCOM G-100 TAPE RECORDER 2
MINCOM G-100 TAPE RECORDER 1
TELETYPE MODEL ASR 28 MODIFIED 505727
BAUDOT
RECORD
CONTROL
SQUELCHES
PLAY BACK
ANTENNA
R.F. SIGNAL 136 MC.
RECEIVER DEFENSE ELECTRONICS
TMR-6
PCM DATA
SYSTEM CONTROL 505460 G2
PCM DATA
BIT SYNCH-RONIZER 602004
SD-S
BIT RATE
4A10 K3
SD-S
BIT RAT
BIT
NR
SIMULATED PCM DATA
BIT SYNCHRONIZ INPUT SIMULATOR
CONTROL

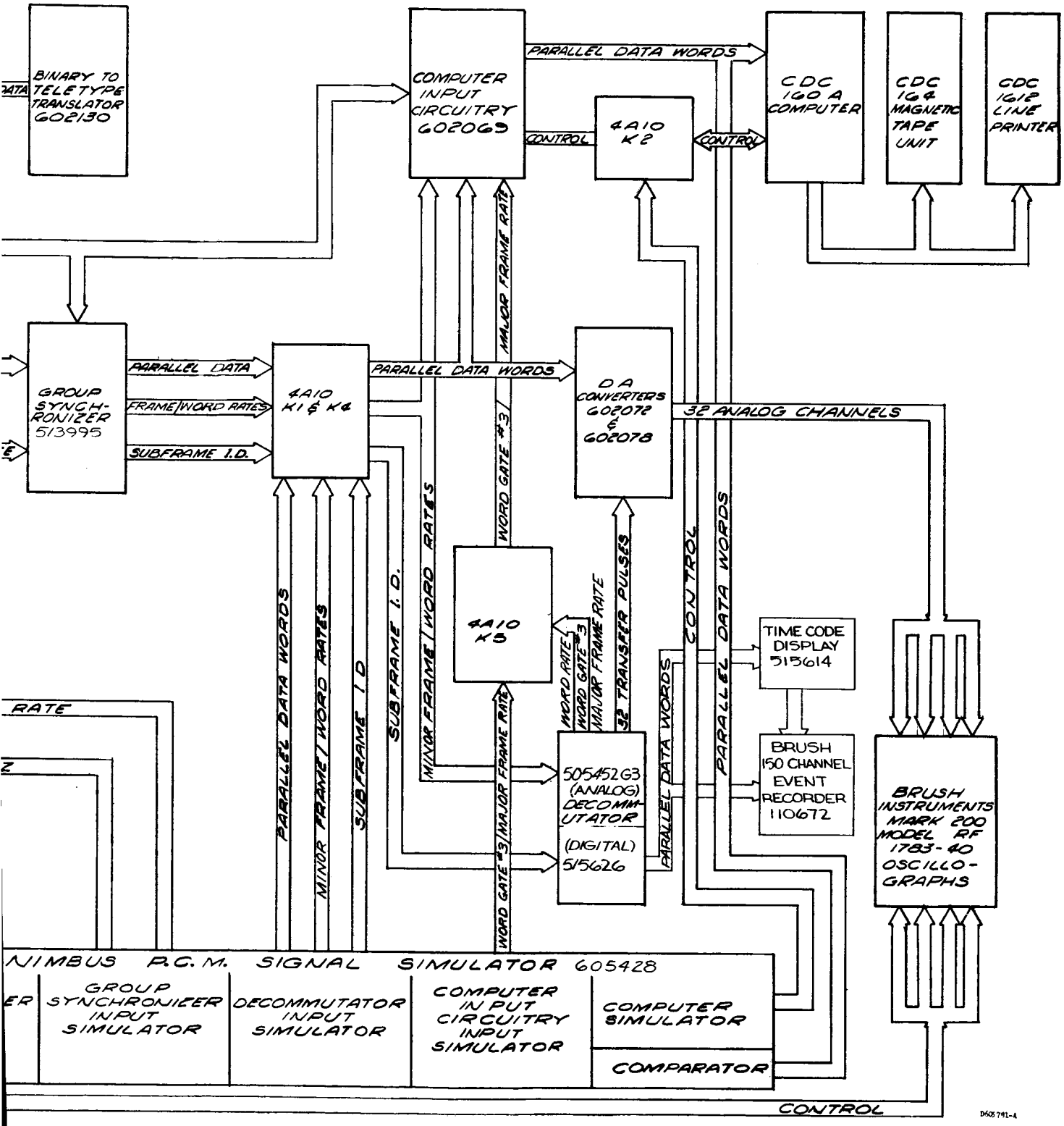
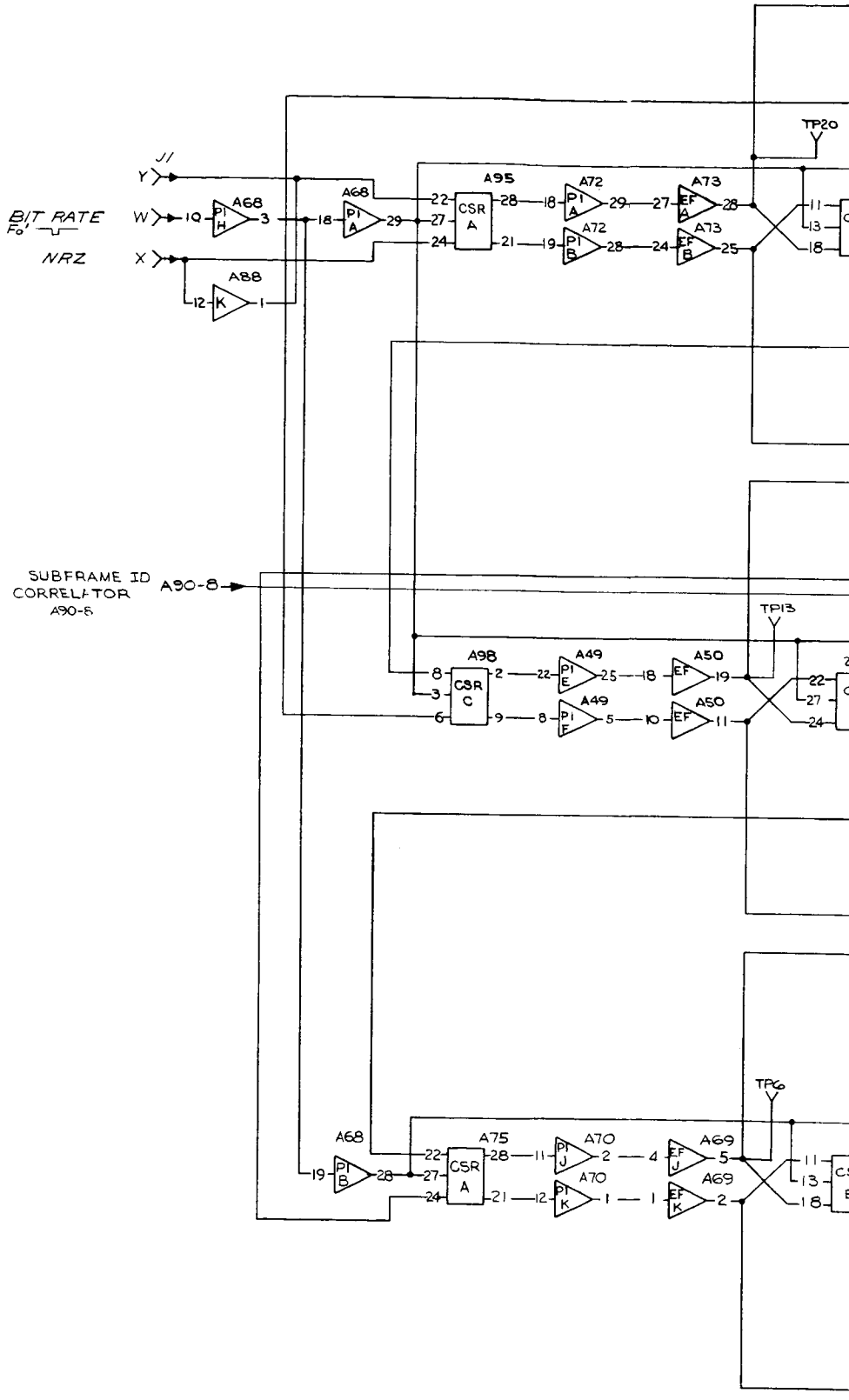


Figure 1-30. PCM Ground Station System 2, Block Diagram


J1
Y
W
X
BIT RATE
Fo
NRZ
A68
A88
A95
A72
A73
TP20
SUBFRAME ID
CORRELATOR
A90-8
A98
A49
A50
TP13
A75
A70
A69
TP6

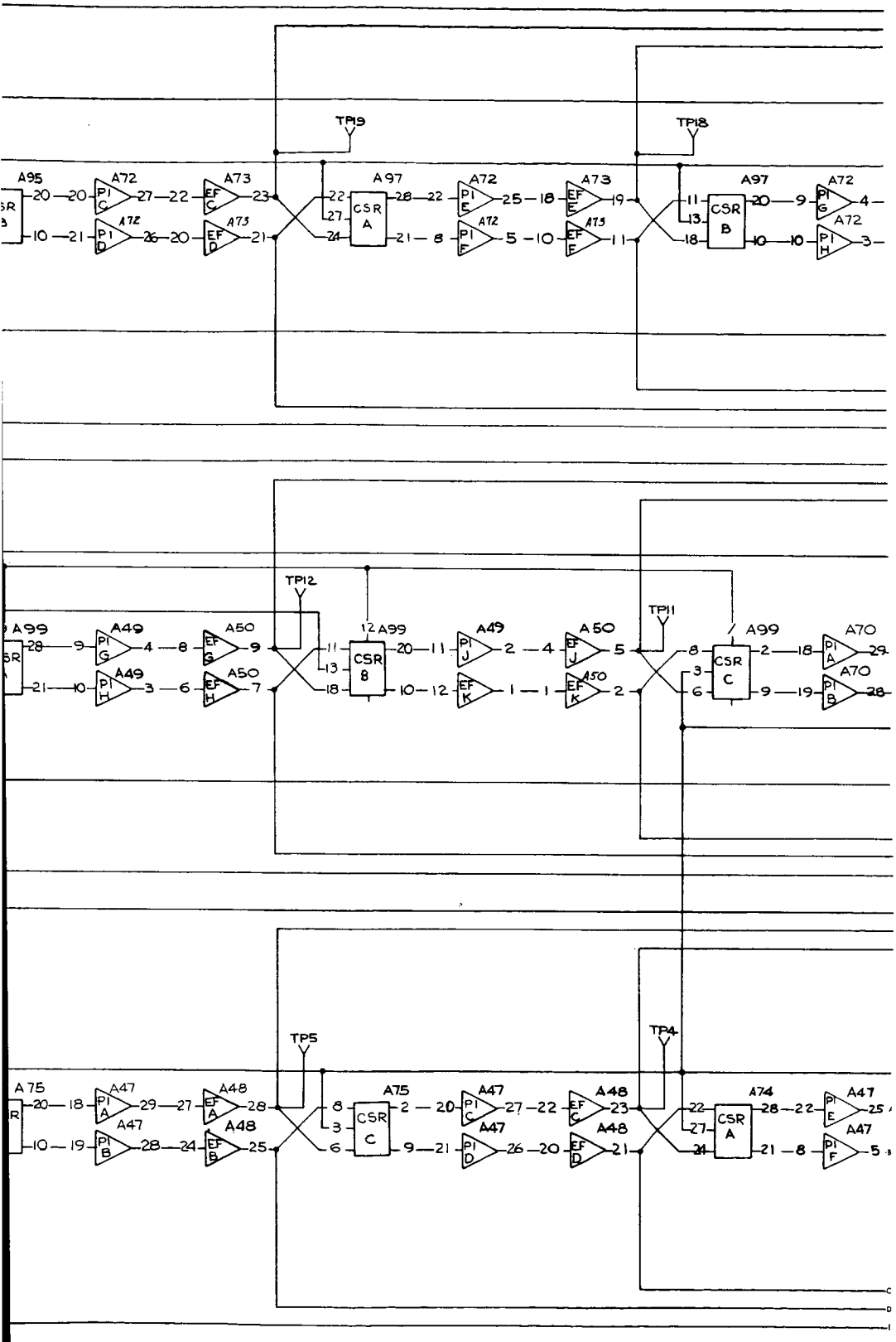
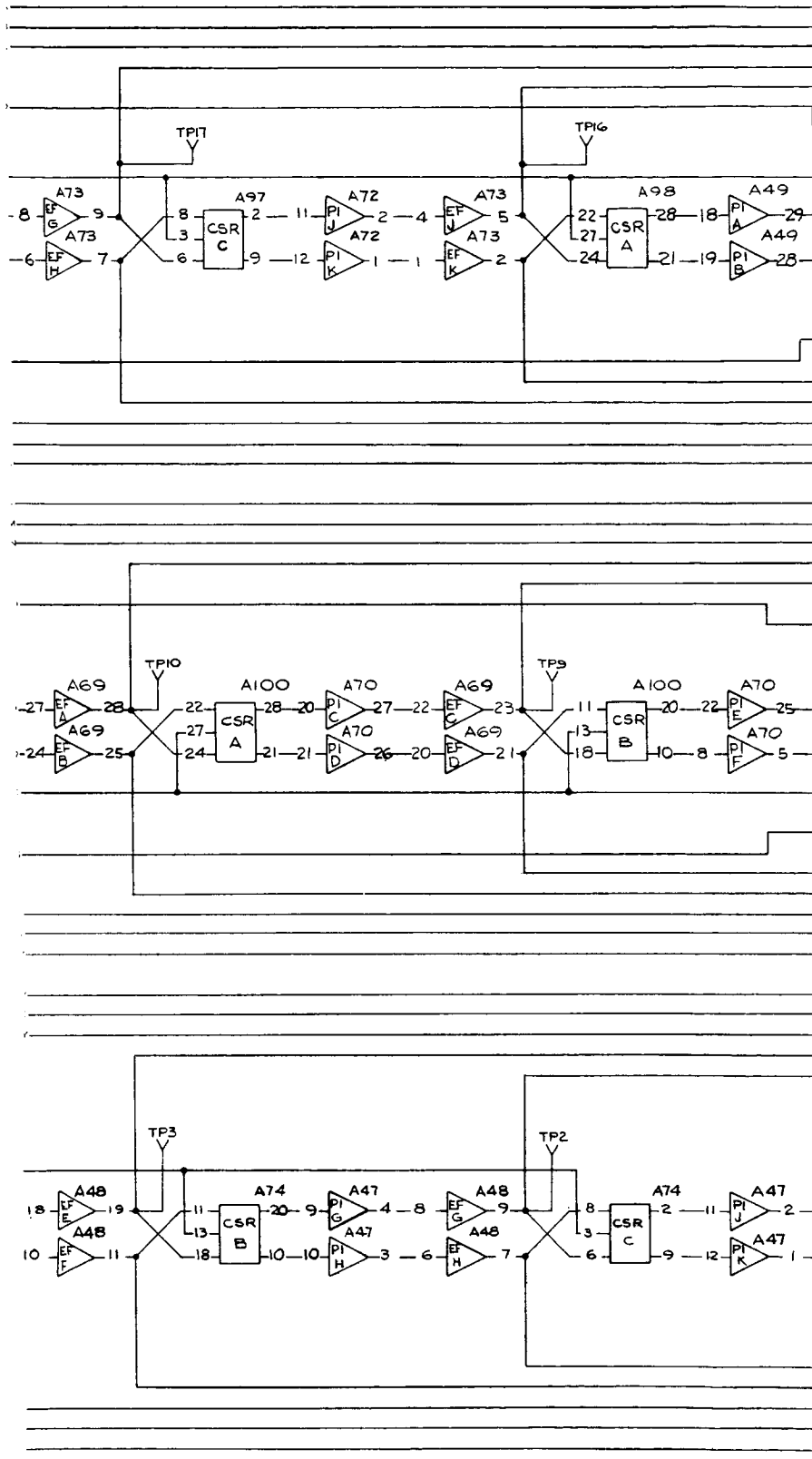


Figure 1-31. Input Shift Register, Logic Diagram (Sheet 1 of 2)


TP17
TP16
A73
A97
A72
A73
A98
A49
CSR C
CSR A
TP10
TP9
A69
A100
A70
A69
A100
A70
CSR A
CSR B
TP3
TP2
A48
A74
A47
A48
A74
A47
CSR B
CSR C

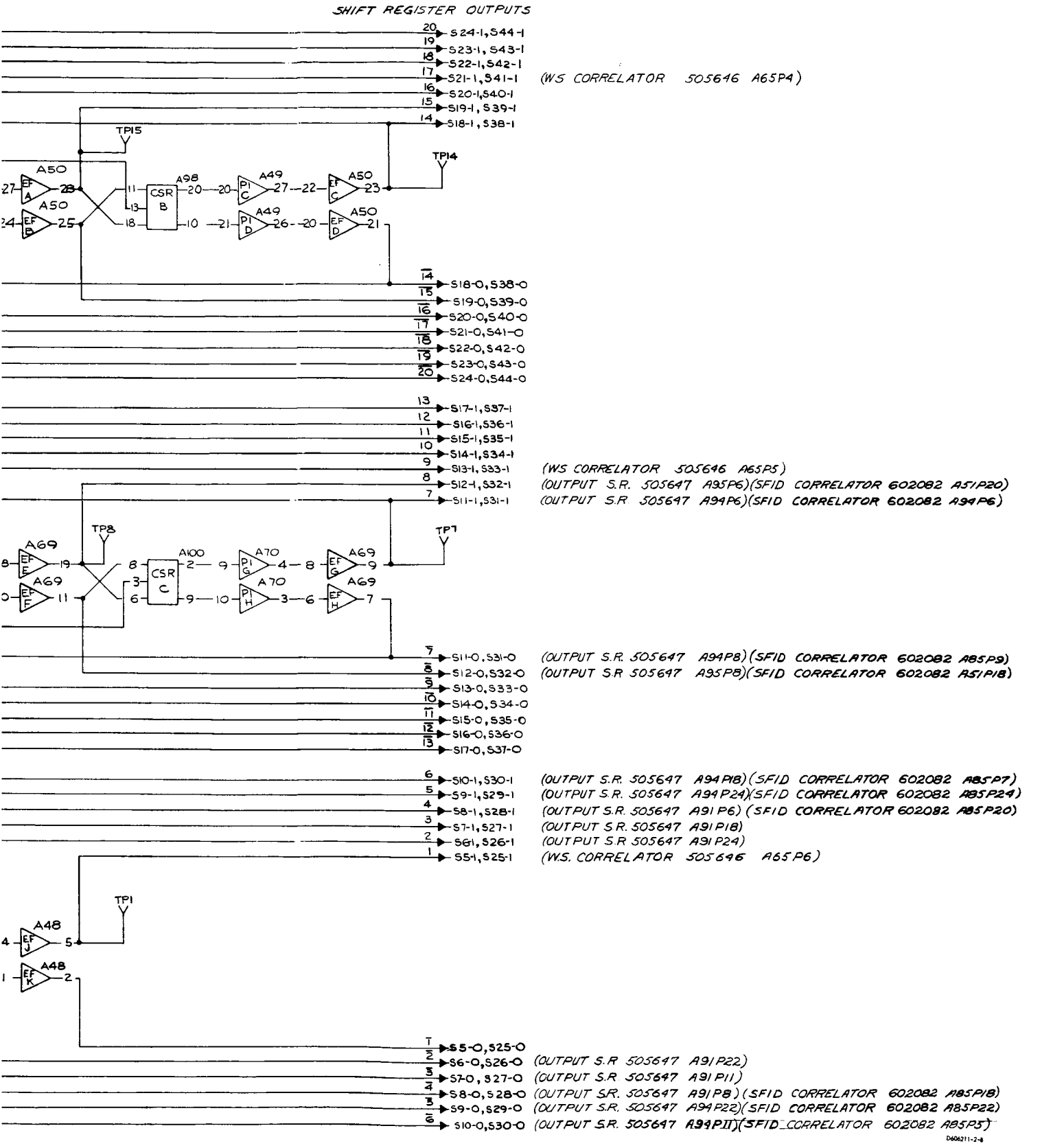
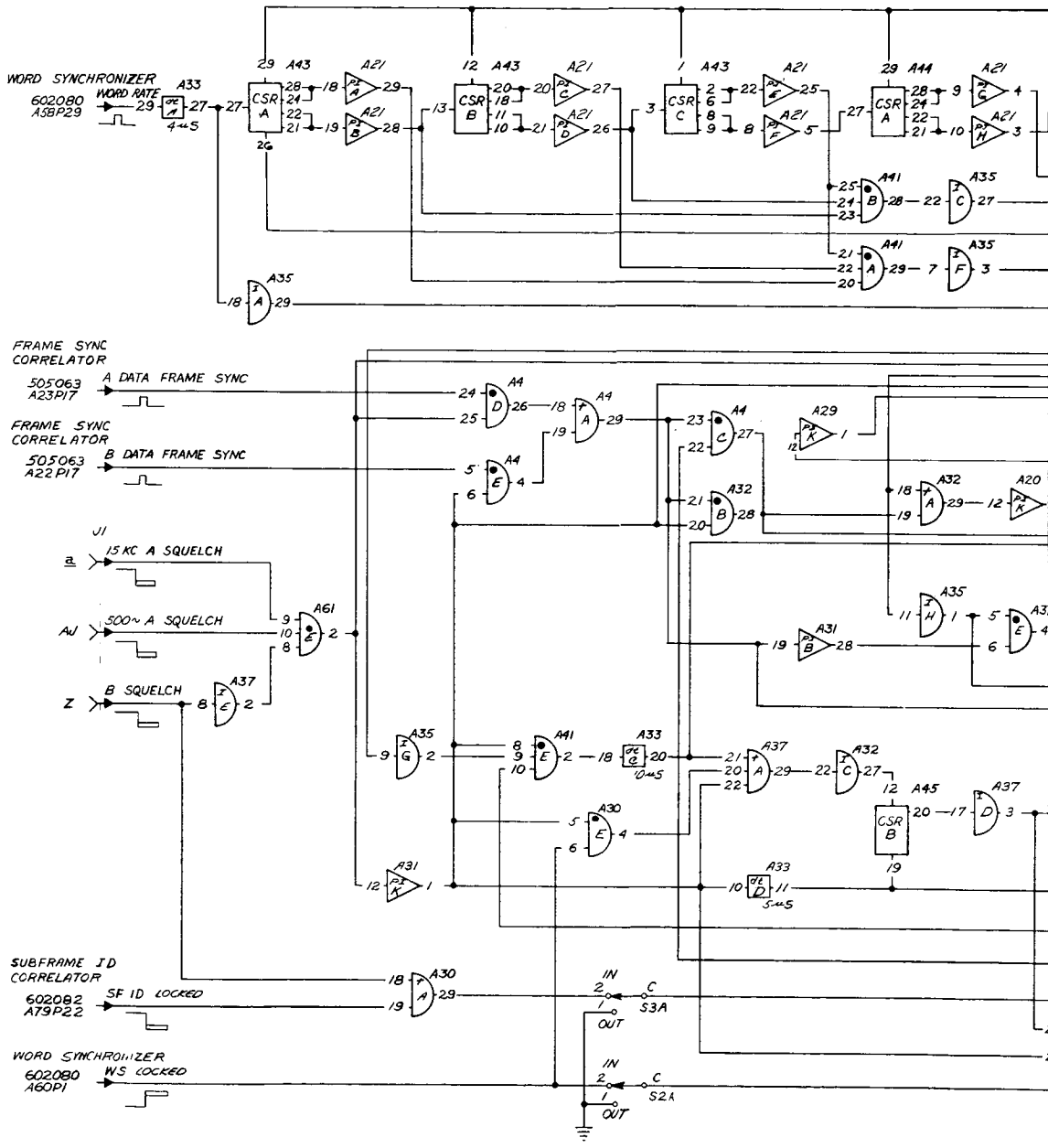


Figure 1-31. Input Shift Register, Logic Diagram (Sheet 2 of 2)


WORD SYNCHRONIZER
602080
A58P29
WORD RATE
FRAME SYNC CORRELATOR
505063
A23P17
A DATA FRAME SYNC
FRAME SYNC CORRELATOR
505063
A22P17
B DATA FRAME SYNC
J1
15 KC A SQUELCH
500~ A SQUELCH
B SQUELCH
SUBFRAME ID CORRELATOR
602082
A79P22
SF ID LOCKED
WORD SYNCHRONIZER
602080
A60P1
WS LOCKED
S3A
S2A
IN
OUT

1-341

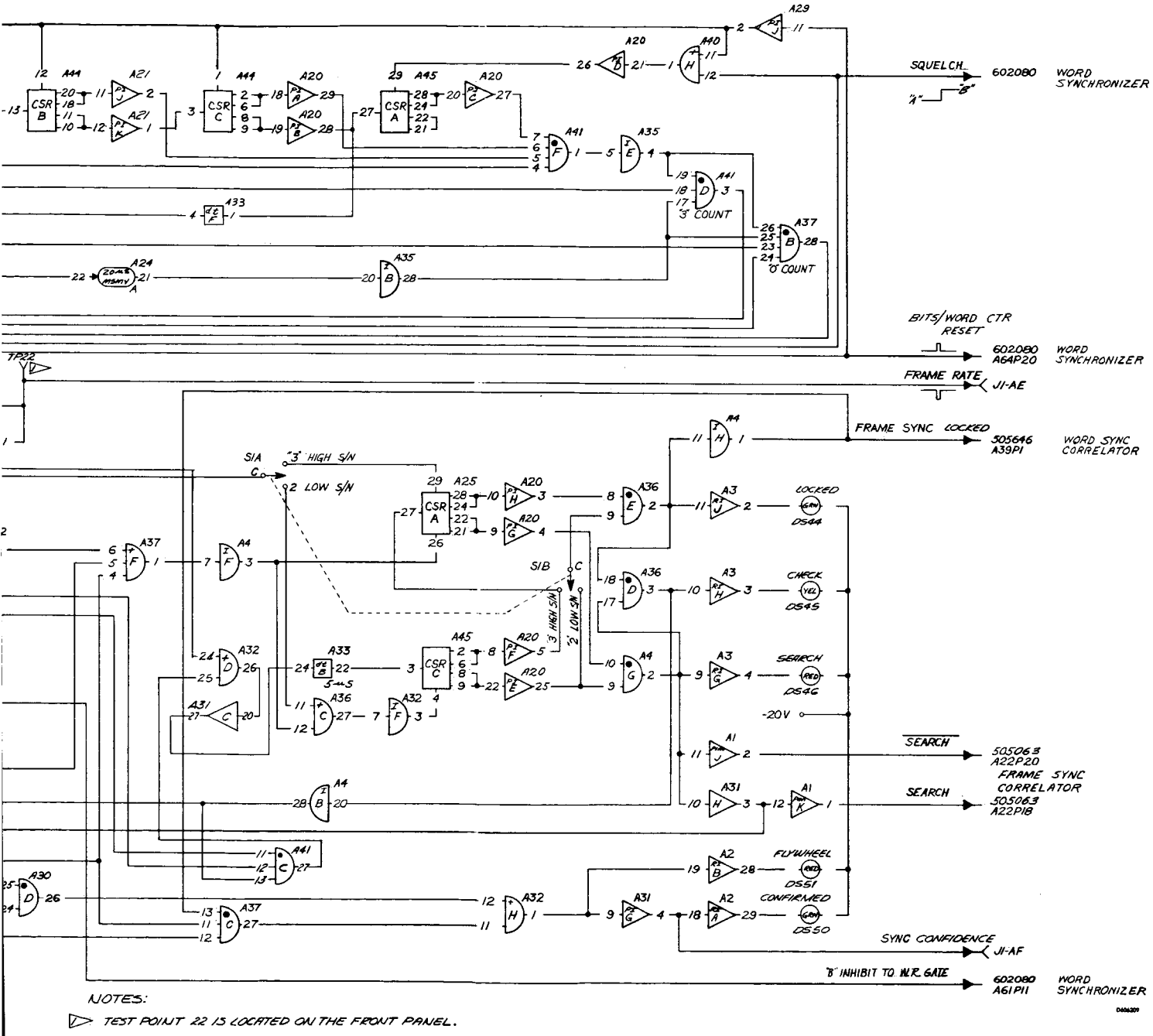
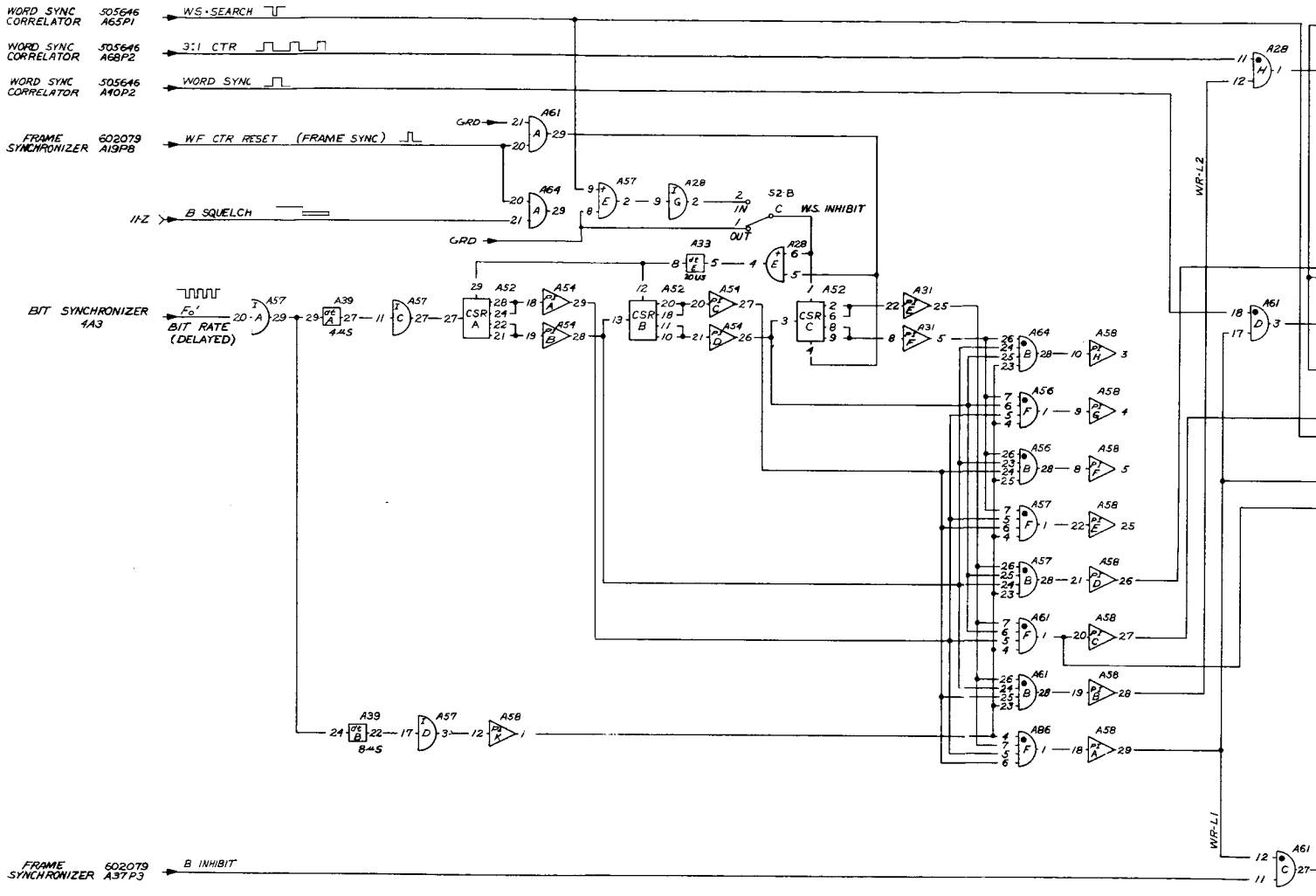


Figure 1-32. Frame Sync Correlator, Logic Diagram


WORD SYNC CORRELATOR 505646 A65P1
W.S. SEARCH
WORD SYNC CORRELATOR 505646 A68P2
3:1 CTR
WORD SYNC CORRELATOR 505646 A10P2
WORD SYNC
FRAME SYNCHRONIZER 602079 A19P8
WF CTR RESET (FRAME SYNC)
11-Z
B SQUELCH
GRD
S2-B
W.S. INHIBIT
IN
OUT
BIT SYNCHRONIZER 4A3
Fo'
BIT RATE (DELAYED)
4.45
8.45
CSR A
CSR B
CSR C
WR-L2
WR-L1
FRAME SYNCHRONIZER 602079 A37P3
B INHIBIT

1-35-1

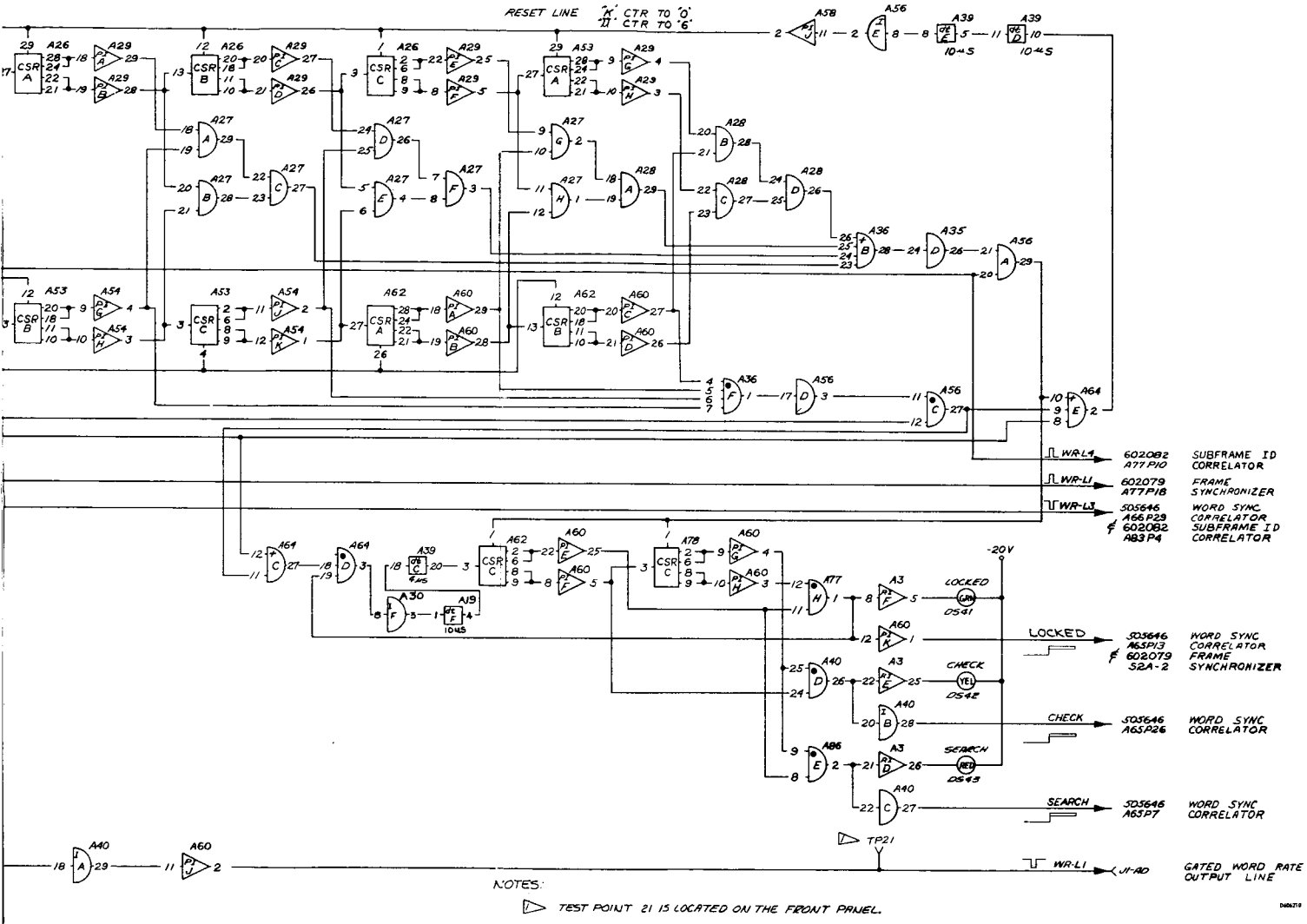
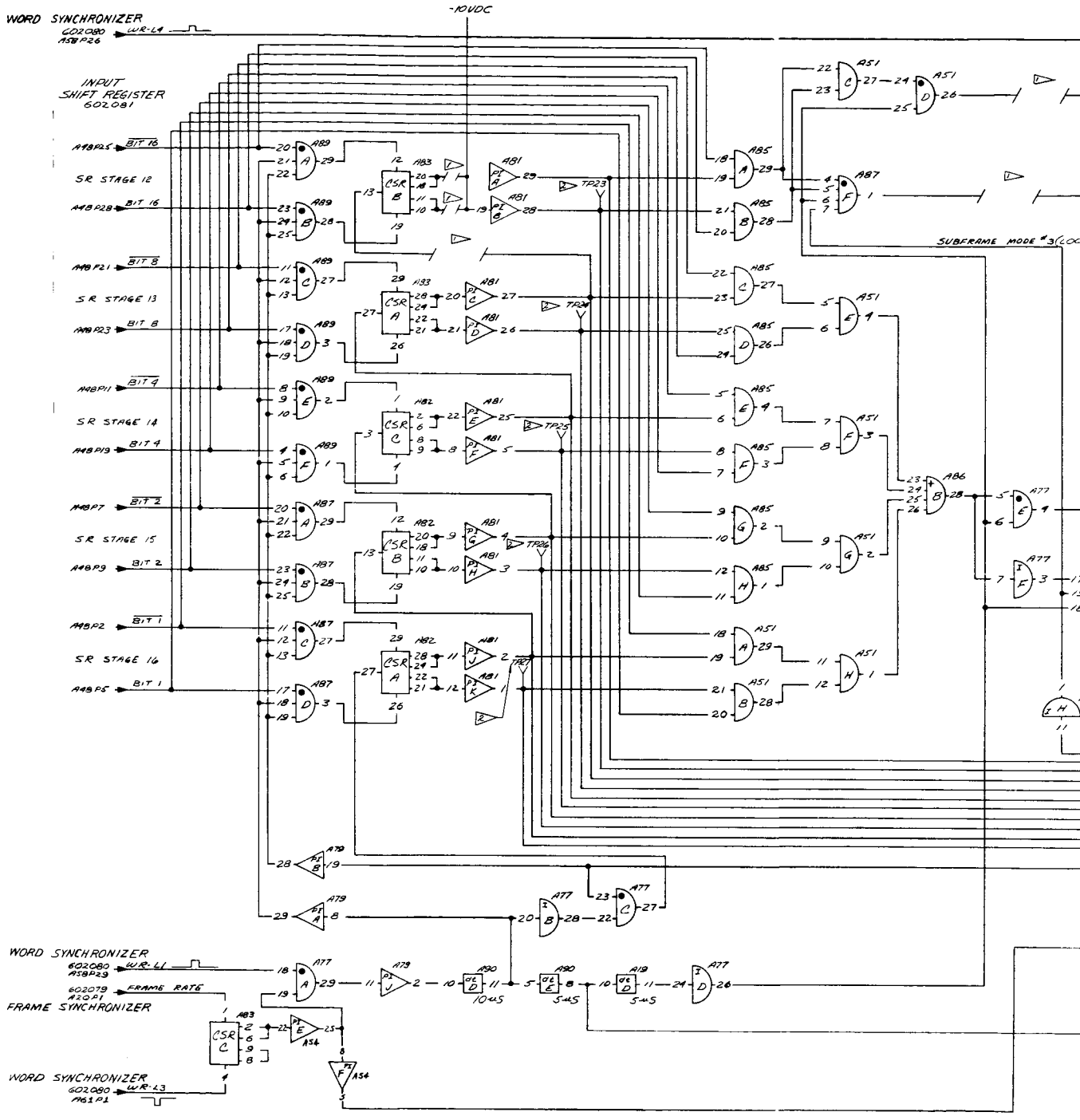


Figure 1-33. Word Synchronizer, Logic Diagram



▷ LEAVE THESE LEADS DISCONNECTED. THIS CIRCUITRY IS PROVIDED FOR EXPANSION OF SUBFRAME ID TO 5 BITS.

▷ TEST POINTS 23 THRU 27 ON FRONT PANEL.

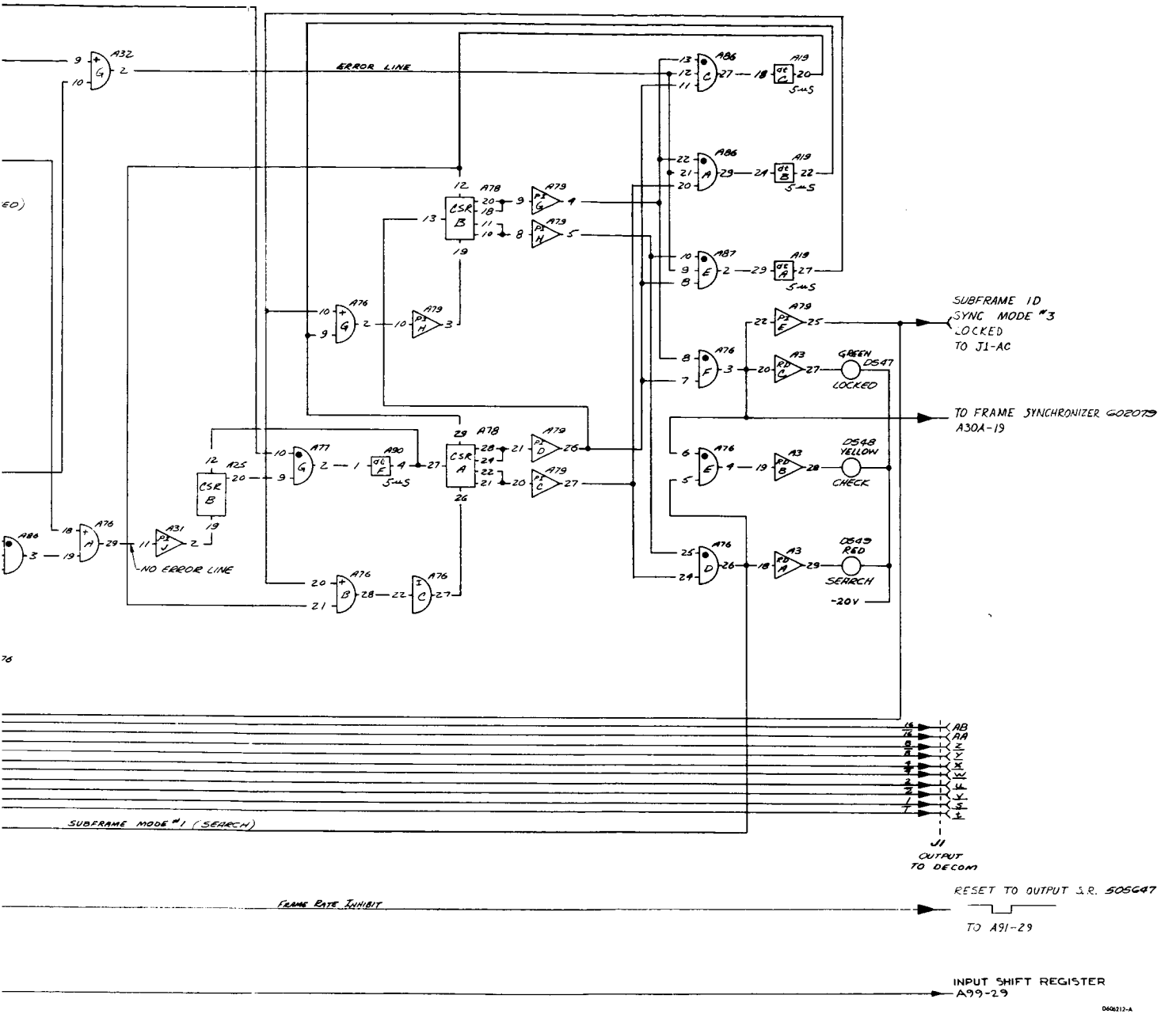


Figure 1-34. Subframe ID Correlator, Logic Diagram

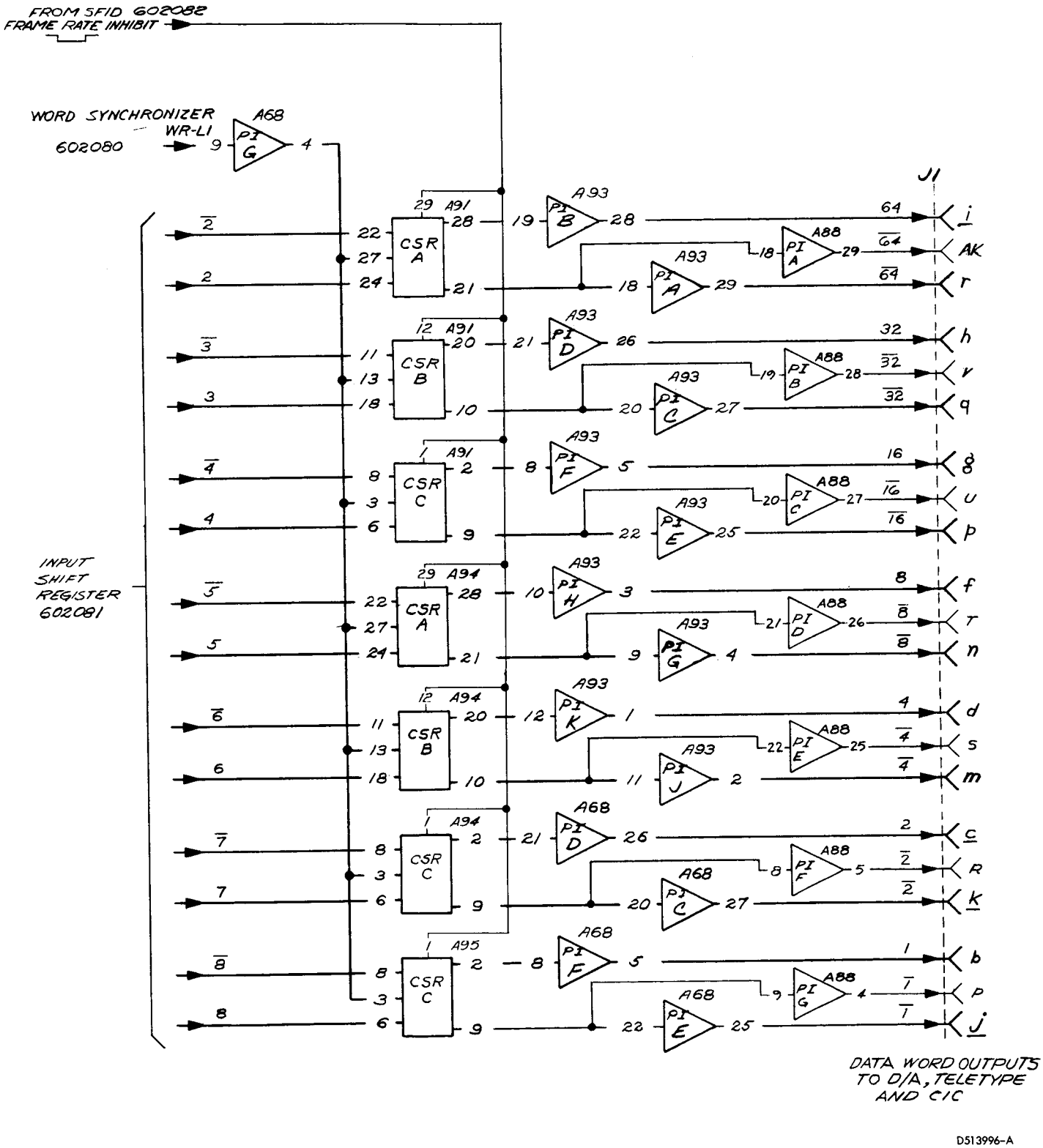
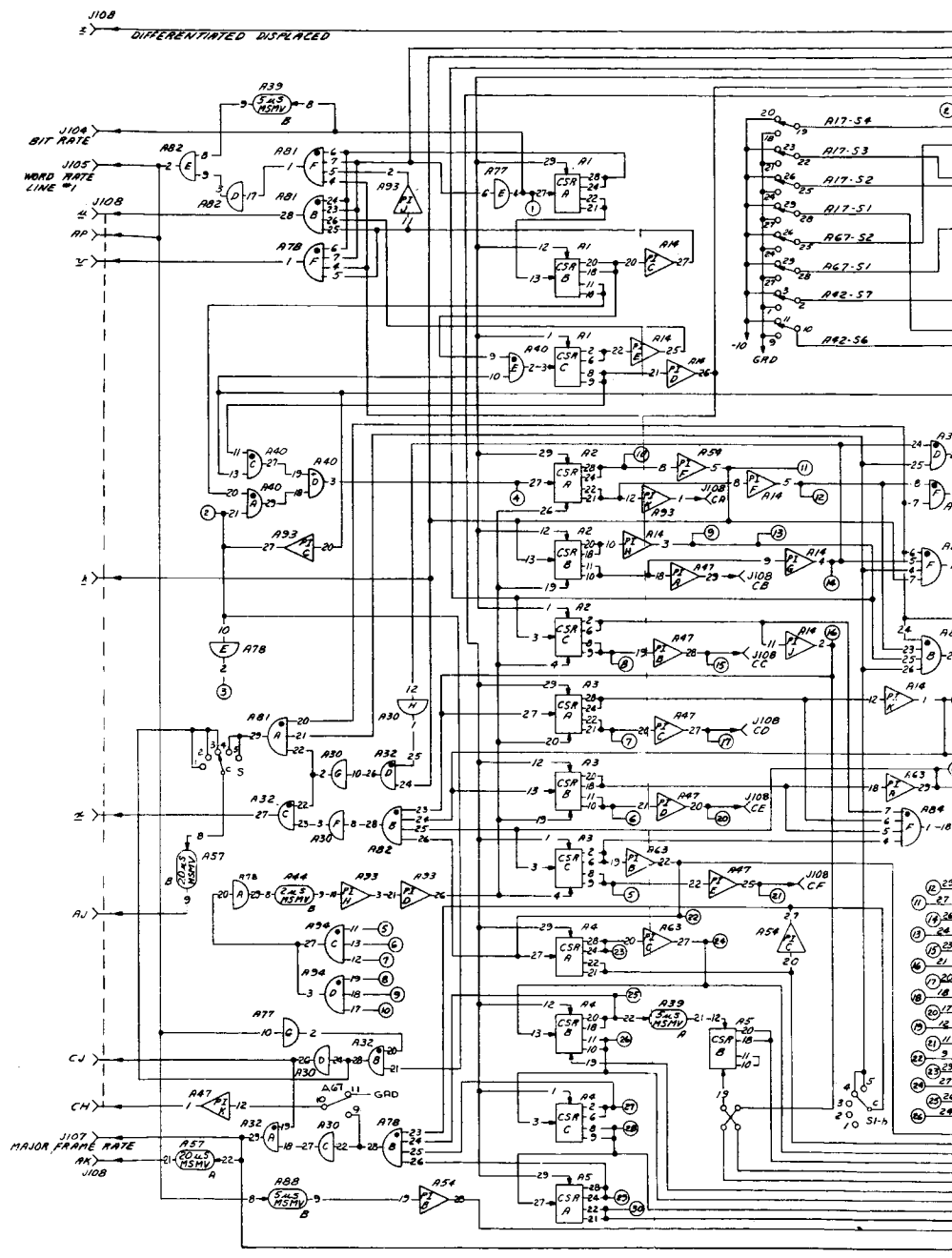


Figure I-35. Output Shift Register, Logic Diagram


J10B
DIFFERENTIATED DISPLACED
J104
BIT RATE
J105
WORD RATE
LINE #1
J10B
J107
MAJOR FRAME RATE
J10B
A17-S4
A17-S3
A17-S2
A17-S1
A67-S2
A67-S1
A42-S7
A42-S6
GRD
J10B CA
J10B CB
J10B CC
J10B CD
J10B CE
J10B CF
S1-b

1-38-1

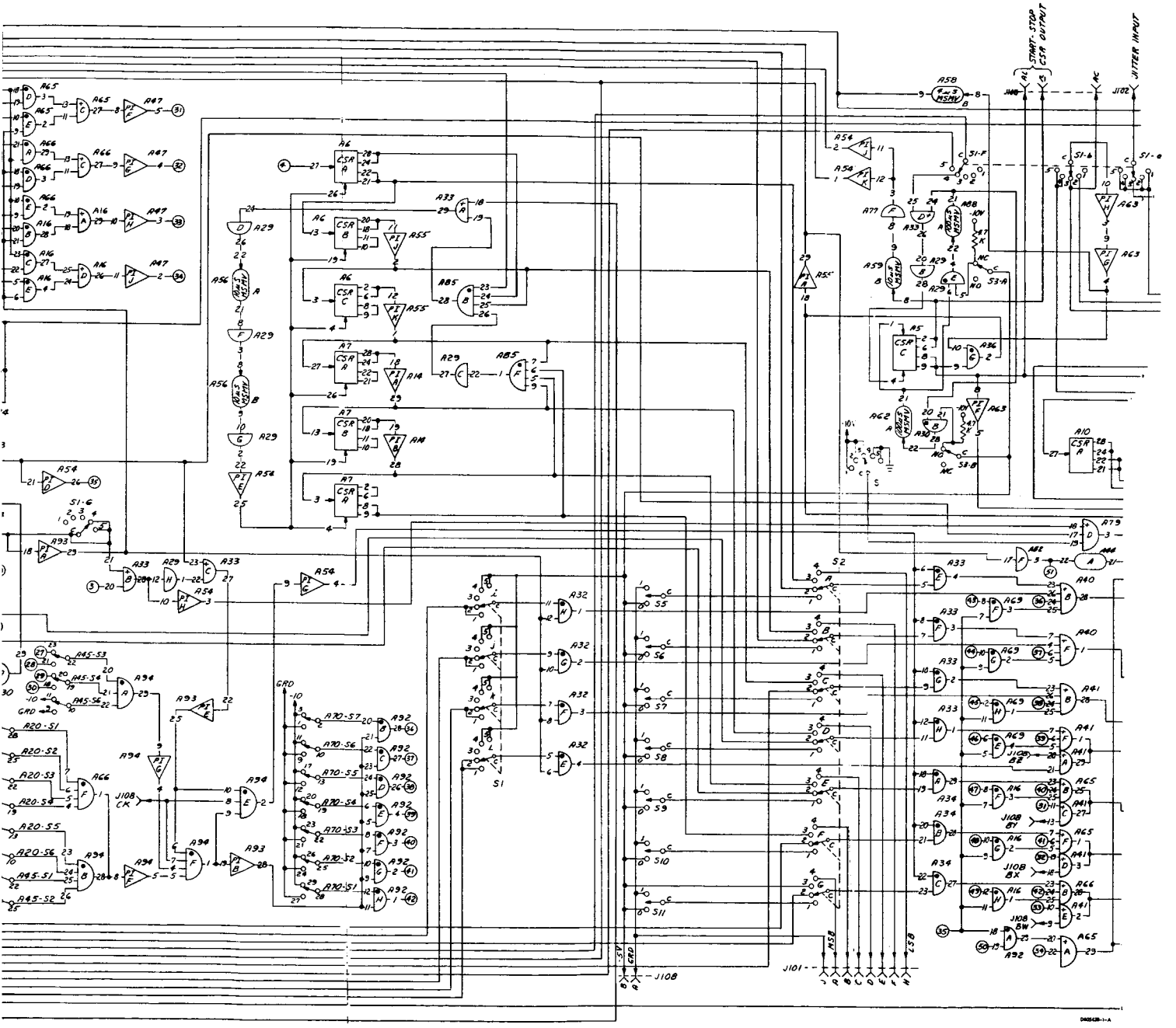
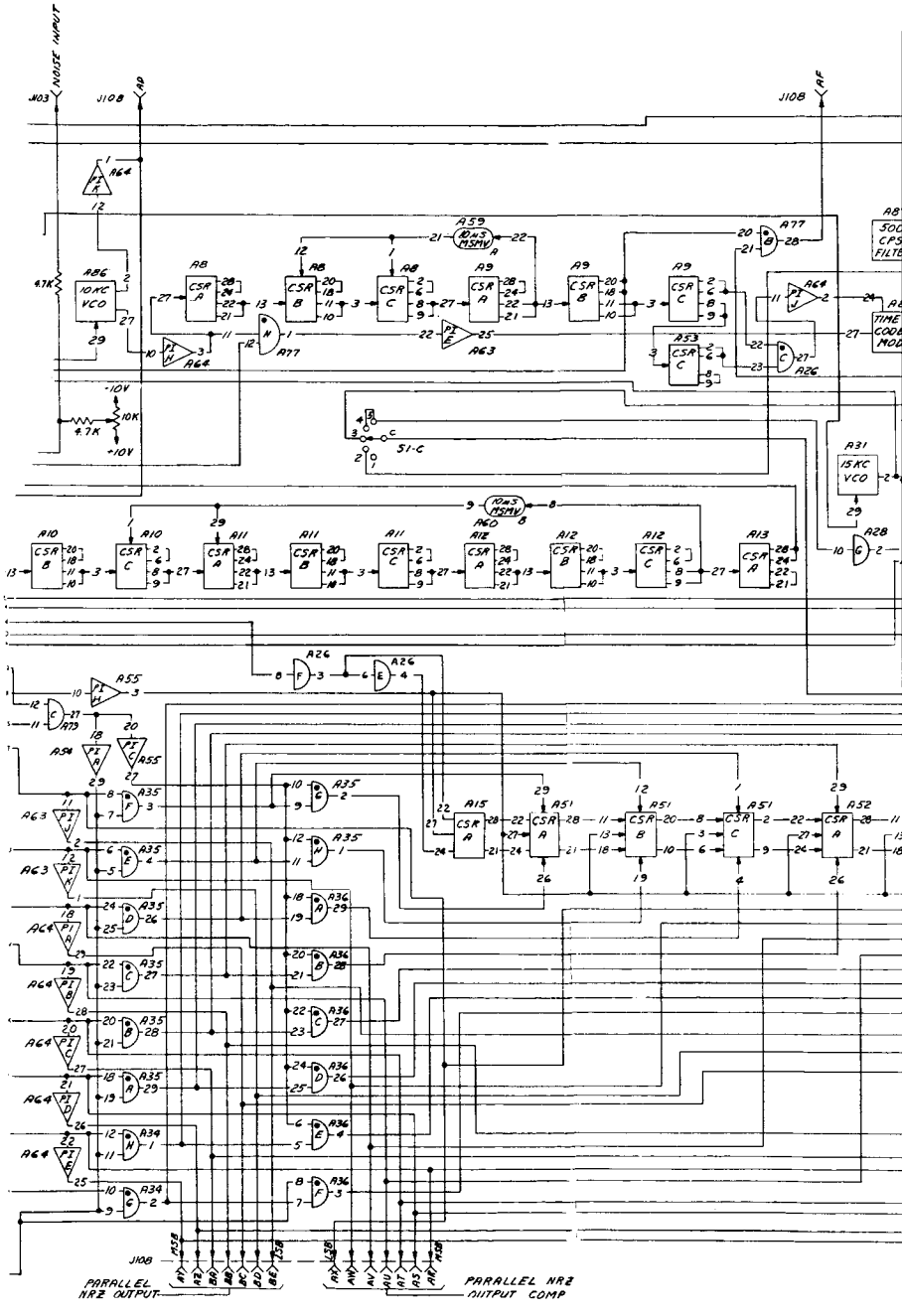


Figure I-36. Simulator, Logic Diagram (Sheet 1 of 2)


NOISE INPUT
J103
J108
AD
AF
A86
10KC VCO
A59
10mS MSMV
A31
15KC VCO
A60
10mS MSMV
S1-C
PARALLEL NRZ OUTPUT
PARALLEL NRZ OUTPUT COMP

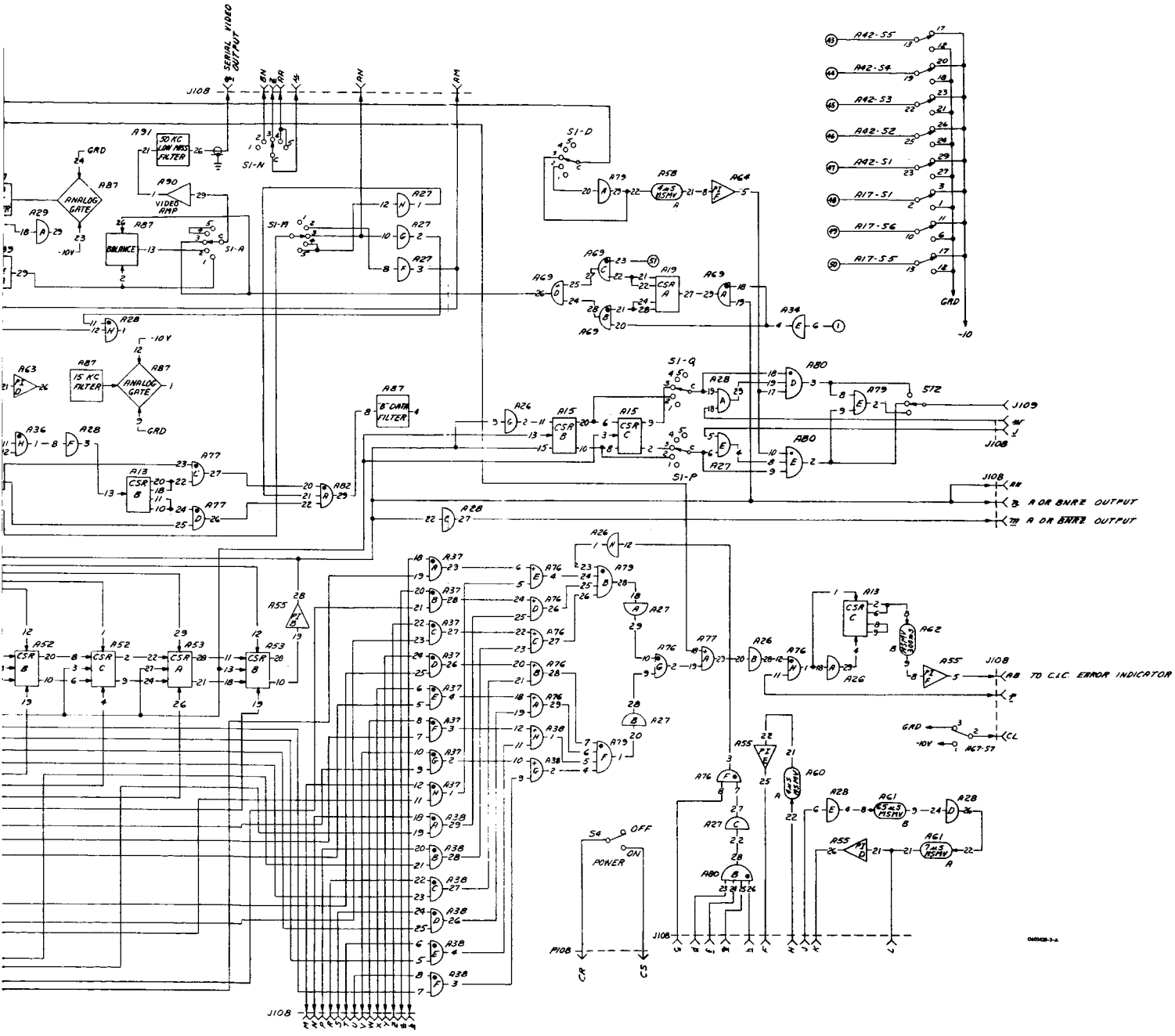
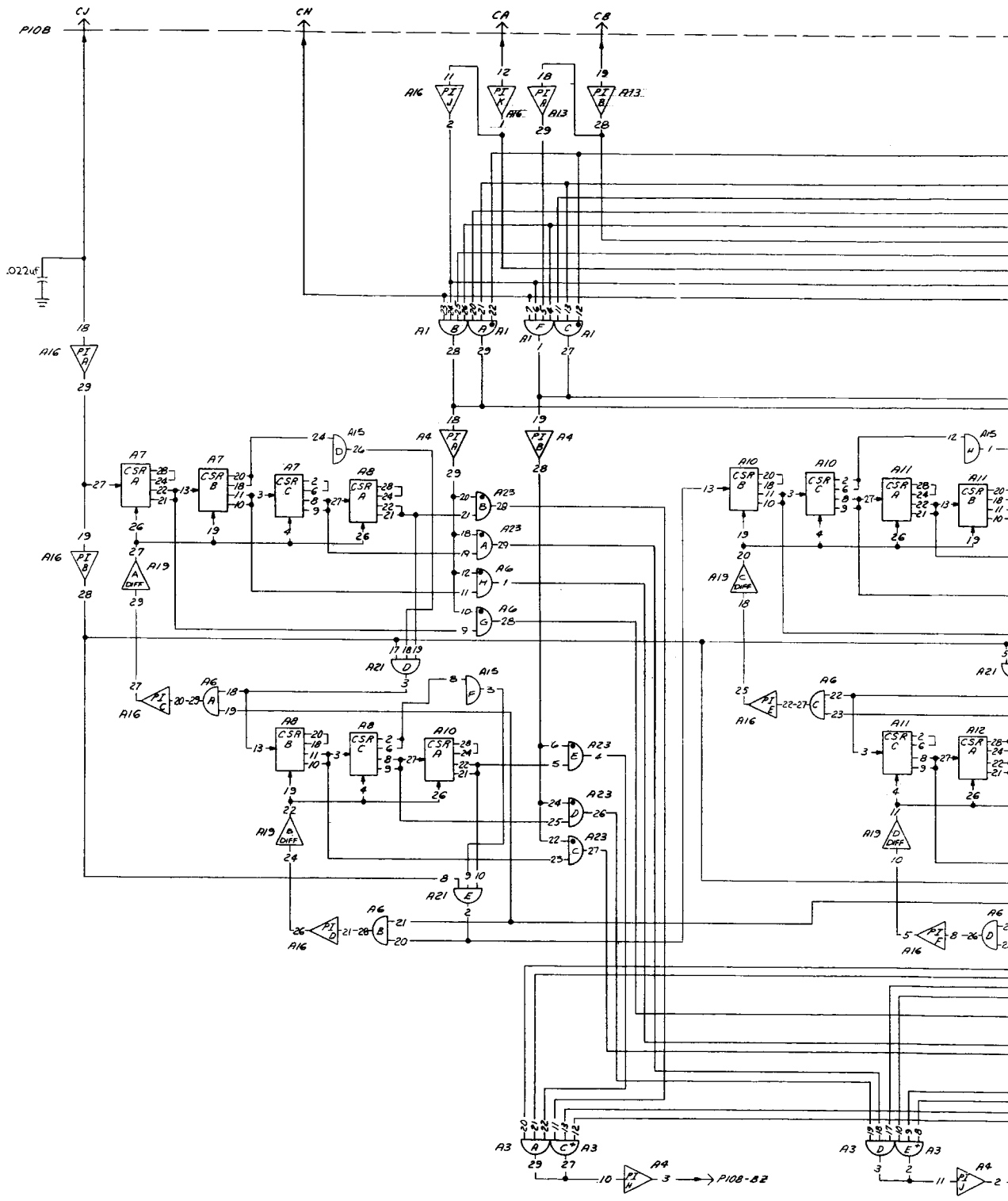


Figure 1-36. Simulator, Logic Diagram (Sheet 2 of 2)



1-40-1

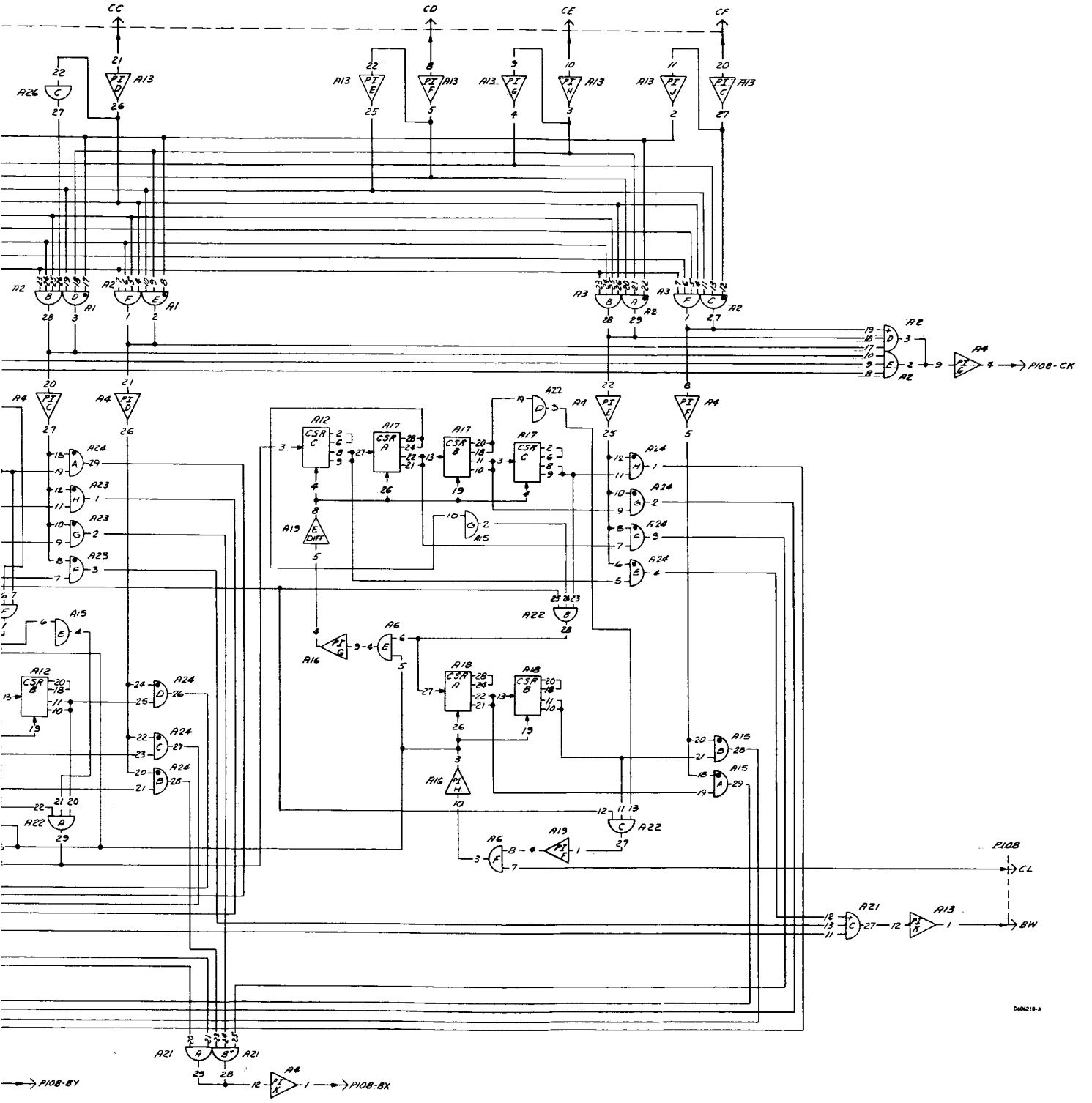
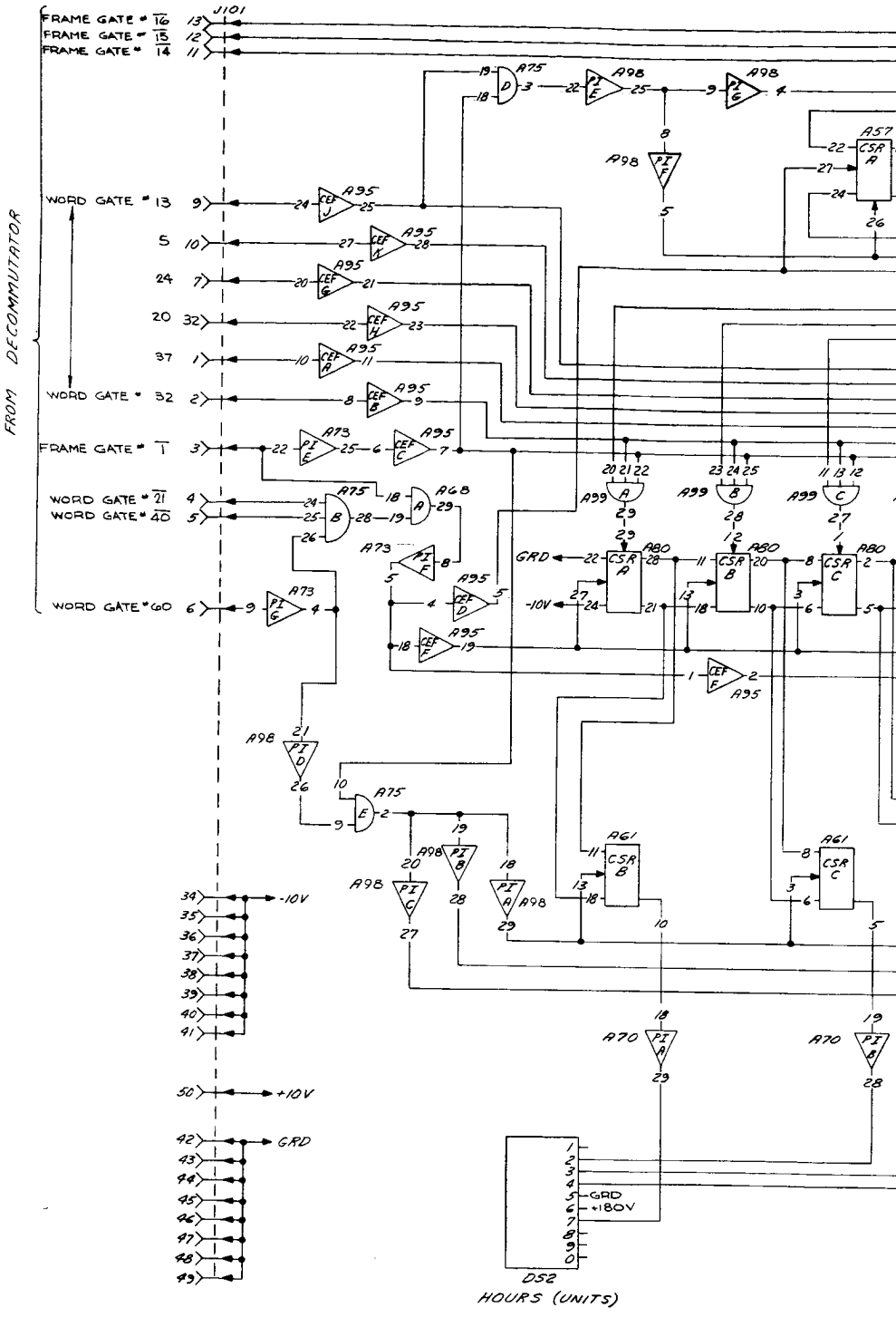


Figure I-37. Time Code Generator, Logic Diagram


FROM DECOMMUTATOR
J101
FRAME GATE # 16
FRAME GATE # 15
FRAME GATE # 14
WORD GATE # 13
5
24
20
37
WORD GATE # 32
FRAME GATE # T
WORD GATE # 21
WORD GATE # 40
WORD GATE # 60
-10V
+10V
GRD
GRD
+180V
DS2
HOURS (UNITS)

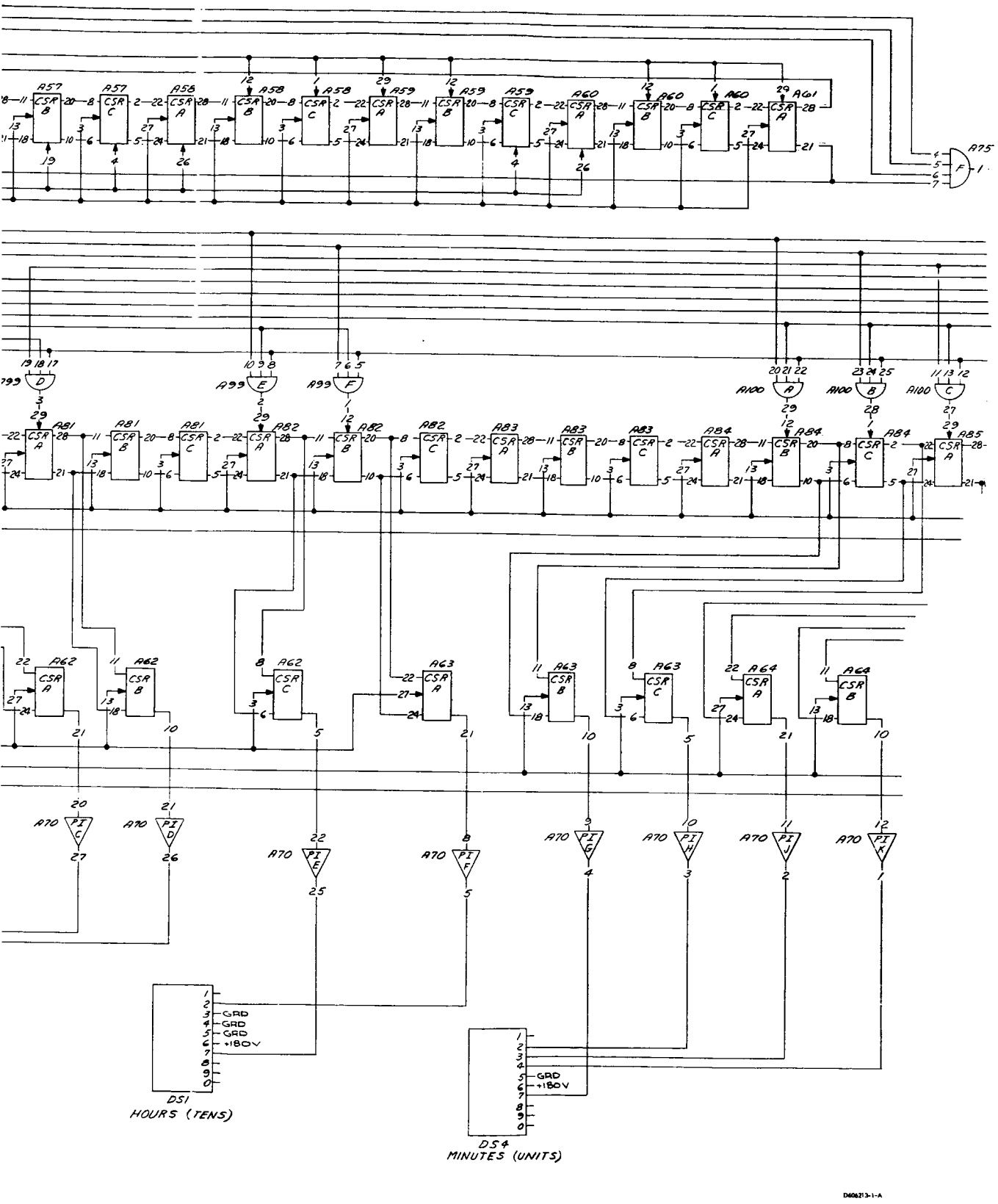
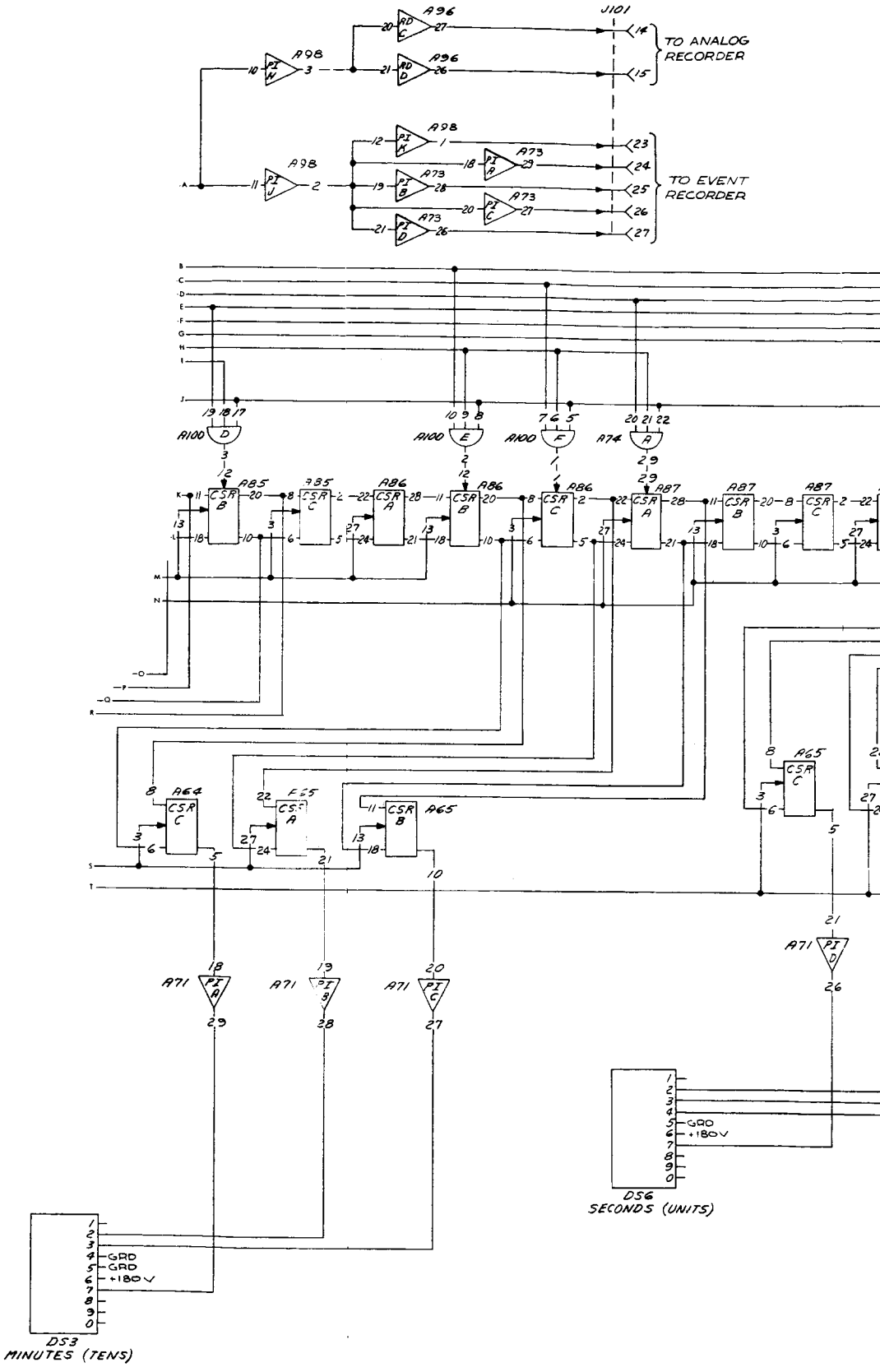


Figure 1-38. Time Code Display, Logic Diagram (Sheet 1 of 2)


J101
TO ANALOG RECORDER
TO EVENT RECORDER
A96
A98
A73
A100
A74
A85
A86
A87
A64
A65
A71
GRD
+180V
DS6
SECONDS (UNITS)
DS3
MINUTES (TENS)

1-42-1

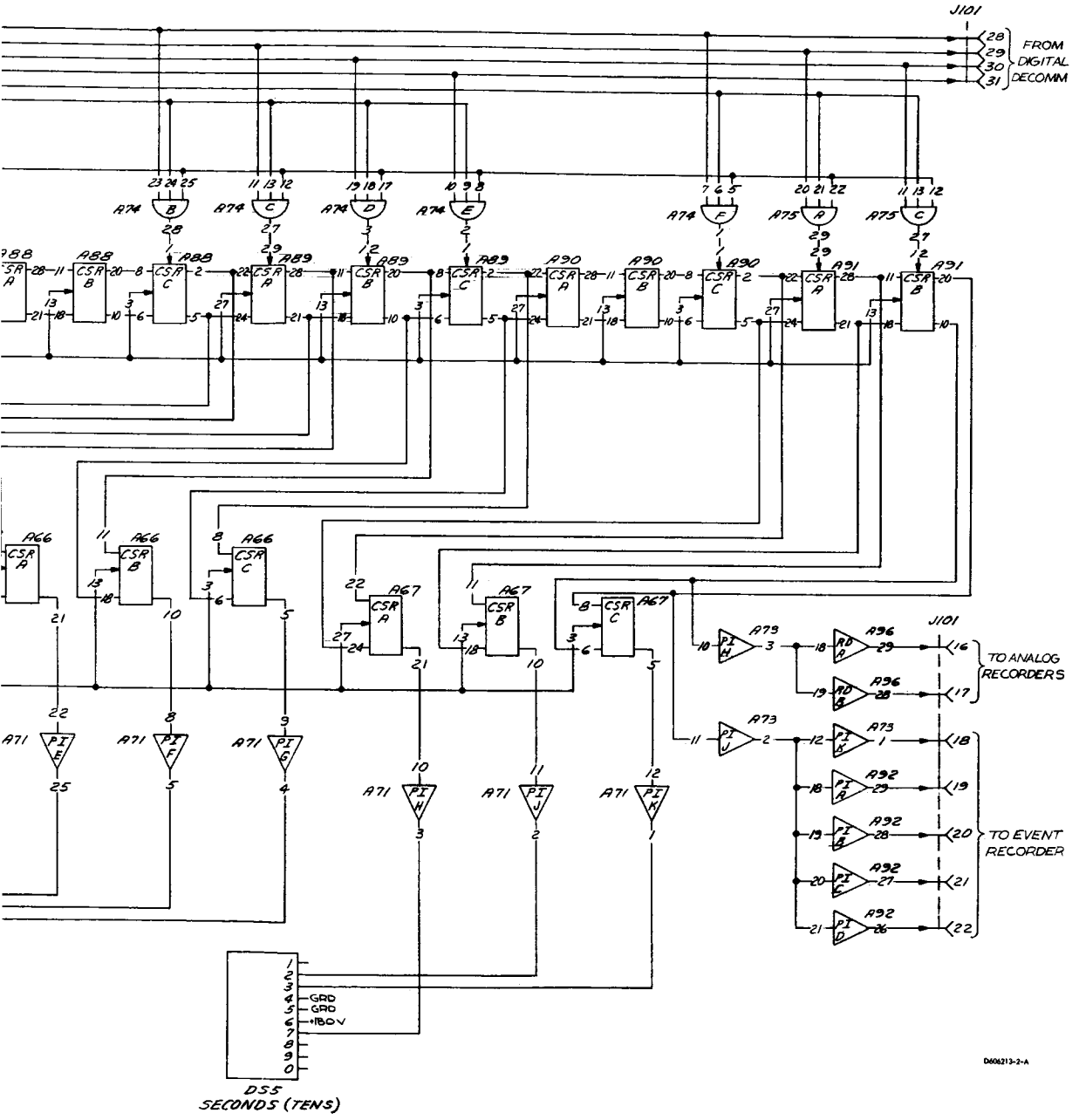
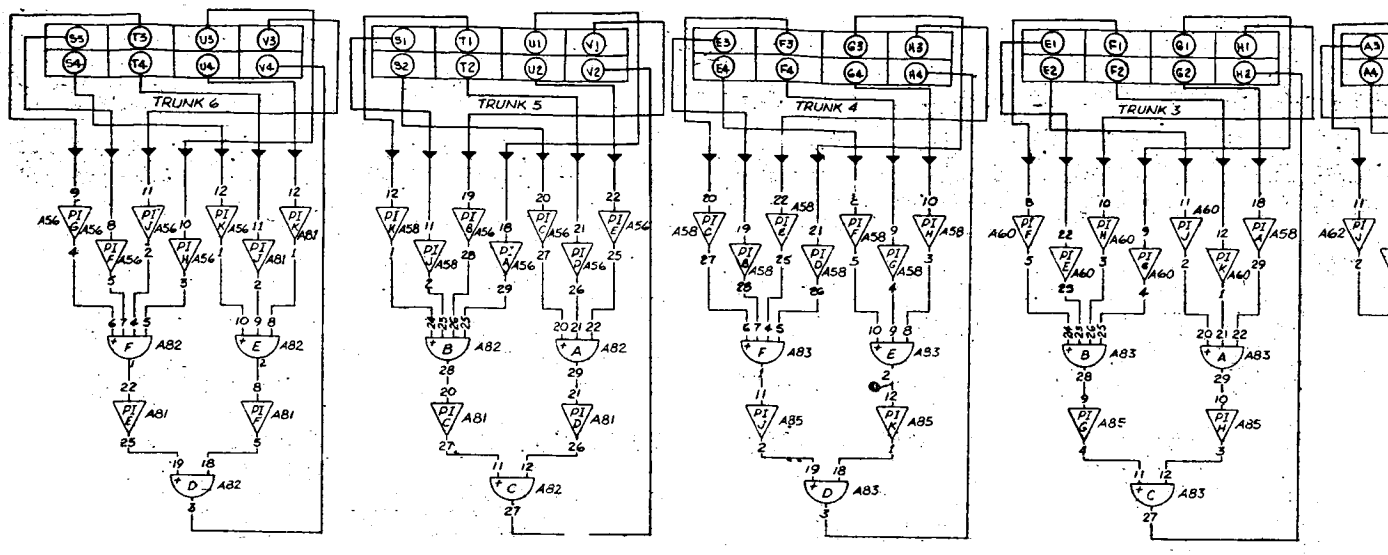
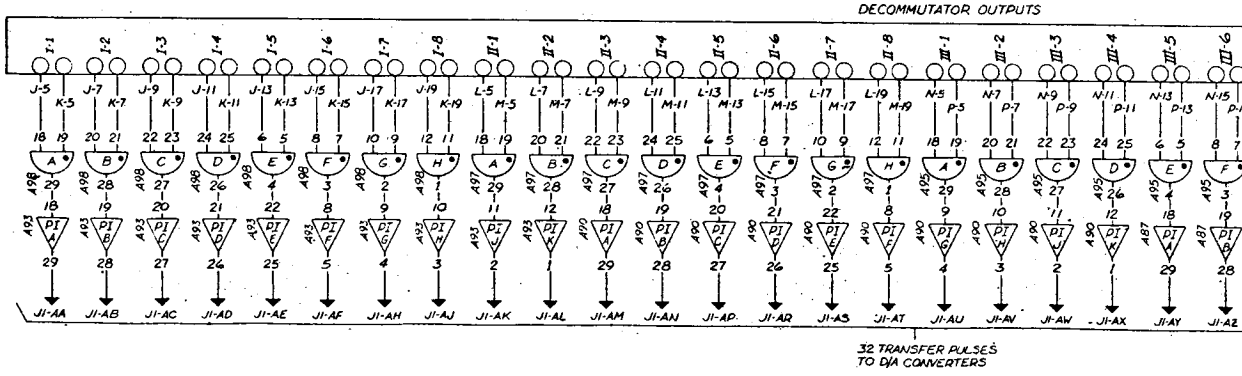


Figure 1-38. Time Code Display, Logic Diagram (Sheet 2 of 2)


TRUNK 6
TRUNK 5
TRUNK 4
TRUNK 3


DECOMMUTATOR OUTPUTS
32 TRANSFER PULSES TO D/A CONVERTERS

1-43-1

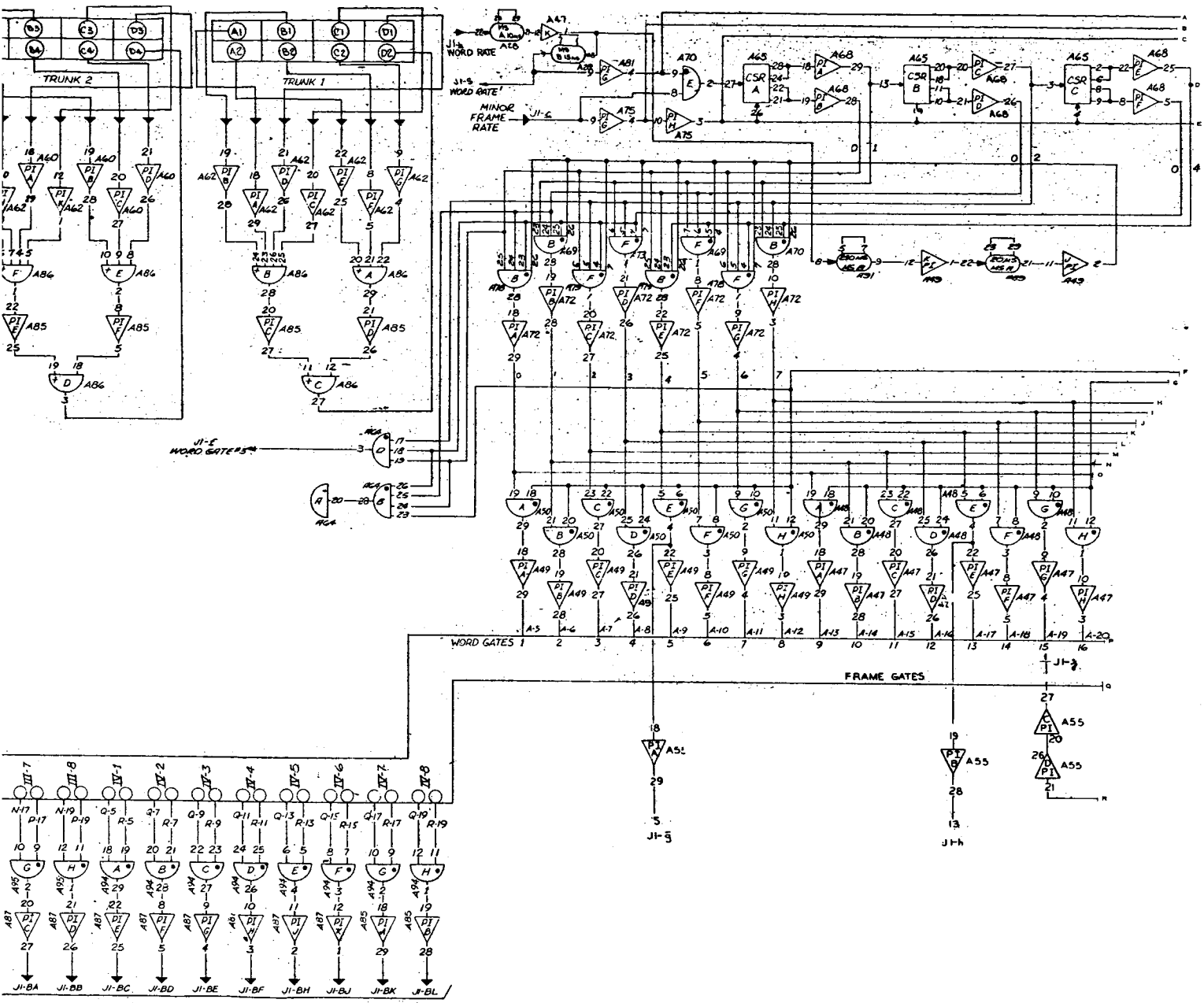
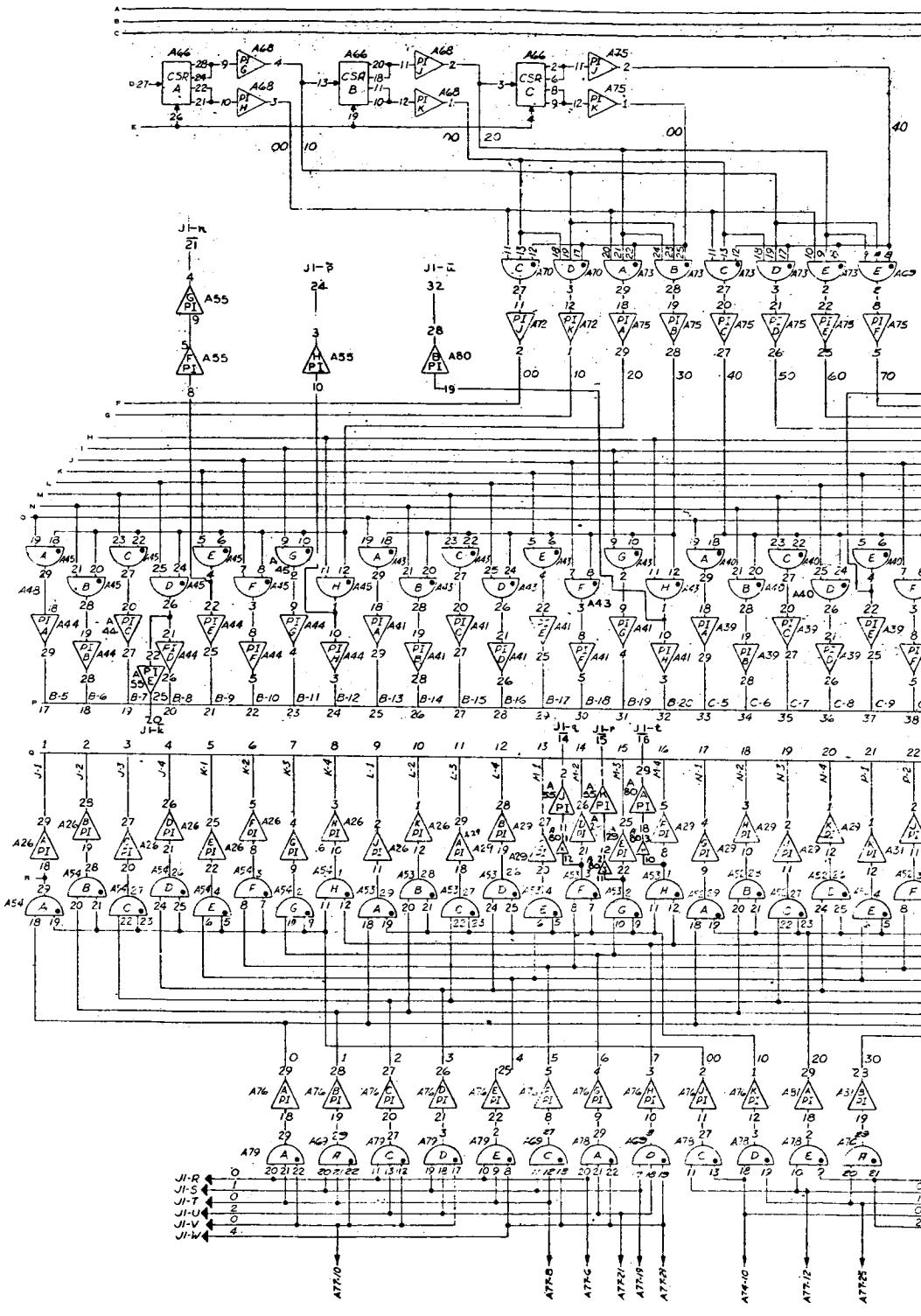


Figure 1-39. Decommutator, Logic Diagram (Sheet 1 of 2)



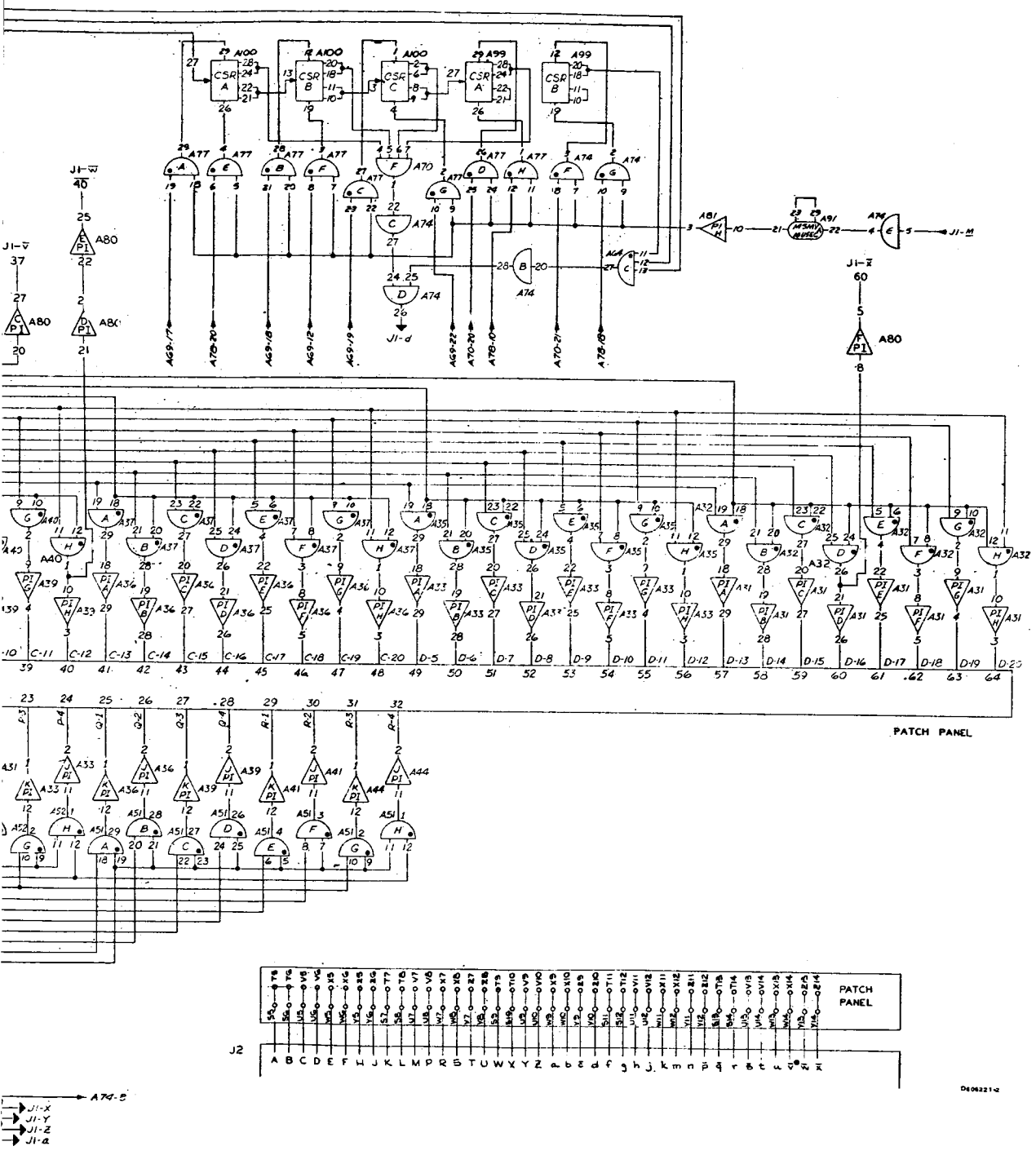
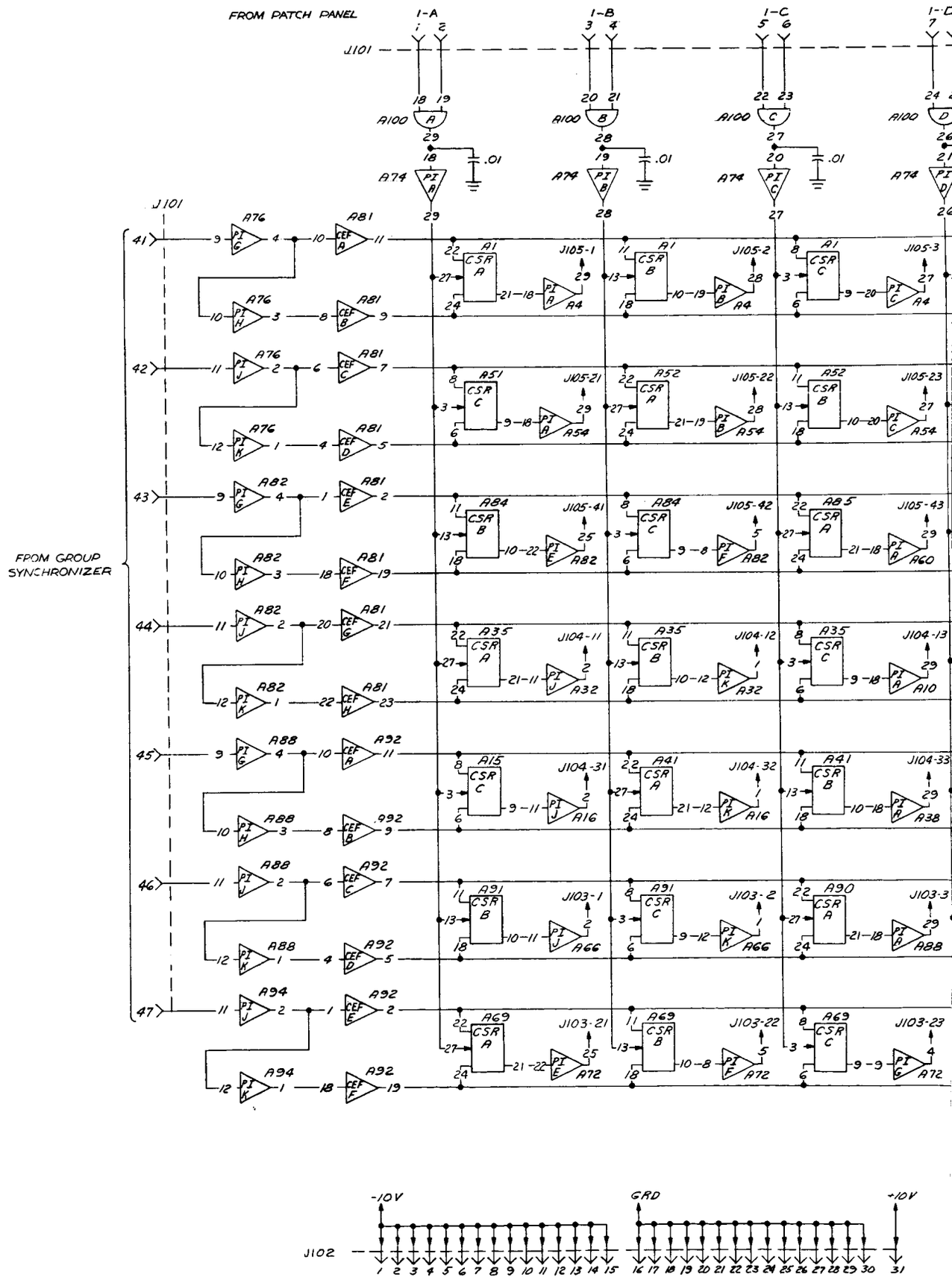


Figure I-39. Decommutator, Logic Diagram (Sheet 2 of 2)


FROM PATCH PANEL
1-A
1-B
1-C
J101
A100
A74
.01
FROM GROUP SYNCHRONIZER
A76
A81
A82
A88
A92
A94
A1
A51
A52
A84
A85
A35
A15
A41
A91
A90
A69
J105-1
J105-2
J105-3
J105-21
J105-22
J105-23
J105-41
J105-42
J105-43
J104-11
J104-12
J104-13
J104-31
J104-32
J104-33
J103-1
J103-2
J103-3
J103-21
J103-22
J103-23
-10V
GRD
+10V
J102

1-45-1

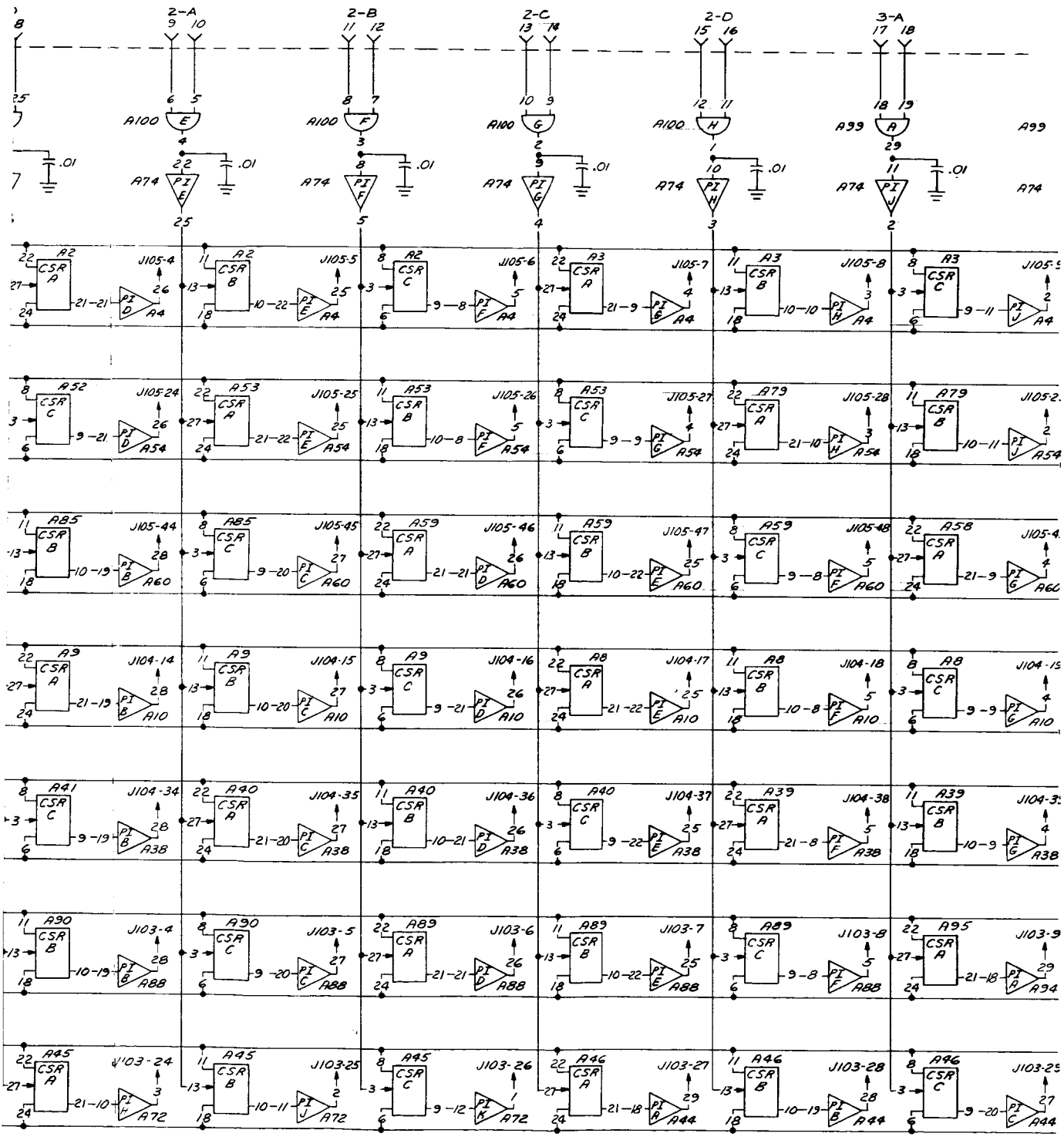
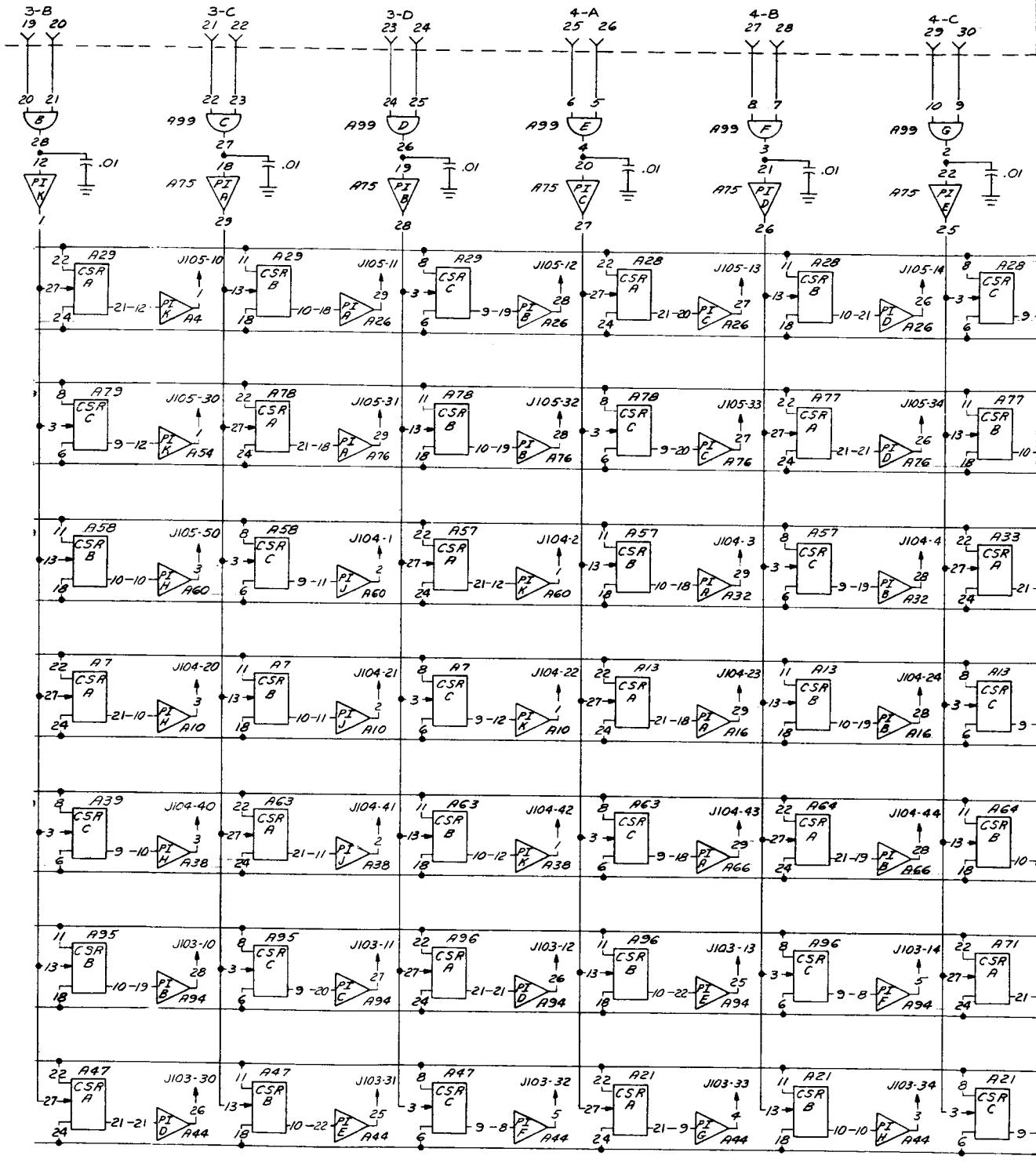


Figure I-40. Digital Decommutator, Logic Diagram (Sheet 1 of 2)


3-B
3-C
3-D
4-A
4-B
4-C
A99
A75
.01
A29
A28
A79
A78
A77
A58
A57
A33
A7
A13
A39
A63
A64
A95
A96
A71
A47
A21
J105-10
J105-11
J105-12
J105-13
J105-14
J105-30
J105-31
J105-32
J105-33
J105-34
J105-50
J104-1
J104-2
J104-3
J104-4
J104-20
J104-21
J104-22
J104-23
J104-24
J104-40
J104-41
J104-42
J104-43
J104-44
J103-10
J103-11
J103-12
J103-13
J103-14
J103-30
J103-31
J103-32
J103-33
J103-34
A4
A26
A54
A76
A60
A32
A10
A16
A38
A66
A94
A44

1-46-1

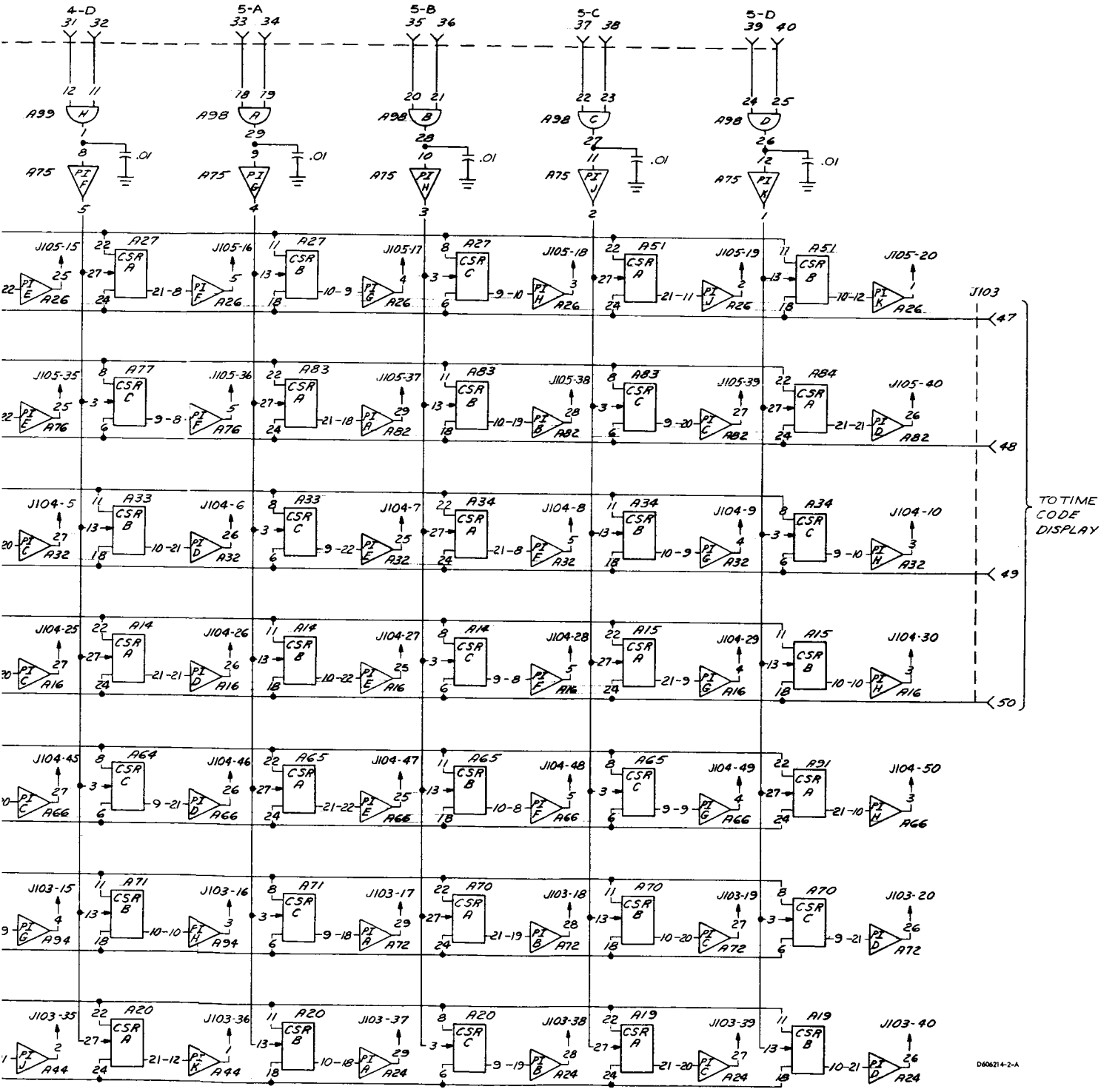
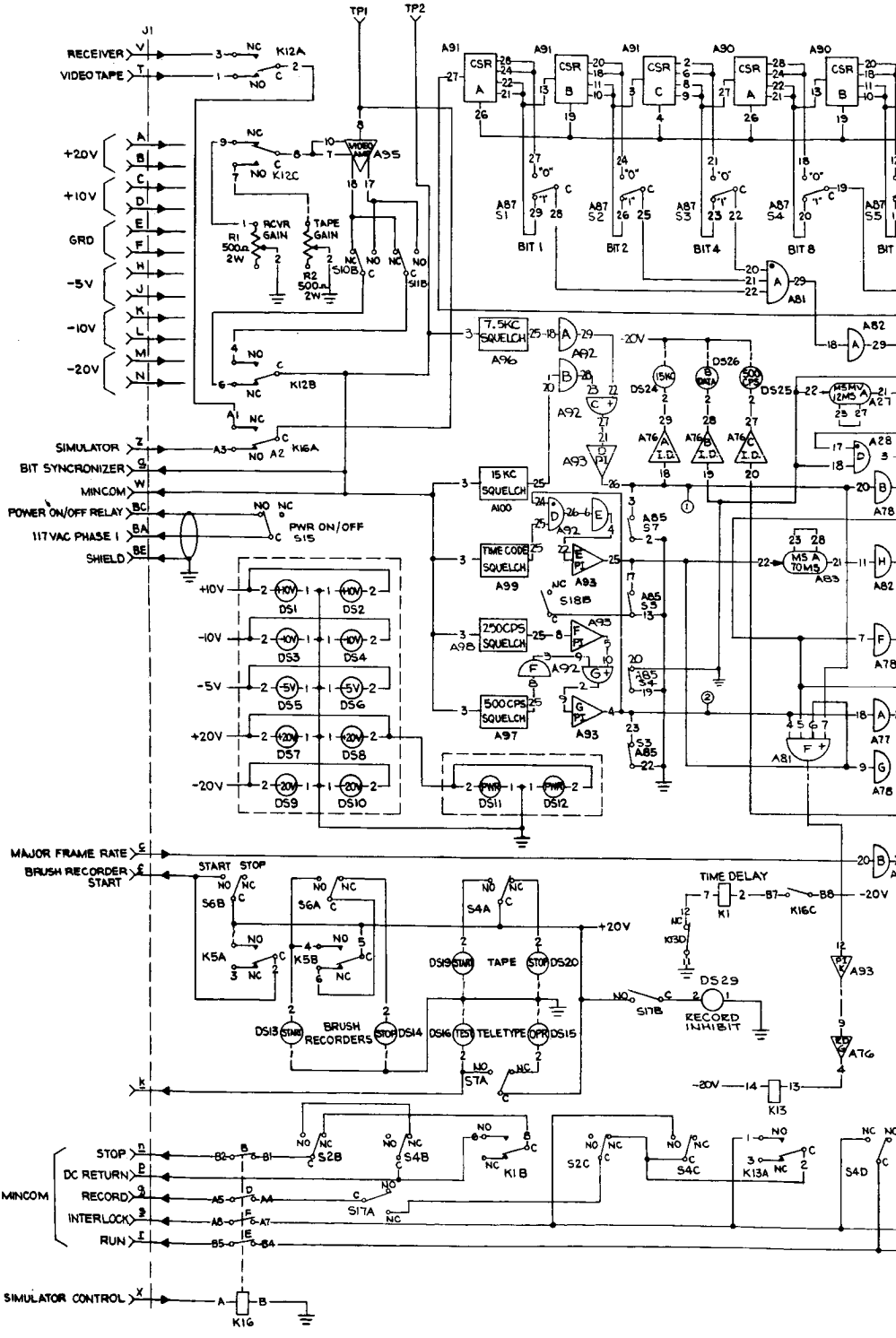


Figure I-40. Digital Decommutator, Logic Diagram (Sheet 2 of 2)


RECEIVER
VIDEO TAPE
+20V
+10V
GRD
-5V
-10V
-20V
SIMULATOR
BIT SYNCRONIZER
MINCOM
POWER ON/OFF RELAY
117 VAC PHASE I
SHIELD
MAJOR FRAME RATE
BRUSH RECORDER START
MINCOM
STOP
DC RETURN
RECORD
INTERLOCK
RUN
SIMULATOR CONTROL
TP1
TP2
RCVR GAIN
TAPE GAIN
PWR ON/OFF
7.5KC SQUELCH
15 KC SQUELCH
TIME CODE SQUELCH
250CPS SQUELCH
500CPS SQUELCH
BIT 1
BIT 2
BIT 4
BIT 8
START
STOP
TAPE
BRUSH RECORDERS
TELETYPE
TIME DELAY
RECORD INHIBIT

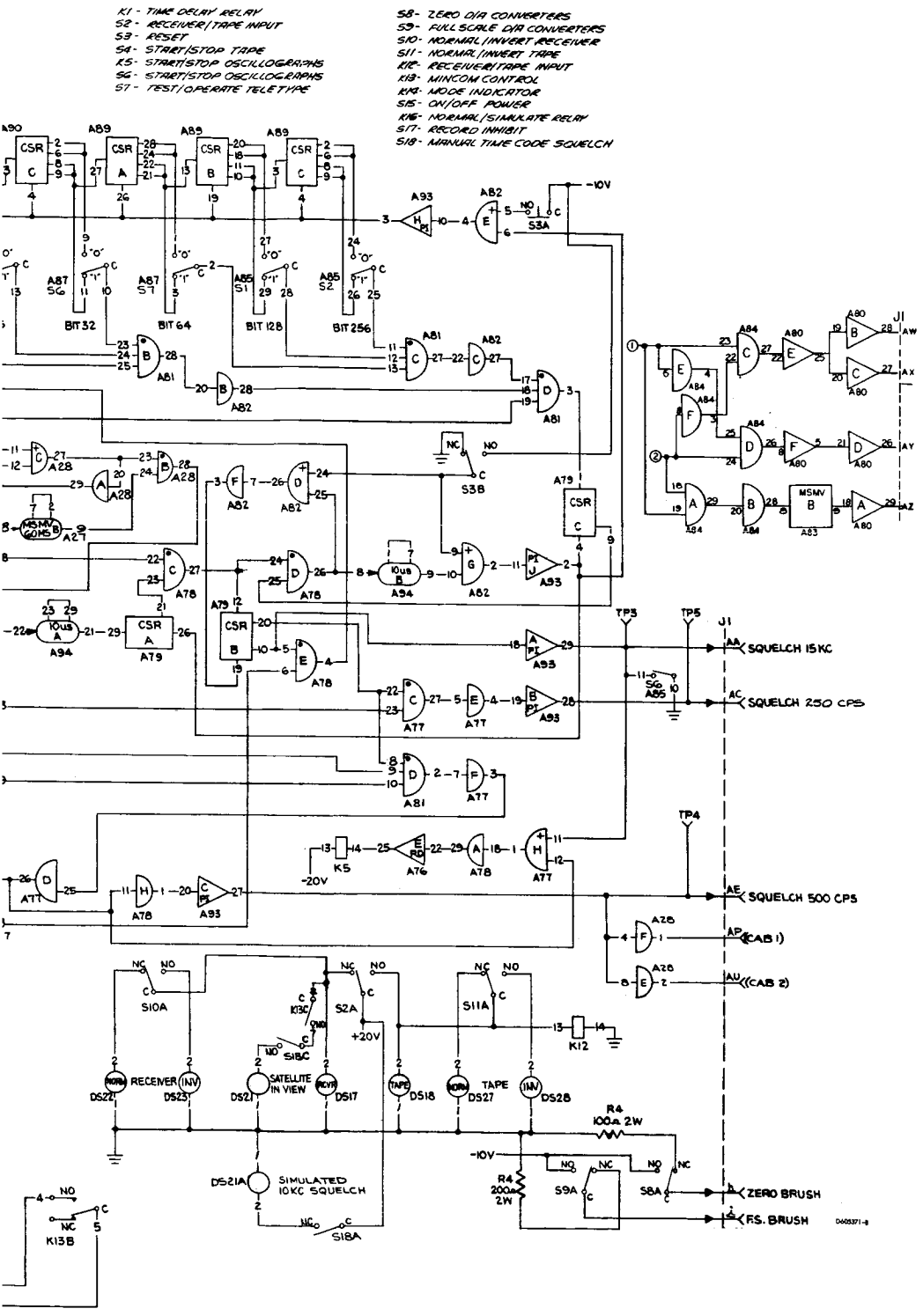


Figure 1-41. System Control, Logic Diagram

APPENDIX II

FAILURE REPORTS

There have been no significant failures during system level tests of the Nimbus Study system.

APPENDIX III

FAILURE RATE DATA SHEETS

APPENDIX III

FAILURE RATE DATA SHEETS

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RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Multiplexer Non-Redundant Circuits

S/N: _____

COMPONENT	N	* $\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Prime Digital				
MOS FET	14	.030	.420	
Diode	16	.001	.016	
Resistor, C.C.	30	.001	.030	
Sub-Com Digital				
MOS FET	56	.030	1.680	
Diode	64	.001	.064	
Resistor, C.C.	120	.001	.120	
Prime Analog				
MOS FET	8	.030	.240	
Integrated Ckt.	8	.016	.128	
Resistor, C.C.	21	.001	.021	
Sub-Com Analog				
MOS FET	128	.030	3.840	
Integrated Ckt.	128	.016	2.048	
Diode	72	.001	.072	
Resistor, C.C.	264	.001	.264	

* BASED ON TEMPERATURE AND STRESS

8.943 = λ TOTAL (%/1000 HOURS)

_____ = MTBF (HOURS)

R-277 (REV 2-64)

RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Multiplexer Redundant Circuits

S/N: _____

COMPONENT	N	* $\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Sequencers				
MOS FET	46	.030	1.380	
Integrated Ckt.	42	.016	.672	
Resistor, C.C.	95	.001	.095	
Drivers				
Integrated Ckt.	18	.016	.288	
Resistor, C.C.	114	.001	.114	
Bias and Clamp				
Diode, Signal	3	.001	.003	
Diode, Zener	6	.001	.006	
Resistor, C.C.	13	.001	.013	
Time Code, Sync, ID				
Integrated Ckt.	2	.016	.032	
Resistor, C.C.	2	.001	.002	
Output				
Custom Circuits	8	.040	.320	
Diode, Signal	2	.001	.002	
Diode, Zener	8	.001	.008	
Capacitor, Ceramic	7	.001	.007	
Resistor, C.C.	49	.001	.049	

* BASED ON TEMPERATURE AND STRESS

2.991 = λ TOTAL (%/1000 HOURS)

_____ = MTBF (HOURS)

R-277 (REV 2-64)

RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Programmer Module No. 1

S/N: Schematic 606202 - Revision-None

COMPONENT	N	* $\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Transistor	32	.002	.064	
Diode	58	.001	.058	
Capacitor				
Ceramic	11	.001	.011	
Tantalum	2	.020	.040	40 % Stress
Glass	4	.001	.004	
Resistor				
Carbon Comp.	79	.001	.079	
Metal Film	10	.022	.220	

* BASED ON TEMPERATURE AND STRESS

0.476 = λ TOTAL (%/1000 HOURS)

_____ = MTBF (HOURS)

R-277 (REV 2-64)

RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Programmer Module No. 2

S/N: Schematic 606203 - Revision-None

COMPONENT	N	* $\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Transistor	31	.002	.062	
Diode	40	.001	.040	
Capacitor				
Ceramic	12	.001	.012	
Tantalum	2	.020	.040	40 % Stress
Tantalum	2	.037	.074	50 % Stress
Met. Plastic	2	.001	.002	
Resistor				
Carbon Comp.	87	.001	.087	
Metal Film	5	.022	.110	

* BASED ON TEMPERATURE AND STRESS

0.427 = λ TOTAL (%/1000 HOURS)

[ ] = MTBF (HOURS)

R-277 (REV 2-64)

RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Programmer Module No. 3

S/N: Schematic 606204 - Revision-None

COMPONENT	N	* $\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Transistor	41	.002	.082	
Diode	33	.001	.033	
Capacitor				
Glass	3	.001	.003	
Tantalum	1	.016	.016	35 % Stress
Tantalum	2	.020	.040	40 % Stress
Tantalum	1	.037	.037	50 % Stress
Tantalum	1	.043	.043	52 % Stress
Tantalum	1	.052	.052	55 % Stress
Resistor				
Carbon Comp.	89	.001	.089	
Metal Film	2	.022	.044	
Thermistor	1	.030	---	

* BASED ON TEMPERATURE AND STRESS

0.439 = λ TOTAL (%/1000 HOURS)

[ ] = MTBF (HOURS)

R-277 (REV 2-64)

RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Coder Module No. 1

S/N: Schematic 606205 - Revision A

COMPONENT	N	* $\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Transistor	20	.002	.040	
MOS FET	1	.030	.030	
Diode				
Signal	19	.001	.019	
Zener	6	.001	.006	
Capacitor				
Mylar	2	.001	.002	
Ceramic	5	.001	.005	
Ceramic	1	.001	.001	20 % Stress
Tantalum	1	.010	.010	25 % Stress
Tantalum	1	.025	.025	43 % Stress
Tantalum	1	.180	.180	75 % Stress
Resistor				
Carbon Comp.	26	.001	.026	
Carbon Comp.	1	.001	.001	14 % Stress
Metal Film	22	.022	.484	

* BASED ON TEMPERATURE AND STRESS

0.829 = λ TOTAL (%/1000 HOURS)

_____ = MTBF (HOURS)

R-277 (REV 2-64)

RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Coder Module No. 2

S/N: Schematic 606206 - Revision-None

COMPONENT	N	* $\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Transistor	41	.002	.082	
Diode				
Signal	26	.001	.026	
Zener	2	.001	.002	
Capacitor				
Glass	2	.001	.002	
Ceramic	12	.001	.012	
Tantalum	1	.008	.008	17 % Stress
Tantalum	1	.020	.020	40 % Stress
Resistor				
Carbon Comp.	86	.001	.086	
Metal Film	5	.022	.110	

* BASED ON TEMPERATURE AND STRESS

0.348 = λ TOTAL (%/1000 HOURS)

_____ = MTBF (HOURS)

R-277 (REV 2-64)

RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Coder Module No. 3

S/N: Schematic 606207 - Revision-None

COMPONENT	N	* $\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Transistor	25	.002	.050	
Diode				
Signal	44	.001	.044	
Zener	1	.001	.001	
Capacitor				
Ceramic	40	.001	.040	
Resistor				
Carbon Comp.	70	.001	.070	

* BASED ON TEMPERATURE AND STRESS

0.205 = λ TOTAL (%/1000 HOURS)

[ ] = MTBF (HOURS)

R-277 (REV 2-64)

RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Output Shift Register and Split Phase Converter

S/N: Schematic 606208 - Revision-None

COMPONENT	N	* $\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Transistor	31	.002	.062	
Diode	45	.001	.045	
Capacitor				
Ceramic	22	.001	.022	
Resistor				
Carbon Comp.	97	.001	.097	

* BASED ON TEMPERATURE AND STRESS

0.226 = λ TOTAL (%/1000 HOURS)

[ ] = MTBF (HOURS)

R-277 (REV 2-64)

RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Power Supply

S/N: Schematic 515601 - Revision-None

COMPONENT	N	* $\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Transistor	4	.002	.008	
Transistor	1	.0027	.0027	21 % Stress
Diode	18	.001	.018	
Diode	1	.0012	.0012	15 % Stress
Diode	1	---	---	Monitor Point Isolation
Capacitor				
Tantalum	1	.012	.012	28 % Stress
Tantalum	3	.020	.060	40 % Stress
Tantalum	3	.028	.084	45 % Stress
Tantalum	2	.052	.104	55 % Stress
Resistor				
Carbon Comp.	6	.001	.006	
Carbon Comp.	2	.001	.002	19 % Stress
Carbon Comp.	1	---	---	Monitor Point Isolation
Metal Film	4	.022	.088	
Transformer	1	.070	.070	
Inductor	2	.050	.100	

* BASED ON TEMPERATURE AND STRESS

0.5559 = λ TOTAL (%/1000 HOURS)

[ ] = MTBF (HOURS)

R-277 (REV 2-64)

RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Record and Playback Amplifier

S/N: Schematic 515612 - Revision A

COMPONENT	N	* $\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Transistor	11	.002	.022	
Diode	4	.001	.004	
Capacitor				
Ceramic	2	.001	.002	
Tantalum	1	.008	.008	17 % Stress
Tantalum	1	.020	.020	40 % Stress
Tantalum	3	.037	.111	50 % Stress
Resistor				
Carbon Comp.	32	.001	.032	
Metal Film	9	.022	.198	
Variable WW	1	.133	.133	
Inductor	1	.050	,050	

* BASED ON TEMPERATURE AND STRESS

0.580 = λ TOTAL (%/1000 HOURS)

_____ = MTBF (HOURS)

R-277 (REV 2-64)

RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Summing Amplifier

S/N: Schematic 515613 - Revision A

COMPONENT	N	* $\lambda \times 10^{-5}$	N $\lambda \times 10^{-5}$	REMARKS
Transistor	4	.002	.008	
Diode	2	.001	.002	
Capacitor				
Ceramic	1	.001	.001	
Tantalum	1	.006	.006	
Tantalum	1	.037	.037	50 % Stress
Resistor				
Carbon Comp.	7	.001	.007	
Metal Film	1	.022	.022	

* BASED ON TEMPERATURE AND STRESS

0.083 = λ TOTAL (%/1000 HOURS)

_____ = MTBF (HOURS)

R-277 (REV 2-64)

RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Monitor Module

S/N: Schematic 409228 - Revision A

COMPONENT	N	* $\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Resistor				
Carbon Comp.	8	.001	.008	
Metal Film	2	.022	.044	
Thermistor	1	.030	.030	

* BASED ON TEMPERATURE AND STRESS

0.082 = λ TOTAL (%/1000 HOURS)

_____ = MTBF (HOURS)

R-277 (REV 2-64)

RELIABILITY CALCULATION FORM

RADIATION INCORPORATED

DATE: _____

PROJECT NO. 1858 Nimbus Study

UNIT TITLE: Tape Recorder (Raymond Engineering Laboratory)

S/N: Drawing 1631-5-1 - Revision Z and 1631-5-2 - Revision B **

COMPONENT	N	* $\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Transistor	14	.002	.028	
Diode	12	.001	.012	
Capacitor				
Tantalum	12	.037	.444	50 % Stress Assumed
Resistor				
Carbon Comp.	26	.001	.026	
Metal Film	7	.022	.154	
Wirewound	4	.014	.056	
Transformer	2	.070	.140	
Thermistor	2	.030	---	
Transducer	1	---	---	
Momentum Motor	1	.175	.175	
Record/PB Motor	1	.175	.175	
Record/PB Head	1	.018	.018	FARADA Failure Rate
Erase Head	1	.018	.018	FARADA Failure Rate
Switch	1	.010	.010	

* BASED ON TEMPERATURE AND STRESS

** Information supplied by
Irving J. Ross
NASA-Nimbus Project Office

1.256 = λ TOTAL (%/1000 HOURS)

_____ = MTBF (HOURS)

R-277 (REV 2-64)

APPENDIX IV

MECHANICAL MODEL TEST REPORT

APPENDIX IV

MECHANICAL MODEL TEST REPORT

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PART 1

NIMBUS PCM VIBRATION TESTS

Universal Report No. _____

Originator's Report No. 8741-2

Revision _____

Report Of Test On NIMBUS PULSE CODE MODULATOR (PCM) DEVELOPMENT VIBRATION

RI # 514026

PERFORMED BY: S. Wier

Authorized By: M. Kann

1858-33

	Date	Signature	
Test Initiated	1/6/66		
Test Completed	1/6/66		
Report Written By	2/2/66	S. Wier	
Technician			
Test Engineer			
Supervisor			
Supervisor			
APPROVED ENVIRONMENTAL ENGINEERING	2/2/66	[illegible]	
Government Representative (If Applicable)			
Final Release			

IV-1 PURPOSE.

To evaluate the Nimbus "B" Pulse Code Modulator (PCM) mechanical model when subjected to vibration environments required by the Nimbus qualification test specification.

IV-2 RESULTS.

The results of the vibration evaluation tests are illustrated by the attached x-y curves produced by accelerometers in and on the package housing.

IV-3 PROCEDURE.

IV-3.1 FIXTURING.

The vibration fixture used for these evaluation tests was an open ended box made of two inch magnesium plate. The end opposite the package had a cover made of one inch aluminum plate which was fastened to the box fixture with bolts. This cover was used in all axes except the thrust or vertical axis. The total weight of the fixture and the adapter plate is 130 pounds.

IV-3.2 FIXTURE MOUNTING.

The fixture is mounted to a standard three inch thick magnesium adapter plate that is attached to the shaker armature head. This plate serves as an armature stiffening member. See figure IV-1 for a sketch of the setup.

IV-3.3 PACKAGE DESCRIPTION.

The PCM consists of an exterior housing measuring 6.0" x 8.0" x 6.5" (figure IV-2), a group of plates and columns used as stack loading structure, and an electronic stack consisting of both modular and planar circuit boards. The loading structure is designed to exert a compressive load on the card stack independent of the exterior housing. The loading structure and stack are completely contained without the housing but effectively isolated from it through the use of silicone rubber.

IV-3.4 VIBRATION TESTS.

The vibration evaluation was as follows:

a. Sine vibration sweeps at various vibration levels up to a maximum of 7.1 Grms from 30 cps to 2 KCS were made. VMS recordings and X-Y records were made of the output voltages of the module and the external accelerometers.

b. Random vibration was applied to the package in the form of a flat spectrum with a bandwidth of 20 cps to 2 KCS at a Power Spectral Density of 0.2G^2/cps (approximately 20 Grms). The random response of the module accelerometer aligned with the axis of input vibration was analyzed and plotted on an X-Y recorder.

U. S. BLUE PRINT PAPER CO. CLEARPRINT 1000H

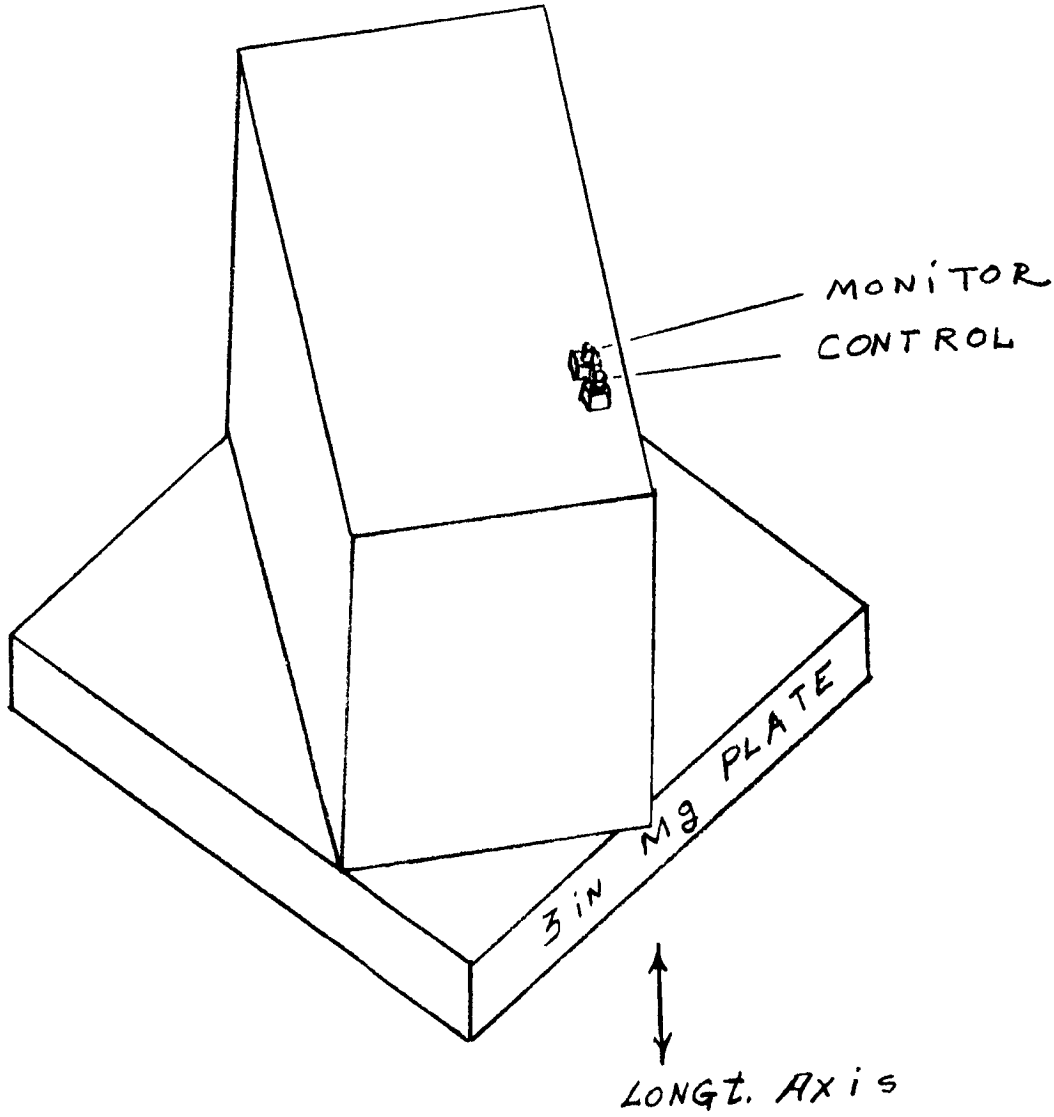

Figure IV-1

U. S. BLUE PRINT PAPER CO. CLEARPRINT 1000H

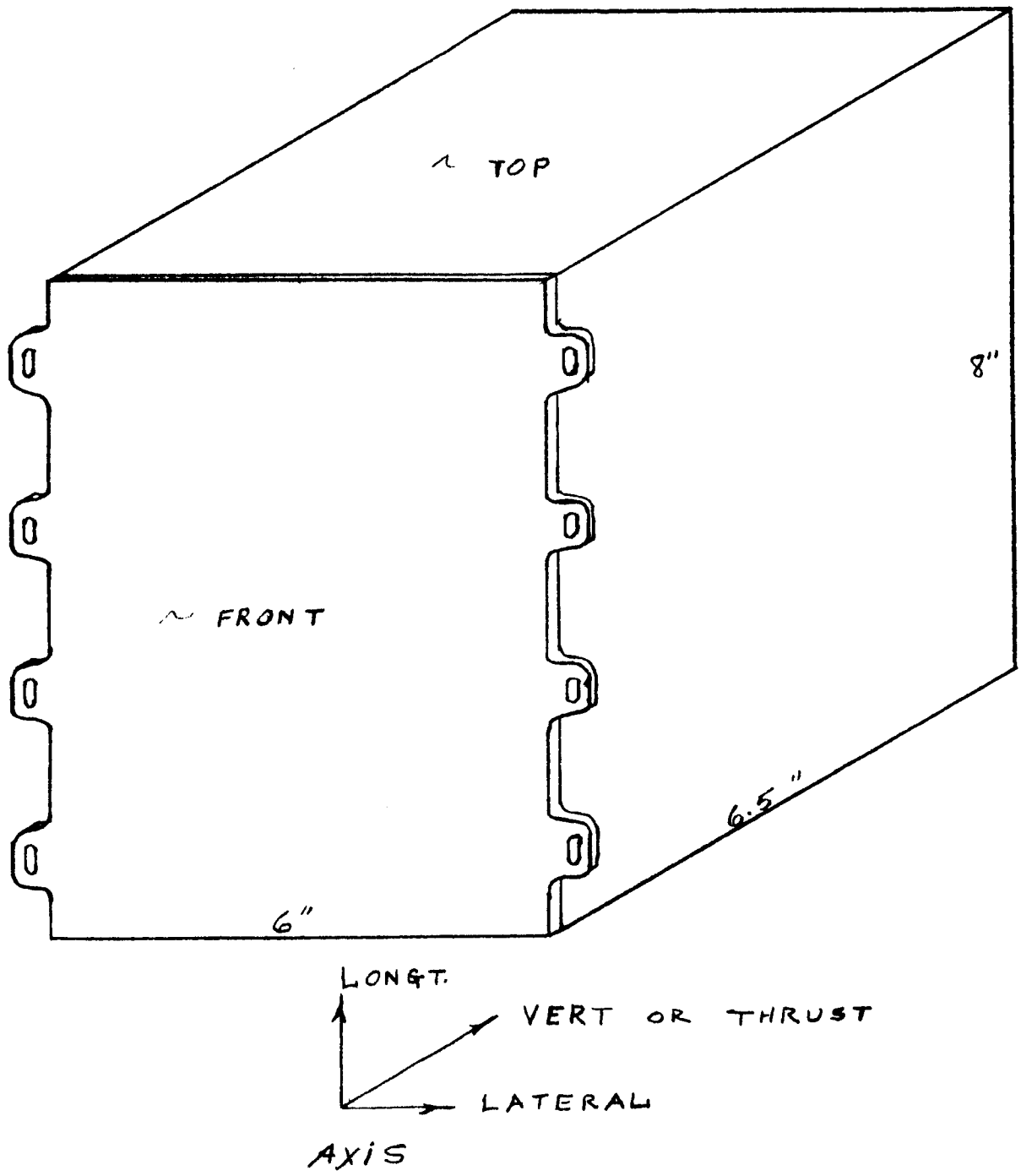

Figure IV-2

The evaluation was started in the longitudinal axis and proceeded as requested by Product Design personnel:

Longitudinal Axis Sine

Flat Pack Board - Figure IV-3
Module - Figure IV-4
Module Vertical Axis Crosstalk - Figure IV-5
Module Lateral Axis Crosstalk - Figure IV-6
Module Vertical Axis Crosstalk - Figure IV-7

Longitudinal Axis Random

Flat Pack Board Random Analysis - Figure IV-8
Module Random Analysis - Figure IV-9

Lateral Axis Sine

Flat Pack Board - Figure IV-10
Module - Figure IV-11

Lateral Axis Random

Flat Pack Board Random Analysis - Figure IV-12
Module Random Analysis - Figure IV-13

Vertical or Thrust Axis Sine

Flat Pack Board - Figure IV-14
Module - Figure IV-15
Flat Pack Board Lateral Crosstalk - Figure IV-16
Module Lateral Crosstalk - Figure IV-17
Flat Pack Board Longitudinal Crosstalk - Figure IV-18

Vertical or Thrust Random

Flat Pack Board Random Analysis - Figure IV-19
Module Random Analysis - Figure IV-20

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS LONGt

TEST ARTICLE Mock Model 8 in INPUT LEVEL 2 & 7.1 G's Rms

RUN NO. 40 & 40A ACCEL. LOCATION ON Module Board

TEST DATE 1/6/66 ACCEL. SER. NO. R37

OPERATOR WiER ACCEL. SENSITIVE AXIS LONG t

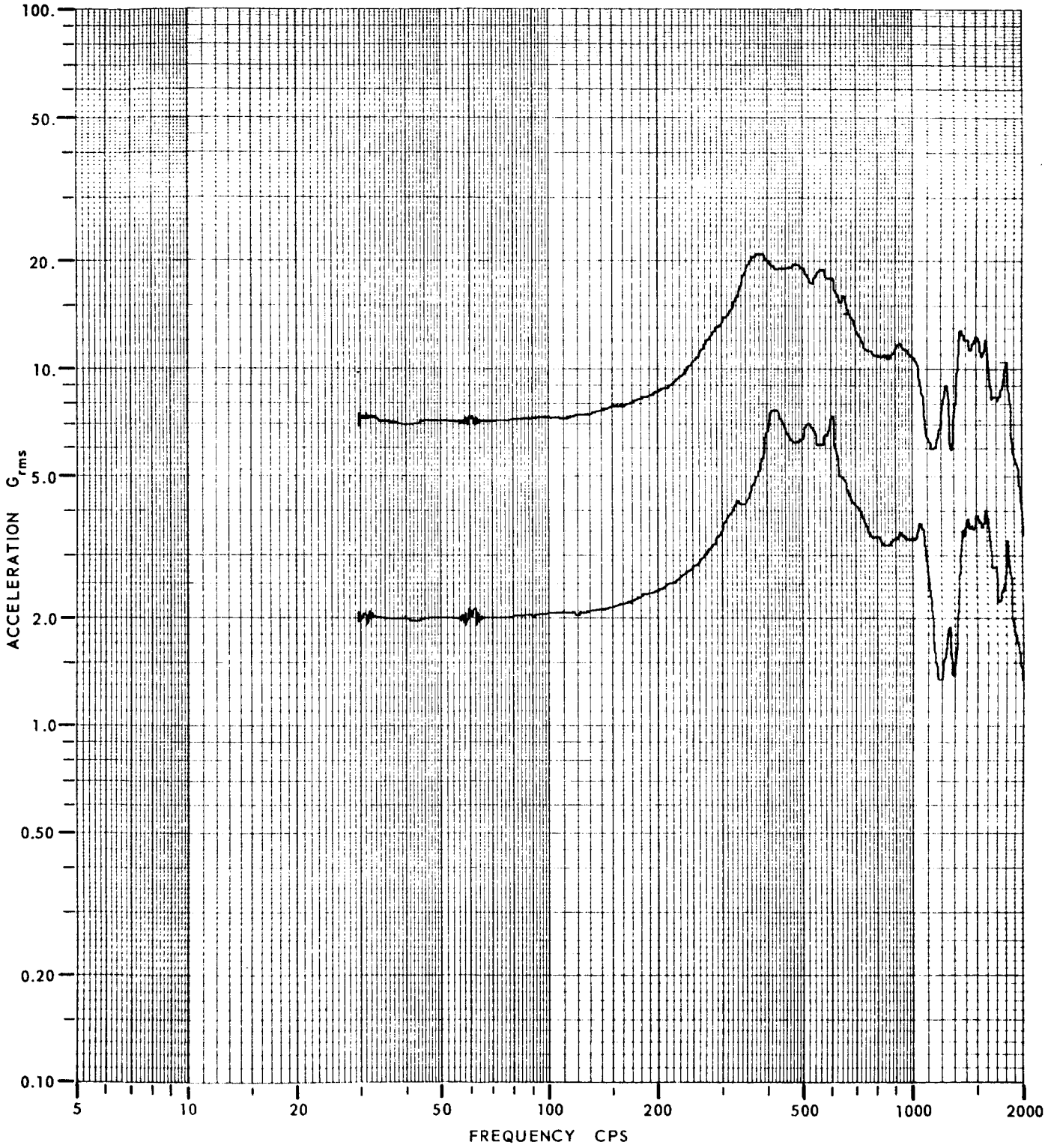

Figure IV-3

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS LONGt.

TEST ARTICLE 8 in. Mech Model INPUT LEVEL 2 & 7.1 G rms

RUN NO. 41 & 41A ACCEL. LOCATION in Module

TEST DATE 1/6/66 ACCEL. SER. NO. 413

OPERATOR WIER ACCEL. SENSITIVE AXIS LONGt.

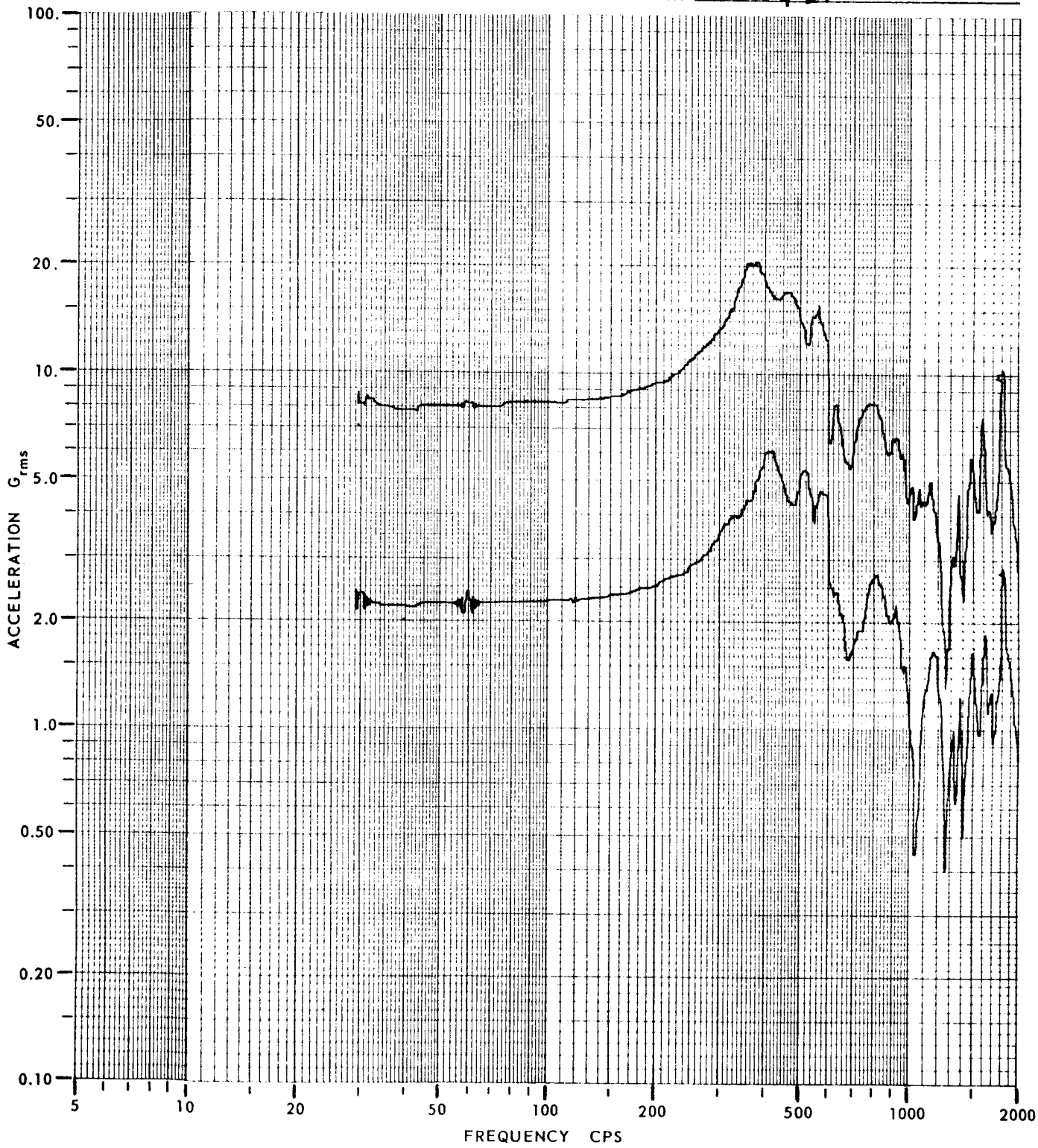

Figure IV-4

R-466

VIBRATION TEST DATA

PROJECT 1858

TEST ARTICLE 8 in. Mech. Model

RUN NO. 42

TEST DATE 1/6/66

OPERATOR Wier

INPUT AXIS LONG t

INPUT LEVEL 2 G rms

ACCEL. LOCATION Module

ACCEL. SER. NO. 399

ACCEL. SENSITIVE AXIS Vert. (Thrust)

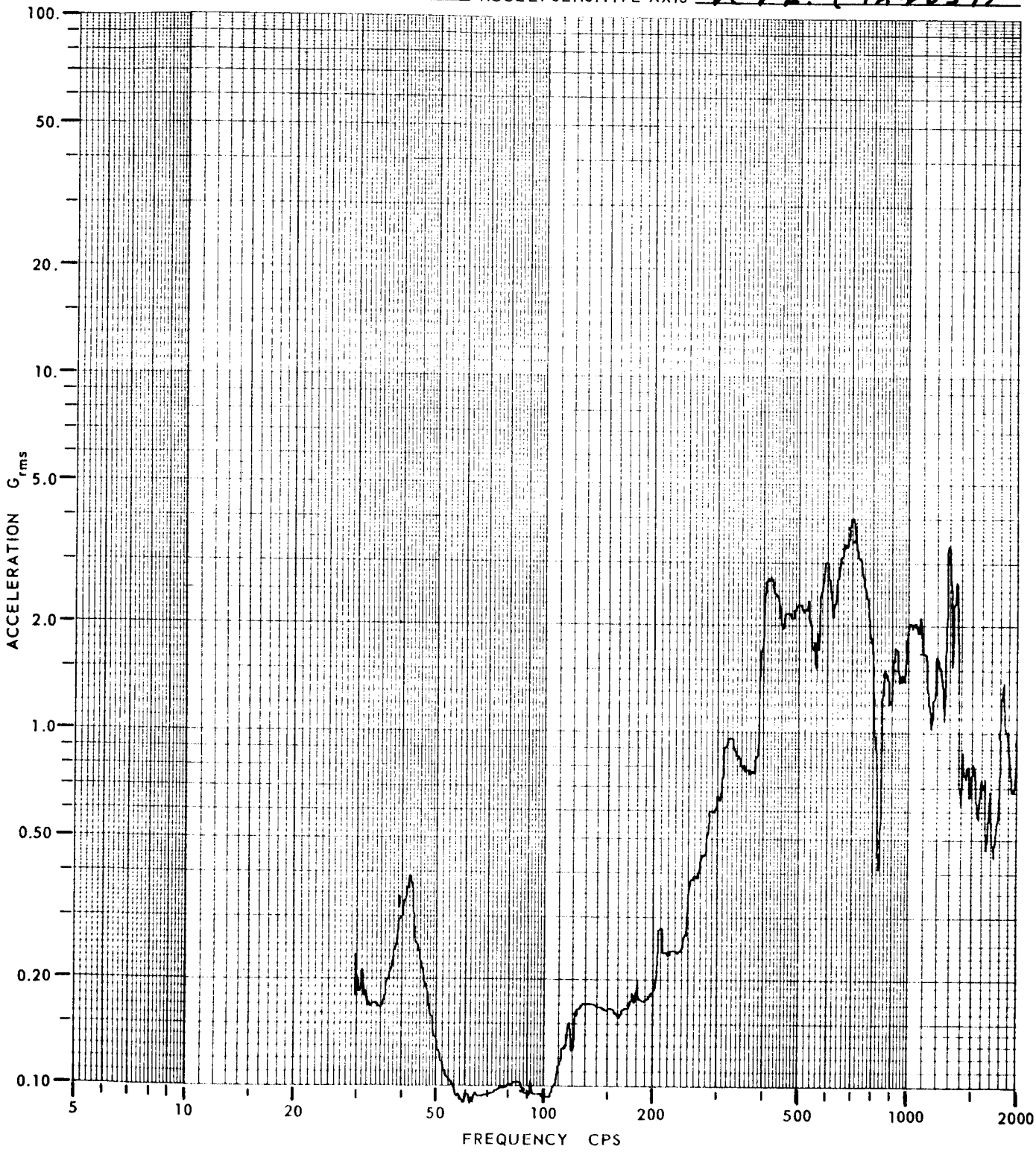

Figure IV-5

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS LONG

TEST ARTICLE 8 in Mech Model INPUT LEVEL 2 Grms

RUN NO. 43 ACCEL. LOCATION Module

TEST DATE 1/6/66 ACCEL. SER. NO. 129

OPERATOR Wier ACCEL. SENSITIVE AXIS LAT CROSS-TALK

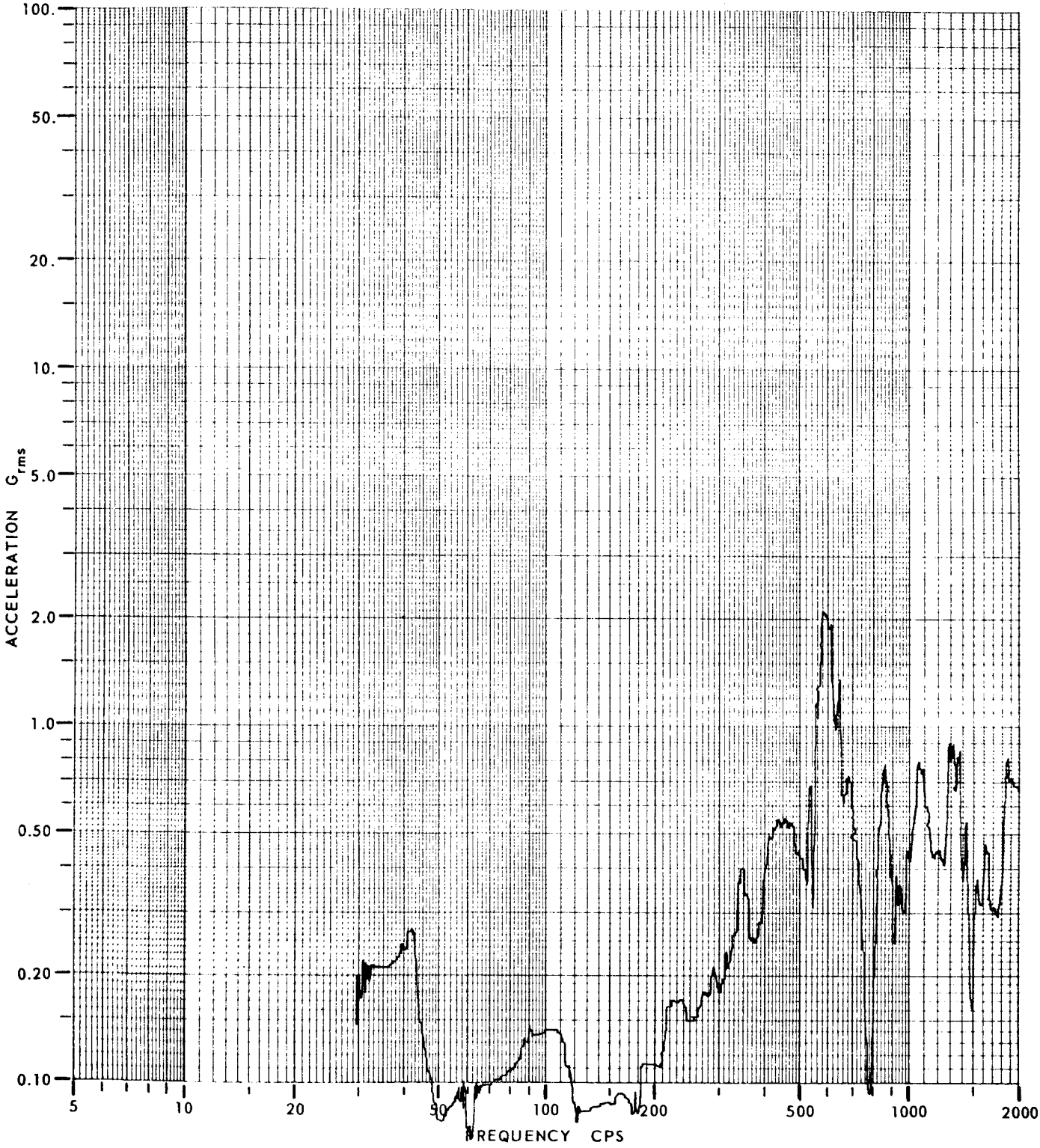

Figure IV-6

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS LONGt

TEST ARTICLE 8in Mech Model INPUT LEVEL 7.1 Grms

RUN NO. 44 ACCEL. LOCATION Module

TEST DATE 1/6/66 ACCEL. SER. NO. 399

OPERATOR WIER ACCEL. SENSITIVE AXIS Vert. (Thrust)

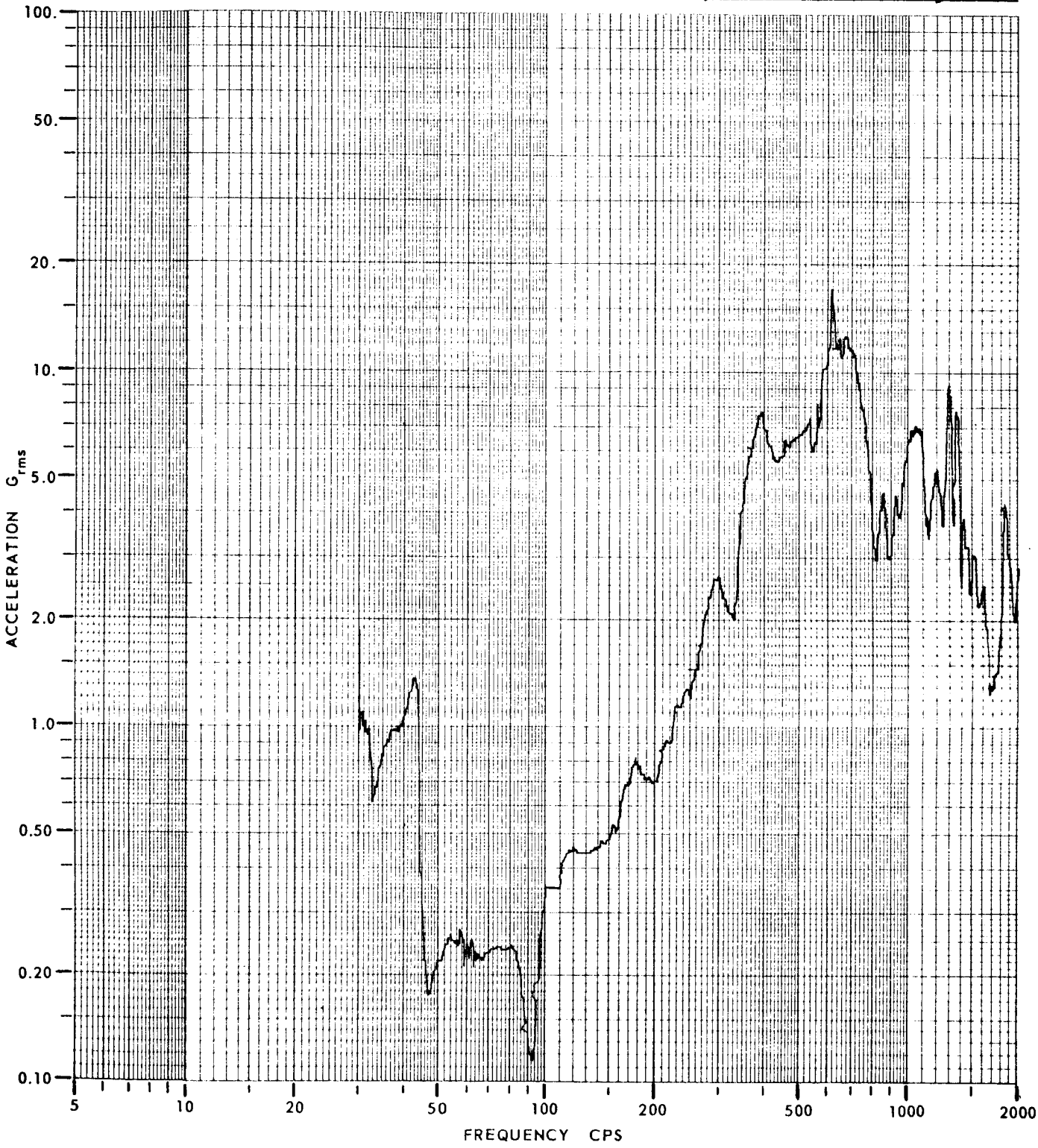

Figure IV-7

R-466-4

VIBRATION TEST DATA

PROJECT 1858
TEST ARTICLE 8 in Model
RUN NO. 45
TEST DATE 1/6/66
OPERATOR Wier

INPUT AXIS LONG t.
INPUT LEVEL .2 G²/cps (≈20G rms)
ACCEL. LOCATION Module Board
ACCEL. SER. NO. 237
ACCEL. SENSITIVE AXIS LONG t.

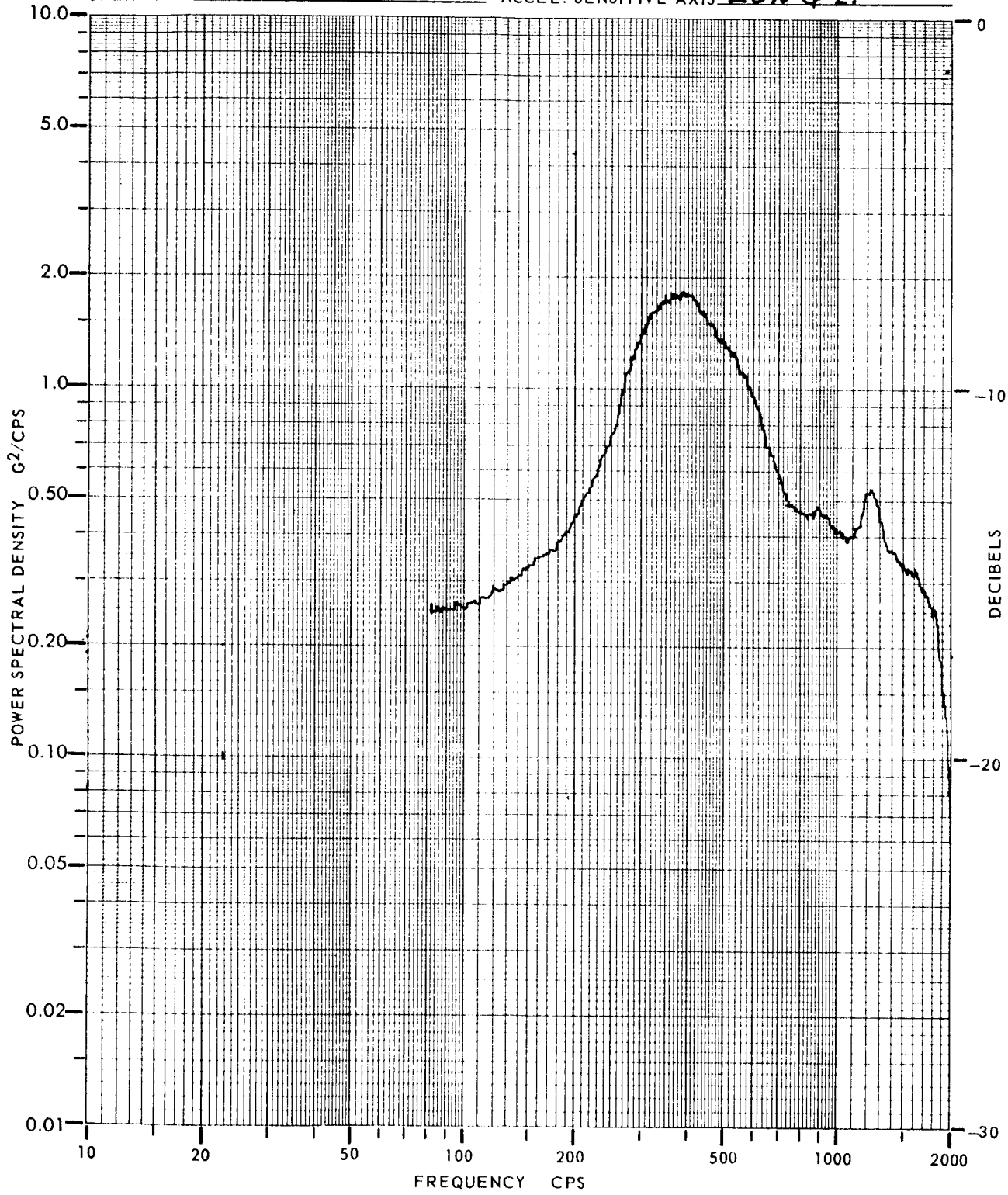

Figure IV-8

R-466-4

VIBRATION TEST DATA

PROJECT 1858
TEST ARTICLE B in Mech. Model
RUN NO. 46
TEST DATE 1/6/66
OPERATOR Wier

INPUT AXIS LONGT.
INPUT LEVEL .2 G²/CPS (≈20 GRMS)
ACCEL. LOCATION Module
ACCEL. SER. NO. 413
ACCEL. SENSITIVE AXIS LONGT

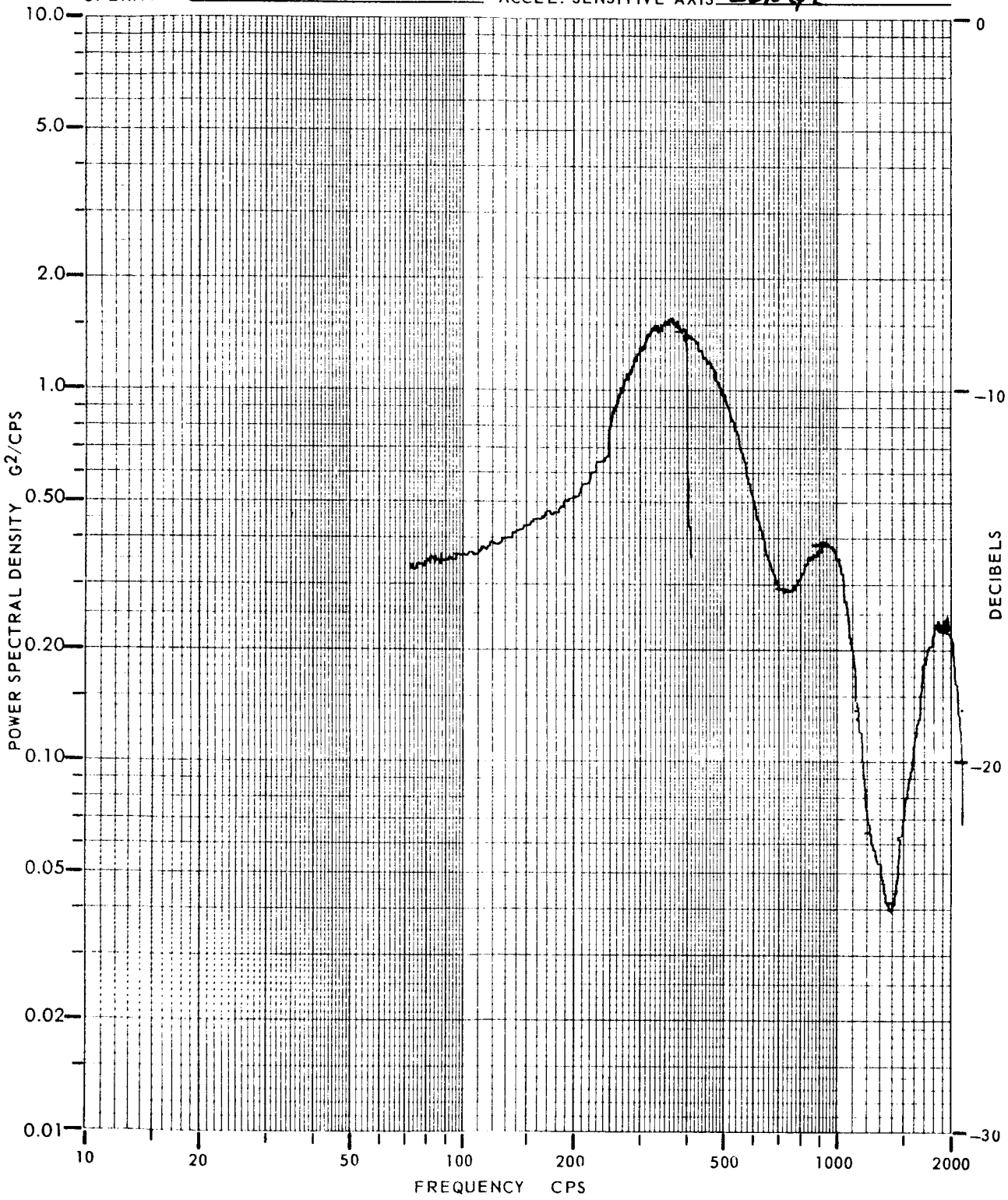

Figure IV-9

R-466

VIBRATION TEST DATA

PROJECT 1858

TEST ARTICLE 8 in Model

RUN NO. 47

TEST DATE 1/6/66

OPERATOR Wier

INPUT AXIS LAT

INPUT LEVEL 2 & 7.1G rms

ACCEL. LOCATION BOARD

ACCEL. SER. NO. 456

ACCEL. SENSITIVE AXIS LAT

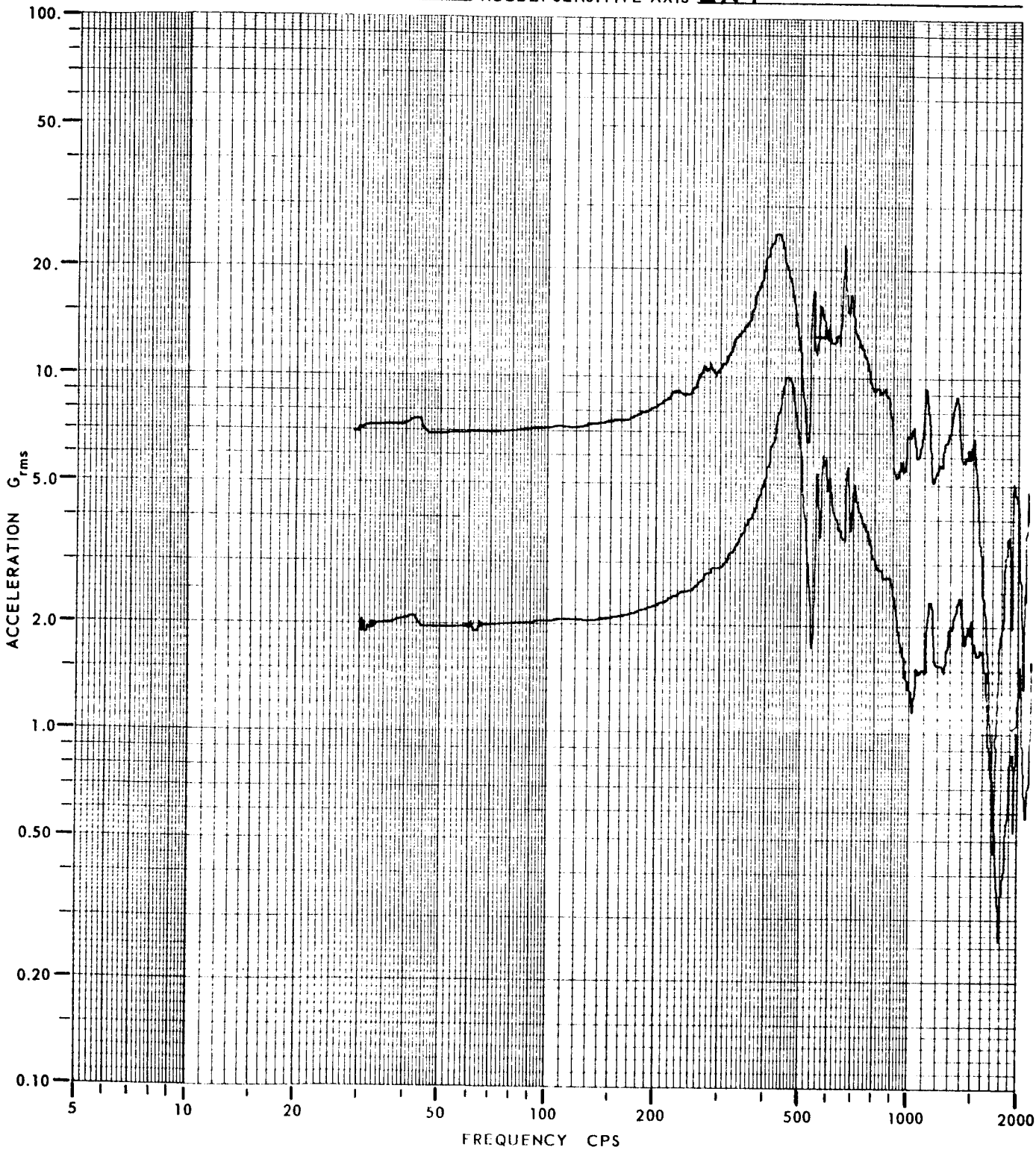

Figure IV-10

R-466

VIBRATION TEST DATA

PROJECT 1858
TEST ARTICLE 8 in Model
RUN NO. 48
TEST DATE 1/6/66
OPERATOR Wier

INPUT AXIS LAT.
INPUT LEVEL 2 & 7.1 GRMS
ACCEL. LOCATION Module
ACCEL. SER. NO. 429
ACCEL. SENSITIVE AXIS LAT.

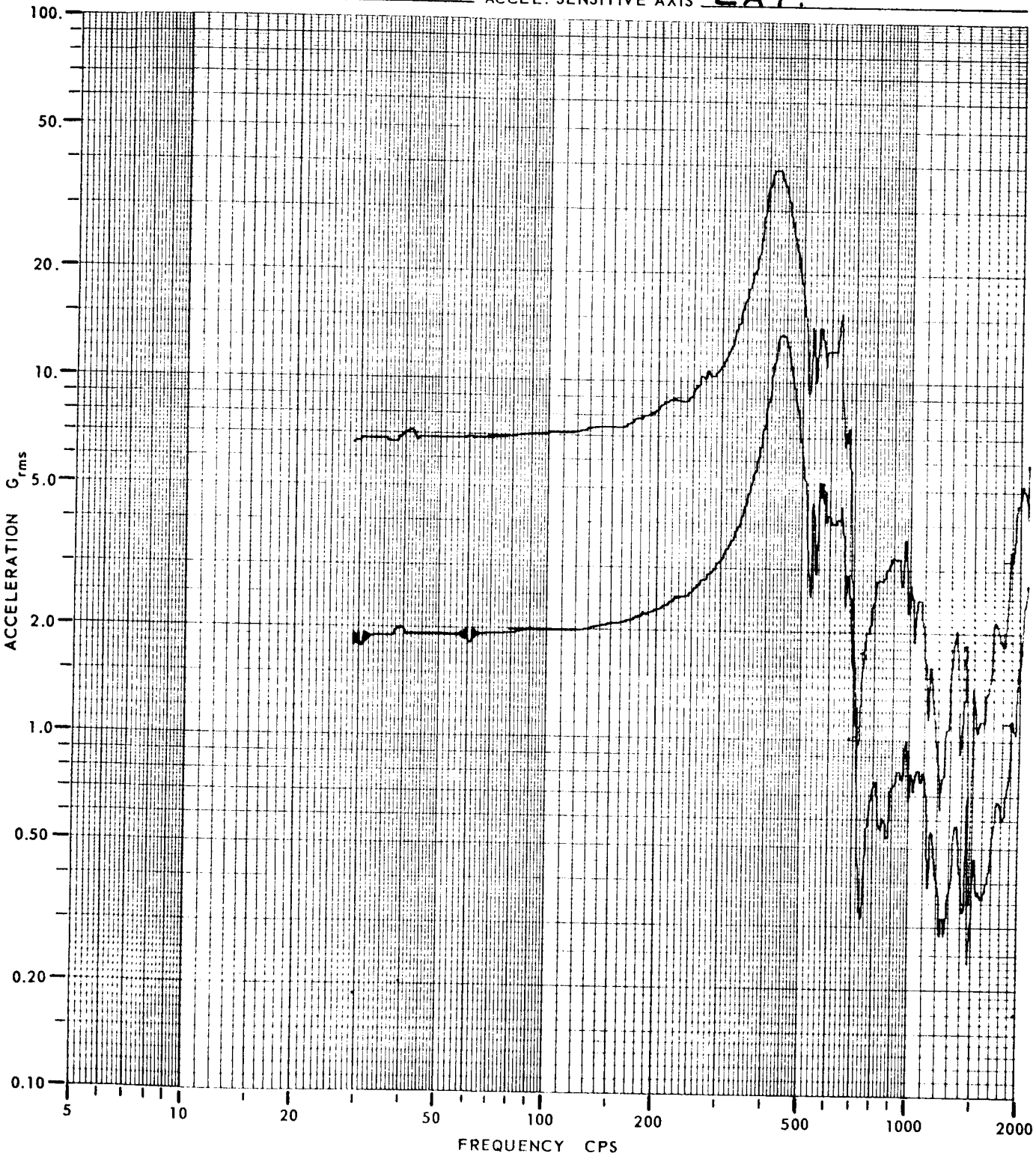

Figure IV-11

R-466 4

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS LAT

TEST ARTICLE 8 in Mech Model INPUT LEVEL .2 G²/CPS 20 RMSG

RUN NO. 48 ACCEL. LOCATION BOARD

TEST DATE 1/6/66 ACCEL. SER. NO. 456

OPERATOR wier ACCEL. SENSITIVE AXIS LAT

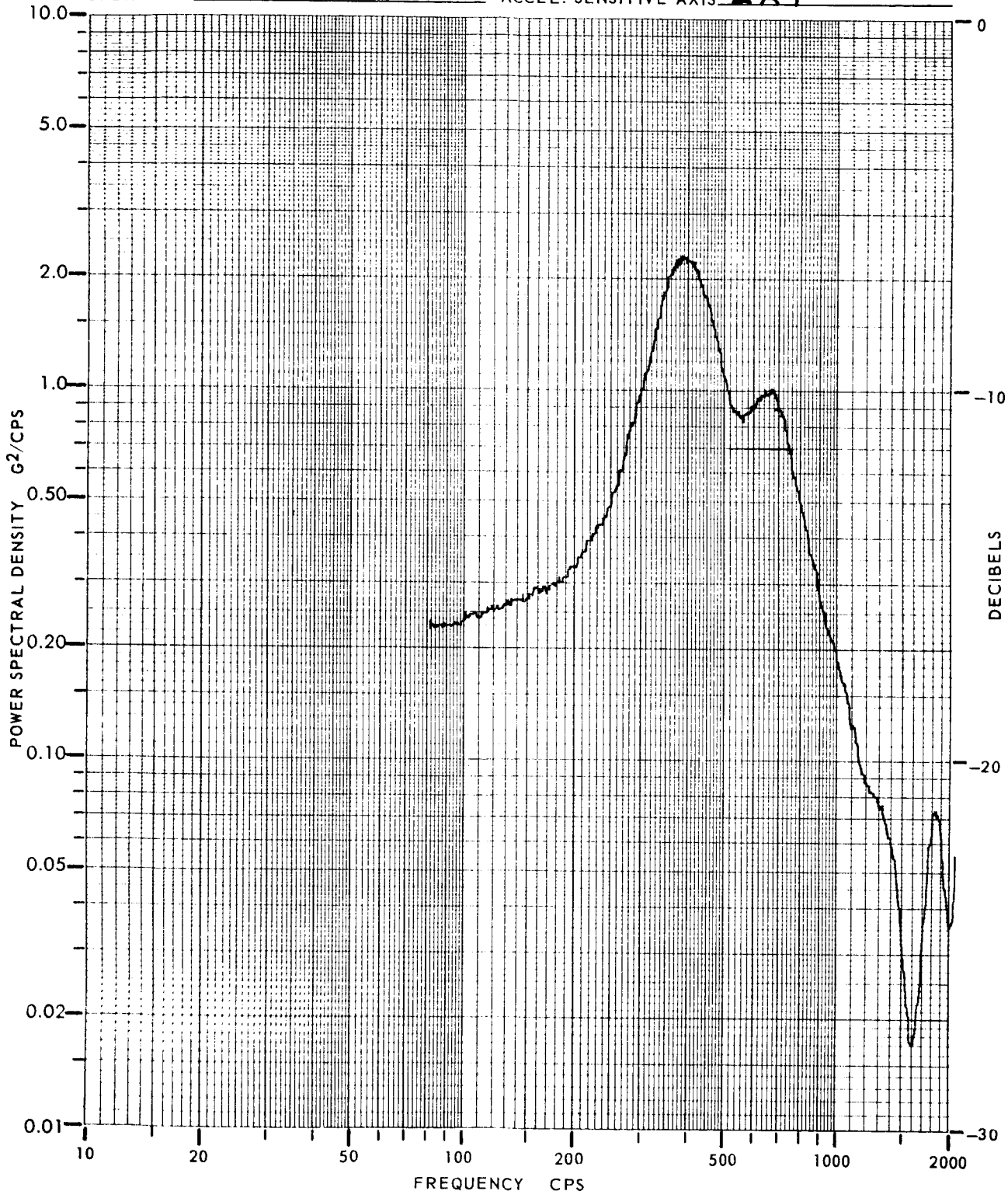

Figure IV-12

R-466-4

VIBRATION TEST DATA

PROJECT 1858
TEST ARTICLE 8in Mech. Model
RUN NO. 49
TEST DATE 1/6/66
OPERATOR wiPR

INPUT AXIS LAT
INPUT LEVEL .2 G²/CPS 20RMSG
ACCEL. LOCATION Module
ACCEL. SER. NO. 429
ACCEL. SENSITIVE AXIS LAT

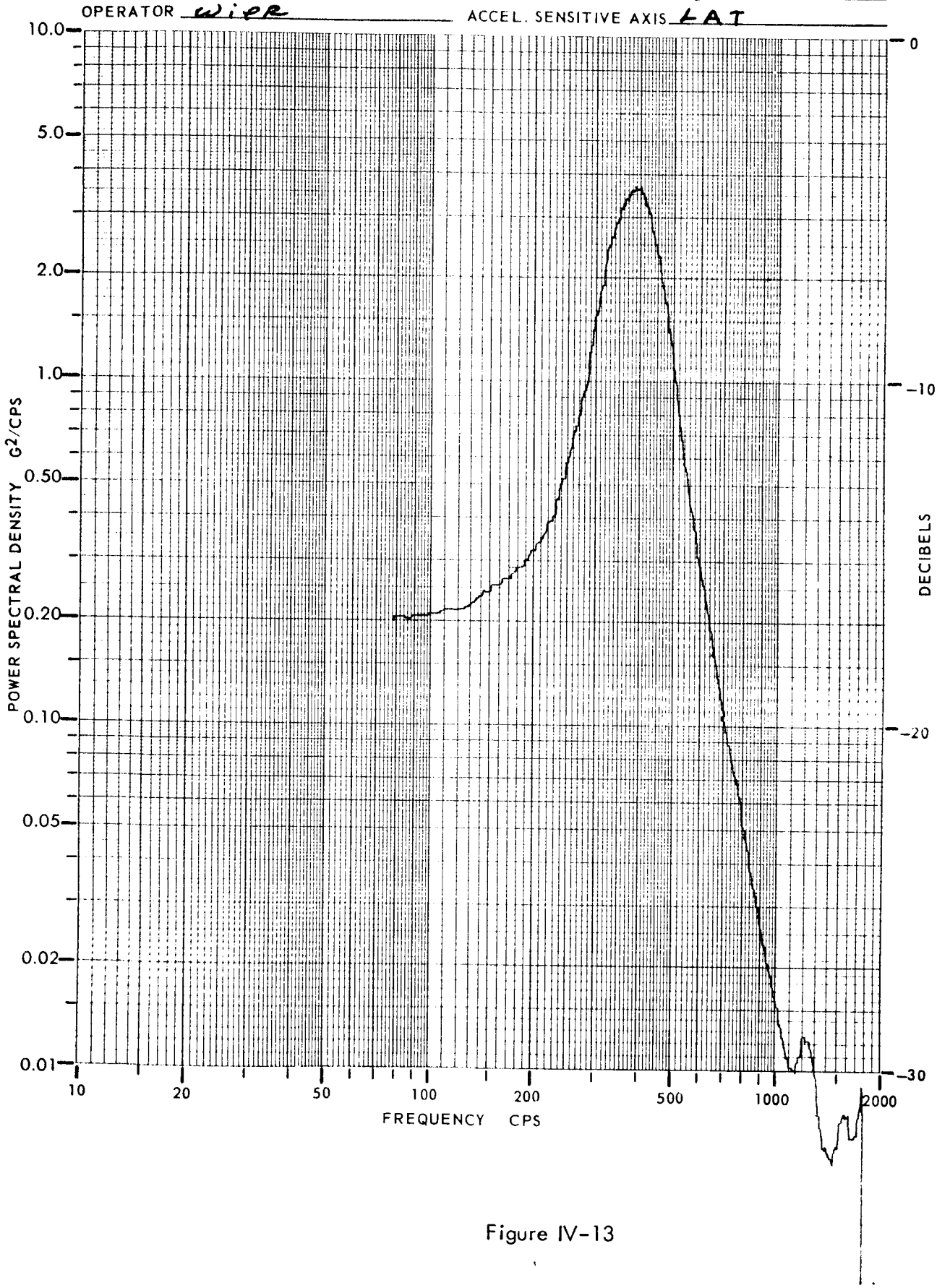

Figure IV-13

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS VERT (Thrust)

TEST ARTICLE 8 in Mech. Model INPUT LEVEL 2 ¢ 7.1 Grms

RUN NO. 51 ACCEL. LOCATION BOARD

TEST DATE 1/6/66 ACCEL. SER. NO. 456

OPERATOR WIER ACCEL. SENSITIVE AXIS VERT (Thrust)

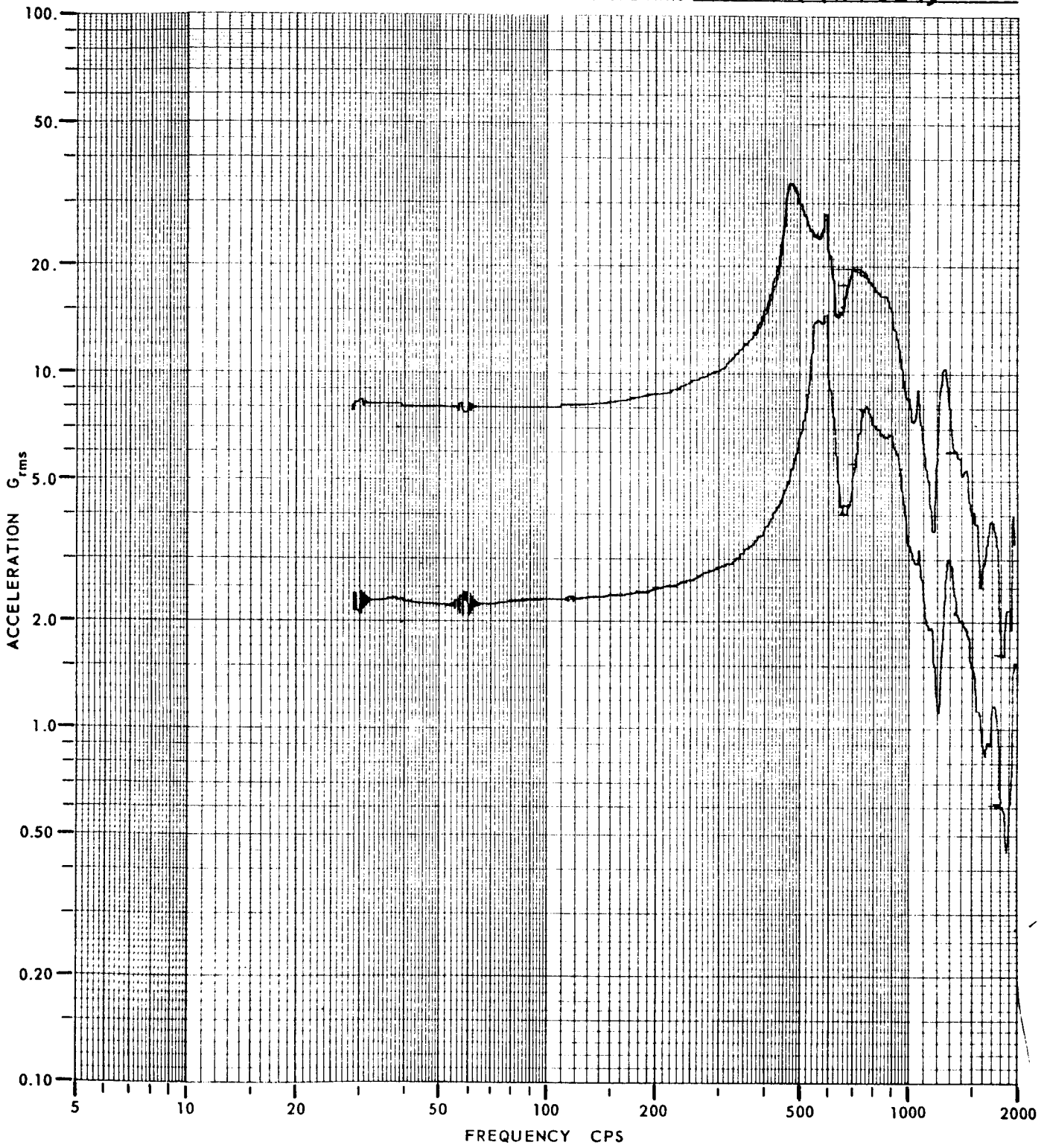

Figure IV-14

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS Vert. (Thrust)

TEST ARTICLE 8 in Mech Model INPUT LEVEL 2 ¢ 7.1 Grms

RUN NO. 50 ACCEL. LOCATION Module

TEST DATE 1/6/66 ACCEL. SER. NO. 399

OPERATOR WIER ACCEL. SENSITIVE AXIS Vert

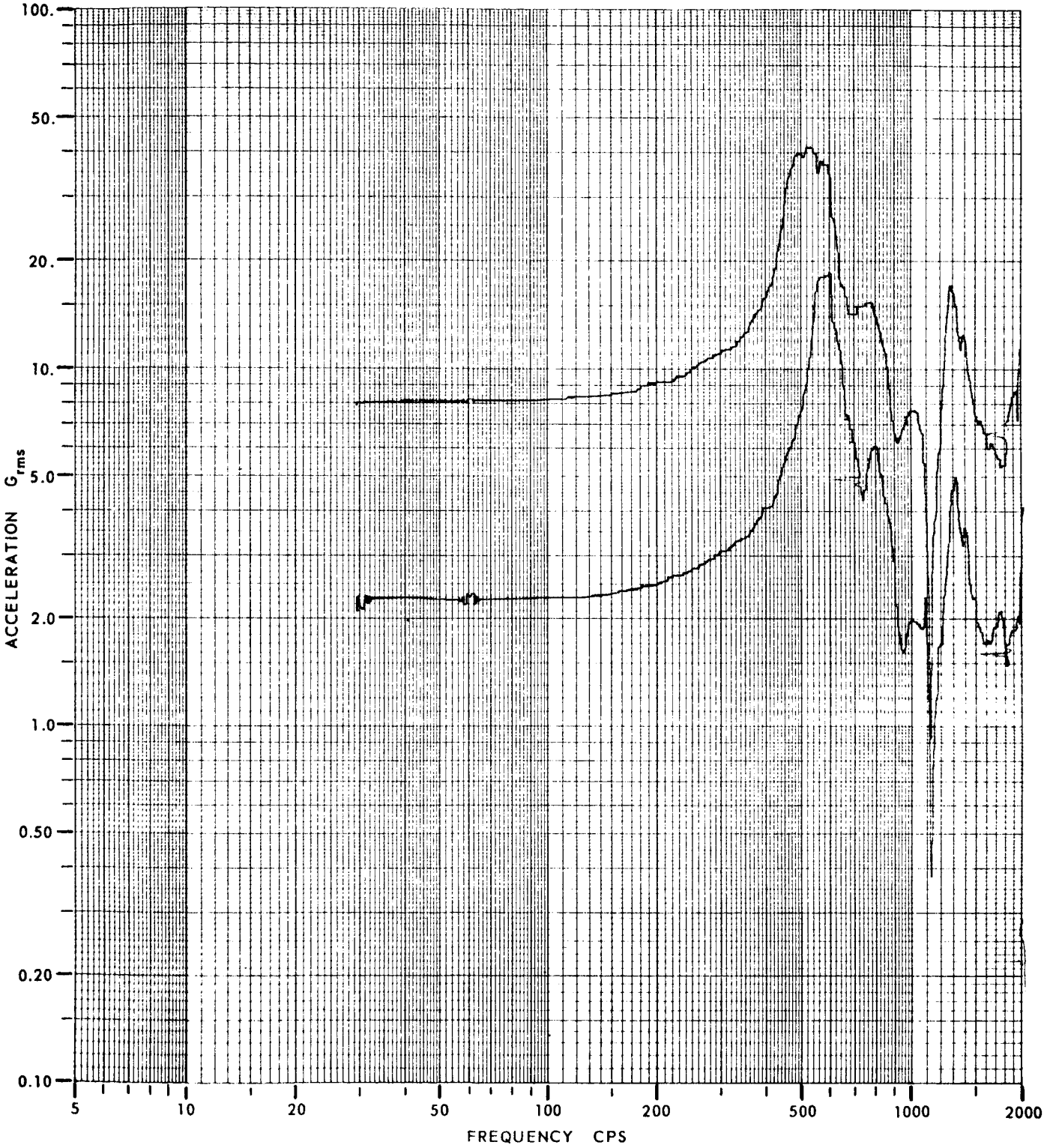

Figure IV-15

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS Vert.

TEST ARTICLE Bin Model INPUT LEVEL 2 G rms

RUN NO. ~~42~~ 52 ACCEL. LOCATION BOARD

TEST DATE 1/6/66 ACCEL. SER. NO. 405

OPERATOR WIER ACCEL. SENSITIVE AXIS LAT C-T

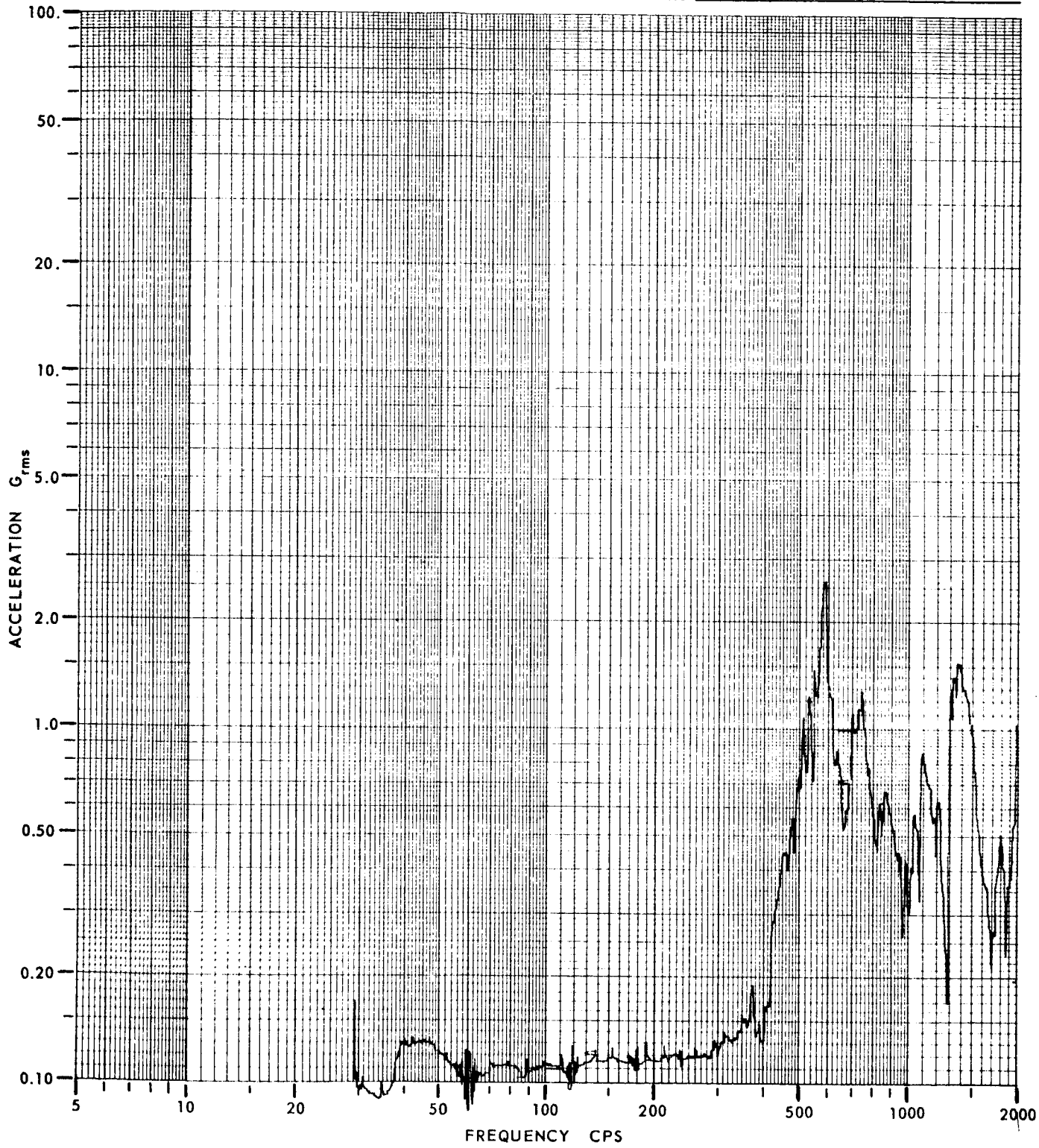

Figure IV-16

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS Vert

TEST ARTICLE Bin Model INPUT LEVEL 2 Grms

RUN NO. ~~50~~ 53 ACCEL. LOCATION Module

TEST DATE 1/6/66 ACCEL. SER. NO. 429

OPERATOR Wier ACCEL. SENSITIVE AXIS LAT C-T

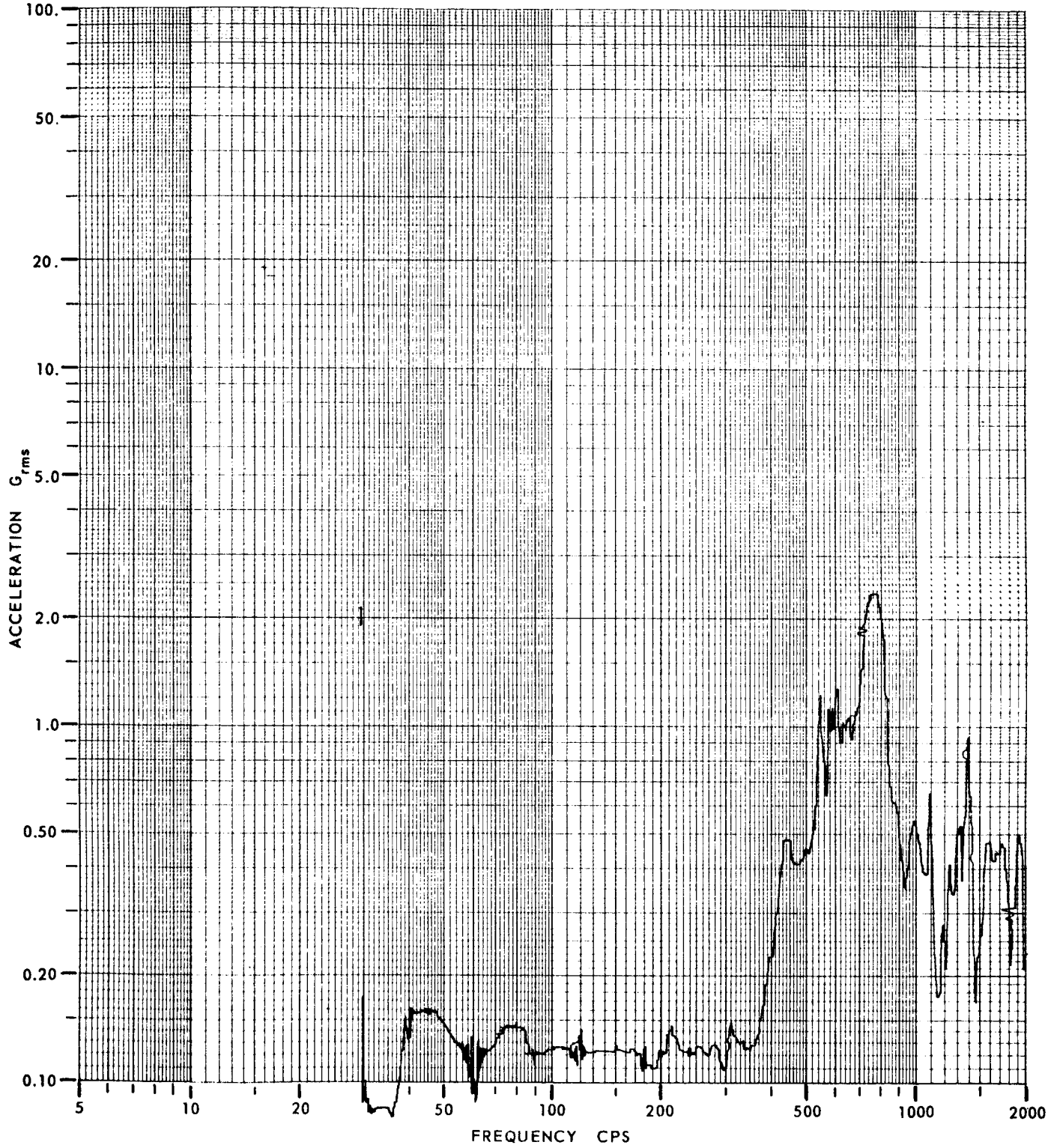

Figure IV-17

R-466

VIBRATION TEST DATA

PROJECT 185B
TEST ARTICLE Bin Mech Model
RUN NO. 54
TEST DATE 1/6/66
OPERATOR WICR

INPUT AXIS Vert
INPUT LEVEL 2 & 7.1 G rms
ACCEL. LOCATION BOARD
ACCEL. SER. NO. 237
ACCEL. SENSITIVE AXIS LONGT C-T

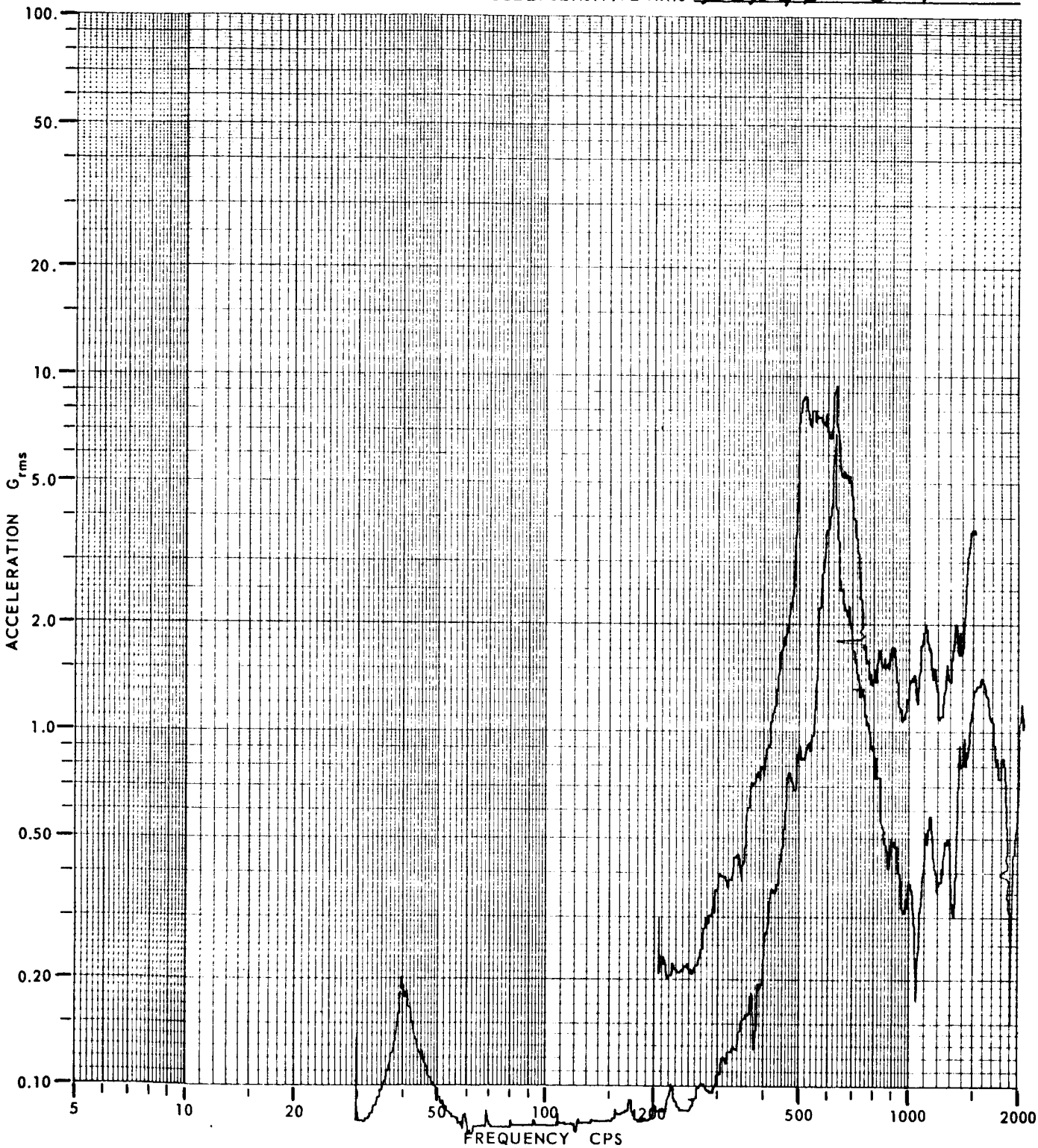

Figure IV-18

R-466-4

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS Vert

TEST ARTICLE Bin Mech Model INPUT LEVEL .2 G²/CPS (20 RMSg)

RUN NO. 56 ACCEL. LOCATION BOARD

TEST DATE 1/6/66 ACCEL. SER. NO. 456

OPERATOR Wier ACCEL. SENSITIVE AXIS Vert

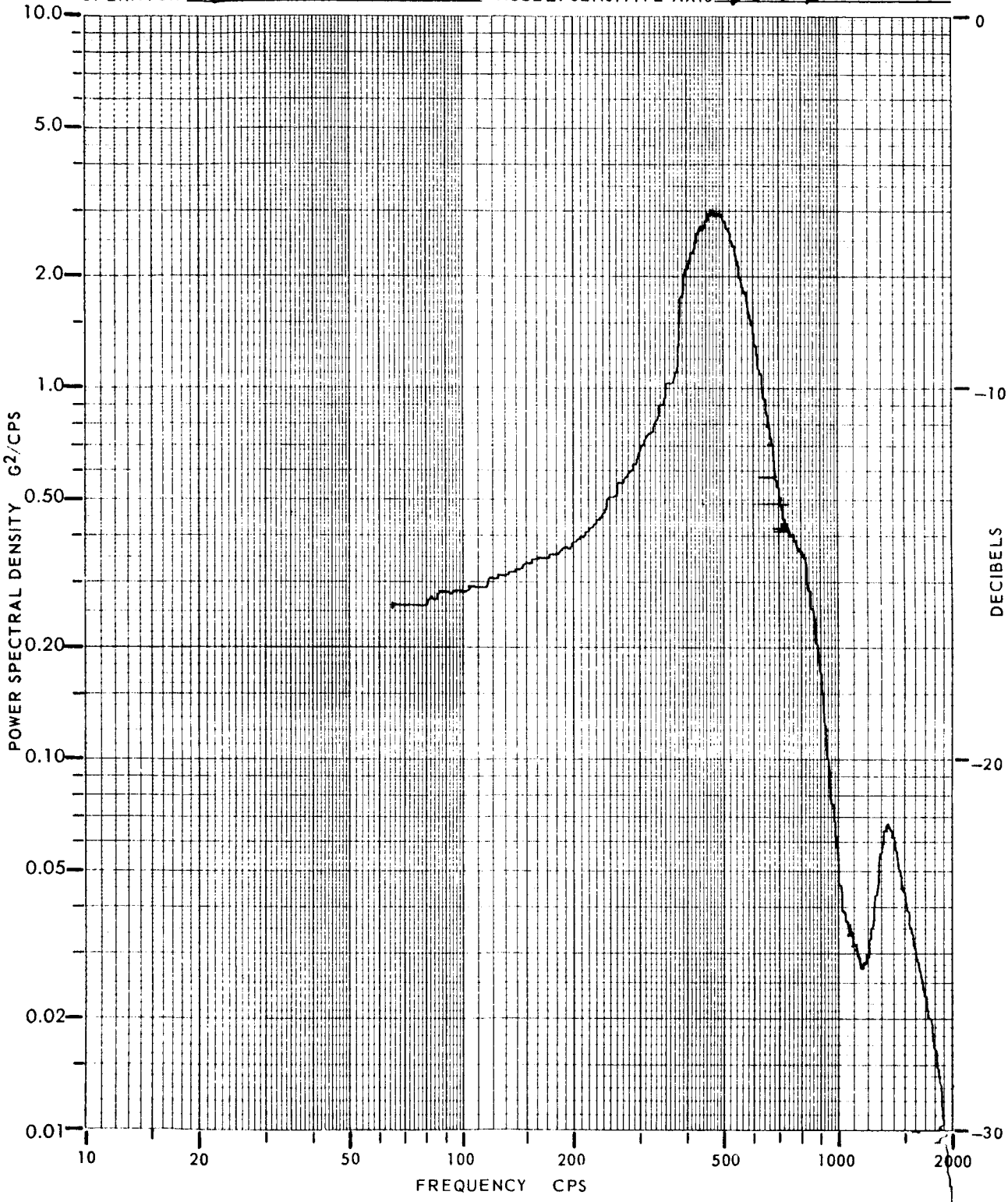

Figure IV-19

R-466-4

VIBRATION TEST DATA

PROJECT 1858
TEST ARTICLE 8 in Mech Model
RUN NO. 55
TEST DATE 1/6/66
OPERATOR Wier

INPUT AXIS Vert
INPUT LEVEL .2 G²/cps (20 RMS G)
ACCEL. LOCATION Module
ACCEL. SER. NO. 399
ACCEL. SENSITIVE AXIS Vert

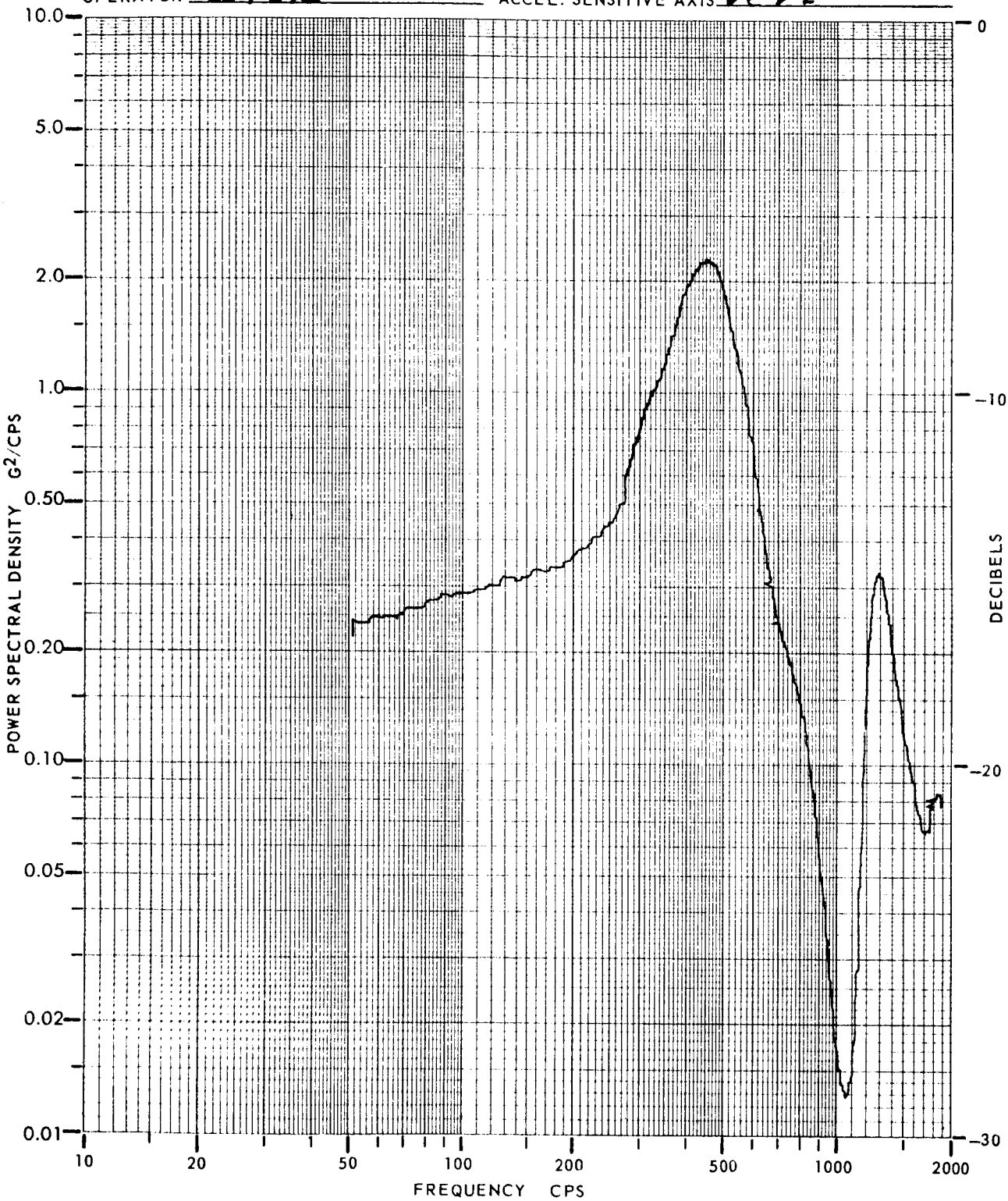

Figure IV-20

IV-4 TEST EQUIPMENT.

Item	Manufacturer	Model No.	Serial No.	Calibration Due Date
Shaker	Ling	A246	12	NA
Power Amplifier	Ling	PP20/24C	85	NA
Console and Associated Control and Monitoring Equipment	Ling	R-1004-C	87	NA

The originals of the x-y curves and VMS oscillograms are on file in the Environmental Laboratory.

PART 2

NIMBUS TME VIBRATION TESTS

Universal Report No. _____

Originator's Report No. 8741-1

Revision _____

Report Of Test On Nimbus Telemetry Electronics Mechanical Model Development Vibration Testing, RI # 513929

PERFORMED BY: S. Wier

Authorized By: M. Kann

(1858-33)

	Date	Signature	
Test Initiated	12/19/65		
Test Completed	12/22/65		
Report Written By	1/11/66	S. Wier	
Technician			
Test Engineer			
Supervisor			
Supervisor			
Approved Environmental Engr	1/20/66	[illegible]	
Government Representative (If Applicable)			
Final Release			

IV-1 PURPOSE.

To evaluate the Nimbus "B" telemetry electronics mechanical model when subjected to vibration environments required by the Nimbus qualification test specification.

IV-2 RESULTS.

The results of the vibration evaluation tests are illustrated by the attached x-y curves produced by accelerometers in and on the package housing.

IV-3 PROCEDURE.

IV-3.1 FIXTURING.

The vibration fixture used for these evaluation tests was T-6134. This fixture is a hollow cube, made of two inch aluminum plate. The open end of this cube has a cover made of one inch magnesium that is fastened to the cube with bolts. The total weight of the fixture and the adapter plate is 105 pounds.

IV-3.2 FIXTURE MOUNTING.

The fixture is mounted to a standard three inch thick magnesium adapter plate that is attached to the shaker armature head. This plate serves as an armature stiffening member. See figure IV-21 for a sketch of the setup.

IV-3.3 PACKAGE DESCRIPTION.

The packaging is a modular system with the modules mounted on printed circuit cards. These module-cards are then packaged in a housing that is designed to contain this module stack under mechanical pressure. The housing size is 6" x 4" x 6.5" (see figure IV-22).

a. Sine vibration sweeps at various vibration levels up to a maximum of 7.1 Grms from 30 cps to 2 KCS were made. VMS recordings and X-Y records were made of the output voltages of the module and the external accelerometers.

b. Random vibration was applied to the package in the form of a flat spectrum with a bandwidth of 20 cps to 2 KCS at a Power Spectral Density of 0.2 G^2/cps (approximately 20 Grms). The random response of the module accelerometer aligned with the axis of input vibration was analyzed and plotted on an X-Y recorder.

The originals of the X-Y curves and VMS oscillograms are on file in the Environmental Laboratory.

The evaluation was started in the longitudinal axis and proceeded as follows:

U. S. BLUE PRINT PAPER CO. CLEARPRINT 1000H

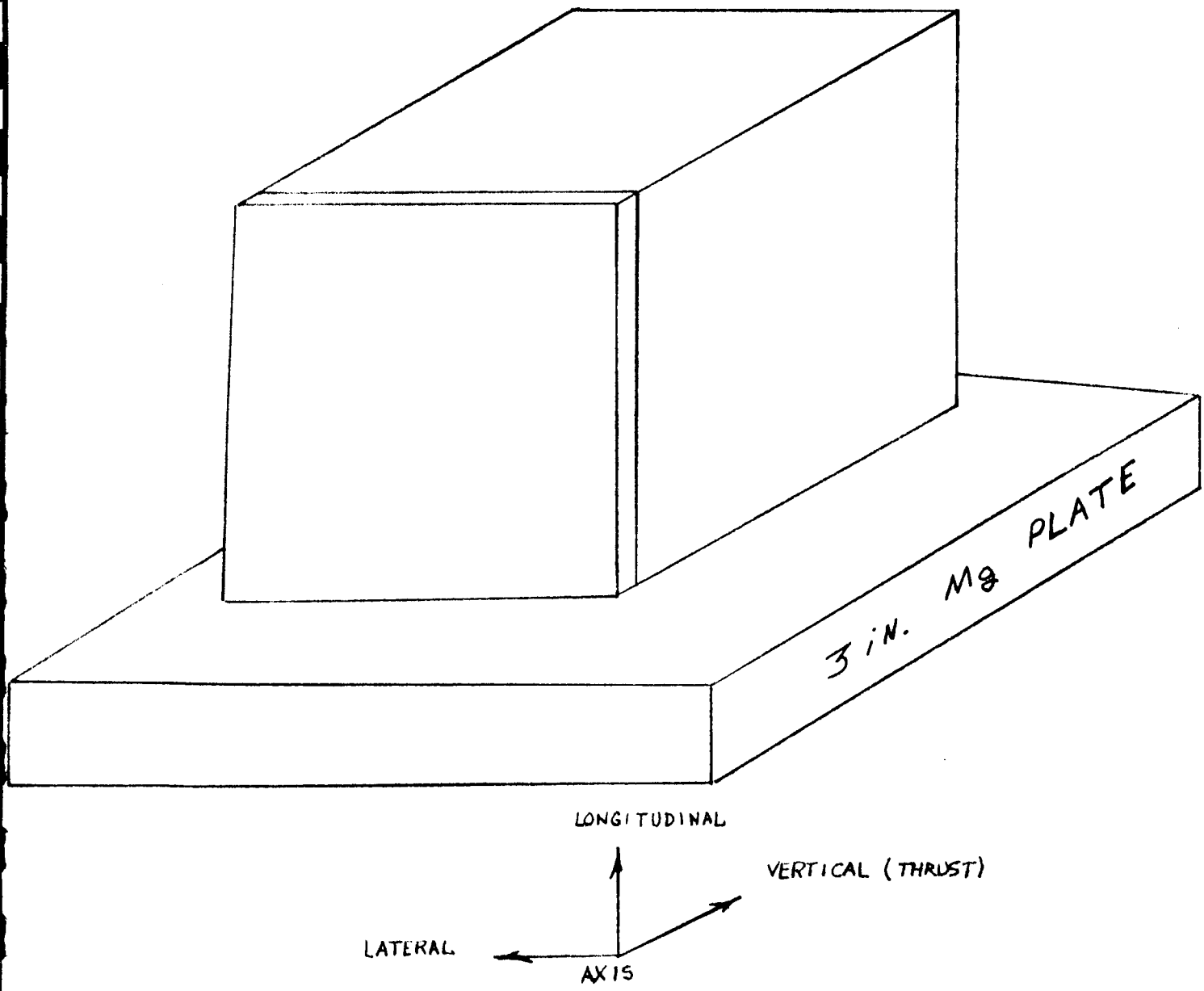

Figure IV-21

U. S. BLUE PRINT PAPER CO. CLEARPRINT 1000H

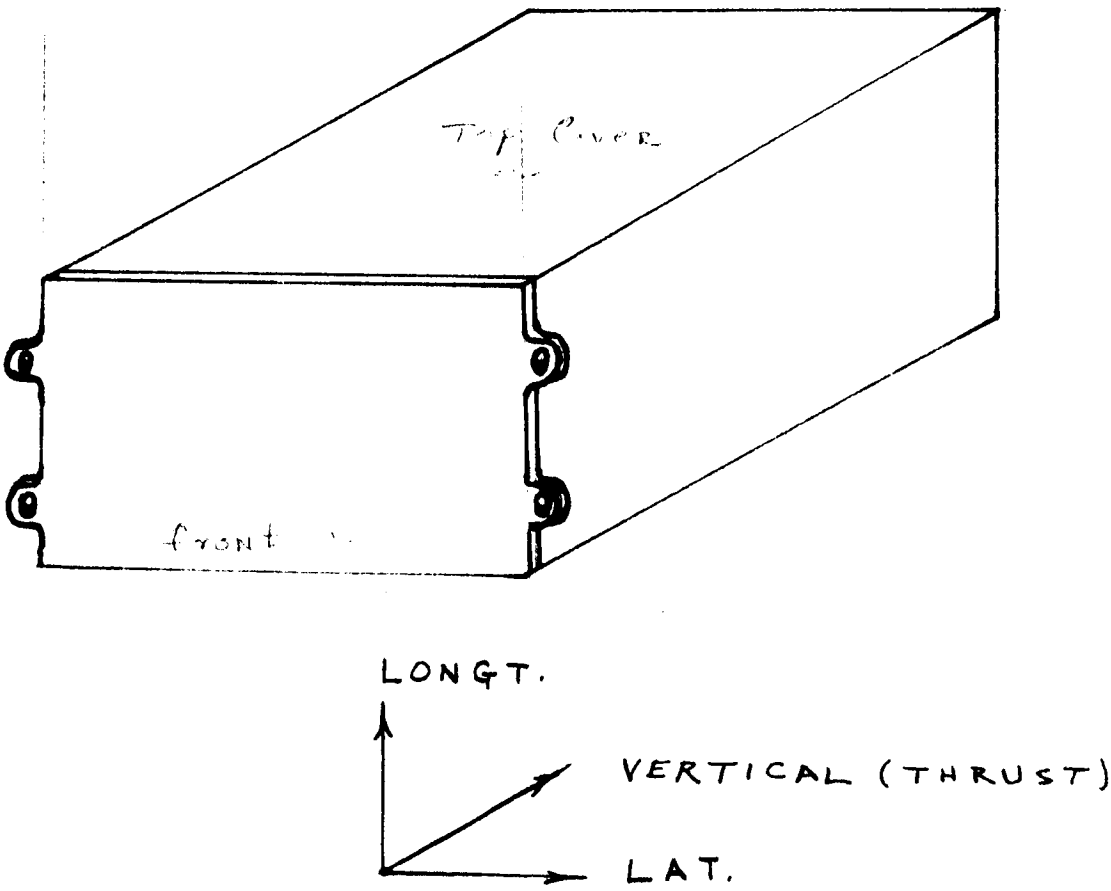

Figure IV-22

Longitudinal Axis Sine

Figures IV-23 and IV-24.

Lateral Axis Sine

Figures IV-25 and IV-26.

Vertical or Thrust Axis Sine

Figures IV-27 and IV-28.

Vertical Axis Random

Figure IV-29.

Longitudinal Axis Random

Figure IV-30.

The tests were discontinued at this point due to a "rattle" which developed in the package. The package was disassembled for inspection. This inspection revealed that the cards had worn in the areas of the loading feet. The cards were resized and epoxy shims were bonded to the loading feet to compensate for the undersize condition of the cards. When the package was reassembled, 1/4" strips of rubber were added between the card-stack and the housing top and bottom covers. The testing was resumed starting in the lateral axis.

Lateral Axis

Figures IV-31 and IV-32.

Longitudinal Axis

Figures IV-33 through IV-35.

Vertical Axis

Figure IV-36.

The tests were discontinued at this point due to a "rattle" which again developed in the package. The package was opened for an inspection and it was found that the corners of the cards had pounded into the tooling holes of the cards creating large tolerances allowing the cards to "rattle." This condition was repaired by adding fiber blocks on the cards to replace the worn corners of the cards and the tests were continued.

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS LONGT

TEST ARTICLE 4 IN. Model INPUT LEVEL 1, 2, 7.1 GRMS

RUN NO. 2 ACCEL. LOCATION Module, Left Rear from Top

TEST DATE 12/19/65 ACCEL. SER. NO. 413

OPERATOR WIER ACCEL. SENSITIVE AXIS LONGT.

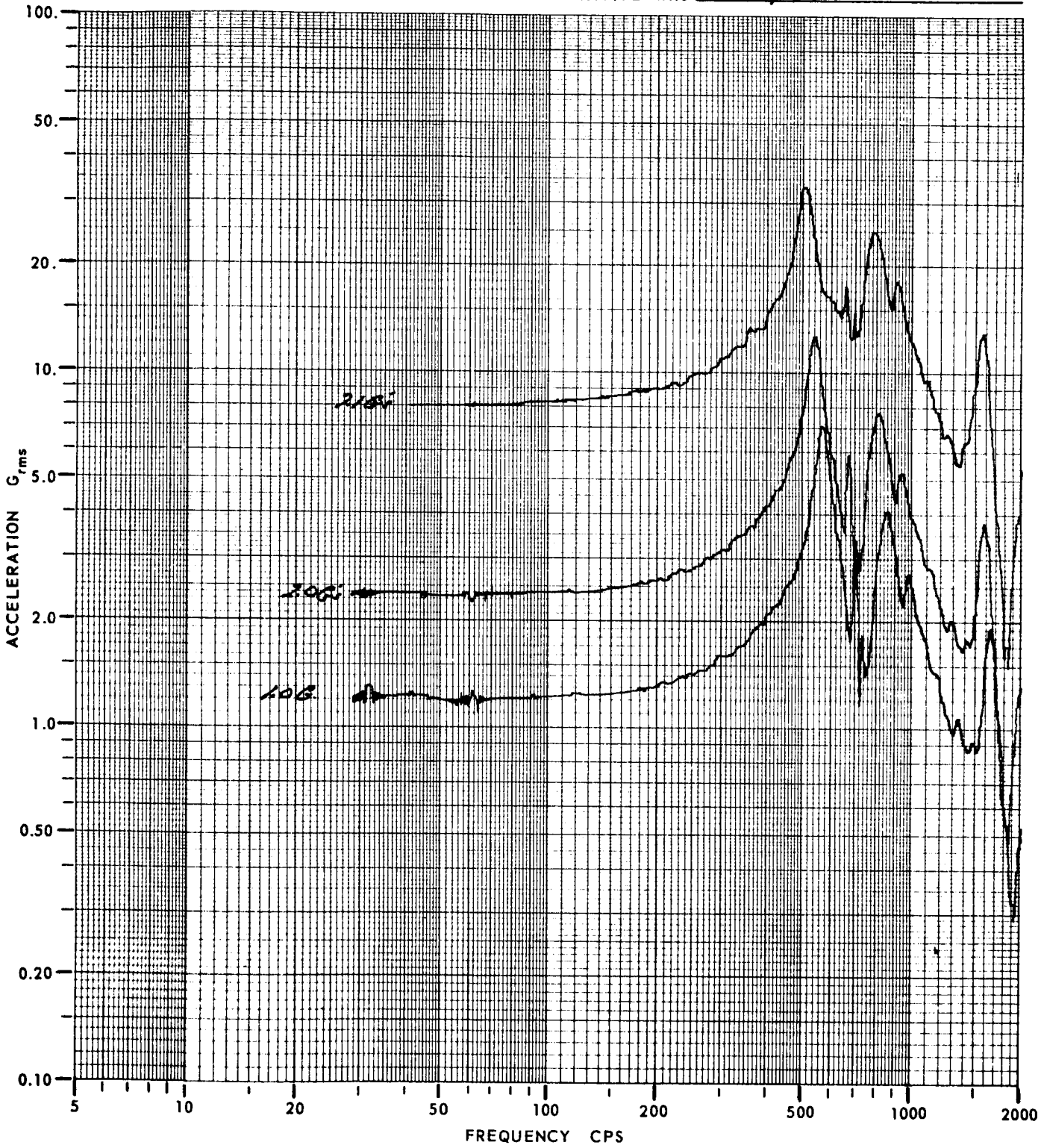

Figure IV-23

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS LONGT.

TEST ARTICLE Mock Model INPUT LEVEL 2 Grms

RUN NO. 3 ACCEL. LOCATION Top Cover

TEST DATE 12/19/65 ACCEL. SER. NO. 237

OPERATOR Wier ACCEL. SENSITIVE AXIS LONGT.

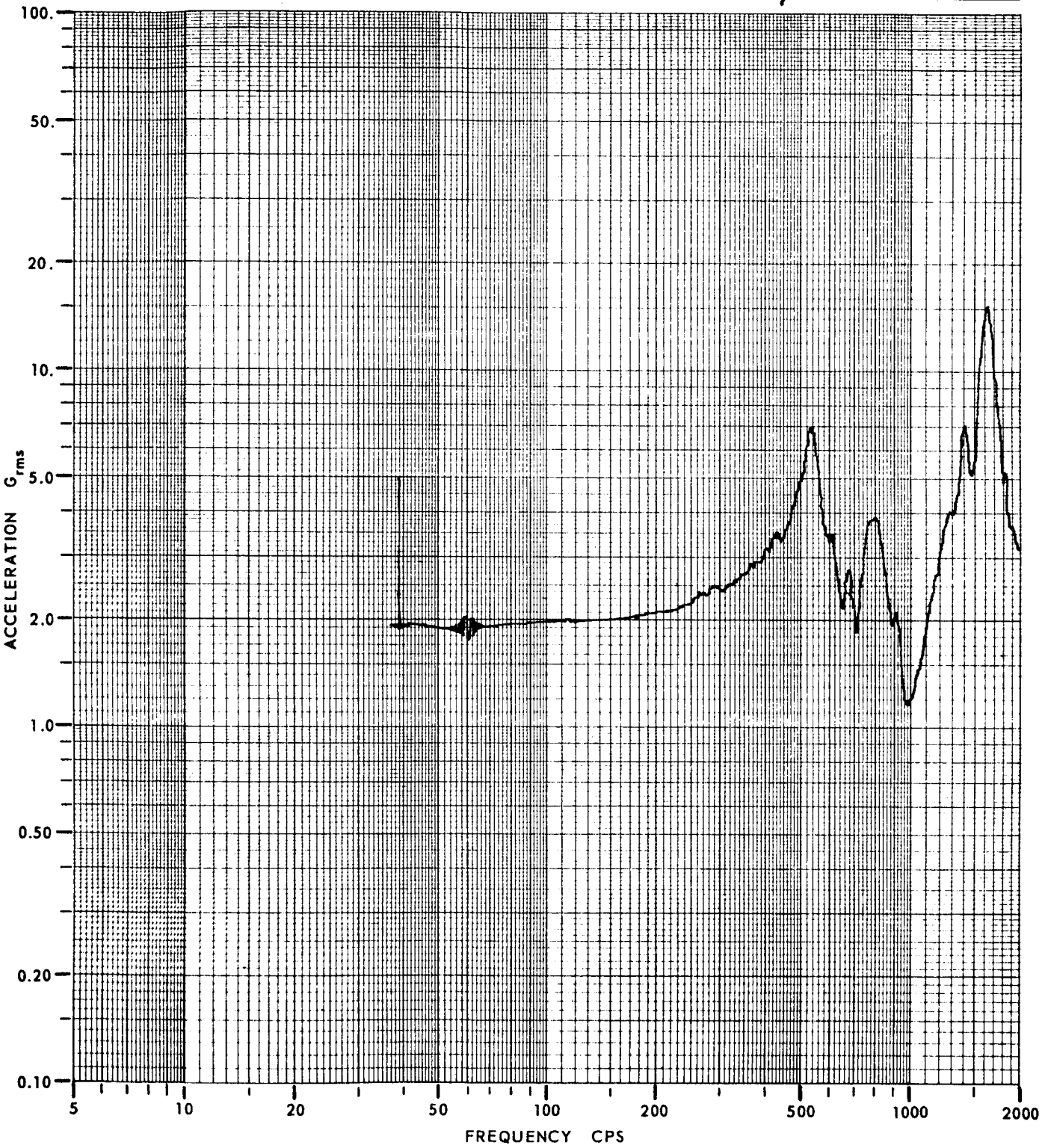

Figure IV-24

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS Lateral

TEST ARTICLE Nimbus Mech. Mod. INPUT LEVEL 1.0, 2.0 and 2.1 G's rms

RUN NO. 4, 4A and 4B ACCEL. LOCATION Module, Left rear Beam Typ.

TEST DATE 8 Dec 1965 ACCEL. SER. NO. 429

OPERATOR S. Wise ACCEL. SENSITIVE AXIS Lateral

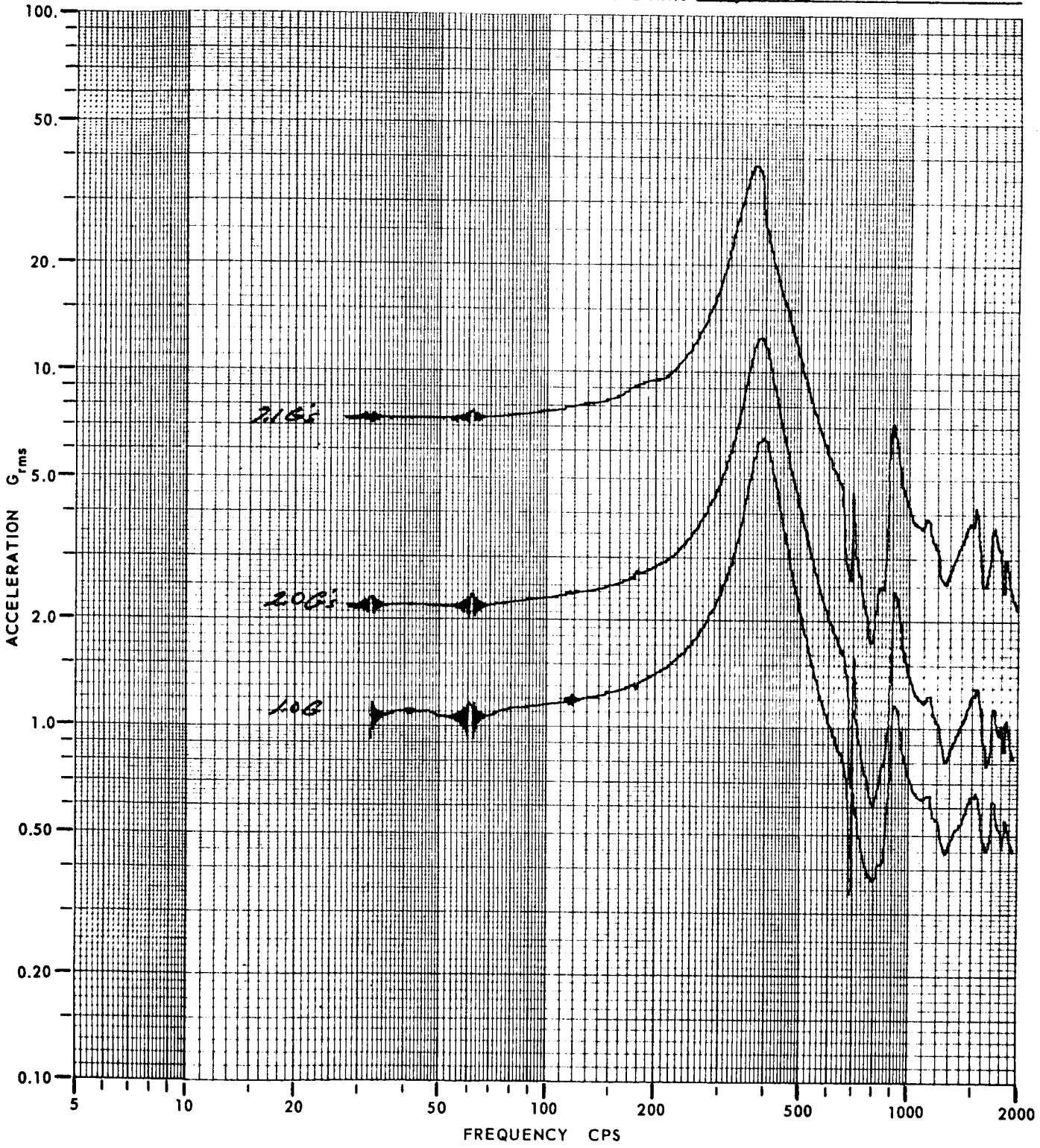

Figure IV-25

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS LAT

TEST ARTICLE Mech. Model INPUT LEVEL 2 G rms

RUN NO. 5 ACCEL. LOCATION TOP COVER

TEST DATE 12/19/65 ACCEL. SER. NO. 237

OPERATOR Wick ACCEL. SENSITIVE AXIS LAT LONGT (CT)

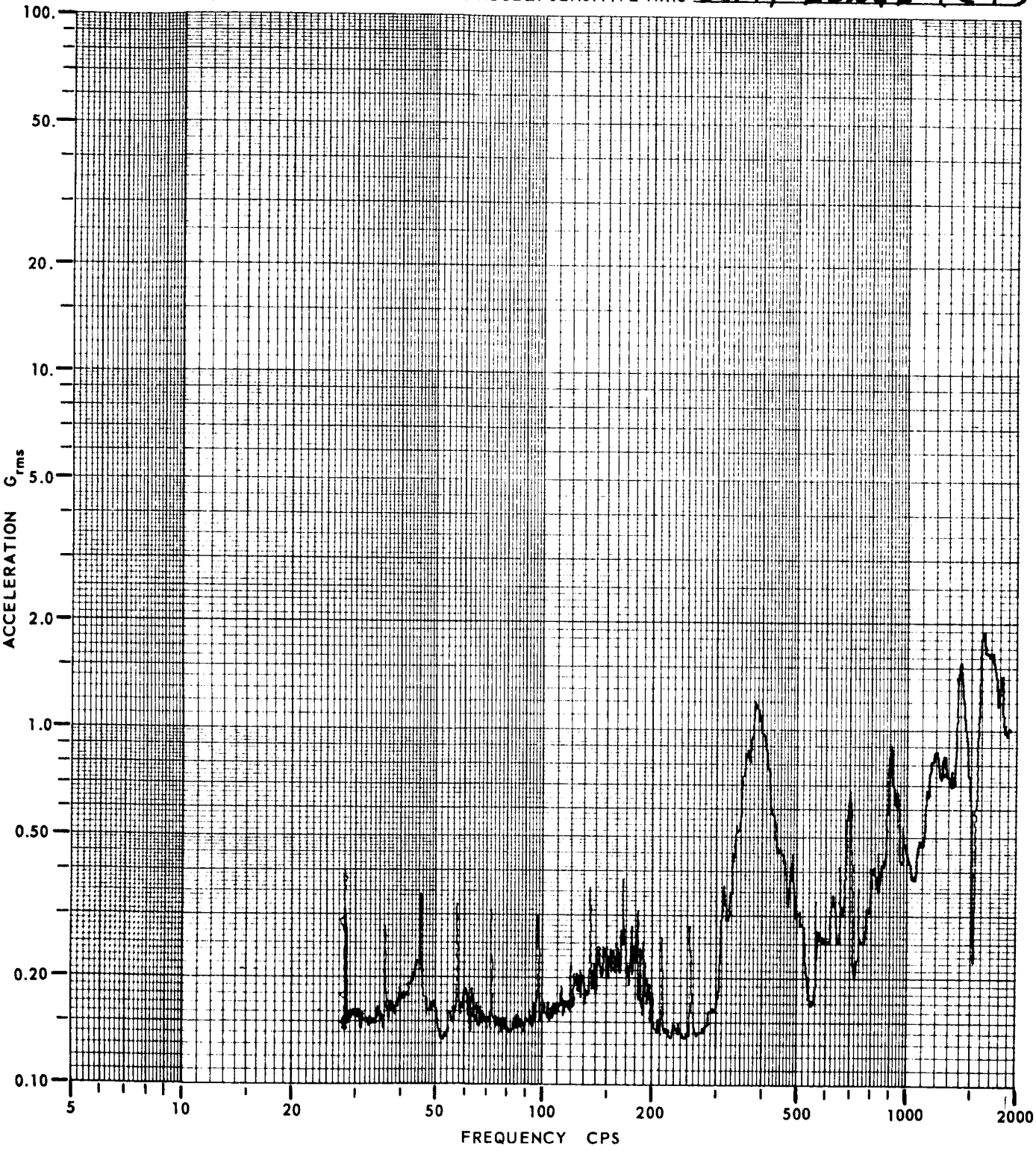

Figure IV-26

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS Thrust

TEST ARTICLE Mech Model INPUT LEVEL 1, 2, 7.1 Grms

RUN NO. 6 ACCEL. LOCATION Module

TEST DATE 12/10/65 ACCEL. SER. NO. 399

OPERATOR Wier ACCEL. SENSITIVE AXIS Thrust

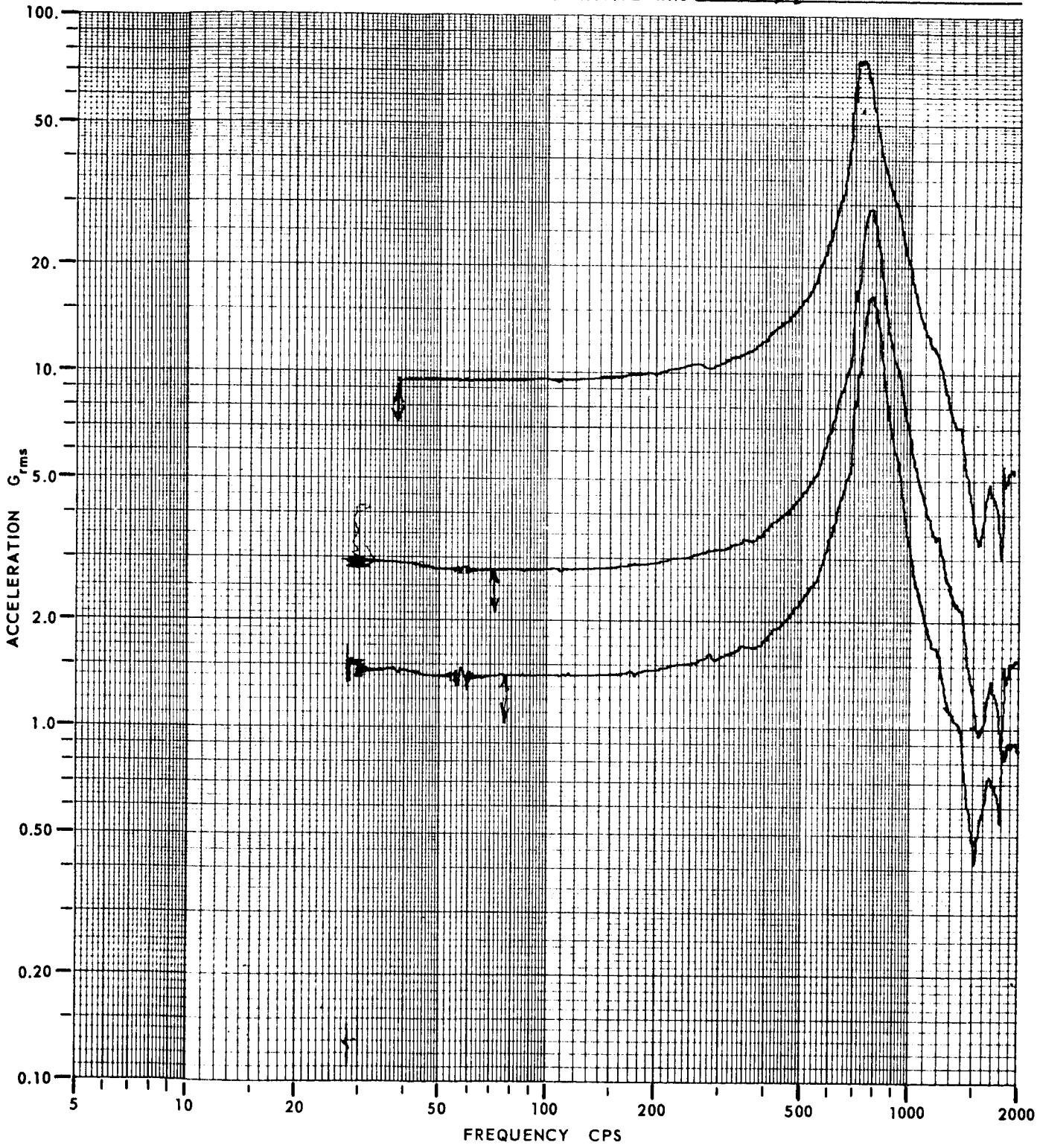

Figure IV-27

R-466

VIBRATION TEST DATA

PROJECT 1850 INPUT AXIS Thrust

TEST ARTICLE Mech. Model INPUT LEVEL 2

RUN NO. 7 ACCEL. LOCATION Top Cover

TEST DATE 12/19/65 ACCEL. SER. NO. 237

OPERATOR Wier ACCEL. SENSITIVE AXIS LONGT (CT)

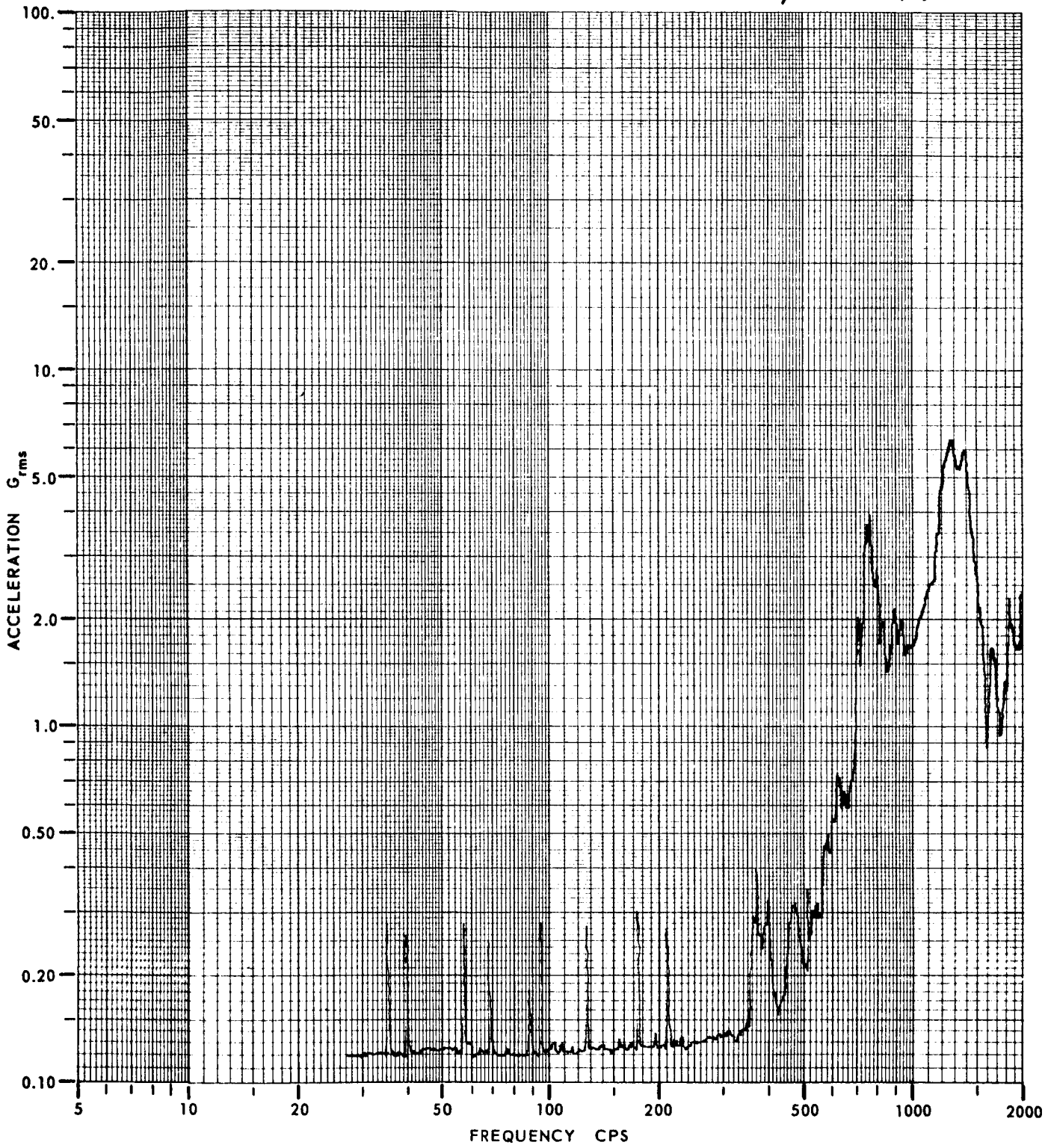

Figure IV-28

R-466-4

VIBRATION TEST DATA

PROJECT 1868 INPUT AXIS Thrust

TEST ARTICLE Model INPUT LEVEL .2 G^2/cps

RUN NO. 8 ACCEL. LOCATION Module

TEST DATE 12/14/65 ACCEL. SER. NO. 399

OPERATOR WICR ACCEL. SENSITIVE AXIS Thrust

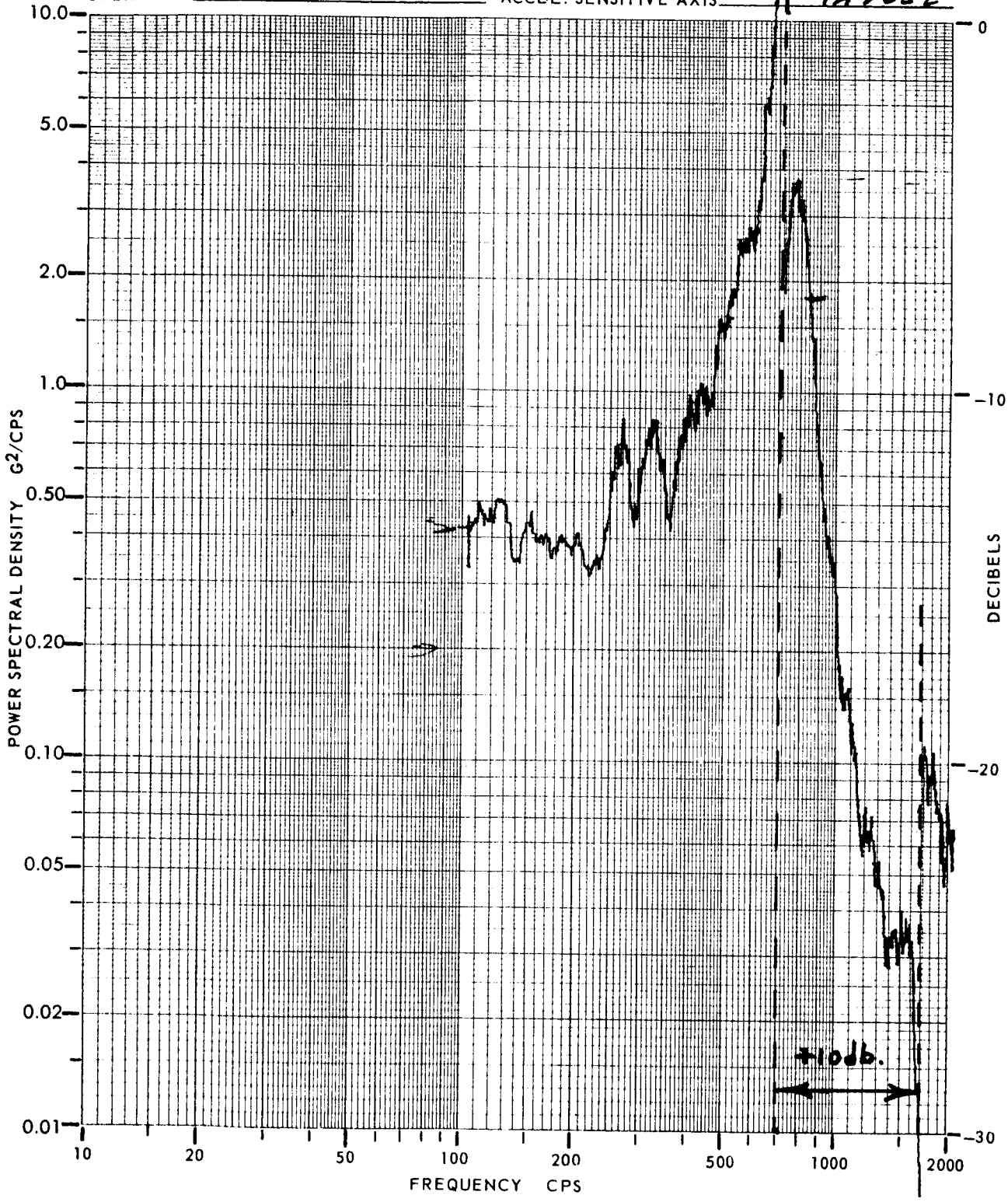

Figure IV-29

R-466-4

VIBRATION TEST DATA

PROJECT 1858
TEST ARTICLE Mech Model
RUN NO. 9
TEST DATE 12/19/65
OPERATOR wier

INPUT AXIS Longt
INPUT LEVEL .2 G^2/CPS (20RMSG)
ACCEL. LOCATION Module
ACCEL. SER. NO. 413
ACCEL. SENSITIVE AXIS Longt

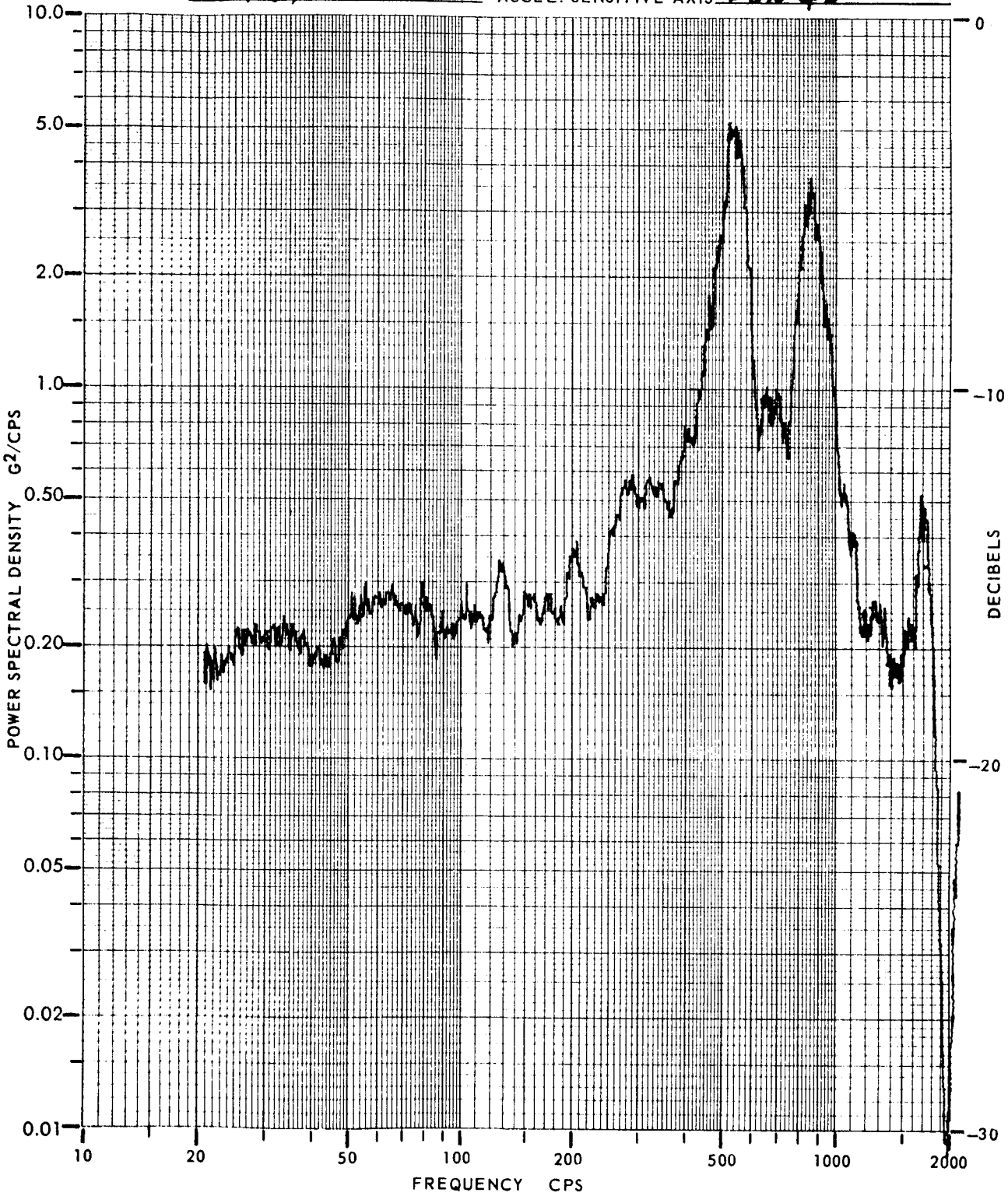

Figure IV-30

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS LAT

TEST ARTICLE Mech Model INPUT LEVEL 2, 7.1 G-rms

RUN NO. 10 ACCEL. LOCATION Module in Package

TEST DATE 12/20/65 ACCEL. SER. NO. 429

OPERATOR Wier ACCEL. SENSITIVE AXIS LAT

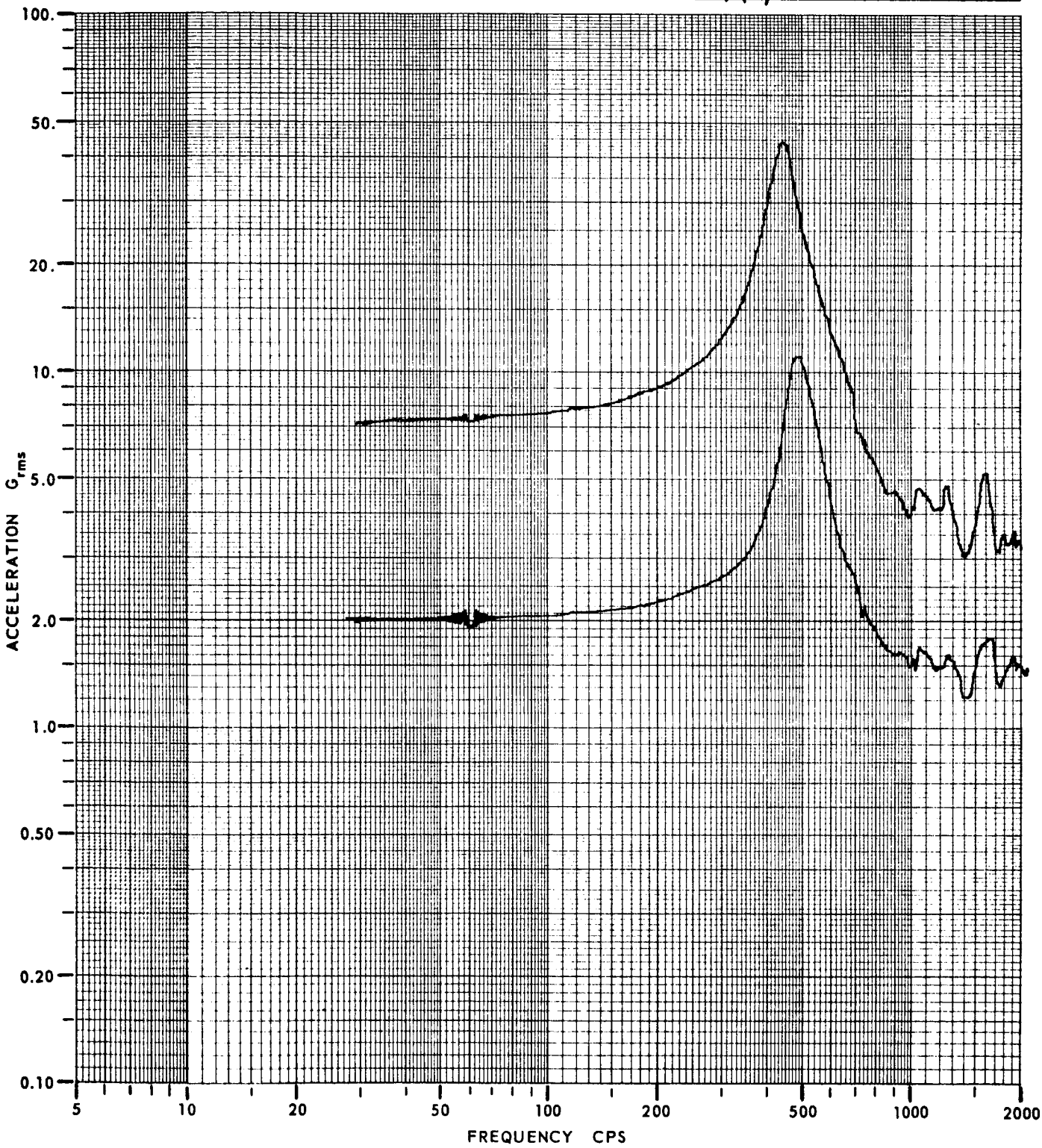

Figure IV-31

R-466-4

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS LAT.

TEST ARTICLE Mech Model INPUT LEVEL .2G²/CPS (20 GRMS)

RUN NO. 11 ACCEL. LOCATION Module

TEST DATE 12/20/65 ACCEL. SER. NO. 429

OPERATOR WIER ACCEL. SENSITIVE AXIS LAT.

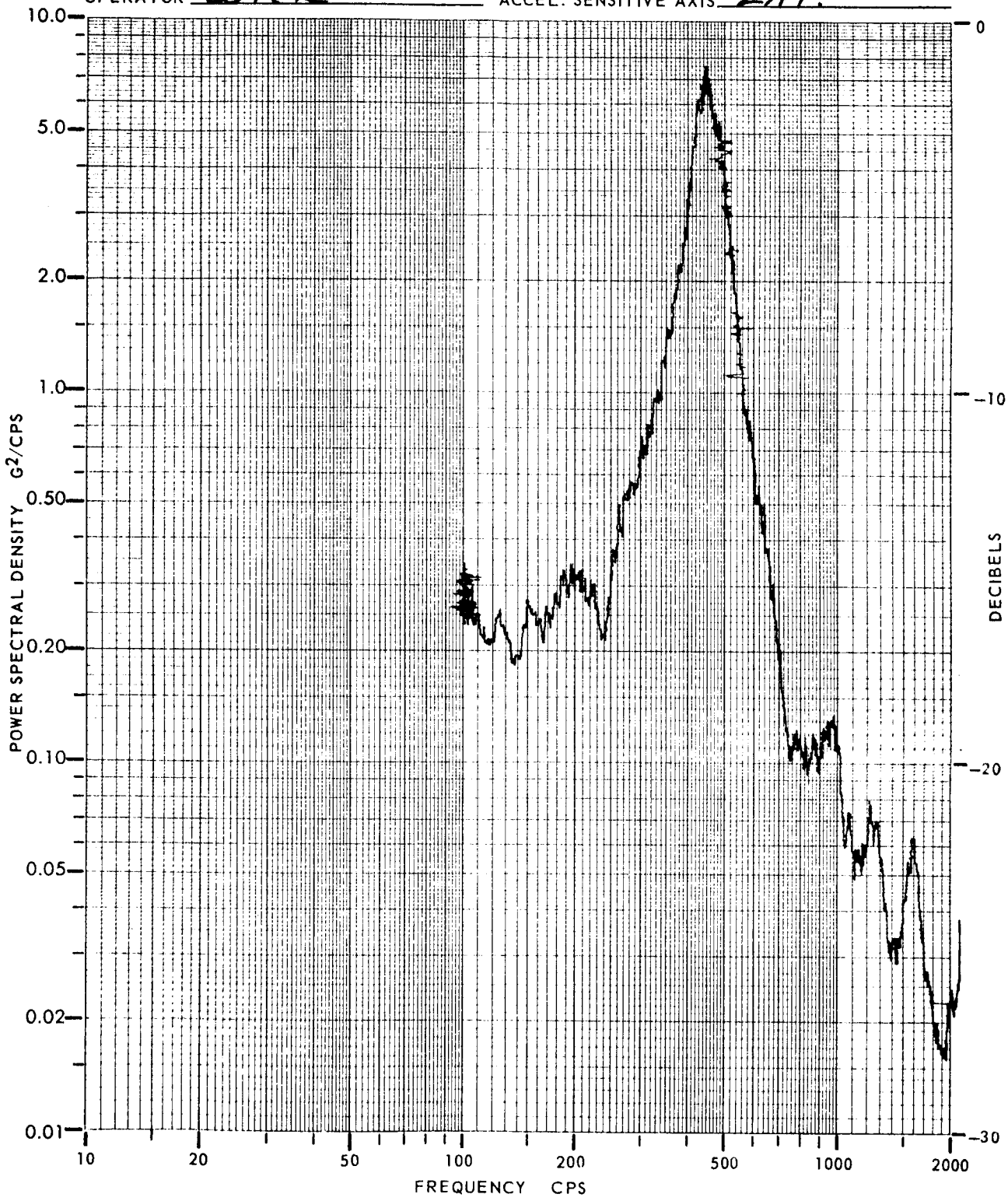

Figure IV-32

R-466

VIBRATION TEST DATA

PROJECT 1858
TEST ARTICLE Mock Model
RUN NO. 12
TEST DATE 12/20/65
OPERATOR Wick

INPUT AXIS LONGT
INPUT LEVEL 2 & 7.1 G rms
ACCEL. LOCATION IN Module
ACCEL. SER. NO. 413
ACCEL. SENSITIVE AXIS LONGT

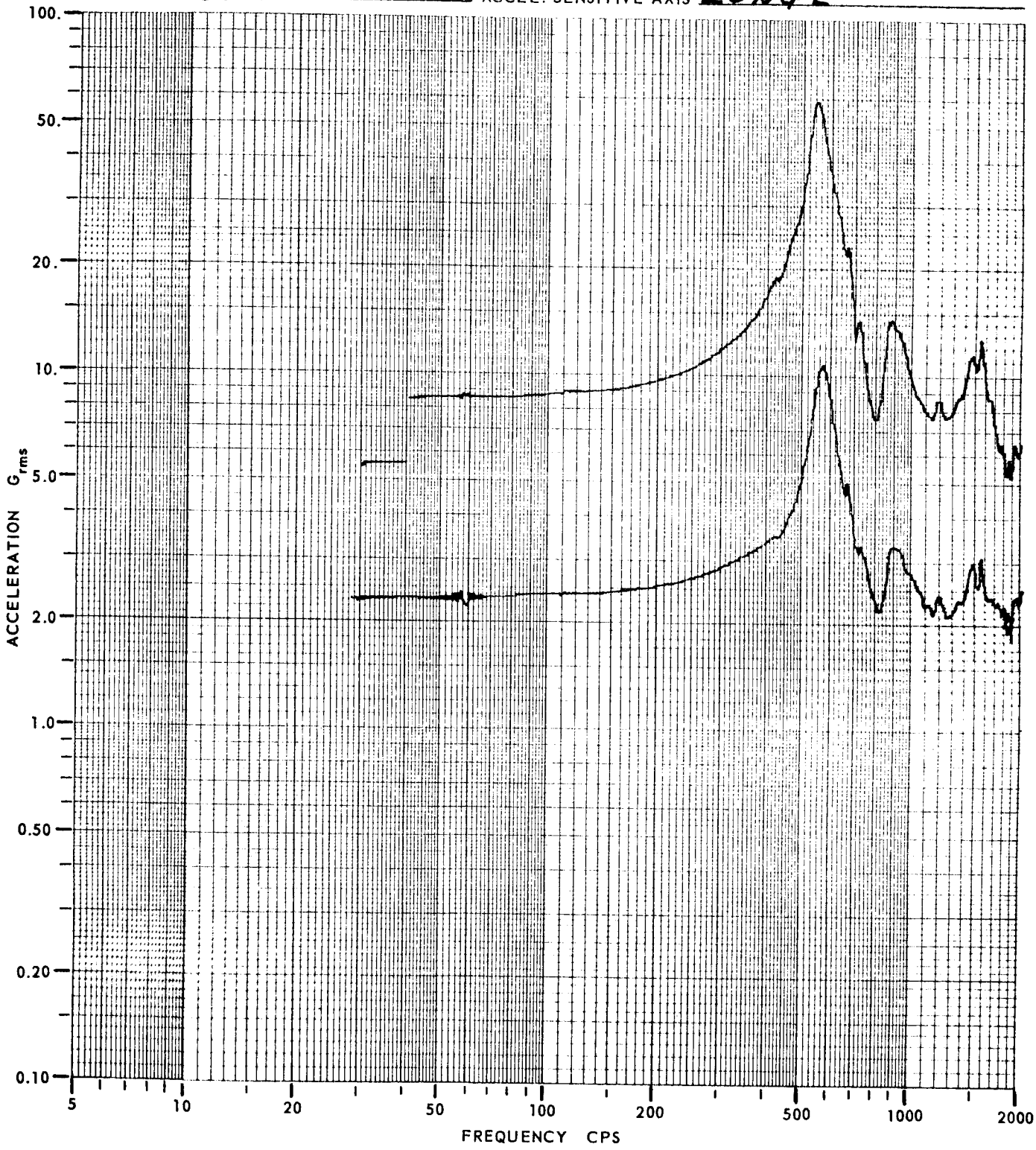

Figure IV-33

R-466

VIBRATION TEST DATA

PROJECT 1858
TEST ARTICLE Mech Model
RUN NO. 13
TEST DATE 12/20/65
OPERATOR Wiper

INPUT AXIS LONGT.
INPUT LEVEL 2 GRMS
ACCEL. LOCATION Top Cover
ACCEL. SER. NO. 237
ACCEL. SENSITIVE AXIS LONGT.

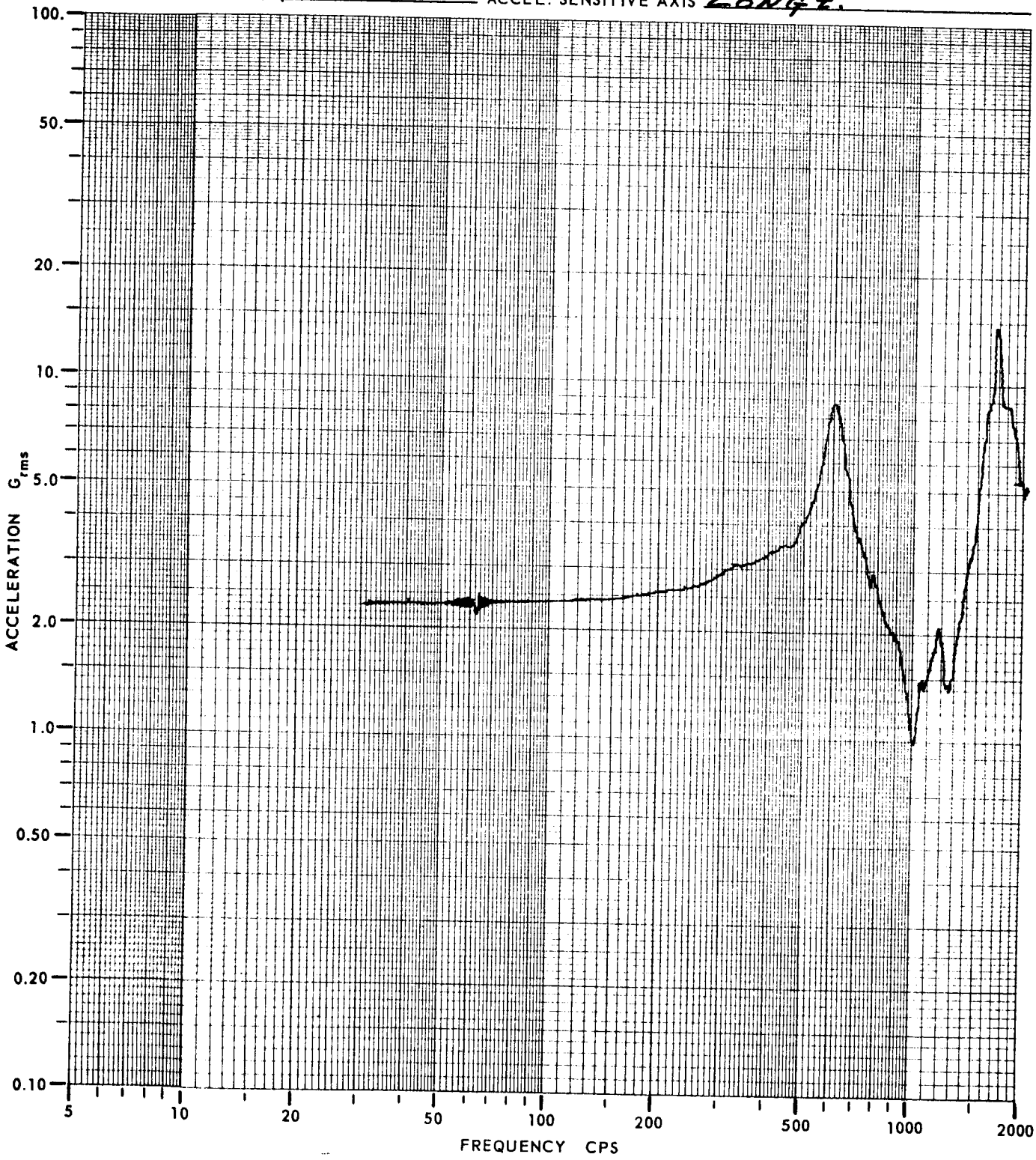

Figure IV-34

R-466-4

VIBRATION TEST DATA

PROJECT 1858
TEST ARTICLE Mech Model
RUN NO. 14
TEST DATE 12/20/65
OPERATOR WIER

INPUT AXIS LONGt
INPUT LEVEL .2G²/CPS (20G rms)
ACCEL. LOCATION Module
ACCEL. SER. NO. 413
ACCEL. SENSITIVE AXIS LONGt.

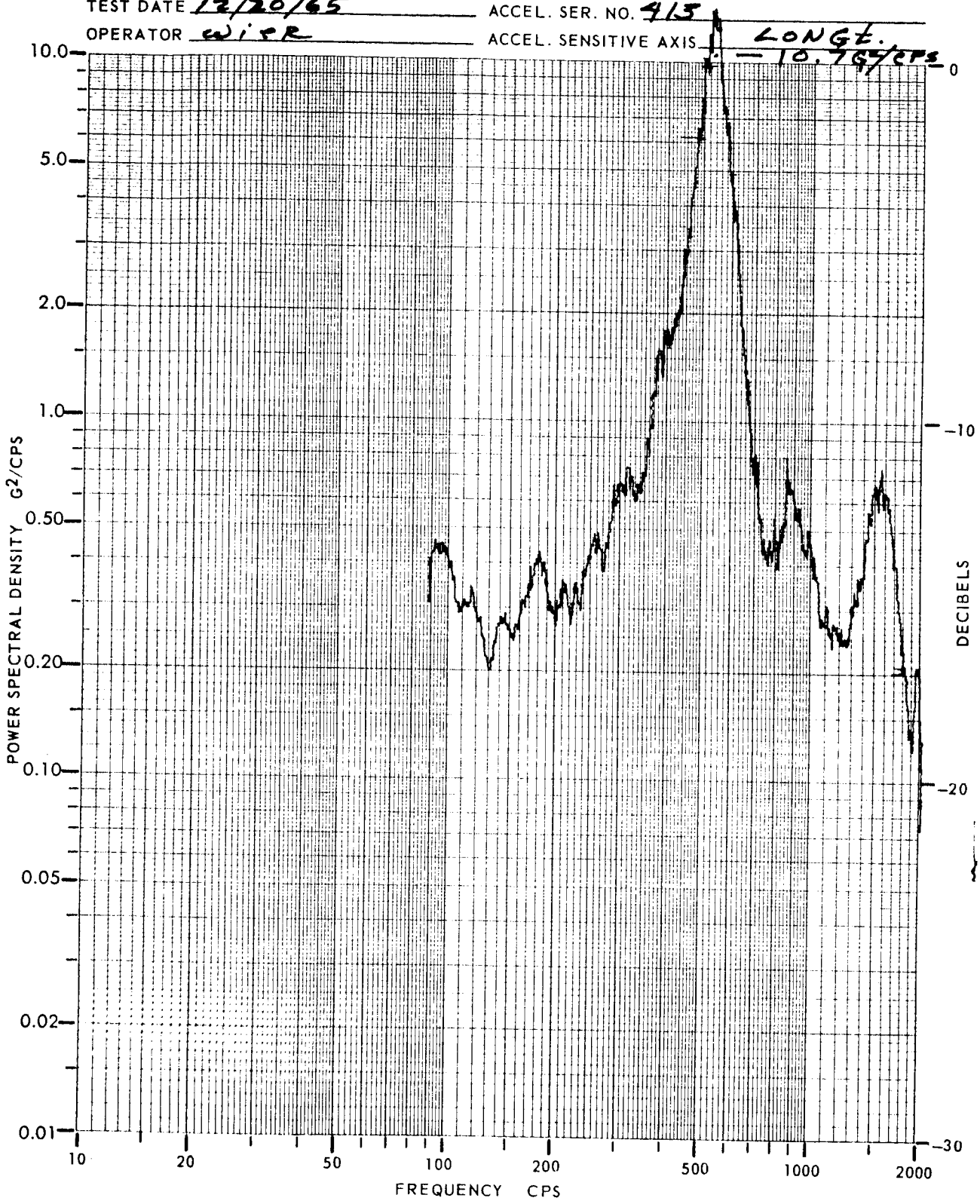

Figure IV-35

R-466

VIBRATION TEST DATA

PROJECT 1858 INPUT AXIS Thrust

TEST ARTICLE Mech Model INPUT LEVEL 2 & 7.1 Grms

RUN NO. 15 ACCEL. LOCATION Module

TEST DATE 12/20/65 ACCEL. SER. NO. 399

OPERATOR CWOR ACCEL. SENSITIVE AXIS Thrust

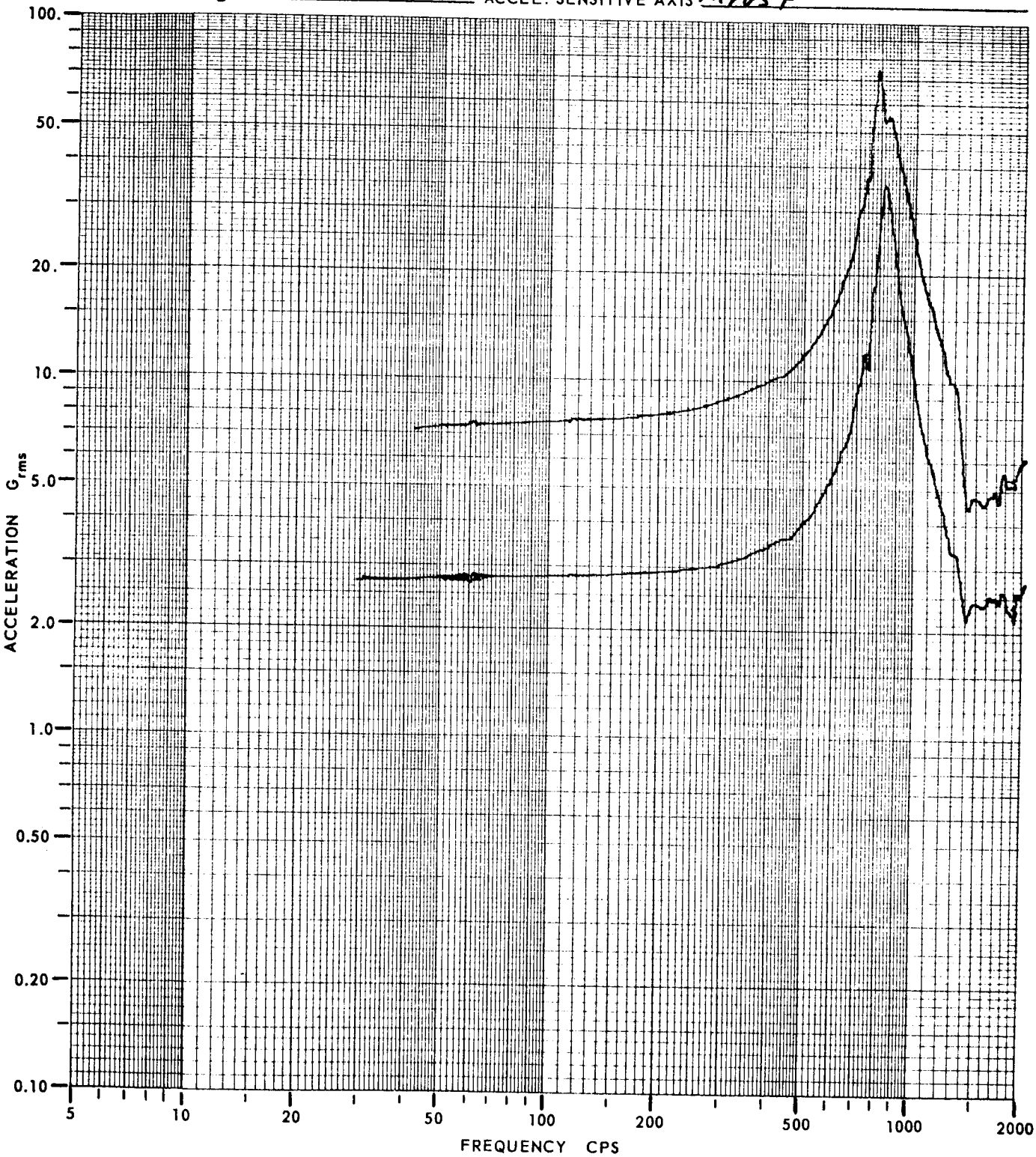

Figure IV-36

Vertical Axis

Figures IV-37 through IV-39.

Longitudinal Axis

Figure IV-40.

(This figure indicates the frequency and "rattle" threshold of 3.2 Grms input.)

The tests were discontinued at this time because of the condition of the boards and acceptable data had been accumulated in each axis.

IV-4 TEST EQUIPMENT.

Item	Manufacturer	Model No.	Serial No.	Calibration Due Date
Shaker	Ling	A246	12	NA
Power Amplifier	Ling	PP20/24C	85	NA
Console and Associated Control and Monitoring Equipment	Ling	R-1004-C	87	NA

R-466

VIBRATION TEST DATA

PROJECT 1858

TEST ARTICLE Mech Model

RUN NO. 18

TEST DATE 12/22/65

OPERATOR WIER

INPUT AXIS Thrust

INPUT LEVEL 2 & 7.1 Grms

ACCEL. LOCATION Module

ACCEL. SER. NO. 399

ACCEL. SENSITIVE AXIS Thrust

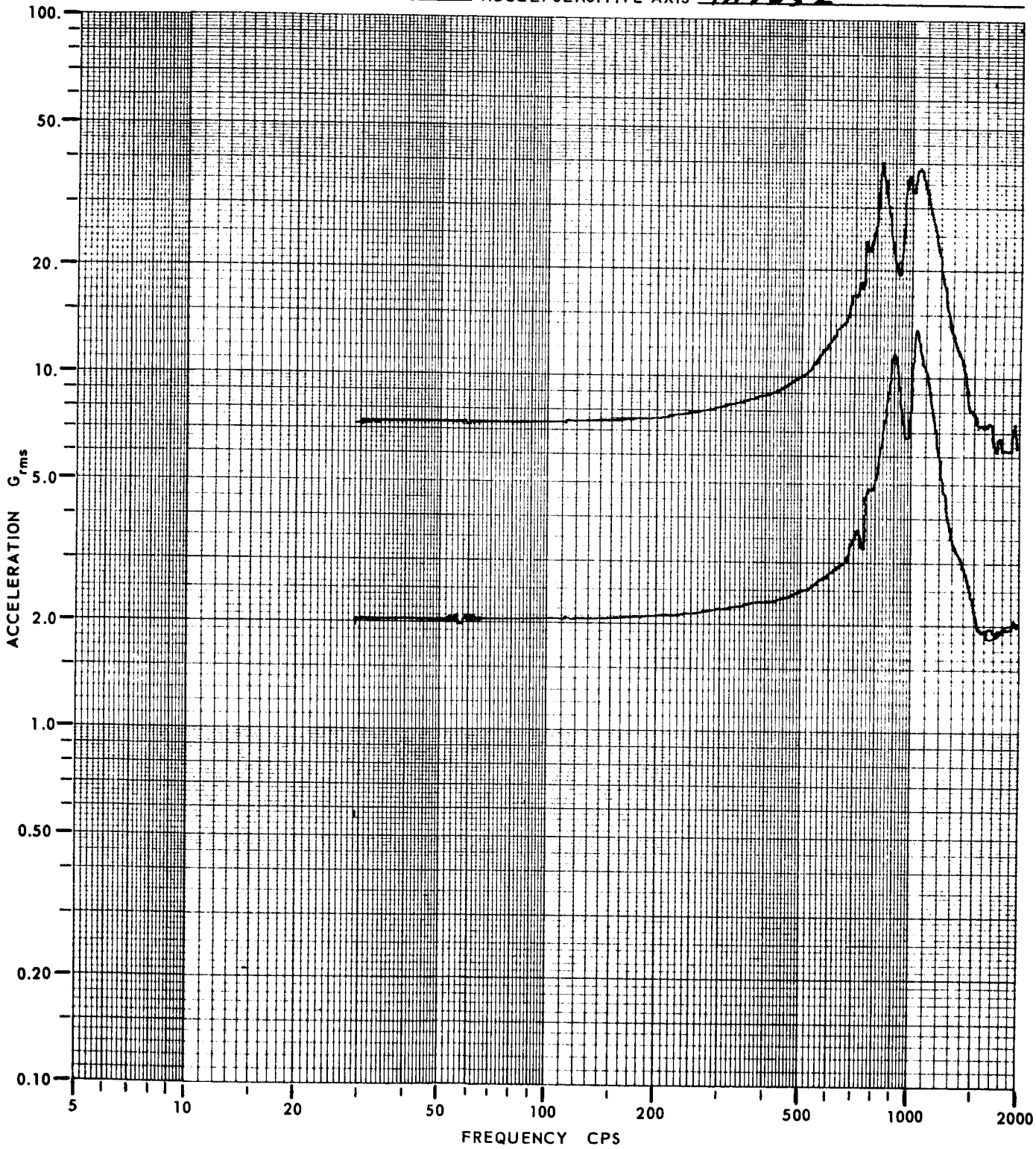

Figure IV-37

R-466

VIBRATION TEST DATA

PROJECT 1858
TEST ARTICLE Mech Model
RUN NO. 19
TEST DATE 12/22/65
OPERATOR Wier

INPUT AXIS Thrust
INPUT LEVEL 2 Grms
ACCEL. LOCATION Front Panel
ACCEL. SER. NO. 237
ACCEL. SENSITIVE AXIS Thrust

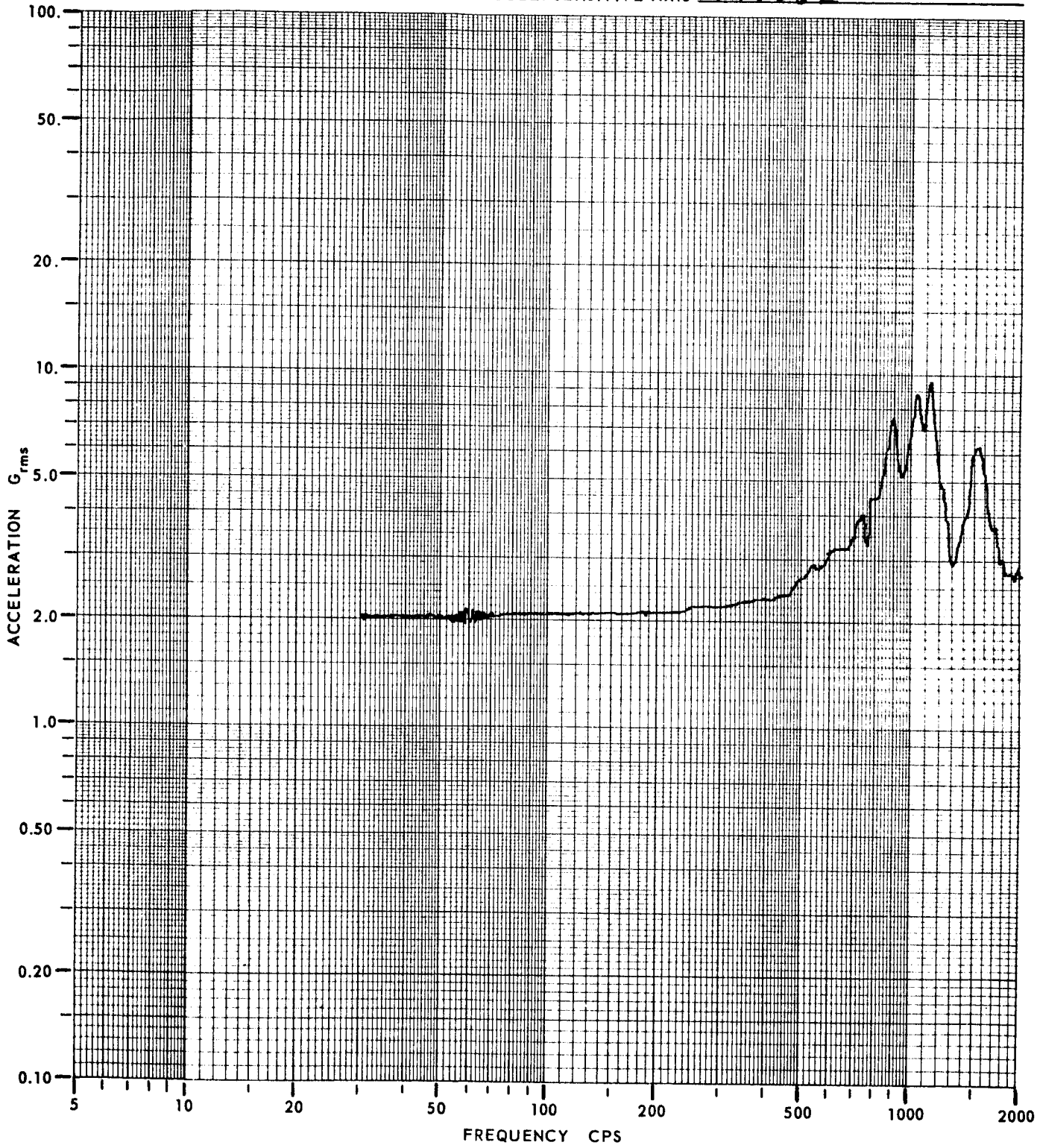

Figure IV-38

R-466-4

VIBRATION TEST DATA

PROJECT 1858
TEST ARTICLE Mech Model
RUN NO. 20
TEST DATE 12/22/65
OPERATOR WIER

INPUT AXIS Thrust
INPUT LEVEL .2 G²/CPS (20G rms)
ACCEL. LOCATION Module
ACCEL. SER. NO. 399
ACCEL. SENSITIVE AXIS Thrust

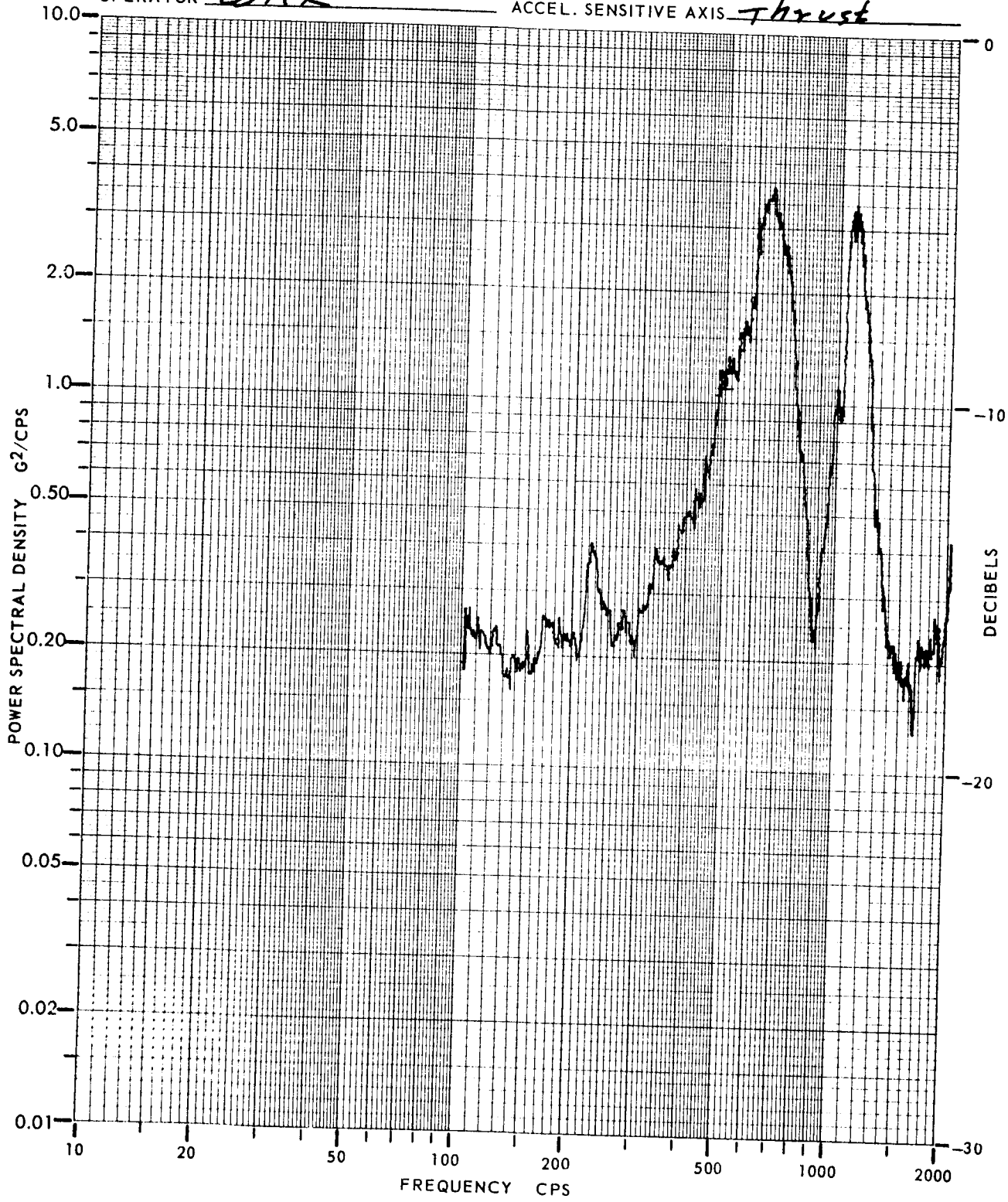

Figure IV-39

R-466

VIBRATION TEST DATA

PROJECT 1858
TEST ARTICLE Mech Model
RUN NO. 21
TEST DATE 12/22/65
OPERATOR WiYR

INPUT AXIS LONGt
INPUT LEVEL Z @ 7.1 G rms
ACCEL. LOCATION Module
ACCEL. SER. NO. 413
ACCEL. SENSITIVE AXIS LONGt

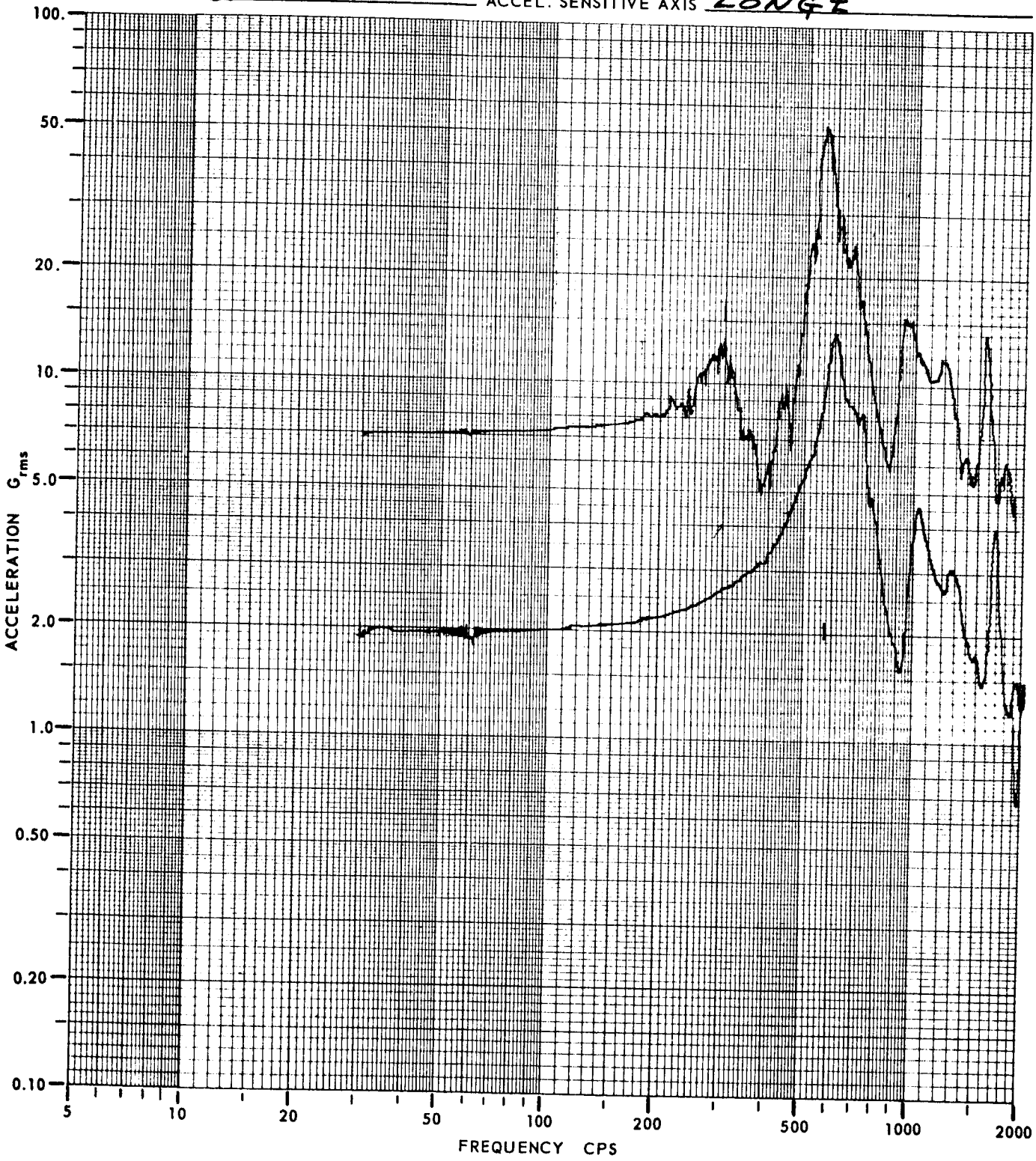

Figure IV-40

APPENDIX V

ENCODING ACCURACY

APPENDIX V

ENCODING ACCURACY

TABLE OF CONTENTS

Paragraph	Title	Page
V-1	General	V-1
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V-5	Feedback Current	V-3
V-6	Aperture Time	V-3
V-7	Capacity Charge Transfer	V-4
V-8	Input Noise	V-4

V-1 GENERAL.

The encoding accuracy of the Nimbus B PCM unit (figure V-1) is primarily dependent on the coder quantizing error, coder linearity, coder input impedance versus transducer source impedance, and feedback leakage current from the multiplexer overvoltage clamp circuit. Other factors that contribute to error but are deemed negligible for the PCM unit are aperture time error and capacity charge transfer error. Noise error could become a large percentage of the total error, but proper signal conditioning and wiring can reduce the total noise to a negligible amount.

V-2 CODER QUANTIZING ERROR.

Coder quantizing error is ± one-half of the least significant bit weight used. For a seven bit coder with 128 total possible binary coded levels, each level represents 0.78 percent of full scale. Thus, the total quantizing error for a 7-bit binary coder is ±0.39 percent.

V-3 LINEARITY.

The encoding process occurs with a design limit of less than ±0.5 percent nonlinearity, with probable nonlinearity being less than ±0.1 percent because of the ramp coder technique used. The low end switching point can be measured at approximately -50 millivolts, the high end switching point can be measured at approximately -6.375 volts, and a straight line can be drawn between these two voltages. All other points should occur within ±0.5 percent, or ±32 millivolts, of this line. In all probability, the points will occur within ±0.1 percent of this line or ±6.4 millivolts. This type of measurement should be made with 0-ohm source impedance to reduce noise to a minimum in order to stabilize the output binary code switching points. Linearity must be measured using the encoder switching points because they are approximately 2 millivolts wide, while the bit weight of a 7-bit coder is 50 millivolts. Thus, the switching points can be in error ±1 millivolt, while the normal output code can be in error ±25 millivolts with no switching taking place.

In summary, total encoding accuracy should be within ±0.78 percent of full scale (±50 millivolts) for the 7-bit code with a maximum source impedance of 3.3K ohms. An increase in source impedance degrades the accuracy due to increased noise and offset voltages. The 10-bit coder resolution of 1024 levels gives an overall resolution of approximately ±0.1 percent of full scale. This is actually 6.256 millivolts per bit or ±3.128 millivolts of overall resolution. Since the noise is a minimum of approximately 3 millivolts, the overall maximum accuracy using the 10-bit coder is ±0.1 percent. If greater noise is present, 8-bit or 9-bit accuracy should be used.

V-4 INPUT TRANSDUCER SOURCE IMPEDANCE VERSUS PCM UNIT INPUT IMPEDANCE.

The input source impedance should be 3.3K ohms (maximum) for an error of ±0.78 percent. Higher input impedances up to 10K ohms can reduce this accuracy to ±1 percent. Actual accuracy is determined by the voltage divider effect of source impedance and input impedance. This input impedance is 1 megohm (minimum) and is greater than 10 megohms in most cases.

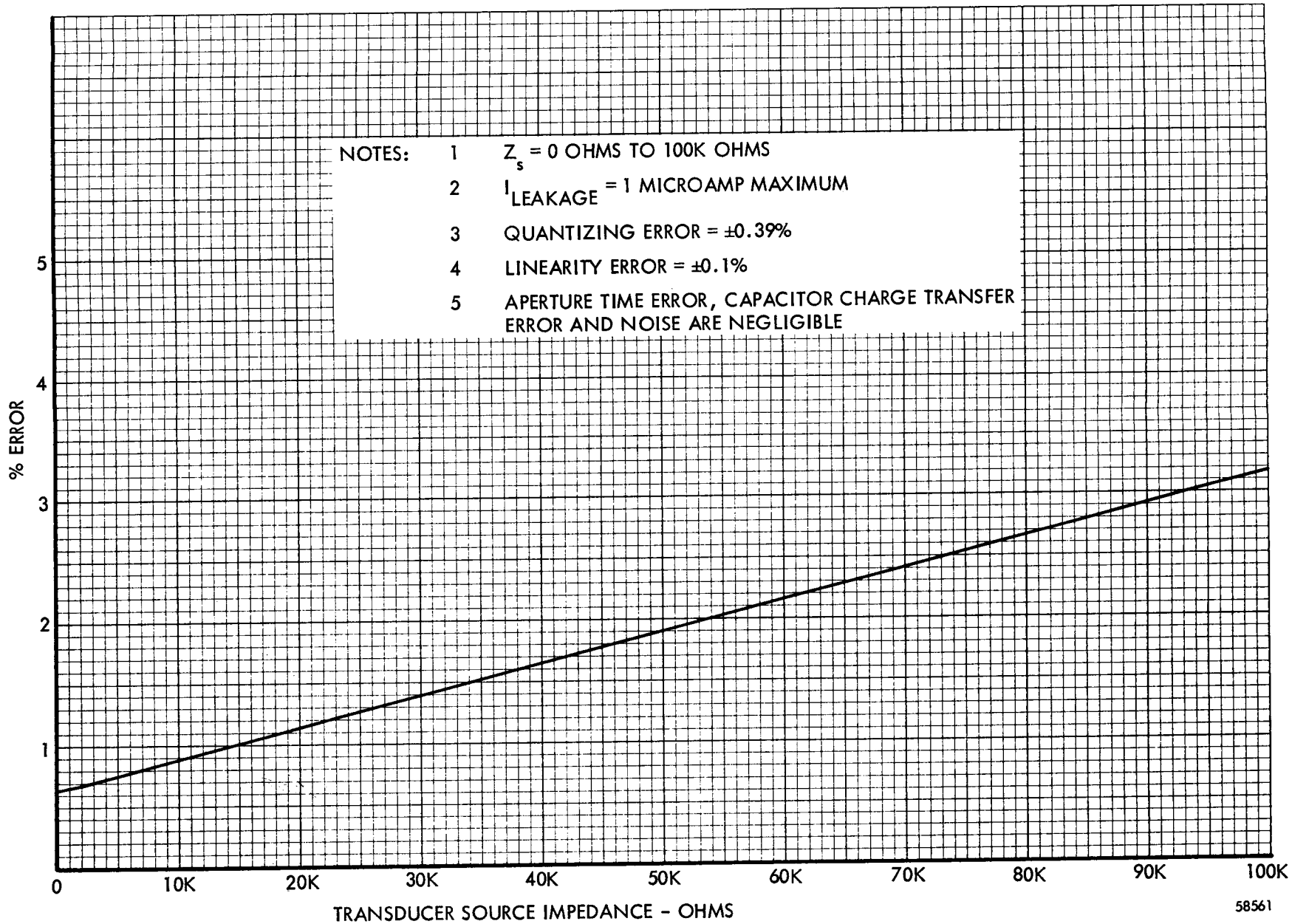


Figure V-1. Nimbus B PCM Unit Encoding Accuracy

However, in the case of 1 megohm (minimum), the 3.3K ohm source impedance becomes a possible error of 0.33 percent, but this error drops to 0.33 percent if the higher value of 10 megohms is realized in every system. The possible error of 0.33 percent of full scale represents a voltage error offset of 21.12 millivolts, which is solely due to the source impedance-input impedance voltage divider action. This offset drops to approximately 2.1 millivolts if the input impedance can be maintained at 10 megohms (minimum).

If the input source impedance goes up to 10K ohms and the input impedance is as low as 1 megohm, a possible error offset of 1 percent results.

V-5 FEEDBACK CURRENT.

The feedback current from the PCM unit to the transducer is a leakage current and can cause a constant signal offset depending on the source impedance. For example, the specified maximum feedback current during sample time is 1 microampere, which drops 3.3 millivolts across the 3.3K ohm input source impedance. If the source impedance is increased to 10K ohms, voltage offset increases to 10 millivolts.

In the Nimbus B PCM, the majority of leakage current is fed back through channel gates from the input channel gate overvoltage protection clamping circuit diodes. These diodes are biased at approximately -20 volts and prevent any fault voltages in excess of -20.5 volts from being applied to the multiplexer output sequencer gates. These diodes protect against multiple gate failures or total failure if a channel gate faults up to -24 volts. (These circuits can protect the input channel gate sequencers up to approximately -35 volts fault at the input.) The diodes are necessary because: if an input channel gate shorts out due to an overvoltage, it will apply the overvoltage to the output sequencer; if the output sequencer gate fails by shorting out, the entire multiplexer is useless. Thus, diode clamps provide fail-safe redundancy during the presence of input fault overvoltages.

The diodes leak a maximum of 100 nanoamperes with 0 volt input (maximum voltage across the clamping diode) at +55°C. Thus, the offset maximum caused by these protection diodes is 0.33 millivolts as seen at the input terminal using 3.3K ohms source impedance. However, because the MOSFET on resistance is approximately 2.2K ohms plus the fixed resistor of 1K ohm, the total offset presented to the coder is approximately (3.3K + 2.2K + 1K) x 0.1 microampere, or 0.65 millivolts.

V-6 APERTURE TIME.

The aperture time of the coder while storing the input analog sample is 170 ±30 microseconds. The aperture time error occurs when the transducer voltage changes during the time the coder is storing the sample. This dv/dt becomes a maximum at the highest input frequency which is 0.2 cps (one fifth of the maximum sampling rate of 1 sps for prime channels). This aperture time error in the Nimbus B PCM is negligible because the resulting maximum dv/dt of a 0.2-cps sine wave during the 170-microsecond sampling time is less than 1 millivolt.

NOTE

If a noise spike occurs on the input sample just before the 170 microsecond aperture time is completed, the sample stored on the ramp capacitor will be in error by the amount of added noise.

V-7 CAPACITY CHARGE TRANSFER.

When any analog channel gate is turned on, the stray capacity (approximately 30 picofarads) inside the Nimbus B PCM multiplexer must be charged and stabilized before the coder completes its 170-microsecond sample time, otherwise an error will result. The correct value of the analog sample is reached only after the multiplexer capacity has been completely charged from both the external capacity and input transducer. Before the sample occurs, the transducer has already completely charged the PCM external stray capacity through the transducer source impedance. When the sample occurs, the external stray capacity discharges into the multiplexer stray capacity and then both the external and internal capacities must be stabilized through the transducer source impedance before the sample time is completed. Because the PCM multiplexer contains only 30 picofarads of stray capacity, this charge transfer time is approximately 30 microseconds for 10 R-C time constants with a source impedance of 100K ohms. Since 30 microseconds is small compared to the 170-microsecond aperture time, the charge transfer error is negligible.

V-8 INPUT NOISE.

Input noise can cause errors depending on the magnitude of the peak noise in the input data sample. However, these errors can be averaged over a period of time if the noise remains fairly constant. If this noise is purely random and occurs with large maximum-to-minimum ratios, some data points will have to be discarded as no correlation will exist between the sample and the noise. This noise will increase directly with an increase in transducer source impedance, so that noise-free measurements require a 0-ohm source impedance. Inversely, large amounts of stray wiring capacity on a transducer will help filter out the noise peaks. With special care and attention given to the transducer cabling problem, the noise can be reduced to a negligible amount.

APPENDIX VI

USE OF 10-BIT CODING CAPABILITY

VI-1 GENERAL.

The accuracy of selected analog measurands can be increased to 8, 9, or 10 bits by externally connecting the desired three least significant bits of the coded value to an immediately following digital channel.

The seven most significant bits from the 10-bit coder are automatically connected into the output register to provide the standard Nimbus B 8-bit data word consisting of a word sync ZERO bit plus seven data bits. The three least significant bits (2^0, 2^1, and 2^2) are applied to failsafe isolation buffer amplifiers in each programmer, thus connecting the three bits from each PCM to the same three outputs. In this way the three bits are always supplied from the selected PCM (PCM 1 or PCM 2). These three wires are applied to pins 1, 2, and 3 of both connector J1 and connector J13. For 8-bit analog words (±0.4 percent resolution), only the 2^2 bit is used; for 9-bit analog words (±0.2 percent resolution) both the 2^2 and the 2^1 bits are used; and for 10-bit analog words (±0.1 percent resolution) the 2^2, 2^1, and 2^0 bits are used. It does not matter which digital channels in the following digital word are used for the three bits, as read-in is performed in parallel for all seven digital bits. However, the BTE equipment is designed such that the first three data bit positions must be used if the analog 10-bit word is to be displayed. The digital channels in the digital word that are not used for the increased resolution bits remain available for use as digital channels.

There are four possible combinations for increased analog word resolution:

a. Prime analog channel followed by a prime digital word.

b. Prime analog channel followed by a subcommutated digital word.

c. Subcommutated analog channel followed by a prime digital word.

d. Subcommutated analog channel followed by a subcommutated digital word.

These four combinations are described in the following paragraphs. The combination in c, above, achieves the maximum number of increased resolution analog channels with the minimum number of external jumper wires.

VI-2 PRIME ANALOG CHANNELS FOLLOWED BY PRIME DIGITAL CHANNELS.

There are five prime analog channels followed by prime digital channels as shown in figure VI-1. (Figure VI-1 is derived from the PCM output format tables.) These channels are 1A1, 1A8, 1A9, 1A20, and 1A21. Ten bits of resolution on any one of these channels requires that three external jumper wires be connected from the drivers for bits 2^2, 2^1, and 2^0 to the digital channel immediately following. Thus, if all five prime analog channels are connected for 10 bits of resolution, 15 external jumper wires are required. All five of these prime analog 10-bit samples will occur at a 1-sps rate.

WORD POSITION WITHIN A SUBFRAME	SUBFRAME NUMBER 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
3										1/16 A244						
										1/16 D22						
5	1A1	1A1	1A1	1A1	1A1	1A1	1A1	1A1	1A1	1A1	1A1	1A1	1A1	1A1	1A1	1A1
	1D1	1D1	1D1	1D1	1D1	1D1	1D1	1D1	1D1	1D1	1D1	1D1	1D1	1D1	1D1	1D1
8	1/16 A3	1/16 A26	1/16 A54	1/16 A82	1/16 A108	1/16 A136	1/16 A162		1/16 A218	1/16 A246	1/16 A276	1/16 A302	1/16 A330	1/16 A356	1/16 A383	1/16 A411
	1D2	1D2	1D2	1D2	1D2	1D2	1D2		1D2	1D2	1D2	1D2	1D2	1D2	1D2	1D2
10	1A2										1A2					
	1/16 D1										1/16 D23					
12		1/16 A28	1/16 A56	1/16 A84	1/16 A110	1/16 A138	1/16 A164	1/16 A190	1/16 A220	1/16 A248		1/16 A304	1/16 A332	1/16 A358	1/16 A385	1/16 A413
		1D3	1D3	1D3	1D3	1D3	1D3	1D3	1D3	1D3		1D3	1D3	1D3	1D3	1D3
14	1A3										1A3					
	1/16 D2										1/16 D25					
18												1A5				
												1/16 D27				
19		1/16 A31														
		1/16 D3														
22												1A7				
												1/16 D28				
23		1/16 A32														
		1/16 D4														
25	1A8	1A8	1A8	1A8	1A8	1A8	1A8	1A8	1A8	1A8	1A8	1A8	1A8	1A8	1A8	1A8
	1D4	1D4	1D4	1D4	1D4	1D4	1D4	1D4	1D4	1D4	1D4	1D4	1D4	1D4	1D4	1D4
27			1/16 A63													
			1/16 D5													
29	1A9	1A9	1A9	1A9	1A9	1A9	1A9	1A9	1A9	1A9	1A9	1A9	1A9	1A9	1A9	1A9
	1D5	1D5	1D5	1D5	1D5	1D5	1D5	1D5	1D5	1D5	1D5	1D5	1D5	1D5	1D5	1D5
31			1/16 A64													
			1/16D6													
34				1A11												
				1/16D7												
35														1/16 A359		
														1/16 D33		
38				1A13										1A13		
				1/16 D9										1/16 D34		
40	1/16 A12	1/16 A40	1/16 A68		1/16 A124	1/16 A152	1/16 A178	1/16 A204	1/16 A234	1/16 A262	1/16 A288	1/16 A316	1/16 A342		1/16 A399	1/16 A427
	1D6	1D6	1D6		1D6	1D6	1D6	1D6	1D6	1D6	1D6	1D6	1D6		1D6	1D6
42					1A14											
					1/16 D11											
43															1/16 A400	
															1/16 D36	
44	1/16 A14	1/16 A42	1/16 A70	1/16 A96	1/16 A125	1/16 A154	1/16 A180	1/16 A206	1/16 A236	1/16 A264	1/16 A290	1/16 A318	1/16 A344	1/16 A371		1/16 A429
	1D7	1D7	1D7	1D7	1D7	1D7	1D7	1D7	1D7	1D7	1D7	1D7	1D7	1D7		1D7
46					1A15											
					1/16 D12											
47															1/16 A401	
															1/16D37	
50						1A7										1A17
						1/16D13										1/16 D38
54						1A19										1A19
						1/16D15										1/16D39
57	1A20	1A20	1A20	1A20	1A20	1A20	1A20	1A20	1A20	1A20	1A20	1A20	1A20	1A20	1A20	1A20
	1D8	1D8	1D8	1D8	1D8	1D8	1D8	1D8	1D8	1D8	1D8	1D8	1D8	1D8	1D8	1D8
61	1A21	1A21	1A21	1A21	1A21	1A21	1A21	1A21	1A21	1A21	1A21	1A21	1A21	1A21	1A21	1A21
	1D9	1D9	1D9	1D9	1D9	1D9	1D9	1D9	1D9	1D9	1D9	1D9	1D9	1D9	1D9	1D9

NOTES:
1. THIS TABLE SHOWS ALL ANALOG CHANNELS THAT ARE FOLLOWED BY DIGITAL CHANNELS IN THE PCM FORMAT, ALONG WITH THEIR WORD POSITIONS WITHIN THE MAJOR FRAME.
2. THERE ARE 5 PRIME ANALOG CHANNELS FOLLOWED BY PRIME DIGITAL CHANNELS.
3. THERE ARE 10 PRIME ANALOG CHANNELS FOLLOWED BY SUBCOMMUTATED DIGITAL CHANNELS.
4. THERE ARE 58 SUBCOMMUTATED ANALOG CHANNELS FOLLOWED BY PRIME DIGITAL CHANNELS.
5. THERE ARE 8 SUBCOMMUTATED ANALOG CHANNELS FOLLOWED BY SUBCOMMUTATED DIGITAL CHANNELS.
6. THERE IS A MAXIMUM OF 81 ANALOG CHANNELS FOLLOWED BY DIGITAL CHANNELS THAT CAN BE USED FOR 8, 9 OR 10 BITS OF RESOLUTION.

Figure VI-1, Ten-Bit Analog Word Availability

VI-3 PRIME ANALOG CHANNELS FOLLOWED BY SUBCOMMUTATED DIGITAL CHANNELS.

There are ten prime analog channels followed by subcommutated digital channels as shown in figure VI-1. Five of these channels (1A5, 1A7, 1A11, 1A14, and 1A15) are each followed by one subcommutated digital channel in each major frame. Each channel requires three external wires for 10-bit capability, but only one analog sample out of 16 has 10 bits of resolution. The other 15 analog samples have the normal seven bits of resolution. The remaining five analog channels (1A2, 1A3, 1A13, 1A17, and 1A19) are each followed by two subcommutated digital channels in each major frame. When connected with three external jumper wires for each digital channel, two increased resolution samples and fourteen 7-bit samples are obtained in every major frame. To connect all 10 channels for maximum capability would require 45 external jumper wires.

VI-4 SUBCOMMUTATED ANALOG CHANNELS FOLLOWED BY PRIME DIGITAL CHANNELS.

There are 58 subcommutated analog channels followed by prime digital channels as shown in figure VI-1, word positions 8, 12, 40, and 44. The 58 subcommutated analog channels can obtain increased resolution through use of only four digital words (1D2, 1D3, 1D6, and 1D7). This arrangement requires only 12 external jumper wires (3 per digital word) for 10 bits of resolution. Thus, the addition of three external jumper wires will provide for 15 high resolution subcommutated analog channels if digital words 1D2 or 1D7 are used, or 14 high resolution subcommutated analog channels if digital words 1D3 or 1D6 are used. For example, if three additional bits from pins 1, 2, and 3 of connector J1 were jumpered into 1D2 and the same 3 bits from pins 1, 2, and 3 of connector J13 were jumpered into 1D7, these six added wires provide a total of 30 subcommutated 10-bit analog words. This is the maximum 10-bit channels-to-external cabling ratio that can be obtained.

VI-5 SUBCOMMUTATED ANALOG CHANNELS FOLLOWED BY SUBCOMMUTATED DIGITAL CHANNELS.

There are eight subcommutated analog channels followed by eight subcommutated digital channels as shown in figure VI-1. The subcommutated analog channels are 1/16 A31, 1/16 A32, 1/16 A63, 1/16 A64, 1/16 A244, 1/16 A369, 1/16 A400, and 1/16 A401. For ten bits of resolution on each one of these channels, three external jumper wires per channel are required. Therefore, 24 external wires are required if all eight channels are to contain ten bits of resolution. All eight channels will have a sampling rate of one sample every 16 seconds (1/16 sps).

VI-6 SUMMARY.

If it is desired that the sampling rates for 8-, 9-, or 10-bit channels be 1 sps, only two of the five available prime analog channels are readily usable. These would be connected with 3 wires from pins 1, 2, and 3 of connector J1 to one digital word, and 3 wires from pins 1, 2, and 3 of connector J13 to a second digital word. More 10-bit channels could be added, but the complexity of the external cabling harness would be increased, and an additional special junction box would probably be required in the satellite.

If only one channel must have a rate of 1 sps, then the three wires from J1 (or J13) will provide this capability. The remaining three wires from the other connector can be used to obtain one of the channels at 1/16 sps or up to 15 channels at 1/16 sps, depending upon the digital words selected.

If the required sampling rate can be the subcommutated rate of 1/16 sps for all 10-bit analog channels, a maximum of thirty 10-bit channels can be used with the addition of 3 jumper wires from J1 and another 3 jumper wires from J13 (paragraph VI-4).

To obtain maximum capability utilizing all 81 available 10-bit channels, 96 external jumper wires are required.

APPENDIX VII

MOSFET HANDLING

VII-1. GENERAL.

This appendix contains a brief history of the MOSFET handling problem and includes handling procedures used by Fairchild and Radiation to prevent MOSFET damage.

VII-2. HANDLING PROBLEMS.

During a visit early in 1964, Fairchild advised Radiation that the biggest problem to be expected in the use of MOSFET's would be the handling of the MOSFET, both at Fairchild and at Radiation. At that time, Fairchild did not have a flatpack carrier designed to protect the MOSFET and a design modification was initiated. Controlled humidity ($< 70\%$) and the wearing of nylon smocks tend to build up an electrostatic charge; thus, the conventional "white room" aggravates the problem. Therefore, operators were instructed to wear grounding bracelets and all test chassis were tied to a common ground.

The three most usual failure modes in a conventional MOSFET are: (1) increased leakage current, gate to body, (2) increased leakage current, drain to body and/or source to body, and (3) change in threshold voltage. These generally occur in the order listed if the device has an "unprotected" gate.

The first evidence of a serious handling problem came with the delay in shipment of the first production run. An excessive number of units failed due to blown gates (excessive potential applied) and a team was dispatched to Fairchild to investigate the situation. Apparently, either a flatpack carrier problem still existed or the devices were destroyed during burn-in.

The first devices received were shipped in plastic boxes lined with a foam filler. This packaging was found to be undesirable from an electrostatic standpoint since all the material was susceptible to charge build-up. Fairchild subsequently prepared (in July 1966) an internal MOSFET handling procedure, adopted a new shipping container, and printed a warning sticker, similar to Radiation form R-599, to be placed on MOSFET shipping containers. A major excerpt from the Fairchild Mos Handling Procedure is shown on subsequent pages of this Appendix.

VII-3. RADIATION HANDLING PROCEDURES.

The MOSFET handling procedures employed at Radiation (Radiation drawing 110174) were developed from experience over the period from early 1964 to mid 1966. Many of these procedures are based on similar procedures developed by Fairchild's R&D facility.

The requirements outlined in Radiation specification 110174 consists of three basic provisions:

(1) Special handling requirements during MOSFET testing, e.g., grounding of the test chassis and operator.

(2) Special packaging provisions that require the MOSFET leads to be shorted together at all times.

(3) Special marking requirements (tag) to be placed on shipping containers. Radiation form R-599, shown below, was developed for this purpose.

III. OPERATOR PROCEDURE

Because MOS devices are extremely sensitive to electrical charges, operators must be careful to observe the following precautions, both in routine handling of the devices and in actual electrical testing.

A. Handling MOS Devices

1. Ground bracelets will be worn by operators during all processing of the MOS devices.

2. Operators will not handle MOS devices with plastic tweezers or with finger cots. Metal tweezers may be used if the operator wears a ground bracelet.

B. Transporting MOS Devices

1. Cans

   MOS cans may be transported only in metal carrier racks. The plug holes in such racks must be small enough to ensure that all leads are shorted to the circumference of the holes when the devices are inserted.

2. Flat Packs

   MOS flat packs may be transported only when the leads have been shorted to a strip of tin foil. The procedure is as follows (see Fig. 1):

   a. Lay a strip of tin foil of suitable length and width on a magnetic holder.

   b. Place the MOS flat packs in the center line of the tin foil strip with the leads perpendicular to the length of the tin foil.

   c. Fold the edges of the tin foil over the flat packs so that all leads are shorted to the foil.

   CAUTION: Steps b and c may be performed only while wearing ground bracelets.

3. MOS jobs may be transported from one location to the next only when accompanied by a Handling Precautions Card (Exhibit I). This card will be attached to the controlling documents by the Control Cage immediately after the documents have been issued by the scheduling group.

C. Testing MOS Devices

1. Ground bracelets must be worn by operators throughout the entire test procedure; when removing and replacing devices from and to the metal carrier racks, and when inserting and pulling devices from test sockets.

2. Operators must be careful not to insert MOS devices into a socket that has power applied to it.

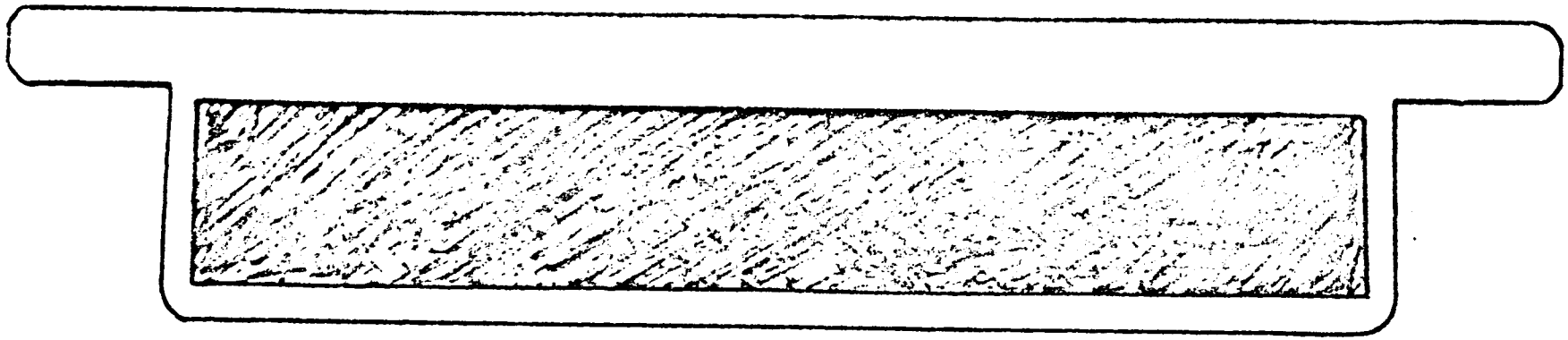
3. Devices shall be inserted carefully into sockets to ensure the best possible contact.

4. Operators shall not test devices on a Curve Tracer without the direct supervision of a foreman.

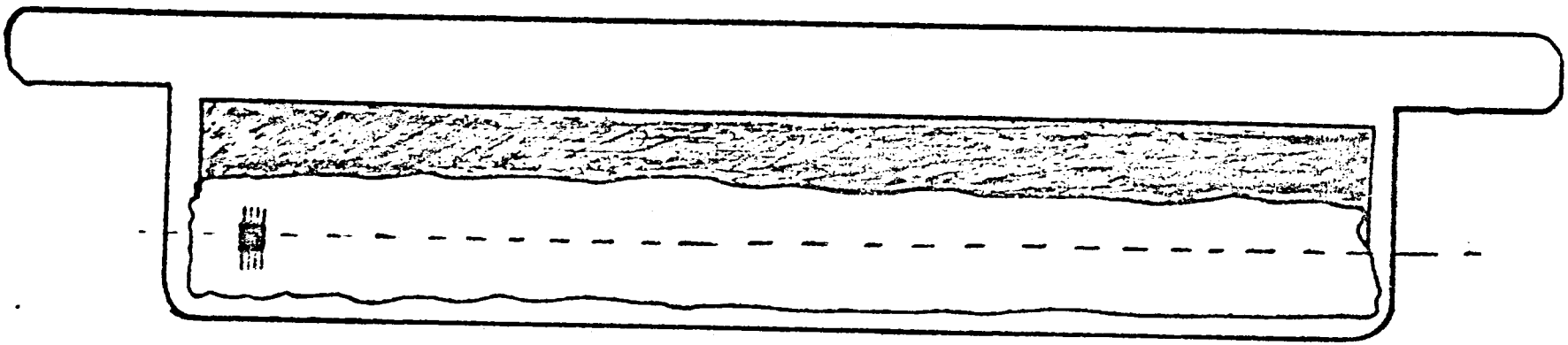
D. Storage of MOS Devices

When MOS devices are awaiting further processing, they shall be stored in the transportation carriers described in paragraph B and the carriers grounded to metal shelves.

FIGURE 1



Place strip of tin foil of suitable length and width on magnetic strip.



Place units on the center line of the tin foil with the leads perpendicular to the length of the foil strip.

Fold the edges of the tin foil over the flat packs so that all leads are shorted to the foil.

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REVISIONS

SYM	DESCRIPTION			DATE	APPROVED
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REVISION INDEX	SHEET	1	2	3
	REV			

DRAWN BY M. Blaker 7/21/65

CHECKED BY J. Skolnik 7/21/65

ENGINEER J. A. Wolcott 7/21/65

PROJECT ENGINEER W. A. Broadway 22 JUL 65

REL J. E. Dulac 7/21/65 | STDS M. Blaker 7/29/65

APPROVAL J. W. Ferguson 7/30/65

APPROVAL

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TITLE

HANDLING AND SHIPPING
FLATPACK AND MOS-FET DEVICES

CODE IDENT NO.	SIZE		REV
91417	A	110174	
SCALE	VII-6	1064	SHEET 1 of 3

RAD FORM 459 REV 7-61

1. SCOPE

This drawing specifies special handling and shipping procedures for flatpacks and MOS-FET (metal oxide silicon-field effect transistor) devices.

1.1 Implementation. The Quality Control Division shall be responsible for enforcing the procedures established in this document.

2. REFERENCED DOCUMENTS

N/A

3. REQUIREMENTS

3.1 General. More than normal care should be exercised in the handling of flatpacks and MOS-FET's because of the fragile nature of the devices.

3.2 Packaging.

3.2.1 Flatpack Packaging. Flatpacks shall be received at Radiation Incorporated in individual packages. In the event they are not:

1. Stop processing of shipment
2. Notify Quality Control and Reliability
3. Determine damage, if any
4. Determine disposition by Engineering Quality Control and Reliability
   (a) Return to manufacturer
   (b) Obtain proper packaging

The units shall remain in their individual packages until removed from the stock room for assembly purposes. The packages shall be of such quality to prevent damage to the device leads.

3.2.2 MOS-FET Packaging. The devices shall be individually packaged with all device leads shorted together. The units shall not be removed from this package except by the approved handling procedures called out herein for purposes of testing. After any required testing is complete, the device shall be repackaged and stored until required by assembly.

3.2.3 Manufacturer Packaging. Each device shall be packaged in such a manner to facilitate easy removal of individual devices. This is best accomplished by placing each device in individual packages which may be packed together in a larger container.

3.3 Handling.

3.3.1 Flatpack Handling. Where at all possible flatpacks shall be handled without removal from the individual packages. When removal is necessary the device shall be removed only by persons wearing finger cots, or equivalent. In no case shall a flatpack be placed in a bare hand. Care should be exercised to avoid bending of the device leads; the best method being to handle flatpacks with tweezers only.

3.3.2 MOS-FET Handling. Where at all possible the devices shall be handled without removal from the individual packages. When removal from the packages is necessary the procedures specified in Paragraph 3.3.2.1 shall be followed.

3.3.2.1 Removal from the Individual Packages. Before the MOS-FET is removed from its individual container the following steps shall be taken.

1. The unit shall be removed from its container only on a conducting bench top: In the event testing is to be performed, a common scheme shall be established.
2. All workers must have ground straps from the bench top attached to their wrists.
3. All workers must wear finger cots, or equivalent.
4. Surfaces of hands and probing tools must be discharged to the bench top prior to touching the devices.

3.3.3 Manufacturer Handling. The manufacturer shall exercise all handling procedures called out in this document or approved equivalent as minimum handling requirements.

3.4 Lead Straightening. In the event the leads inadvertantly become bent they may be straightened by use of tweezers or fingers (properly cotted) provided the bend is a gentle bend having no crimping. In the event the lead is sharply bent or crimped or bent in two or more opposing directions, the device shall be forwarded to the Reliability Section for evaluation.

3.5 Purchasing. The responsible Radiation Incorporated buyer shall attach Radiation Form Number R-599 to all copies of the Purchase Order, and provide the manufacturer with an adequate number to be attached to the outside of the device shipping containers.

3.6 Improper Shipping Notice. In the event that an MOS shipment is received without the required marking (reference Para 3.9) and/or packaging, Receiving shall notify Purchasing, the appropriate project, Quality Control, and the Reliability Components Engineer.

3.7 MOS Storing. The devices shall be stored (in the individual packages with all leads shorted together), by normal stockroom procedures. However, precautions shall be taken to assure the devices are stored in an area absent of any strong magnetic or electric fields, such as those found around electric motors and immediately surrounding fluorescent lights.

3.8 MOS-FET Leads. Each MOS-FET shall have all leads shorted together.

3.9 MOS-FET Shipping Instructions. Each shipment of MOS-FET's shall be marked plainly and visibly on at least two opposing sides of the shipping container "MOS-FET - SPECIAL HANDLING REQUIRED". Special Radiation Form Number R-599 for this purpose may be obtained from the Purchasing Department, Radiation Incorporated.

APPENDIX VIII

GLOSSARY OF TERMS

TERM	DEFINITION
A	Analog measurand
A/D Converter	Converts analog measurements to equivalent digital words.
Accuracy	Accuracy of final encoded data compared to original analog transducer input is ±0.7%.
Analog Gate	A transistor switch through which an analog measurand is applied to the A/D converter.
Aperture Time	The time a given measurand is applied to the A/D converter (170 ±30 μs).
BTE	Bench Test Equipment
Beacon	Transmitted 10-kc time code or transmitted 10-kc time code plus PCM real-time data.
Binary Code	A combination of bits, each of which can assume one of two possible states.
Bit	One binary digit
Bit Rate	500 cps in real-time; 15 kc in playback
Block Redundant	Identical assemblies/circuits within the PCM.
CC	Column command
Clock (Nimbus C Clock)	Master timing device in the Nimbus B satellite.
Clock Command	Command to the PCM subsystem; originated by the clock from ground command.
Coder	A/D converter
CY1A	1 cps from clock
CY10	10 cps from clock
CY500	500 cps from clock
D	Digital measurand

TERM	DEFINITION
DC-to-DC Converter	Converts -24.5 vdc to all voltages required for PCM operation.
DG	Subcommutated digital channel
DGP	Prime digital channel
Data	The final encoded output of all measurands.
Data ZERO	Digital bit between +0.5 vdc and -1 vdc at input.
Data ONE	Digital bit between -5 vdc and -10 vdc at input.
Digital Gate	A transistor switch through which a digital measurand is applied.
Energy Gap	Voltage magnitude required to break down a semiconductor in the forward bias direction.
Fail-Safe	Built-in safeguard that reasonably ensures the recovery of data through redundant techniques and ensures that chain reaction as a result of any one failure is limited.
Flat-Pack	A device containing several integrated circuits.
Format	The composition of the telemetered data.
GPA	General purpose amplifier
Ground Command	Command from the ground station causing the PCM subsystem to execute a given function.
Integrated Circuit	Diffused electronic circuit including transistors, diodes, resistors and capacitors.
LSB	Least significant bit
Line Capacity	Stray internal or external wiring capacitance to ground.
Linearity	All PCM encoded levels must be within ±0.5% of a straight line from zero scale to full scale (-6.4 vdc).
MD	Matrix driver

TERM	DEFINITION
MM10A	10-kc time code from clock; pulse width modulated.
MO	Time code from clock
Major Frame	One complete sample of all data plus time code; 1000 words (16 subframes).
MOSFET	Metal oxide silicon field effect transistor.
NRZ	Non-return-to-zero; a form of coding telemetry data.
NRZ to Split-Phase Converter	Converts non-return-to-zero type binary code to split phase Mark 0 type of code.
Nimbus A	The first Nimbus weather satellite, launched 8-28-64.
Nimbus B	The third Nimbus weather satellite; a redesigned version of Nimbus A .
Nimbus C	The second Nimbus weather satellite. Designed as back-up for Nimbus A but since modified to include additional experiments. Successfully launched 5-15-66.
Noise Immunity	The ability of a device to resist the effects of electrical noise.
PAM	Pulse amplitude modulation
PCM	Pulse code modulation. PCM telemetry unit.
PSC	Power supply common
Prime	Data channels sampled once per second.
RC	Row command
Real Time	Time in which reporting on events or recording of events is simultaneous with the events.
Resolution	Binary weight of least significant bit of the encoded word.
SPS	Samples per second
Sample Time	The time during which an analog gate or digital gate is enabled and capable of accepting a data input.

TERM	DEFINITION
SAT	Select at test.
Sequencer	A device used to make a series of events follow in a given sequence. Used as a commutator and subcommutator.
Split Phase	A form of coding telemetry data.
Strobe	A digital pulse used to enable a gate or trigger a flip-flop.
Subcommutated	Data sampled every 16 seconds.
Subframe	One complete sample of all prime data (62.5 words).
Supercommutation	Data sampled more than once per second.
Sync Word	Fixed binary code used as recognition for start of every major frame, subframe and word.
TME	Telemetry electronics unit
Time Code	Code generated by the clock and included with the data; used as a time reference.
Transducer	A device that responds to a physical stimulus and produces an electrical signal equivalent.
Word	Eight binary digits
YA1	100 cps from clock
YB1	100 cps from clock