GIMBAL POSITION CONVERTER

FINAL REPORT

April 10, 1967

SUBMITTED TO: National Aeronautics and Space Administration
George C. Marshall Space Flight Center,
Huntsville, Alabama 35812

REFERENCE: Contract No. NAS8-20655
Control No. DCN-17-40-79010

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GIMBAL POSITION CONVERTER

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Data Systems Division

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1.0 INTRODUCTION

This is a final report which documents and summarizes the results of the Gimbal Position Converter contract. Specifically, this report contains a summary of the System Design Objectives, the Mechanical and Electrical Design and Test Results and Conclusions.

2.0 DESIGN OBJECTIVES

The Gimbal Position Converter was designed as a functional piece of ground support equipment with maximum reliability and minimum maintenance as design goals.

In general, the system employs high reliability MIL-STD parts, or equivalent, to the greatest extent possible. Due to the prototype nature and short delivery requirements, screened components were not used. However, the components used are unscreened versions of components whose reliability performance has been proven by a number of previous applications on Data Systems Division designed and delivered systems.

The finalized design objectives are listed below:

2.1 Digitize the pulse width outputs of a two speed resolver, every 4 milliseconds in such a way that the basic resolver accuracy and resolution are maintained to the greatest extent possible. That is, a selectable resolution for the converter of 17 or 19 bits with an accuracy of $\pm$ 1 bit.

2.2 Display the digitized resolver position in natural binary form and provide a capability for remote readings.

2.3 Provide a digitized position output in cyclic binary (gray) code form.

2.4 Accept cyclic binary code from the computer data channels (Position Command) and compare it with the digitized position and compute the difference (Error).

2.5 Display the five (5) least significant bits of the difference (command minus position) in natural binary form and provide a sign bit indication to indicate direction of desired rotation for minimum angle of travel.

2.6 Provide continuous bipolar analog output ($\pm$ 0.5 volt) proportional to the command position difference. Since the analog signal is derived from a digital word, it will have short transition periods once every 4 milliseconds as the data is updated. Full scale error output will be provided when error greater than 5 bits exist and the 5 LSB difference is 0. Any non-zero difference in the 5 LSB will control the magnitude of the analog error output. The sign of the analog

2.6 (Continued)

signal will indicate the desired rotation for minimum angle of travel.

2.7 The system will operate on 115 $\pm$ 10 volts, 60 $\pm$ 10 HZ power.

2.8 Maximum use is to be made of microelectronic circuits and all electronic components are to meet or exceed military standards. Temperature range is to be from $0^{o}C$ to + $70^{o}C$.

2.9 The design will be all electronic (i.e., no electromechanical parts will be considered).

2.10 Reliability will be a design criteria of the converter. The Data Systems Division reliability program, which conforms to NASA Document NPC 250-1, will be utilized to ensure that reliability and maintainability requirements are met during the design, manufacturing, and test phases of the contract.

2.11 Packaging of the system is to be such that it will mount on slides in a standard 19" relay rack utilizing minimum volume while maintaining good human engineering and

2.11 (Continued)

maintainability considerations. Mechanical design will be such that the unit will withstand the rigors of handling and shipment.

2.12 The system, including all parts and accessories, will be of high quality construction and finish.

3.0 DESIGN SUMMARY

3.1 Mechanical Design

3.1.1 Package

The Gimbal Position Converter components are packaged in a relatively conventional manner. The basic circuitry is on printed circuit modules that mount along with the power supplies in a chassis designed for use in standard 19" racks. Locking chassis slides are provided which allow the chassis to be locked in either the closed or extended position and which allow the chassis to be rotated up or down when extended. This feature allows maximum accessibility to the modules and chassis wiring for trouble-shooting. The packing density of the converter is sufficiently low as to make the use of forced air cooling unnecessary.

The chassis and front panel used in the Gimbal Position Converter is aluminum with the chassis being protected by a chemical film (Alodine) per MIL-C-5541. The front panel is painted with grey enamel. The chassis and mounting provisions are capable of withstanding a 5 "g" shock load.

3.1.2 Front Panel

The Gimbal Position Converter front panel layout conforms with "human engineering" requirements. The control switches are located conveniently and are sufficiently large to ensure ease of operation. Each control switch function is provided with an indicator lamp with visually identifies the status of the system. All indicator lamps are Eldema long-life cartriges with an extended lens to facilitate viewing from wide angles.

3.1.3 Printed Circuit Cards

The system incorporates a Gulton Industries Standard PC Board size for integrated circuits. The PC Boards are 4.250" wide and 2.375" high, excluding keyboard. The cards consist of an epoxy glass substrate with copper circuitry per MSFC-STD-154. The circuitry is hot tin-lead coated for improved environmental protection of the copper circuitry and ease of soldering. The use of the hot tin-lead coating rather than gold also prevents detrimental effects of the gold-solder amalgamation on solder joints. The sixty (60) contact fingers, which are on 0.1"

3.1.3 (Continued)

centers on both sides of the board, are gold plated to lower contact resistance and provide protection for the copper.

After assembly and inspection, the PC module, excluding the contact area, is conformal coated with polyurethane, Laminar X500, Printed Circuit Clear 7-C-23, mixed with Fungitrol #11.

3.1.4 Special Tools

Module extenders are required to extend the plug-in type modules contained in the unit. Other than this, the system is designed to require no other special tools, maintenance kits, or similar items for system maintenance, repair, or calibration.

3.2 Electrical Design

See Figure 1, "Gimbal Position Converter Block Diagram."

3.2.1 Input Conditioners

Input signal conditioning is accomplished to perform logic level interfacing, to prevent loading of input signals, to "square up" wave forms, and to provide noise immunity

3.2.1 (Continued)

against normal line noise.

3.2.1.1 Course and Fine Resolver Input Conditioner (See Sketch 1)

The course and fine resolver inputs are routed to Fairchild μA 710 high speed differential comparators. These units are differential voltage comparators intended for applications requiring high accuracy and fast response times. The device is used in this configuration as a variable threshold Schmitt Trigger. A potentiometer is provided to adjust the triggering threshold from 0 to +3 volts to allow for variation in pulse level as well as to provide a means of increasing the noise threshold if necessary.

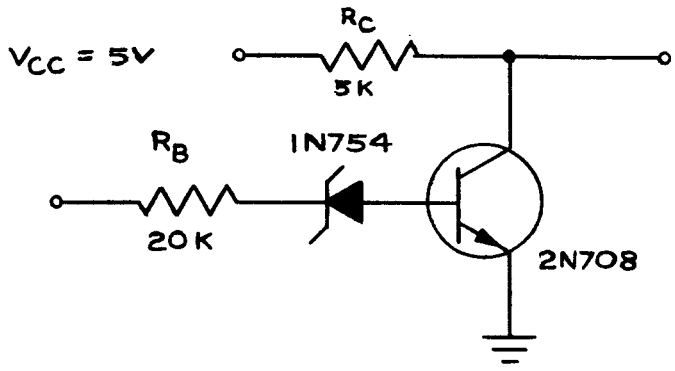
The output of the μA 710 comparator is logic compatable and drives the digitizer isolation gates directly. A 1.8K resistor connected between the minus six (-6) volt supply and the comparator output increases the comparator fanout to ensure sufficient drive.

3.2.1.2 Computer Command Input Conditioners

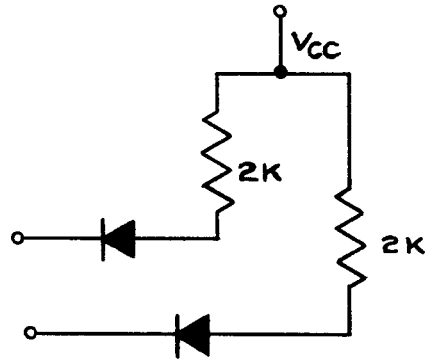
The 19 bit computer position command inputs are level shifted to match the converter micrologic levels. The input level is

3.2.1.2 (Continued)

Low = 0V, High = 28V. The output of the level shifter is Low = 0V, High = + 5V. The level shifter is a discrete component device consisting of a 2N708 switching transistor in the common emitter configuration. A 1N754 zener diode is included in the base circuit to increase the input threshold and provide added noise immunity.



DRIVING 2 - 949 GATES



$$I\ gate \approx \frac{V_{CC}}{2K} = \frac{6}{2 \times 10^3} = 3\ ma/gate$$

$$\text{then } I_G = \overline{6\ ma}$$

INPUT LEVELS	OUTPUT LEVELS
H = 28 ± 3V	H = 4.5 ± .5V
L = 0 + 3V	L = 0 + .5V

3.2.1.2 (Continued)

$$I_C = \frac{V_{CC}}{R_C} + I_G = \frac{5}{5K} + 6 \text{ ma} = 7 \text{ ma}$$

$$I_B = \frac{I_C}{\beta} = \frac{7 \times 10^{-3}}{10} = 0.7 \text{ ma}$$

$$R_B = \frac{V_{BB} - V_Z}{I_B} = \frac{25-7}{7 \times 10^{-4}} = 2.58 \times 10^4 = 25K$$

(use R_B = 20 K based on worst case analysis shown below.)

WORST CASE ANALYSIS ON

$$\overline{I_C} = \frac{\overline{V_{CC}} - \overline{V_{SAT}}}{\underline{R_C}} + \overline{I_G}$$

$$\underline{R_C} = 5K - 10\% = 4.5K$$

$$= \frac{5.5 - .5}{4.5 \times 10^3} + 6 = 7.1 \text{ ma}$$

$$\underline{I_B} = \frac{\overline{I_C}}{\underline{\beta}} = \frac{7.1}{10} = .71 \text{ ma}$$

$$\underline{I_B} = \frac{\underline{V_{BB}} - \overline{V_Z} - \overline{V_{BE}}}{\overline{R_B}}$$

$$\overline{R_B} = 20K + 10\% = 22K$$

$$= \frac{25 - 7.1 - .9}{2.2 \times 10^4} = \frac{17}{2.2 \times 10^4} = .77 \text{ ma}$$

WORST CASE ANALYSIS OFF

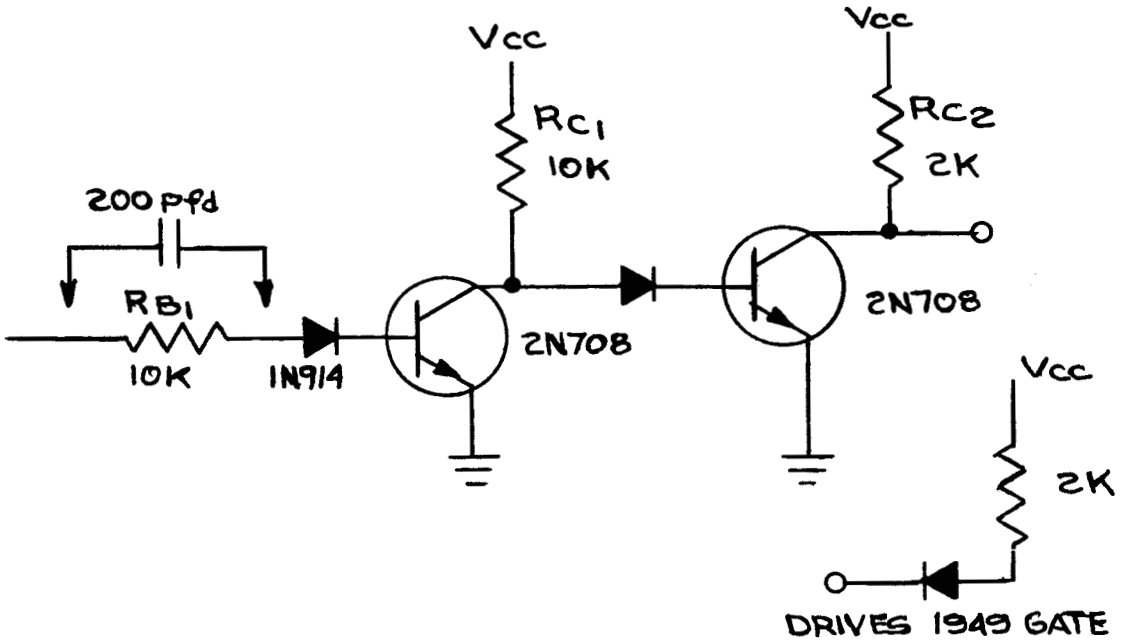
$$\bar{I}_{B\ Off} = \frac{\overline{V}_{BB} - \underline{V_Z} - \underline{V_{BE}}}{R_B} = 3 - 6 = 0$$

$$\bar{I}_{CO} = \frac{\overline{V}_{CC} - \overline{V_{C\,OFF}}}{\overline{R}_C} \qquad R_C = 5K + 10\% = 5.5K$$

$$= \frac{5.5-4}{5.5 \times 10^3} = .275 \text{ ma}$$

3.2.1.3 Clock Input Conditioner

The clock input conditioner consists of a two stage saturated amplifier with a diode input to provide a 1 volt minimum threshold for noise immunity. An input base resistor capacitor bypass can be included to provide 8 MHz transmission line termination.



Second Stage

$$I_{C_2} = \frac{V_{CC}}{R_{C_2}} + I_G = \frac{5}{2K} + 3 \text{ ma}$$

$$= 5.5 \text{ ma}$$

$$I_G = \frac{5}{2K} = 3 \text{ ma}$$

$$I_{B_2} = \frac{I_C}{\beta} = \frac{5.5 \text{ ma}}{10} = 0.55 \text{ ma}$$

3.2.1.3 (Continued)

First Stage

$$I_{C1} = \frac{V_{CC}}{R_{C1}} + I_{B2} = \frac{5}{10K} + .55 \text{ ma}$$

$$I_{C1} = 1.5 \text{ ma}$$

$$I_{B1} = \frac{I_{C1}}{\beta} = \frac{1.5 \text{ ma}}{10} = .15 \text{ ma}$$

$$R_{B1} = \frac{V_{BB} - V_{DF} - V_{BE}}{I_{B1}} = \frac{5 - 1 - 1}{1.5 \times 10^{-4}}$$

$$= \frac{3}{1.5 \times 10^{-2}} = 20 \text{ K use } 10 \text{ K}$$

Worst Case ON

Second Stage:

$$\overline{I}_{C2} = \frac{\overline{V}_{CC} - \overline{V}_{SAT}}{\underline{R}_{C2}} + I_G \qquad \underline{R}_C = 2K - 10\% = 1.8K$$

$$\overline{I}_{C2} = \frac{5.5 - .5}{1.8K} + 3 \text{ ma} = \frac{5}{1.8} + 3 \text{ ma} = 5.8 \text{ ma}$$

$$\underline{I}_{B2} = \frac{\overline{I}_{C2}}{\underline{\beta}} = \frac{5.8 \text{ ma}}{10} = .58 \text{ ma} \qquad \overline{R}_{C1} = 10K + 10\% = 11K$$

$$\underline{I}_{B2} = \frac{\overline{V}_{CC} - \overline{V}_{BE}}{R_{C1}} = \frac{5.5 - 1}{11K}$$

$$= \frac{4.5}{11K} = 4.1 \text{ ma}$$

First Stage:

$$\overline{I}_{C1} = \frac{\overline{V}_{CC} - \overline{V}_{SAT}}{\underline{R}_{C1}} + \overline{I}_{B2} = \frac{5.5 - .5}{9K} + 4.1 \text{ ma}$$

$$\underline{R}_{C1} = 10K - 10\% = 9K$$

3.2.1.3 (Continued)

First Stage:

$$= \frac{5}{9K} + 4.1 \text{ ma} = 4.7 \text{ ma}$$

$$\underline{I_{B1}} = \frac{\overline{I_{C1}}}{\underline{\beta}} = \frac{4.7 \text{ ma}}{10} = .47 \text{ ma}$$

$$I_{B1} = \frac{\underline{V_{BB}} - \overline{V_{DF}} - \overline{V_{BE}}}{\overline{R_{B1}}} = \frac{6 - 1 - 1}{11K} = \frac{4}{11K} = .36 \text{ ma}$$

$$\overline{R_{B1}} = 10K + 10\% = 11K$$

Worst Case Off

$$\overline{I_{B\ off}} = \frac{\overline{V_{BB}} - \underline{V_{DF}} - \underline{V_{BE}}}{\underline{R_B}} = \frac{.5 - .4 - .2}{9K} = \frac{-.1}{9K}$$

For 8 MHZ Transmission Line Termination of 100 Ohm

For 200 pfd capacitor

$$X_C = \frac{1}{2\pi fc}$$

$$= \frac{1}{(2\quad)(8X10^6)(200X10^{-12})}$$

= 99 ohms at 8 MHZ

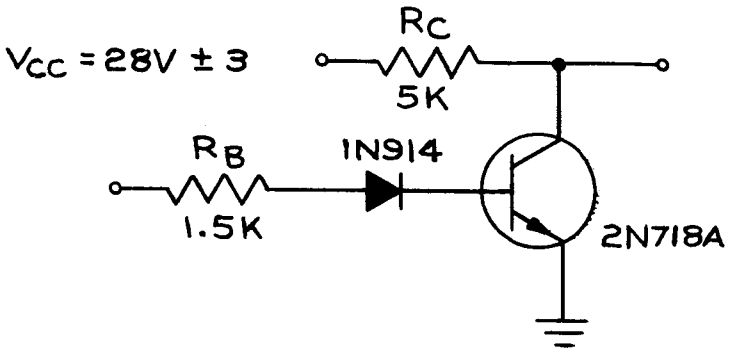
3.2.2 Output Conditioners

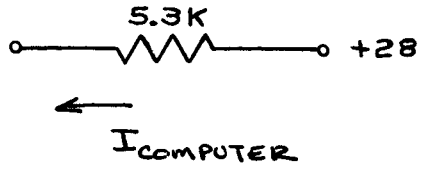
3.2.2.1 Position Gray Code Output Conditioners

The outputs of the binary-to-gray code converter (DTL 932 gates) drive discrete component level shifters which provide output logic levels of Low = 0V, High = + 28V. The level shifters are switching transistors in the common emitter configuration. The collector resistors are 3K ohm yielding an output impedance of approximately 3K ohm in "H" logic

3.2.2.1 Cont'd.

state and essentially 0 in the "L" state.





Computer Input Z = 5.3 K min
Assume worst case current of

$$\overline{I}_{comp} = \frac{31V}{5.3K} = 5.9 \text{ ma}$$

Input Levels	Output Levels
H = 5 ± .5 V	H = 28 ± 3V
L = 0 + .5 V	L = 0 + 3V

$$I_C = \frac{V_{CC}}{R_C} + I_{comp} = \frac{28}{5K} + 5.9 \text{ ma} = 11.5 \text{ ma}$$

$$I_B = \frac{I_C}{\beta} = \frac{11.5}{10} = 1.15 \text{ ma}$$

$$R_B = \frac{V_{BB} - V_{DF} - V_{BE}}{I_B} = \frac{4.5 - 1 - 1}{1.15 \times 10^{-3}} = \frac{2.5}{1.15 \times 10^{-3}} = 2.18 \text{ K}$$

Use 2.0 K

Worst Case On

$$\overline{I_C} = \frac{\overline{V_{CC}} - \overline{V_{SAT}}}{\underline{R_C}} + I_{comp} = \frac{31 - 1.2}{4.5 \times 10^{-3}} + 6 = 12.7 \text{ ma}$$

$$\underline{R_C} = 5K - 10\% = 4.5K$$

3.2.2.1 (Continued)

Worst Case On

$$\underline{I_B} = \frac{\overline{I_C}}{\underline{\beta}} = \frac{12.7}{10} = 1.27 \text{ ma}$$

$$\overline{R_B} = 1.5 \text{ K} + 10\% = 1.65\text{K}$$

$$\underline{I_B} = \frac{V_{BB} - V_{DF} - V_{BE}}{R_B} = \frac{4.5 - 1 - 1}{1.65\text{K}} = 1.5 \text{ ma}$$

Use $R_B = 1.5\text{K}$

$$\overline{I_{CO}} = \frac{\overline{V_{CC}} - \overline{V_{C\ off}} - I_{B\ leakage}\ \overline{\beta}\ \overline{R_C}}{\overline{R_C}}$$

$$= \frac{31 - 25 - (2 \times 10^{-3})(2 \times 10^{2})(6 \times 10^{3})}{6\text{K}}$$

$$\approx \frac{6}{6\text{K}} = 1 \text{ ma}$$

Worst Case Off

$$\overline{I_{B\ off}} = \frac{\overline{V_{BB}} - \underline{V_{DF}} - \underline{V_{BE}}}{R_B} = \frac{.5 - .4 - .2}{1.35\text{K}}$$

$$R_B = 1.5\text{K}\ 10\% = 1.35\text{K}$$

$$= \frac{-.1}{-.35\text{K}}$$

3.2.2.2 Binary Position Output Drivers

Nineteen DTL 932 indicator lamp drivers are wired to the "Q" side of the position storage flip-flops to provide drive for the front panel indicators. Outputs in parallel with the front panel are available at connector J6. The drivers are limited to .075 amp current. The panel lamps require .060 amp, thus, the remote outputs may not be used to drive high current lamps directly.

3.2.3 Clock Divider

A clock divider is provided to produce a 2 MHZ clock to drive the strobe generator. Divider counter decoding gates are provided to produce a 2 microsecond pulse every 4 milliseconds which is used to reset the strobe generator, digitizers, and the 19 bit serial subtractor. A Data Start Pulse, which occurs simultaneously with the reset pulse, is also provided by the clock divider. The actual data start must be triggered by the trailing edge of the start pulse. Since reset of the converter is accomplished during the pulse interval, the converter will not be ready to accept data until immediately after the pulse fall time.

3.2.3 (Continued)

The least significant bit of the divider is gated out by NAND gates in the low resolution mode to maintain the same divider output signal timing regardless of resolution mode.

The divider is composed of a 15 bit ripple-carry counter made up of DTL 950 pulse triggered flip-flops. The 950 binarys are capable of operating in excess of 20 MHZ over a temperature range of $0^{o}C$ to $+ 70^{o}C$. The first three flip-flops of the counter are contained on the same printed circuit module as the 8 MHZ clock input conditioner to provide 8 MHZ isolation from the rest of the system.

3.2.4 Coarse and Fine Digitizers

Each of the digitizers consist of a gated 13 bit ripple-carry counter. The resolver input pulses, from the pulse input conditioners, gate the 8 MHZ clock and allow the counter to accumulate clock pulses in proportion to the resolver pulse width. The first binary in each digitizer is gated out by NAND gates in the low resolution mode. The digitizers are cleared once every 4 milliseconds by the reset pulse.

3.2.4 (Continued)

This counter is also composed of DTL 950 pulse triggered binarys.

3.2.5 Ambiguity Eliminator

Error between the coarse and fine resolver outputs may cause ambiguity between the most significant bit of the fine digitizer and the corresponding coarse bit. Since the fine data always leads to the coarse data, the ambiguity can be eliminated by forcing the coarse bit to agree with the fine MSB after digitizing is complete. NAND gates, partially enabled by the status of the fine MSB, drive the direct inputs (DC) of the corresponding coarse bit. The data is transferred when the gates are enabled by the ambiguity strobe from the strobe generator when digitization is complete. The ambiguity strobe is of 1 microsecond duration which is ample time to allow any change in the coarse digitizer to ripple through and stabilize before data transfer and storage which occurs on the fall of the strobe.

3.2.6 Strobe Generator

The converter timing is based on the strobe generator

3.2.6 (Continued)

outputs which provide the necessary sequencing within the converter. The entire generator is cleared by the reset pulse every four milliseconds.

The strobe generator consists of four sections of gated ripple-carry (reset) counters made up of DTL 950 pulse triggered binarys. The 2 MHZ clock from the clock divider is gated successively to each of the four sections of counters immediately following the trailing edge of the last resolver input pulse. See Figure 2, "Gimbal Position Converter Timing Diagram."

3.2.6.1 Strobe Generator Inhibit

The strobe generator is inhibited following the reset pulse until the completion of both the coarse and the fine resolver pulses. Two DTL 950 binarys sense the fall of the resolver output pulses from the threshold Schmitt Triggers and enable the 2 MHZ clock gate for the digital position store strobe generator.

3.2.6.2 Digital Position Store Strobe

Two DTL 950 binarys, a 2 input NAND gate for counter decoding, and a counter clock control gate are used as a one pulse generator. On release of the strobe generator inhibit, the 2 MHZ clock drives the counter through the control gate. The control gate is inhibited when the counter reaches the 01 state which produces a 0.5 microsecond pulse.

The output pulse is used to strobe the ambiguity eliminator and to store the digitized position into the 19 bit storage register.

3.2.6.3 Subtractor Store Strobe

This single pulse generator is identical to the digital position store strobe generator. The clock control gate is enabled by the completion of the digital position store strobe. The .5 microsecond pulse causes parallel transfer of the stored 19 bit binary position and the 19 bit position command into the serial subtractor.

3.2.6.4 Subtractor Shift Strobes

The subtractor shift pulse generator consists of six DTL 950

3.2.6.4 (Continued)

binarys, necessary counter decoding gates, and 2 MHZ clock gate. The completion of the subtractor store strobe enables the 2 MHZ clock gate.

The position of the resolution switch sets the counter decoding to produce 19 pulses in the high resolution mode and 21 pulses in the low resolution mode. These pulses are used to circulate the data through the subtractor. The two extra shift pulses in the low resolution mode are generated to replace the two least significant bits in the subtractor which will always be "0".

3.2.6.5 Error Store Strobe

This single pulse generator is the same as the digital position and subtractor store strobe generators. On completion of the subtractor shift strobes, the 2 MHZ gate is enabled. When the second binary is set, the 5 bit subtractor error data is parallel transferred into subtractor error storage.

3.2.7 Binary Position Storage

The digitized binary position data is routed from the coarse

3.2.7 (Continued)

and fine digitizers through the resolution gates to the position storage flip-flops.

3.2.7.1 Resolution Gating

The resolution gating provides a means of routing the coarse and fine digitizer bits into the proper storage position for the selected resolution mode. In high resolution mode, all 13 fine bits and the 6 most significant bits of the coarse are stored. In the low mode, the resolution gating stores 0 in the 2 least significant bit storage positions, gates out 1 coarse bit and routes the 12 fine bits into their proper storage positions. The gating is controlled by the front panel resolution switch.

3.2.7.2 19-Bit Storage Register

Storage of the 19 bit digitized position is provided by 19 DTL 945 clocked flip-flops. The DTL 945 binarys are direct coupled operating on the "master-slave" principle. Information enters the "master" while the trigger input voltage is high and transfers to the slave when the trigger

3.2.7.2 (Continued)

input voltage goes low. Output buffers provide isolation between the "slave" and the output load, thereby enhancing immunity to signal line noise.

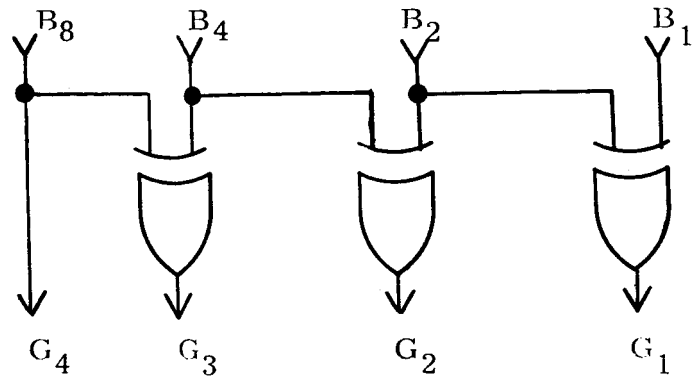
Set and clear inputs come from the 5 MSB of the coarse digitizer and from the resolution gating. The digital position store strobe, applied to the Cp inputs, stores the selected bits. The storage register flip-flops provide outputs to the indicator lamp drivers, the binary-to-gray code converter, and to the position side of the 19 bit serial subtractor (Section 3.2.11).

3.2.8 Position Display

Front panel indicators are provided to present the stored binary position. In high resolution mode all 19 indicators are utilized and their weight (2^n) is engraved above the indicators. In low resolution mode, only 17 indicators are utilized and the bit weight (2^n) engraved below the indicates is used.

3.2.9 Binary-To-Gray Code Converter

The binary-to-gray code converter consists of NAND gates wired in an exclusive-or configuration. The basic scheme of the conversion is shown below:



Boolean Equation

$G_4 = B_8$

$G_3 = B_8 \cdot \bar{B}_4 + \bar{B}_8 \cdot B_4$

$G_2 = B_4 \cdot \bar{B}_2 + \bar{B}_4 \cdot B_2$

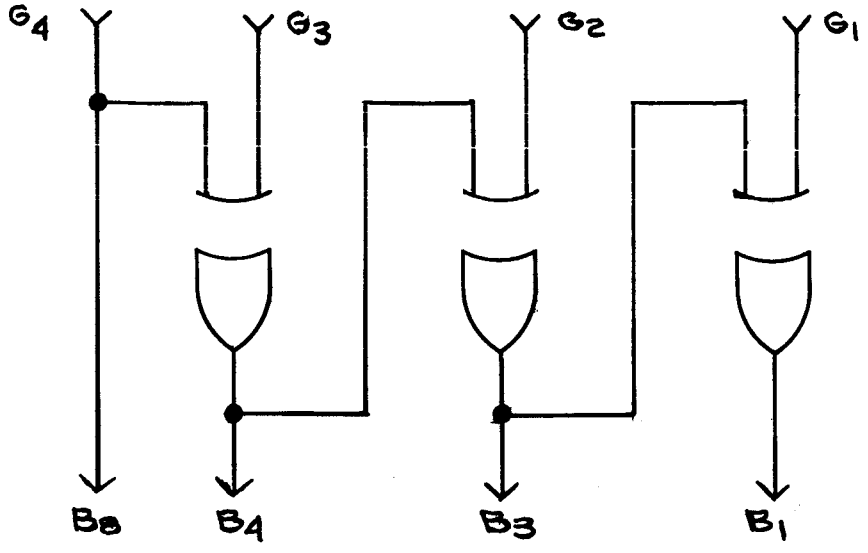
$G_1 = B_2 \cdot \bar{B}_1 + \bar{B}_2 \cdot B_1$

3.2.9 (Continued)

Note that the MSB of binary and gray are the same. In the converter, the wiring is such that the gray outputs are inverted. An additional inversion in the output level shifters provides the required gray code outputs.

3.2.10 Gray-To-Binary Code Converter

NAND gate implementation of exclusive-or is used in the gray-to-binary code converter in a manner similar to that in the binary-to-gray code converter. As shown below, gray-binary conversion differs from binary-gray conversion only in the exclusive-or input wiring.



3.2.10 (Continued)

Boolean Equation

$B_8 = G_4$

$B_4 = (G_3 + G_4)(\overline{G}_3 + \overline{G}_4)$

$B_2 = (B_4 + G_2)(\overline{B}_4 + \overline{G}_2)$

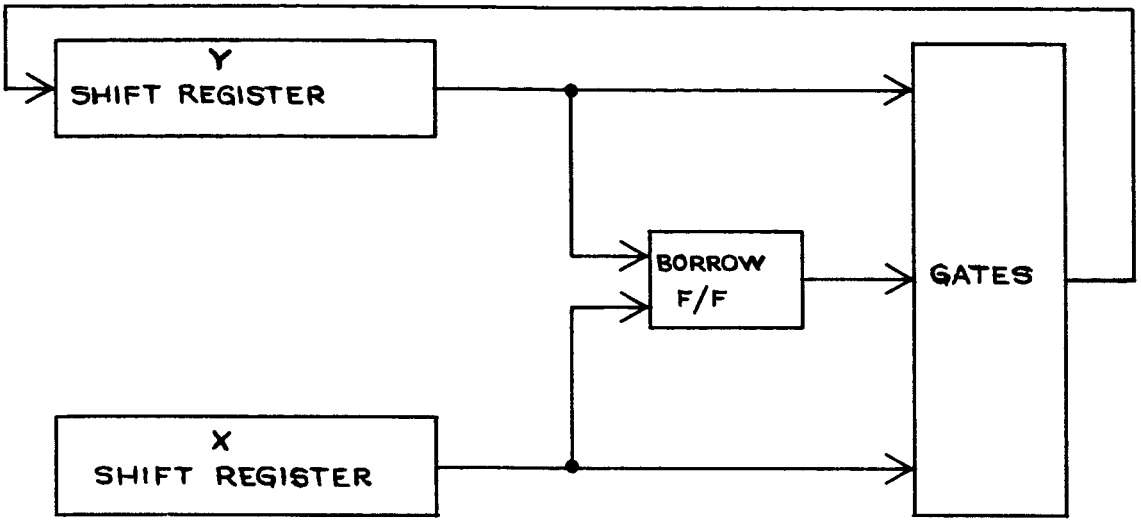
$B_1 = (B_2 + G_1)(\overline{B}_2 + \overline{G}_1)$

The binary outputs of the code converter are routed through inverters to provide both Q and $\overline{Q}$ of each command bit. The resulting binary command is stored in the command side of the 19 bit serial subtractor.

3.2.11 19 Bit Serial Subtractor

The 19 bit computer command input is subtracted from the 19 bit digitized position. The basic scheme of the subtractor is as follows:

3.2.11 (Continued)



The digitized position and computer position command data is stored in two 19 bit shift registers (registers "Y" and "X" respectively) consisting of DTL 945 "master-slave" flip-flops.

After the data has been stored, the subtractor gates and borrow flip-flop interrogate the data one bit at a time as the register contents are shifted out. The difference data from the gates is circulated back into the "Y" register. On completion of the 19 bit serial subtraction, the "Y" register will contain the 19 bit difference data.

3.2.11 (Continued)

Borrow flip-flop equations:

Set Carry FF = $\overline{X} \cdot Y$

Reset Carry FF = $X \cdot \overline{Y}$

Subtractor output gate equations:

Set Enable (Q) $= \overline{X}.\overline{Y}.C + \overline{X}.Y.\overline{C} + X.\overline{Y}.\overline{C} + X.Y.C$

Reset Enable (Q) $= X.Y.\overline{C} + X.\overline{Y}.C + \overline{X}.Y.C + \overline{X}.\overline{Y}.\overline{C}$

If the difference is negative (Position larger than command) the "Y" register will contain the complement of the desired data.

3.2.12 Error Storage

The error store strobe enables gating which parallel transfers the five LSB difference and borrow into the subtractor error storage register which consists of DTL 945 clocked flip-flops. The output of the register is routed to the Digital to Analog Converter and to the complementer for error display.

3.2.13 Complementer

The complementer provides a "ONES" complement of the subtractor data when the difference is negative (Position larger

3.2.13 (Continued)

than command). The complementer also provides full scale error output when an error greater than five bits exists and the five LSB difference is zero. (Any non-zero difference in the five LSB controls the magnitude of the analog output error).

Since this complementer is a "ONES" complementer, a one bit error will be produced for negative numbers. This error will only affect the error display and not the analog outputs as one bit is added to the D/A converter for negative numbers. For a negative number, the actual error will be the displayed number plus one (1).

The complementer is controlled by gating from the subtractor 14 MSB's and 5 LSB's, the MSB difference storage flip-flop, and the borrow flip-flop. The relationship between the complementer inputs and outputs are shown in Table 3.2.13.

TABLE 3.2.13

Complementer Truth Table

14 MSB	5LSB	MSB Diff.	Borrow	Sign Bit	Error Lamp +	Error Lamp -	Comp.	Comp. Output 1-0
No Error	No Error	0	0	L	OFF	OFF	Not	No Effect
No Error	Error	0	0	L (+)	ON	OFF	Not	No Effect
No Error	Error	0	1	H (-)	OFF	ON	Comp	No Effect
Error	Error	0	0	L (+)	ON	OFF	Not	No Effect
Error	Error	0	1	H (-)	OFF	ON	Comp	No Effect
Error	Error	1	0	H (-)	OFF	ON	Not	No Effect
Error	Error	1	1	L (+)	ON	OFF	Comp	No Effect
Error	No Error	0	0	L (+)	ON	OFF	Not	All Is
Error	No Error	0	1	H (-)	OFF	ON	Comp	All 0s
Error	No Error	1	0	H (-)	OFF	ON	Not	All 0s
Error	No Error	1	1	L (+)	ON	OFF	Comp	All 1s

As can be observed from the Complementer Truth Table, the longest interval the analog output can be full scale is the time interval required for the data (position) to change by 2 bits.

3.2.14 Error Display Drivers

DTL 932 power gates provide drive for the five bit error indication and two error sign indicators on the front panel. The driver inputs are derived from the com menter outputs.

3.2.15 Error Display

Front panel indicators provide visual indication of stored five bit error and the sign (±) of the analog output. When all five error bit indicators and the sign bit indicators are extinguished, the difference between command and position is 0.

3.2.16 Digital to Analog Converter

The digital to analog converter consists of reference voltage regulators, a voltage ladder adder with solid state switches and output amplifiers.

3.2.16.1 General

Using a voltage ladder adder configuration, the equation representative of the output of the latter as a function of inputs and sign is:

3.2.16.1 (Continued)

$$E_o = \frac{E_{REF}}{3} S - \frac{E_{REF}}{3} \left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} \right]$$

Where S represents the sign bit and can have values of 1 or 0, and Ai 's represent the 5 binary bits whose values are limited to 1 or 0.

Maximum outputs occur where S = 0 and Ai = 1 or when S = 1 and Ai = 0.

Since $\lim \sum_{i=1}^{5} A_i 2^{-i} = \frac{31}{32}$, then the maximum negative output possible is $\frac{31}{96}$ Eref and the maximum positive output is $\frac{Eref}{3}$. The maximum bipolar output is approximately $\frac{E_{ref}}{3}$ thus for $\pm$ .5V output, E_{ref} must be approximately 1.5V. To avoid switching errors, E_{ref} = 6V is used with a gain less than one amplifier on the ladder output.

The maximum bipolar output swing noted above shows a difference of E_{ref} or 1 bit difference between the $\pm$ outputs. This is because the $\lim \sum_{i=1}^{\infty} A_i 2^{-1} = 1$, thus for a finite number of Ai the fraction can never be $\frac{E_{ref}}{3}$ exactly.

3.2.16.1 (Continued)

Examination of the following truth table shows that there will be a difference of 1 bit $\left(\frac{Eref}{12}\right)$ between any positive output voltage and its corresponding negative voltage, where the negative number is obtained by complimenting the positive and setting the sign bit to 1. This difference can be eliminated by adding $\frac{E_{ref}}{12}$ to the output for all negative numbers. The example is based on two binary inputs for simplicity.

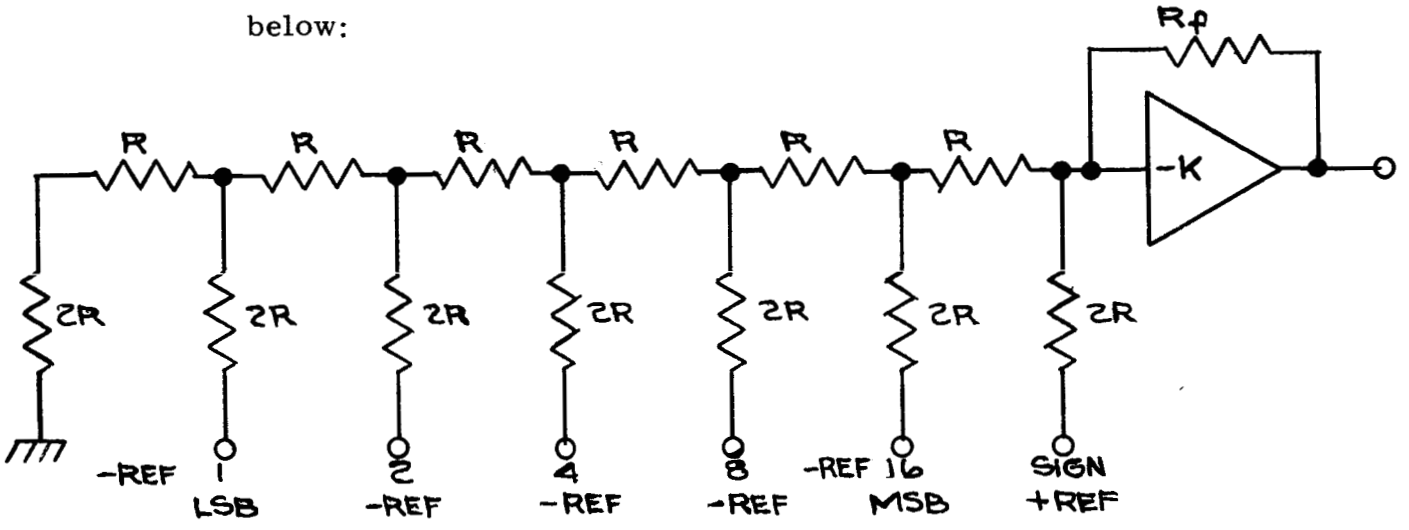
$$E_o = \frac{ErS}{3} - \frac{Er}{3}\left[\frac{A_1}{3} + \frac{A_7}{4}\right]$$

Number	A1	A2	S	Eo
+3	1	1	0	- 1/4
+2	1	0	0	- 1/6
+1	0	1	0	- 1/12
	1	1	1	+ 1/12 can't occur
-1	1	0	1	+ 1/6
-2	0	1	1	+ 1/4
-3	0	0	1	+ 1/3

3.2.16.1 (Continued)

The table also shows the reason for the one bit error discussed above. Since $A_1 = A_2 = 0$ represents zero, this combination must not be complimented since the output would not then be zero. This possibility can be eliminated since the sign bit can never be 1 if $A_i = 0$. Removal of this bit $(\frac{E_{ref}}{12})$ accounts for the one bit difference between corresponding positive and negative outputs.

A schematic of the DA ladder and output amplifier is shown below:



The ladder output is directly connected to the amplifier input thus it is effectively grounded. R_5 is the ladder impedance and $\frac{Rf}{Rs}$ determines the gain. Since the ladder

3.2.16.1 (Continued)

is terminated in zero ohms, the output current not voltage is proportional to the binary inputs. The input current caused by the LSB = 1 and all others 0 is $\frac{Er}{48r}$ since Er is divided by 3 at the first ladder junction and by 2 at each successive junction. One bit must be added to the output when the sign bit is 1 (i.e. for negative binary numbers); thus, the sign Eref must be increased by $\frac{Eref}{24}$. This means that the reference voltage to the five ladder inputs corresponding to the 5 bit digital word must be - Eref and the reference to the sign bit must be + Eref $+\frac{Eref}{24} = +\frac{25\ Eref}{24}$. With - Eref = 6V, + Eref = 6.25V.

The $\pm$ Er = 6V will give ladder outputs of approximately $\pm$ 2V which will be reduced to $\pm$ .5 by a K $\approx$ 1/4 amplifier.

3.2.16.2 <u>Reference Regulators</u> (See Sketches 2 and 3)

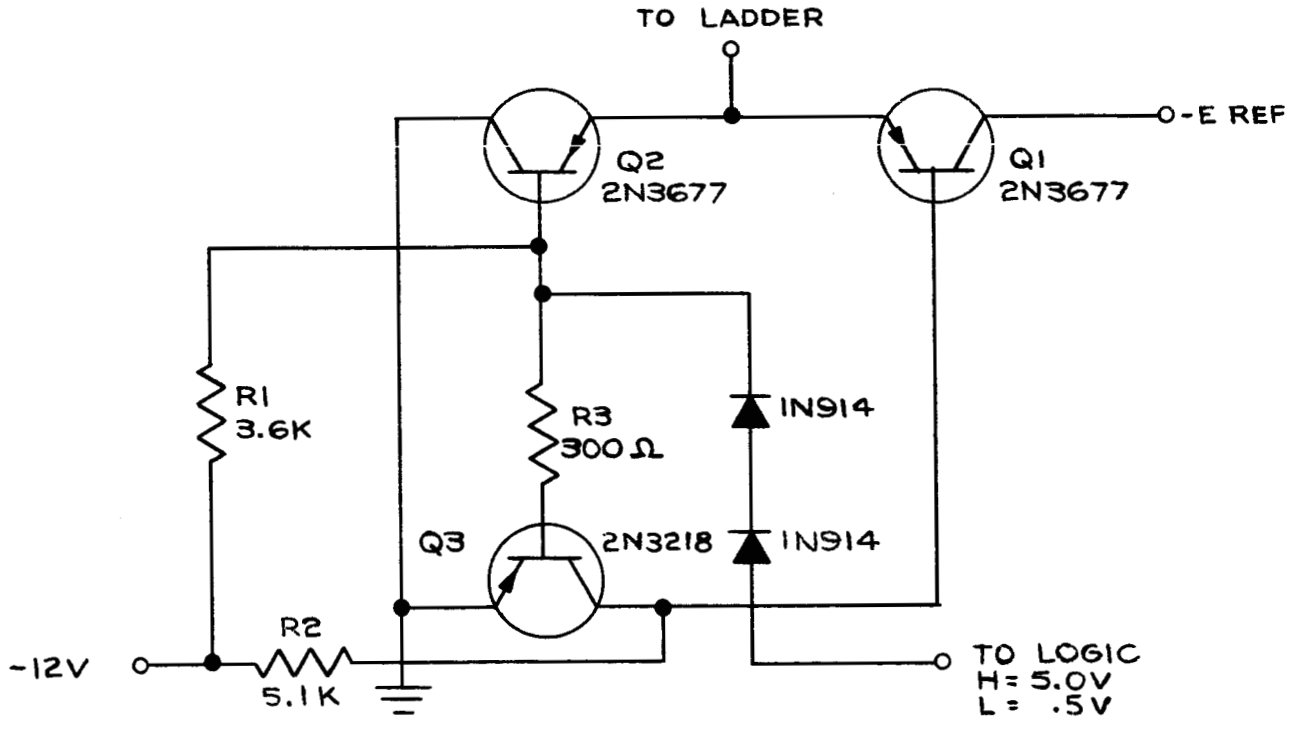
Positive and negative reference voltages are derived from two regulators. The regulators consist of A 709 operational amplifiers with an emitter follower output stage. A + 12V reference voltage is derived from the +28 volt

3.2.16.2 (Continued)

volt power supply by a 1N759 zener diode. A temperature compensated reference diode (1N939) provides a stable plus nine (+ 9) volt reference input to the reference supply amplifiers. Amplifier feedback is provided from the output of the emitter follower. A potentiometer in the feedback loop provides small adjustments in the amplifier gain and output voltage.

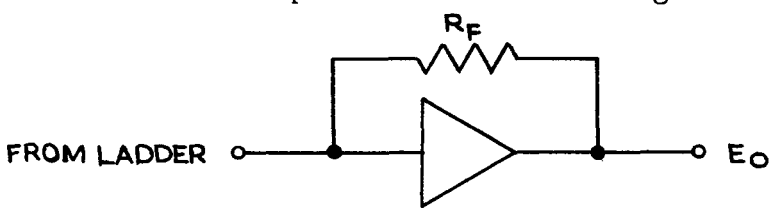
3.2.16.3 DA Ladder Switch

Low V_{sat} transistors are used in the inverted connection to switch the ladder inputs.



3.2.16.4 Output Amplifiers (See Sketch 4)

The ladder output is connected directly to the input of a non-inverting operational amplifier (A 709) which effectively grounds the ladder output. The effective ground at the ladder input allows the following:



$$I_{in} = \frac{Ein}{R_{ladder}}$$

I_{in} flows through R_f since the amplifier input impedance is much larger than R_f. Then $I_{in} = \frac{Eo}{R_f}$ and $Eo = Ein \frac{R_f}{R_{ladder}}$

Maximum ladder output current is given by:

$$T_1 = Iin = \frac{+ E_{ref}}{2R}$$ where R = ladder resistor

then $$\frac{Eo}{R_f} = \frac{E_{ref}}{2R}$$

$$R_f = \frac{Eo\ 2R}{E_{ref}}$$ where Eo is the desired full scale output

The output of the ladder amplifier is routed to an inverting operational amplifier with a gain of approximately 0.3, and then through an emitter follower. The meitter follower is included in the feedback loop to insure stability. A feedback potentiometer allows small gain adjustments.

3.2.17 Power Supplies

Three basic power supplied provide DC power for the various converter circuits. Other voltages are derived from these supplies using zener diode regulators.

3.2.17.1 + 5 Volt Supply

A Dressen Barnes 41-5S, regulated power supply, 5 volts at up to 5 amps is provided for the converter logic. The + 5 volts is wired to a buss located along the "Z" side of the card tray.

POWER CALCULATIONS

5-Volt Micro Logic and Electronics

TYPE	TOTAL NUMBER	MW/UNIT	TOTAL POWER WATTS
950	50	30	1.5
949	96	53	4.9
945	96	50	4.8
944	3	100	.3
933	3	--	--
932	31	100	3.1
μA 710	2	200	.400
		TOTAL	14.6 at 5V

$$I_{\text{Microelectronics}} = \frac{14.6}{5} = 2.92 \text{ amps}$$

I_{lamps} (29 at 60 ma) = 1.74 amps

I input level shifters (19 at 7 ma) = .133 amp

3.2.17.1 Cont'd.

Total 5 Volt Current 4.79 amps

3.2.17.2 + 28 Volt Supply

A Dressen Barnes 20 - 28S power supply provides 28 volts at up to 0.55 amps to the level shifters and to the +12 volt and + 10 volt zener diode regulators.

POWER CALCULATIONS

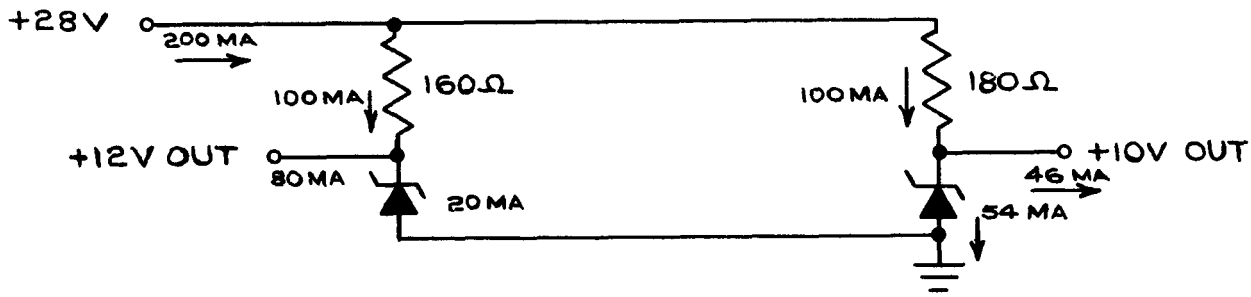
Imax + 12 volt Supply	.100 amp
Imax + 10 volt Supply	.100 amp
Imax output level shifters (19 at 12 ma ea)	.228 amp
Total	.428 amp at 28 volt

3.2.17.3 - 12 Volt Supply

A CEA 6B120Y251 power supply provides -12 volts at up to 0.25 amp to the -12 volt buss located adjacent to the card tray.

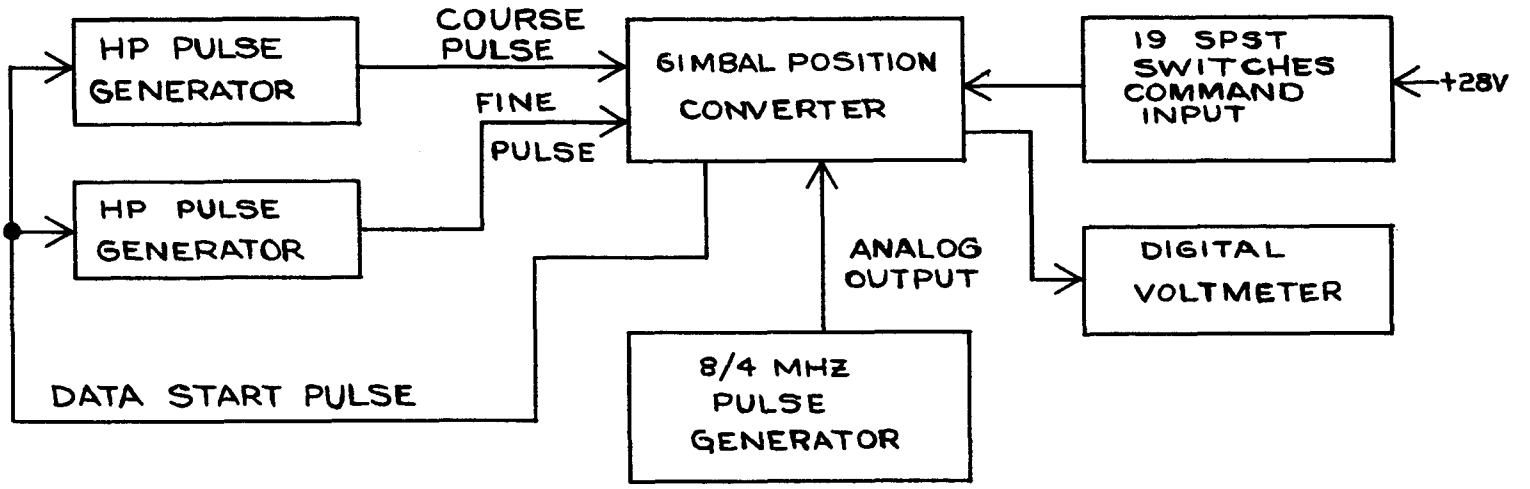
3.2.17.4 Zener Regulators

The +10 and +12 volts are derived from the +28 volt power supply:



4.0 TESTING

System checkout and testing was accomplished using standard laboratory equipment to simulate the converter interface equipment:



Tests were performed as accurately as possible on the Pulse Width Digitizers by varying the generator pulse widths. The clock and coarse and fine pulse widths were correlated to the digitized position display. This test indicated that the digitizers were working properly. However, it was not possible to determine the exact accuracy (should be accurate to within $\pm$ 1 count) due to difficulties in accurately measuring the 8 MHZ clock and regulating the position pulse widths. However, this method of simulating the resolver input pulses does allow a thorough check of the rest of the converter circuits.

4.0 TESTING, Cont'd.

Nineteen SPST switches connected to a 28V supply were used to simulate the command inputs. By using these switches and varying the position input pulse widths the entire 19-bit serial subtractor, complementer and analog outputs may be tested. Table 4.0 "Gimbal Position Converter Analog Output" provides a tabulation of the analog output levels.

GIMBAL POSITION CONVERTER ANALOG OUTPUT

+ ERROR BIT	VOLTAGE	- ERROR BIT	VOLTAGE
0	-.00034	0	-.00034
1	+.01583	1	-.01609
2	+.03195	2	-.03228
3	+.04810	3	-.04843
4	+.06424	4	-.06462
5	+.08040	5	-.08075
6	+.09653	6	-.09693
7	+.11268	7	-.11307
8	+.12875	8	-.12925
9	+.14491	9	-.14529
10	+.16104	10	-.16148
11	+.17720	11	-.17763
12	+.19334	12	-.19382
13	+.20949	13	-.20996
14	+.22562	14	-.22614
15	+.24178	15	-.24228
16	+.25804	16	-.25845
17	+.27420	17	-.27456
18	+.29033	18	-.29075
19	+.30647	19	-.30689
20	+.32261	20	-.32307
21	+.33877	21	-.33922
22	+.35490	22	-.35538
23	+.37107	23	-.37154
24	+.38714	24	-.38771
25	+.40329	25	-.40379
26	+.41942	26	-.41996
27	+.43559	27	-.43611
28	+.45172	28	-.45226
29	+.46789	29	-.46841
30	+.48403	30	-.48449
31	+.50018	31	-.50063

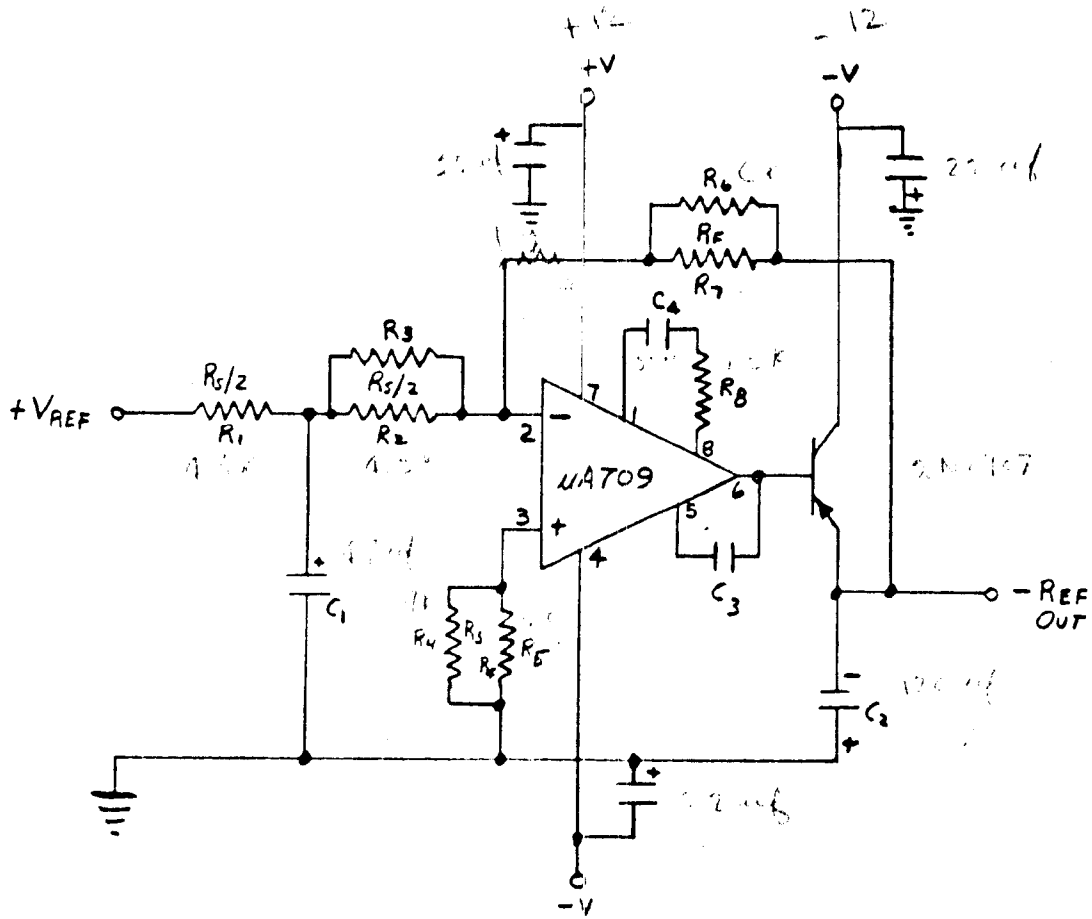
TABLE 4.0

5.0 CONCLUSIONS

We believe that we have designed and manufactured the Gimbal Position Converter Prototype to be a quality instrument of very high reliability. Our quality and reliability programs have been utilized fully during all design, manufacturing and testing phases. However, as is the case with most prototype systems, working with the completed system points out some areas of over design resulting in unnecessary system complexity. Simplification of these areas would decrease the number of system circuits and components, thus the overall system reliability could be enhanced. Several such areas have already been noted. For example, the strobe generator could be simplified by relocating the outputs thus eliminating six flip-flops from the generator circuitry. The subtractor gating could be simplified to reduce the number of NAND gates by four. At the expense of approximately twenty additional microseconds of calculation time for negative numbers, a "twos" complement of the 19 bit subtractor difference may be made. (End around carry addition) This will eliminate the 1 bit error in the indicated difference and will also greatly simplify the complementer and output gating.

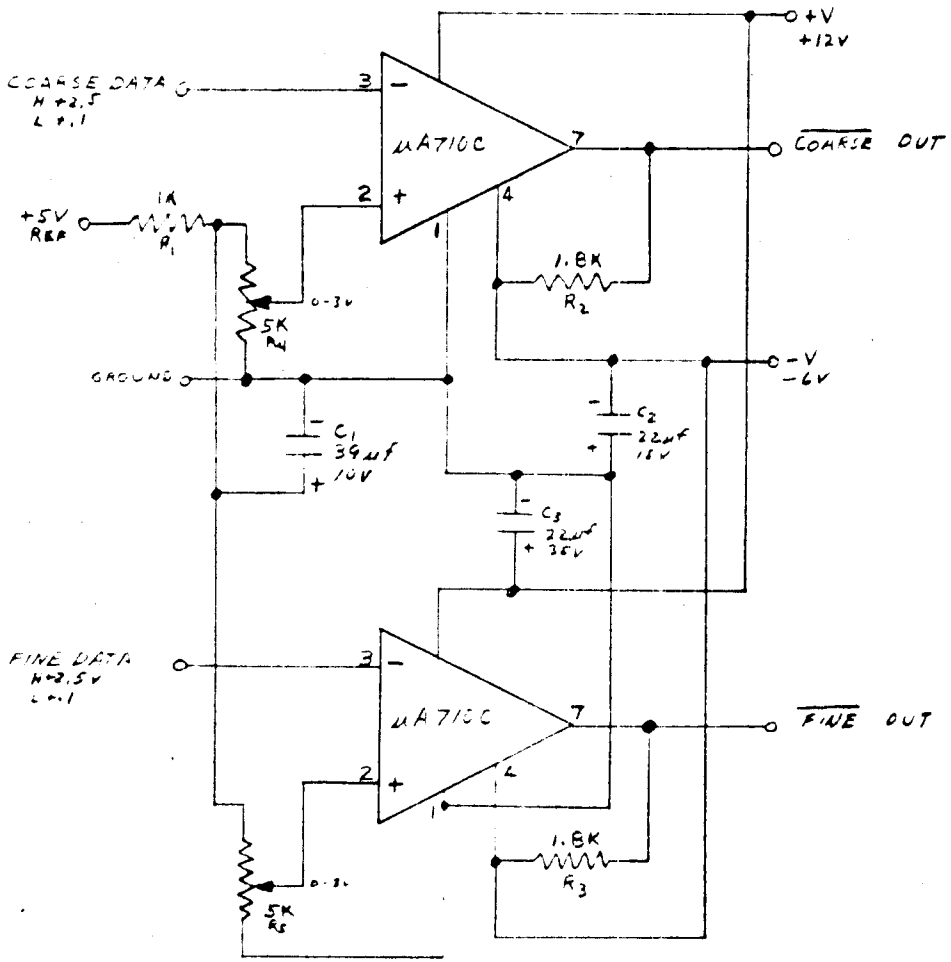
5.0 CONCLUSIONS, Cont'd.

We suggest that for any future models of the converter, tester be designed and fabricated which will accurately generate the 8 and 4 MHZ clocks and simultaneously simulate the resolver output pulse widths. This would allow full range accuracy checks of the digitizers along with checks on the performance of the rest of the system.



INVERTING REFERENCE REGULATOR
SKETCH #1

10-6-66



NOTE: R_1 - 1K 1% PRECISION

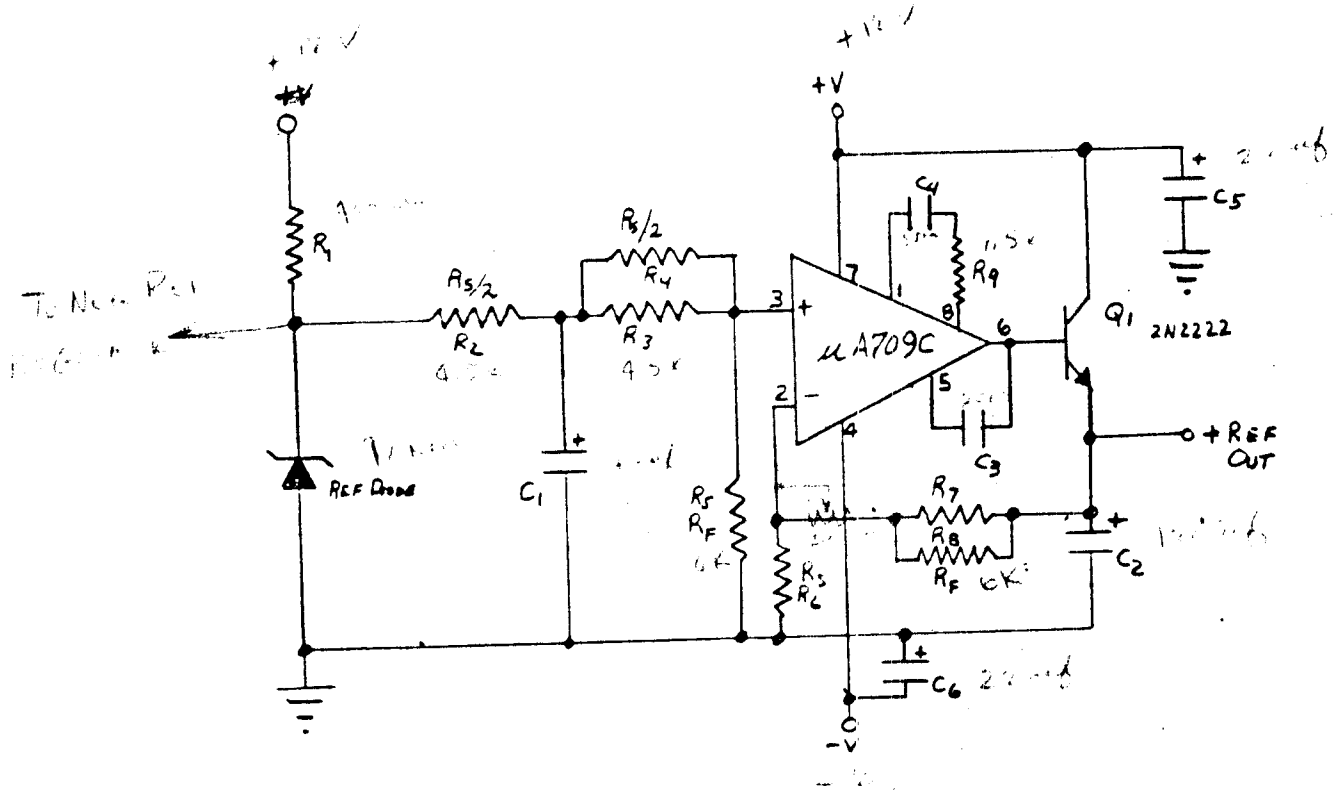
R_2, R_3 - 1.8K 1/8W 5% CARBON

R_4, R_5 - 5K 20 TURN LOW TEMP COEF WW 1/10W

INVERTING INPUT COMPARATORS

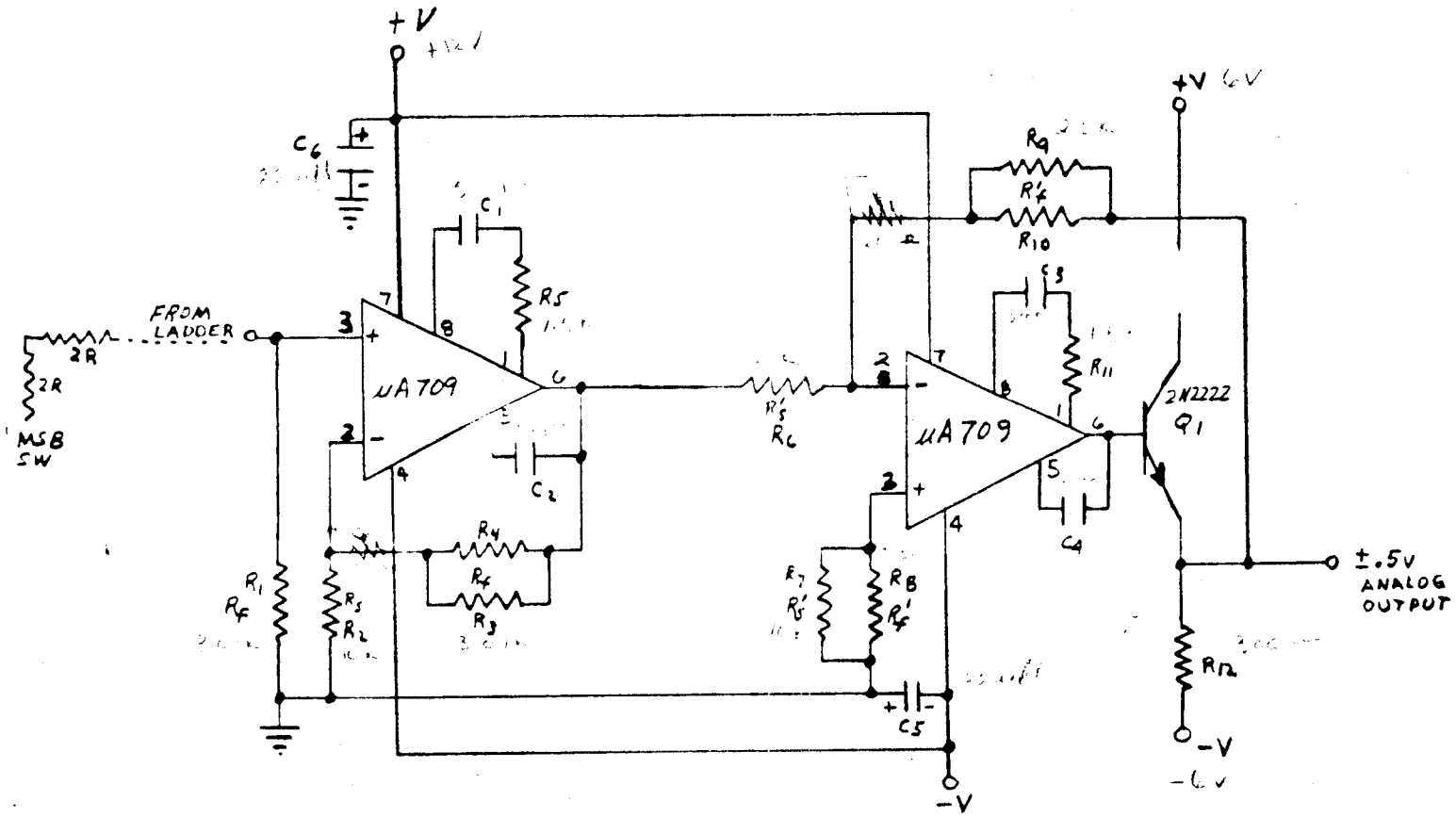
SKETCH #2

10-7-66 [illegible]



NON-INVERTING REFERENCE REGULATOR
SKETCH #3

10-6-66



DA LADDER AMPLIFIER AND OUTPUT DRIVER

SKETCH # 4

10-6-66

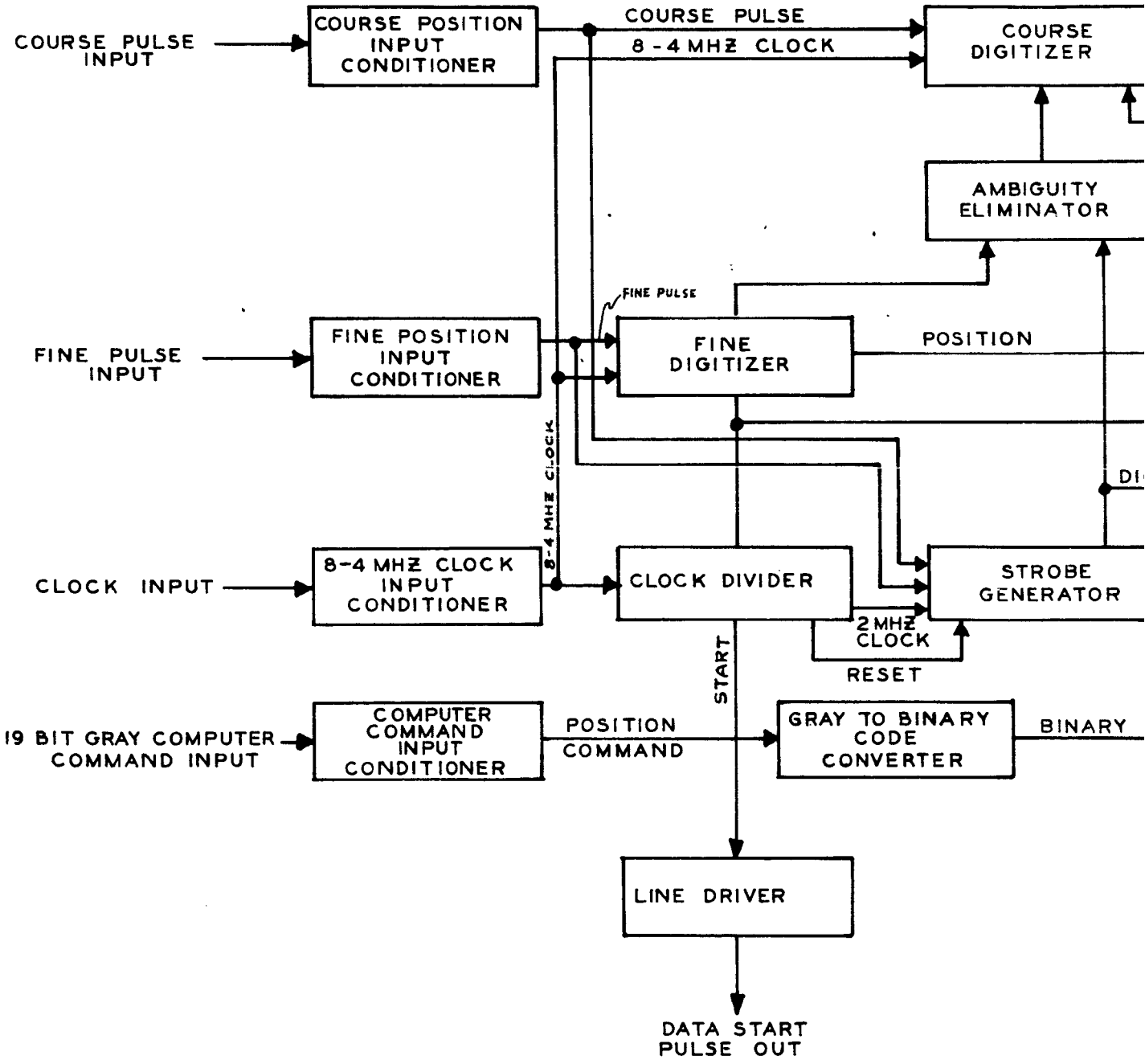
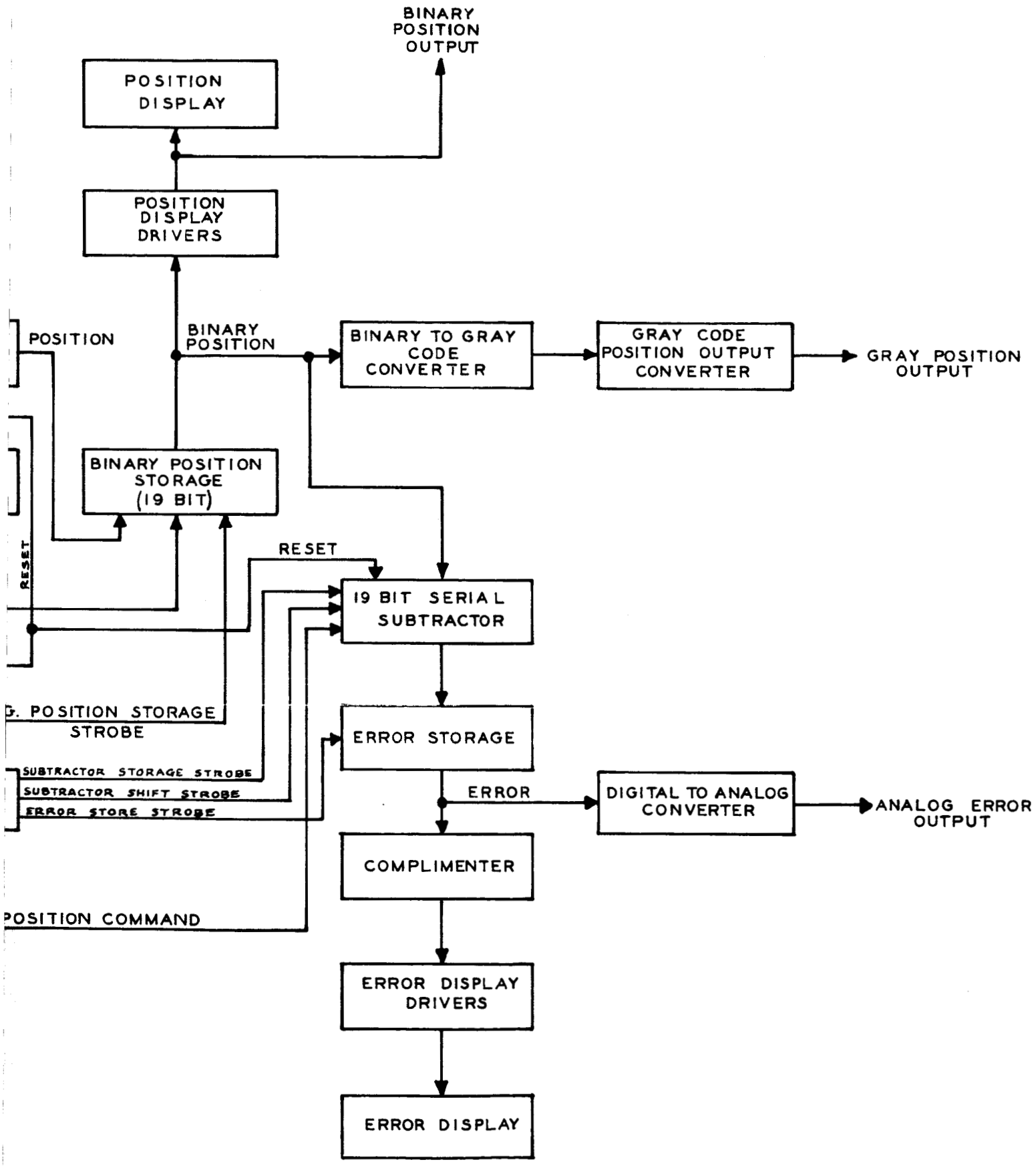

COURSE PULSE INPUT
COURSE POSITION INPUT CONDITIONER
COURSE PULSE
8-4 MHZ CLOCK
COURSE DIGITIZER
AMBIGUITY ELIMINATOR
FINE PULSE
FINE PULSE INPUT
FINE POSITION INPUT CONDITIONER
FINE DIGITIZER
POSITION
8-4 MHZ CLOCK
CLOCK INPUT
8-4 MHZ CLOCK INPUT CONDITIONER
CLOCK DIVIDER
STROBE GENERATOR
2 MHZ CLOCK
RESET
START
19 BIT GRAY COMPUTER COMMAND INPUT
COMPUTER COMMAND INPUT CONDITIONER
POSITION COMMAND
GRAY TO BINARY CODE CONVERTER
BINARY
LINE DRIVER
DATA START PULSE OUT

Fig-1-A



GIMBAL POSITION CONVERTER
BLOCK DIAGRAM
FIG. 1-8

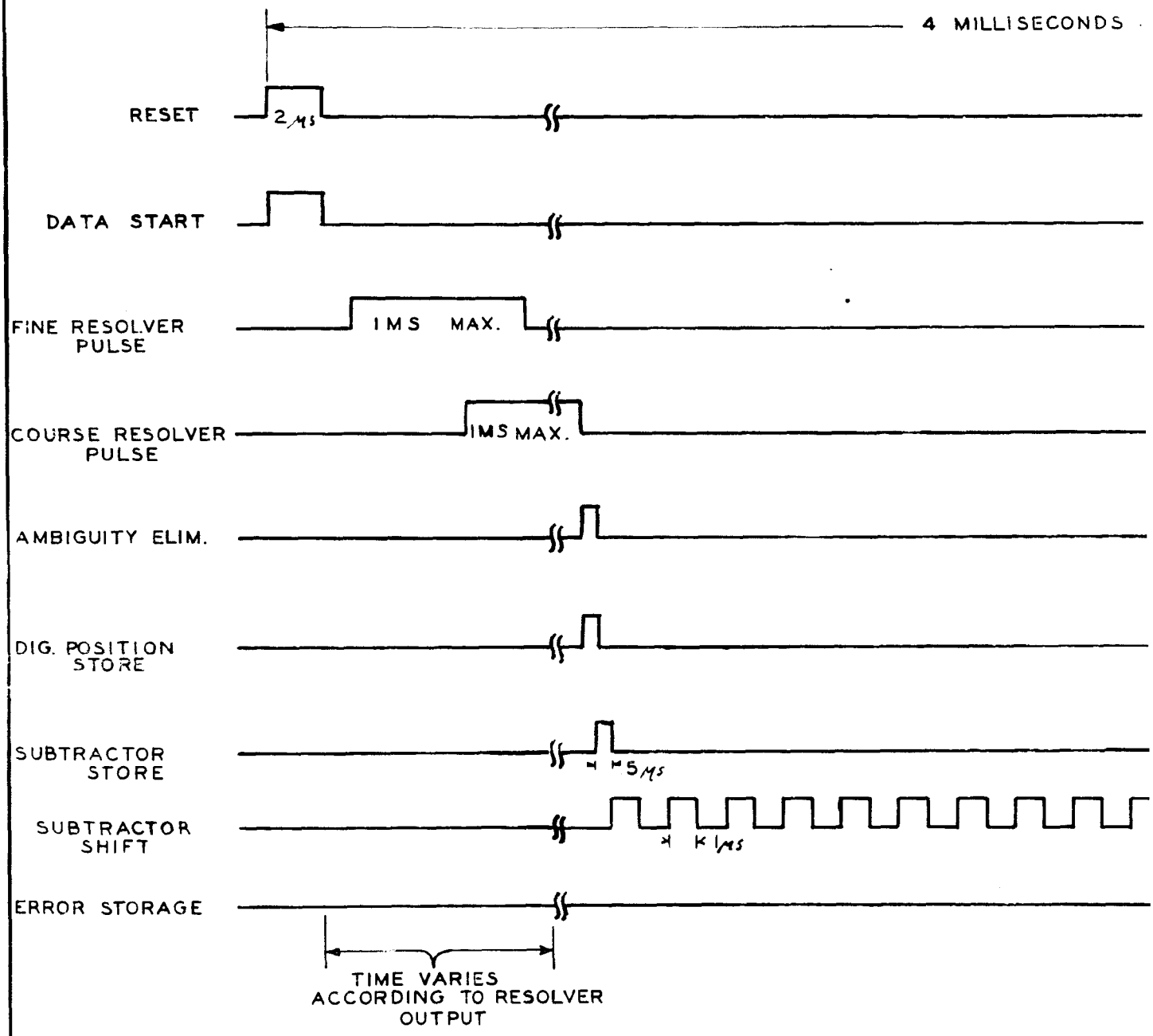
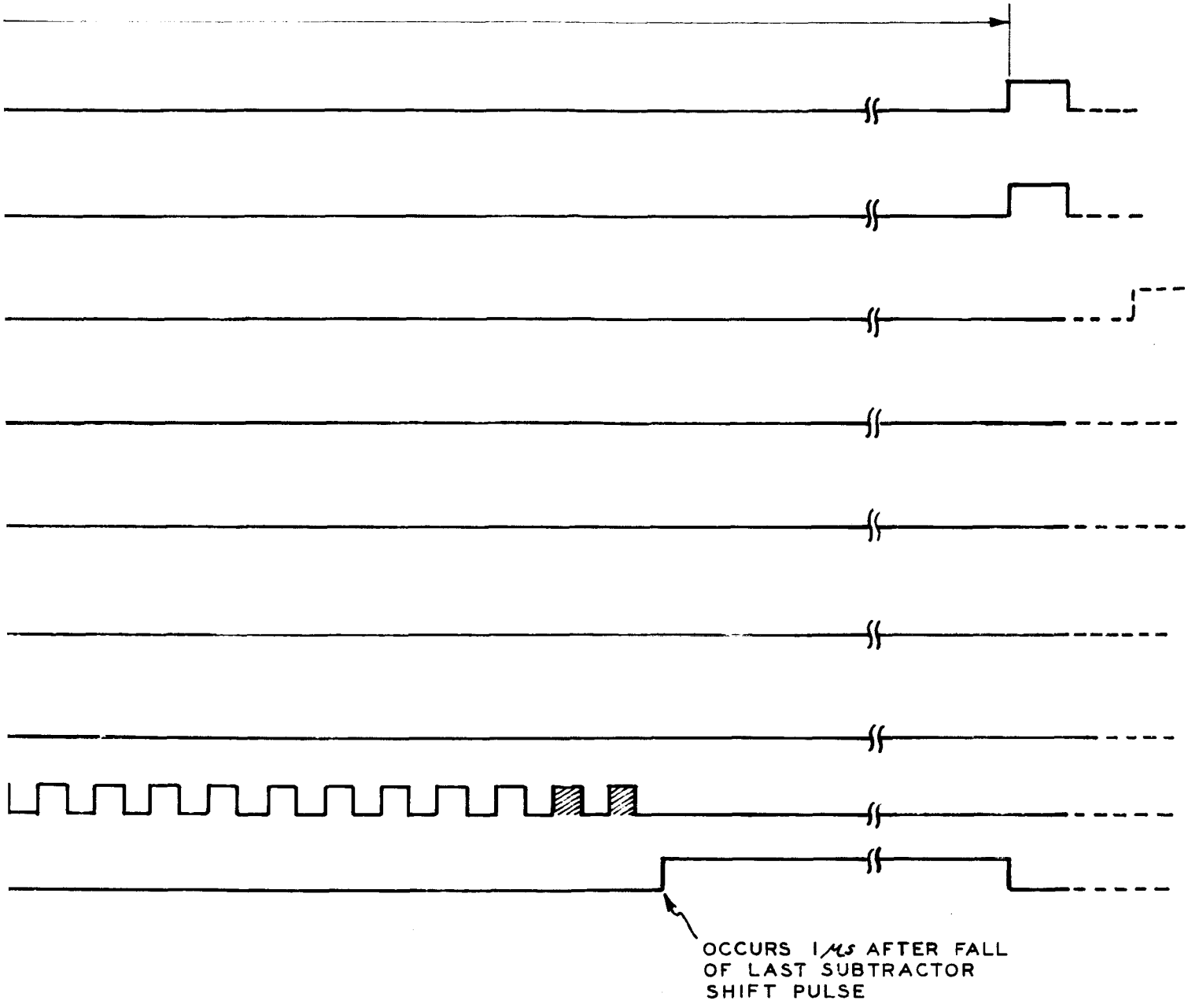

4 MILLISECONDS
RESET
2 μs
DATA START
FINE RESOLVER PULSE
IMS MAX.
COURSE RESOLVER PULSE
IMS MAX.
AMBIGUITY ELIM.
DIG. POSITION STORE
SUBTRACTOR STORE
5 μs
SUBTRACTOR SHIFT
1 μs
ERROR STORAGE
TIME VARIES ACCORDING TO RESOLVER OUTPUT

Fig. 2-A



SHADED SHIFT PULSES ARE GATED OUT IN HIGH RESOLUTION MODE -
IN LOW RESOLUTION MODE THEY SHIFT THE DATA TWO BITS TO THE RIGHT TO REPLACE THE TWO MISSING LSB'S.

GIMBAL POSITION CONVERTER
TIMING DIAGRAM

FIG. 2-B