RE-ORDER NO. 67-493

Final Report

R.F. TEST CONSOLE

Contract No. 951140

Date: 10 May 1967

Prepared For: Jet Propulsion Laboratory
4800 Oak Grove Dr.
Pasadena, California

Prepared by: Westinghouse Electric Corp.
Surface Division
P. O. Box 1897
Baltimore, Md. 21207

MDE 2591

FOREWORD

The enclosed report is a technical summary of the R. F. Test Console Design and test completed for the Jet Propulsion Laboratory on contract 951140. This report covers the work performed in the period from July 1965 through January 1967. The objective of the Phase II program was to design, fabricate and test the PM/AM Sub-System and the FM/AM Sub-System as outlined in the Phase I final report (Jet Propulsion Laboratory Contract 950144). The work has been completed and the results achieved meet the specifications outlined at the termination of the Phase I program except the FM Transmitter/Receiver pair residual FM spec. and the PM Modulator bandwidth spec.

Each portion of the work is documented in this report and Appendices A through D. Appendix A is included in this volume. However, Appendices B, C and D are submitted as separate documents.

The following individuals were the principal contributors to this program:

Kenneth Peterson
George Vaughan
Roger Ubben
M. Driscoll
Chris Vale
Ray Parrack
Les Edwards

Written by G.R. Vaughan
G.R. Vaughan
Fellow Engr.

Approved by C. D. Hedges
C.D. Hedges
Manager

Approved by G. L. Henry
G.L. Henry
Supvr. Engr.

ACKNOWLEDGEMENT

The contributors to this program acknowledge the technical contributions and encouragement offered by the Jet Propulsion Laboratory throughout the course of this program. In particular, the technical contributions of the Cognizant Engineer, Francis Charles, were valuable in the design of the Phase Lock Phase Modulator and test of the PM and FM Receivers' Phase Lock Demodulators. Further, the assistance given by the Jet Propulsion Laboratory in procuring state-of-the-art test equipment and components proved very helpful.

TABLE OF CONTENTS

Section		Page
1.0	INTRODUCTION	1-1
1.1	Program Goals	1-1
1.2	Summary And Conclusions	1-1
2.0	GENERAL DESCRIPTION AND DESIGN PLAN	2-1
2.1	System	2-1
2.2	Frequency Synthesizers	2-1
2.2.1	Transmitter Synthesizer Design Plan	2-6
2.2.2	Receiver Synthesizer Design Plan	2-6
2.3	P.M. Subsystem	2-8
2.3.1	P.M. Modulator Design Plan	2-11
2.3.2	P.M. Receiver Design Plan	2-12
2.4	F.M. Subsystem	2-17
2.4.1	F.M. Transmitter Deeign Plan	2-10
2.4.2	F. M. Receiver Deeign Plan	2-21
2.5	Linear S/N Summer	2-25
2.6	Phase Noise And Test Instrumentation	2-27
3.0	TECHNICAL DESCRIPTION AND CORRELATION OF DESIGN PLAN AND PERFORMANCE	3-1
3.1	Frequency Synthesizers	3-1
3.1.1	Transmitter Frequency Synthesieer	3-1
3.1.1.1	Transmitter Frequency Synthesizer Module Design	3-2
3.1.1.2	Test Results.	3-11
3.1.2	Receiver Frequency Synthesizer	3-12
3.1.2.1	Receiver Frequency Synthesizer Module Deeign	3-13
3.1.2.2	Test Results	3-13
3.2	P.M. Subsystem	3-14
3.2.1	P.M. Modulator	3-19
3.2.1.1	Theoretical Considerations	3-23
3.2.1.2	Modulator Design and Test Results	3-24

Section		Page
3.2.1.3	Module Design	3-38
3.2.2	P. M. Receiver	3-44
3.2.2.1	Input Amplifier (code 207)	3-44
3.2.2.2	Balanced Modulators (Mixers)	3-47
3.2.2.3	Narrow Band IF (code 206)	3-55
3.2.2.4	Wideband IF (Code 214)	3-55
3.2.2.5	Wideband Phase Detector (Code 203A and 203)	3-60
3.2.2.6	Carrier Tracking Loop	3-60
3.2.2.7	AGC Loop	3-65
3.2.2.8	Feedback Pair	3-67
3.3	F.M. Subsystem	3-80
3.3.1	F.M. Modulator	3-86
3.3.1.1	F.M. Modulator Components	3-95
3.3.2	F.M. Receiver	3-95
3.3.2.1	Phase Lock Discriminator AFC Loop	3-95
3.3.2.2	Phase Lock Discriminator APC Loop	3-99
3.3.2.3	Module Design	3-103
3.3.2.3.1	Input Filter and Amplifier	3-103
3.3.2.3.2	Limiter	3-105
3.3.2.3.3	Phase Detector	3-106
3.3.2.3.4	Discriminator	3-107
3.3.2.3.5	Phase Lock Discriminator VCO	3-111
3.3.2.3.6	F.M. Receiver Operational Amplifier	3-112
3.3.2.4	Test Results	3-112
3.4	Linear S/N Summer	3-112
3.5	Phase Noise and Test Instrumentation	3-149

Appendix	Title	
A	Specification	Enclosed in this Report
B	Filter Design and Performance	Separate Document
C	Operators Manual	Separate Document
D	Maintenance Data	Separate Document

LIST OF ILLUSTRATIONS

Figure		Page
2.2.1	Functional Block Diagram R. F. Test Console	2-3
2.2.1.1	Block Diagram. Transmitter Frequency Synthesizer	2-5
2.2.2.1	Block Diagram. Receiver Frequency Synthesizer	2-7
2.3.1	P. M. Subsystem	2-9
2.3.1.1	Black Diagram. P. M. Modulator	2-11
2.3.2.1	Block Diagram. P.M. Receiver	2-13
2.4.1	Block Magram. Basic F.M. Subsystem VCO	2-18
2.4.1.1	Block Diagram F.M. Transmitter	2-20
2.4.2.1	Block Magram F.M. Receiver	2-23
2.5.1	Block Magram Signal/Noise Summer	2-26
2.6.1	Block Diagram Phase Noise Instrumentation	2-28
3.1.1.1.1	Oscillator Characteristic $\frac{\Delta f}{f}$ vs τ	3-4
3.1.1.1.2	Simplified Clapp Oscillator	3-5
3.1.1.1.3	Equivalent Circuit of Crystal and Sustaining Circuit	3-6
3.1.1.1.4	Simplified Diagram of Oscillator and AGC System	3-7
3.1.1.1.5	Simplified Reference Oscillator	3-7
3.1.1.1.6	Frequency Multiplier Coupling Circuit	3-9
3.1.1.1.7	Step Recovery Diode Frequency Multiplier Waveforms	3-10
3.2.1	P.M. Subsystem Frequency Stability Test System	3-15
3.2.2	Frequency Stability Test Results (1 Minute)	3-16
3.a.3	Frequency Stability Test Results (4 hours)	3-17
3.2.4	P.M. Subsystem Phase stability Test System	3-18
3.2.5	P.M. Subsystem Phase stability Test Results.	3-20
3.2.6	P.M. Subsystem Fidelity Test System	3-21
3.2.7	P.M. Subsystem Fidelity Test System Tone Generator Characteristics	3-22
3.2.1.1	Simplified Block Diagram. Locked Oscillator Phase Modulator	3-23
3.2.1.2	Linear Phase Model. Locked Oscillator Phase Modulator	3-24
3.2.1.3	Root Locus Diagram 3 Pole Butterworth Synthesis	3-25
3.2.1.4	Root Locus Diagram 4 Pole Butterworth Syntheseis	3-27
3.2.1.5	Linearized Phase Model With Transport Lag	3-28
3.2.1.6	4 Pole Response With Time Delay ($T_1 + T_2$)	3-30

Figure		Page
3.2.1.7	3 Pole Response With Time Delay ($T_1 + T_2$)	3-31
3.2.1.2.1	Normalized Loop Filter. 3 Pole Butterworth Synthesis	3-33
3.2.1.2.2	Closed Loop Response. 200 KC/s Bandwidth. 3 Pole Butterworth	3-34
3.2.1.2.3	Closed Loop Response. 500 KC Bandwidth. 3 Pole Butterworth	3-35
3.2.1.2.4	Closed Loop Response. 4 Pole Butterworth	3-37
3.2.1.2.5	P.M. Transmitter Phase Deviation Test System	3-38
3.2.1.3.1	Two Port Network	3-39
3.2.1.3.2	Transistor Common Base Two Port Model	3-39
3.2.1.3.3	Basic Oscillator Circuit	3-40
3.2.1.3.4	Circuit Diagram 400 MC/s VCO	3-41
3.2.1.3.5	400 MC/s VCO Characteristic	3-42
3.2.1.3.2.1	P.M. Modulator Counter Logic	3-44
3.2.1.3.2.2	P.M. Modulator Phase Detector Characteristic	3-45
3.2.1.3.2.3	Block Diagram Burr-Brown Model 1510 Operational Amplifier	3-46
3.2.2.1	Input Amplifier Noise Figure Considerations	3-47
3.2.2.2	Amplitude Response Input Amplifier (I_c = 0)	3-48
3.2.2.3	Phase Response Input Amplifier (I_c = 0)	3-49
3.2.2.4	Amplitude Response Input Amplifier (I_c = 0.85 ma)	3-50
3.2.2.5	Phase Response Input Amplifier (I_c = 0.85 ma)	3-51
3.2.2.6	Amplitude Response Input Amplifier (I_c = 4.0 ma)	3-52
3.2.2.7	Phase Response Input Amplifier (I_c = 4.0 ma)	3-53
3.2.2.8	Input Amplifier AGC Range VS Control Current and Noise Figure VS Control Current	3-54
3.2.2.9	Balanced Mixer Characteristics	3-56
3.2.2.10	P.M. Rx Narrow Band IF Amplitude and Phase Response	3-57
3.2.2.11	P.M. Rx Wideband IF Amplitude Response	3-58
3.2.2.12	P.M. Rx Wideband IF Phase Response	3-59
3.2.2.13	PM Rx Demod Channel Phase Detector Amplitude characteristic (5 Mc/s Filter)	3-61
3.2.2.14	PM Rx Demod Channel Phase Detector Amplitude Characteristic (2 MC/s Filter)	3-62
3.2.2.15	P.M. Rx Demod. Channel Phase Detector Dynamic Range	3-63
3.2.2.16	P.M. Rx Carrier Tracking Loop Gain Test System	3-64
3.2.2.17	P.M. Rx Carrier Tracking Loop Design	3-66
3.2.2.18	P.M. Rx Carrier Tracking Loop Parameters	3-67

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
3.2.2.19	P.M. Rx Carrier Tracking Loop Bandwidth Test Derivation	3-68
3.2.2.20	P.M. Rx Carrier Tracking Loop Bandwidth Test System	3-69
3.2.2.21	P.M. Rx Carrier Tracking Loop XTAL VCO Characteristic (Uncorrected)	3-70
3.2.2.22	P.M. Rx Carrier Tracking Loop VCO Linearity Characteristic	3-71
3.2.2.23	AGC Loop Test System	3-72
3.2.2.24	AGC Loop Design Summary	3-73
3.2.2.25	P.M. Rx AGC Loop Bandwidth Test System	3-74
3.2.2.26	P.M. Rx AGC Loop Bandwidth Plots	3-75
3.2.2.27	P.M. Rx Predetection Playback and Record	3-76
3.2.2.28	Feedback Pair Characteristics	3-77
3.2.2.29	Feedback Fair Root Locus	3-78
3.2.2.30	Amplitude Response of 3 Cascaded Feedback Pairs	3-79
3.3.1	F.M. Subsystem Residual F.M. Test	3-82
3.3.2	F.M. Subsystem Static Linearity Phase Lock Receiver	3-83
3.3.3	F.M. Subsystem Static Linearity Conventional Discriminator	3-84
3.3.4	F.M. Subsystem Dynamic Linearity	3-85
3.3.1.1	Linear Frequency Model F.M. Transmitter, Major Loop	3-86
3.3.1.2	Root Locus Diagram F.M. Modulator, Major Loop	3-87
3.3.1.3	F.M. Modulator Response	3-89
3.3.1.4	Linear Frequency Model with Simulated VCO Input	3-90
3.3.1.5	Bode Magram, VCO Correction	3-91
3.3.1.6	Linear Phase Model, F.M. Modulator Carrier Stabilization Loop	3-91
3.3.1.7	F.M. Modulator Low Frequency Response Compensated for Carrier Stabilization Loop	3-93
3.3.1.8	VCO Static Characteristics	3-96
3.3.2.1	Bode Diagram VCO Correction F.M. Phase Lock Discriminator	3-99
3.3.2.2	Block Magram, Phaee Lock Discriminator	3-100
3.3.2.3	Phase Lock Discriminator Linearized Model	3-100
3.3.2.4	Low Noise Amplifier Input Circuit	3-104
3.3.2.5	Basic R F. Test Console Limiter Circuit	3-105
3.3.2.6	R F. Test Console Limiter Configuration	3-106
3.3.2.7	Basic R. F. Test Console Phase Detector	3-107
3.3.2.8	Simplified Schematic Diagram R F. Test Console Phase Detector	3-108

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
3.3.2.9	Conventional Discriminator	3-108
3.3.2.10	Delay Line Frequency Discriminator	3-110
3.3.2.11	Delay Line Phase Characteristic	3-110
3.3.2.12	F.M. Receiver Input Amplifier Phase and Amplitude Response (10KC B.W.)	3-113
3.3.2.13	F.M. Receiver Input Amplifier Phase and Amplitude Response (200 KC B.W.)	3-114
3.3.2.14	F.M. Receiver Input Amplifier Phase and Amplitude Response (1MC B.W.)	3-115
3.3.2.15	F.M. Receiver Limiter Characteristic (Code 408)	3-116
3.3.2.16	F.M. Receiver Limiter Characteristic (Code 409)	3-117
3.3.2.17	Phase Lock Discriminator Phase Detector Characteristic	3-118
3.3.2.18	Phase Lock Discriminator VCO Characteristic (Closed Loop)	3-119
3.3.2.19	F.M Receiver APC Loop Gain Test Set	3-120
3.3.2.20	F.M. Receiver APC Loop Bandwidth Test Set	3-121
3.3.2.21	F.M. Receiver Phase Lock Discriminator Amplitude Response (fo = 3 Kc)	3-122
3.3.2.22	F.M. Receiver Phase Lock Discriminator Amplitude Response (fo = 30 KC)	3-123
3.3.2.23	F.M. Receiver Phase Lock Discriminator Amplitude Response (fo = 300 KC)	3-124
3.3.2.24	F.M. Receiver Output Filter, Attenuation Response, Butterworth, 1 KC	3-125
3.3.2.25	F.M. Receiver Output Filter, Phase Response, Butterworth. 1KC	3-126
3.3.2.26	F.M. Receiver Output Filter, Attenuation Response, Butterworth, 10 KC	3-127
3.3.2.27	F.M. Receiver Output Filter, Phase Response. Butterworth, lOKC	3-128
3.3.2.28	F.M. Receiver Output Filter, Attenuation Response, Butterworth, lOOKC	3-129
3.3.2.29	F.M. Receiver Output Filter, Phase Response, Butterworth, lOOKC	3-130
3.3.2.30	F.M. Receiver Output Filter, Attenuation Response, Bessel 1KC	3-131
3.3.2.31	F.M. Receiver Output Filter, Phase Response, Bessel 1KC	3-132
3.3.2.32	F.M. Receiver Output Filter, Attenuation Response, Bessel lOKC	3-133
3.3.2.33	F.M. Receiver Output Filter, Phase Response, Bessel, 10KC	3-134
3.3.2.34	F.M Receiver Output Filter, Attenuation Response, Bessel lOOKC	3-135
3.3.2.35	F.M. Receiver Output Filter, Phase Response, Bessel, lOOKC	3-136

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
3.4.1	Noise Amplifier Characteristics as a Function of Bias Voltage	3-138
3.4.2	Power Transfer of Noise Amp./Filter Taken at 39.5°C oven Temperature	3-139
3.4.3	Block Diagram. Test Set. Noise Amp. Frequency Response	3-140
3.4.4	Noise Amp. Pass Band. AGC. (0 Volts)	3-141
3.4.5	Noise Amp. Pass Band. AGC. (0.5 Volts)	3-142
3.4.6	Noise Amp. Pass Band. AGC. (0.7 Volts)	3-143
3.4.7	Noise Amp. Pass Band. AGC. (0.9 Volts)	3-144
3.4.8	Noise Amp. Freq. Response. AGC. (1.0 Volts)	3-145
3.4.9	Summer Noise Power Output for Various "Bias Dial Settings"	3-146
3.4.10	Block Diagram. Test Set. 10 KC Noise Filter Freq. Response	3-147
3.4.11	10KC Noise Filter Frequency Response	3-148
3.5.1	Phase Detector Characteristics. Phase Noise Instrumentation	3-150
3.5.2	Carrier Suppression Measurement System	3-151

LIST OF TABLES

Table		Page
2.3.1	P.M. Subsystem Principal Specifications	2-10
2.3.1.1	P.M. Modulator Principal Specifications	2-11
2.3.2.1	P.M. Receiver Principal Specifications	2-14
2.4.1	F.M. Subsystem Principal Specifications	2-17
2.4.1.1	F.M. Transmitter Principal Specifications	2-19
2.4.2.1	F.M. Receiver Principal Specifications.	2-21
2.5.1	Signal/Noise Summer Specifications	2-25
3.1.1.2.1	Transmitter/Receiver Oscillator Stability Test Data	3-11
3.1.1.2.2	Transmitter Frequency Synthesizer Multipliers Relative Spurious Levels	3-12
3.3.1.1	F.M. Modulator Nomenclature	3-94
3.3.2.1	F.M. Receiver AFC Loop Nomenclature	3-97

1.0 INTRODUCTION

The Radio Frequency Test Console is a precision Simulator whereby the characteristics of a deep space communications system are realistically simulated. The unit is a laboratory device designed to evaluate advanced telemetry and ranging systems.

The Simulator duplicates the characteristics of a spacecraft transmitter, the ground receiver and the transmission media. The PM/AM Subsystem includes a PM/AM transmitter, PM receiver and coherent AM receiver. The FM Subsystem consists of an FM transmitter, Phase Lock FM receiver and conventional FM discriminator. The Signal-to-Noise Summer establishes accurate signal-to-noise ratios over a dynamic range of 100 db. The Phase Noise Instrumentation feature provides a means of measuring the phase noise of the PM receiver carrier tracking loop VCO at various signal-to-noise ratios. Auxiliary test instruments provide a means of accurately measuring carrier suppression as a function of modulation index. The RF Test Console also includes various commercial instruments required to measure both baseband and RF signal parameters.

1.1 PROGRAM GOALS

The Phase II program goals are stated simply as follows: "Design, fabricate and test an RF Test Console as outlined in Appendices A through K of the Phase I Final Report". The hardware that was designed and fabricated in Phase II correlates quite closely with the design plans outlined in the Phase I Final Report.

1.2 SUMMARY AND CONCLUSIONS

The RF Test Console test results indicate that the specifications outlined in Appendix A of the Phase I Final Report were met with the following exceptions:

1.2.1. PM MODULATOR

The PM Modulator response was specified to exhibit a transfer of output phase deviation to input baseband within ±0.5 db from DC to 1.5 Mc. The modulator design achieved ±0.5 db from DC to 1.0 Mc. The modulator was designed as a wideband phase lock loop. The loop transport lag introduced peaking (as predicted in the Phase I study) near the loop cut frequency. The loop transport lag was minimized but not sufficiently to meet the specifications as originally stated.

1.2.2. FM TRANSMITTER/RECEIVER PAIR RESIDUAL FM

The FM Subsystem Residual FM characteristic was specified to exhibit 15 cps RMS residual FM with the transmitter operating in the AFC mode and 60 cps

RMS residual FM in the NON/AFC mode or conventional receiver. The FM Subsystem exhibited 170 cps residual FM with the transmitter in the Non AFC mode measured with the phase lock receiver and 211 cps measured with the conventional receiver. The Subsystem exhibited 165 cps residual FM with the transmitter in the AFC mode measured with the phase lock receiver and 195 cps measured with the conventional receiver. All measurements were made in a 500 Kc bandwidth. The transmitter AFC system reduced the residual FM considerably when the measurements were made in a narrow bandwidth (100 Kc); however, as noted the system residual FM is essentially the same (measured in 500 Kc) with the transmitter in AFC or Non AFC.

During the course of the Phase II design effort it became evident that a trade off existed between system linearity and residual FM. Initially, the system exceeded the linearity spec. and exhibited poor residual FM characteristics. Subsequently, the residual FM was reduced at the expense of linearity; however, the original residual FM specification was not met as noted. The conclusion reached (after the design and test program was concluded) is that the original specification is unrealistic. It is unrealistic in the sense that the residual FM is measured in too wide a bandwidth.

1.2.3 MISCELLANEOUS

The Phase Noise Instrumentation system was modified from that outlined in the original design plan. The modification became evident with the availability of the Hewlett Packard Vector Voltmeter Model 840A. This instrument reconstructs repetitive waveforms in the 1 Mc to 1 Gc band by a sampling technique. The waveforms are reconstructed at 20 Kc; however, the phase and amplitude information is retained as dictated by the Nyquist sampling rate. This instrument is used in the RF Test Console to reconstruct both the PM Receiver carrier tracking loop VCO output and the loop reference. The resulting 20 Kc waveforms are linearily phase compared to yield a measure of the VCO jitter and cycle slippage at threshold. The obvious advantage is that the 10 Mc phase measurement is made at 20 Kc.

1.2.4 PM SUBSYSTEM PHASE STABILITY

The PM Transmitter/Receiver Pair Phase Stability was specified as 1.0 degree RMS measured in 2 BLo of 3.0 cps. The system yielded 0.25 degrees RMS in 2 BLo of 3.0 cps. Further, the phase stability spec. was exceeded with both a DC amplifier and Non Linear Diode Function Generator (and associated 1/f noise) inside the loop. The latter units were required to meet loop gain and linearity specifications. However, the PM Subsystem phase stability can be decreased from 0.25 degrees RMS at the expense of loop gain and linearity.

2.0 GENERAL DESCRIPTION AND DESIGN PLAN

The organization of this report is outlined as follows:

Section 2 includes the principal subsystem specifications and a brief review of the design plan formulated in the Phase I program, Changes from the design plan are outlined and the reasons for the deviations are listed.

Section 3 is the main body of the report, In this section the design and test results are correlated with the design plan and specification. Section 3 includes loop design details and module designs that are considered to be of interest. Conventional module designs are not included. Appendix A (Specification) is included as the last portion of this volume. Appendix A includes a correlation of the original specification and measured data.

2.1 SYSTEM

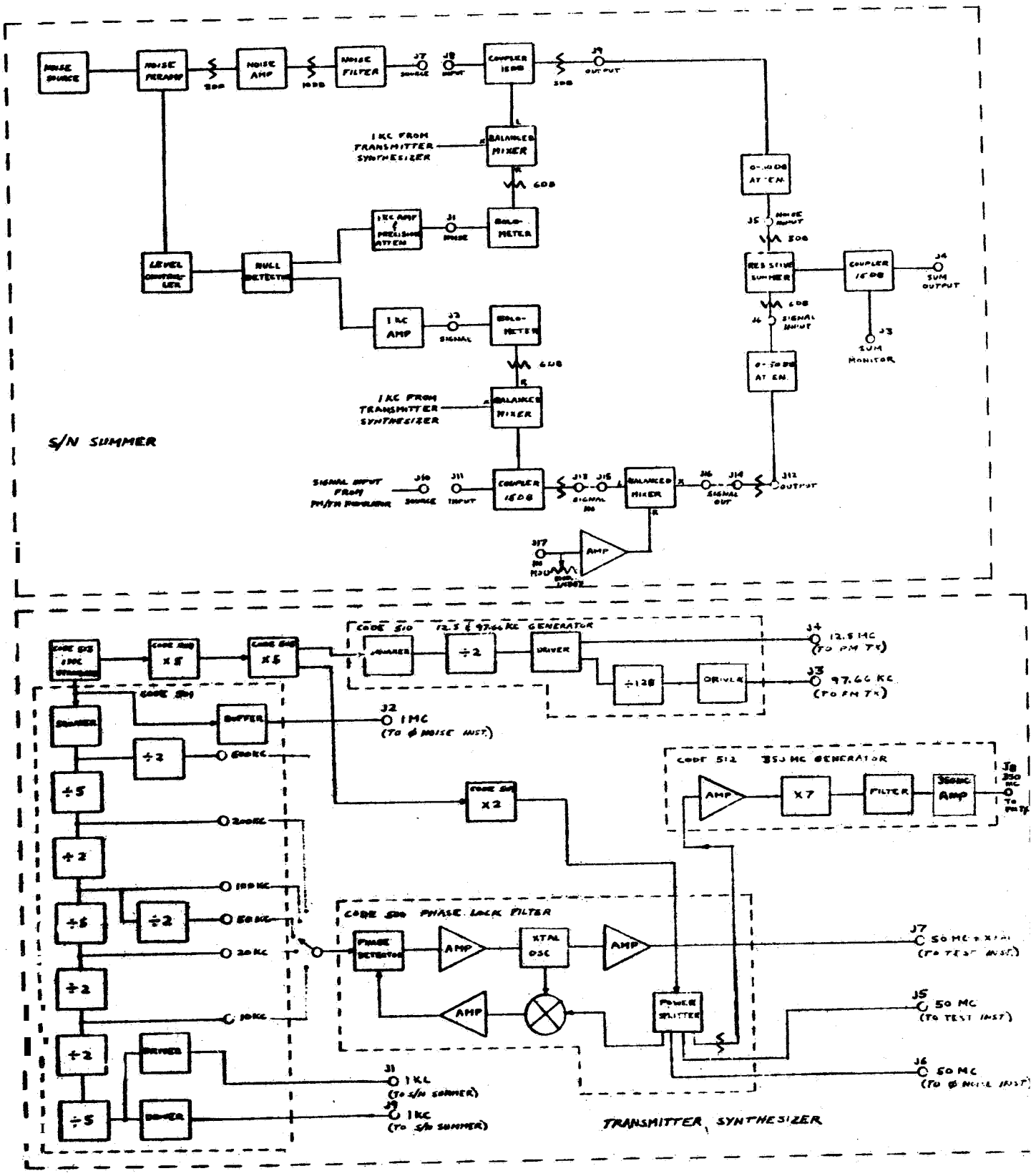
Figure 2.1.1 presents a block diagram of the R. F. Test Console. The system is packaged in four Holloway Cabinets. One cabinet includes the P. M., F. M. Transmitter Test Equipment and Transmitter Frequency Synthesizer. The Linear/Signal to Noise Summer is included in a second cabinet, The Commercial Test Equipment is packaged in a third cabinet and the P. M. /F, M. Receivers and Receive Frequency Synthesizer are packaged in the fourth cabinet.

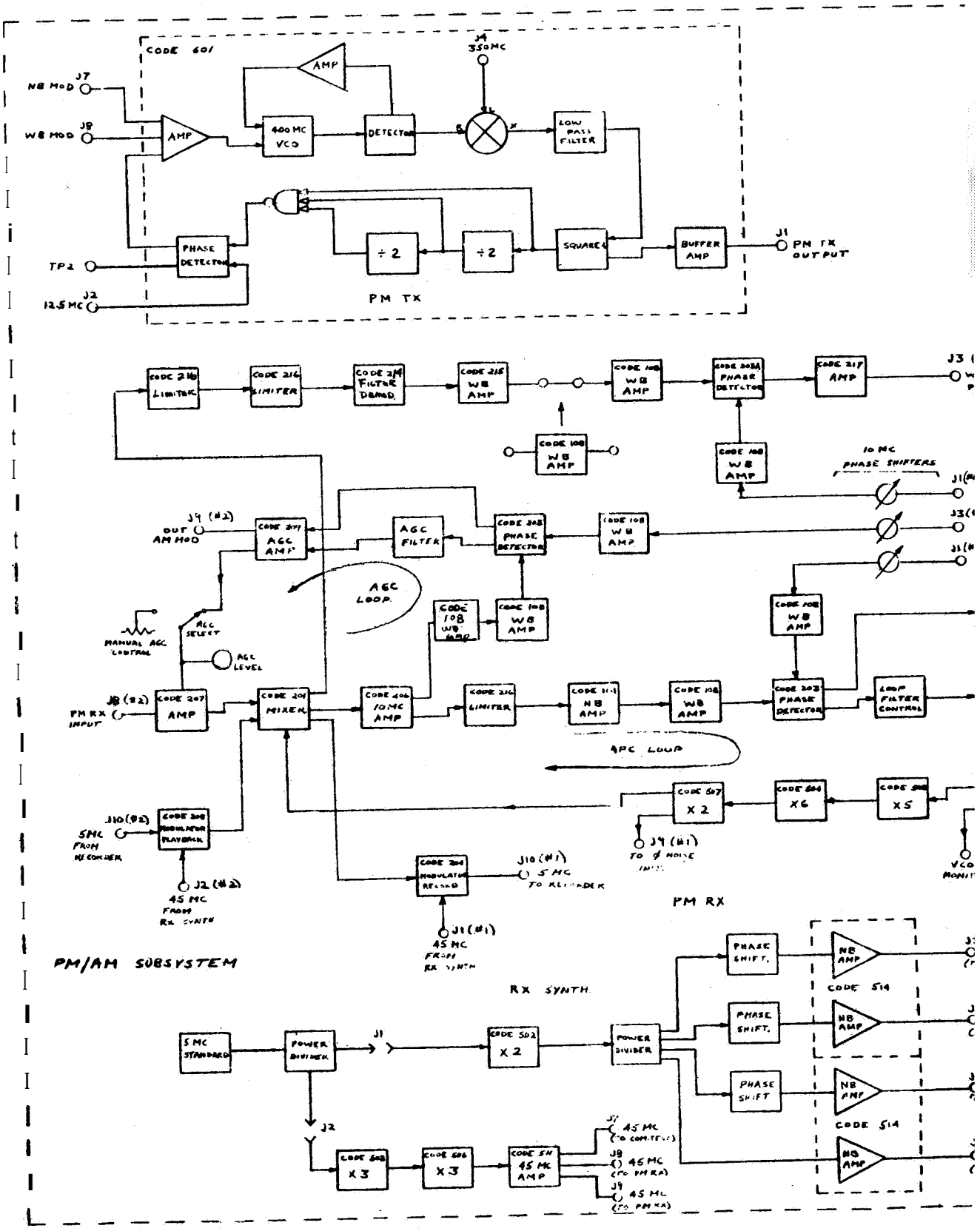
The individual circuits are packaged in RF tight modules. All module signal connections are made with double shielded cables and TSM connectors. The power supply voltages are connected to each module through line filters, The module enclosures are packaged in drawers that can be extended from the cabinets on elides. The drawer cables are connected to the cabinets through cable guides to prevent tangling when the drawers are extended.

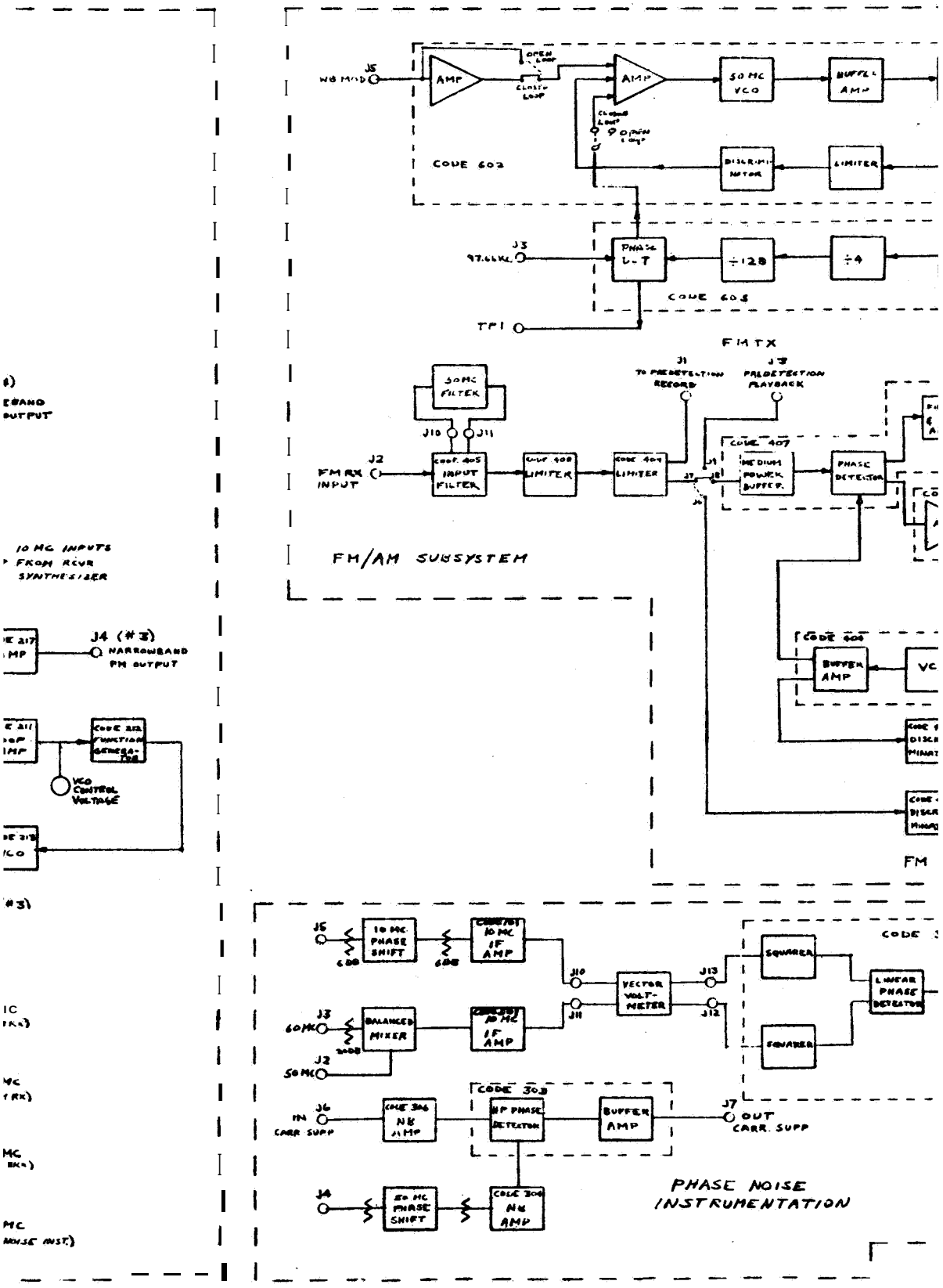
The Operator's Manual is included in Appendices C and D (separate volumes) of this report, Appendix B contains the system filter designs and test data. Appendix A includes the revised performance specifications. Appendix A has been revised to reflect the measured system performance. Test data has been correlated with the original specifications.

2.2 FREQUENCY SYNTHESIZERS

There are two frequency synthesizers in the RF Test Console. The transmitter synthesizer provides outputs for the P. M. and F. M. transmitters, S/N Summer, Phase Noise Instrumentation, Special Test Instrumentation and Commercial Test Instrumentation. The receiver synthesizer provides frequencies for the P. M. receiver, Commercial Test Instrumentation, and Phase Noise Instrumentation.


S/N SUMMER
NOISE SOURCE
NOISE PREAMP
NOISE AMP
NOISE FILTER
COUPLER 15DB
1KC FROM TRANSMITTER SYNTHESIZER
BALANCED MIXER
SOLO-METER
LEVEL CONTROLLER
NULL DETECTOR
1KC AMP
SIGNAL
SUM OUTPUT
SUM MONITOR
SIGNAL INPUT
SIGNAL OUT
OUTPUT
AMP
CODE 510 12.5 & 97.66 KC GENERATOR
DRIVER
12.5 MC (TO PM TX)
97.66 KC (TO FM TX)
1MC (TO Ø NOISE INST.)
CODE 512 350 MC GENERATOR
FILTER
CODE 500 PHASE LOCK FILTER
PHASE DETECTOR
XTAL OSC
POWER SPLITTER
50 MC (TO TEST INST.)
50 MC (TO Ø NOISE INST.)
1KC (TO S/N SUMMER)
TRANSMITTER SYNTHESIZER


CODE 601
J4
350MC
NB MOD
J7
WB MOD
J8
AMP
AMP
400 MC VCO
DETECTOR
LOW PASS FILTER
PHASE DETECTOR
÷ 2
÷ 2
SQUARER
BUFFER AMP
J1
PM TX OUTPUT
TP2
J2
12.5 MC
PM TX
CODE 216 LIMITER
CODE 216 LIMITER
CODE 219 FILTER DEMOD.
CODE 218 WB AMP
CODE 108 WB AMP
CODE 203A PHASE DETECTOR
CODE 217 AMP
CODE 108 WB AMP
CODE 108 WB AMP
10 MC PHASE SHIFTERS
J9 (#2)
OUT AM MOD
CODE 211 AGC AMP
AGC FILTER
CODE 203 PHASE DETECTOR
CODE 108 WB AMP
AGC LOOP
CODE 108 WB AMP
CODE 108 WB AMP
MANUAL AGC CONTROL
AGC SELECT
AGC LEVEL
J8 (#2)
PM RX INPUT
CODE 207 AMP
CODE 201 MIXER
CODE 406 10 MC AMP
CODE 216 LIMITER
CODE 111 NB AMP
CODE 108 WB AMP
CODE 203 PHASE DETECTOR
LOOP FILTER CONTROL
APC LOOP
CODE 507 X 2
CODE 506 X6
CODE 505 X5
J10 (#2)
5MC FROM RECORDER
CODE 209 MODULATOR PLAYBACK
J2 (#2)
45 MC FROM RX SYNTH
CODE 204 MODULATOR RECORD
J10 (#1)
5 MC TO RECORDER
J9 (#1)
TO ∅ NOISE
J1 (#1)
45 MC FROM RX SYNTH
PM RX
PM/AM SUBSYSTEM
RX SYNTH
PHASE SHIFT.
NB AMP
CODE 514
PHASE SHIFT.
NB AMP
PHASE SHIFT
NB AMP
CODE 514
NB AMP
5 MC STANDARD
POWER DIVIDER
J1
CODE 502 X 2
POWER DIVIDER
J2
CODE 503 X 3
CODE 506 X 3
CODE 511 45 MC AMP
J5 45 MC (TO COMPUTER)
J8 45 MC (TO PM RX)
J9 45 MC (TO PM RX)


J5
AMP
OPEN LOOP
CLOSED LOOP
AMP
50 MC VCO
BUFFER AMP
CODE 602
DISCRIMINATOR
LIMITER
J3
PHASE L-T
÷128
÷4
CODE 603
TP1
FM TX
J1
TO PREDETECTION RECORD
J3
PREDETECTION PLAYBACK
50MC FILTER
J10
J11
J2
FM RX INPUT
CODE 405 INPUT FILTER
CODE 408 LIMITER
CODE 409 LIMITER
CODE 407
MEDIUM POWER BUFFER
PHASE DETECTOR
FM/AM SUBSYSTEM
CODE 404
BUFFER AMP
FM
J5
10 MC PHASE SHIFT
10 MC IF AMP
J10
J11
VECTOR VOLT-METER
J13
J12
SQUARER
SQUARER
LINEAR PHASE DETECTOR
J3
60MC
BALANCED MIXER
10 MC IF AMP
J2
50MC
CODE 303
J6
IN CARR SUPP
CODE 306 NB AMP
HP PHASE DETECTOR
BUFFER AMP
J7
OUT CARR. SUPP
J4
20 MC PHASE SHIFT
CODE 304 NB AMP
PHASE NOISE INSTRUMENTATION
10 MC INPUTS FROM RCVR SYNTHESIZER
J4 (#3)
NARROWBAND PM OUTPUT
VCO CONTROL VOLTAGE

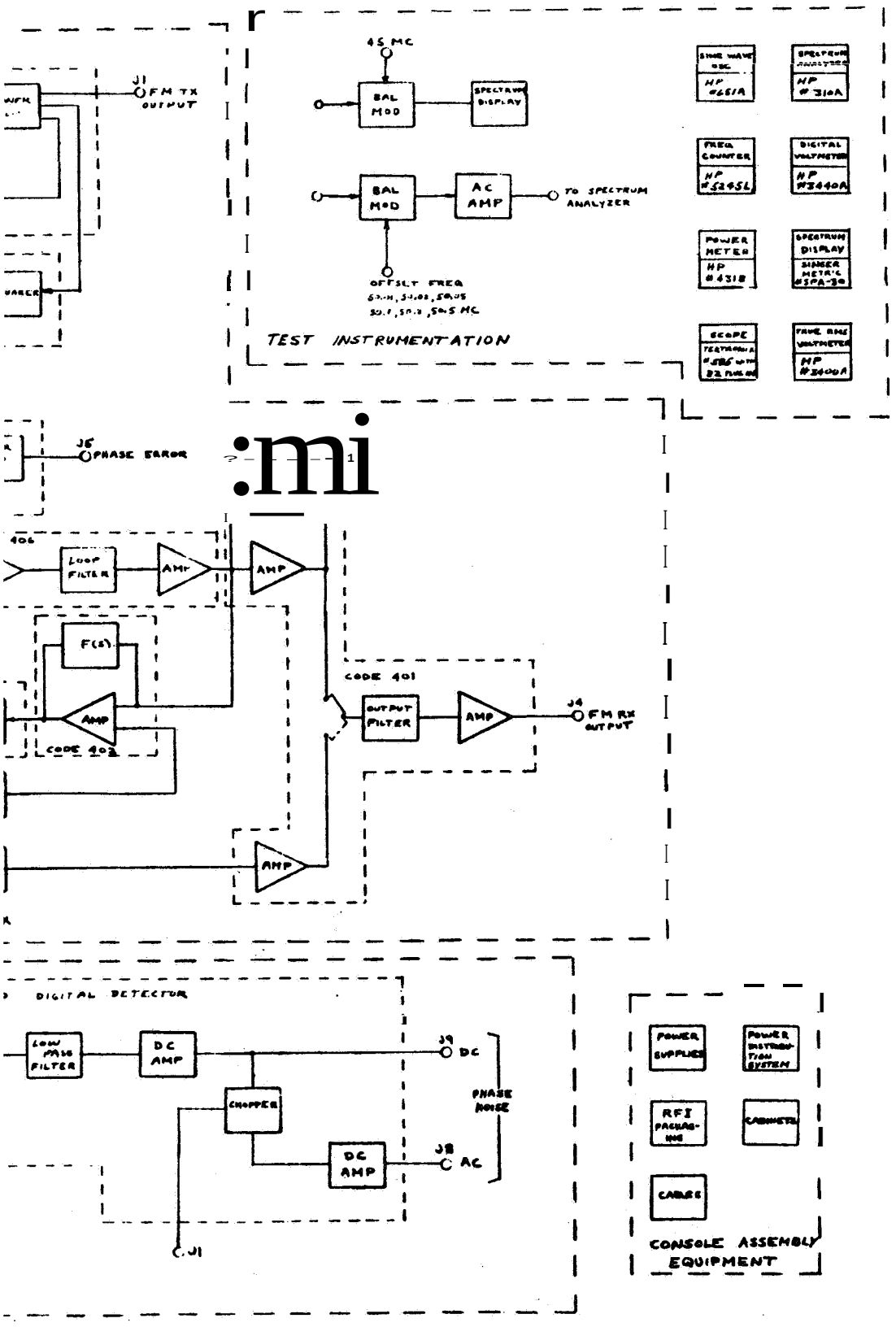


Figure 2.2.1. Functional Block Diagram R. F. Test Console

2.2.1 Transmitter Frequency Synthesizer

Figure 2.2.1.1 indicates a simplified block diagram of the transmitter frequency synthesizer. The following system specifications are applicable to the transmitter frequency synthesizer:

Frequency Stability. The frequency stability of both the transmitter frequency source and the receiver reference oscillator shall be as follows:

a. Each shall have a short-term stability, measured over a one-minute period, of 1 part in 10^7.

b. Each shall have a long-term stability, measured over a four hour period of 5 parts is 10^7.

Phase Stability. The phase stability of the unmodulated transmitter-receiver pair shall be such as to cause no more than a one degree RMS phase error in a noise-free phase-coherent receiver with a 2BLo of 3.0 cps.

Frequency. The transmitter center frequency shall be exactly 50 Mc and shall be continuously tunable ±500 cps about this frequency by manual control.

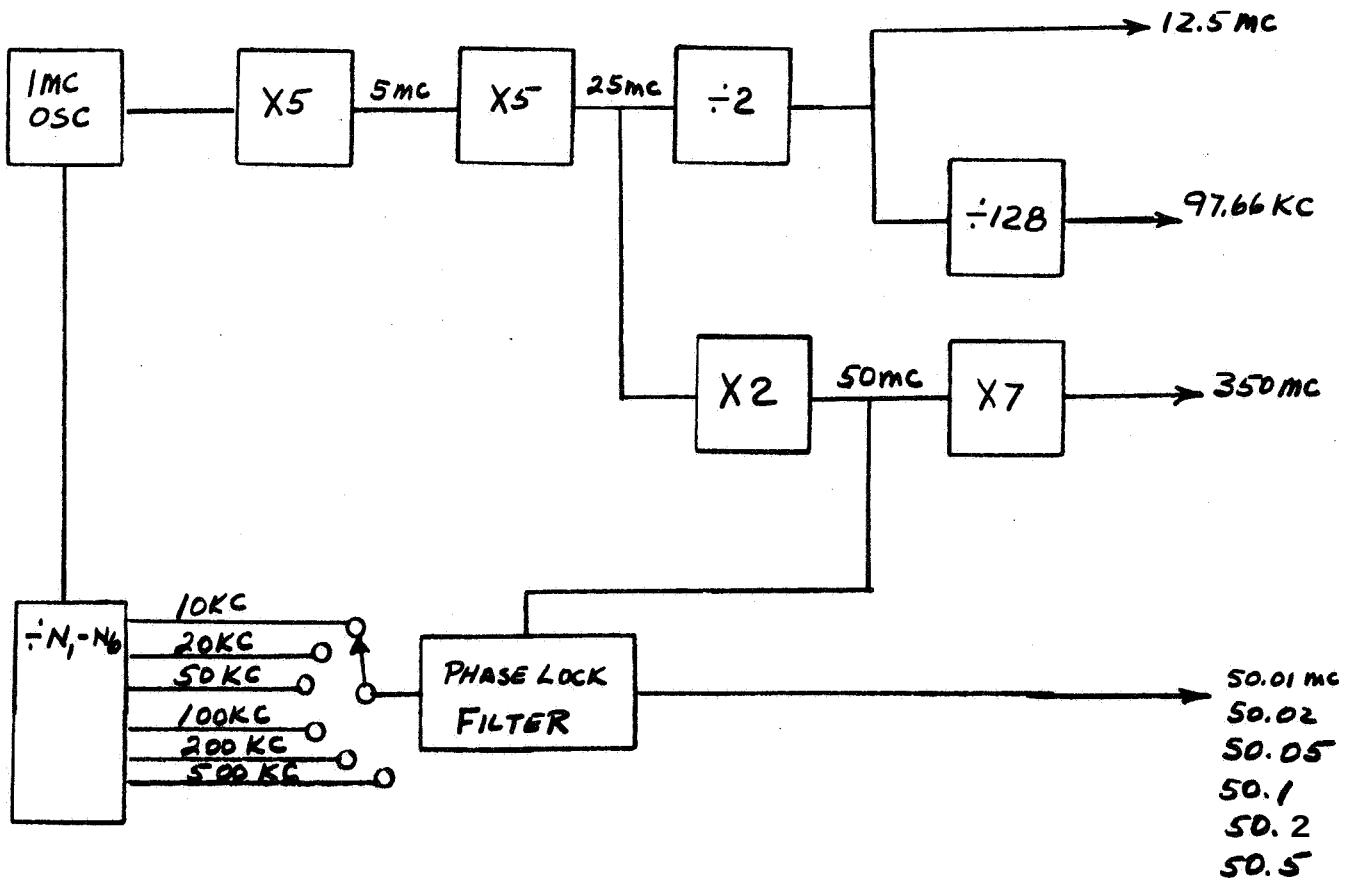


Figure 2.2.1.1. Block Diagram, Transmitter Frequency Synthesizer

The design plan formulated during the Phase I effort to fulfill the frequency and phase stability specifications, is summarized as follows: The one minute and four hour frequency stability specifications dictated that the transmitter master oscillator be proportionally temperature controlled. The oscillator was designed and packaged in two Dewar flasks. The inner oven is temperature controlled. The outer oven is not heated, but serves to decouple the inner oven from cabinet drafts, etc.

The phase stability specification requires that the system exceed the one minute frequency stability specification by at least an order of magnitude. Preliminary tests during the course of the Phase I effort indicated that in order to meet the phase stability specification, the double oven system and an extremely low noise oscillator would be required. However, the specification also requires manual tuning of the master oscillator of ±500 cps at 50 Mc. Therefore, a high Q ($Q = 2.5 \cdot 10^{+6}$) fundamental, 1 Mc crystal oscillator was planned as the transmitter reference.

State-of-the-art commercial oscillators exhibit adequate phase stability: however, these units utilize overtone crystals that cannot be tuned over the specific range.

The design plan was followed during the Phase II design effort with the following modifications: a field effect transistor was used to achieve active gain in the first oscillator stage in place of a low noise transistor. The proportional control oven reference (10 Kc) produced sidebands on the oscillator output (-90 db) with respect to the 1 Mc output. The sideband level was not acceptable, as revealed by residual F. M. tests. Attempts to reduce the sideband level by reorganizing the oscillator package (shielding, etc.) was not successful. Ultimately, the oscillator output was filtered (after multiplication to 5 Mc) with a narrow band crystal filter centered on 5 Mc. This brute force technique reduced the sidebands (multiples of 10 Kc) to a level -135 db with respect to the 5 Mc multipler output. Aside from these changes in design plan, the transmitter frequency synthesizer performed within specification as described in Section 3 of this report.

2.2.2 Receiver Frequency Synthesizer Design Plan

Figure 2.2.2.1 presents the Receiver Frequency Synthesizer block diagram. The Receiver Frequency Synthesizer specifications are essentially the same as those of the transmitter synthesizer and are as follows:

Frequency Stability. The frequency stability of both the transmitter frequency source and the receiver reference oscillator shall be as follows:

a. Each shall have a short-term stability, measured over a one-minute period, of 1 part in 10^7.

b. Each shall have a long-term stability, measured over a four hour period, of 5 part in 10^7.

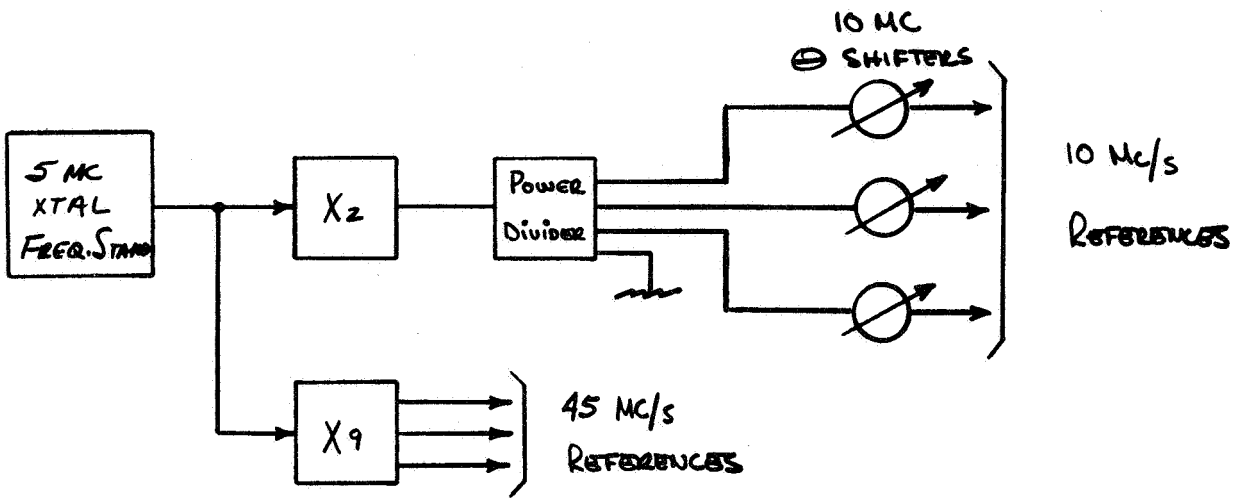


Figure 2.2.2. 1. Block Diagram, Receiver Frequency Synthesizer

Phase Stability. The phase stability of the unmodulated transmitter-receiver pair, shall be such as to cause no more than a one degree RMS phase error in a noise-free, phase-coherent receiver with a 2 BLo of 3.0 cps.

Reference Oscillator. The P. M. Receiver Reference Oscillator shall have a fixed-frequency output tunable to exactly 10 Mc. 1 Mc multiplier to 10 Mc.

The frequency and phase stability of the receiver synthesizer oscillator are essentially the same as for the transmitter synthesizer. However, the specified tuning range is considerably less for the receiver synthesizer. Therefore, a General Radio oscillator was purchased. The advertised short-term stability of this unit was equal to or better than the two principal competitors; namely, Hewlett Packard and Frequency Electronics. However, all vendors specified their oscillator's phase stability in terms of the dimensionless ratio, $(\frac{\Delta f}{f})$, change in frequency normalized to center frequency referenced to an integration time τ. This parameter is a comparative guide, but the specification is written in terms of the system phase noise in the frequency domain.

For the reasons noted, the General Radio Oscillator was purchased for the receiver reference oscillator. The unit's basic frequency is 5 Mc. As outlined in the design plan, the

17

oscillator output was multiplied to 10 Mc and to 45 Mc to provide receiver 10 Mc references and the 45 Mc conversion frequency for predetection record and playback.

The Phase I design plan included transistor frequency multipliers applicable to both the transmitter and receiver frequency synthesizers. The basic multiplier included a harmonic generator consisting of an over-driven linear amplifier and subsequent linear narrow band amplifiers tuned to the desired harmonic. The multipliers were fabricated according to the original design plan with the exception that hot carrier diodes were used as the harmonic generators. The 50 to 350 Mc multiplier used in the transmitter synthesizer, utilized a step recovery, or snap diode, harmonic generator.

The individual multiplier test data indicatedthat all harmonics of the input and output frequencies were a minimum of -60 db with respect to the desired output frequency. The frequency multiplier phase noise contribution to the overall system phase noise was sufficiently small that the system phase stability was within specification. Frequency multiplier design and test data is included in Section 3.

2.3 P. M. SUBSYSTEM

The P. M. Subsystem is outlined in detail as a portion of figure 2. 3. 1. The P. M. Subsystem consists of the P. M. Modulator and P. M. Receiver. Each of these units was fabricated to its own specification; however, several specifications pertain to the performance of the transmitter/receiver pair. This section deals with the P. M, Transmitter/Receiver pair specification and the design plan utilized to meet specified parameters. Table 2. 3. 1 presents the principal P. M. Subsystem specifications. The frequency and phase stability specifications pertain to not only the P. M. Transmitter Receiver pair but also the Transmitter and Receiver frequency synthesizer. The sections of this report that include the frequency synthesizer discuss these same two specifications; however, the P. M. Subsystem's influence on the overall system frequency and phase stability is included here.

The P. M. Subsystem short and long term frequency stability parameters, as defined by the specifications, are determined by the Transmitter Reference Oscillator, located in the Transmitter Frequency Synthesizer, and the P. M. Receiver Reference oscillator, in the Receiver Frequency Synthesizer. The design plan derived in Phase I and implemented in Phase 11 indicated that the Transmitter/Receiver frequency stability specification required proportional temperature control of the oscillator's crystal. Further, the regulation of the oscillator power supplies must absorb variations in both primary line voltage and load currents. The test results listed in Section 3.0 of this report indicate that the precautions taken were more than adequate to meet the subsystem frequency specification. However, one cannot assume that "over design" was involved, for an overlap exists between the one minute frequency stability and phase stability specifications. To meet the latter specification, the system's one minute frequency stability had to be overdesigned.

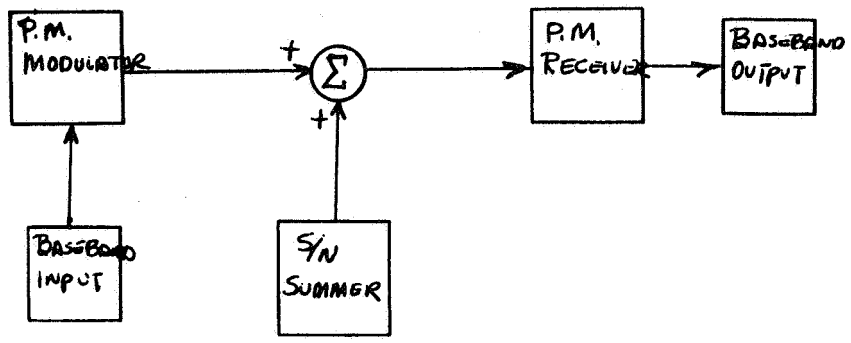


Figure 2.3.1 P. M. Subsystem

The P. M. Subsystem Phase Stability (specification listed in table 2.3.1) is a function of the phase stability of the transmitter frequency standard, the P. M. Receiver Reference oscillator, the carrier tracking loop VCO, the system frequency multipliers, amplifiers, and receiver noise figure. The Phase I Design plan included a lengthy description of oscillator and frequency multiplier design plus experimental evidence that the system could be built to achieve one degree RMS phase noise in 2 BLO 3.0 cps. The Phase II design correlated very closely with the Phase I design plan. The measured system phase noise was 0.25 degrees RMS in 2 Blo of 3.0 cps. Further, it is our opinion that a phase noise of 0.1 degrees (or less) RMS in 2 Blo of 3.1 cps is achievable. However, it was necessary to include a loop D. C. amplifier and a diode function generator to achieve loop gain linearity. The l/f noise of these units contributes a large share of the 0.25 degree phase noise measured. The P. M. Subsystem Fidelity Specification (shown in table 2.3.1) is a function of the P. M. Modulator Linearity, the phase linearity of the receiver input amplifier, mixer, and wide band 10 mc i-f amplifier. The Phase I design plan included an analysis relating the P. M. Modulator intermodulation to the modulator phase detector, loop amplifier and VCO. The modulator phase detector was designed as a high speed set-reset flip flop. The linearity of the transfer of output voltage to input phase is included in Section 3 of this report. The nonlinearity of the

Table 2.3.1. P. M. Subsystem Principal Specifications

1. Frequency Stability The frequency stability of both the transmitter frequency scource and the receiver reference oscillator shall be as follows:	a. Each shall have a short term stability measured over a one-minute period of 1 part in 10^7 b. Each shall have a long-term stability measured over a four hour hour period of five (5) parts in 10^7
2. Phase Stability	The phase stability of the unmodulated Tx/Rx pair shall be such as to cause no more than one degree rms phase error in 2 BL of 3.0 cps.
3. Fidelity	The fidelity of the Tx/Rx pair shall be such that all spurious sidebands within the modulation passband are 30 db (40 db design goal) below the modulated carrier or 40 db (50 db design goal) below unmodulated power when the transmitter is modulated with two pure sinusoids of any frequency and at modulation indices within the phase modulator design limits.

modulator VCO was minimized by designing the VCO as a UHF oscillator (400 Mc) to minimize the ratio of peak-to-peak frequency deviation to center frequency).

The receiver Input amplifier and Wideband I-F amplifier were designed to exhibit maximally flat group delay or linear phase response. The receiver mixer and limiters were designed as broad band units that exhibit a linear phase response over the band of interest. These precautions summarize the steps outlined in the Phase I design plan and implemented in the Phase II fabrication to meet the P. M. Subsystem fidelity specification. The receiver demodulation channel phase detector is a non-linear sinusoidal unit (as required by DSIF simulation) and the phase detector output filter exhibits a Butterworth amplitude response with an inherent non-linear phase response. Therefore, the subsystem fidelity was measured from the modulator baseband input to receiver phase detector input. A linear phase detector was used to demodulate the two-tone baseband.

2.3.1 P. M. Modulator Design Plan

Figure 2.3. 11 is the simplified P. M. Modulator block diagram. The P. M. Transmitter specifications are listed below:

Table 2.3.1.1 P. M. Modulator Principal Specifications

Carrier Frequency	50 Mc tunable ±500 cps
Phase Modulator	
a. Frequency Response	±0. 1 DB, to 500 Kc ±0. 5 db 500 Kc to 1.0 Mc
b. Phase Deviation	±3. 0 radians DC to 500 Kc ±1. 0 radian DC to 1.5 Mc
c. Deviation Linearity	See P. M. Tx/Rx pair spec.
d. Incidental A.M.	See P. M. Tx/Rx pair spec.

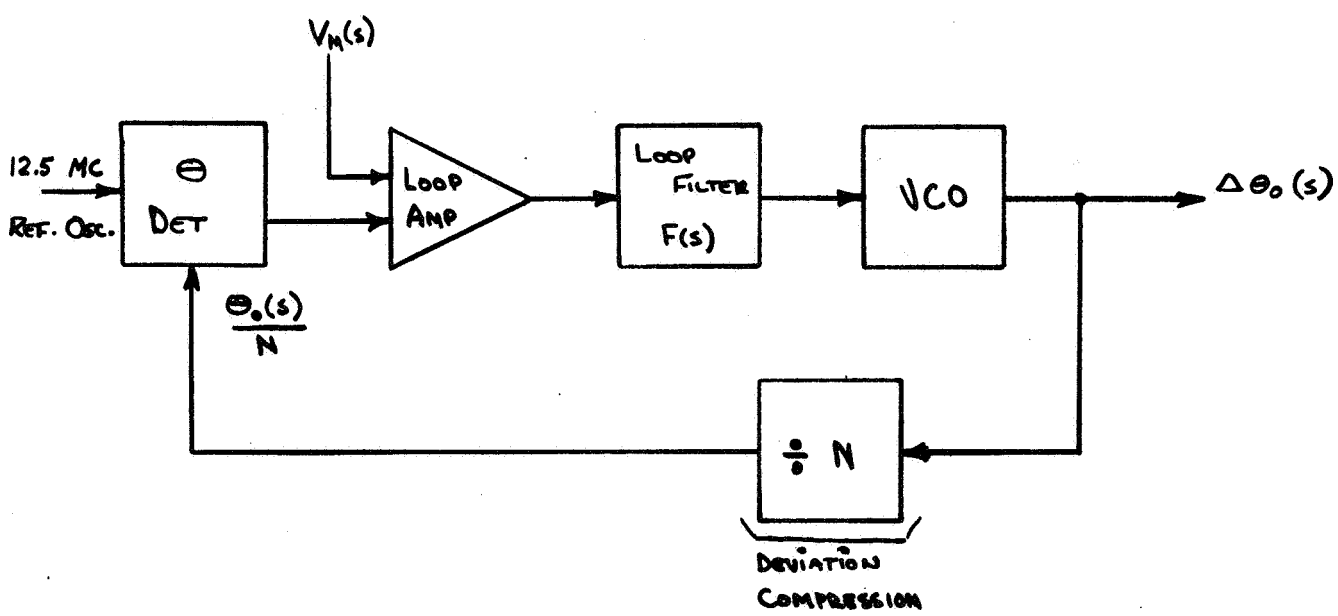


Figure 2.3.1.1. Block Diagram, P. M. Modulator

The Phase Modulator Design Plan is detailed in Appendices D and E of the Phase I Final Report. These reports outline two principal techniques. One includes the locked oscillator phase modulator and the other the limited phase deviation frequency multiplier phase modulator. Of the two, the latter was judged the more difficult to implement due to the wide bandwidths involved. The frequency multiplier, phase modulator was used as a back up approach in the event the locked oscillator phase modulator could not be realized.

The locked oscillator phase modulator was chosen as the first approach. Although this technique was untried, it is based on control theory and network synthesis, both of which are well defined in today's technology. The distinct advantage of being able to reduce the entire modulator to a single transfer function makes this form of phase modulator very desirable. A multiple pole baseband response reduces to a root locus analysis and a network synthesis problem.

The Phase I study selected the criteria for a locked oscillator phase modulator to be the minimization of modulation error and intermodulation by use of a "maximally" flat delay response. The loop gain and bandwidth must be consistent with the modulation spectrum and have adequate rejection of spurious harmonics generated by the loop multiplier.

Several loop designs were investigated in Phase I. The designs were primarily 3 and 4 pole Butterworth and Bessel low pass baseband transfer functions.

The details of the modulator design are included in Section 3 of this report. During the Phase II fabrication, it became evident that the inherent loop transport lag dictated a minimum closed loop bandwidth compatible with the specified amplitude response. As a result, the 4 pole Butterworth response was fabricated.

As noted before, the Butterworth synthesis yields a maximally flat amplitude response an4as such, was implemented to meet the amplitude response specification. However, the phase response of the Butterworth synthesis is quite non-linear in the region of loop cut off frequency. As a result, the transient response and intermodulation (as a function of phase non-linearity) characteristics are inferior to a linear phase synthesis.

2.3.2 P. M. Receiver Design Plan

A simplified block diagram of the P. M. Receiver is shown in figure 2.3.2. 1. The principal P. M. Receiver Specifications are shown in Table 2.3.2.1. A brief review of the Phase I design plan and deviations from the design plan are included in this section. The receiver tests and test results are listed in Section 3. 2. 2.

The design plan formulated in Phase I proved to be extremely useful during the Phase II design and fabrication phase. Although deviations from the Phase I Design Plan resulted during the course of the design, the basic plan was implemented.

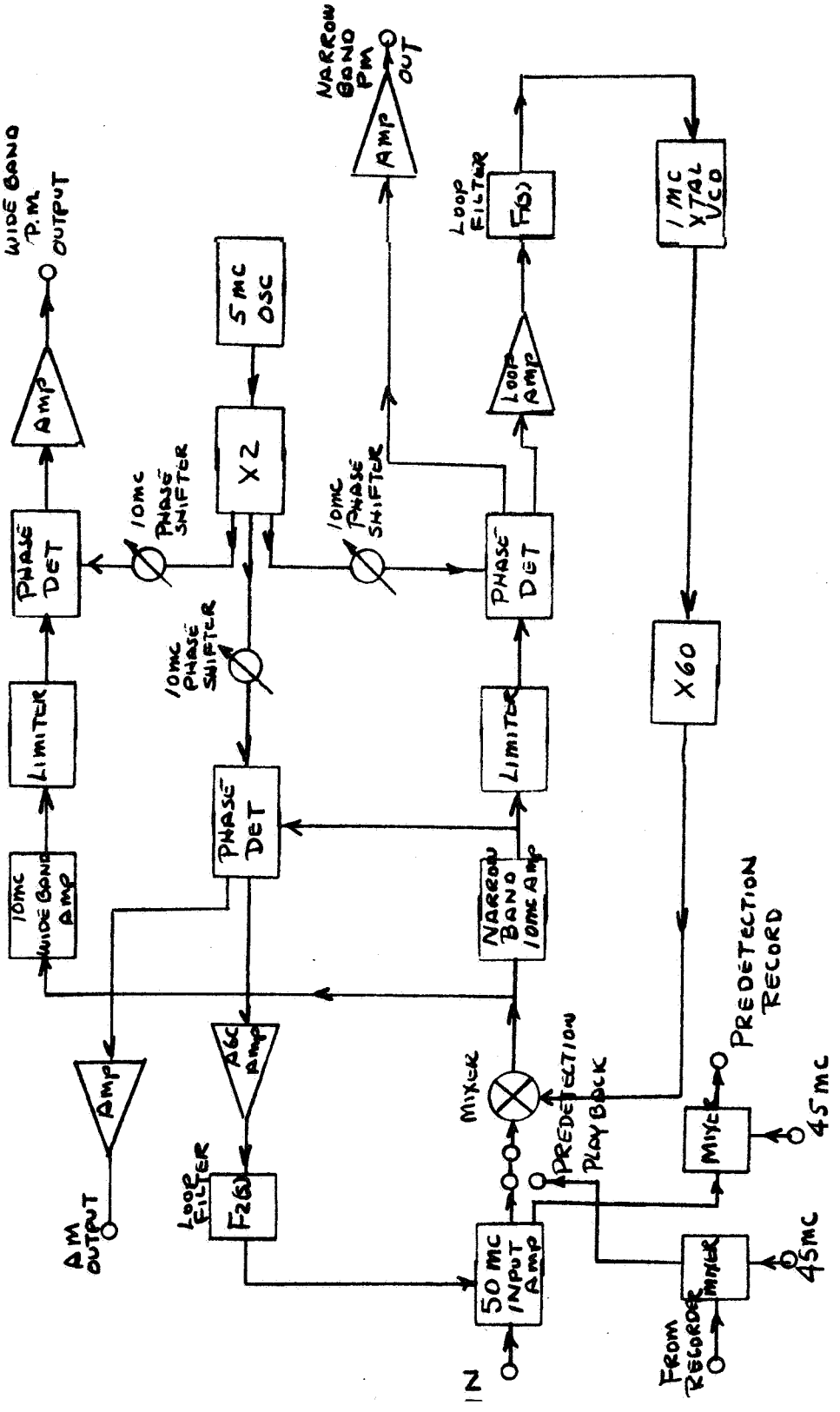


Figure 2. 3. 2. 1. Block Diagram, P.M. Receiver

Table 2.3.2.1. P. M. Receiver Principal Specifications

1. Carrier Frequency	50 Mcs
2. Input Amplifier	
a. Bandwidth	3 db B. W. 10 Mcs min. flat within ±0.25 db within ±2 mc of 50 Mcs
b. Phase Linearity	Compatible with P. M. Subsystem Linearity Spec.
c. AGC Range	30 db
3. Narrow Band IF	
a. Center Frequency	10 Mcs
b. Bandwidth	2 Kz (3 db)
c. Phase Symmetry	±5° for frequencies ±1 Kc of center frequency (±6 Kc Design Goal)
4. Wideband IF	
a. Center Frequency	10 Mcs
b. Bandwidth	6 Mcs (3 db) ±0.5 db within 1.5 mcs of center frequency
c. Phase Symmetry	±5 degrees over 6 mc passband
5. Wideband Phase Detector	
a. Video 3 db Bandwidth	5 mc
b. Dynamic Range	40 db
c. Fidelity	Compatible with P. M. Subsystem Linearity Spec.
6. Carrier Tracking Loop	
a. No Noise Loop Gain	Constrain Static Phase Error 1 Degree, Transmitter Detuning ±500 cps
b. Loop Bandwidths 2 BLo	3.0, 12.0, 20.0 and 48.0 cps, variable 1.0 cps = 1 Kc
c. Loop Filter	Active and passive, 1% resistors, 3% capacitors
d. Loop Gain Stability	±3% over transmitter tuning range

Table 2.3.2.1. P. M. Receiver Principal Specifications (Continued)

7. AGC Loop	
a. Min. Loop Gain	20
b. Loop Noise Bandwidths	.01, 0.1, 1.0 and 10 cps
c. Loop Filter	Passive, 1% resistors 2% capacitors
8. Predetection Record and Playback	
a. Record	P. M. Spectrum down converted to 50 Mc
b. Playback	Recorder spectrum up converted to 50 Mc

The P. M. Receiver and, indeed, the RF Test Console system consists of a group of basic circuits or modules that were designed to module specifications. The basic modules are interconnected to form the various subsystems. By necessity, some modules are used only once but many are used in several places in the system. Several simple basic precautions were taken that later proved valuable. In general, 30 DB maximum gain was alloted per module. Each module was packaged in an RF tight enclosure. All module power lines were filtered at each module enclosure and double shielded 50 ohm cables with threaded RF connectors were used in all signal paths. Each transistor within a module circuit was both RC and LC decoupled from the plus and minus power supplies. Nearly all the system amplifiers were designed as feedback amplifiers with a large ratio of open to closed loop gain. The precautions listed were quite expensive and wasteful of power; however, in system test the usual RF problems of leakage, extraneous coupling and oscillation were practically non-existant.

The P. M. Receiver processes and demodulates an angle modulated carrier. Considerable design effort was expended to assure that all RF amplifiers, limiters, and mixers exhibited a linear phase response in the band of interest. We were fortunate to secure an early model of the Hewlett Packard 8405A Vector Voltmeter which enabled us to measure module phase responses and group delay. The Weinschel Dual channel Insertion Loss Test Set was used to measure amplitude responses in instances where extreme accuracy was required.

The receiver block diagram, shown in figure 2.3.2.1, includes a 50 Mc input amplifier, 10 Mc wide band amplifier, and 10 Mc narrow band amplifier. In accordance with the design plan, the actual devices used in these units are broadband feedback amplifiers that exhibit linear phase response and flat amplitude response in the frequency band of interest. The

specified amplitude and phase responses are achieved with plug-in passive filters. The filter source and load impedances were designed to achieve fifty ohms resistive over the filter bandwidth; therefore, the amplifier phase and amplitude response may be easily changed by substituting passive filters.

The Phase I design plan outlined a VCO design approach whereby the VCO frequency was established at 1 Mc and subsequently multiplied to 60 Mc. The VCO crystal was selected for maximum Q ($2.5 \times 10^{+6}$) and packaged in a proportionally temperature controlled oven. A fundamental crystal was selected because the oscillator's center frequency must be changed plus or minus ten cycles with a reasonable scale factor (1 cycle/volt sec). A low noise oscillator circuit was designed utilizing a field effect transistor. Admittedly, the oscillator's phase noise is multiplied by 60; however, as discussed earlier in the report, the system easily meets the phase stability specification. It is of interest to note that the oscillator crystal and circuit must be proportionally temperature controlled to meet the system phase stability specification when 2 Blo is 3.0 cps. For example, the oscillator cover may be removed and cabinet drafts allowed to circulate about the oven and low frequency phase errors in excess of one degree will result due to temperature variations.

As shown in figure 2.3.2. 1, the system utilizes three power phase detectors. A universal phase detector was designed; however, the demodulation channel unit was modified to provide a larger dynamic range. A universal wideband power amplifier with a linear 2 watt capacity was designed to serve as a phase detector driver. Neither the carrier tracking loop nor the coherent AGC phase detectors require the inherent phase detector or drive bandwidth capabilities. The receiver output amplifiers are low power broadband operational amplifiers capable of driving a 600 ohm load.

The P. M. Receiver play-back and record system was modified from the Phase I design plan. As shown by figure 2.3.2. 1, an auxiliary output is provided from the 50 Mc input amplifier which is down-converted to 5 Mc for recording. The recorded spectrum retains the influence of the input amplifier AGC system. In turn, the predetection play-back 5 Mc spectrum is up-converted to 50 Mc and is patched into the receiver behind the input amplifier to avoid traversing the AGC system twice. Both the record and play-back modules include linear phase filters and buffer amplifiers in addition to the mixers.

The receiver gain distribution was modified from that outlined in the Phase I design plan. The principal change involved increasing the gain in the input amplifier. This choice was made to avoid excessive degradation of the receiver noise figure, a function of AGC. This change resulted in a receiver AGC threshold of -85 DBM carrier power. A disadvantage

of this design approach is the presence of relatively high noise levels in the receiver output at minimum carrier power. The receiver output signal to receiver self noise ratio at AGC threshold is as follows:

$KTB_{1\ cps}$ = -174 DBM

$KTB_{(4\ Mc)}$ = -108 DBM Demod channel predetection noise bandwidth = 4 Mc

$KTB_{(4\ Mc)}$ plus Receiver noise Figure = - 105 DBM

minimum carrier = -85 DBM

Receiver S/N at AGC Threshold = +20 DB

Obviously, if the receiver AGC threshold is increased 10 DB the output S/N is increased 10 DB provided the noise figure remains 3.0 DB. However, this logic is not without compromises. If the AGC threshold is increased, the receiver front end gain must be decreased to avoid overload on S/N Summer Noise. This results in a higher receiver noise figure at maximum AGC. However, the noise viewed at the receiver output will be decreased provided the signal increases (with AGC threshold increase) faster than the noise figure. The low noise figure design was selected, although the latter option is easily implemented by simply decreasing gain in the receiver input amplifier. In either case, the error contribution of the receiver self noise summed with the S/N Summer Noise is negligible. For example, if the Summer Noise is maintained 20 DB above receiver self noise referenced to the receiver input, a 0.01 DB error in the Summer S/N ratio results.

2.4 F.M. SUBSYSTEM

The following specifications pertain to the F. M. Subsystem:

Table 2.4.1. F. M. Subsystem Principal Specifications

1. Frequency Stability	The frequency stability of the Tx/Rx pair shall be such as to cause less than 15 cps RMS residual F. M. with the Tx operating in the AFC Mode and 60 cps RMS residual F. M. in non/AFC Mode measured in either conventional or phase lock receiver in a 500 Kc bandwidth.
2. Static Linearity	The Tx/Rx pair shall exhibit a static linearity of ±0.5 percent over the full-scale frequency deviation with the non/AGC Transmitter and either receiver, above and beyond the inherent sinusoidal phase detection non-linearity.

Table 2.4.1. F. M. Subsystem Principal Specifications (Continued)

3. Dynamic Linearity	The Tx/Rx pair shall exhibit a dynamic linearity of ±1.0 percent over all combinations of modulating frequency and frequency deviation in both AFC and non/AFC transmitter modes and with either receiver, above and beyond inherent sinusoidal phase detector non-linearity.

The design plan formulated during the course of the Phase I effort outlined a basic 'YCO" to be used in both the F. M. Modulator and Phase Lock F. M. Receiver. The VCO was intended to improve the specified parameters exhibited by the usual open loop voltage controlled oscillator. Briefly, the VCO analyzed is a closed loop system, consisting of a VCO, discriminator, loop amplifier and loop filter as shown in figure 2.4.1. It is well known that a VCO exhibits the transfer $\frac{\Delta f}{Vm}(s)$. The system shown in figure 2.4.1 duplicates the transfer function; however, several other advantages are evident. All the advantages are based on the assumption that, in a practical sense, it is simpler to build a more linear and less noisy discriminator and loop amplifier than a VCO. If this is a valid statement, then it becomes a simple matter to transfer the static and dynamic linearity and noise characteristics of the discriminator and loop amplifier to the VCO. This basic assumption formed the basis for meeting the F.M. Subsystem specifications. The results of this effort are outlined in detail in Section 3 of this report.

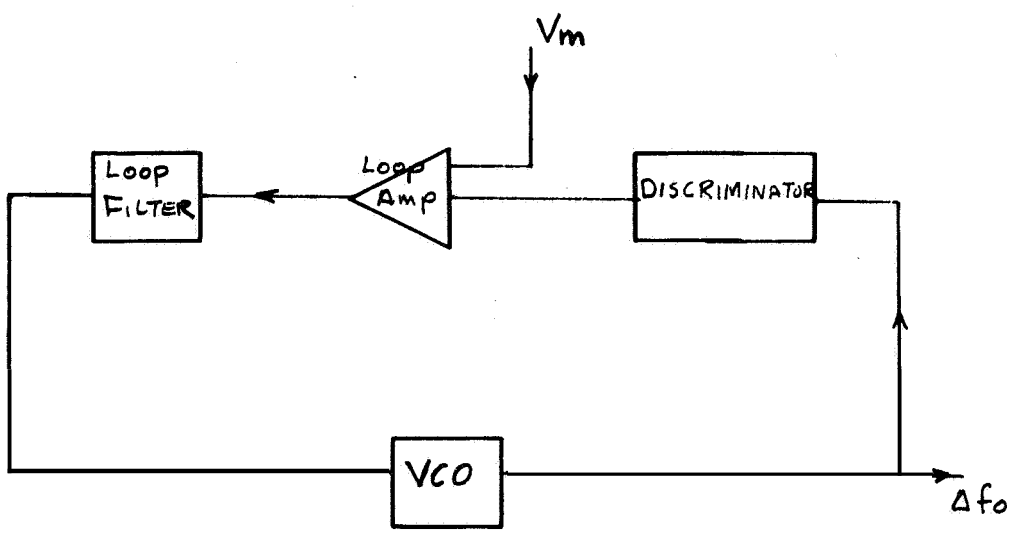


Figure 2.4.1. Block Diagram, Basic F. M. Subsystem VCO

The basic idea proved to be a valid improvement; however, the design was not without problems. For example, a more linear discriminator inherently exhibits a lower slope sensitivity ($\frac{\text{Volts}}{\text{cps}}$) and a lower loop gain resulting in an extremely linear but noisy modulator. Therefore, a compromise between dynamic linearity and residual F. M. proved necessary. Further, the bandwidth of the system is ultimately limited by the loop transport lag. Therefore, (as in the case of the Phase Lock F. M. Receiver "VCO") interaction between the VCO minor loop and the wideband APC major loop was a problem. However, for the modulation indices and loop bandwidths specified the problems were solved and the system proved superior to a simple open loop VCO.

2.4.1 F. M. Transmitter Design Plan

Figure 2.4.1.1 presents a block diagram of the F. M. Transmitter. A brief outline of the principal F. M. Transmitter specifications are listed in Table 2.4. 1. 1.

Table 2.4. 1.1. FM Transmitter Principal Specifications

CARRIER FREQUENCY	50 Mc Tunable ±500 cps
a. Frequency Response	The frequency response of the frequency modulator shall be constant with ±0. 1 db from 50 cps to 100 Kc and ±0. 5 db from 3 cps to 50 cps and 100 Kc to 500 Kc.
b. Frequency Deviation	The modulator shall be capable of deviating the carrier ±500 Kc about its center frequency with a maximum modulation index of 512 in the AFC mode.
c. Deviation Linearity	Refer to F. M. Subsystem Specifications.
AFC Operation	The F. M. Transmitter shall be capable of operating either with or without automatic frequency control. In the AFC mode its modulation response shall be from 3 cps to 500 Kc and in non/AFC from DC to 500 Kc.
RESIDUAL F. M.	15 cps AFC Mode 60 cps Non-AFC Mode.

The transmitter design plan formulated in Phase I to meet the specifications included the closed loop VCO described earlier and a minor APC loop to stabilize the carrier. The closed loop VCO was synthesized to exhibit a closed loop transfer function, mathematically equivalent to a two pole Butterworth passive filter. The cut off frequency was selected such that the transfer $\frac{f_m(s)}{A}$ was maximally flat within ±0. 5 db at 500 Kc.

A minor, narrow band APC loop was included to serve as a means of stabilizing the carrier center frequency and reducing the residual F. M.

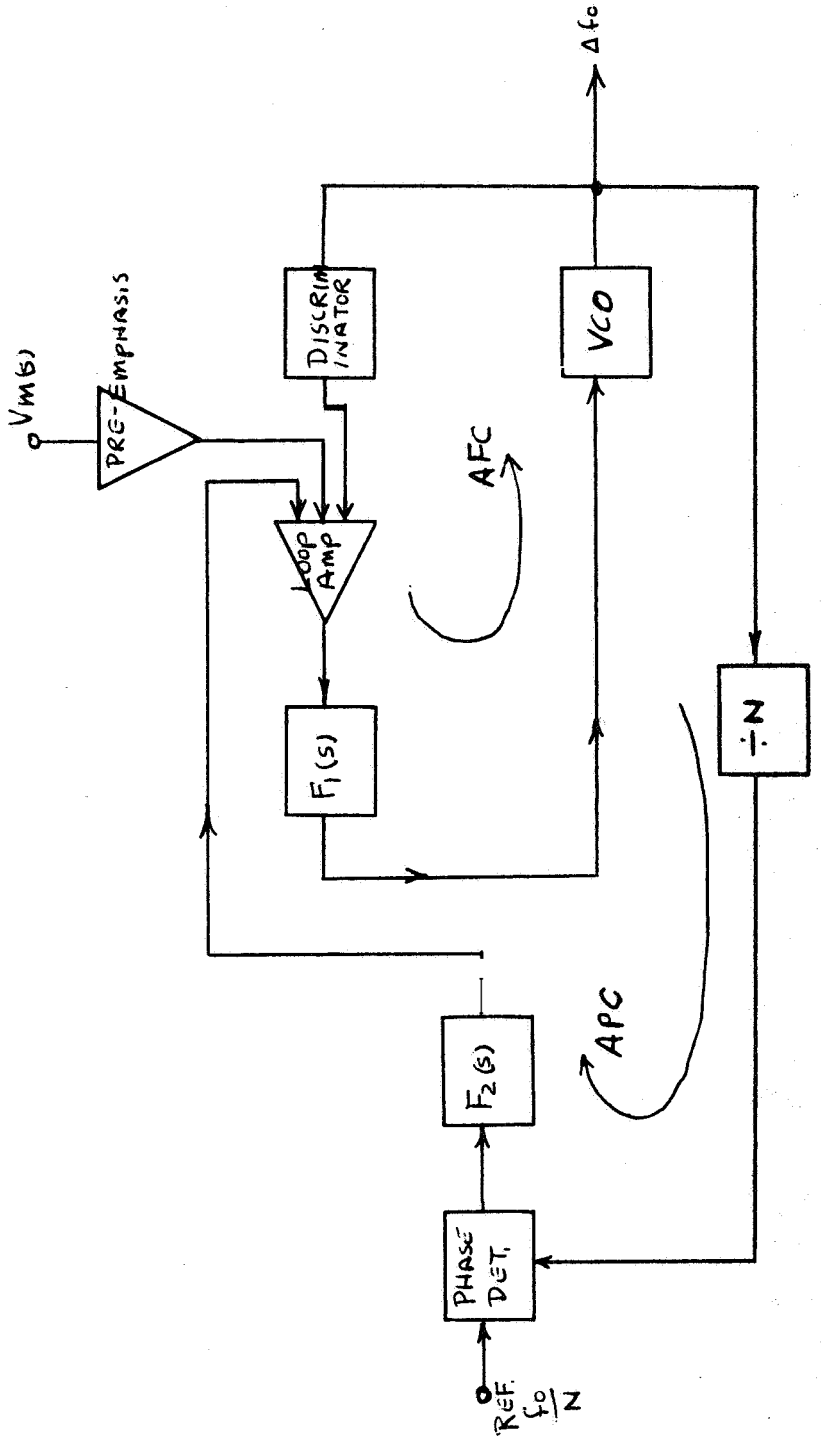


Figure 2.4.1.1. Block Diagram, F. M. Transmitter

This feature of the design plan was implemented; however, the closed loop transfer function of the minor loop was modified to simplify the pre-emphasis network required in the AFC mode.

The carrier stabilization loop proved successful in the sense that it diminished the carrier drift as monitored on a frequency counter (absolute carrier frequency measured over an integration time). However, the reduction in residual F. M. measured in a 500 Kc bandwidth proved insignificant. These results are not surprising if one considers that the carrier stabilization loop is narrow band (50 cps) and that noise reduction results only within the stabilizer loop bandwidth, Aside from this characteristic, the stabilizer loop dictates that the modulation index cannot exceed 512. This latter characteristic limits the peak frequency deviation for low frequency baseband components. Therefore, the "APC" mode is most useful when a reduction in residual F. M. close to the carrier is required and the baseband frequencies do not extend below 50 cps. The latter characteristic allows the operator to use a larger peak frequency deviation without exceeding a modulation index of 512.

2.4.2 F. M. Receiver Design Plan

Table 2.4.2.1 lists the principal F. M. Receiver specifications.

Table 2.4.2.1. F. M. Receiver Principal Specifications

1. Input Band Pass Filters	The input filters shall have half power bandwidths within ±2 percent of 1 Mc, 200 Kc and 10 Kc, (Center frequency, 50 Mc).
a. Phase Response	The filter's phase response shall be linear as established by a Bessel response.
b. Amplitude Response	The amplitude response shall be established by the 3 db bandwidth and the phase characteristic.
2. Limiter	
a. The Dual F.M. Rx shall contain a hard limiter following the input band-pass filter with the following characteristics :	The limiter shall have a dynamic range of 60 db.
3. Conventional F. M. Detector	The dual F. M. Rx shall include a conventional F. M. detector with performance characteristics consistent with the F. M. Subsystem frequency stability and static and dynamic linearity requirements.

Table 2.4.2.1. F. M. Receiver Principal Specifications (Continued)

4. Phase Lock F. M. Detector	The VCO shall have a center frequency of 50 Mc.
a. VCO	The deviation capability shall be consistent with the transmitter modulator characteristics. The static and dynamic linearity and stability shall be consistent with the F. M. Subsystem Specifications.
b. Phase Detector	The phase detector bandwidth shall be consistent with the Tx modulator frequency response. It shall be of sufficient fidelity to meet the subsystem dynamic linearity requirements.
c. Loop Gain	Sufficient to constrain static phase error to 10 degrees when Tx deviation is maximum (500 Kc).
d. Loop Filter	Three standard loop information bandwidths of 3, 30, and 300 Kc shall be supplied.
e. Compensation Filter	A single pole R. C. low pass filter shall be employed at the loop filter output such that the overall phase-lock F. M. detector transfer function is that of a pure loop.
5. Output Low Pass Filter	
The dual F. M. Rx shall include a single low-pass output filter with the following characteristics:	The output filter shall have more than three poles and shall have either maximally flat amplitude or maximally flat phase response. Filter bandwidths of 1, 10 and 100 Kc shall be supplied.
6. Predetection Record and Playback	
a. Record	F.M. Spectrum down converted to 5 Mc
b. Playback	Recorder Spectrum up converted to 50 Mc.

Figure 2.4.2.1 indicates a simplified block diagram of the F. M. Receiver. A brief review of the design plan formulated in Phase I, to meet these specifications follows.

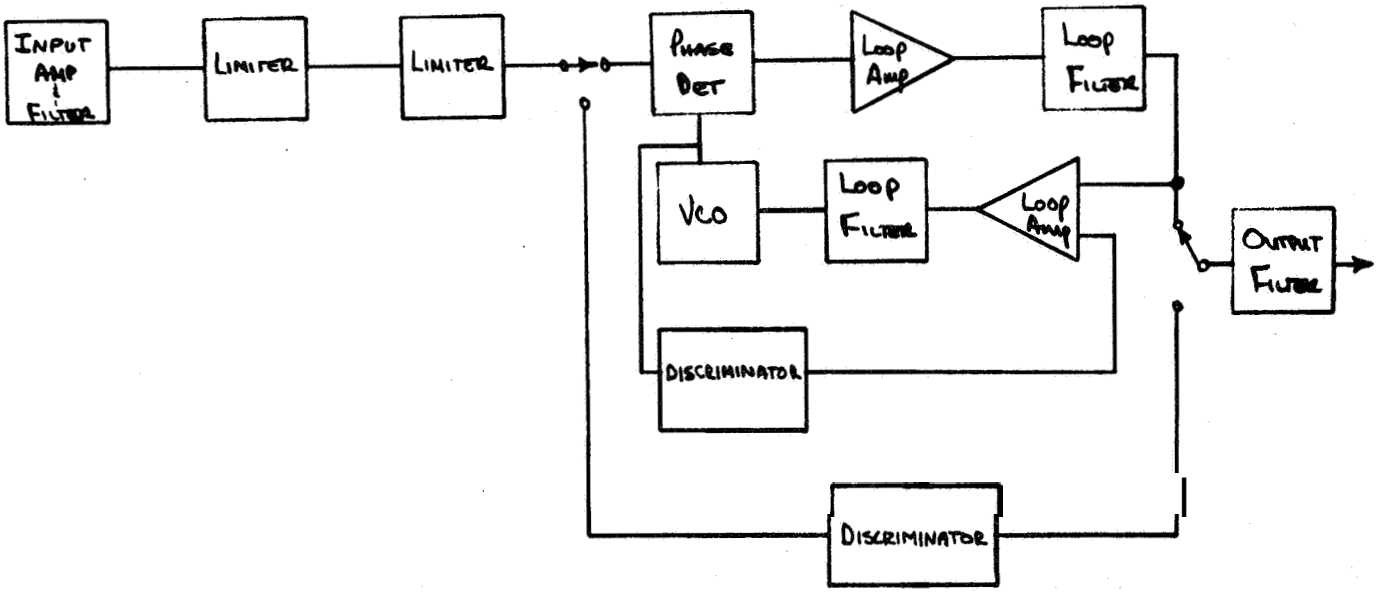


Figure 2.4.2.1. Block Diagram F.M. Receiver

The F. M. Receiver input amplitude and phase response was planned to be established by passive filters, with the active gain to be contributed by low noise broadband amplifiers. The 1 Mc (3 db bandwidth) filter was fabricated as a helical structure and the 10 Kc unit utilized a 4 crystal lattice arrangement. The original specification also called for a 100 Kc, 3 db bandwidth filter, centered on 50 Mc. This unit proved to exist in no man's land. The bandwidth required resonators with Q's too high to be achieved with a helical structure and the bandwidth (combined with the 50 Mc center frequency) made a crystal design impractical.

The problems attendant with the crystal filter design are summarized as follows: The crystals used in a crystal filter must be ground in the fundamental mode to avoid filter harmonic response. However, a fundamental crystal ground to exhibit a fundamental center frequency of 50 Mc is physically small in diameter and the wafer is fragile and the yield of a batch of crystals is low. This problem is not insurmountable (at high cost); however it is nearly impossible to fabricate such a crystal which does not exhibit spurious modes (on the high side of center frequency) less than 30 Kc from center frequency. Thus, the 100 Kc filter utilizing a crystal structure, would exhibit an unacceptable passband amplitude and phase response in a region 30-100 Kc from center frequency. For these reasons, it was practical to build the 10 Kc filter with crystals, but not the 100 Kc filter.

Therefore, a compromise was reached with the cognizant engineer and the original 100 Kc filter 3 db bandwidth was increased to 200 Kc and the unit was designed in a helical structure.

Aside from the input filter problem, the original design plan was utilized for the most part. However, the receiver input amplifier noise figure was minimized in an effort to minimize noise figure contribution to the F.M. Subsystem residual FM. The limiter design included sufficient dynamic range in the interstage amplifiers to minimize carrier phase shift (A. M. to F. M. conversion) as a function of carrier level. The phase lock discriminator VCO was designed as a closed loop system, as described earlier. The Phase I design plan outlined a linear delay line discriminator for use in the closed loop VCO. This unit exhibited the required linearity; however, the slope sensitivity and resulting noise proved unsatisfactory. Subsequent modifications, consisting of a multiple quarter wavelength delay line design, improved the slope sensitivity at little sacrifice of linearity; however, the increased time delay introduced by the longer line, ruined the loop phase margin. The resulting peaking was intolerable. Therefore, a more conventional discriminator was used in the phase lock discriminator and the delay line design was used as the conventional discriminator.

The F. M. Subsystem dynamic linearity was interpreted in terms of a series expansion in which the relationship between receiver output and transmitter baseband input is defined by several terms of a Taylor series.

The voltage e_{out} is the output of the F. M. Receiver while e_{in} is the modulation input to the F. M. transmitter. Thus $e_{out} = f(e_{in})$. Using a Taylor's Series expansion for this function, $e_{out} = a_o + a_1 e_{in} + a_2 e_{in}^2 + a_n e_{in}^n$. The 1 percent linearity is interpreted from the Taylor's Series to mean that $a_n/a_1 \leq \frac{1}{100}$ for all $n > 1$. Thus, if a single pure sine wave is used to modulate the transmitter, each harmonic appearing at the receiver output should be a minimum of 40 db below the fundamental. If two pure sinusoids are summed and used as the modulation input (two tone test), a more complex relationship exists between the fundamental component and the cross-modulation products in terms of the a_n. The harmonics of each of the two tones should, however, still be 40 db below their respective fundamentals to meet the 1% linearity requirement. Therefore, the two tone test results outlined in Section 3 of this report, relate the 1 percent dynamic linearity and intermodulation components as described.

Aside from the design plan deviations listed, the F. M. Receiver playback and record system was modified to utilize the predetection playback and record down-converter and up-converter provided in the P. M. Receiver. This arrangement avoided duplication of hardware.

2.5 LINEAR S/N SUMMER

The Linear S/N Summer was fabricated and tested during Phase I of the RF Test Console project. Results of the Phase I tests were reported in the Phase I Final Report, Appendices B and C, "Linear Signal/Noise Summer" and "Linear Signal/Noise Spectral Density Test". The Signal/Noise Summer specifications and test results are repeated in this report.

The S/N Summer Specifications are listed in Table 2.5.1 and a block diagram is shown in figure 2.5.1.

The Phase I test results indicated that the unit's noise amplifier response is sensitive to ambient temperature variations. Therefore, in Phase 11, the noise amplifier and noise filter were packaged in an oven. Further, the other Summer components were mounted in one of the Test Console cabinets.

The Phase II activity included retuning the noise amplifier at the oven temperature and measurement of the amplifier response as a function of AGC control current at rated oven temperatures. The wideband and narrow band noise filter 3 db bandwidths were accurately measured. Further, the maximum Summer carrier and noise power output levels were measured as a function of carrier input from the transmitters. The results of the Phase II test activity are included in Section 3.4 of this report.

Table 2.5.1. Linear Signal/Noise Summer Specifications

1.	S/N Dynamic Range	0 to 100 db (+30 db to -70 db)
2.	Absolute Accuracy	±.3 db over 4 Hour Period
3.	S/N Ratio Repeatability	±.05 db over 4 Hour Period
4.	Precision Noise and Signal Attenuators	Resolution of 0.1 db with ±0.1 db uncertainty
5.	Power Monitor	Resolution better than .05 db with ±.1 db uncertainty
6.	Noise Power Stability	Resolution of 0.1 db with ±0.1 db uncertainty
7.	Noise Bandwidth	46 to 54 Mc ±.05 db
8.	Noise Amplitude	Linear up to 5 σVRMS
9.	Noise Power Spectral Density	Constant within ±.05 db from 48 Mc to 52 Mc

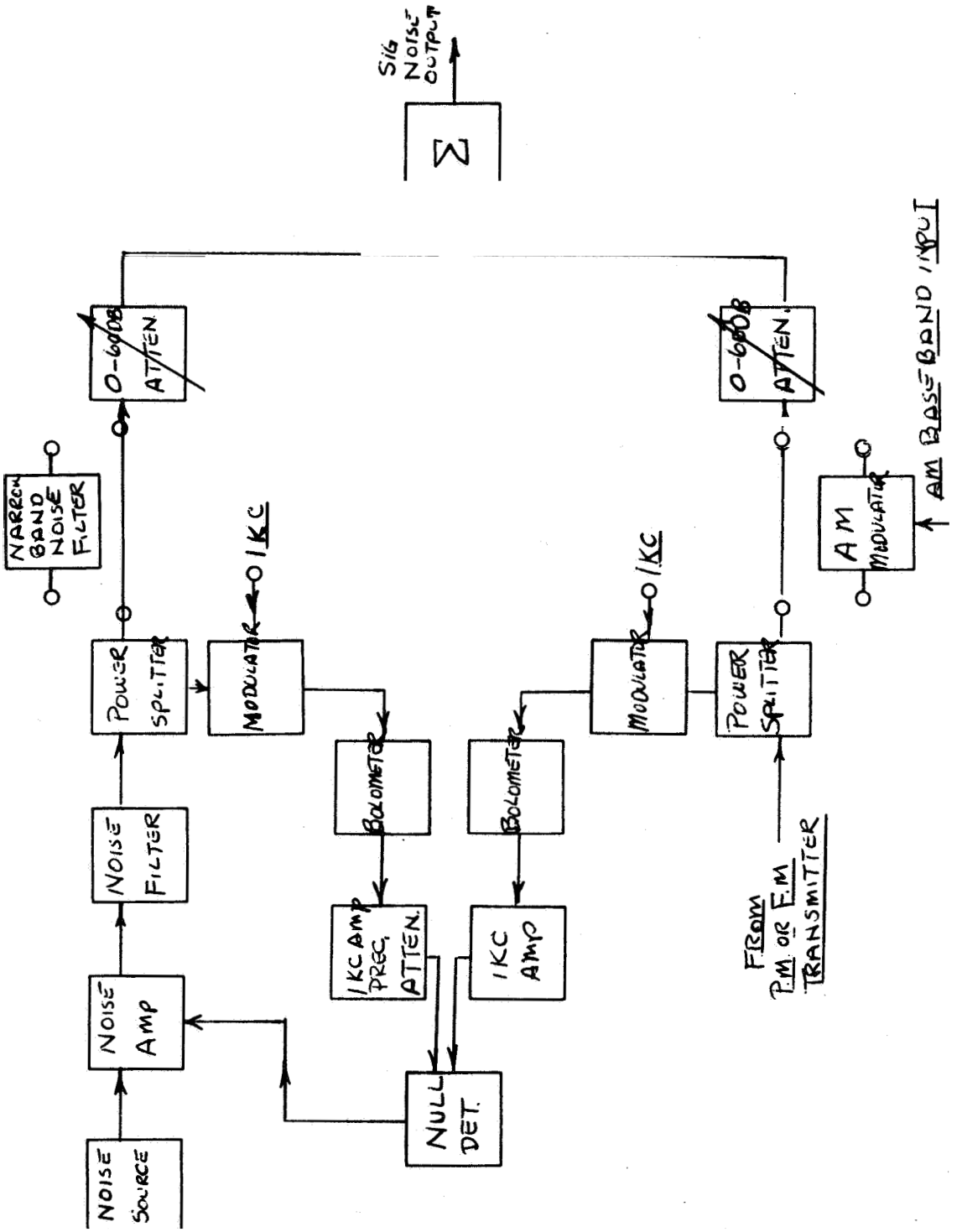


Figure 2.5.1. Block Diagram Signal/Noise Summer

2.6 PHASE NOISE AND TEST INSTRUMENTATION

Figure 2.6.1 is a simplified block diagram of the Phase Noise and Test instrumentation. The narrow band I-F amplifier is specified to exhibit the same amplitude and phase characteristics as the P.M. Receiver narrow band I-F amplifier. The Phase Shifter is specified to operate at 10 Mc and to provide a continuously variable phase shift from 0 to 360 degrees with a calibrated dial accurate to within ±1 degree over this range.

The original specification and block diagram described in detail the hardware required to limit and linearily phase compare the 10 Mc reference and the 10 Mc carrier contaminated with VCO phase noise. However, as shown in figure 2.6.1, the system was considerably improved and simplified by substituting the Hewlett Packard Vector Voltmeter for most of the hardware originally planned. Briefly, this device samples both the 10 Mc reference and 10 Mc spectrum and provides audio (20 Kc) outputs that retain the original 10 Mc phase and amplitude information well beyond the 2 Kc bandwidth of the narrow band I-F amplifier. The obvious advantage of this technique is that the 10 Mc signals are linearily phased detected at 20 Kc rather than 10 Mc. Further, the 20 Kc linear phase detector (set, reset, flip flop) exhibits a linear transfer of output voltage to input phase over a range that extends from nearly $-\pi$ to $+\pi$. The latter advantage precludes the binary dividers (before the phase detector) originally planned.

In summary, the portion of the original specification that is pertinent includes the linearity and range of the 20 Kc linear phase detector. This characteristic is outlined in Section 3.5 of this report.

In addition to comniercial test equipment, a means of measuring the P.M. Transmitter carrier suppression is provided and is outlined in figure 2.6.1. This system includes a 50 Mc precision phase shifter with the same characteristics as the 10 Mc unit outlined earlier. The carrier component is converted to a D.C. voltage and the polarity of the carrier is retained by the coherent detector enabling the system operator to accurately compare the D.C. output to the normalized Bessel carrier coefficient.

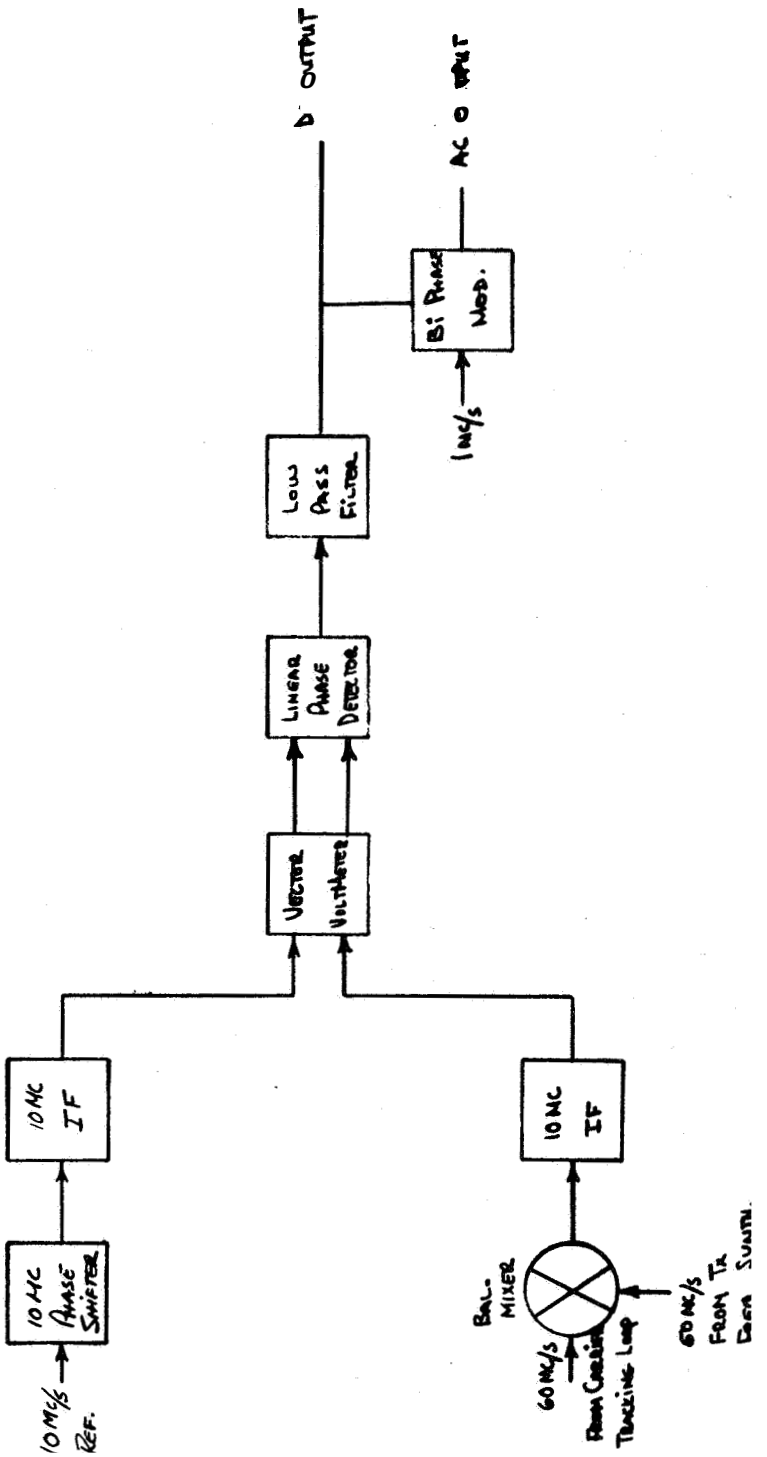


Figure 2.6.1. Block Diagram Phase Noise Instrumentation

3.0 TECHNICAL DESCRIPTION AND CORRELATION OF DESIGN PLAN AND PERFORMANCE

Section two of this report included a brief review of each Subsystem design plan outlined in Phase I. Deviations from the design plan were summarized and the contractual specifications listed. This section of the report includes detailed deviations from the design plan, design data and test results.

3.1 FREQUENCY SYNTHESIZERS

The basic synthesizer modules are common to both the transmitter and receiver frequency synthesizers. For example, the basic transistor multiplier is used in both subsystems. Hence, the design details are listed once; however, all test data is included.

3.1.1 Transmitter Frequency Synthesizer

Figure 3.2.1.1 presents a block diagram of the Transmitter Frequency Synthesizer. The logic of the synthesizer has been modified from the Phase I design plan as follows:

1. The 65 and 55 Mc references for predetection record and playback have been deleted. The reference frequency was changed to 45 Mc and is generated in the receiver synthesizer.

2. The F. M. Transmitter reference frequency was changed from 12.5 Mc to 97.66 Kc.

3. The P. M. Transmitter 350 Mc reference was added, This reference is mixed with the 400 Mc VCO output to form the 50 Mc transmitter carrier. This change was made to utilize a 400 Mc VCO which permitted greater linearity and larger gain $\left[\frac{\text{cycles}}{\text{volt-sec.}}\right]$ to be realized.

4. Originally seven phase lock filters were planned, However, one unit proved adequate by simultaneously switching both the crystals and the reference frequency.

5. The Phase Noise Instrumentation reference was changed from 1 Kc to 1 Mc. This modification was necessary in order to use an improved bi-phase-modulator.

6. The P. M. Transmitter 12.5 Mc reference is generated by dividing 25 Mc by two. This technique avoids the mixing problems of the original system included in the design plan.

3.1.1.1 Transmitter Frequency Synthesizer Module Design.

This section includes module design considerations applicable to the transmitter synthesizer. One of the more important frequency standard parameters is the resonator Q. This must be of sufficient magnitude to yield a stability of 2.8 parts in 10" referenced to a 1 sec. integration time. The short term frequency stability is determined by noise generated in the oscillator.

There are two principal sources of crystal oscillator phase noise or short term instability: the crystal and the sustaining circuit. The equivalent circuit of a crystal is either a series resonant circuit or parallel resonant circuit depending on the crystal load. For either case, the circuit resistance can be represented by a series resistance which constitutes the crystal's equivalent noise resistance. The short term instability attributed to the resultant noise is expressed by equation 1.

$$\frac{\Delta f}{f} = \frac{2\pi \; E_N}{\tau f_o E_S} \tag{1}$$

E_N = Noise voltage

E_S = Signal voltage developed across the crystal terminals

f_o = Oscillator frequency

τ = Averaging time

$$P_{NOISE} = \frac{E_N^2}{Req} = 4KTB \tag{2}$$

or

$$E_N = \sqrt{4\,KTB\,R_{eq}} \tag{3}$$

$$E_S = \sqrt{P_{signal}\;R_{eq}} \tag{4}$$

$$\frac{\Delta f}{f} = \frac{2\pi}{\tau f_o}\sqrt{\frac{4\,KTB}{P}} \tag{5}$$

$$B = \frac{1}{Q}\,f_o \tag{6}$$

$$\frac{\Delta f}{f} = \frac{2\pi}{\tau}\sqrt{\frac{4\,KT}{P\,Q\,f_o}} \tag{7}$$

P signal = Signal power dissipated in crystal equivalent series resistance

B = crystal bandwidth

K = Boltzman's constant

T = absolute temperature

R_{eq} = crystal equivalent series resistance

Q = crystal storage factor

From equation 7, the short term instability is inversely proportional to the averaging time. Further, a short term stable oscillator must have a large Q and signal drive power. However, higher frequency crystals have a lower Q, therefore the produce of f_o Q is more meaningful. A Bliley BG93A fundamental 1 Mc crystal with the following characteristics was used:

$$Q = (3)\ 10^{+6} \tag{8}$$

$$f_o = (1)\ 10^{+6} \tag{9}$$

$$P = (10)\ 10^{-6} \tag{10}$$

$$T = 350°K \text{ oven temperature} \tag{11}$$

$$\frac{\Delta f}{f} = \frac{2\pi}{\tau} \sqrt{\frac{4 \cdot 1.38 \cdot 10^{-23} \cdot 350}{10^{-5} \cdot 3 \cdot 10^{6} \cdot 10^{6}}} = \frac{1.6 \times 10^{-13}}{\tau} \tag{12}$$

Figure 3.1.1.1.1 indicates a plot of Δf as a function of the averaging time, τ. This is the theoretical limit of short term stability of the oscillator as established by the crystal.

The oscillator sustaining circuit degrades the theoretical performance of the crystal. The major sources of sustaining circuit noise are as follows:

(1) 1/f noise of the transistors
(2) power supply ripple
(3) stray magnetic fields
(4) vibration
(5) loading effects
(6) temperature regulation of the crystal and associated oscillator circuitry.

The latter fault is not usually a problem in dealing with short term stability (long term stability is another matter); however, as outlined earlier, an averaging time beyond 10 seconds is meaningful for $2\ B_{LO}$ or 3.0 cps. Therefore, temperature variations over a 10 second period within the proportionally temperature controlled oven are important.

The reference oscillator sustaining circuit designed is of the form indicated in figure 3.1.1.1.2.

$$E_1 = I Z_1 + (I + I_E)\ Z_2 \tag{13}$$

provided $Z_1 << r_b$ the transistor input impedance. The transistor emitter base voltage is $I Z_1$, the base current $I Z_1/r_b$, and the emitter current becomes:

$$I_E = \frac{B I Z_1}{r_b} \tag{14}$$

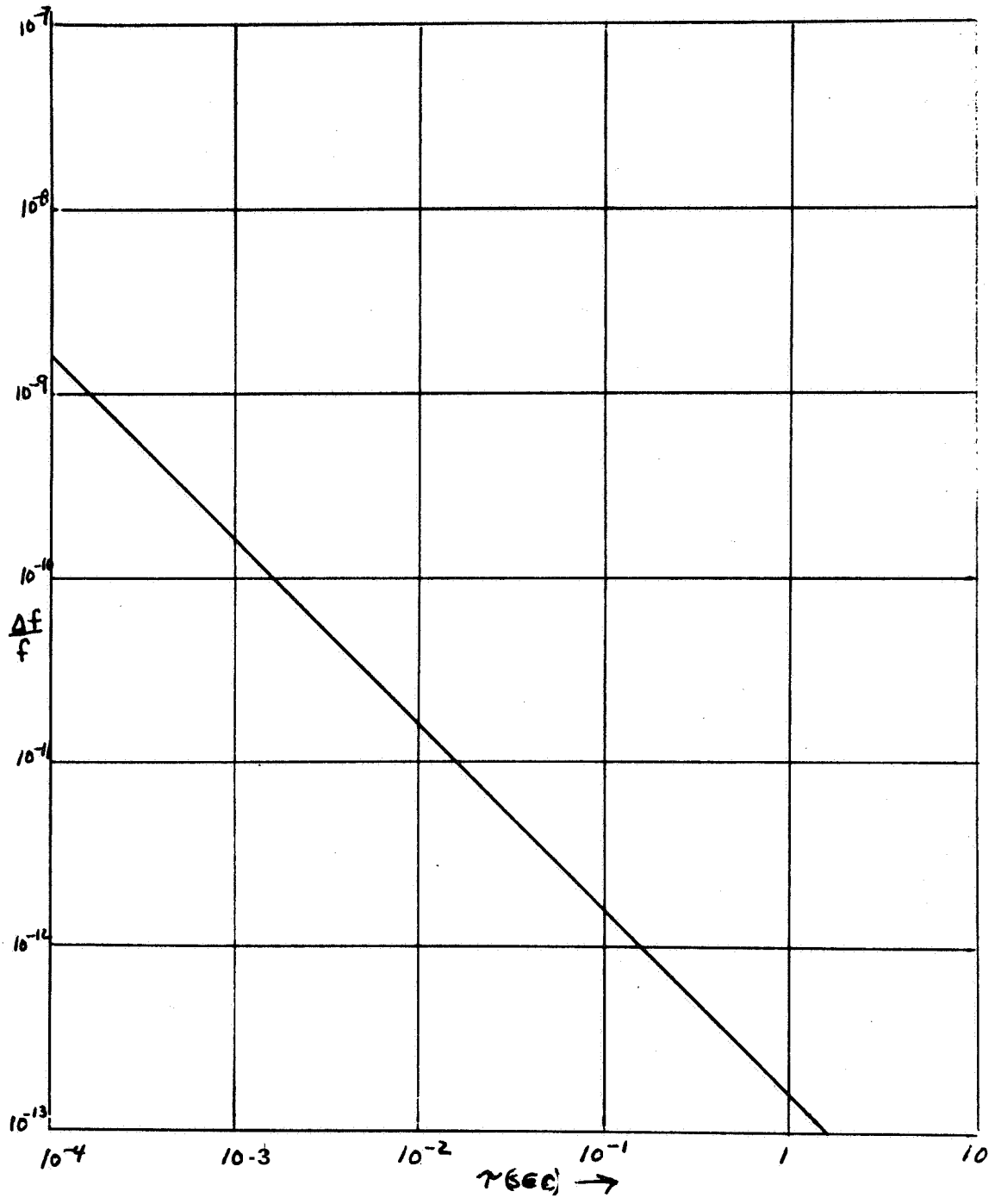


Figure 3.1.1.1.1. Oscillator Characteristic $\frac{\Delta f}{f}$ Vs τ

42

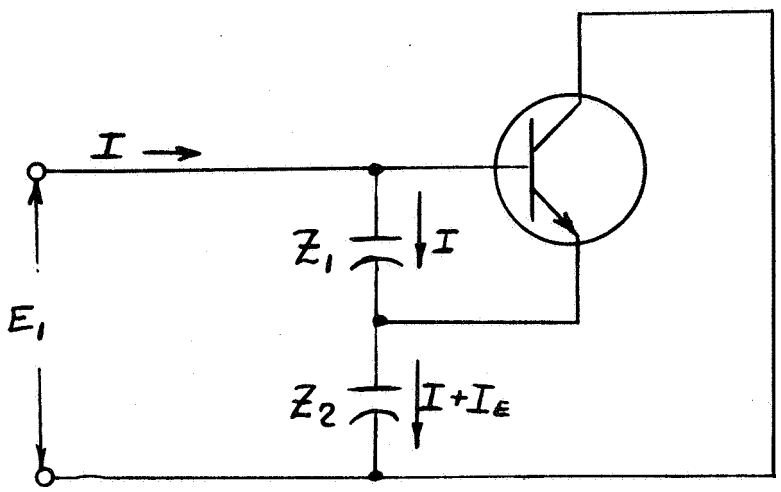


Figure 3.1.1.1.2. Simplified Clapp Oscillator

Substituting equation (14) in (13)

$$E_1 = I Z_1 + I Z_2 + \frac{B I Z_1}{r_b} Z_2 \tag{15}$$

The input impedance becomes:

$$Z_{IN} = \frac{E_1}{I} = Z_1 + Z_2 + \frac{B}{r_b} Z_1 Z_2 \tag{16}$$

If Z_1 and Z_2 are capacitors, equation (16) becomes:

$$Z_{IN} = -j X_{c_1} - j X_{c_2} + \frac{B}{r_b} (-j X_{c_1}) (-j X_{c_2}) \tag{17}$$

$$Z_{IN} = -j X_{c_1} - j X_{c_2} - \frac{B}{r_b} X_{c_1} X_{c_2} \tag{18}$$

Typical circuit values are: $B = 50$, $r_b = 500$, $X_{c_1} = -j10$, $X_{c_2} = -j100$. The latter term of equation (18) represents the negative resistance generated by the sustaining circuit. A crystal (in this case almost series resonant) connected across the input terminals of the sustaining circuit is shown in the equivalent circuit of figure 3.1.1.1.3.

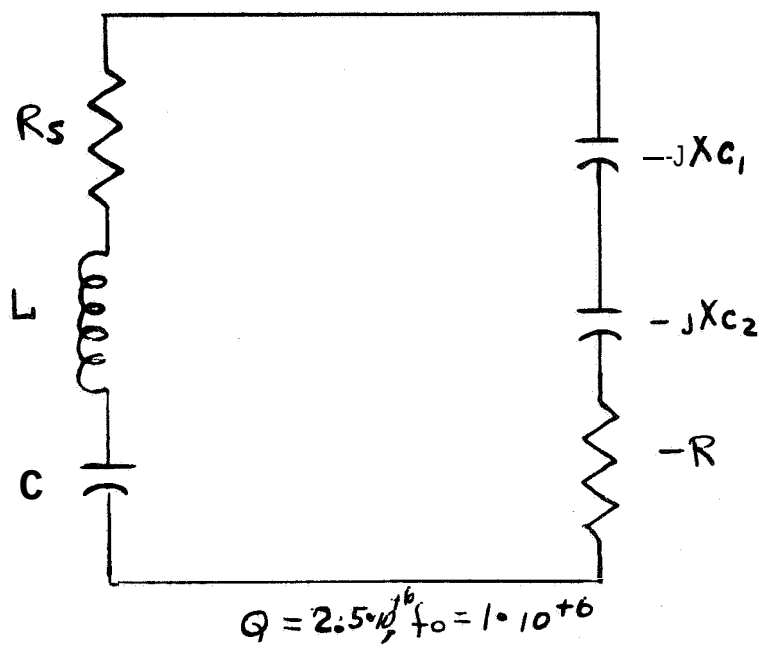


Figure 3.1. 1.1.3. Equivalent Circuit of Crystal and Sustaining Circuit

If the negative resitance of the sustaining circuit is greater than the series resistance of the crystal, the circuit is oscillatory at the crystal's resonant frequency modified by X_{c_1} and X_{c_2}. An inductance whose susceptance cancels the susceptance of X_{c_1} and X_{c_2} is connected in series with the crystal to cancel the detuning of X_{c_1} and X_{c_2}.

The sustaining circuit of a precision oscillator is gain controlled such that the forward gain is linear over the complete cycle of the sinusoid. This is essential as changes in the active devices of the sustaining circuit are never completely decoupled from the crystal. Further, the loop gain control accurately establishes the crystal drive power. A simplified diagram of this system is shown in figure 3.1.1.1.4.

The system is organized such that a portion of the RF output is rectified, filtered and compared against a reference. The resulting D.C. error controls the crystal drive level by modifying the bias point of the sustaining circuit. Unfortunately, transistor input and output admittances are a function of bias (base current). Further the oscillator stability is slightly modified by changes in the sustaining circuit admittances. The system is improved if the AGC system changes the AC loop gain without changing transistor bias levels. A simplified schematic of the reference oscillator is given in figure 3.1.1.1.5.

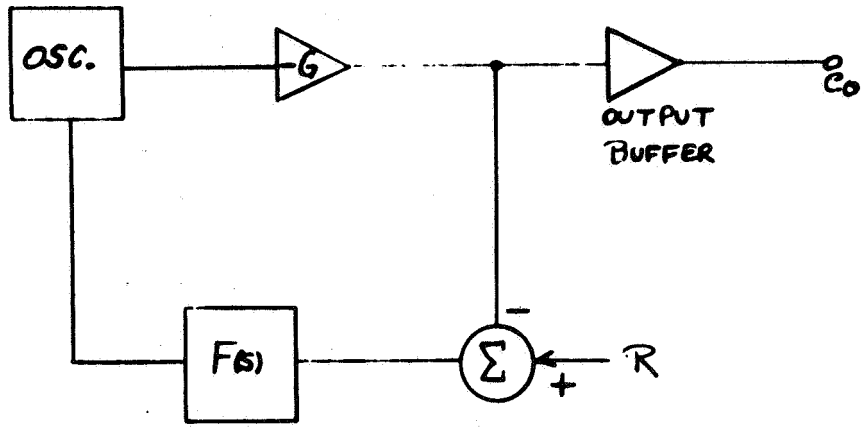


Figure 3. 1. 1. 1.4. Simplified Diagram of Oscillator and AGC System

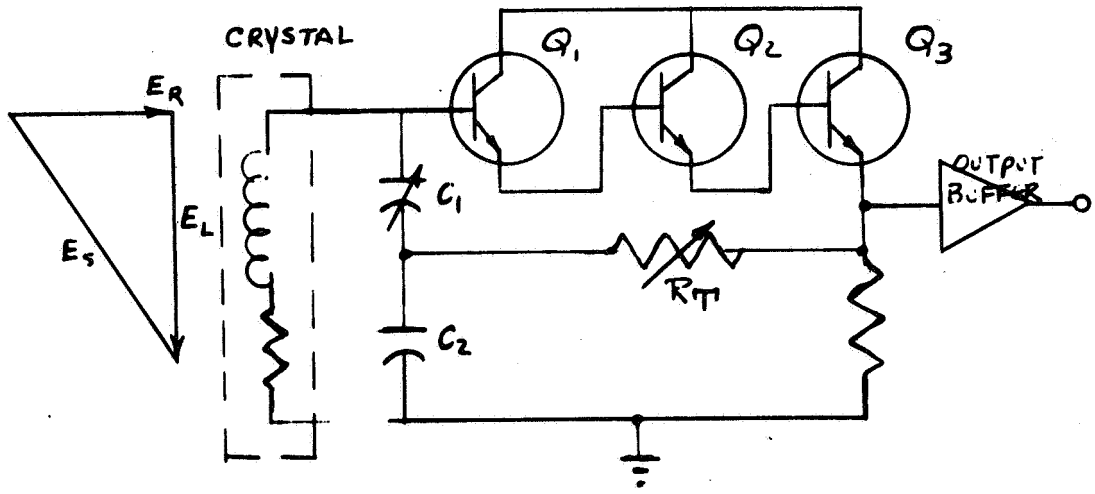


Figure 3. 1. 1. 1. 5. Simplified Reference Oscillator

This arrangement is essentially the same as outlined in figure 3.1.1.1.2 and described by equations (13) through (18). The following modifications are noted: (1) three emitter followers provide increased forward gain ($B_1B_2B_3$) and high input impedance, (2) the crystal is operated slightly off series resonance and its equivalent circuit is a large inductance in series with a small resistor. A thermistor (R_T) regulates the AC loop gain and crystal drive without modifying transistor bias levels. Low noise high frequency transistors minimize sustaining circuit noise. The emitter followers are inherently gain stabilized and resistant to power supply ripple.

The voltage developed across the crystal (E_S) is relatively large, 2 volts p to p. As shown by equation (1), $\frac{\Delta f}{f}$ is inversely proportional to E_S. Further, the crystal heating is acceptable as the principal part of E_S is developed across Leq, figure 3.1.1. 1.5.

The sustaining circuit provides low output impedance; however, three additional output buffers are provided to further isolate the load from the oscillator. The crystal and sustaining circuit are packaged in a proportionally temperature controlled oven whose temperature is regulated at the crystal turning point. This oven in turn is housed in a larger oven although the outer oven is not heated. Since the long term stability requirement is not particularly stringent, it can be met without proportional heat applied to the outer oven.

The reference for the servo system controlling the temperature of the inner oven is obtained from a 10 Kc oscillator. This oscillator couples energy into the 1 Mc output from the frequency standard. The result is that some mixing between the 1 Mc and 10 Kc takes place in the oscillator buffer amplifiers producing 10 Kc sidebands about 1 Mc. These sidebands are on the order of 80 db. below the desired 1 Mc output. A crystal filter with a 3 Kc bandwidth was used to further attenuate these sidebands. The filter was inserted in code 505 although it could have been placed anywhere in the multiplier chain. The code 505 module input was selected for the filter location because a XTAL filter was readily available.

Standard frequency multipliers (codes 505, 508, and 509) employ standard transistor amplifiers that are overdriven. The collector current is rich in harmonics of the input frequency. The collector circuit is tuned to the desired harmonic.

The heart of such a frequency multiplier is the collector tuned circuit or coupling circuit. Each multiplier includes two coupling circuits. The coupling circuit used is shown in figure 3 1 1 1.6.

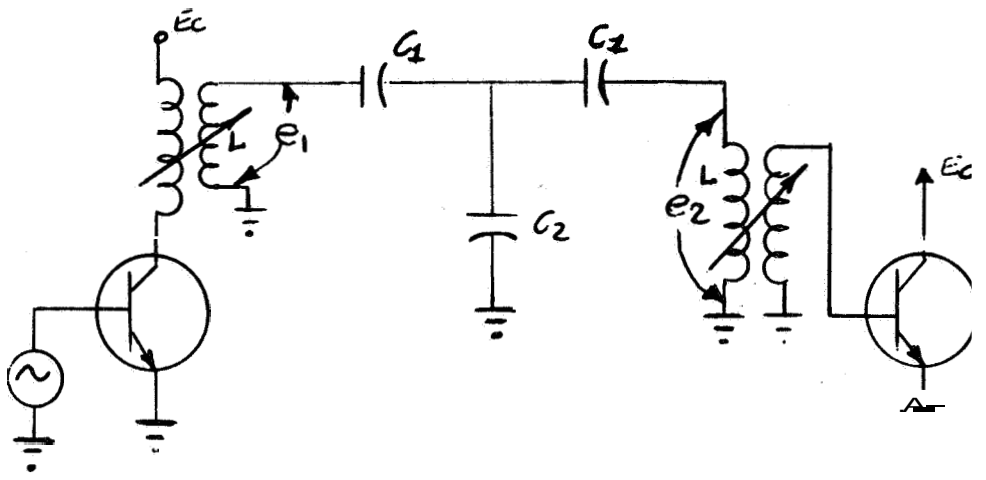


Figure 3.1. 1.1.6. Frequency Multiplier Coupling Circuit

The frequency response of this coupling network is given by equation 19[1]

$$\frac{e_2}{e_1}(f) = \frac{1}{\dfrac{(f-f_o)^2}{\dfrac{(KQ+1)f_o^2}{4Q^2}} + 2j\left(\dfrac{1}{\sqrt{KQ+1}}\right)\dfrac{(f-f_o)}{\dfrac{\sqrt{KQ+1}\ f_o}{2Q}} + 1} \qquad (19)$$

In this expression, f_o is the center frequency of the tuned circuit, Q is the loaded Q of the inductors, K is the coefficient of coupling ($K = c_1/c_2$), and f is frequency. If $2\pi(f-f_o)$ is replaced by S, and $2\pi f_o$ is replaced by W_o then,

$$\frac{e_2}{e_1}(S) = \frac{}{\dfrac{S^2}{\dfrac{(KQ+1)W_o^2}{4Q^2}} + 2\left(\dfrac{1}{\sqrt{KQ+1}}\right)\dfrac{S}{\dfrac{\sqrt{KQ+1}\ W_o}{2Q}} + 1} \qquad (20)$$

This will be recognized as the reeponse of a 2 pole Butterworth, $F(S) = \dfrac{1}{\dfrac{S^2}{W_n^2} + \dfrac{2\zeta S}{W_n} + 1}$ where

1. Reference Data for Radio Engineers (page 242, Fourth Edition)

$W_n = \sqrt{\frac{(KQ+1)}{2Q}}\, W_o$ and $\varepsilon = 1/\sqrt{KQ+1}$ the response is maximally flat for KQ = 1. With this value of KQ the 3 db bandwidth is given by $BW_{3db} = \sqrt{2}\, f_o/Q$. For the standard multipliers the loaded Q of the inductors is about 25. Thus it will be seen that the ratio of the capacitors is $K = c_1/c_2 = 1/20$. The bandwidth then is given by $BW_{3db} = \sqrt{2}\, f_o/25$. For the 1 to 5 Mc multiplier the bandwidth of each coupling network is: $BW_{3db} = (\sqrt{2})(5 \times 10^6)/25 = 282$ Kc. Each frequency multiplier includes two cascaded coupling networks plus an output matching network. The resultant rejection of multiples of the input frequency for each multiplier is listed in section 3.1.1.2 of this report.

The 50 Mc to 350 Mc multiplier (code 512) utilizes a step recovery diode as a harmonic generator. The diode is driven from a Class A amplifier and loaded with a 350 Mc bandpass filter. The step recovery diode (see figure 3.1.1.1.7) has been analyzed by Krakaner[2], portions of his analysis are listed as follows:

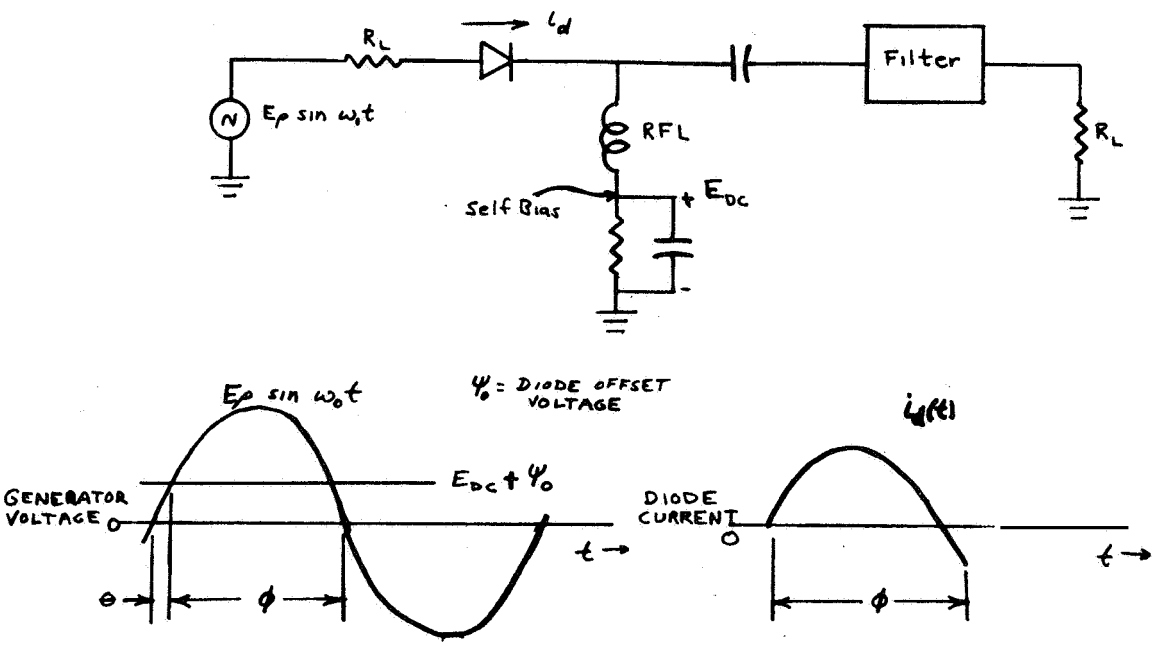


Figure 3.1.1.1.7. Step Recovery Diode Frequency Multiplier Waveforms

2 Harmonic Generation, Rectification and Lifetime Evaluation with the Step Recovery Diode. Proceedings of the IEEE, pp. 1665-1676, July 1962.

The diode current is given by

$$i_d = \frac{E_p}{R_c} \sum_{n=-a}^{00} C_n \; e^{J n W_o T}$$

For large n (n=7 in this case),

$$C_n = \frac{\sin(\theta + \phi) - \sin\theta}{n}. \quad \text{The quantity } \frac{E_p}{R_c} \left[\sin(\theta - \phi) - \sin\theta\right]$$

is the magnitude of the peak current conduction in the reverse direction. The advantage of using such a diode can be seen upon examining C_n. For the step recovery diode, C_n decreases as 1/n while for other types of harmonic generators C_n decreases as $1/n^2$. The only known exception is the varactor diode. However, multiplication by seven with a varactor diode requires extremely complicated circuitry. Also, varactor multipliers are subject to instabilities resulting from non-linear resonance phenomena. Divider modules (codes 501 and 510) utilize available integrated circuit flip-flops with the exception of the high frequency divider (÷ 2) in code 510. The fastest integrated circuit flip flops available were used to minimize time jitter.

3.1.1.2 Test Results

The principal transmitter frequency synthesizer test results include the frequency standard's long, medium and short term stability and the frequency multiplier's relative spurious outputs. The test results of the former parameters are summarized in Table 3.1.1.2.1. The data includes the behavior of both the transmitter frequency standard and the P.M. Receiver Reference oscillator. The test system utilized to measure the data listed is discussed in Section 3.2 of this report.

Table 3.1.1.2.1. Transmitter/Receiver Oscillator Stability Test Data.

$\frac{\Delta f}{f_o}$	(1 minute)	2.3 parts in 10^{-10}
$\frac{\Delta f}{f_o}$	(4 hours)	4.5 parts in 10^{-9}
RMS Phase Noise		0.25° ($2B_{Lo}$=3 cps)

The transmitter oscillator is tunable ± 13 cps at 1 Mc. When multiplied to 50 Mc the frequency variation is ±650 cps. The specification requires ±500 cps variation at 50 Mc.

Table 3.1.1.2.2 lists the spurious outputs of the transmitter frequency synthesizer multipliers relative to the desired outputs.

Table 3.1 1.2.2. Transmitter Frequency Synthesizer Multipliers' Relative Spurious Levels

Code 505 (5-25 Mc)

Frequency (Mc)	Attenuation (db)
5	68
10	70
15	60
20	68
25	0
30	84
35	100
40	100
45	100
50	74
75	93
100	100

Code 508 (1-5 Mc)

Frequency (Mc)	Attenuation (Db)
1	87
2	90
3	90
4	90
5	0
6	90
7	90
8	90
9	90
10	63
15	90
20	90
25	90

Code 509 (25-50 Mc)

Frequency (Mc)	Attenuation (Db)
25	55
50	0
75	94
100	86
125	100
150	100
175	100
200	100

Code 512 (50-350 Mc)

Frequency (Mc)	Attenuation (Db)
50	60
100	70
150	70
200	70
250	70
300	70
350	0
400	70

3.1.2 Receiver Frequency Synthesizer

Figure 2.2.2.1 presents the Receiver Frequency Synthesizer block diagram. The following changes were made as contrasted with the Phase I Design Plan. The frequency of the reference oscillator was changed from 1 Mc to 5 Mc. This change deleted a 1 to 5 Mc frequency multiplier. Further, a commercial 5 Mc oscillator (General Radio Type 115-B) with suitable short and long term stability was available. The center frequency of this oscillator can be varied approximately one half cps; however, there is no practical

reason for a larger variation since the transmitter standard and P. M. Receiver xtal VCO are variable at least ±500 cps (at the carrier frequency). In addition to this change, the 40 Mc output originally planned (for predetection record and playback) was changed to 45 Mc. The latter change simplified the predetection up and down conversion.

3.1.2.1 Receiver Frequency Synthesizer Module Design.

The receiver synthesizer design makes use of the basic frequency multiplier discussed earlier. The input and output frequencies differ slightly; however, the harmonic generation and interstage filtering is identical to the system described in Section 3. 1. 1. The distribution amplifiers utilized in the receiver synthesizer are simple feedback pairs in which the narrow band output networks match the 50 ohm coaxial lines with the 150 ohm amplifier source impedance.

3.1.2.2 Test Results

The principal receiver synthesizer test results include the frequency multiplier spurious levels relative to the proper output frequency. This data is listed in Table 3. 1.2.2. 1. The short and long term behavior of the synthesizer oscillator contribute to the P. M. Subsystem data discussed in Section 3.2.

Table 3. 1.2.2. 1. Receiver Frequency Synthesizer Multipliers' Relative Spurious Levels

Code 502 (5-10 Mc)		Code 503 (5-15 Mc)	
Frequency (Mc)	Attenuation (Db)	Frequency (Mc)	Attenuation (Db)
5	55	5	78
10	0	10	85
15	94	15	0
20	86	20	80
25	100	25	100
30	100	30	65
35	100	35	100
40	100	40	100

Table 3.1.2.2. 1. Receiver Frequency Synthesizer Multipliers? Relative Spurious Levels (Continued)

Code 506 (15-45 Mc)

Frequency (Mc)	Attenuation (Db)
15	57
30	120
45	0
60	130
75	102
90	78
105	113

3.2 P. M. SUBSYSTEM

The P. M. Subsystem description and design plan were reviewed in Section 2.3. The following section correlates the P. M. Subsystem specifications and test results. Figure 3.2.1, 3.2.2, and 3.2.3 indicate the P. M. Subsystem frequency stability test set and test results. As shown, the frequency stability was determined by measuring the phase drift between the transmitter and receiver reference oscillators. Although the specification pertains to each individual oscillator, one may argue that if the two oscillators are compared and the resulting frequency stability is within the specification, each unit will meet the specification. Further, the oscillators are tested as used in the system and the combined error is more meaningful than a comparison of each individual oscillator with a third standard.

Figure 3. 2. 3A indicates the phase drift of the two oscillators taken over a three hour period. The test was made during the evening when the transients on the primary power lines were minimum. Figure 3. 2. 3B shows the oscillators? relative phase drift over a five hour period during a typical working day. Figure 3. 2. 2A indicates the oscillator's relative phase drift referenced to 1 minute time periods. The data was taken during the evening while figure 3. 2. 2B shows data taken during a typical working period. As shown, the two oscillators exhibit a one minute stability of 2.3 parts in 10^{-10} and a four hour stability of 4.5 parts in 10^{-9}.

The P. M Transmitter Receiver pair phase stability specification is listed in table 2.3.1 as one degree RMS in 2 Blo of 3.0 cps. Initially, verification of 2 Blo of 3.0 cps was necessary. The verification was accomplished as shown in figure 3.2.4. Initially, the limiter suppression was simulated by attenuating the carrier tracking loop phase detector signal input. The loop bandwidth was measured by frequency modulating the Hewlett Packard

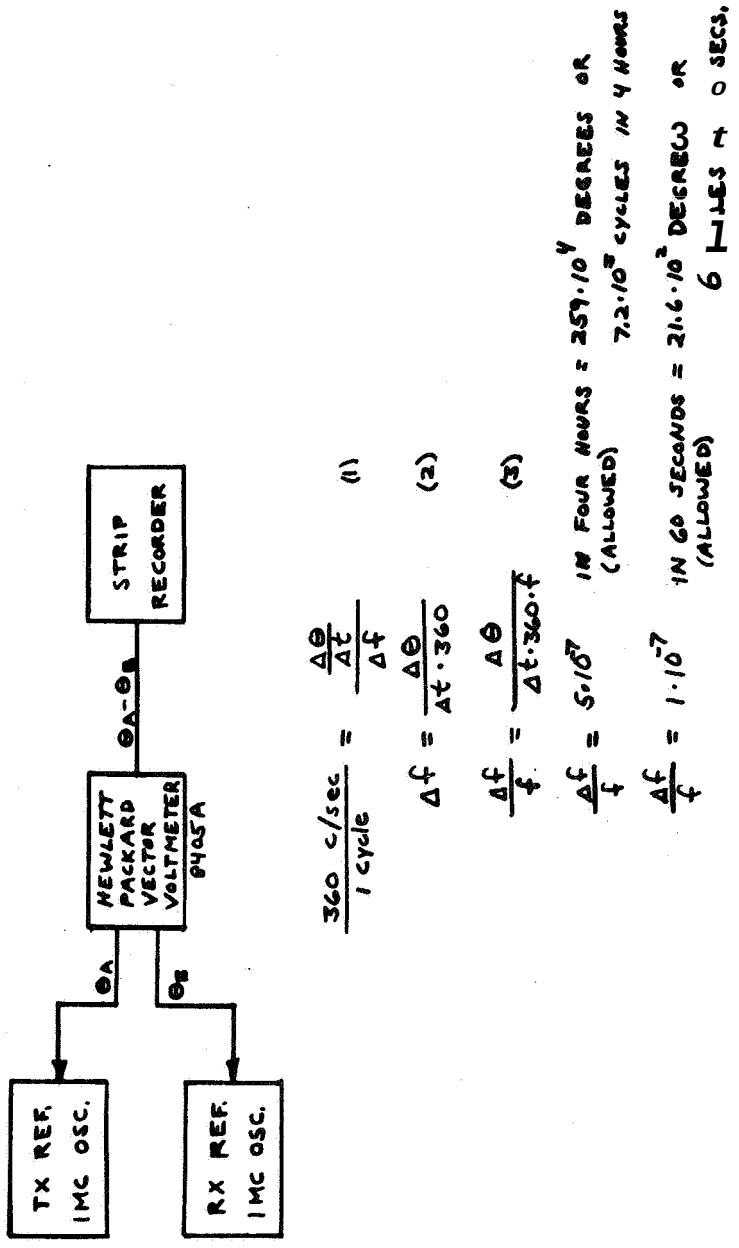


Figure 3. 2. 1. P. M Subsystem Frequency Stability Test System

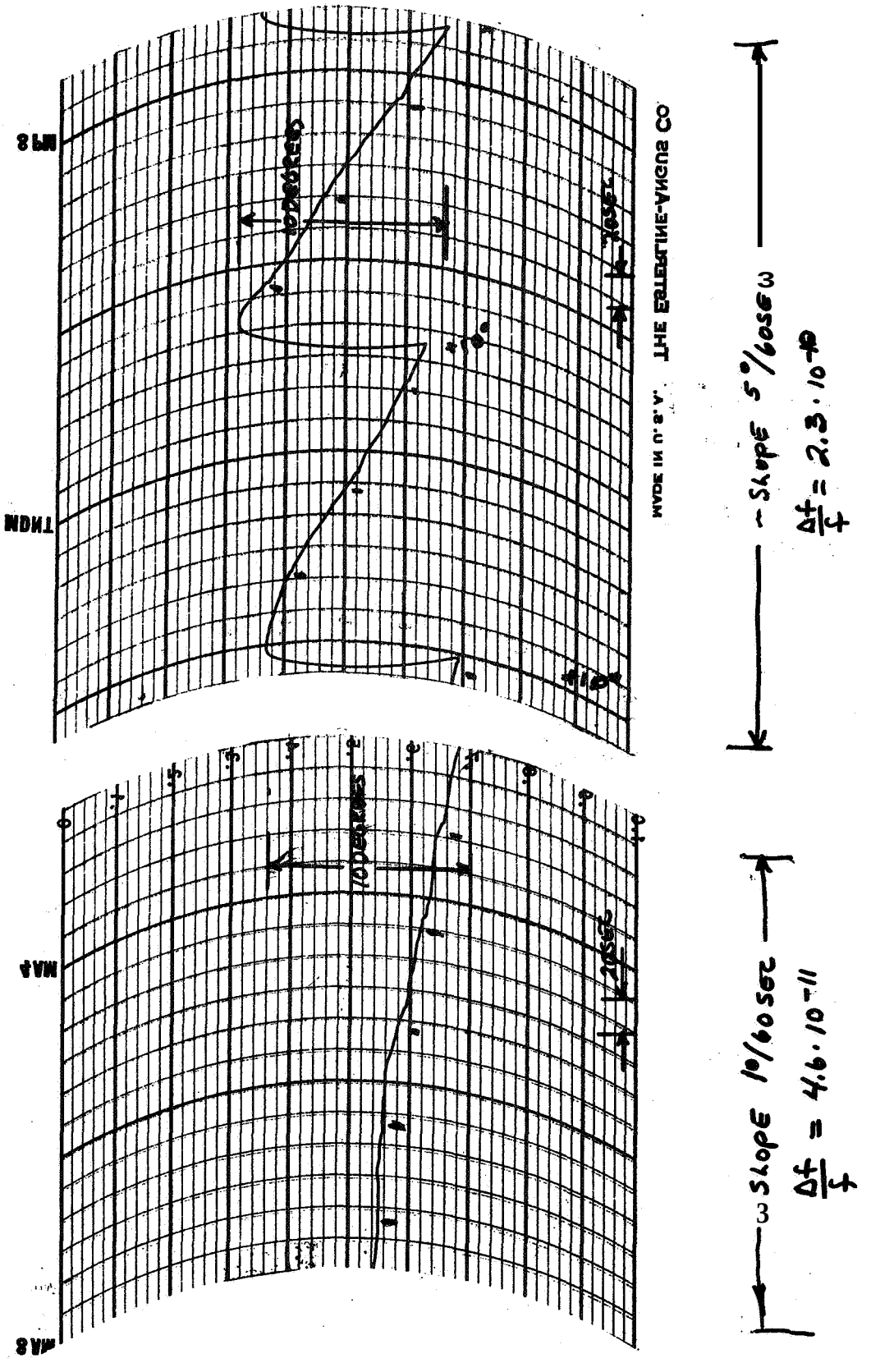


Figure 3.2.2. Frequency Stability Test Results (1 minute)

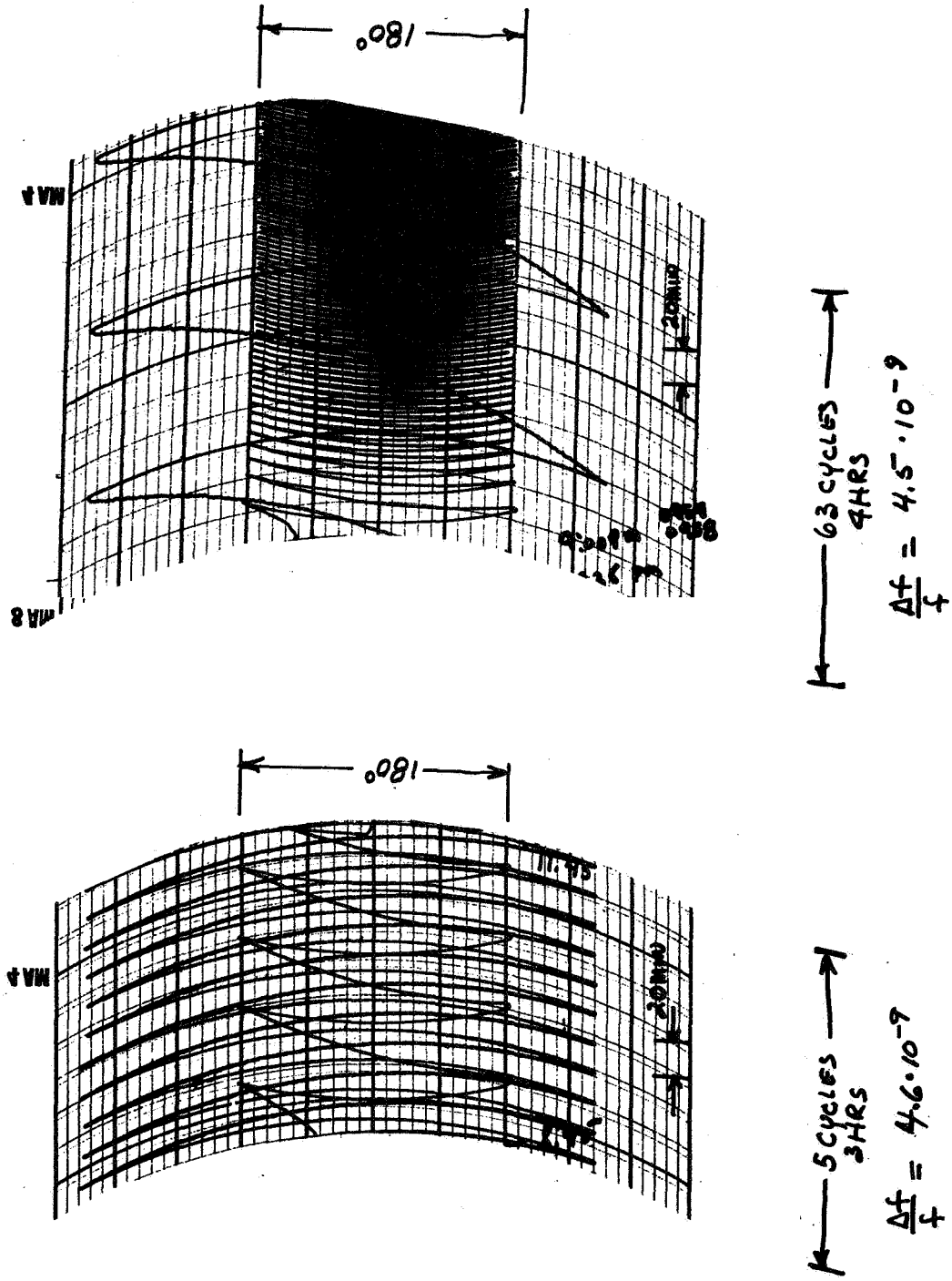


Figure 3.2.3. Frequency Stability Tests Results (4 hours)

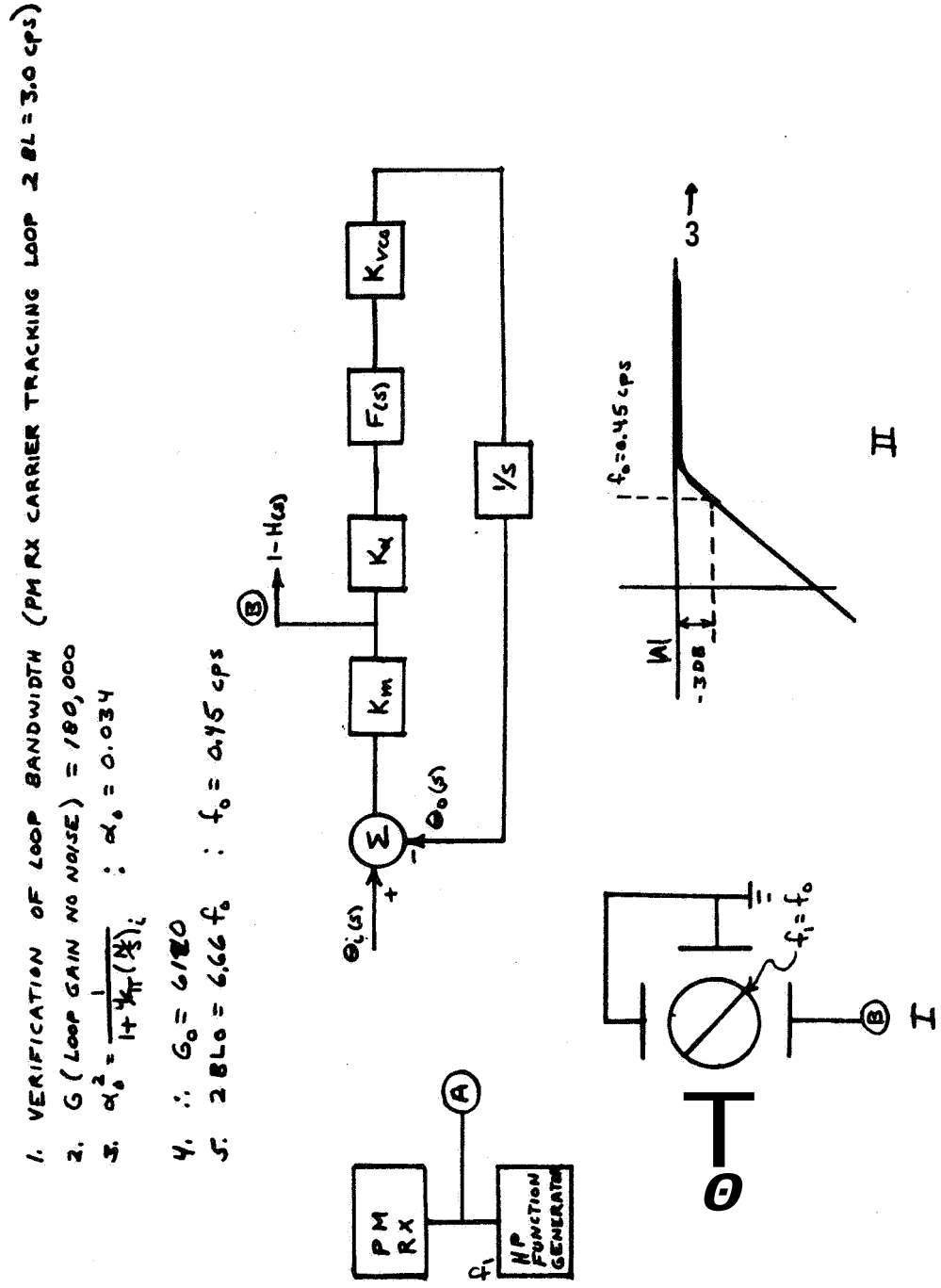


Figure 3.2.4. P. M. Subsystem Phase Stability Test System

Frequency Synthesizer whose output provided the receiver carrier. The phase of the loop error response (1-H (s)) was examined by driving the horizonal and vertical scope inputs with the loop error, e(s), and the modulating frequency f_m. It has been shown[3] that the phase relationship between fm and fo is 180° when fo equals fm. After verification of f_o, the P. M. modulator was connected to the receiver and the carrier tracking loop unlocked. The resulting beat note was measured with a true RMS Voltmeter. The loop was locked and the resulting noise measured. The data shown by figure 3.2.5 indicates that the system residual phase jitter is 0.25 degrees measured in 2Blo of 3.0 cps.

The P. M Subsystem Fidelity specification listed in table 2.3.1 can be interpreted to refer to the transmitter spectrum and the relationship between spurious sidebands and the modulated carrier. It was considered more meaningful to apply the specification to the transmitter/receiver pair by comparing in-band intermodulation products relative to either of two equal tones measured at the receiver output, as the two tones are applied to the P. M. modulator. This technique provides a measure of the transmitter/receiver pair fidelity. In normal operation, the receiver phase demodulator is a non-linear sinusoidal phase detector. The non linearity of this unit masks the system non-linearities; therefore, a linear flip flop phase detector was used as the demodulator as shown in figure 3.2.6. The worst case intermodulation products are listed in figure 3.2.6 for various modulation indices and tone frequencies. Figure 3.2.7 shows the harmonic content of the tone generators used. No doubt the tone generators' spurious contributes to the measured system intermodulation. The data indicates that the intermodulation is worst at higher baseband frequencies. This is expected for two reasons. The non-linearity of the P. M. Modulator phase detector is corrected by loop feedback. However, the correction is a function of frequency; hence the correction is minimum at the loop cut off frequency. Secondly, the P. M Modulator closed loop transfer function of output phase to input baseband was synthesized to approximate a four pole Butterworth response. The Butterworth response exhibits a non-linear phase response near the loop cut off frequency.

3.2.1 P. M. Modulator

The pertinent P. M. Modulator specifications have been listed earlier in this report. A principal specification dictates the amplitude response of the modulator's transfer function of output phase deviation as a function of baseband input $\left[\frac{\Delta\theta_o(s)}{V_m}\right]$, Therefore, a Butterworth response was utilized yielding a maximally flat amplitude response (although a maximally flat group delay constitutes a reasonable choice under different circumstances). However,

3. Reference: JPL TECHNICAL MEMO TM3341-64-2, 22 Oct. 1964. By F. J. Charles

6. B MEASURED WITH TRUE RMS VOLTMETER (NO MODULATION INPUT TO MODULATOR), RX CARRIER TRACKING LOOP UNLOCKED (VOLTMETER BANDWIDTH 2 cps - 500 Kc) BEAT NOTE 100 cps

$E_1 = 3.1$ VOLTS RMS

7. B MEASURED WITH TRUE RMS VOLTMETER, LOOP LOCKED - NO MODULATION.

$E_2 = .0038$ VOLTS RMS

RMS PHASE NOISE : $\frac{E_1}{57.2} = \frac{E_2}{X}$

$X = 0.7°$ RMS

NOTE THIS VALUE OF PHASE JITTER IS TH SAME ON A STRONG AND WEAK SIGNAL

Figure 3.2.5. P.M. Subsystem Phase Stability Test Results

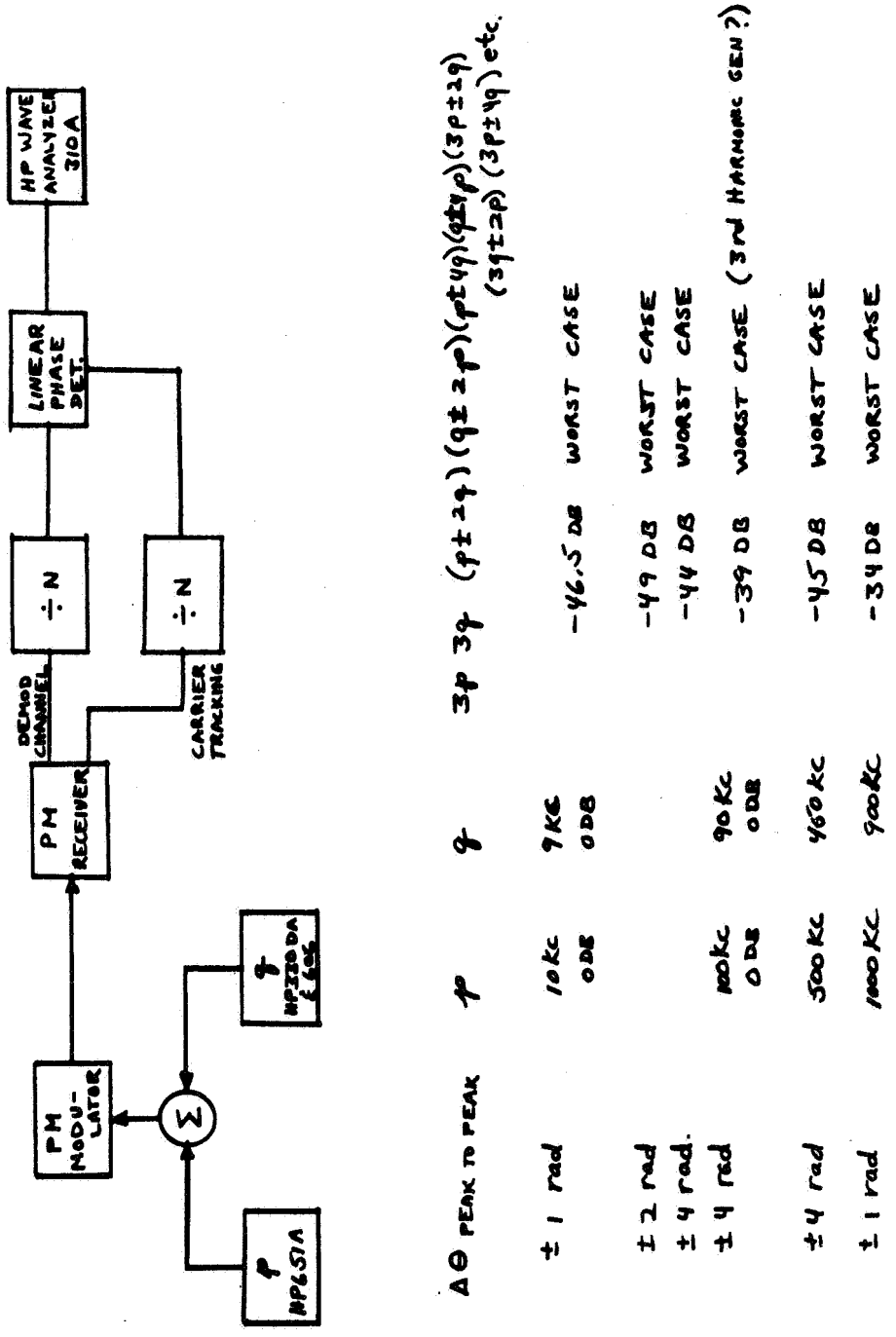


Figure 3.2.6. P.M. Subsystem Fidelity Test System

TONE GENERATOR SPURIOUS DATA

GENERATOR	f	2f	3f	4f	5f	6f
HEWLETT PACKARD 651A	100 KC 0 DB	200 KC -56.5 DB	300 KC -68 DB	400 KC -59.5 DB	500 KC -60 DB	600 KC -63.5 DB
HEWLETT PACKARD 3300A	90 KC 0 DB	180 KC -38.5 DB	270 KC -38.5 DB	360 KC -53 DB	450 KC -48.5 DB	540 KC -63.5 DB
HEWLETT PACKARD 606	450 KC 0 DB	900 KC -50 DB	1350 KC -37.5 DB			

Figure 3.2.7. P. M. Subsystem Fidelity Test System Tone Generator Characteristics

in a practical sense the overall modulator bandwidth (compatible with the amplitude response spec.) was minimized to lessen the influence of loop transport lag. The latter tactic dictates a higher order Butterworth Synthesis.

3.2.1.1 Theoretical Considerations

The simplified block diagram of the locked oscillator phase modulator is shown in figure 3.2.1.1. The linear phase model of the loop is presented in figure 3.2.1.2. As shown in the diagrams the baseband input is injected into the loop in summation with the error voltage. The second loop input θ_r is a phase stable reference derived from the transmitter frequency synthesizer. The behavior of the VCO output phase, $\Delta\theta_o$, as a function of the baseband input, V_m, is:

$$\frac{\Delta\theta_o}{V_m}(s) = \frac{K_a \, K_{vco} \frac{F(s)}{s}}{1 + K_a \, K_m \, K_{vco} \frac{F(s)}{s}} \tag{21}$$

$$\text{Let } K_v = \frac{K_a \, K_d \, K_{vco}}{N} \tag{22}$$

$$\frac{\theta_o}{V_m}(s) = \frac{N}{K_D} \left[\frac{1}{1 + \frac{s}{K_v \, F(s)}} \right] \tag{23}$$

where $\frac{N}{K_D}$ can be considered a constant, independent of frequency.

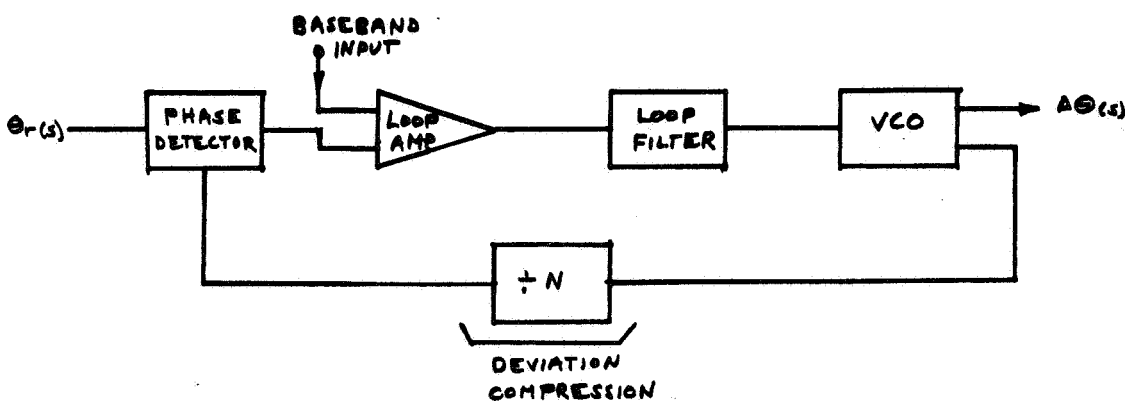


Figure 3.2.1.1. Simplified Block Diagram, Locked Oscillator Phase Modulator

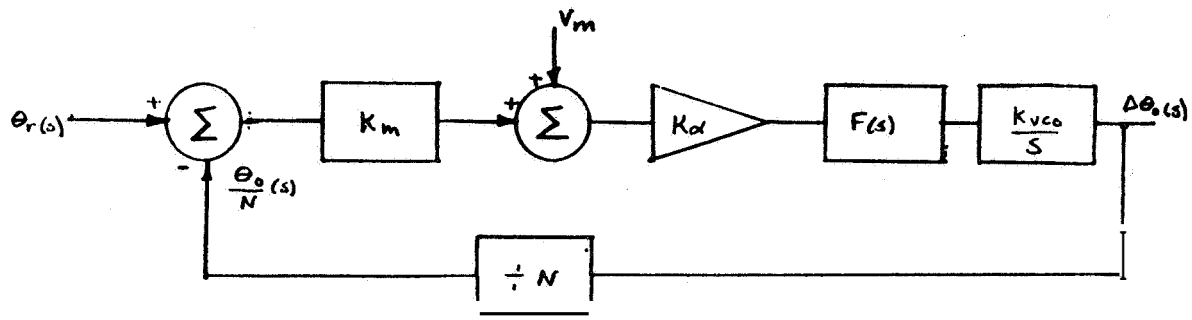


Figure 3.2.1.2. Linear Phase Model, Locked Oscillator Phase Modulator

Therefore, the closed loop transfer function, $\frac{\Delta\theta_o}{V_m}(s)$ is determined by the loop gain and loop filter. The loop gain and loop filter can be designed such that the relationship $\frac{\Delta\theta_o}{V_m}(s)$ exhibits either a Butterworth or Bessel response. The order of the response is established by the proper choice of Kv and F(s). The technique is illustrated by the following 3 pole Butterworth synthesis:

The three pole Butterworth response is characterized in the S plane by 3 poles equally spaced on a semicircle. The intersection of the semicircle and the jW axis is the cut off (3DB) frequency. However, the open loop pole distribution exhibits a pole at the origin plus a complex pole pair contributed by the loop filter. The synthesis technique provides the proper loop gain such that the open loop poles terminate on the semicircle when the loop is closed. The root locus diagram illustrated in figure 3.2.1.3 displays this important feature.

Mathematically, the closed loop response shown in figure 3.2.1.3 is described by equation (24).

$$F_c(s) = \frac{1}{\left(\frac{S}{W_n} + 1\right)\left(\frac{S^2}{W_n^2} + \frac{2\zeta}{W_n} s + 1\right)} \qquad (24)$$

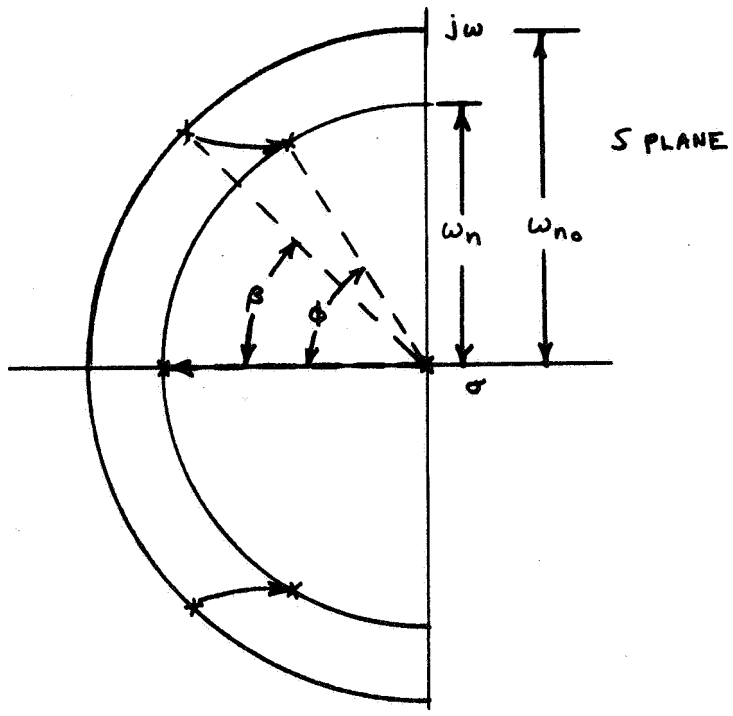


Figure 3.2. 1.3 Root Locus Diagram 3 Pole Butterworth Synthesis

The loop filter's transfer function is (as suggested by Figure 3. 2. 1. 3):

$$F_1(s) = \frac{1}{\left(\frac{s^2}{W_{no}^2} + \frac{2\xi_o}{W_{no}}s+1\right)} \tag{25}$$

Substituting equation (25) in equation (23), it becomes a simple matter to write the clored loop transfer function in terms of open loop parametera. The exprearion indicated by equation (26) rerultr:

$$\frac{\Delta\theta_o}{V_m}(s) = \frac{N}{K_D}\left[\frac{1}{\frac{s^3}{K_v W_{no}^2} + \frac{2\xi_o s^2}{K_v W_{no}} + \frac{s}{K_v} + 1}\right] \tag{26}$$

Equating equations (24) and (26) (recalling that $\frac{N}{K_D}$ is a simple constant) results in the following:

$$\frac{s^3}{W_n^3} + \frac{(2\xi+1)}{W_n^2}s^2 + \frac{(2\xi+1)}{W_n}s + 1 = \frac{s^3}{K_v W_{no}^2} + \frac{2\xi_o}{K_v W_{no}}s^2 + \frac{s}{K_v} + 1 \tag{27}$$

Equating the coefficients of like powers of s and solving for the open loop parameters in terms of the closed loop resonant frequency and damping:

$$K_v = \frac{W_n}{2\xi+1} = \frac{W_n}{2} \tag{28}$$

$$W_{no} = W_n \quad 2\xi+1 = \sqrt{2}\, W_n \tag{29}$$

$$\xi_o = \frac{W_{no}}{2W_n} = \frac{1}{\sqrt{2}} \tag{30}$$

The values of W_n (and the order of the synthesized closed loop response) uniquely determine the open loop parameters. The cut off frequency W_n is selected such that the amplitude response at the upper bound of the baseband spectrum is within the specification. However, the upper bound of the baseband frequency must be much less than the loop reference frequency, fr, to permit the loop filter to discriminate between the baseband and the reference frequency. The latter consideration influences the choice of the loop order and compression factor N.

The previous explanation is intended to clearly outline the synthesis technique. In a practical sense, the modulator built and tested was synthesized to exhibit a fourth order Butterworth response. This precaution was required to minimize the value of W_n and diminish the influence of loop transport lag and still meet the passband specification. The fourth order Butterworth synthesis is a simple extension of the technique outlined earlier and is listed as follows:

The Root Locus Diagram of the fourth order Butterworth is shown in figure **3.2.1.4.**

Mathematically, the closed loop response shown in figure **3.2. 1.4** is described by equation **31.**

$$F_c(s) = \frac{1}{\left(\frac{s^2}{W_n^2} + \frac{2\xi_1}{W_n} s+1\right)\left(\frac{s^2}{W_n^2} + \frac{2\xi_2}{W_n} s+1\right)} \tag{31}$$

The damping coefficients are defined as follows:

$$\xi_1 = \cos\theta_1 = 0.924 \tag{32}$$

$$\xi_2 = \cos\theta_2 = 0.383 \tag{33}$$

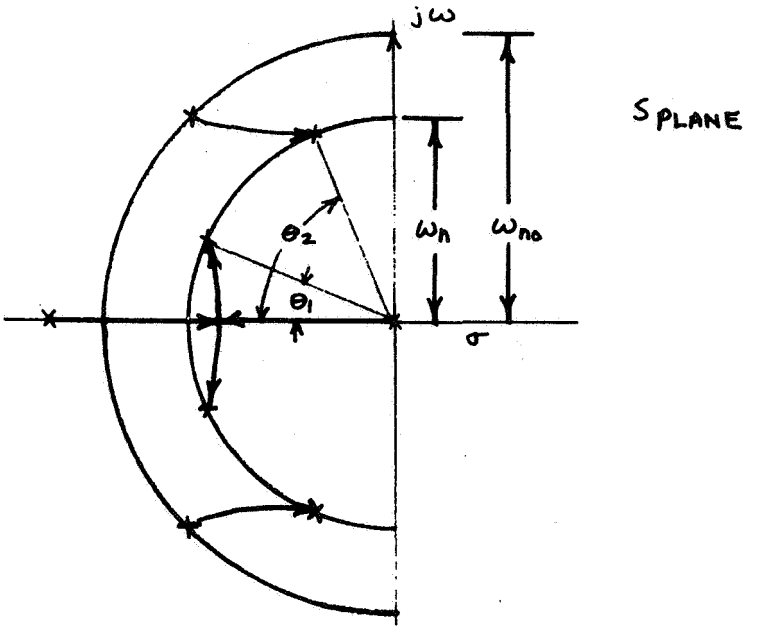


Figure 3, 2, 1, 4, Root Locus Diagram 4 Pole Butterworth Synthesis

Substituting equation (32) and (33) in (31) and expanding, the desired closed loop transfer function becomes:

$$F_c(s) = \frac{1}{\frac{S^4}{W_n^4} + \frac{2.614}{W_n^3} S^3 + \frac{3.42}{W_n^2} S^2 + \frac{2.614}{W_n} S + 1} \tag{34}$$

The loop filter's transfer function is suggested by figure 3, 2, 1, 4 as:

$$F_1(s) = \frac{1}{\left(\frac{S}{W_1} + 1\right)\left(\frac{S^2}{W_{no}^2} + \frac{2\varepsilon_o}{W_n} S + 1\right)} \tag{35}$$

Substituting equation (36) in equation (23) the closed loop transfer function is expressed in terms of the open loop parameters. The following expression results:

$$\frac{\Delta\theta_o}{V_m}(s) = \frac{1}{\frac{S}{K_v}\left(\frac{S}{W_1} + 1\right)\left(\frac{S^2}{W_{no}^2} + \frac{2\varepsilon_o}{W_{no}} s + 1\right) + 1} \tag{36}$$

Expanding equation (36) and equating to equation (34) the following results:

$$\frac{S^4}{K_v W_1 W_{no}^2} + \frac{1}{K_v W_{no}}\left[\frac{1}{W_{no}} + \frac{2\xi_o}{W_1}\right] S^3 + \frac{1}{K_v}\left[\frac{1}{W_1} + \frac{2\xi_o}{W_{no}}\right] S^2 + \frac{S}{K_v} + 1 =$$

$$\frac{S^4}{W_n^4} + \frac{2.614}{W_n^3} S^3 + \frac{3.42}{W_n^2} S^2 + \frac{2.614}{W_n} S + 1 \qquad (37)$$

Equating the coefficients of like powers of S, the open loop parameters are solved in terms of the closed loop cut off frequency and damping coefficients as follows:

$$W_1 = 1.53\, W_n \qquad (38)$$

$$W_{no} = 1.32\, W_n \qquad (39)$$

$$K_v = \frac{W_n}{2.614} \qquad (40)$$

$$\xi_o = 0.422 \qquad (41)$$

3.2.1.1.2 Loop Transport Lag

The loop time delay or transport lag limits the achievable loop bandwidth. The larger the value of W_n (cut off frequency) the greater the influence of transport lag. Its effect, as a function of W_n, is observed as increased closed loop peaking and in the limit instability. The influence of time lag in the loop forward and feedback paths is examined in the following paragraphs.

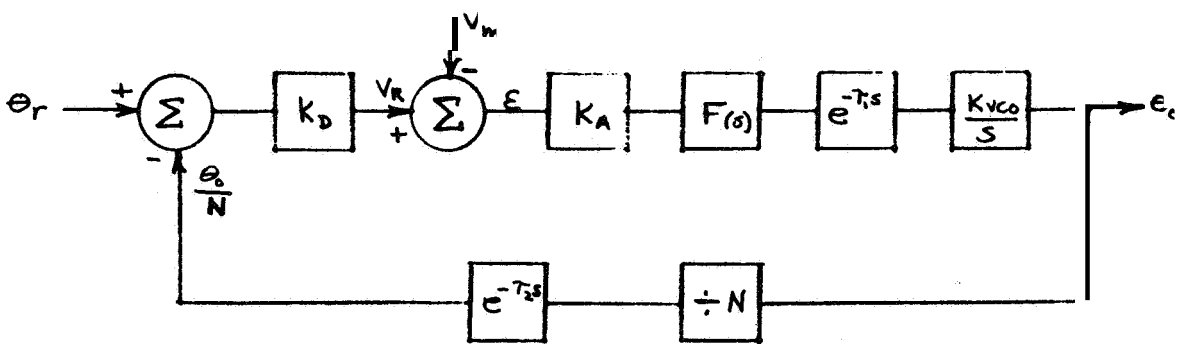


Figure 3.2.1.5. Linearized Phase Model With Transport Lag

The transfer function is developed in detail as follows:

The nodel equation at the second summing point is:

$$V_m - V_R = \varepsilon \tag{42}$$

and

$$E = \frac{\theta_o}{\frac{K_{vco}}{s}\left(e^{-\tau_1 s} F(s) K_A\right)} \tag{43}$$

Therefore

$$V_m - V_R = \frac{\theta_o}{\frac{K_{vco}}{s}\left(e^{-\tau_1 s} F_{(s)} K_A\right)} \tag{44}$$

Also

$$V_R = \frac{\theta_o}{N} e^{-\tau_2 s} K_D \tag{45}$$

Substituting this in equation (44) gives

$$V_m = \frac{\theta_o}{\frac{K_{vco}}{s}\left(e^{-\tau_1 s} F_{(s)} K_A\right)} + \frac{\theta_o}{N} e^{-\tau_2 s} K_D \tag{46}$$

Solving for $\frac{\theta_o}{V_m}(s)$,

$$\frac{\theta_o}{V_m}(s) = \frac{1}{\frac{1}{\frac{K_{vco}}{s} e^{-\tau_1 s} F(s) K_A} + \frac{e^{-\tau_2 s} K_D}{N}} \tag{47}$$

For a 4-pole response

$$F(s) = \frac{1}{\left(\frac{s}{W_1} + 1\right)\left(\frac{s^2}{W_{no}^2} + \frac{2E_o}{W_{no}} s + 1\right)} \tag{48}$$

Substituting F(s) into equation (48) and rearranging to the standard format gives

$$\frac{\theta_o}{V_m}(s) = \frac{N}{K_D}\left[\frac{e^{\tau_2 s}}{1 + e^{(\tau_1 + \tau_2)s} \frac{s}{K_v}\left(\frac{s}{W_1} + 1\right)\left(\frac{s^2}{W_{no}^2} + \frac{2E_o s}{W_{no}} + 1\right)}\right] \tag{49}$$

where:

$$K_v = \frac{K_{vco} K_D K_A}{N} \tag{50}$$

From the above equation it can be seen that it is the total delay $(\tau_1 + \tau_2)$ that affects the loop stability and the amplitude response. The feedback delay τ_2 in the numerator produces a frequency varying phase shift from input to output but does not change the amplitude of the transfer function. Since it is the denominator of the transfer function that determines the stability and amplitude response, the denominator was evaluated on a computer to determine the effects of various time delays $(\tau_1 + \tau_2)$ for a 4 pole Butterworth response with a cut off frequency of 2.0 Mc. Results of this study are shown in figure 3.2.1.6.

A similar analysis was made for a 3 pole Butterworth response with a cut off frequency of 2.5 Mc. The results of that exercise are shown in figure 3.2.1.7.

It should be noted that the 3 pole case requires a 3 db bandwidth of 2.5 Mc and the 4 pole case requires a 3 db bandwidth of 2.0 Mc to achieve the specified amplitude response. Since delay is a linear function of frequency, the wider bandwidth closed loop must have a smaller delay in order to achieve the necessary characteristics. It is estimated that the 4 pole Butterworth synthesis can tolerate 15 nsec. delay and the 3 pole system, 10 nsec. before the resulting peaking forces the amplitude response out of spec. For this reason, the Phase Modulator was designed to exhibit the 4 pole Butterworth response.

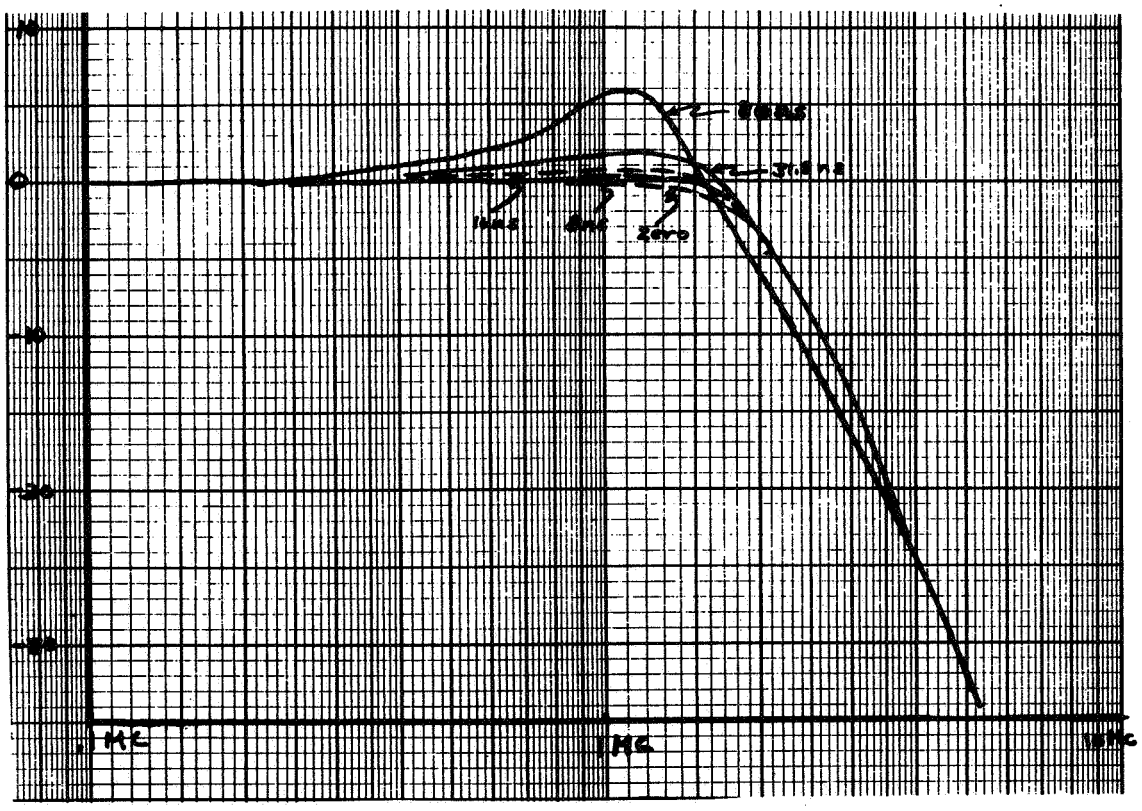


Figure 3.2.1.6. 4 Pole Response With Time Delay $(\tau_1 + \tau_2)$

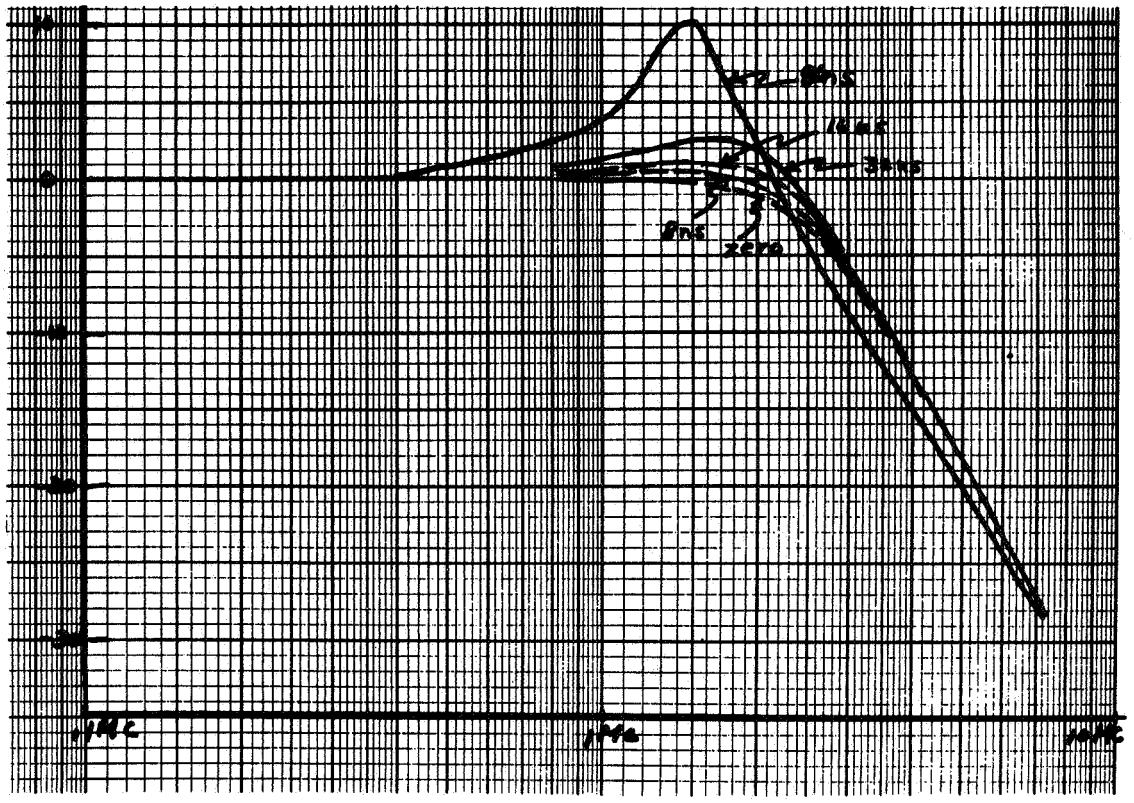


Figure 3.2.1.7. 3 Pole Response With Time Delay $(\tau_1+\tau_2)$

Nomenclature

PARAMETER	DIMENSION	DEFINITION
W_n	Radian/Sec	Closed Loop Cutoff Frequency
W_{no}	Radian/Sec	Complex Pair Open Loop Cutoff Frequency
ε_o		Damping factor of complex pole pair.
K_v	1/Sec	Loop Gain Constant
K_A	volts/volts	Amplifier Gain
Kvco	Radians/volt	VCO Gain
K_D	Volts/Radian	Phase Detector Gain
N		Counter Division Ratio
V_m	Volts	Baseband input

Nomenclature (Continued)

PARAMETER	DIMENSION	DEFINITION
θ_o	Radians	Phase Output Deviation
θ_r	Radians	Reference Phase
W_1	Radians/Sec	Real pole

3.2.1.2 Modulator Design and Test Results

During the Phase I effort the Phase Locked Phase Modulator **was** analyzed and limited experimental effort was expended. However, the modulator **was** essentially a new device and the fabrication was performed in a conservative, logical sequence. Initially a 3 pole Butterworth response was built, with a cut off frequency (f_n) of **200** Kc. This initial design minimized the influence of transport lag and allowed the designer to "separate the variables." Further, the initial design proved the analysis to be valid and provided a basis for the final modulator.

The 3 pole Butterworth synthesis for a cut off frequency of 200 Kc is listed **as** follows:

$$W_v = \frac{W_n}{2} = 6.28 \cdot 10^{+5} \text{ 1/sec} \tag{51}$$

$$W_{no} = \sqrt{2}\, W_n = 1.78 \cdot 10^{+6} \text{ rad/sec} \tag{52}$$

$$E_o = \frac{1}{\sqrt{2}} = 0.707 \tag{53}$$

The loop filter is **of** the form:

$$G_{(s)} = \frac{1}{\frac{s^2}{W_{no}^2} + \frac{2\zeta_o}{W_{no}} s + 1} \tag{54}$$

The loop filter diagram normalized to one ohm and one radian is listed as follows:

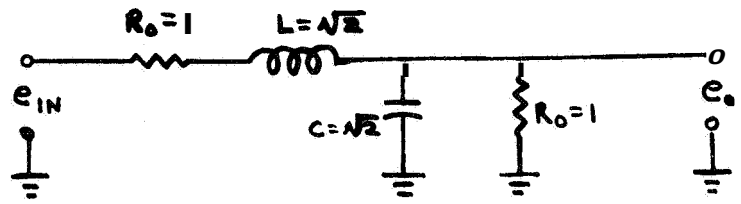


Figure 3.2.1.2.1. Normalized Loop Filter, 3 Pole Butterworth Synthesis

Figure 3.2.1.2.2 presents the experimental data achieved for the 3 Pole Butterworth synthesis.

The loop bandwidth was extended to 500 Kc to experimentally examine the influence of transport lag and the loop amplifier pole. The latter unavoidable pole was initially established at a much higher frequency than the loop cut off frequency and its influence was negligible, However, for a wider bandloop, the loop amplifier gain must be larger and practical limitations on the amplifier gain bandwidth product force the amplifier pole to a lower frequency such that its influence is no longer negligible, Therefore, two loop amplifiers were cascaded to reduce the gain contribution of each and maximize each amplifier's bandwidth. The 500 Kc, 3 Pole Synthesis was mechanized whereby the two loop amplifiers contributed a double pole at 6 Mc. Figure 3.2.1.2.3 indicates the resulting response whereby the amplifiers' poles introduce peaking.

At this point in the Modulator development the tactics were modified. Rather than attempting to make the loop amplifier bandwidth much larger than the loop cut off frequency, it was decided to allow the loop amplifier to contribute a real pole in the synthesis and accept the corresponding gain. The Burr Brown Model 1510 operational amplifier was selected as the loop amplifier for the following reasons, It exhibits a well behaved 6 db/octave roll off closed loop transfer function, $\left[\frac{K}{\left(\frac{s}{W}+1\right)}\right]$ with stated-the-art gain bandwidth product and suitable power capability, Further, the amplifier's drift and noise characteristics are as good as, or better than, comparable units.

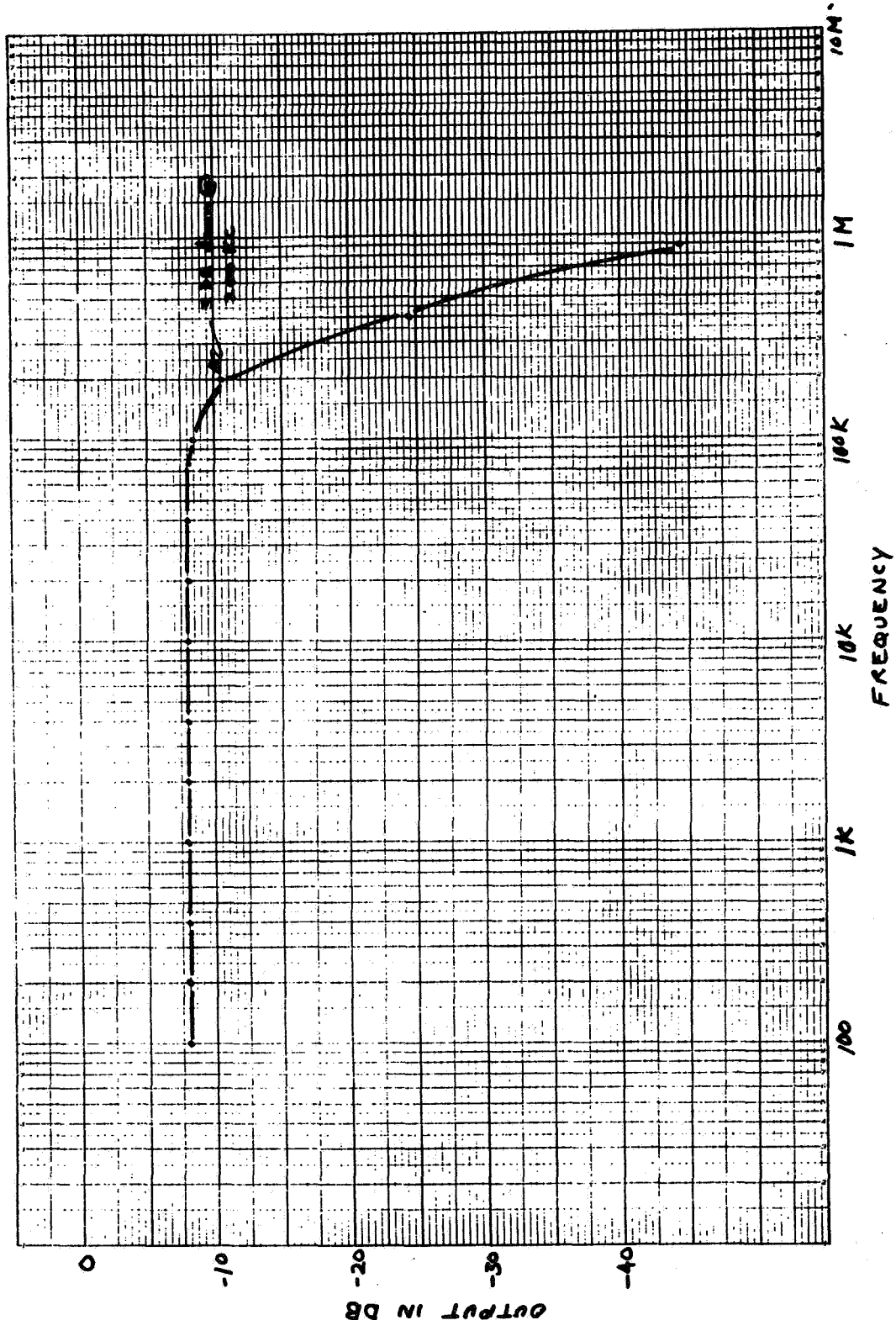


Figure 3.2.1.2.2. Closed Loop Response - 200Kc Bandwidth
3 Pole Butterworth

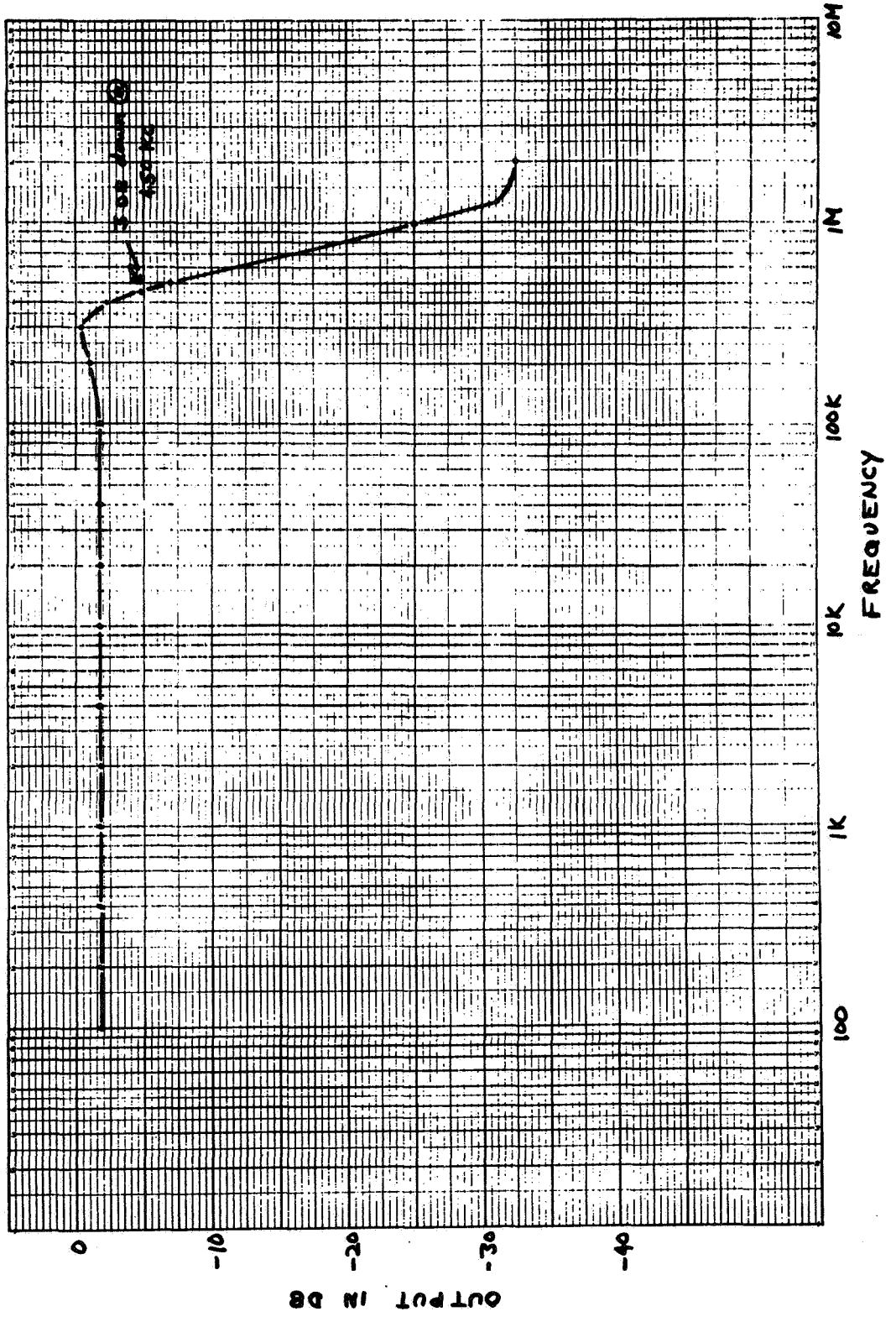


Figure 3. 2. 1. 2. 3. Closed Loop Response - 500 Kc Bandwidth 3 Pole Butterworth

The loop synthesis was changed to a 4 Pole Butterworth to accommodate the loop amplifier's real pole and reduce the effects of transport lag as outlined previously.

The modified loop amplifier application resulted in a fixed amplifier gain and, unfortunately, insufficient loop gain to satisfy the 4 Pole Butterworth synthesis. The phase detector loop gain contribution was maximum; therefore, the VCO gain constituted the remaining variable available to the designer. Initially, the VCO center frequency was designed at the 50 Mc carrier frequency. However, the unit's gain constant and linearity were marginal. Therefore, the VCO was redesigned at 400 Mc and its output mixed with 350 Mc (derived from the transmitter frequency synthesizer) to achieve the 50 Mc carrier. This modification resulted in a larger VCO gain constant and improved linearity. The latter characteristic is self evident if one considers that the ratio of peak frequency deviation to center frequency is less at 400 Mc than at 50 Mc. Admittedly, the short term stability of the system described is degraded by the larger frequency multiplication factor (350 Mc reference); however, this disadvantage was accepted in view of the advantages. The 400 Mc VCO exhibits a gain constant of 1.8 Mc/volt.

The 4 Pole Butterworth loop with a 2.0 Mc cut off frequency was fabricated, whereby the loop amplifier and VCO were organized as described. The influence of transport lag was evident as displayed by peaking in the modulator amplitude response. The transport lag was minimized by minimizing the physical length of the loop (short cables, etc.) and clocking the feedback dividers with the 50 Mc output from the 50 Mc shaping circuit. These efforts yielded a total loop time delay of approximately 30 nanosec. The resulting peaking was minimized by reducing the loop gain slightly from the value dictated by the synthesis resulting in a cut off frequency less than synthesized. The response of the final P. M. Modulator design is shown in figure 3.2.1.2.4. Aside from the difficulties discussed the mixer required to down-convert the 400 Mc to the final 50 Mc carrier contributed its problems. The mixer is, of course, inside the loop and its upper sideband output (750 Mc) produced variations in the zero crossings of the feedback divider resulting in distortion in the recovered baseband. This problem was solved by including a low pass filter after the loop mixer. The filter was designed to exhibit a linear phase response and flat amplitude response in the region 45-55 Mc while contributing 3.5 nanosec. of time lag and at least 40 db attenuation to the 750 Mc spectrum. These requirements dictated a 3 Pole Butterworth low pass filter with a 100 Mc cut off frequency.

Aside from the frequency response and deviation linearity, the P. M. Modulator specifications include a phase deviation capability of 13.0 radians from D. C. to 500 Kc and ±1.0 radian from D. C. to 1.5 Mc. The modulator design includes a feedback divider which

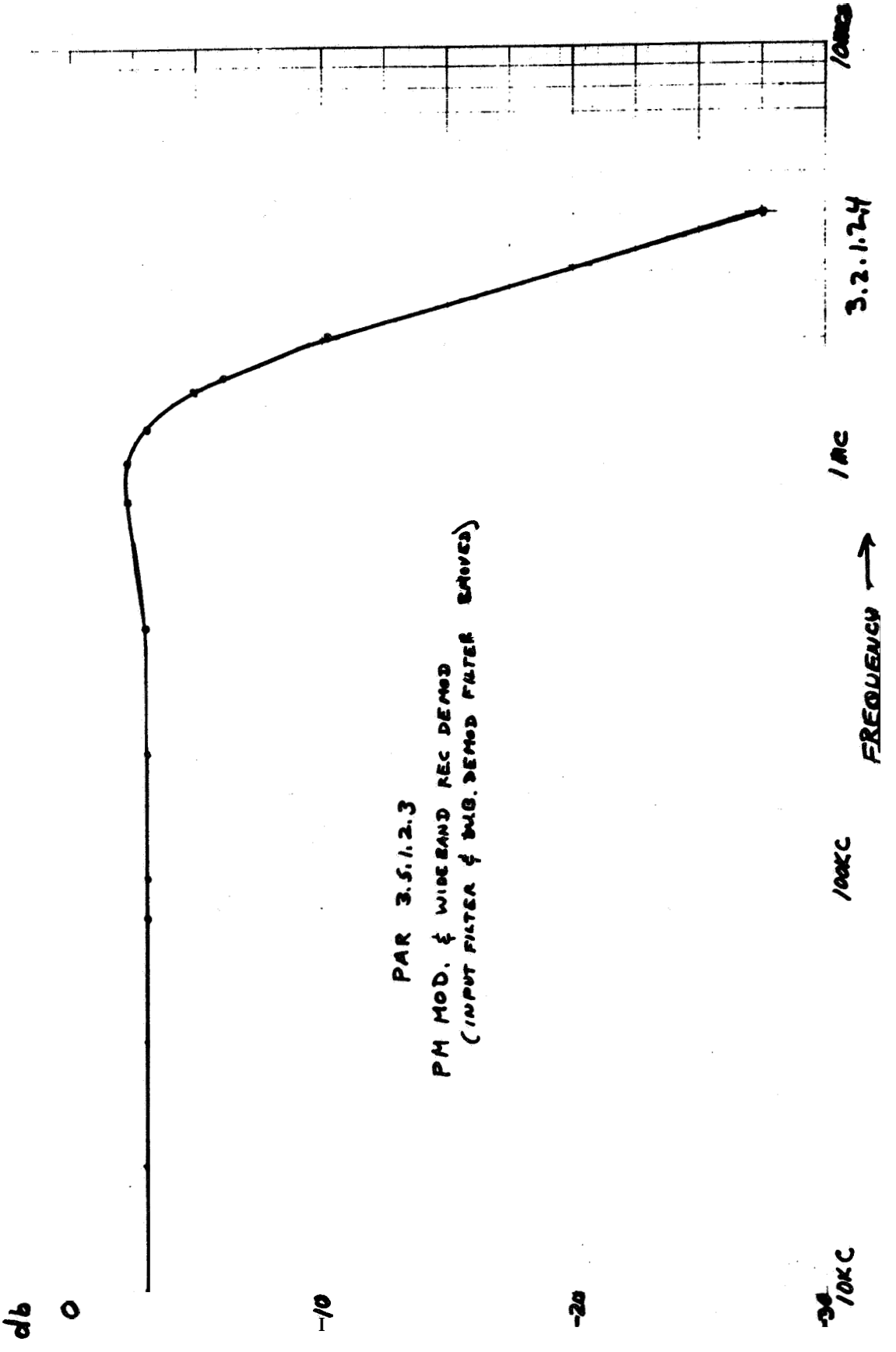


Figure 3. 2. 1. 2. 4. Closed Loop Response 4 Pole Butterworth

compresses the output phase deviation by a factor of four which allows the APC loop to retain lock as the output phase traverses ±4 radians. However, a simple test system which relates the baseband input voltage to the output phase deviation is outlined in figure 3.2.1.2.5. As shown, a tone frequency provides both the transmitter baseband input and the scope horizontal sweep. The scope's vertical input is the P. M. Receiver's demodulated output. This simple system results in a scope display that traces out the receiver's phase detector s curve as a function of the magnitude of the tone generator output.

In turn the operator can easily relate baseband input voltage to output phase deviation. The test system outlined in figure 3.2.1.2.5 indicated that the modulator is capable of a peak-to-peak phase modulation of 10 radians.

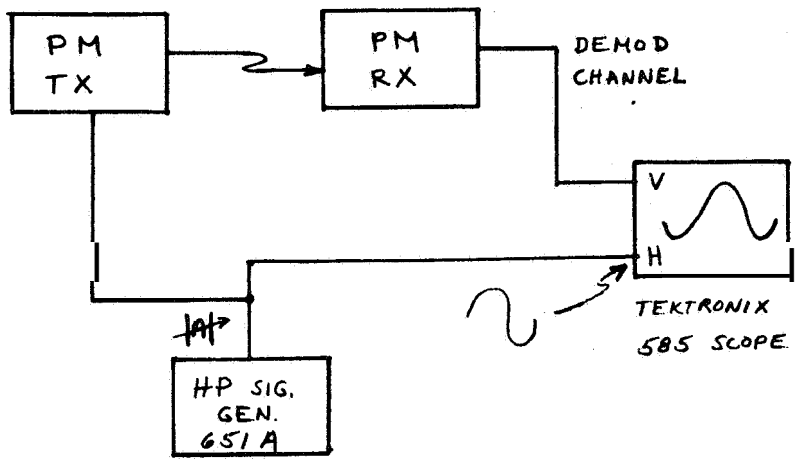


Figure 3.2.1.2.5. P. M. Transmitter Phase Deviation Test System

The R. F. Test Console includes the capability of verifying the modulation index by two additional test systems. The first and second carrier nulls are observed as a function of baseband input. The second includes the carrier suppression test system whereby the carrier component is displayed as a D. C. voltage (with the polarity of the carrier retained). The latter two systems are dependent on the normalized Bessel coefficients as a function of the modulation index.

3.2.1.3 Module Design

The following section includes a design description of the various P. M. Modulator circuits.

76

3.2.1.3. 1 VCO

As outlined earlier, the initial modulator VCO was designed at 50 Mc; however, since the unit was not included in the final system, the design is not included. The 400 Mc VCO design was based on the following considerations.

The transistor model is written in terms of its Y parameters in a linear two port device as shown in figure 3.2.1.3.1.

3.2.1.3.1

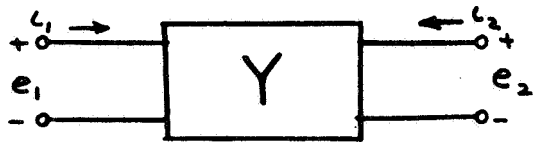


Figure 3, 2, 1, 3, 1, Two Port Network

$$i_1 = y_{11}e_1 - y_{12}e_2 \tag{55}$$

$$i_2 = y_{21}e_1 + y_{22}e_2 \tag{56}$$

A transistor connected in common base and its equivalent two port model is shown in figure 3.2. 1.3. 2.

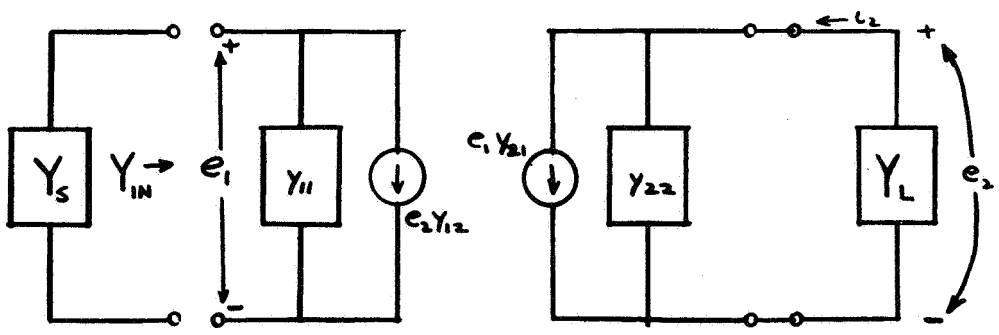


Figure 3.2.1.3.2. Transistor Common Base Two Port Model

The input admittance Y_{in} is:

$$Y_{in} = y_{11} - \frac{y_{12}\, y_{21}}{y_{22}+y_L} = G_{in} \pm jB_{in} \tag{57}$$

It is obvious that if $\frac{y_{12}y_{21}}{y_{22}+Y_L} \geq y_{11}$ such that G_{in} (real part of Y_{in}) is negative the device is potentially unstable. Bahrs(4) has shown that $G_{in} \simeq \frac{1}{g_{11}}\left[g_{11}g_{22} - \frac{M}{2}(1+\cos\theta)\right]$ where $M/\theta = y_{12}y_{21}$. Consider the case where the two port operates between a load and generator such that $G_A = g_{11}+G_s$, $G_B = g_{22}+G_L$. The condition for potential instability is $G_A G_B = M/2$ $(1+\cos\theta)$. In a practical manner this means that if the source and load conductance, G_S and G_L are large, one condition for instability is fulfilled. Further, if the sum of the angles of $(y_{11} + y_{IN})$, exceed the angle of $y_{12}\, y_{21}$ the second condition exists for instability; namely, the proper phase relationship between output and input. Therefore, if the transistor source and load have large conductances and proper susceptances the device is unstable. The connection in figure 3.2. 1 3. 3 fulfills these requirements.

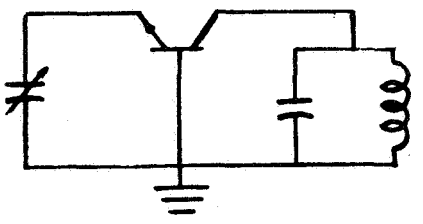


Figure 3.2. 1 3. 3. Basic Oscillator Circuit

A transistor oscillator was designed based on these considerations. The collector tuned circuit is a quarter wave shorted line enclosed in a cavity. The line length was made variable by an adjustable shorting bar. The oscillator is tunable over the band 300-500 Mc. The oscillator was made electronically tunable (VCO), aside from the mechanical tuning, by connecting a varicap across the quarter wave line. The outputs are taken from the cavity by adjustable capacitive probes. The output power is a function of emitter current. A coaxial detector was arranged to measure the oscillator power and an AGC system used to level the output power. Figures 3.2.1. 3. 4 and 3.2.1. 3. 5 are the schematic diagram and $\frac{\Delta f}{V_m}$ transfer.

(4) "Amplifiers Employing Potentially Unstable Units", By George Bahrs, Doctors Thesis, Stanford University, 1956

78

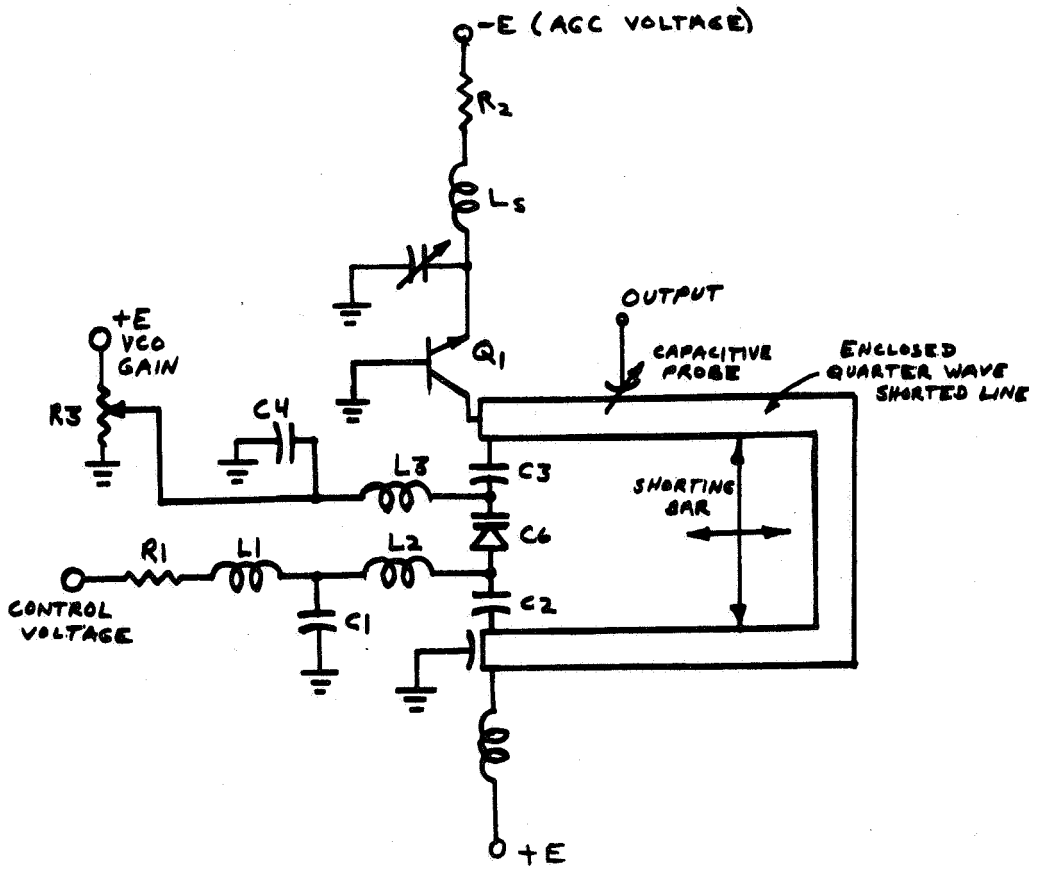


Figure 3. 2. 1. 3. 4. Circuit Diagram 400 Mc VCO

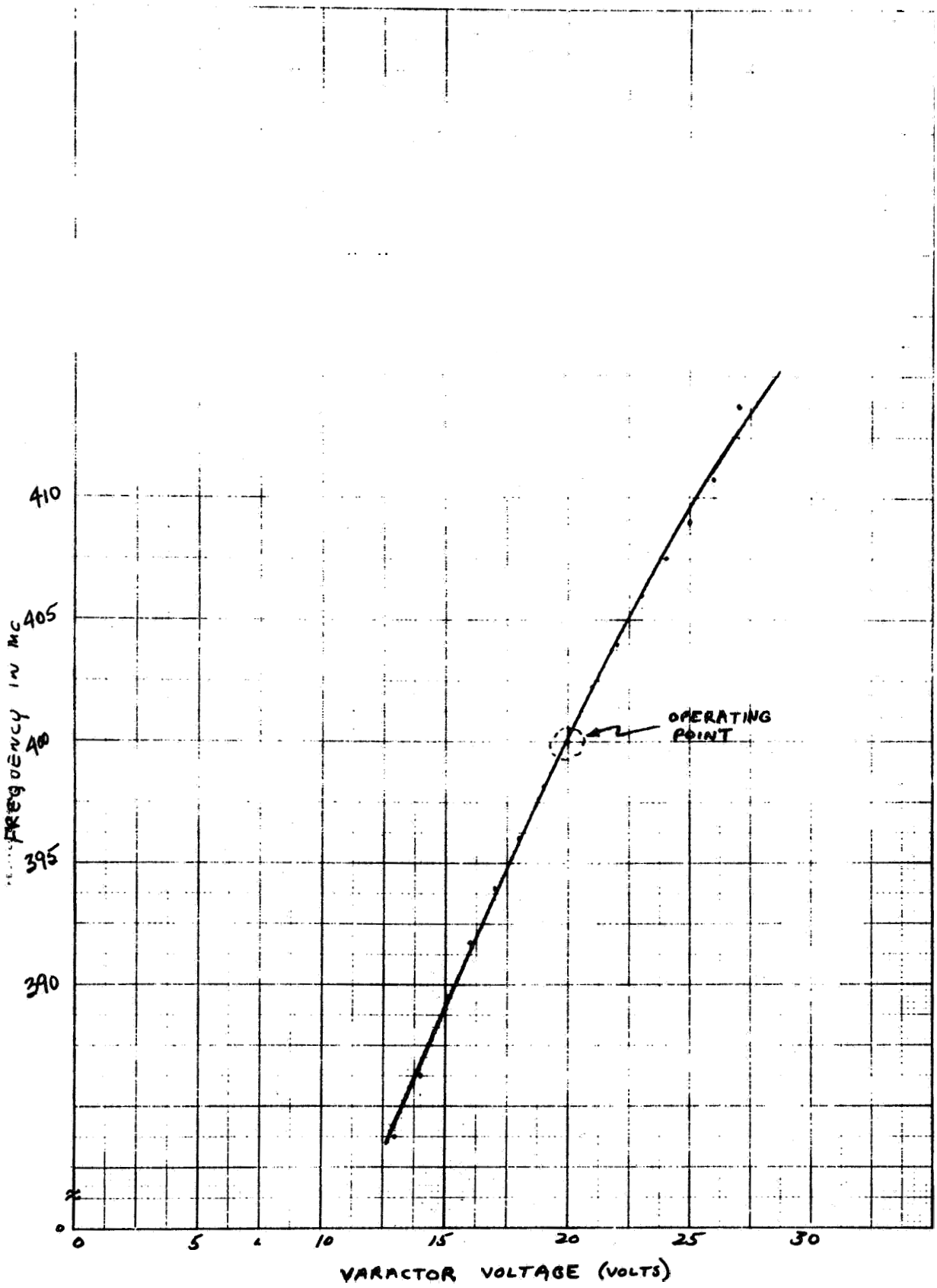


Figure 3.2.1.3.5. 400 Mc VCO Characteristics

80

3.2.1.3.3 High Speed Dividers, Linear Phase Detector, and Loop Amplifier

As outlined earlier, the Modulator carrier frequency is specified as 50 Mc and the peak-to-peak phase deviation is ± 4 radians. Further, a phase deviation compression factor of 4 is included in the feedback path. The latter precaution constrains the phase detector dynamic range to a maximum of ± 1 radian, thus allowing operation over the unit's most linear region. Aside from this feature, the feedback dividers are required to maintain lock at large modulation indices.

A basic, high speed flip-flop was developed to serve as both the dividers and linear phase detector, The units toggle reliably at 50 Mc with sufficiently fast rise and fall times and dwell level times to exhibit a linear sawtooth transfer of output voltage to input pulse position. Initially, a non-saturated current mode switching arrangement was considered. However, this device exhibits a small voltage swing and the resulting phase detector gain constant would be inadequate. Therefore, a more conventional saturated, voltage switching flip-flop was designed. The fastest transistors available (2N 3960, ft = 1.6 Gc) and hot carrier diodes were used to enhance the speed. Each flip-flop (and phase detector) exhibited 6 nanosec. propagation delay and the squaring circuit, 10 nanosec. for a total feedback path delay of 28 nanoseconds. However, the squaring circuit and two dividers were clocked to avoid the delay of the two dividers (at the expense of adding 2 nanosec. gate delay, The logic diagram and truth table of this arrangement is shown in figure 3. 2. 1. 3. 2. 1.

This arrangement yielded 18 nanoseconds time delay. Note from the truth table that the delay thru the two counters is used to advantage. Namely, when both counters are in the "one" state the next clock pulse is propogated thru the gate before the counters can respond.

The digital circuity was packaged compactly whereby a solid copper clad ground plane served as the mounting surface. This subtle precaution was an absolute necessity to achieve the switching speeds referenced. The flip-flop phase detector transfer is shown in figure 3.2. 1 3.2. 2

The loop amplifier was discussed earlier. Figure 3.2.1.3.2. 3 indicates the open loop Bode Diagram of the Burr Brown Model 1510. Although some deviation from a 6 db/octave roll off is evident (attributed to feed forward compensation) the unit exhibited a single pole transfer in closed loop operation. Its closed loop response formed the single real pole in the 4 Pole Butterworth synthesis.

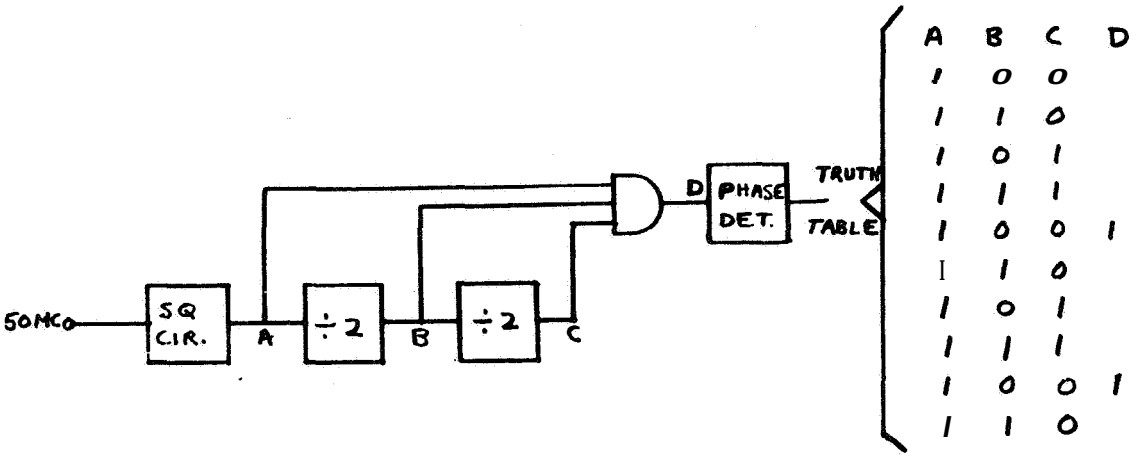


Figure 3.2. 1. 3.2. 1. P. M. Modulator Counter Logic

3.2.2 P. M. Receiver

The P, M Receiver block diagram is shownin figure 3.2.2.1 and the principal specification are listed in Table 2. 3. 2. 1. This section of the report correlates the test results with the specification. The principal design considerations are included.

3.2.2.1 Input Amplifier (Code 207)

The input amplifier 3DB bandwidth, amplitude response, phase response and AGC range are specified. Aside from the specified parameters, system responsibility was assumed for the unit's noise figure, phase shift, and amplitude response variation as a function of AGC. The input amplifier's active gain is achieved with two low noise stages and a medium power broadband amplifier. The gain control is contributed by passive pin diode attenuators staggered between stages. The amplitude and phase response is established by a passive linear phase filter. The AGC system described yields minimum carrier phase shift and variations in amplitude response as a function of AGC. The input amplifier noise figure consideration determines the maximum input signal that can be accomodated without overload. As shown in figure 3. 2. 2. 1, the noise figure is degraded as the attenuation factors A1 and A2 are increased, if the gain G1 and G2 are not large. The specification dictates 30DB (maximum)

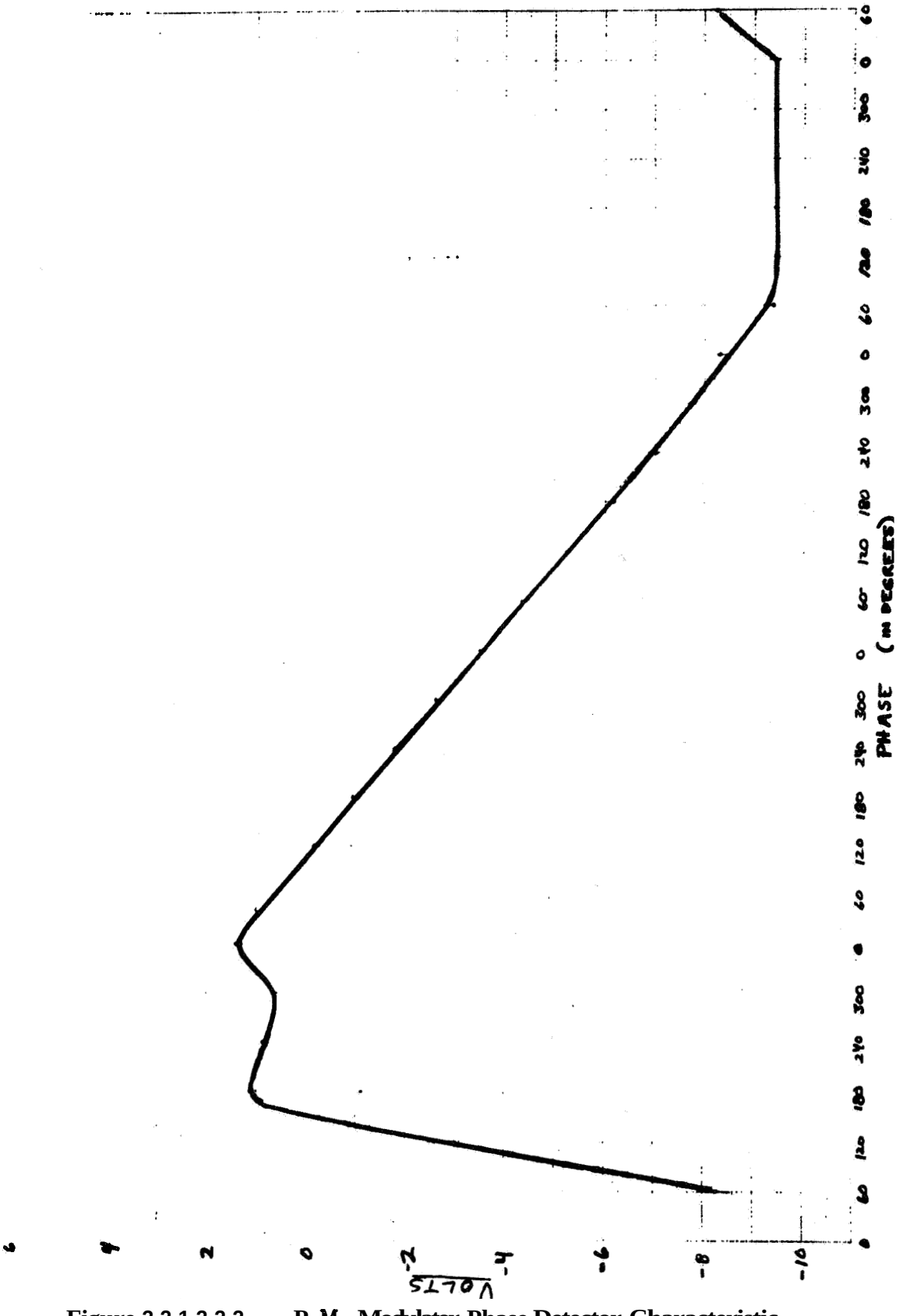


Figure 3.2.1.3.2.2. P. M. Modulator Phase Detector Characteristic

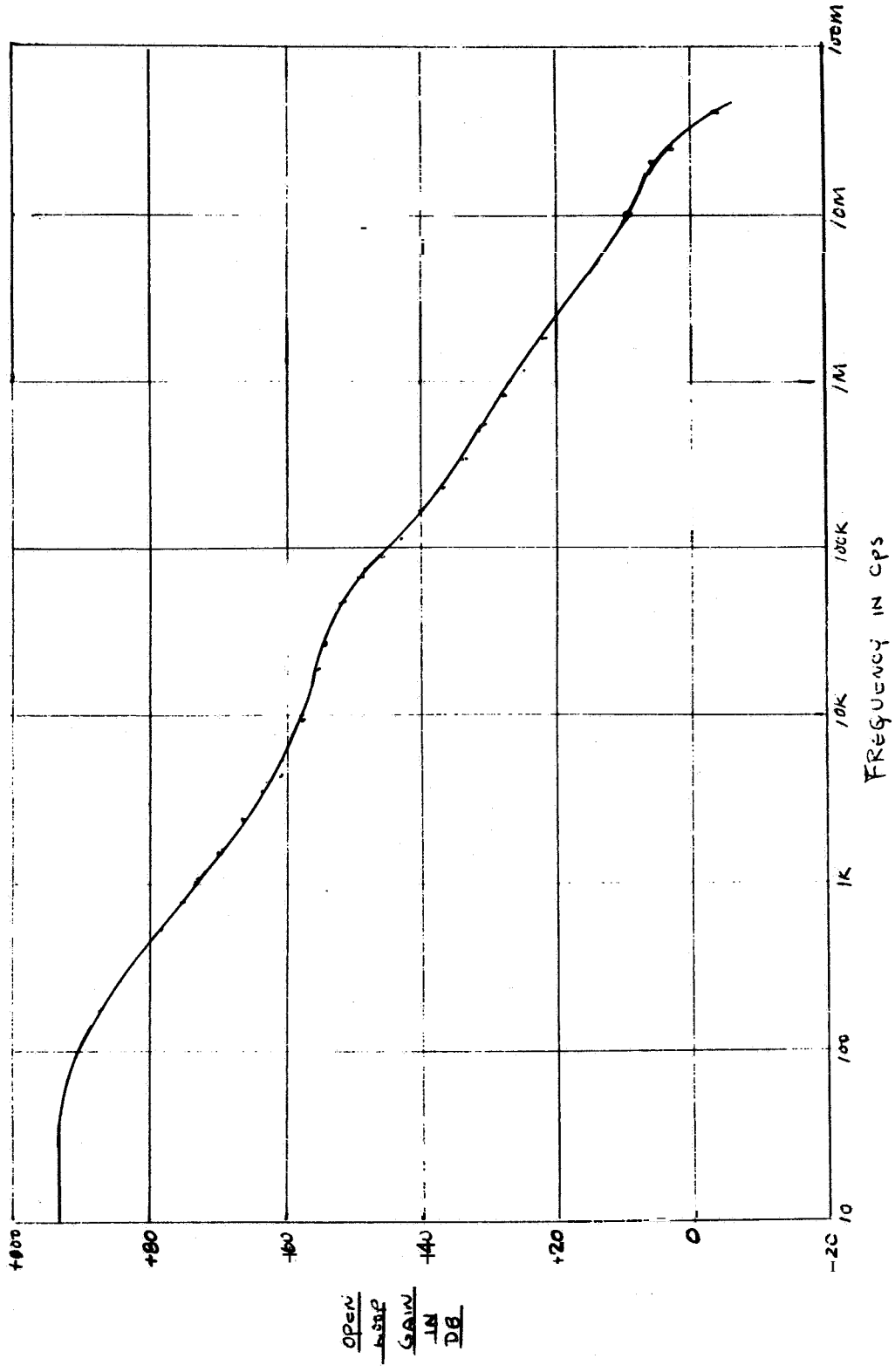


Figure 3.2.1.3.2.3. Bode Diagram Burr Brown Model 1510 Operational Amplifier

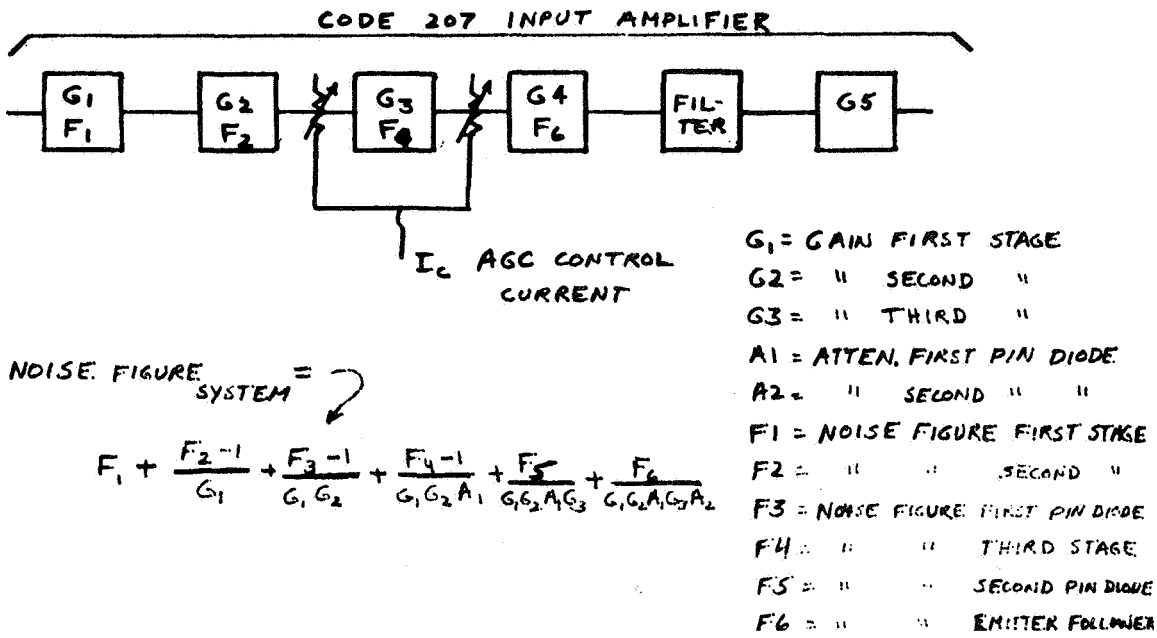


Figure 3.2.2.1. Input Amplifier Noise Figure Considerations

attenuation of A1 and A2; therefore, the gain G1, G2, G3 must exceed 30DB if the noise figure is held to a reasonable limit at full AGC. The product G1, G2, G3 was selected as 45DB. However, the power capabilities of a low noise amplifier is limited, as a result the maximum input power must be constrained to -45DBM or less to avoid overload. Clearly, a larger input power can be tolerated if G1, G2, G3 is reduced; however, a larger noise figure results.

Figures 3.2.2.2 thru 3.2.2.7 indicate the test system and test results of the input amplifier amplitude and phase response at minimum, maximum, and mid range AGC. Figure 3.2.2.8 indicates the 50 mc carrier phase shift and noise figure as a function of AGC.

3.2.2.2 Balanced Modulators (Mixes)

The specification requires that the modulators be equivalent to ideal voltage multipliers in the time domain or translators in the frequency domain such that all spurious and feedthrough products are 50DB below the desired output. The Hewlett Packard

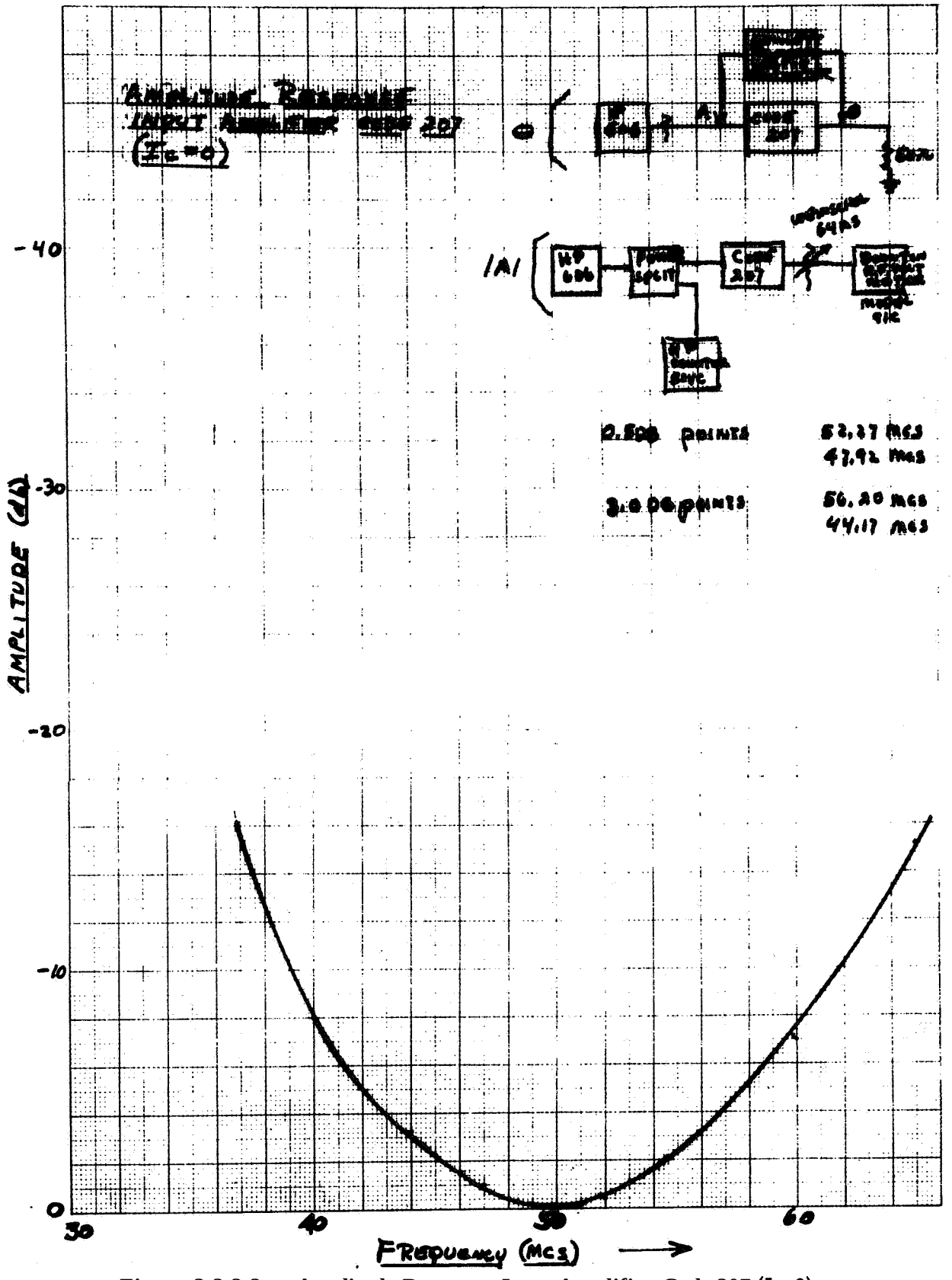


Figure 3.2.2.2. Amplitude Response Input Amplifier Code 207 (Ic=0)

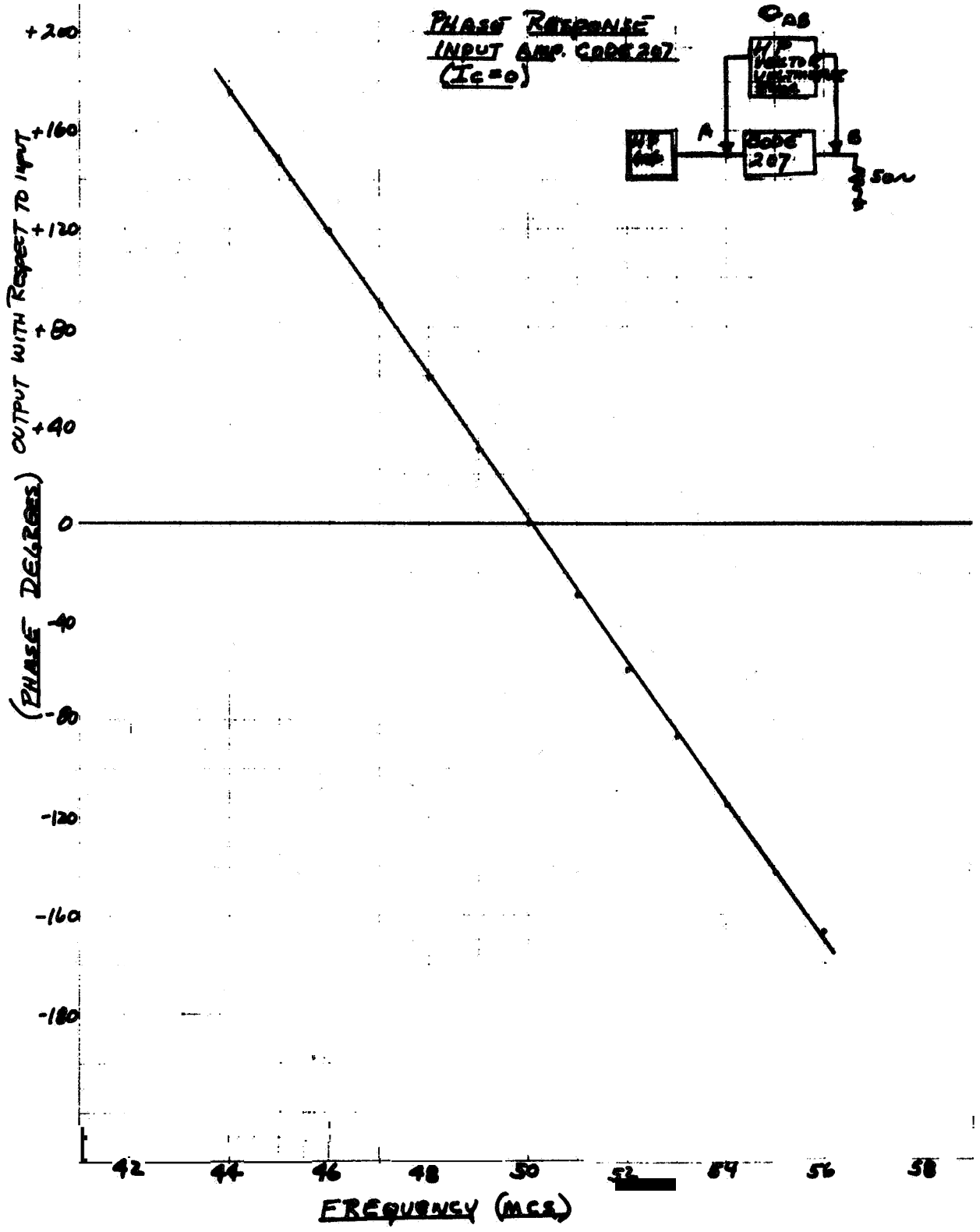


Figure 3. 2. 2. 3. Phase Response Input Amplifier Code 207 (Ic-0)

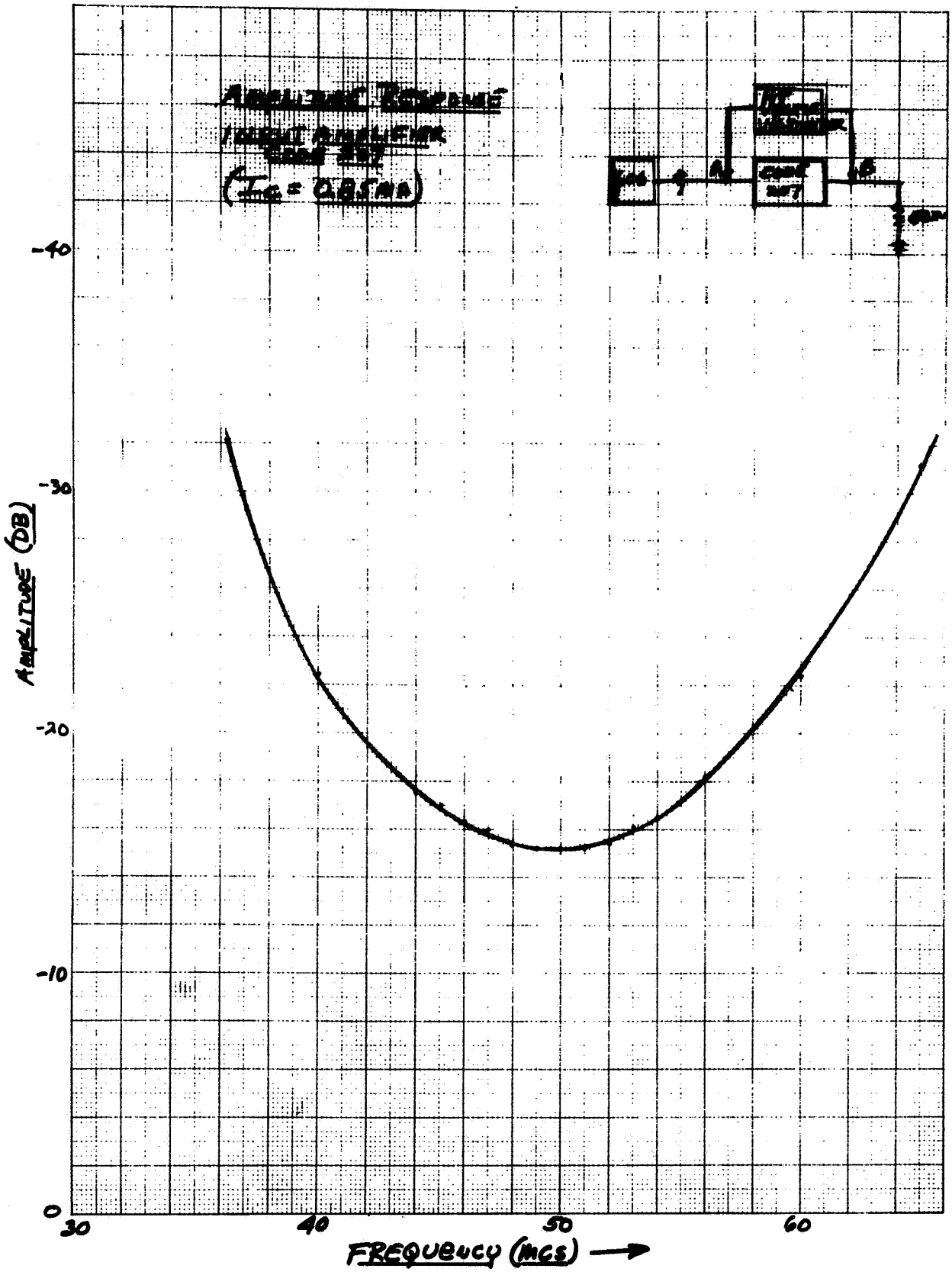


Figure 3. 2. 2. 4. Amplitude Response Input Amplifier Code 207 (Ic=0. 85 MA)

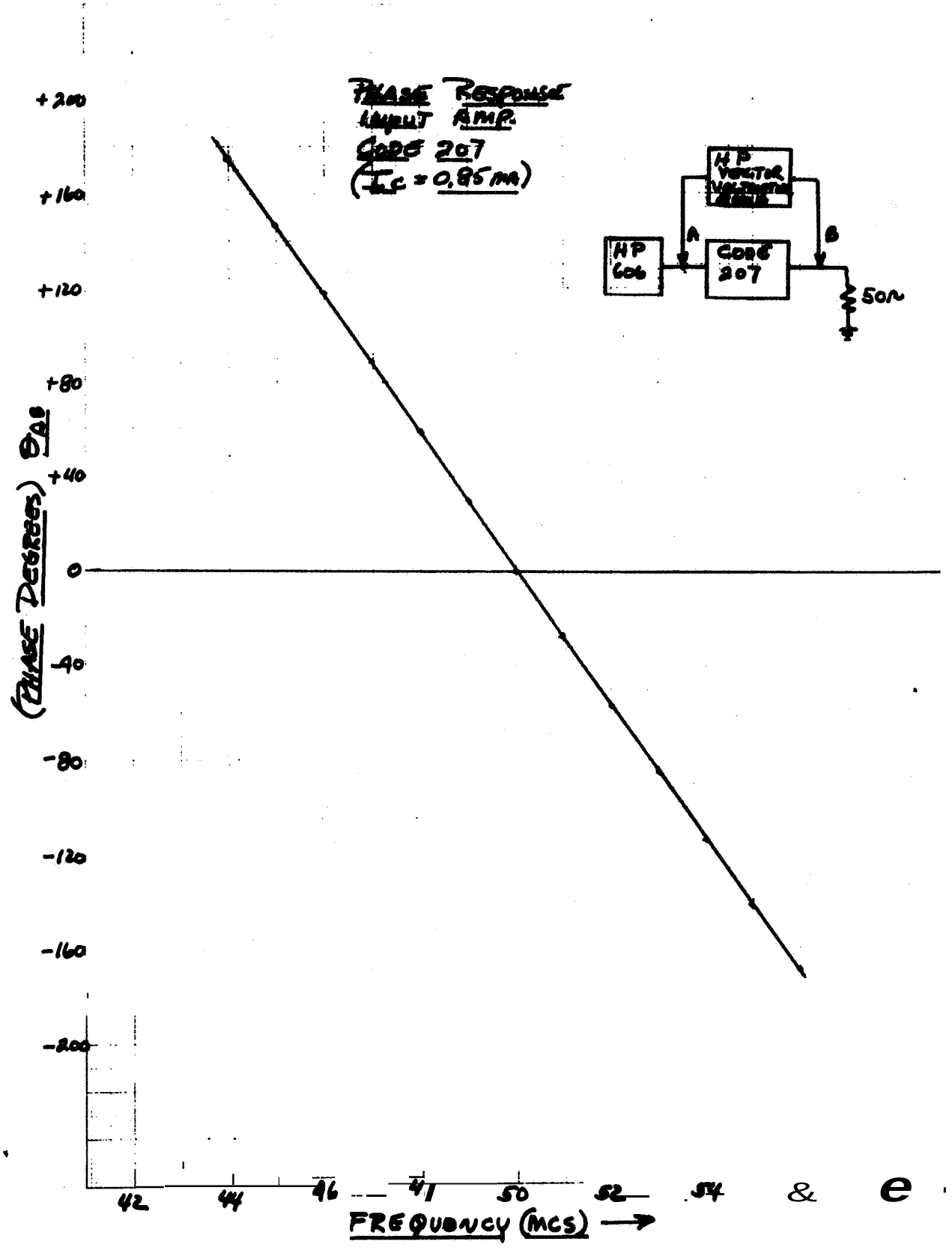


Figure 3.2.2.5. Phase Response Input Amplifier Code 207 (Ic=0. 85 MA)

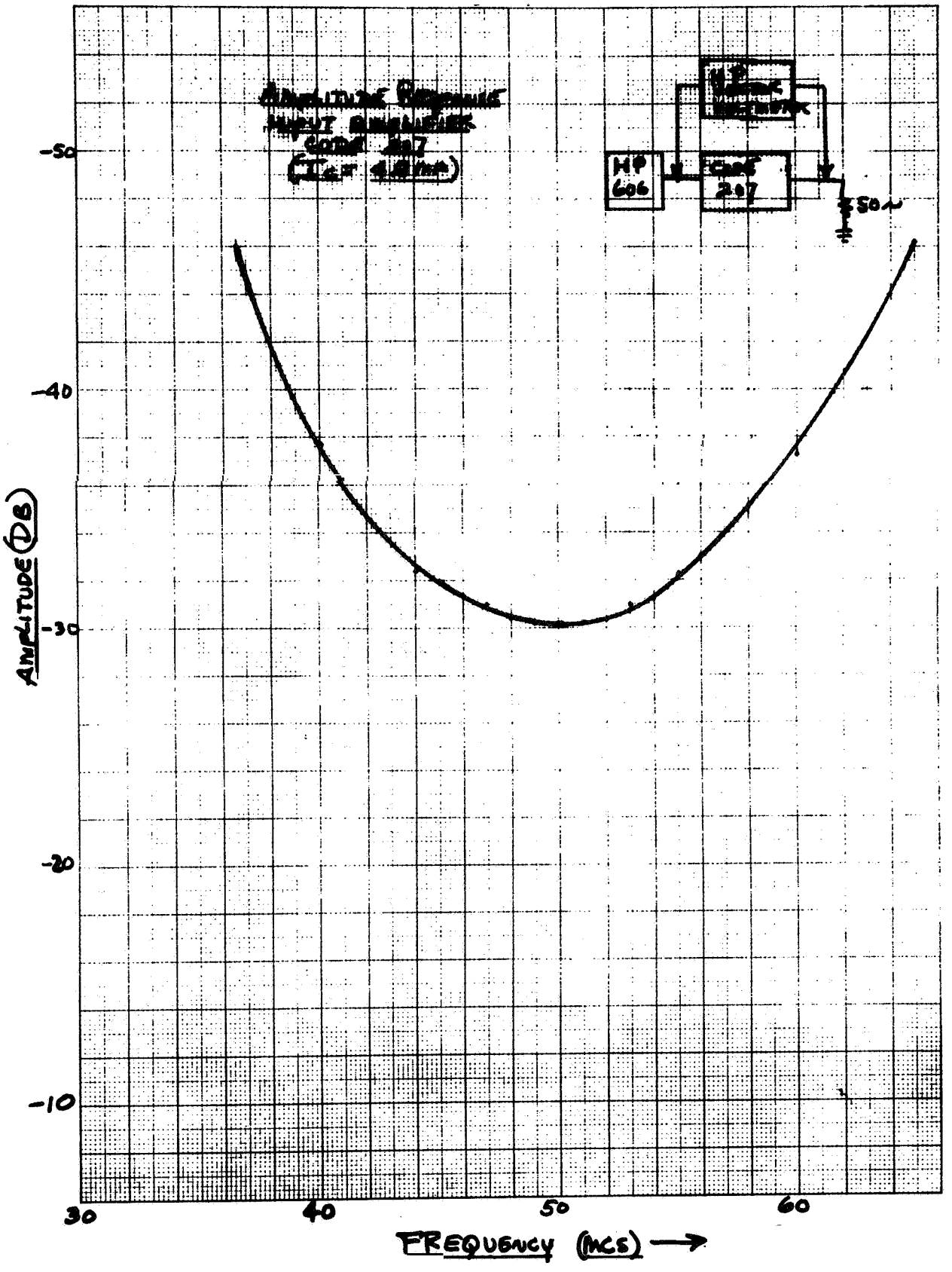


Figure 3.2.2.6. Amplitude Response Input Amplifier Code 207 (I_C-4. 0 MA)

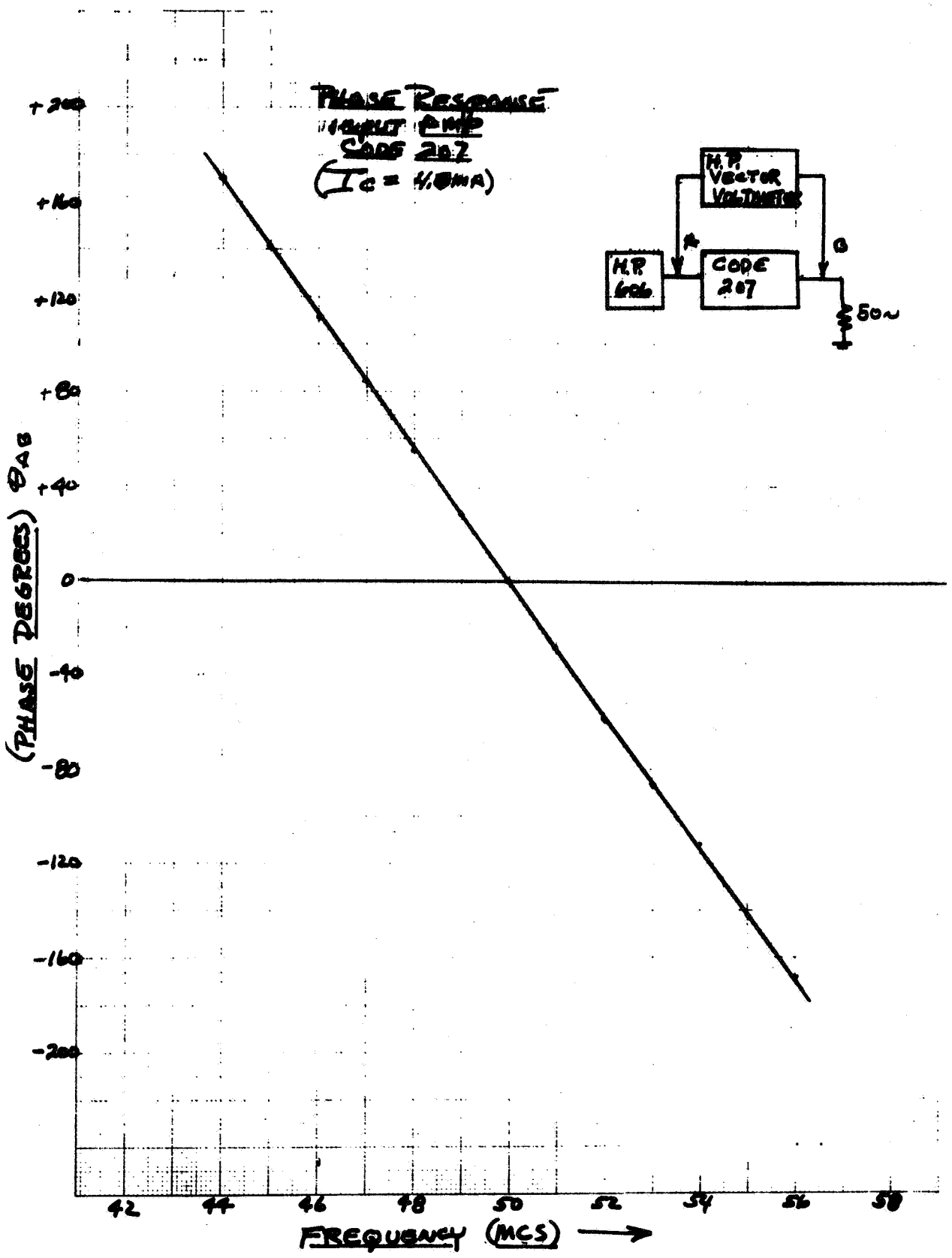


Figure 3. 2. 2. 7. Phase Response Input Amplifier Code 207 (Ic-~0 MA)

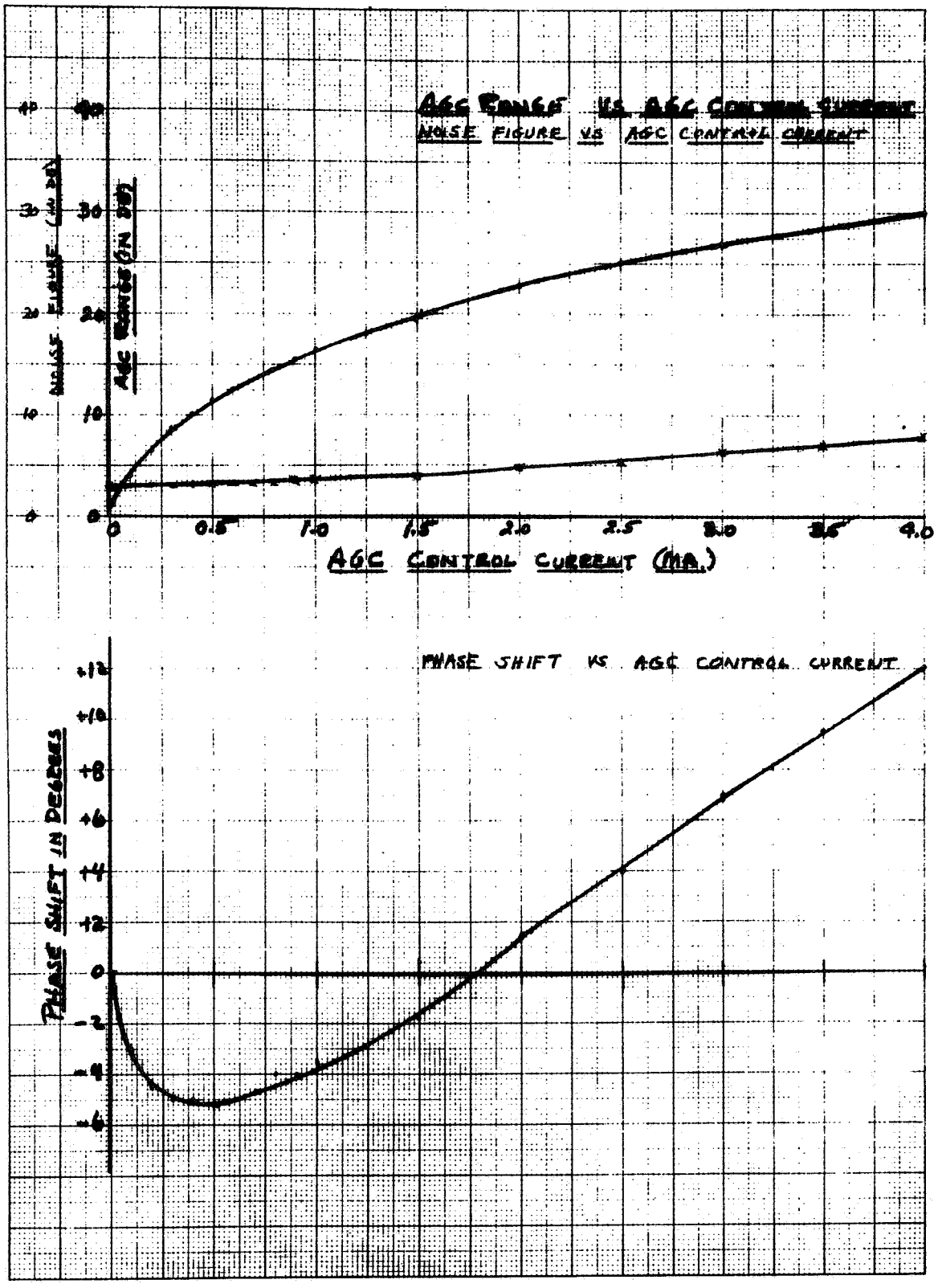


Figure 3.2.2.8. AGC Range Vs AGC Control Current, Noise Figure Vs AGC Control Current

model 10514A double balanced mixer was used as a frequency translator throughout the R. F. test console. Our experience indicated that this unit represents state of the art achievement with regard to intermodulation or spurious products. Figure 3.2.2.9 lists the characteristics of this unit. The third order product ($2f_e - f_r$) is 10DB above the specification: however, as stated, this represents state of the art. The parameters listed are achieved by utilizing carefully matched hot carrier diodes. The mixer input and output transformers are wide-band, accurately balanced units such that the mixer output is constant within 0.1DB between 1Mc and 100 Mc. The phase shift or group delay in the region of 50 Mc and 10 Mc was measured and found to be compatible with the R. F. Test Console requirements.

3.2.2.3 Narrow Band IF (Code 206)

The narrow band i-f amplifier specification is listed in Table 2.3.2.1. The unit's active gain is contributed by tuned feedback amplifiers. The amplitude and phase response of the unit is determined by a crystal filter. The tuned amplifier bandwidth is very large compared to the filter. Input and output emitter followers establish a 50 ohm source and load for the filter, The filter was designed to exhibit amaximally flat group delay or linear phase characteristic, Figure 3.2.2.10 indicates the amplitude and phase response of the overall amplifier. The 3DB bandwidth is 2.13Kc and the phase symmetry is within ±5 degrees for frequencies within ±3.5 Kc of 10 Mc center frequency,

3.2.2.4 Wideband I-F (code 214)

The 10 Mc wideband amplifier specifications are listed in Table 2.3.2.1. The unit's active gain is established by broadband feedback amplifiers. The basic feedback amplifier design is discussed later in this report. The module's phase and amplitude response is established by a passive filter. The module amplitude response (and test set) is shown in figure 3.2.11. The phase response is indicated by figure 3.2.2.12. The filter was designed for maximally flat group delay (linear phase) and an amplitude response roll off of ±0.5DB within 1.5 Mc of the 10 Mc center frequency. These constraints determined the 3DB bandwidth as 6.8 Mc. The specification dictates sixty percent bandwidth (6 Mc bandwidth centered on 10 Mc), as a result the filter exhibits geometric symmetry but not arithmetic symmetry. Arithmetic and geometric symmetry are essentially the same for a filter whose percentage bandwidth is ten percent or less. The technique to build a filter with sixty percent bandwidth that yields arithmetic symmetry has not been completed. The phase response of the 10 Mc wideband I-F amplifier shown in figure 3.2.2.12 exhibits geometric not arithmetic phase symmetry of ±5° over a 6 Mc passband.

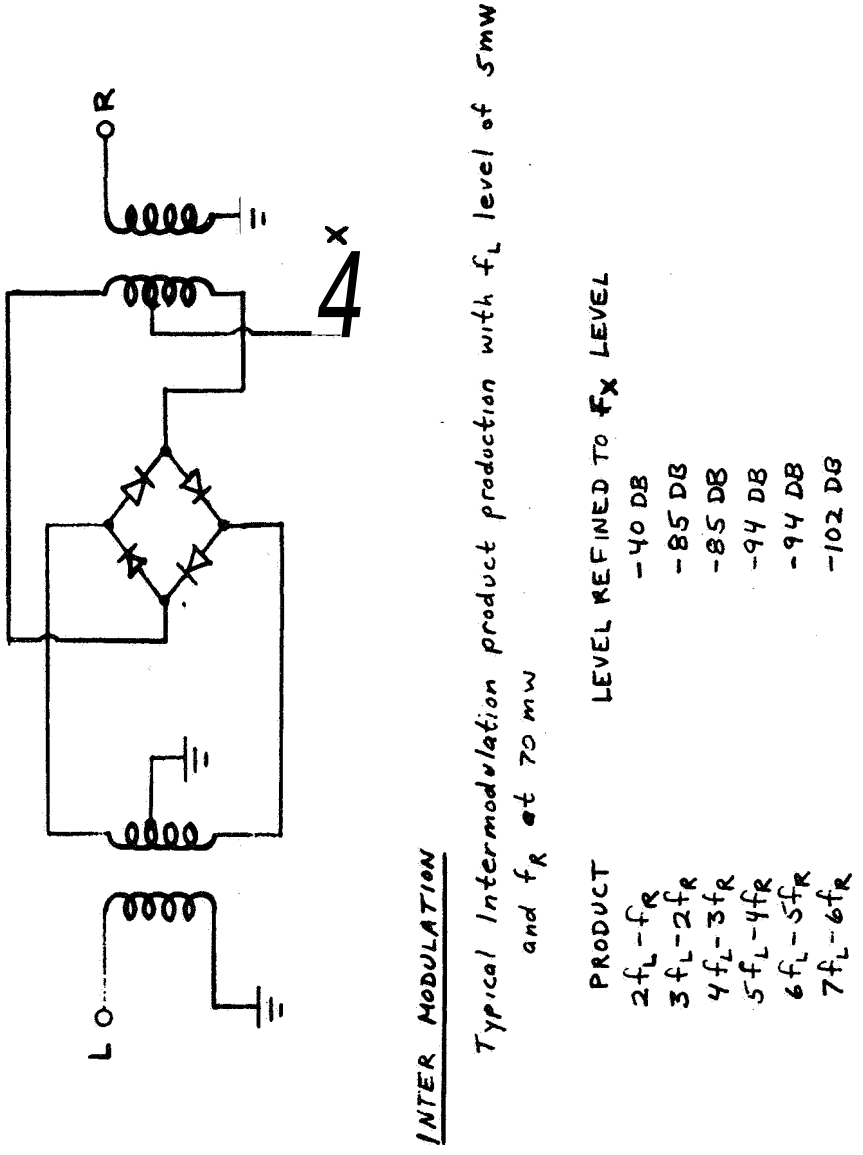


Figure 3.2.2.9. Balanced Mixer Characteristics

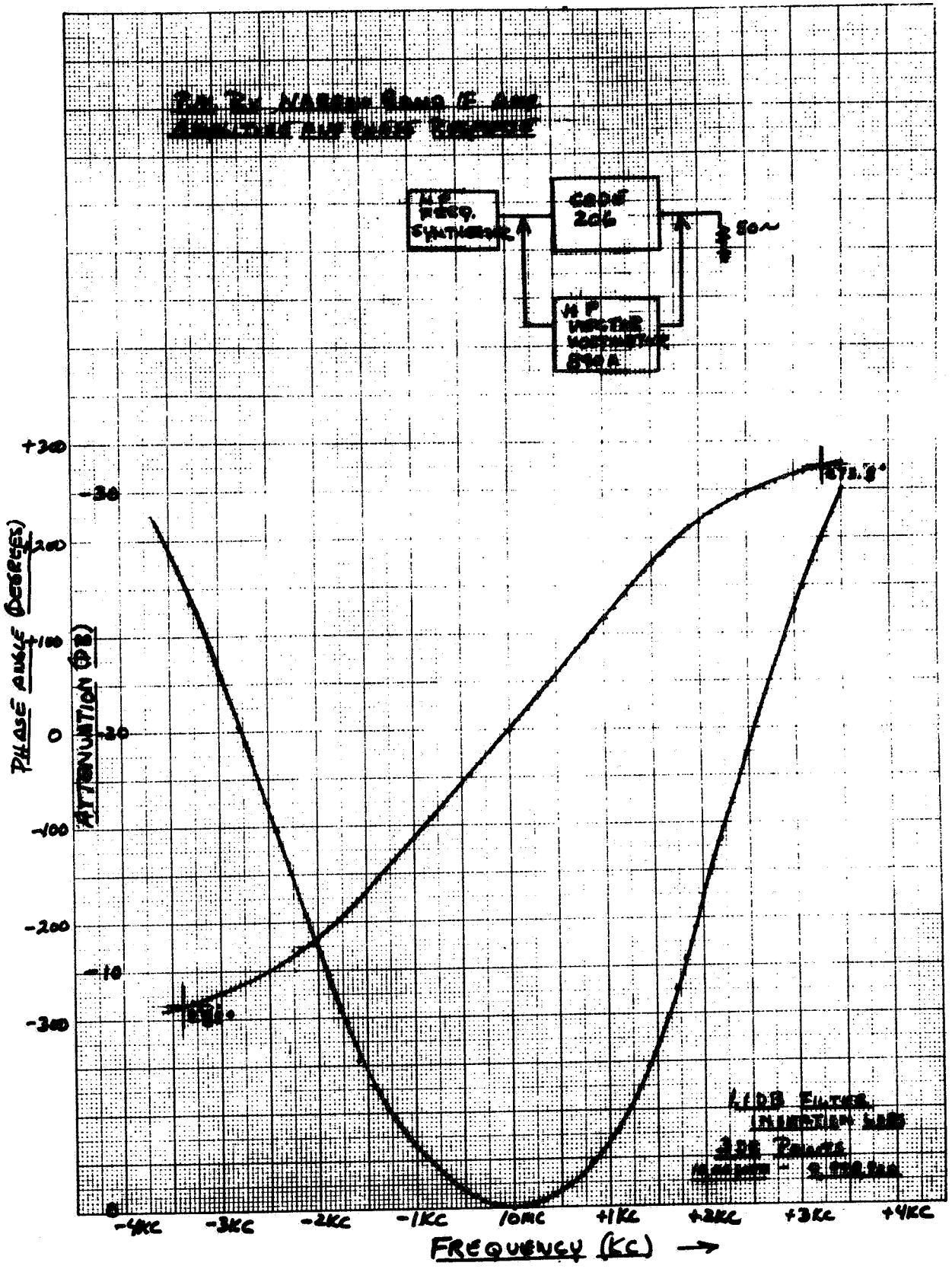


Figure 3.2.2.10. P.M.RCVR Narrow Band I-F Amplifier Amplitude and Phase Response

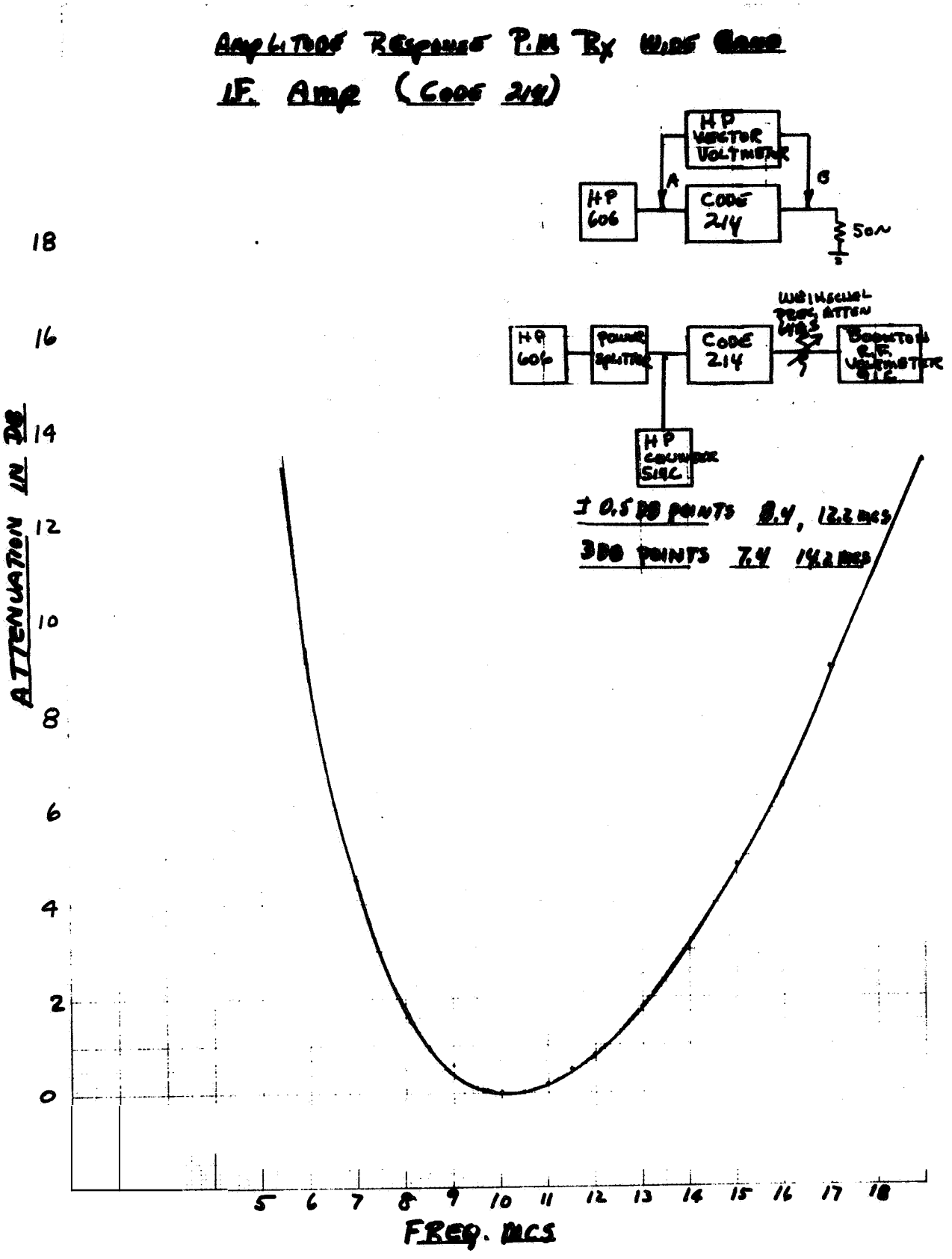


Figure 3.2.2.11. Amplitude Response P.M. RCVR Wide Band I. F. Amplifier (Code 214)

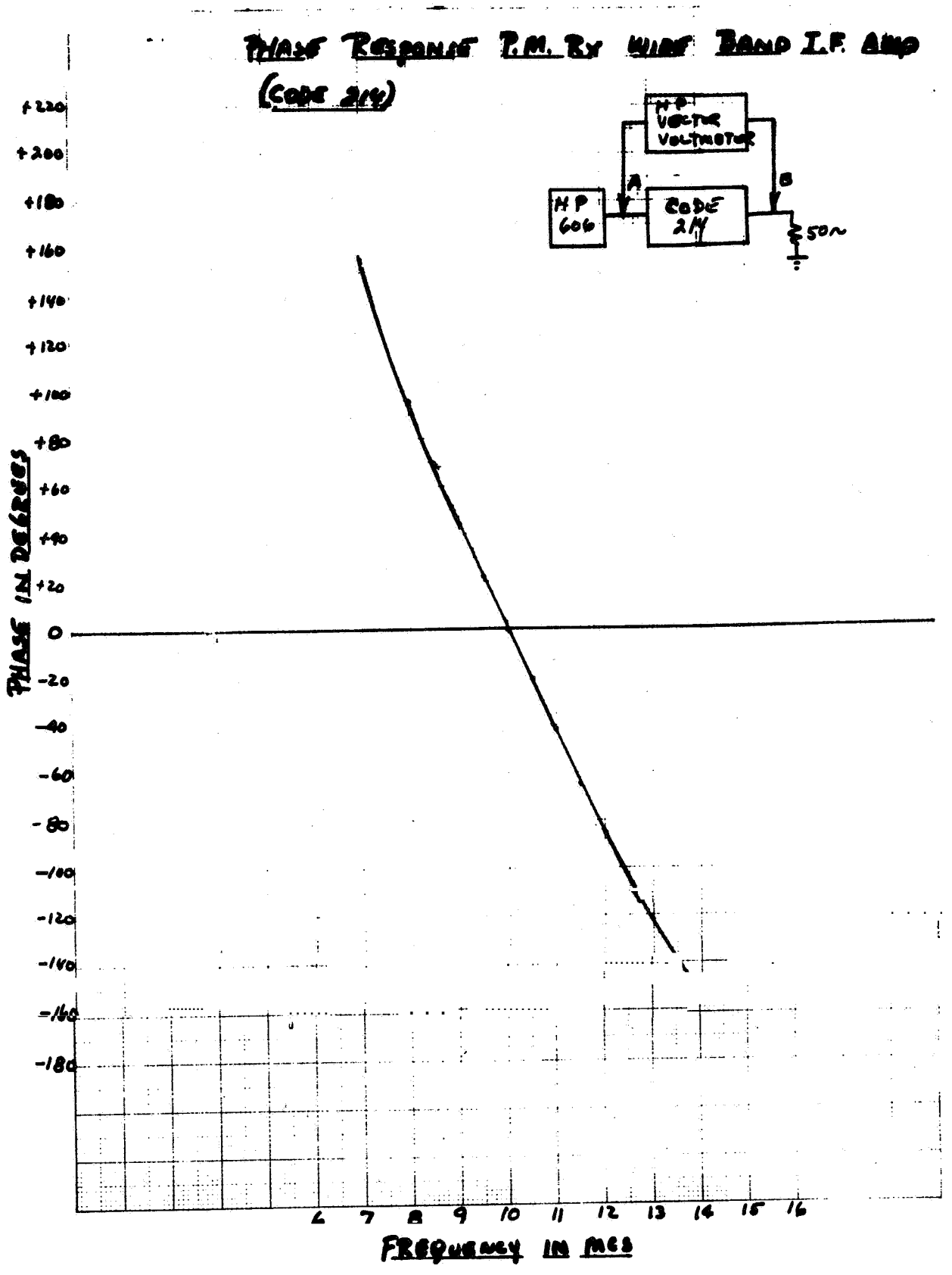


Figure 3.2.2.12. Phase Response P.M.RCVR Wide Band I-F Amplifier (Code 214)

3.2.2.5 Wideband Phase Detector (Code 203A and 203)

The wideband phase detector specifications are listed in Table 2.3.2.1. A basic module design was developed and used three places in the receiver. The wideband phase detector was modified slightly to exhibit larger dynamic range and greater bandwidth than the carrier track and AGC units. The basic phase detector bandwidth is established by the input transformer and extends well beyond 10 Mc; however, the bandwidth of the wideband unit is established by its output filter which initially was designed for 5 Mc as shown in figure 3.2.2.13. The output bandwidth of the carrier track and AGC phase detectors (code 203) are required to accomodate only half the predetection bandwidth or 1Kc; therefore, the outputfilters of these units were designed primarily to suppress the 10 Mc feedthru and 20 Mc product. During the course of system test, it was mutually agreed with the cognizant engineer to modify the wideband phase detector output and decrease the bandwidth to 2 Mc. This modification was implemented to match the receiver output bandwidth to the P. M. Modulator bandwidth capability. The resultant response is shown in figure 3.2.2.14.

The wideband phase detector dynamic range was specified as 40DB. This may be defined as the transfer of the amplitude output beat note as a function of the signal level input. The plot of this transfer is shown in figure 3.2.2. 15. The limits of the plot are bounded at one extreme by the unit's noise level and at the .other extreme whereby the output beat note distortion. The distortion results when the signal level approaches the reference level. The 10 Mc reference power is 2 watts. As shown on figure 3. 2. 2. 15, a 50DB dynamic range of input signal; (Pin between the limits of (0 and -50DBM) results in a linear variation of output beat note well above noise and 10DB below the upper bound.

3.2.2.6 Carrier Tracking Loop

The specified receiver carrier tracking loop parameters are shown in Table 2.3.2.1. The no noise loop gain required to constrain the static phase error to one degree for 500 cps of transmitter detuning is 180,000 or 105DB. Figure 3.2.2.16 indicates the test system and loop gain distribution required to achieve 105DB of loop gain. An alternate test system (not shown) that was used in system test involved the substitution of a Hewlett Packard Model 5100A frequency synthesizer to provide the variable frequency receiver input carrier.

The specification requires loop bandwidths (2Blo) of 3.0, 12.0, 20.0 and 48.0 cps. The loop design is based on the JAFFE, RECHTIN[5] technique which relates the loop filter

5 - Jaffe, W and E. Rechtin, Design and Performance of Phase Lock Logics Capable of Near Optimum Performance over wide Range of Input Signal and Noise Levels, Trans IEE IT-lpp 66-76 March 1955

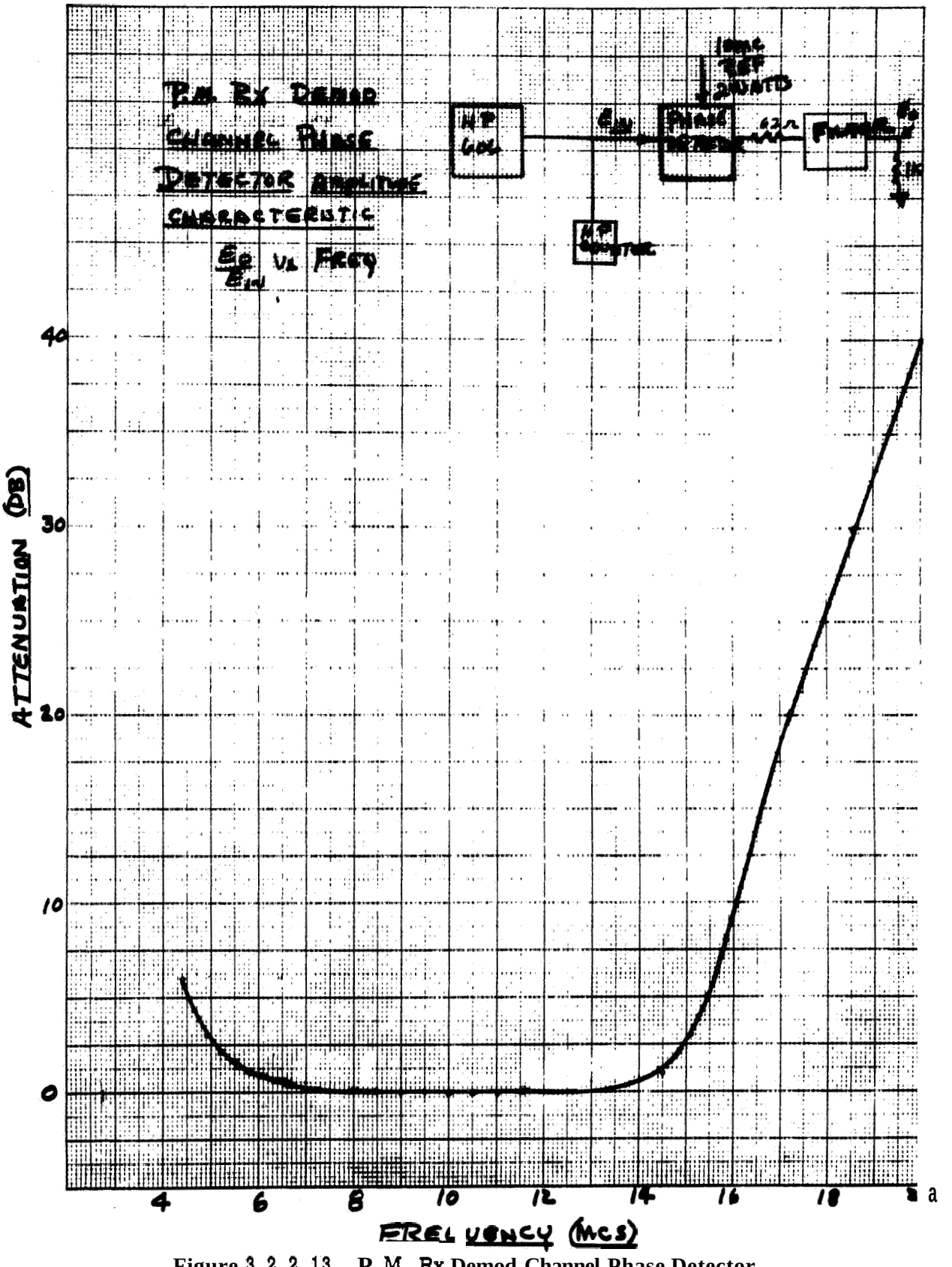


Figure 3, 2, 2, 13. P. M. Rx Demod Channel Phase Detector Amplitude Characteristic $\frac{E_o}{E_{in}}$, Vs Freq.

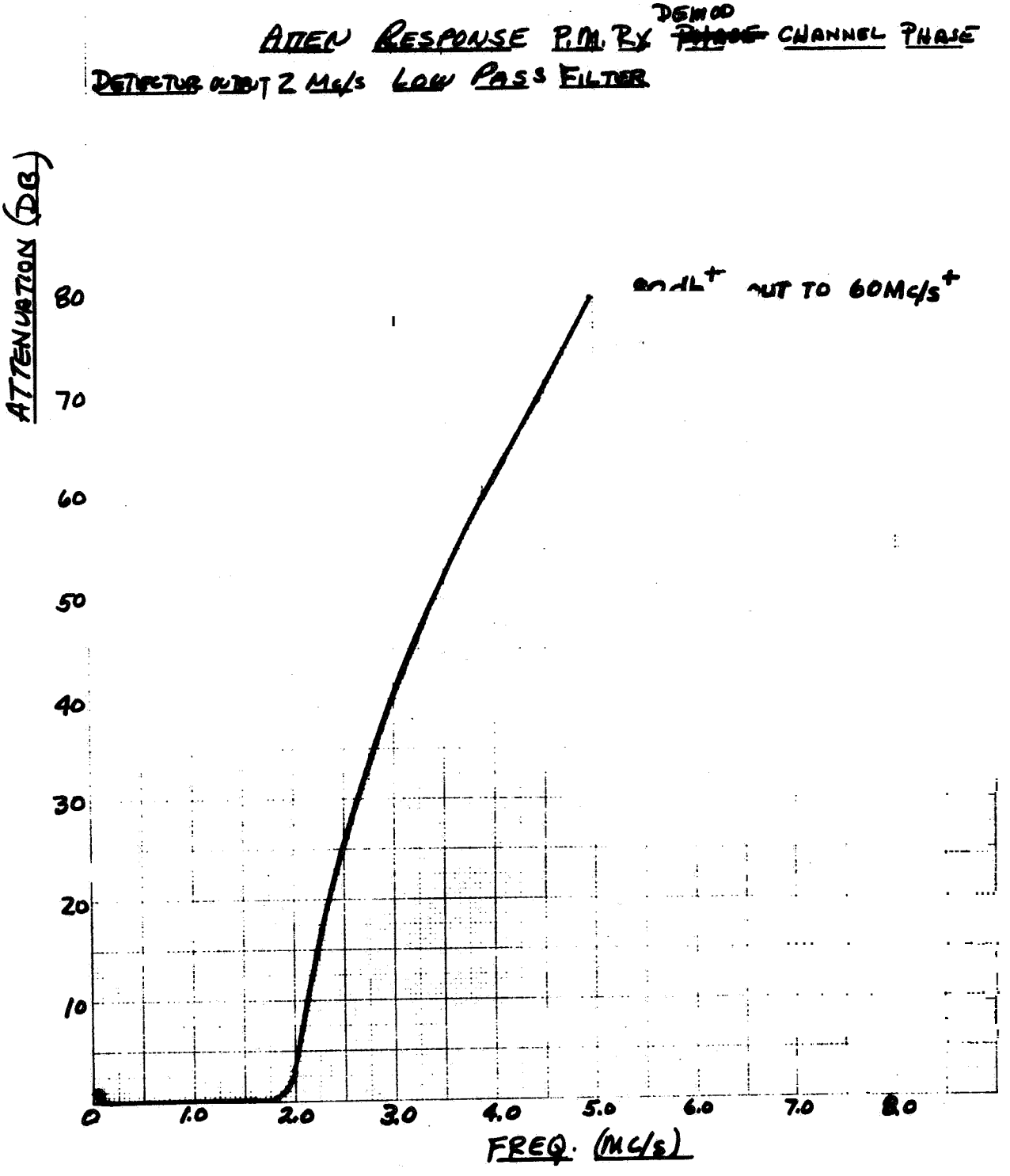


Figure 3.2.2.14. Atten Response P. M. RCVR Demod Channel Phase Detector

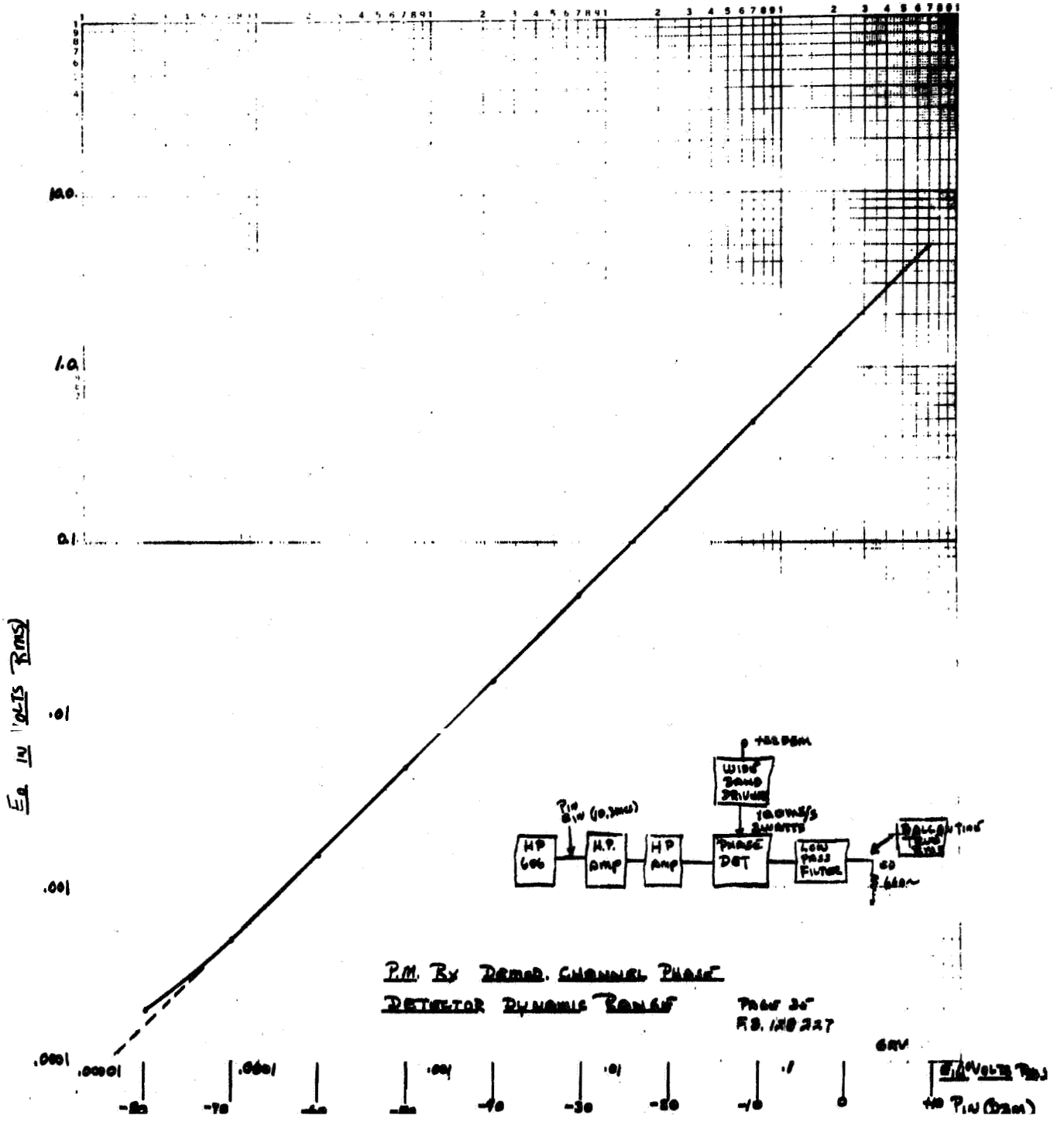


Figure 3.2.2.15. P.M.RCVR Demod Channel Phase Detector Dynamic Range

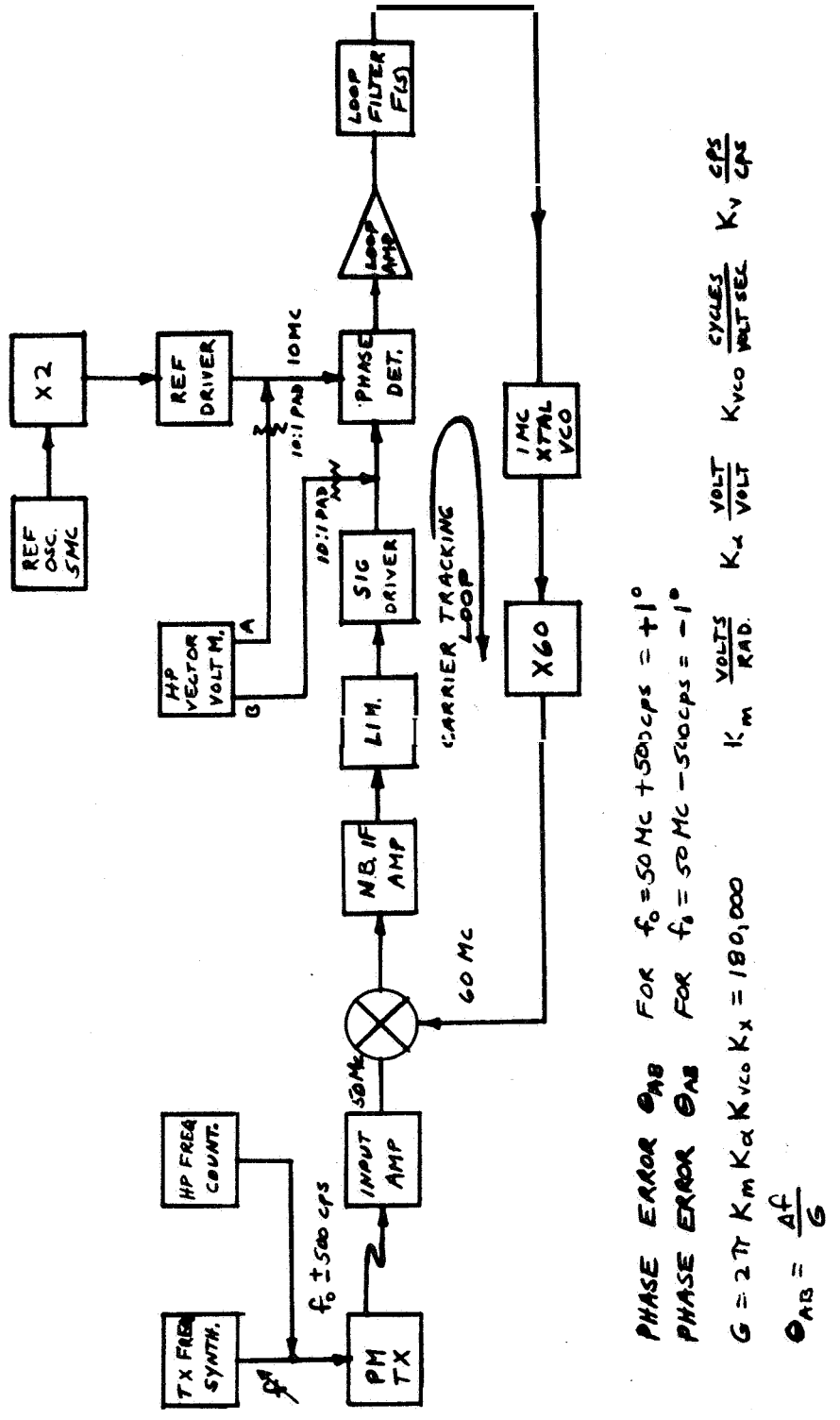


Figure 3.2.2.16. P.M.RCVR Carrier Tracking Loop Gain Test System

time constants to the loop gain at threshold. The principal parts of the JAFFE RECHTIN design are listed in figure 3.2.2.17. The loop parameters, computed and measured are shown in figure 3.2.2.18. The technique used to measure the loop information bandwidth is shown in figures 3.2.2. 19 and 3.2.2.20.

The loop filter components are comprised of one percent resistors and 3 percent capacitors. Two capacitors (10 mf and 100 μf) are used in conjunction with the various resistors to enable the operator to select the four loops bandwidths (either active or passive mode). The same loop bandwidthe (2 Blo of 3. 0, 12.0, 20.0 and 48.0) are also selectable at one thirtieth maximum loop gain such that the operator may rimulate a static loop phase error of 30 degrees by detuning the transmitter 500 cps.

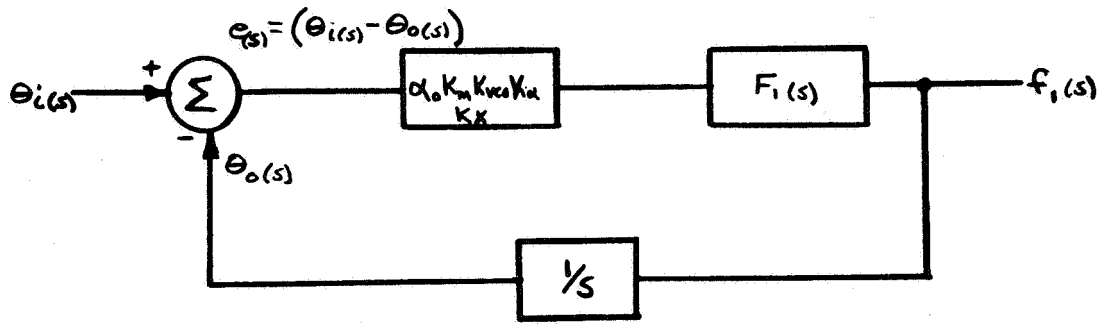
The tracking loop XATL. VCO tranefer of output frequency to input control voltage is inherently nonlinear as determined by the nonlinear change in capacitance of the varactor as a function of control voltage,

The VCO output frequency as a function of control voltage is ehown by figure 3. 2. 2. 21. The nonlinear characteristic is compensated by a non linear function generator. The compensating characteristic of the function generator is determined by straight line approximations whereby 10 segments comprise the total curve. The corrected VCO transfer and test set is ehown in figure 3.2.2.22.

Aside from the principal specifications discussed, the receiver has been designed such that the operator may open the loop and manually change the VCO frequency for acquisition. The VCO control voltage is monitored on a front panel meter. Various loop bandwidths and loop filters (active or passive) are selectable at the receiver front panel.

3.2.2.7 AGC Loop

The receiver AGC loop specifications are listed in Table 2. 3.2. 1. Figure 3.2.2.23 indicates the test system used to verify the AGC loop gain. Note that the Hewlett Packard Vector Voltmeter is used simply as a null device, The receiver input signal was attenuated in 6DB steps with R, and sufficient attenuation was subtracted from R2 to maintain a null on the Vector Voltmeter. This technique referenced the measurement accuracy to the Weinschel attenuators. The loop gain is non linear. The minimum gain was established as 20. The AGC loop amplifier is assigned a gain of 68 and the combined minimum gain of the coherent amplitude detector and input amplifier, is 0.29. This arrangement established a peak to peak beat note from the coherent AGC detector (when the APC loop is unlocked) of 0.6 volts. The unit is capable in deliverying 24 volts peak-to-peak; therefore, the unit can deal with a signal to noise ratio of -40 db, whereby the predetection signal to noise ratio at carrier



Linear Phase Model Phase Lock Loop

$$G_o = 2\pi\ (\alpha_o K_m K_{vco} K_\alpha K_x)$$

$$F_1(s) = \frac{f_1(s)}{e(s)} = \frac{1+\tau_2 S}{\tau_1 s} = B_o^2 \frac{1+\sqrt{2}}{B_o} \qquad (1)$$

where $\tau_1 = \frac{G_o}{B_o^2}$ and $\tau_2 = \frac{\sqrt{2}}{B_o}$ | for either active or passive filter

open loop transfer function

$$Ho_{(s)} = \frac{\theta o(s)}{e(s)} = \frac{Bo^2\left(1+\frac{\sqrt{2}}{Bo} S\right)}{S^2} \qquad (2)$$

closed loop transfer function

$$H(s) = \frac{\theta o(s)}{\theta i(s)} = \frac{Ho(s)}{1+Ho(s)} = \frac{1+\frac{\sqrt{2}}{Bo} S}{1+\frac{\sqrt{2}S}{Bo}+\frac{S^2}{Bo^2}} \qquad (3)$$

$$2\ Blo = \frac{1}{2\pi j}\int_{-j\infty}^{f+j\infty} |H(s)|^2\ ds = 1.06\ Bo \qquad (4)$$

$$Go = \alpha_o G \qquad (5)$$

$$\alpha_o^2 = \frac{1}{1+\frac{4}{\pi}\left(\frac{N}{S}\right)_i} \qquad (6)$$

where **N/S** = Ratio of Predetection Noise Bandwidth to 2 Blo

Therefore: τ_2 and τ_1 are determined **by 2** Blo, **G** and α_o

Figure 3.2.2.17. P. **M.** Receiver Carrier Tracking Loop

Given		Computed		Measured	
2 Blo	Bo	α_o	fo	fo(passive filter)	fo(active filter)
3.0 cps	2.83 rad/sec	0.0343	0.45 cps	0.4 cps	0.4 cps
12.0	11.23	0.0685	1.8	1.7 cps	1.8 cps
20.0	18.9	0.0888	3	2.9 cps	2.9
48.0	45.3	0.138	7.2	7.3	7.3

Note: Values of α_o Simulated by Attenuating Phase Detector Signal Input

Figure 3.2.2.18. P.M. Receiver Carrier Tracking Loop Parameters

tracking loop threshold (2 Blo of 3.0 cps) is -28.24 DB. The AGC loop design is summarized in figure 3.3.2.24. The loop 3DB bandwidth as a function of the specified 2 BL is also listed on figure 3.3.2.24. The system outlined in figure 3.2.2.25 was used to measure the loop 3 Db bandwidth. As shown, the modulation signal was applied to the transmitter A, M. Modulator and the AGC error voltage was monitored on a brush recorder, The resulting recorder plots are shown In figure 3.2.2.26. The minimum loop bandwidth (2BL = 0.1 cps) was not measured, as the minimum function generator frequency is 0.01 cps. The minimum loop bandwidth was extrapolated by adding a filter resistor to the single pole filter an order of magnitude greater than for the 0.1 cps bandwidth loop.

3.2.2.8 Feedback Pair

In general, the tactic used throughout the P. M. Receiver and other R. F. Test Console subsystems to achieve accurately specified amplitude and phase responses is outlined as follows: the active gain is contributed by broad band feedback amplifiers (feedback pairs) and the phase and amplitude response is establiehed by paesive filters.

The feedback pair served as a basic "building block" throughout the system and merits attention in this report, Figure 3.2.2.28 indicates the basic circuit diagram and an equivalent circuit diagram. The closed-loop circuit gain[6] is as outlined by equation 58:

$$A = \frac{a}{1-at} = \frac{ao}{\frac{s^2}{P_1P_2} + \frac{P_1P_2}{P_1P_2} S + (1 + ao\, fo)} \tag{58}$$

$$A = \frac{Re + Rf}{Re} \quad \text{for } |af| >> 1 \tag{59}$$

6 Analysis and Design of the Shunt Series Feedback Pair by M. S. Ghausi, Report No 112 office of Naval Research, August 16, 1960

Note: This Technique Suggested by F. J. Charles, JPL Tech Memo 3341-64-2

Loop Error: $$e(s) = \theta(s) \frac{S^2}{B_o^2 + \sqrt{2}B_o S + S^2} \quad (1)$$

The loop error to a Sinusoidal Input Modulation whereby, ΔW=Maximum frequency deviation, W_m=modulation frequency

$$fi(t) = AW \sin Wmt$$

$$fi(s) = \frac{\Delta W \cdot Wm}{S^2 + Wm^2} \quad (2)$$

$$\theta i(s) = \frac{\Delta W \cdot Wm}{S(S^2 + Wm^2)} \quad (3)$$

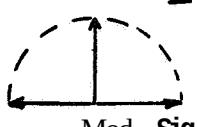
$$e(s) = \frac{\Delta W \cdot Wm}{S(S^2 + Wm^2)} \frac{S^2}{Bo^2 + \sqrt{2}Bo S + S^2} \quad (4)$$

$$et(\ _\ ) = \frac{\Delta W \cdot Wm}{\sqrt{Bo^4 + Wm^4}} \cos(Wmt + \phi_1) \quad (5)$$

$$\text{where } \phi_1 = -\tan^{-1}\left(\frac{\sqrt{2}\,Bo\,Wm}{Bo^2 - Wm^2}\right) \quad (6)$$

The phase relationships between the modulating signal and modulation error become

$B_o < W_m \leq \infty$ Error Sig $\leq W_m < B_o$



Mod. Sig.

The loop adds an additional 90° phase shift, therefore, the lissajous pattern formed by the modulating signal and modulation error becomes a straight line only when $W_m = B_o$

Figure 3.2.2.19. P. M. Receiver Carrier Tracking Loop Bandwidth Test Derivation

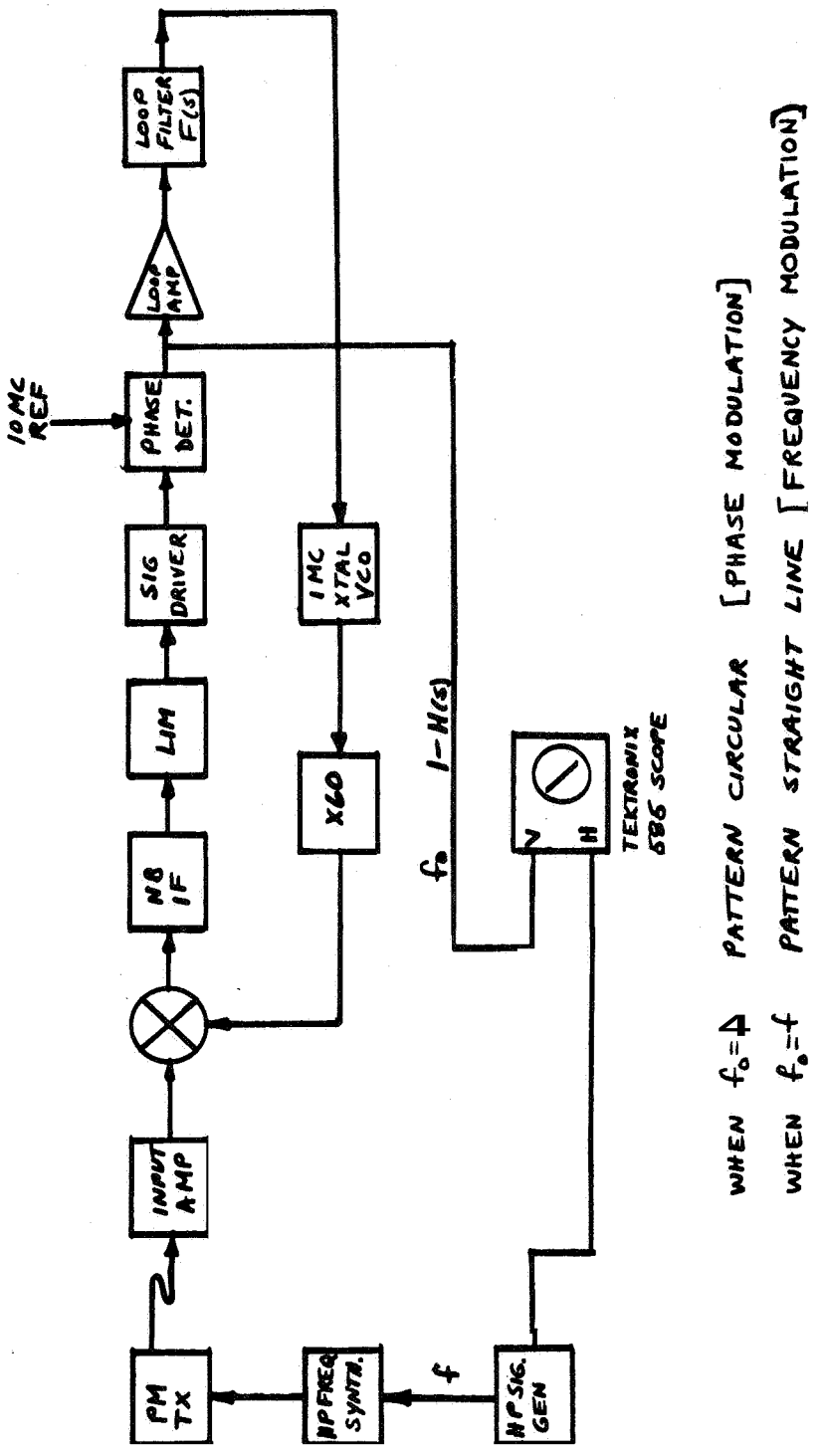


Figure 3. 2. 2. 20. P.M.RCVR Carrier Tracking Loop Bandwidth Test System

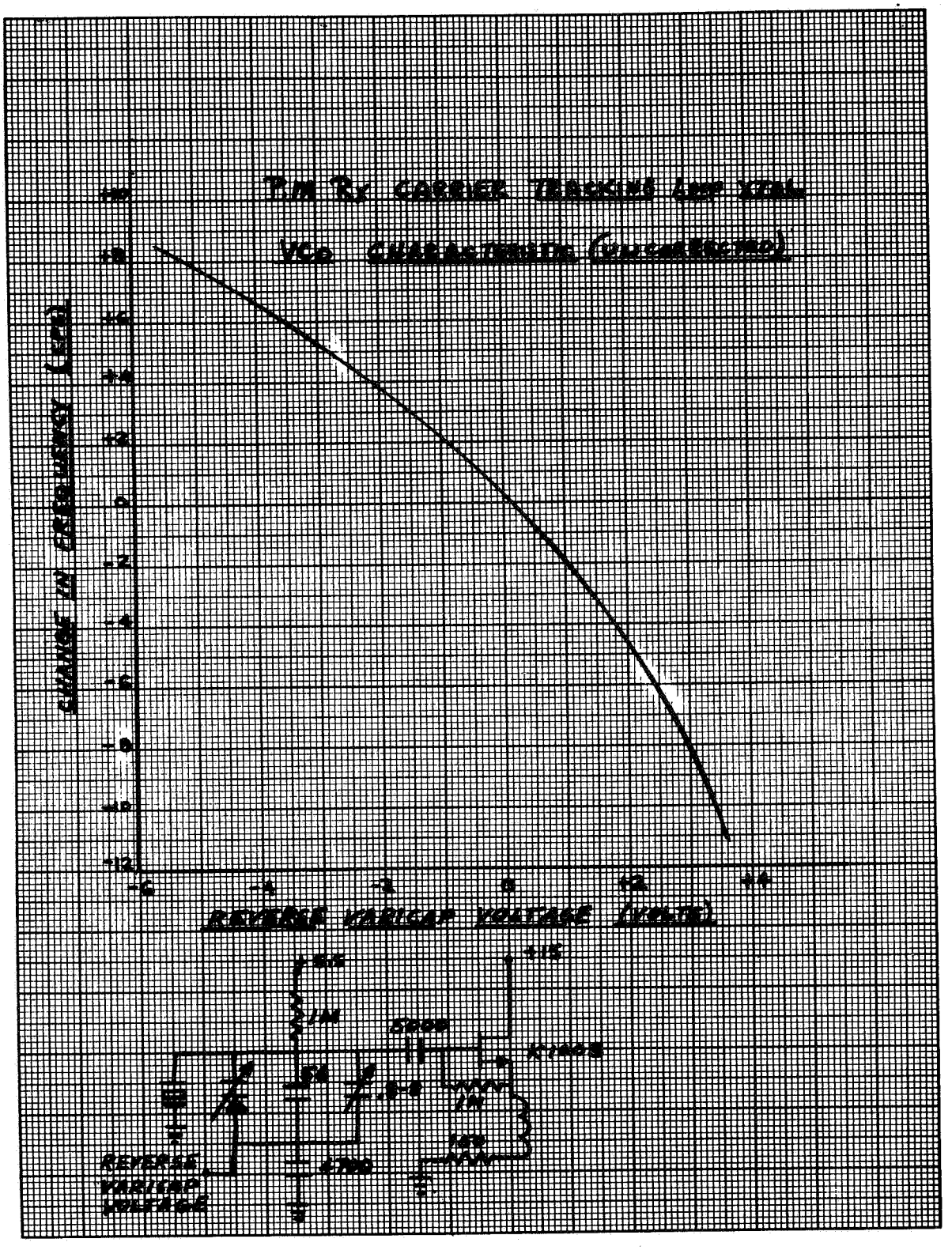


Figure 3.2.2.2 1.P.M.RCVR Carrier Tracking Loop XTAL VCO Characteristic (Uncorrected)

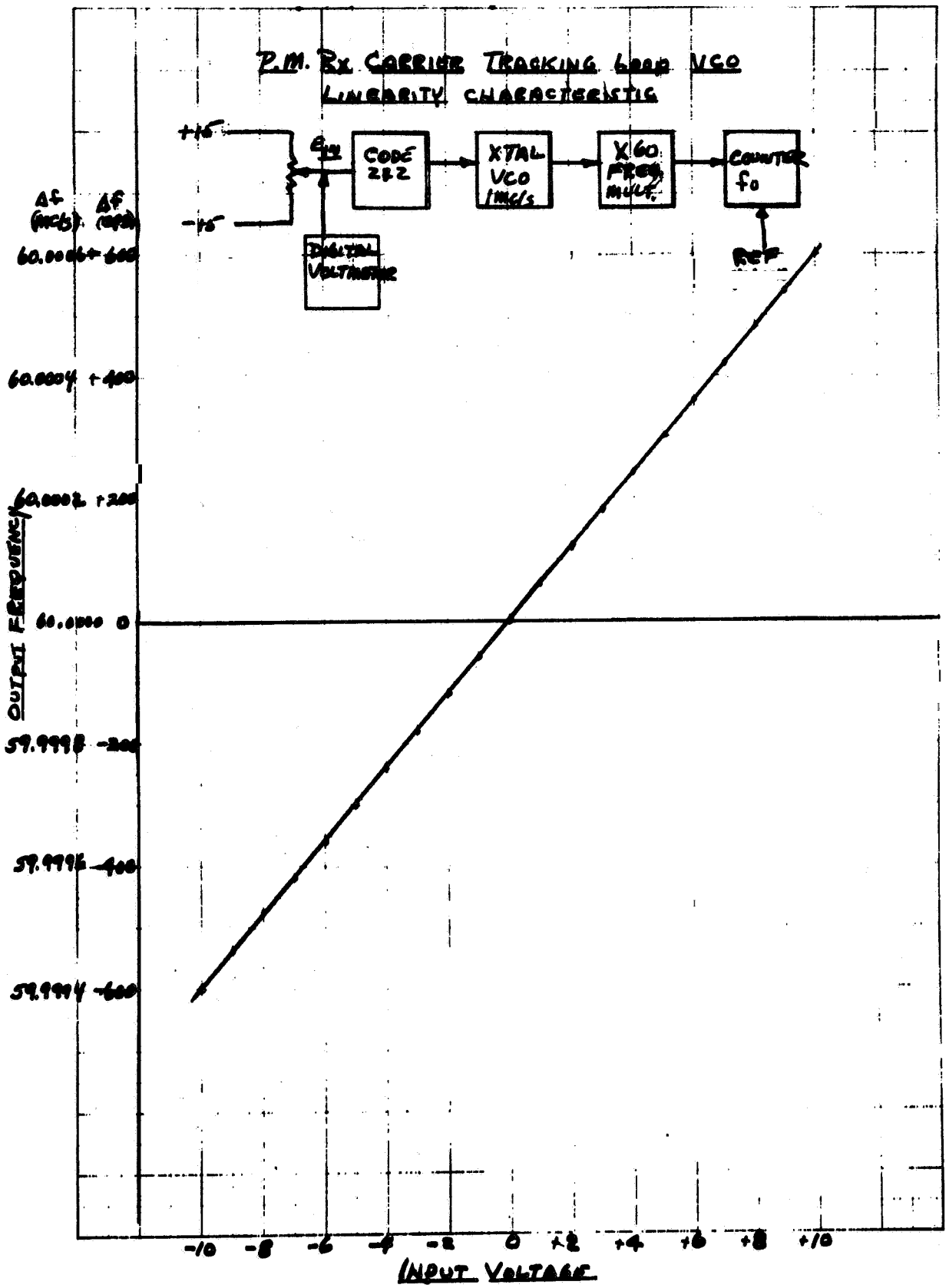


Figure 3.2.2.22. P. M. RCVR Carrier Tracking Loop VCO Linearity Characteristic

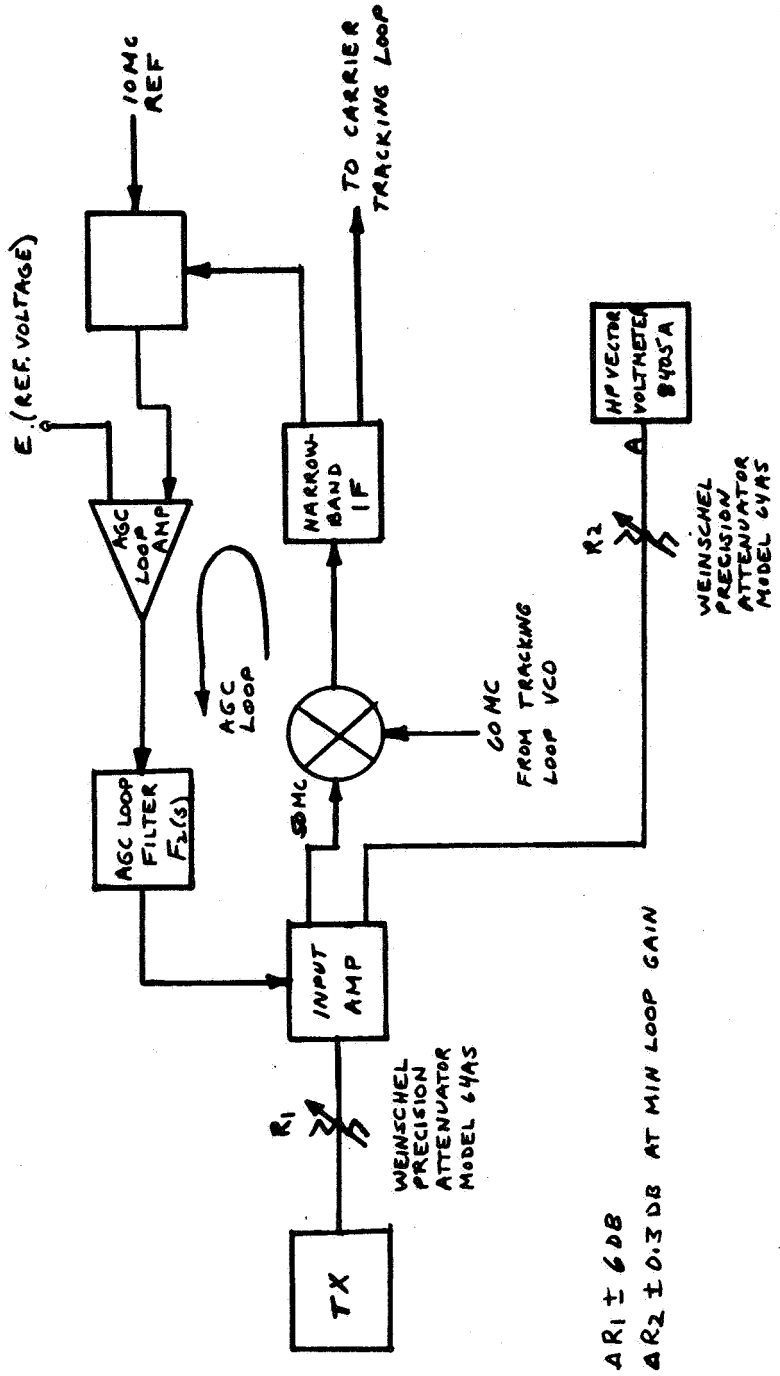
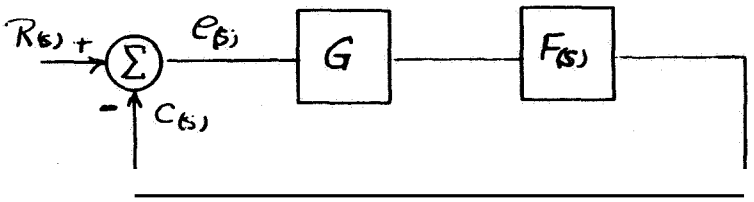


Figure 3. 2. 2. 23. P. M. RCVR AGC Loop Gain Test System



Linear Model AGC Loop

$$G = K_D \text{ I-F Gain}\left(\frac{DB}{Volt}\right) \cdot \text{KA Detector Gain}\left(\frac{Volts}{DB}\right) \cdot K_{\delta} \text{ Loop Amplifier Gain } \left(\frac{Volts}{Volt}\right)$$

$$F(s) = \frac{1}{\tau s + 1} \qquad \text{(specified)}$$

open. loop transfer

$$Ho(s) = GF(s) = \frac{G}{1+\tau s} \tag{1}$$

closed loop transfer

$$H(s) = \frac{Ho(s)}{1 + Ho(s)} = \frac{\frac{G}{1+\tau S}}{1+\frac{G}{1+\tau s}} \tag{2}$$

$$2BL = \frac{1}{2\pi j} \int_{-j\infty}^{+j\infty} |H(s)|^2 \, ds \tag{3}$$

$$\tau = \frac{G}{4\,BL} \tag{4}$$

Minimum Gain and BL specified

fo AGC Loop 3DB Bandwidth $= \frac{BL}{1.57}$ for single pole closed loop response

Figure 3.2.2.24. AGC Loop Design Summary

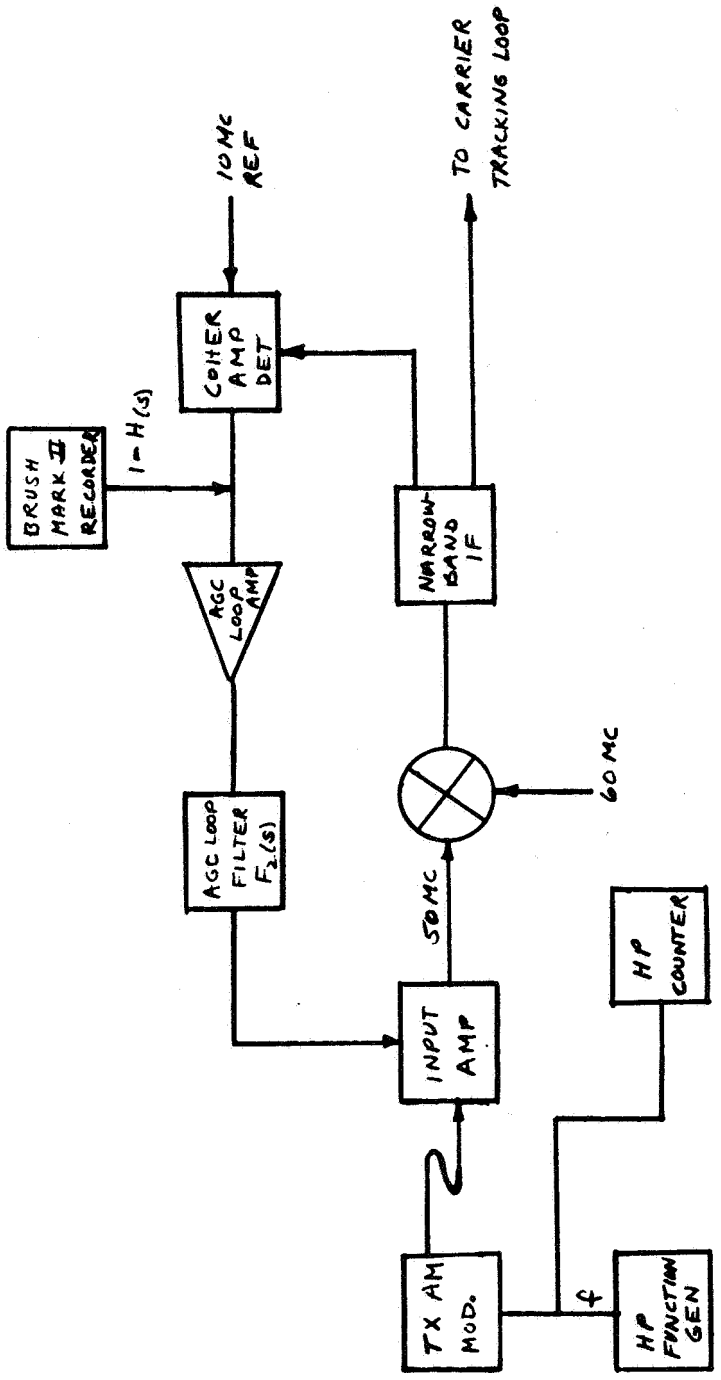
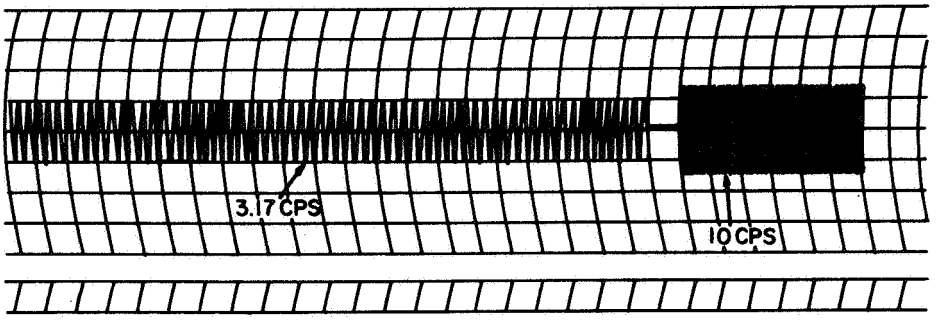
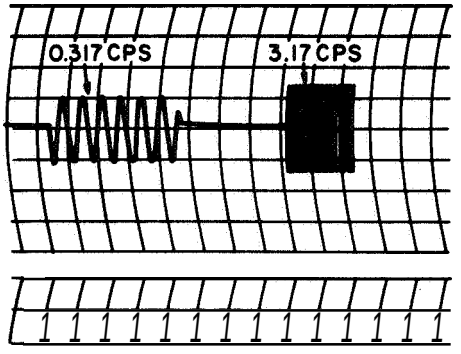


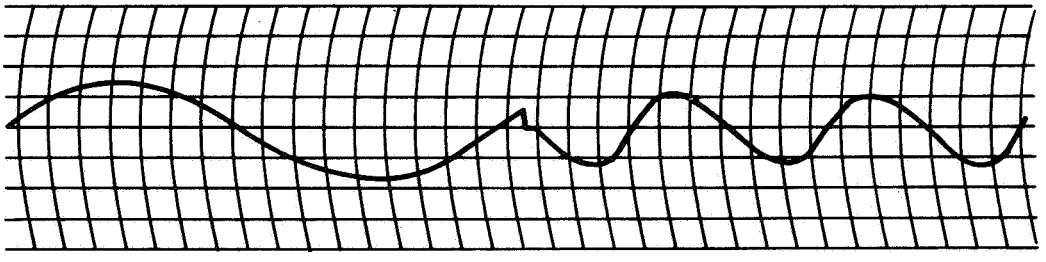
Figure 3.2.2.25. P.M.RCVR AGC Loop Bandwidth Test System



2 BL = 10.0 CPS
f_o = 3.17 CPS



2BL = 1.0 CPS
f_o = 0.317 CPS



2 BL = 0.1 CPS
f_o = 0.0317 CPS

Figure 3.2.2.26. P. M. Receiver AGC Loop Bandwidth Plots

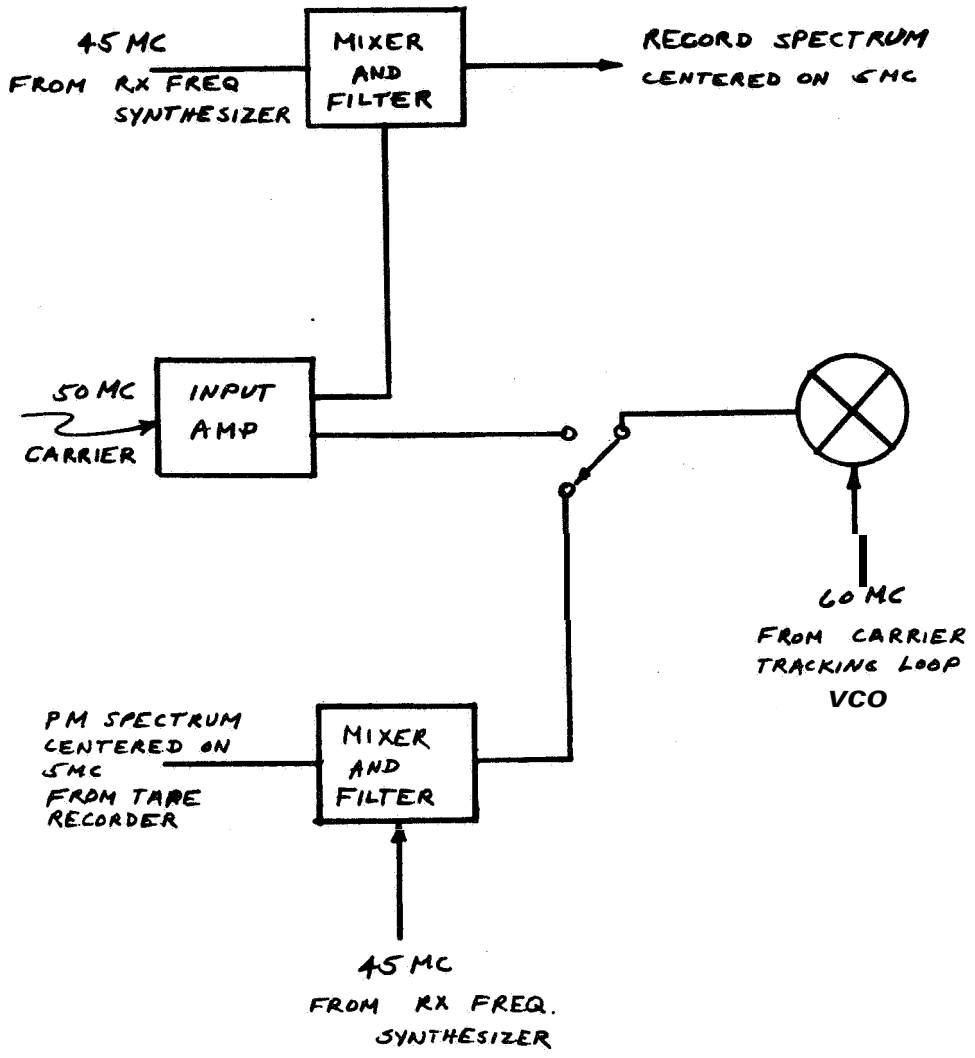
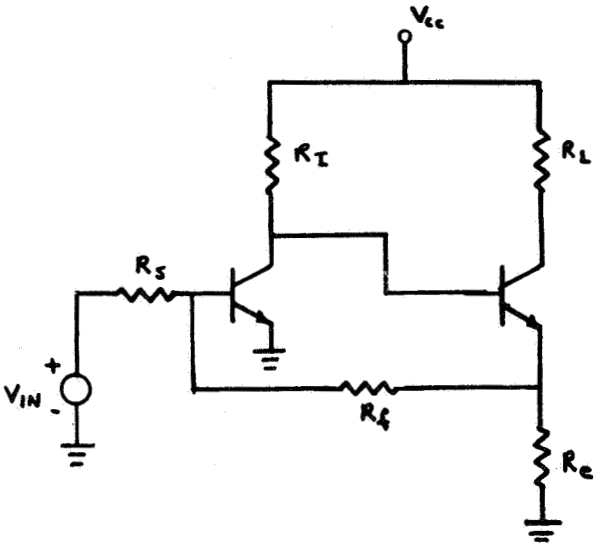


Figure 3.2.2.27. P. M. RCVR PreDetection Record and Playback



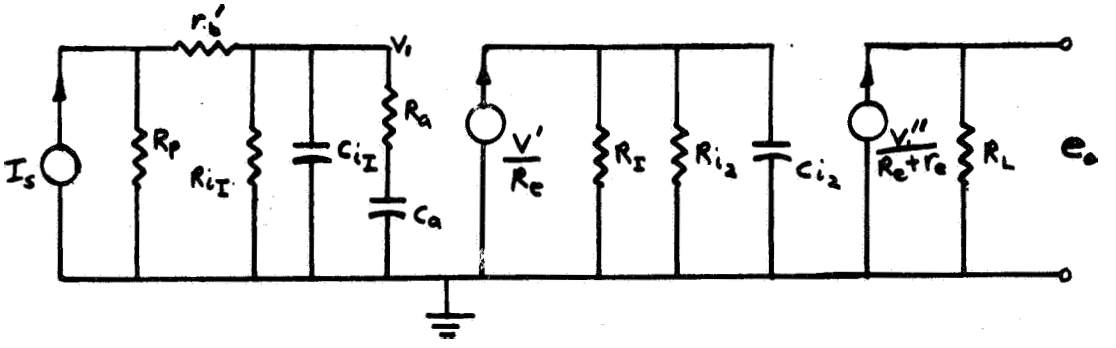


Figure 3. 2.2.28. Feedback Pair Characteristics

Equation (58) is recognized as the familiar quadratic in which a proper choice of the damping coefficient yields a two pole Butterworth (maximally flat amplitued) response. The poles p_1 and p_2 are contributed by the two transistors shown in figure 3.2.2.28. The root locus diagram of the system is shown in figure 3.2.2.29.

Figure 3.2.2.30 shows a typical amplitude response of 3 cascaded low power units used in the R. F. Test Console. In the region of 10 and 50 Mc the phase response is linear. The ratio of open to closed loop gain is 25 DB (for a closed loop gain of 15 DB) at 50 Mc. The inband intermodulation products are a minimum of -60 DB with respect to either of two equal tones when the total peak output power is within rating. The closed loop gain is easily changed (equation 59) by selection of feedback resistors. The closed loop gain and bandwidth are resistant to power supply and temperature variations. In summary, this relatively simple, basic amplifier provided a means of combating the stringent R. F. Test Console specifications.

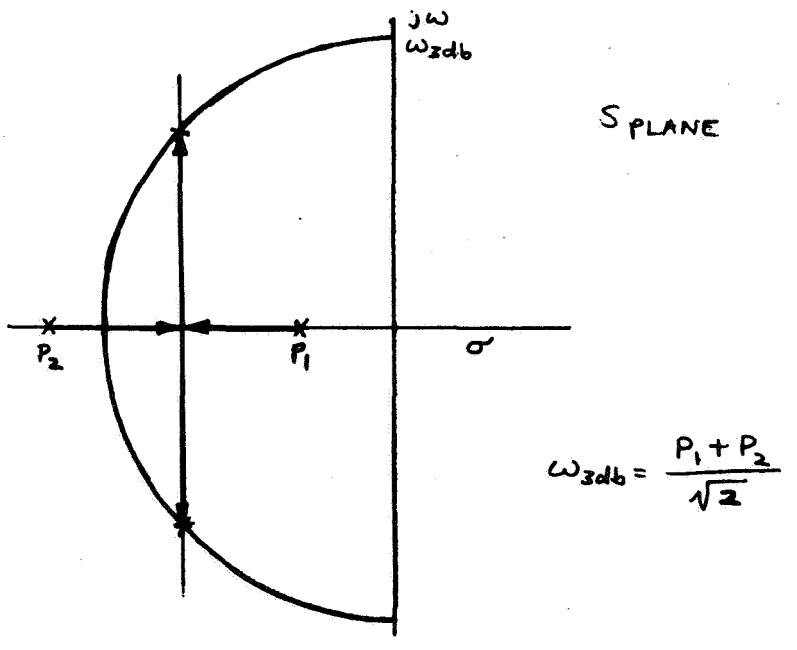


Figure 3.2.2.29. Feed Back Pair Root Locus

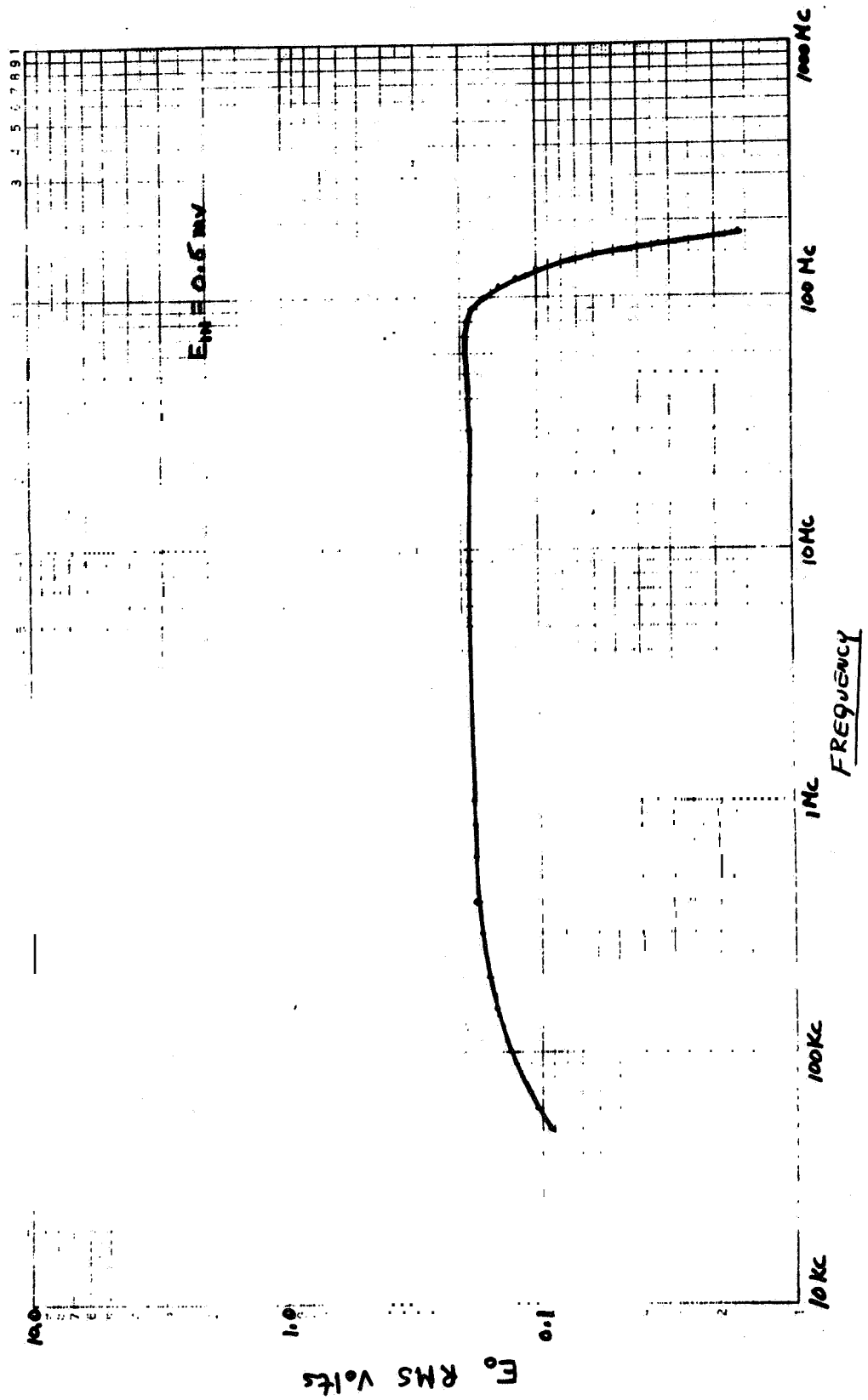


Figure 3.2.2.30. Amplitude Response of 3 Cascaded Feedback Pairs

3.3 F.M. SUBSYSTEM

The F. M. Subsystem specifications are listed in Table 2.4.1. The F, M. transmitter/receiver pair residual F. M. was measured as follows: the transmitter was deviated a known frequency excursion and the receiver output voltage measured. Subsequently, the receiver output noise voltage was measured with no intentional transmitter frequency deviation. A simple ratio between the measured receiver noise voltage and *signal* voltage yields a measure of the residual F. M. The technique is outlined by the following relationships:

$$V_{o(SIG)} = K \Delta f_{(SIG)} \tag{60}$$

$$B = \frac{\Delta f}{f_m \cdot 0.707} \tag{61}$$

$$\therefore V_{o(SIG)} = K B f_m \cdot 0.707 \tag{62}$$

$$V_{o(NOISE)} = K \Delta f_{(NOISE)} \tag{63}$$

$$\frac{V_{o(NOISE)}}{V_{o(SIG)}} = \frac{K \Delta f_{(NOISE)}}{K B f_m \cdot 0.707} \tag{64}$$

$$\therefore \Delta f_{(NOISE)\,Rms} = \frac{V_{o(NOISE)} \cdot B \cdot f_m \; 0.707}{V_{o(SIG)}} \tag{65}$$

The modulation index, B, was conveniently chosen as 2.4, the first carrier null as observed on the spectrum display. The baseband tone (fm) was chosen as a midband frequency. The peak-to-peak transmitter frequency deviation $[\Delta f\ (SIG)]$ was purposely chosen much larger than $[\Delta f\ (NOISE)]$ such that the ratio $\frac{V_o\ (SIG)}{V_o\ (NOISE)}$ reflects accurate and separate receiver signal and noise output voltages. Admittedly, V_o *(SIG)* is a measure of V_o(SIG) plus V_o (NOISE).

The results of this measurement are outlined in figure 3.3.1. Note that combinations of data include the noise measured in both 100 and 500 Kc bandwidths. Further, combinations of AFC and Non AFC transmitter operation coupled with both the phase locked and conventional F. M. Receiver are included

The residual F. M. listed exceeds the specification shown in Table 2.4.1. Further, there is little difference between the residual F. M. measured with the transmitter in either AFC or the Non-AFC mode. In defense of the system, the latter characteristic is not surprising as the TX AFC system reduces the residual F. M. over a small bandwidth adjacent to the carrier and its influence is not particularly noticeable when the measurement is made in either 100 Kc or 500 Kc bandwidth Apart from that, the output noise measured was devoid of spurious and other extraneous signals. Further, care was taken to design an F. M. transmitter with minimum residual F. M. and a low noise receiver with reasonably large slope sensitivity discriminators. Although the residual F. M. was reduced considerably during the course of the development, it was not reduced to the specified level.

The transmitter/receiver pair static linearity test set-up and test data is shown in figure 3.3.2 and 3.3.3. This test is relatively simple, whereby an accurately measured D. C. voltage used to modulate the transmitter is plotted versus the recovered voltage from the receivers.

The data indicates both a linear transmitter and receiver. This characteristic could not have been achieved without linearizing both the transmitter and phase lock receiver voltage controlled oscillators with feedback. This technique is outlined in detail later in the report.

The transmitter/receiver pair dynamic linearity was tested as outlined in figure 3.3.4. Two dynamic linearity tests were conducted; namely, the two tone test and noise loading tests. From a system point of view it is interesting to note that the dynamic linearity and residual F. M. requirements are in conflict. Initially, the transmitter and phase locked receiver "voltage controlled oscillators" (closed loop systems) were synthesized with extremely linear, low slope sensitivity, discriminators within the feedback loop. This design resulted in two tone intermodulation products at least -50 db with respect to either of two equal tones. Further, the noise loading tests revealed slot ratios in excess of 50 db. However, this type of system exhibited a large residual F. M. Therefore, a compromise was made to increase discriminator slope sensitivity at the expense of linearity to reduce the residual F. M. The slope sensitivity was tailored such that the system met the dynamic linearity specification; however, the residual F. M. was not reduced to within specification limits, as outlined earlier. The intermodulation components (two tone tests) are shown to be in excess of -40 db with respect to either of two equal tones. The intermodulation level can be related to the

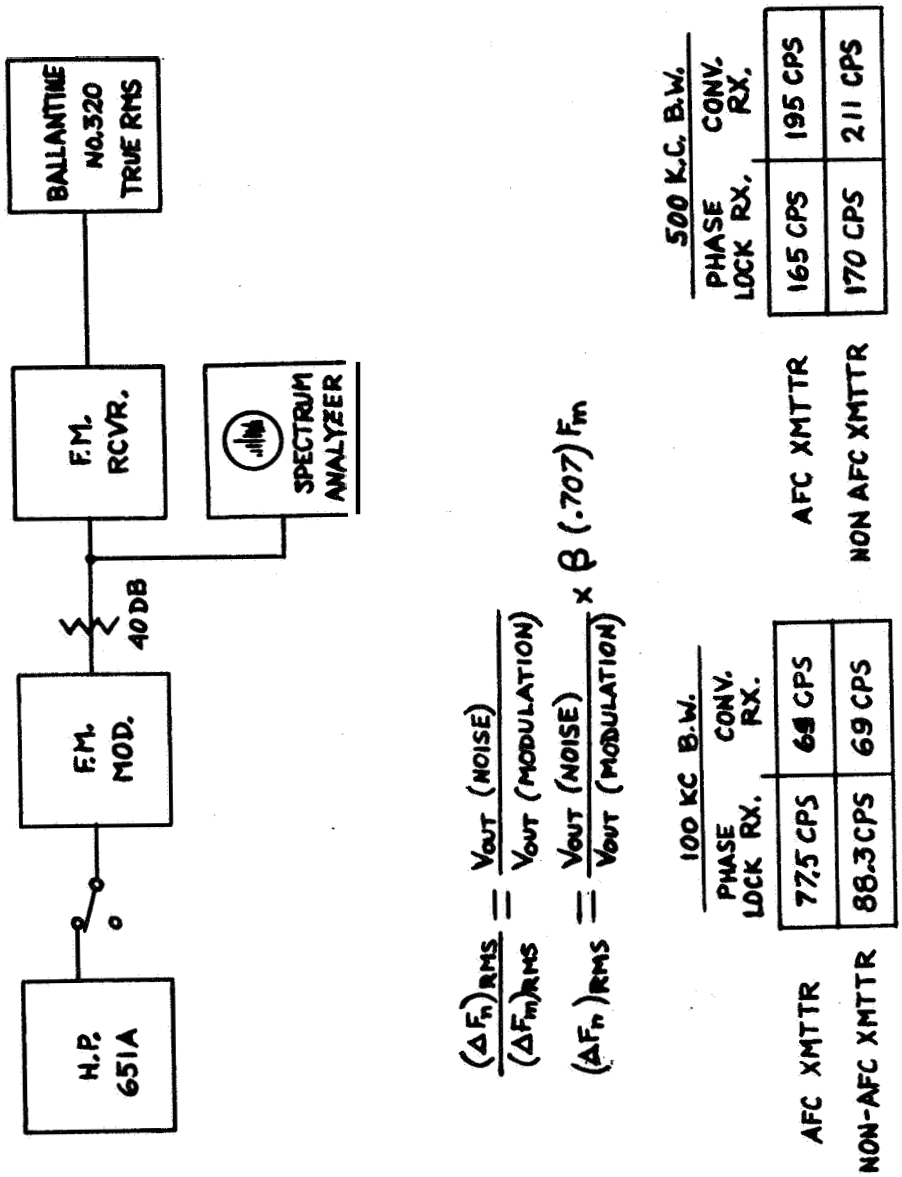


Figure 3.3.1. F.M. Subsystem Residual F.M. Test

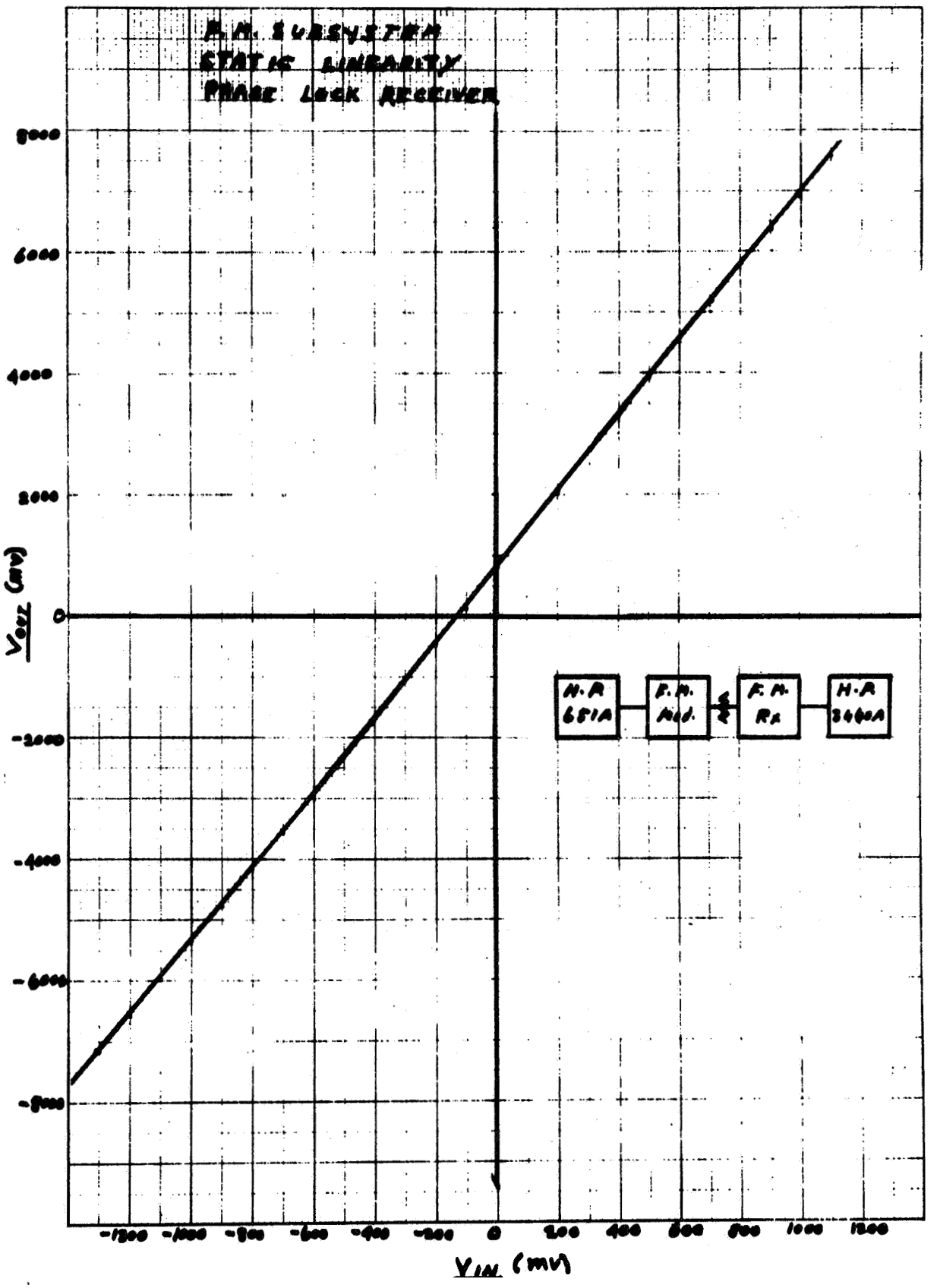


Figure 3.3. 2. F. M. Subsystem Static Linearity Phase Lock Receiver

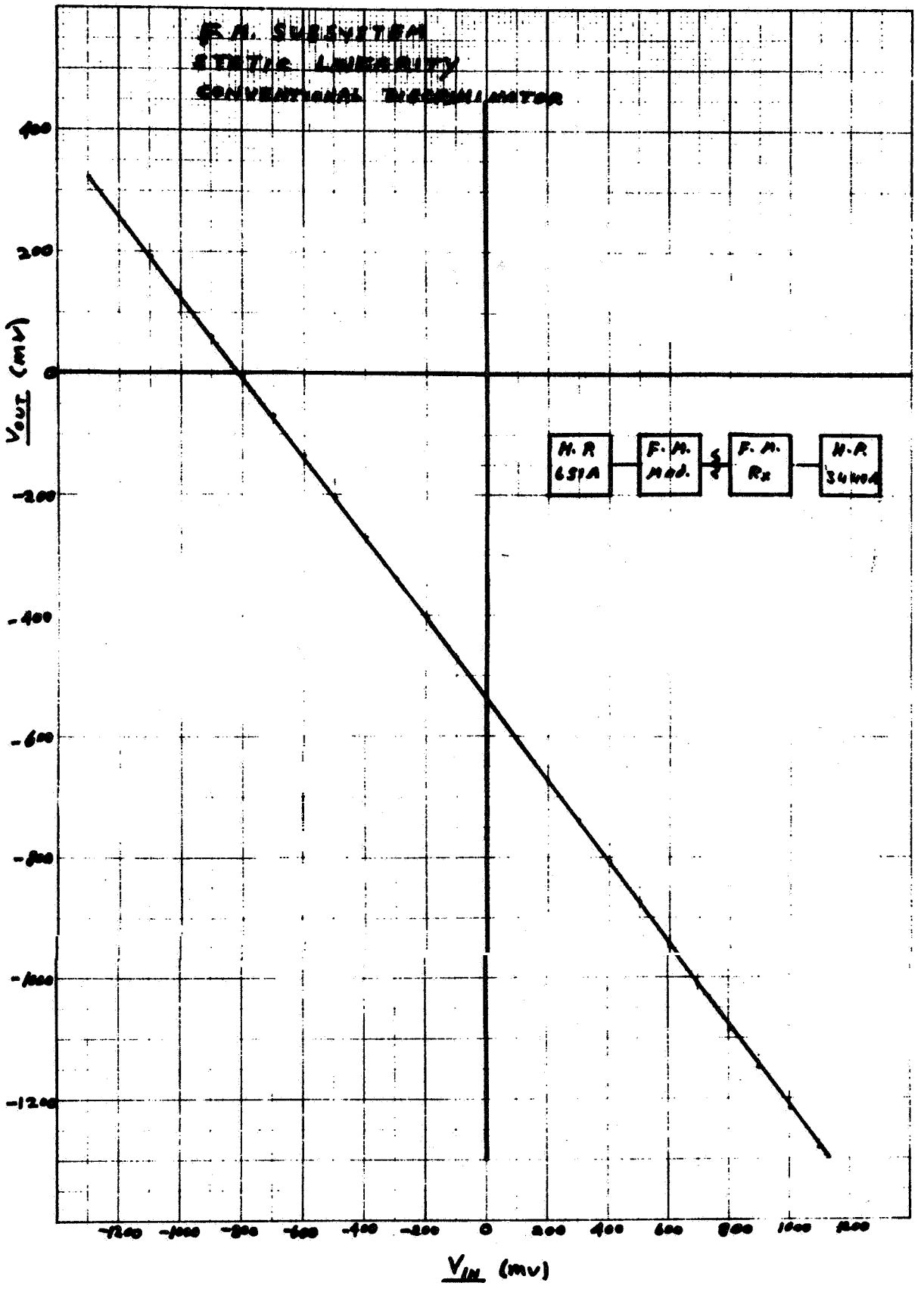


Figure 3.3.3. F. M. Subsystem Static Linearity Conventional Discriminator

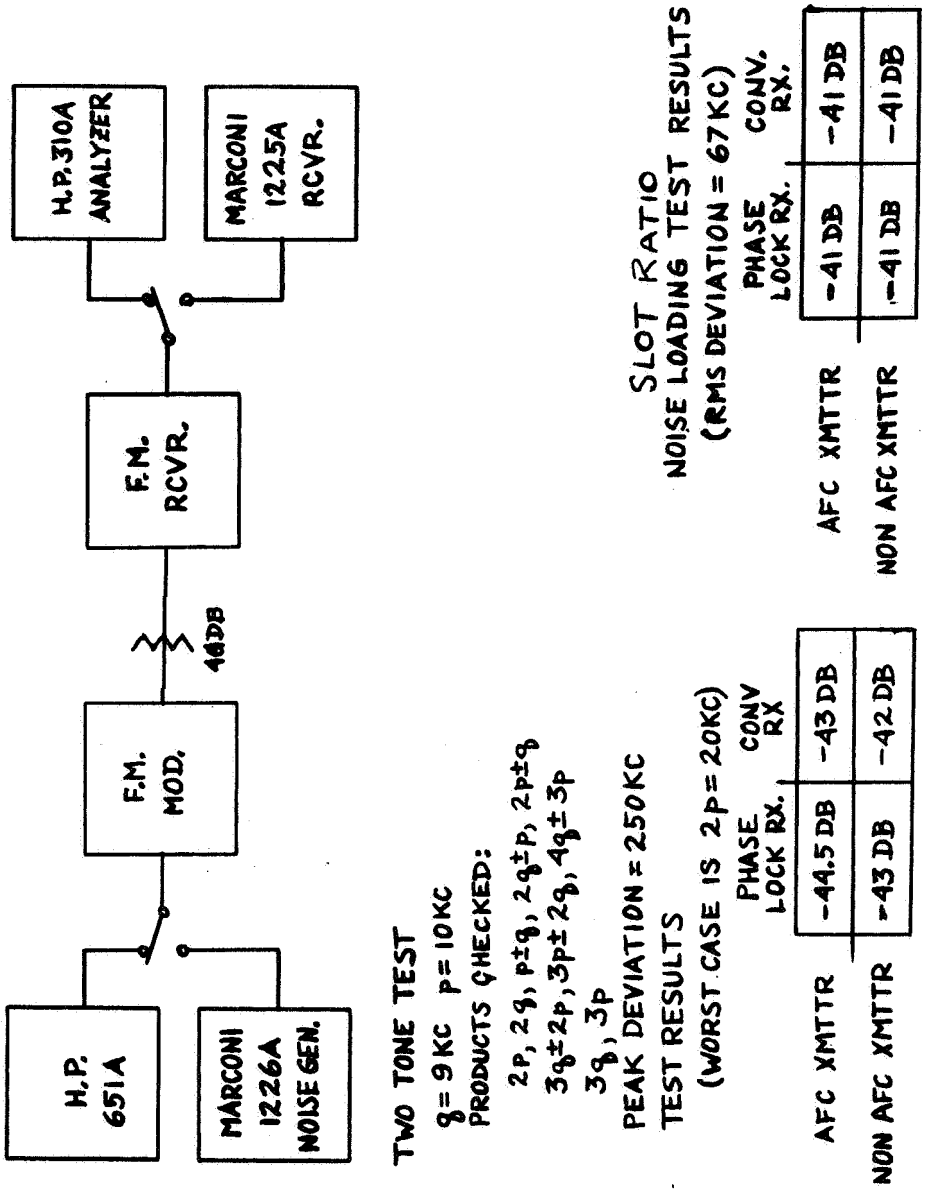


Figure 3.3.4. F. M. Subsystem Dynamic Linearity

Taylor Series coefficients whereby second order (and higher) coefficients are less than 1/100 of the desired first order coefficient. This interpretation of -40 db components indicates one per cent linearity.

3.3.1 F. M. Modulator

The F. M. Modulator block diagram is shown in figure 2.4.11 and the principal specifications are listed in Table 2.4.1.1. As shown, the modulator is comprised of a two loop system. The minor, narrow band loop contributes carrier stabilization and the major, wide-band loop provides a means of synthesizing the transfer function of output frequency to base-band input. The major loop also transfers the linearity of the discriminator to the VCO within the loop constraints. Figure 3.3.1.1 indicates the linear frequency model of the major loop.

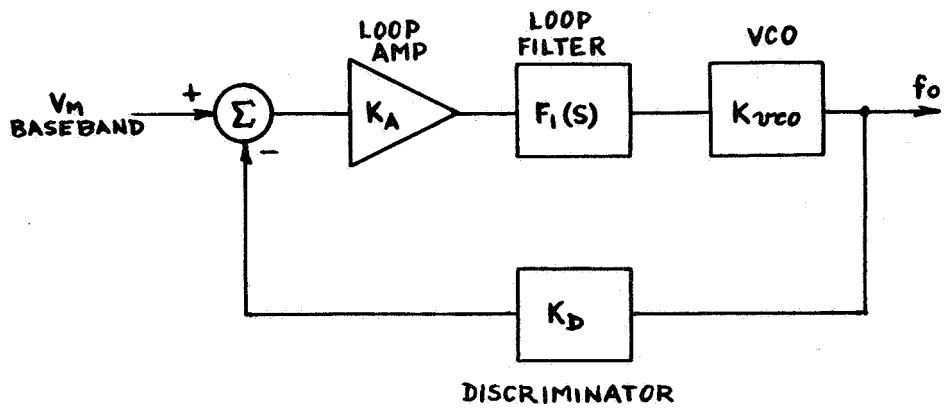


Figure 3.3.1.1. Linear Frequency Model F. M. Transmitter, Major Loop

The transfer function of output frequency to baseband input is:

$$\frac{f_o}{V_m}(s) = \frac{K_A K_{vco} F_1(s)}{1+K_A K_{vco} K_D F_1(s)} \tag{66}$$

$$\text{LET } K_P = K_A K_D K_{vco} \tag{67}$$

Then

$$\frac{f_o}{V_m}(s) = \frac{1}{K_D}\left[\frac{K_p F_1(s)}{1+K_p F_1(s)}\right] \tag{68}$$

The open loop gain K_p, and loop filter, $F_1(s)$, are optimized to form a closed loop transfer function that yields a two pole Butterworth response. The loop filter is of the form shown by equation 69.

$$F_{1(s)} = \frac{1}{\left(\frac{S}{W_1} + 1\right)\left(\frac{S}{W_2} + 1\right)} \tag{69}$$

The root locus diagram of the system is indicated by figure 3.3.1.2. The closed loop transfer function synthesized is as listed in equation 70.

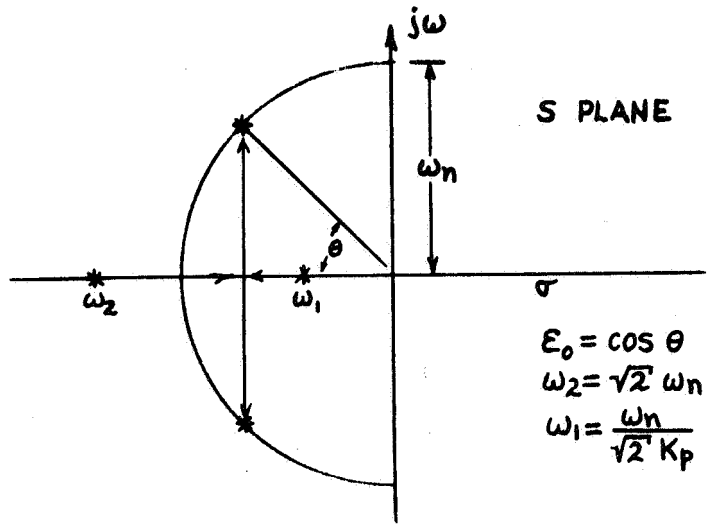


Figure 3.3.1.2. Root Locus Diagram F. M. Modulator, Major Loop

$$F_{c(s)} = \frac{1}{\left(\frac{S^2}{W_n^2} + \frac{2\varepsilon}{W_n} s + 1\right)} \tag{70}$$

Substituting equation 69 in 68, the closed loop transfer function is written in terms of the open loop gain and loop filter. Equation 71 results:

$$\frac{F_o}{V_m}(s) = \frac{1}{K_D}\left[\frac{1}{\frac{1}{K_p}\left(\frac{S}{W_1} + 1\right)\left(\frac{S}{W_2} + 1\right) + 1}\right] \tag{71}$$

$$\frac{f_o}{V_m}(s) = \frac{1}{K_D}\left[\frac{1}{\frac{S^2}{K_p W_1 W_2} + \frac{1}{K_p}\left(\frac{1}{W_1} + \frac{1}{W_2}\right) S + 1 + \frac{1}{K_p}}\right] \tag{72}$$

The open loop parameters K_P, W_1 and W_2 are computed in terms of the closed loop parameters W_n and ξ by equating equation 72 to equation 70 and equating coefficients of like powers of S The constant term, K_D, is independent of frequency and is not retained

$$\frac{1}{\frac{S^2}{K_p W_1 W_2} + \frac{1}{K_p}\left(\frac{1}{W_1} + \frac{1}{W_2}\right) S + 1 + \frac{1}{K_P}} - \frac{1}{\frac{S^2}{W_n^2} + \frac{2\xi}{W_n} S + 1} \tag{73}$$

A large open loop gain is assumed such that $1/K_P$ approaches zero.

$$K_p W_1 W_2 = W_n^2 \tag{74}$$

$$\frac{1}{K_p}\left(\frac{1}{W_1} + \frac{1}{W_2}\right) = \frac{2\xi}{W_n} \tag{75}$$

Three unknowns K_P, W_1 and W_2 must be found; however, only two equations are available. In a practical sense the loop gain (K_P) is assigned as large a value as possible within the constraints of the hardware limitations and the loop filter poles, W_1 and W_2 are solved in terms of K_p, W_n and ξ. Equations 76 and 77 result.

$$W_1 = \frac{W_n}{\sqrt{2}\, K_p} \tag{76}$$

$$W_2 = \sqrt{2}\, W_n \tag{77}$$

The closed loop cut off frequency, W_n is selected such that the amplitude response $\left[\frac{f_{o(s)}}{V_m}\right]$ is within specification (±0.5 db at 500 Kc). The experimental data achieved with this synthesis is shown in figure 3.3.1.3.

126

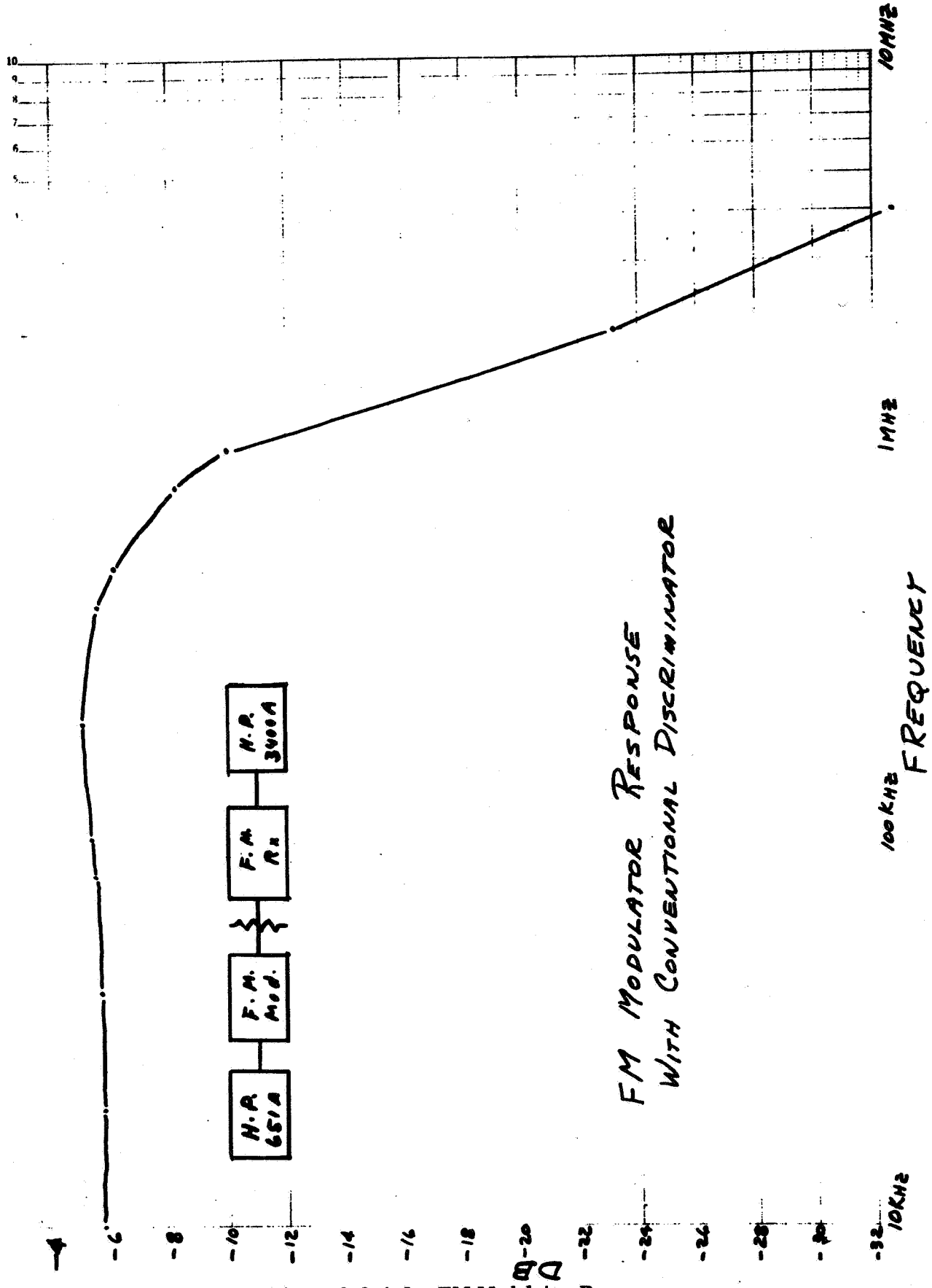


Figure 3.3.1.3. FM Modulator Response

Aside from providing a controlled transfer of output frequency to baseband input, the closed loop system corrects the VCO non-linearity, residual F. M. and frequency drift. If the latter three undesirable parameters are considered as a system input, (I_D), (a linear system assumed) the loop correction is examined as follows:

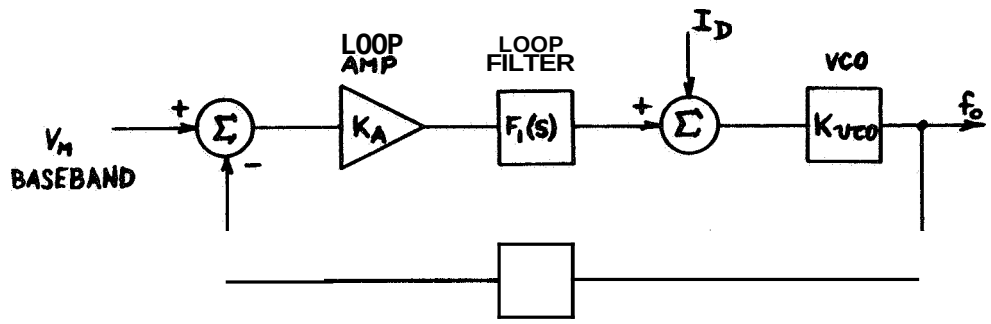


Figure 3.3.1.4. Linear Frequency Model With Simulated VCO Input

$$\frac{f_o}{I_D}(s) = \frac{K_{VCO}}{1 + K_{VCO} K_D K_A F_1(s)} \tag{78}$$

$$\text{LET } K_p = K_{VCO} K_A K_D \tag{79}$$

$$\frac{f_o}{I_D}(s) = \frac{1}{K_A K_D}\left[\frac{K_p}{1+K_p F_1(s)}\right] \tag{80}$$

$$\frac{f_o}{I_D}(s) = \frac{1}{K_A K_D}\left[\frac{1}{\frac{1}{K_p} + F_1(s)}\right] \tag{81}$$

$$\text{ASSUME } K_p >> 1,\ F_1(s) = \frac{1}{\left(\frac{S}{W_1} + 1\right)\left(\frac{S}{W_2} + 1\right)} \tag{82}$$

$$\frac{f_o}{I_D}(s) = \frac{1}{K_A K_D}\left(\frac{S}{W_1} + 1\right)\left(\frac{S}{W_2} + 1\right) \tag{83}$$

The Bode diagram of equation 83 is shown in figure 3.3.1.5.

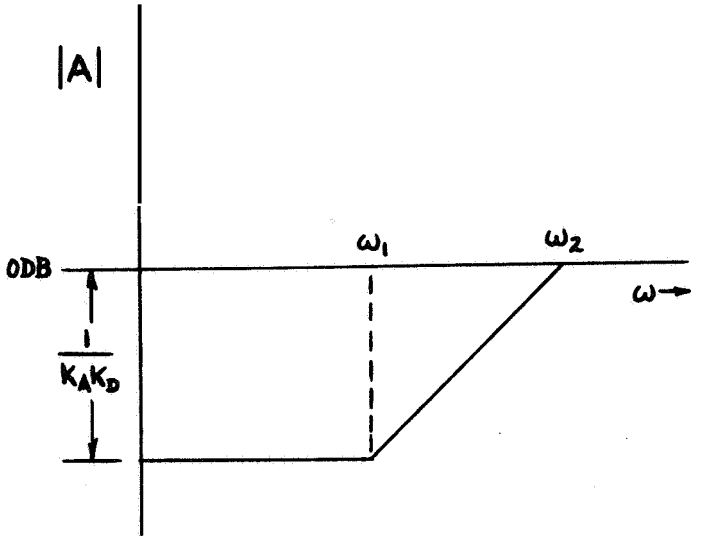


Figure 3.3.1.5. Bode Diagram, VCO Correction

This simple diagram reveals essential loop gain data. The VCQ non-linearities are attenuated by the product of the discriminator and loop amplifier gains. Therefore, in assignment of the gain gradient around the loop, the following is evident. The VCQ gain should be minimized and the loop amplifier and discriminator gains should be maximum within hardware constraints. Further, the discriminator and amplifier should be linear and contribute minimum noise. If these simple precautions are not considered the closed loop system may well degrade the VCO characteristics.

The closed loop system outlined exhibits a controlled transfer identical to an open loop VCQ. Therefore, the wideband closed loop system can be considered as the VCO in the narrow band carrier stabilization loop shown in figure 3.3.1.6.

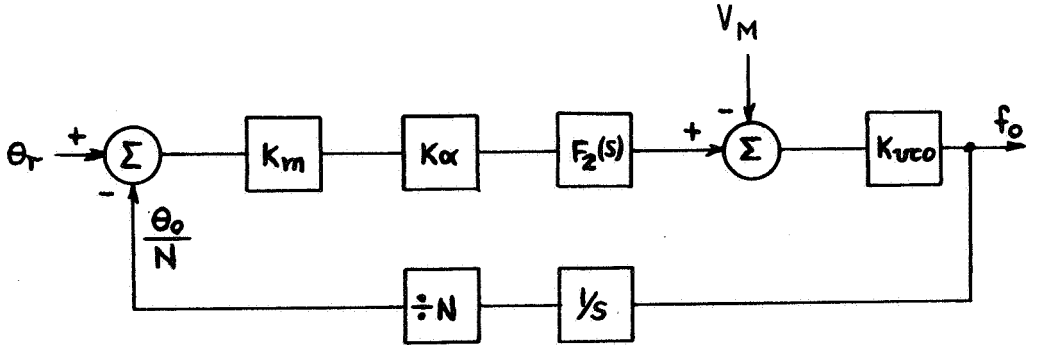


Figure 3.3.1.6. Linear Phase Model, F. M. Modulator Carrier Stabilization Loop

The transfer of output frequency to baseband input is:

$$\frac{f_o}{V_m}(s) = \frac{K_{vco}}{1 + \frac{K_{vco}}{N} K_m K_\alpha \frac{F_2(s)}{S}} \tag{84}$$

$$\text{Let } G = \frac{K_{vco} K_\alpha K_m}{N} \tag{85}$$

$$\text{Then } \frac{f_o}{V_m}(s) = \frac{K_{vco}}{1 \quad G \frac{F_{2(s)}}{S}} \tag{86}$$

Let $F_{2(s)} = 1$ (NO LOOP FILTER)

$$\frac{f_o}{V_m}(s) = \frac{K_{vco}}{1 + \frac{G}{S}} = \frac{K_{vco}}{G} \cdot \frac{S}{\frac{S}{G} + 1} \tag{87}$$

A transfer independent of frequency results by adding the following pre-emphasis network at the baseband input.

$$\frac{V'_m}{V_m} = \frac{\frac{S}{G} + 1}{S} \tag{88}$$

The network described by equation 88 requires a perfect integrator. This is not realizable but an approximation is adequate to extend the low frequency response to meet the amplitude response specification at 3 cps. The pre-emphasis network chosen exhibits the following transfer function:

$$\frac{V_{m'}}{V_m} = \frac{\frac{S}{W_3} + 1}{\frac{S}{W_o} + 1} \tag{89}$$

The zero, W_3, is equal to G and W_o was selected to extend the low frequency response beyond 3.0 cps. The overall transfer function indicated by equation (90) results:

$$\frac{f_o}{V_{m'}}(s) = \frac{K_{vco}}{G}\left[\frac{\frac{S}{G}}{\frac{S}{G}+1}\right]\left[\frac{\frac{S}{W_3}+1}{\frac{S}{W_o}+1}\right] = \frac{K_{vco}}{G}\left[\frac{S}{\frac{S}{W_o}+1}\right] \qquad (90)$$

The Bode diagram of the overall transfer function is shown in figure 3.3.1.7.

In a practical sense the loop gain G $\left(\text{and loop bandwidth}\left(\frac{S}{G}+1\right)\right)$ was chosen as 50 cps to correct for oscillator instabilities. The compression factor, N, was chosen as 512, thus limiting the allowing modulation index to 512. The phase reference, θr, is derived from the transmitter reference frequency standard. The pre-emphasis network was mechanized as an active filter,

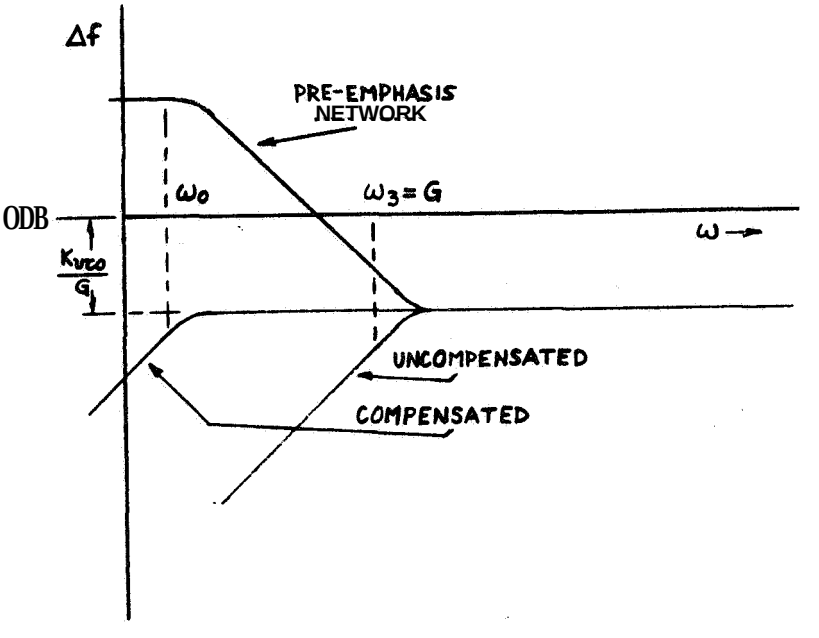


Figure 3.3.1.7. F. M. Modulator Low Frequency Response, Compensated For Carrier Stabilization Loop

Table 3.3.1.1. F.M Modulator Nomenclature

PARAMETER	DIMENSION	DEFINITION
V_m	VOLTS	BASE BAND INPUT
$V_{m'}$	Volts	Baseband Input With Pre-emphasis
K_A	Volts/Volt	Amplifier Gain
K_{VCO}	Cycles/Sec	VCO Gain
K_D	Volts/Radian	Discriminator Gain
f_o	Cycles/Sec	Output Frequency Deviation
N		Counter Division Ratio
W_n	Radian/Sec	Closed Loop Cutoff Frequency
θr	Radian	Reference Phase
E		Damping Factor of Complex Pole Pair
W_1	Radian/Sec	Open Loop Real Pole
W_2	Radian/Sec	Open Loop Real Pole
K_P	Volts/Volt	Loop Gain Constant
K_α	Volts/Volt	APC Amplifier Gain
G	1/Seconds	APC Loop Gain Constant
W_o	Radians/Second	Low Frequency Cutoff Frequency with Pre-Emphasis
W_3	Radians/Second	Low Frequency Cutoff Frequency without Pre-Emphasis

3.3.1.1 F. M. Modulator Components

The F. M. Modulator VCO was designed in a Clapp configuration. The parameters of this circuit are outlined in Section 3.1 of this report and are not repeated here. The unit was designed to exhibit minimum residual F. M. However, the oscillator transfer of $\frac{\Delta f_o}{V_m}$ is inherently non-linear. Therefore, the feedback system described was utilized. The peak frequency deviation was specified as 500 Kc which dictated a rather low Q, L/C oscillator. The resultant long term stability was poor, as a result the carrier stabilization system was used. The closed loop VCO transfer is shown in figure 3.3.1.8.

The loop discriminator was designed as a conventional unit, whereby the slope sensitivity and bandwidth was tailored to fit the intermodulation and residual F. M. specifications. Initially a very linear, low slope sensitivity, delay line discriminator was utilized. Unfortunately, the resulting time delay ruined the closed loop response and the unit could not be used. A limiter precedes the discriminator in the major loop.

The Burr Brown Model 1510 operational amplifiers were selected as the loop amplifiers. These units were chosen for their gain bandwidth product and low noise characteristics.

The feedback divider chain (N = 512) consists of two high speed dividers (designed for this project) plus cascaded Fairchild integrated circuit DT μL950 flip-flops to achieve the total division of 512.

3.3.2 F. M. Receiver

The F. M. Receiver Block diagram is shown in figure 2.4.2.1. As shown in figure 2.4.2.1, the receiver R. F. Section includes a low noise input amplifier, selectable passive filter and limiter. A conventional and phase lock discriminator plus selectable output filters provide the baseband circuitry. The predetection record and playback circuitry included in the P. M. Receiver are time shared with the F. M. Receiver.

3.3.2.1 Phase Lock Discriminator AFC Loop

The system static and dynamic specifications dictate that the phase lock discriminator VCO exhibit a linear transfer of output frequency to baseband input. Therefore, the phase lock discriminator VCO was linearized by an auxiliary AFC loop in a manner similiar to that described in the previous F. M. Modulator section by equations (66) thru (77).

A principal difference between the two AFC loops merits an explanation. The transmitter AFC loops transfer function is modified by the narrow band carrier stabilization loop.

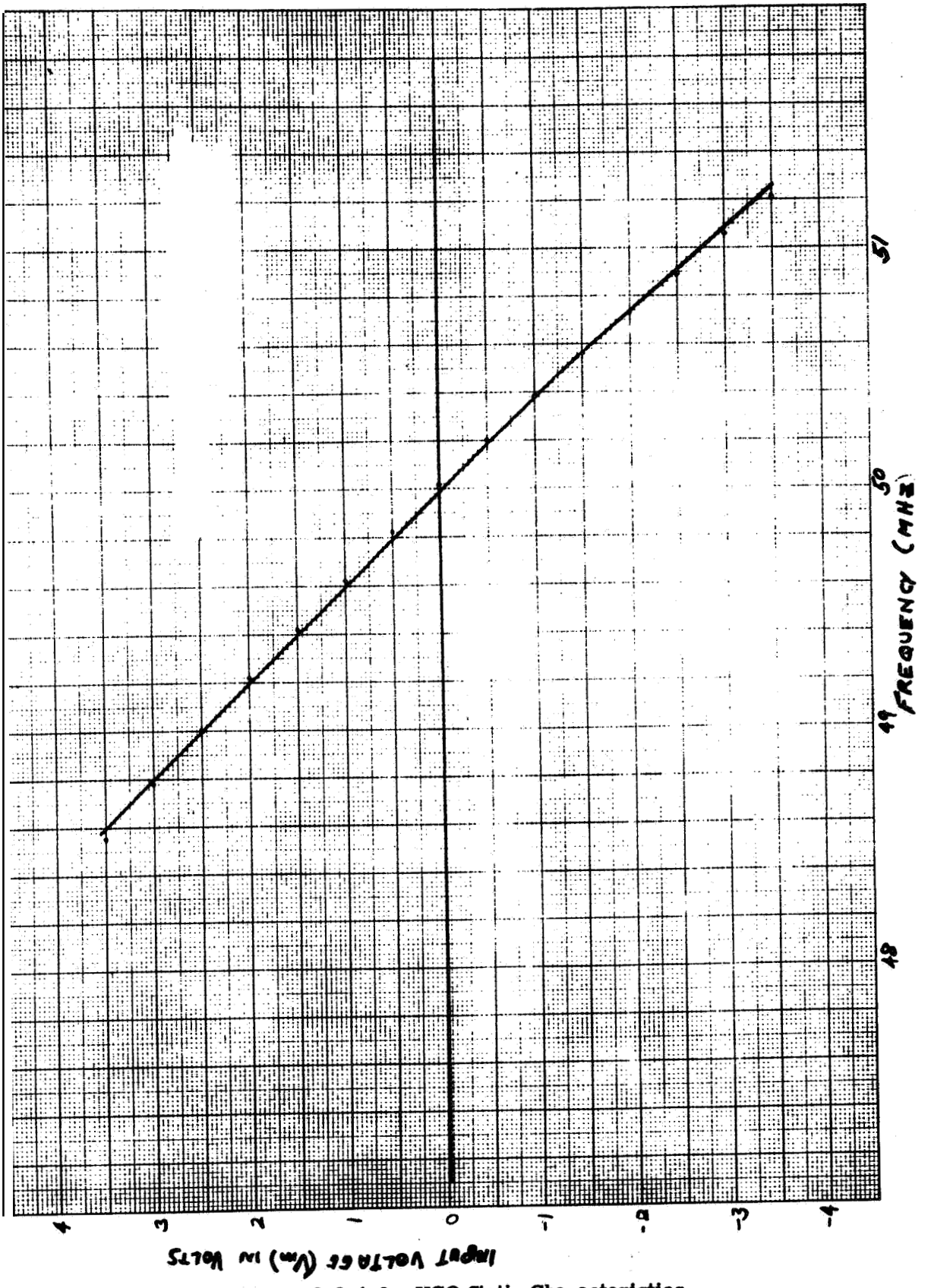


Figure 3.3.1.8. VCO Static Characteristics

However, the difference in the two loop bandwidths is very large and loop interaction is not a problem. The receiver AFC loop bandwidth is variable whereby the largest bandwidth is 300 Kc (at maximum limiter suppression). Therefore, the receiver two loop system posed a problem non-existant in the transmitter; namely, the AFC loop bandwidth must be sufficient not to interfer with the AFC loop transfer function. Aside from the AFC loop bandwidth constraint, it became evident that the AFC closed loop transfer function should ideally exhibit a single ~~real pole~~ at a much higher frequency than the largest APC loop information bandwidth. If this precaution was ignored, the AFC loop design would be modified by the AFC loop transfer function. As indicated later in this section, the loop interaction is still evident at the 300 Kc APC loop bandwidth.

The AFC loop reduction in the VCO residual F. M. is examined as follows. The VCO noise input I_D is assummed to be gaussian with a spectral density η . The comparison of the AFC case compared to the conventional VCO is examined The various notations shown in Table 3.3.2.1 are referenced.

Table 3.3.2.1. F. M. Receiver AFC Loop Nomenclature

NOTATION	DIMENSION	
I_D	volts	noise voltage at VCO input
f	cycles per second	frequency, an independent variable
f_1	cycles per sec.	AFC open loop corner frequency
K_P	dimensionless	AFC open loop gain
K_{vco}	cycles per volt second	VCO gain
η	watts per cycle per sec.	noise power spectral density at VCO input
$P_{o(f)}$	watts per cycle per sec.	noise power spectral density of residual F. M. out of VCO.
σ_1^2	watts	noise power of VCO output (residual F. M. with AFC)
σ_2^2	watts	noise, power of VCO output (residual F. M. with no AFC.)

$$\sigma_1^2 = 2\int_0^{500\ Kc} P_{o(f)}\, df \tag{98}$$

For the AFC case $P_{o(f)} = \eta \left| \frac{f_{o\,(f)}}{I_{D\,(f)}} \right|^2$ (99)

$$P_{o(f)} = \eta \left| \frac{K_{vco}}{K_p} \cdot \frac{1 + j f/f_1}{1 + j \frac{f}{K_p f_1}} \right|^2 \tag{100}$$

$$P_{o(f)} = \eta \left(\frac{K_{vco}}{K_p} \right)^2 \frac{1 + \left(f/f_1\right)^2}{1 + \left(\frac{f}{K_p f_1}\right)^2} \tag{101}$$

The upper limit of the specified bandwidth (500 Kc) is 3 times smaller than $K_p f_1$ (1.3 Mc); therefore:

$$P_{o(f)} \cong \eta \left(\frac{K_{vco}}{K_p} \right)^2 \left[1 + \left(f/f_1\right)^2 \right] \tag{102}$$

Substituting equation (102) in (98)

$$\sigma_1^2 = 2\eta \left(\frac{K_{vco}}{K_p} \right)^2 \int_0^{500\ KC} \left[1 + \left(f/f_1\right)^2 \right] df \tag{103}$$

$$\sigma_1^2 = 2\eta \left(\frac{K_{vco}}{K_p} \right)^2 f \left[1 + \frac{1}{3} \left(\frac{f}{f_1} \right)^2 \right]_0^{500\ Kc/s} \tag{104}$$

$$f_1 = 1.3' \quad 10^{+5} \tag{105}$$

$$\sigma_1^2 = 6.\ 10^{+6} \eta \left[\frac{K_{vco}}{K_p} \right]^2 \tag{106}$$

For the non AFC case:

$$\sigma_2^2 = 2\eta\,(K_{vco})^2 \int_0^{500\,Kc} df = 10^{+6}\eta\,(K_{vco})^2 \tag{107}$$

Then:

$$\frac{\text{F. M. NOISE WITHOUT AFC}}{\text{F.M. NOISE WITH AFC}} = \frac{\sigma_2^2}{\sigma_1^2} = \frac{10^{+6}\eta\left(K_{vco}\right)^2}{6.\,10^{+6}\eta\left(\frac{K_{vco}}{K_p}\right)^2} = \frac{K_p^2}{6} \tag{108}$$

The **design** value of K_p is **10**

$$\frac{}{\sigma_1^2} = 16.67 = 12.30B \text{ improvement} \tag{109}$$

3.3.2.2 Phase Lock Discriminator APC Loop

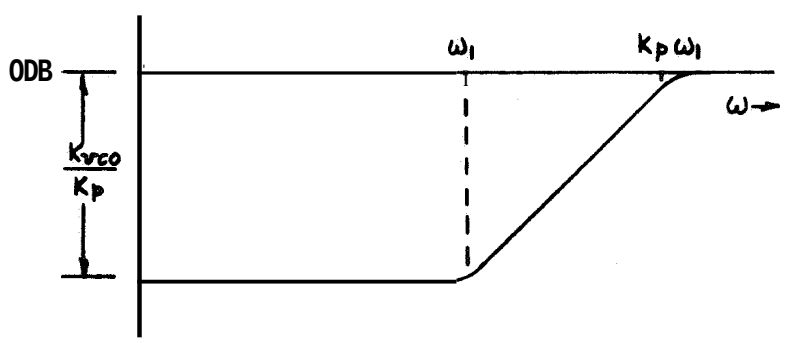


Figure 3.3.2.1 Bode Diagram VCO Correction F. M. Phase Lock Discriminator

7 Jaffe, L. and E Rechtin, **Design** and Performance of Phase Lock Loops Capable **of** Near Optimum Performance over a Wide Range of Input Signal and Noise Levels, Trans. IRE IT - **1** pp **66-76** March **1955.**

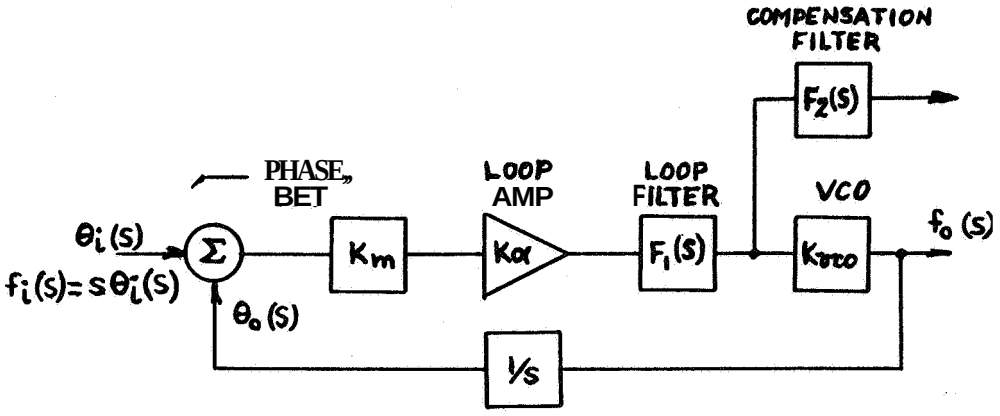


Figure 3.3.2.2. Block Diagram, Phase Lock Discriminator

The loop model is simplified as follows:

$$G_o = 2\pi\left(\alpha_o K_m K_\alpha K_{vco}\right)$$

Where G_o is the open loop gain at threshold and α_o is the limiter suppression. The linearized model shown in figure 3.3.2.3 results.

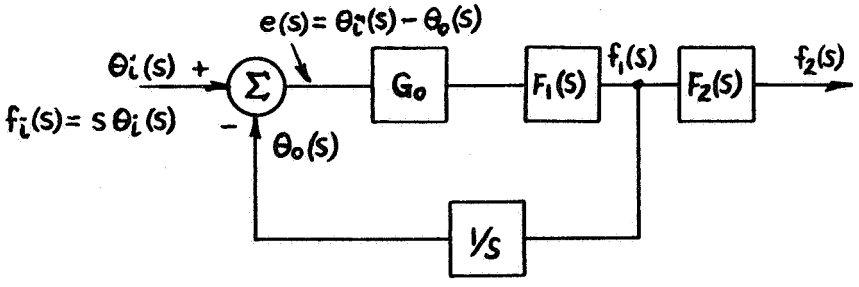


Figure 3.3.2.3. Phase Lock Discriminator Linearized Model

The loop filter time constants, τ_2 and τ_1, are listed as functions of the threshold open loop gain, G_o, and loop information bandwith, $\$$, as follows:

$$\tau_2 = \sqrt{2}/B_o \tag{110}$$

$$\tau_1 = G_o/B_o^2 \tag{111}$$

The loop filter is of the form:

$$F_{1(s)} = \frac{\tau_2 s + 1}{\tau_1 s} = B_o^2 \left(\frac{1 + \sqrt{2}/B_o}{G_{o(s)}} \right) s \tag{112}$$

The open loop transfer function is:

$$H_o(s) = \frac{\theta_o(s)}{e(s)} = \frac{B_o^2 \left(1 + \sqrt{2}/B_o \, s\right)}{s^2} \tag{113}$$

The closed loop transfer function becomes:

$$H(s) = \frac{H_o(s)}{1 + H_o(s)} - \frac{\theta_o(s)}{\theta_i(s)} - \frac{1 + \sqrt{2}/B_o \, s}{\frac{s}{B_o^2} + \frac{\sqrt{2}}{B_o} s + 1} \tag{114}$$

The previous equations are written in terms of phase parameters; however, the phase lock discriminator is a frequency demodulator. Therefore, the parameters are converted to frequency as shown.

$$f_{i(s)} = s\theta_{i(s)} \tag{115}$$

$$f_{1(s)} = s\theta_{o(s)} \tag{116}$$

The closed loop transfer function written in terms of frequency becomes:

$$\frac{f_{1(s)}}{f_{i(s)}} = \frac{S\,\Theta_{o(s)}}{S\,\Theta_{i(s)}} = \frac{1 + \sqrt{2}/B_o s}{\frac{S^2}{B_o^2} + \frac{\sqrt{2}}{B_o} S + 1} \tag{117}$$

Equation 117 includes a zero at $\sqrt{2}/B_o$ which is indicative of peaking in the overall phase lock demodulator response. Therefore, a second filter , $F_{2(s)}$, is added outside the loop to yield a response determined by the transfer function denominator.

$$F_{2(s)} = \frac{1}{\sqrt{2}/B_o\, S + 1} \tag{118}$$

$$\frac{f_{2(s)}}{f_{i(s)}} = \frac{f_{1(s)}}{f_{i\,s}} \cdot F_2(s) = \frac{1}{\frac{S^2}{B_o^2} + \frac{\sqrt{2}}{B_o}\, s + 1} \tag{119}$$

Equation 119 is of the form

$$\frac{1}{\frac{S^2}{W_n^2} \quad \frac{2\varepsilon}{W_n}\, s + 1} \tag{120}$$

Whereby $W_n = B_o$ and $\varepsilon = \frac{\sqrt{2}}{2} = 0.707$ (121)

The specified parameters include a no noise loop gain sufficient to constrain the loop static phase error to ± 10 degrees for a transmitter determing of ±500 Kc. The minimum loop gain is:

$$G = \frac{\Delta f}{\Theta_{ss}} = 1.8 \cdot 10^{+7}\ \frac{1}{\text{sec.}} \tag{122}$$

The no noise open loop gain G was designed as $3.14 \cdot 10^{+7}\ \frac{1}{\text{sec}}$ yielding a static phase error of 5.7 degrees for 500 Kc of transmitter detuning.

The limiter suppression factor[8] α_o is defined as follows:

$$\alpha_o^2 = \frac{1}{1 + \frac{4}{\pi}\left(N/S\right)_i} \tag{123}$$

The ratio N/S is the ratio of the predetection noise bandwidth to the two sided loop noise bandwidth $(2B_{lo})$. The predetection noise bandwidth is established by the receiver input filter. The two sided loop noise bandwidth is defined by equation 124, whereby $H_{(s)}$ is the closed loop transfer function at minimum loop gain.

$$2B_{lo} = \frac{1}{2\pi j}\int_{-j\infty}^{+j\infty} \left|H_{(s)}\right|^2 ds = 3.33\, f_o \tag{124}$$

Three loop information bandwidths (f_o) were specified, 3 Kc, 30 Kc and 300 Kc. The corresponding two sided loop noise bandwidths $(2\ B_{lo})$ are 20 Kc, 200 Kc and 2 Mc. The largest bandwidth input filter $(3DB_{B.W}$ of 1.0 Mc) determines the predetection bandwidth. The corresponding limiter suppression factors (α_o) are 0.15, 0.36, and 0.7.

In summary, the loop information bandwidth, loop gain, predetection noise bandwidth and loop two sided noise bandwidths were specified. The loop filter time constants and limiter suppression factors were computed.

3.3.2.3 Module Designs

This section includes the principal F. M. Receiver module design considerations. Modules designs that have been described in previous sections and are used in the F. M. Receiver are not repeated (phase lock discriminator VCO, feedback pair amplifiers). By the same token, module designs common to both the P. M and F. M Receivers that have not been described previously are listed in this section (low noise R. F. amplifier, limiter).

3.3.2.3.1 Input Filter and Amplifier (Code 405)

This module includes the low noise input amplifier and replaceable 50 Mc bandpass filter. Two low noise amplifier stages comprise the module input circuitry. The unit exhibits a 4DB noisefigureandcontributes 30 DB of gain. The receiver noise figure (aside

8 Davenport, W. B. Jr. Signal-to-Noise Ratios in Band Pass Limiters, J. Appl. Phys., Vol. 24, pp. 720-727, June 1953.

from oscillator stability) influences the transmitter/receiver pair residual F.M. discussed previously. The noise figure determines to some extent the magnitude of the receiver self noise and hence the ratio of S/N Summer noise and receiver self noise.

The first of the two low noise stages employs a matching transformer to match the sorce impedance to the transistor input impedance. The input circuitry is outlined in figure 3.3.2.4.

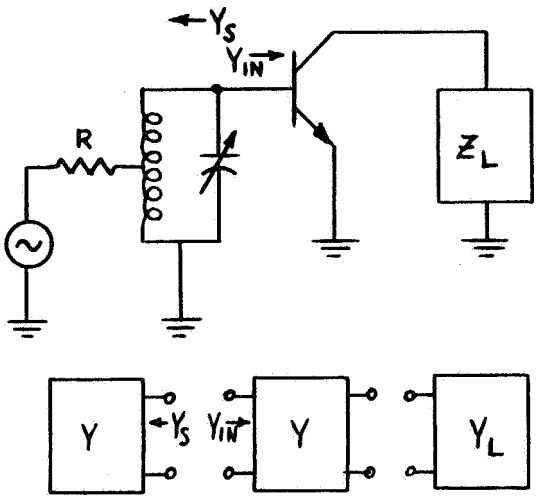


Figure 3.3.2.4. Low Noise Amplifier Input Circuit

The input circuit is designed[9] to yield a minimum noise figure. The transformed source admittance (Y_s) and transistor input admittance (Y_d are comprised of real and imaginary components as shown by equations 125 through 128.

$$Y_s = g_s \pm jbs \tag{125}$$

$$Y_{in} = g_{in} \pm jbin \tag{126}$$

$$Y_s + Y_{in} = (g_s + g_{in}) \pm (jbs \pm jbin) \tag{127}$$

$$\text{Let } jbs \pm jbin = c \tag{128}$$

9 "Principals of Noise", page 145 by J.J. Freeman.

Assuming correlation between the transistor base and collector noise generators, the noise figure can be expressed as follows:

$$N.F. = \frac{1 + R_{eq.}\left[(g_s + g_{in})^2 + (6^c - \sigma)^2\right]}{g_s} \qquad (129)$$

The coefficient, σ, is a function of the correlation between the base and collector noise generator and Req is an equivalent noise resistance referred to the input. Note that the noise figure is minimized not only as a function of gs (the source conductance) but also the total susceptance, c. For minimum noise figure, c must be positive (capacitive) and equal to σ. Experimentally, the latter characteristic was verified as the minimum noise figure was achieved when the input circuit was detuned from center frequency (50 Mc). Aside from the characteristics listed, collector to base feedback was added to the input amplifier to increase the amplifier bandwidth at a sacrifice of 0.5DB in noise figure.

3.3.2.3.2 Limiter (codes 408 and 409)

The F.M. R.F. Receiver section includes two cascaded limiters each with a limit range of -30DBM to ODBM. The basic diode limiter circuit is shown in figure 3.3.2.5.

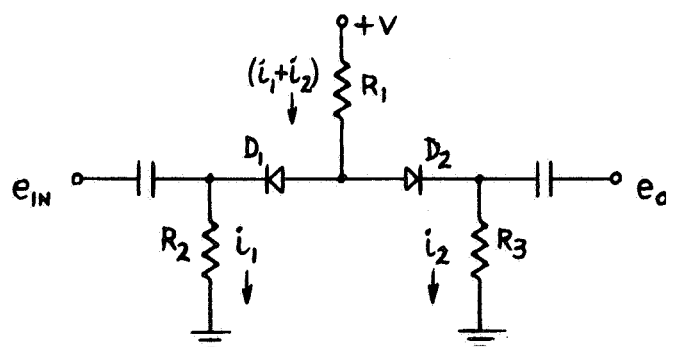


Figure 3.3.2.5. Basic R.F. Test Console Limiter Circuit

The resistor R_1 is large compared to R_2 and R_3 such that the current through R_2 and R_3 is supplied by a constant current source. In the absence of the input voltage (e_{in}), the current thru R_1 is evenly divided between R_2 and R_3. The input voltage, e_{in}, turns diode, D_1, on and off; therefore, the total current ($i_1 + i_2$) either flows thru R_3 or is evenly divided between R_2 and R_3. The peak-to-peak limiter output voltage (limit level) is $(V/_{R_1} \cdot R_2)$. The diode's dynamic resistance establishes the limiter insertion loss.

The basic limiter circuit and feedback pair amplifiers are arranged as shown in figure 3.3.2.6. to form a limiter module. Each amplifier gain is designed to absorb the preceeding limiter stage's insertion loss and maintain the limit range. The limiter stages are driven and loaded with emitter followers to minimize insertion loss.

Figure 3.3.2.6. R. F. Test Console Limiter Configuration

The amplifier gain gradient and limiter insertion loss gradient was carefully designed such that each amplifier's maximum output level is limited well below amplifier saturation for a limiter signal input dynamic range of -30DBM to 0 DBM. This simple precaution minimized the limiter A. M. to P. M. Conversion. Test results revealed that the amplifier exhibited excessive phase shift if operated near saturation. The basic limiter yielded eight degrees of carrier phase shift over a 30DB dynamic range of input signal at 10 Mc and fifteen degrees over the same dynamic range at 50 Mc. The broad band limiter exhibited a constant group delay (linear phase shift) from 5 to 15 Mc and 45 to 55 Mc at all carrier input levels within the power range of -30DBM to ODBM.

3.3.2.3.3 Phase Detector

A basic broadband power phase detector was developed for the R. F. Test Console. The unit was used at either of the two system frequencies of 10 Mc and 50 Mc. The unit was designed to exhibit minimum drift and offset voltage. A simplified diagram of the circuit is shown in figure 3.3.2.7.

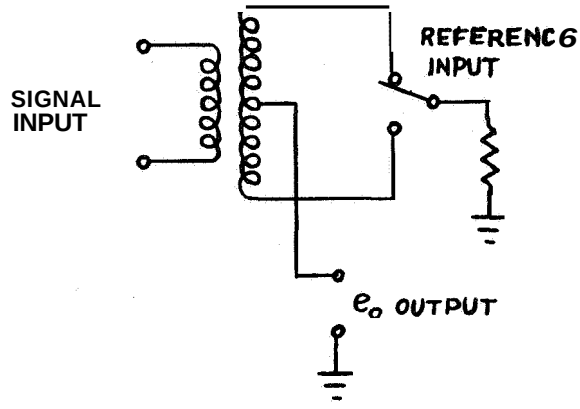


Figure 3.3.2.7. Basic R. F. Test Console Phase Detector

The simple arrangement shown chops the input signal spectrum at the reference rate. Mathematically, this arrangement provides a means of multiplying the signal spectrum by the reference. The resulting terms at the output include a voltage proportional to a constant multiplied by the differences between the signal and reference phase angles. The bipolar switch was mechanized as two diode quads driven from a reference transformer. Opposite ends of the signal transformer are alternately shorted to ground (at the reference rate) through terminating resistors. This precaution yielded a broadband unit as the signal transformer is terminated by its proper load resistance over an entire cycle of reference voltage. A simplified schematic diagram of the phase detector is shown in figure 3.3.2.8. The basic phase detector was used in the P. M. Receiver at 10 Mc and in the F. M. Receiver at 50 Mc.

3.3.2.3.4 Discriminator (Codes 403 and 403A)

The F. M. Receiver includes two types of discriminator. A conventional unit was used in the phase lock discriminator AFC loop and a delay line discriminator was utilized as the open loop demodulator. The delay line discriminator is more linear (at a sacrifice of slope sensitivity); however, the time delay contributed by the coaxial transmission lines resulted in excessive transport lag. As a result the unit was not suitable for the AFC loop.

A simplified schematic diagram of the conventional discriminator is shown in figure 3.3.2.9.

The unit exhibited a slope sensitivity of 1.7 Mc/volt and a 9 Mc bandwidth.

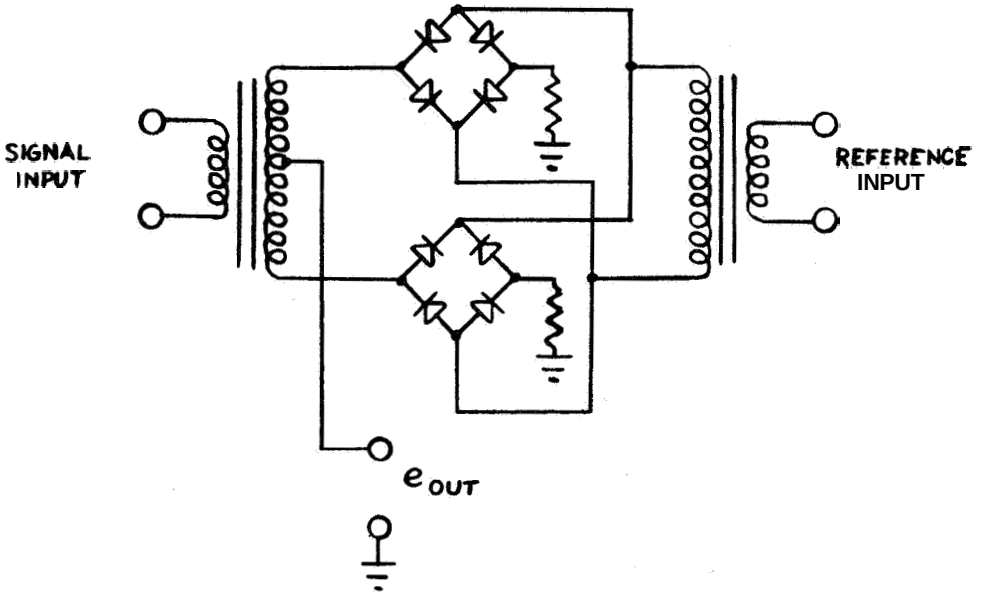


Figure 3.3.2.8. Simplified Schematic Diagram
R. F. Test Console Phase Detector

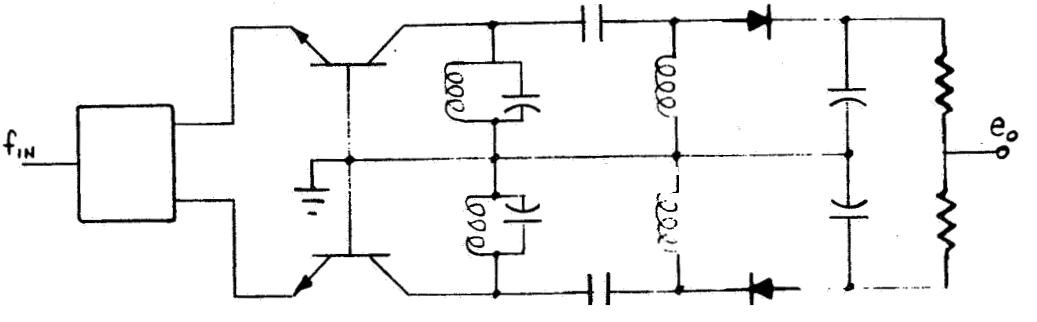


Figure 3.3.2.9. Conventional Discriminator

14

The delay line discriminator is shown in figures **3.3.2.10** and **3.3.2.11.** Both the phase splitting and the development of quadrature voltage is accomplished with a delay line. The $\lambda/2$ section *of* line provides out *of* phase **"sampling"** voltages while the $\lambda/4$ section provides the quadrature voltage to **be** sampled. The ***peak*** detecting or sampling diodes are connected as in a conventional phase detector.

The discriminator characteristic is computed for sine wave inputs using the labels **of** figure **3.3.2.3.8.** The phase shift at points B and C are

$$\phi_B = \pi f/f_o \quad J \qquad \phi_C = \frac{(n+1)\,nf}{2f_o} \tag{130}$$

moreover, the voltages at A, B, and C may be written as:

$$V_A = \cos wt \tag{131}$$

$$V_B = \cos(wt - \phi_B) \tag{132}$$

$$V_C = \cos(wt - \phi_C) \tag{133}$$

The first peak detector **has an** output proportional to the difference between V_A and V_C.

$$V_{A-C} = \cos wt - \cos(wt - \phi_C) \tag{134}$$

The second ***peak*** detector has an output proportional to the difference between V_B and V_C.

$$V_{B-C} = \cos(wt - \phi_B) - \cos(wt - \phi_c) \tag{135}$$

Equations **(134)** and **(135)** can be reduced to the forms

$$V_{A-C} = -2\sin\left(wt - \frac{\phi_C}{2}\right)\sin\phi_{C/2} \tag{136}$$

$$V_{B-C} = -2\sin\left(wt - \frac{\phi_B}{2} - \frac{\phi_C}{2}\right)\sin\left(\frac{\phi_C}{2} - \frac{\phi_B}{2}\right) \tag{137}$$

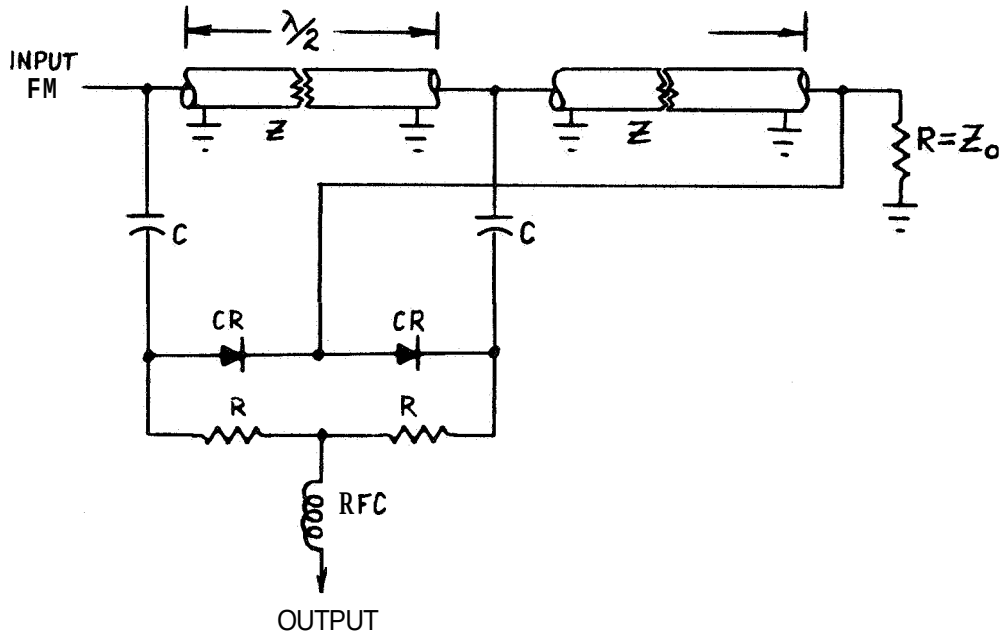


Figure 3.3.2.10 Delay Line Frequency Discriminator

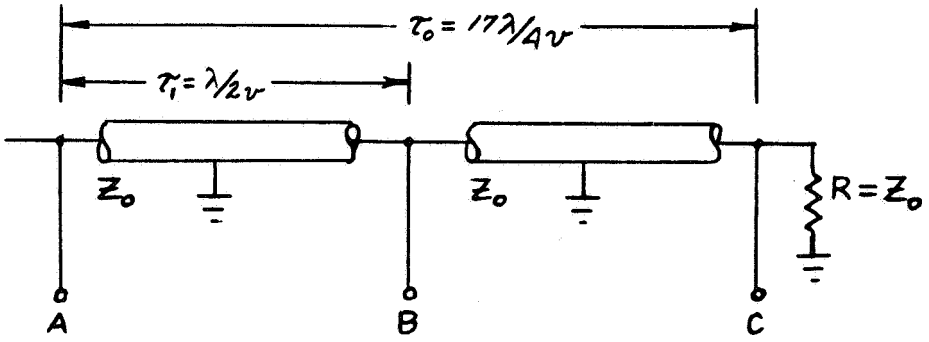


Figure 3.3.2.11 Delay Line Phase Characteristics

Thus one detector will have an output nearly equal to the peak value of V_{A-} (V_1) and the other a value near the peak value of V_{B-C} (V_2).

$$V_1 = \sin \phi_{C/2} \tag{138}$$

$$V_2 = \sin (\phi_{\frac{C}{2}} - \phi_{\frac{B}{2}}) \tag{139}$$

The detector outputs are of opposite polarity being summed with equal weight giving an output proportional to $V_1 - V_2$.

$$V_1 - V_2 = K \left[\sin \phi_{\frac{C}{2}} - \sin (\phi_{\frac{C}{2}} - \phi_{\frac{B}{2}}) \right] \tag{140}$$

Substituting $\phi_C = (n+1)\ \phi_{\frac{B}{2}}$, $V_1 - V_2$ becomes

$$V_1 - V_2 = 2\,K \sin n\phi_{\frac{B}{4}} \cos \phi_{\frac{B}{4}} \tag{141}$$

Using the relation between phase and frequency, $B = 180\, f/f_o$, equation (141) becomes:

$$V_1 - V_2 = \sin 45\, n\, f/f_o \cos 45\, f/f_o \tag{142}$$

A plot of equation (142) reveals a linear characteristic of output voltage $(V_1 - V_2)$ as a function of input frequency f. An interesting feature of the discriminator design is that the quarter wave transmission line may be made any number of quarter wavelengths enabling the designer to trade off linearity (bandwidth) and slope sensitivity. The discriminator designed in the RF Test Console includes a half wave and $^{15}/_{4}$ wavelengths transmission line yielding a slope sensitivity of $0.4 \frac{\text{volt}}{\text{Mc}}$ and a 3 Mc bandwidth.

3.3.2.3.5 Phase Lock Discriminator VCO

The phase lock discriminator VCO was designed in a Clapp configuration. The Clapp design was outlined earlier in the report in Section 3.1 and is not repeated here.

3.3.2.3.6 F. M. Receiver Operational Amplifiers

Several operational amplifiers are included in the F. M. Receiver output baseband circuitry. Specific operational amplifier applications include the AFC loop amplifier, APC Loop amplifier and various output amplifiers. The Burr Brown Model 1510 and 1560 amplifiers were chosen on the basis of gain bandwidth product, low noise and drift characteristic.

3.3.2.4 Test Results

The F. M. Receiver test results (aside from the FM Subsystem test results listed previously) are included in this section. Figure 3.3.2.12 indicates the receiver input amplifier phase and amplitude response combined with the 10 Kc 'plug in" filter, figure 3.3.2.13 indicates the response with the 200 Kc filter and figure 3.3.2.14 with the 1 Mc filter.

Figures 3.3.2.15 and 3.3.2.16 show the limiter characteristics of the two F. M. Receiver limiters. Figure 3.3.2.16 indicates the phase lock discriminator phase detector characteristic. Figure 3.3.2.17 shows the phase lock discriminator VCO characteristic (closed loop). Figure 3.3.2.18 indicates the test set used to measure the phase lock discriminator open loop gain. Figure 3.3.2.19 shows the test set used to measure the phase lock discriminator loop bandwidths. Figures 3.3.2.20 thru 3.3.2.22 indicate the phase lock discriminator loop amplitude responses. Figures 3.3.2.23 thru 3.3.2.34 show the phase and amplitude responses of the six F. M. Receiver output baseband filters.

3.4 LINEAR S/N SUMMER

The Linear S/N Summer was designed and tested during Phase I of this project. The results of that effort were reported in the Phase I Final Report, Appendixes B and C entitled "Linear Signal/Noise Summer" and "Linear Signal/Noise Summer Spectral Density Test". The principal test results reported in Phase I are summarized in Table 3.4.1.

In the course of the Phase II effort, the S/N Summer was repackaged in a Holloway cabinet. The noise amplifier and noise filter were repackaged in an oven (to diminish response variations as a function of temperature) and retuned at 40°C.

The noise amplifier is gain controlled whereby the angle modulated carrier serves as the AGC loop reference. Variations in either carrier power or noise power results in a change of absolute signal and noise power from the Summer; however, the S/N ratio is maintained constant within the constraints of the control loop. The loop operating point is established by the "Bias Adjust" control which regulates a DC potential which is combined with the loop error voltage. Figure 3.4.1 indicates the noise amplifier characteristic of relative attenuation as a function of the bias voltage at different noise amplifier input power levels.

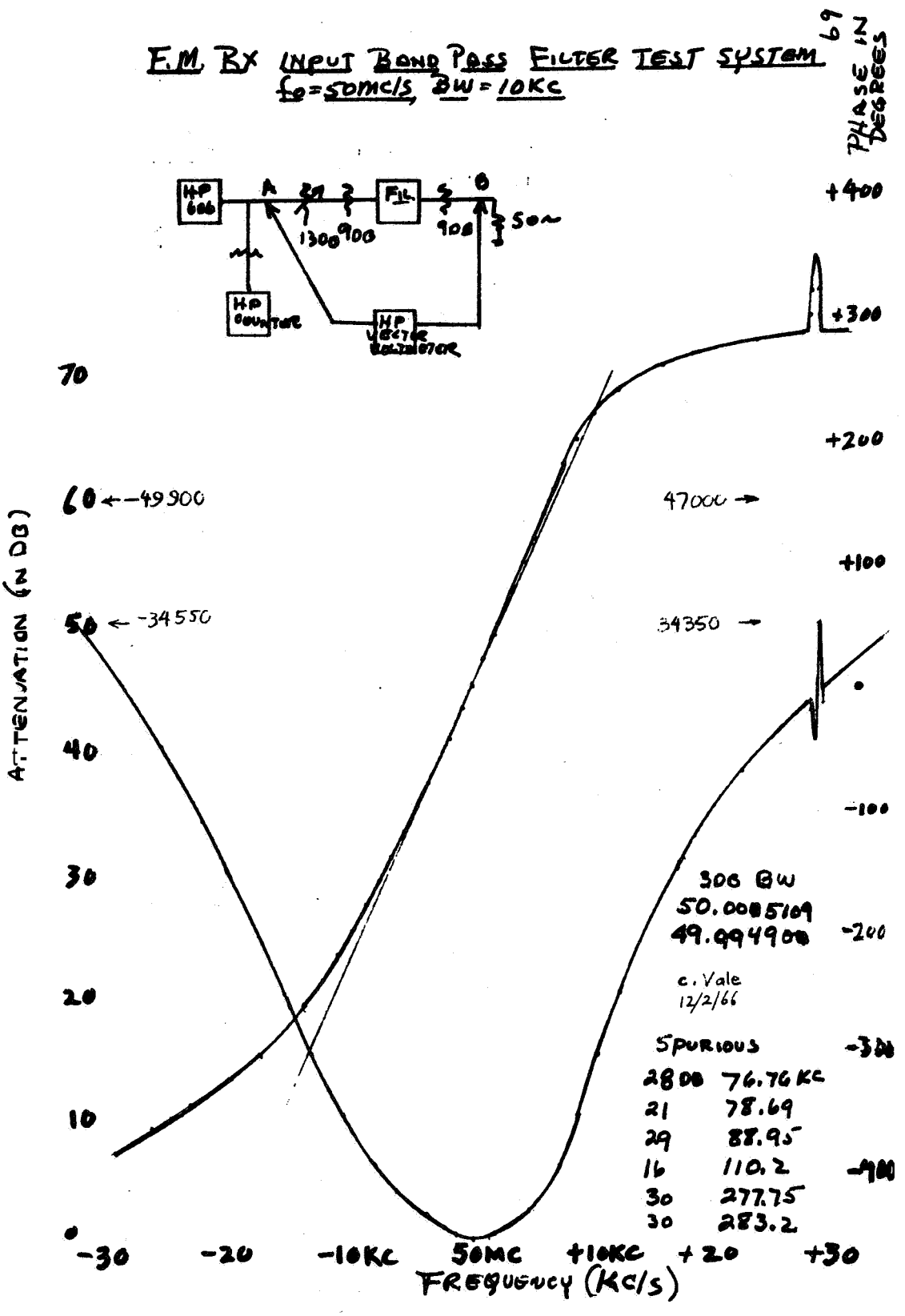


Figure 3.3.2.12. F. M. Rx Input Band Pass Filter Test System
fo = 50 Mc/s, BW = 10 Kc.

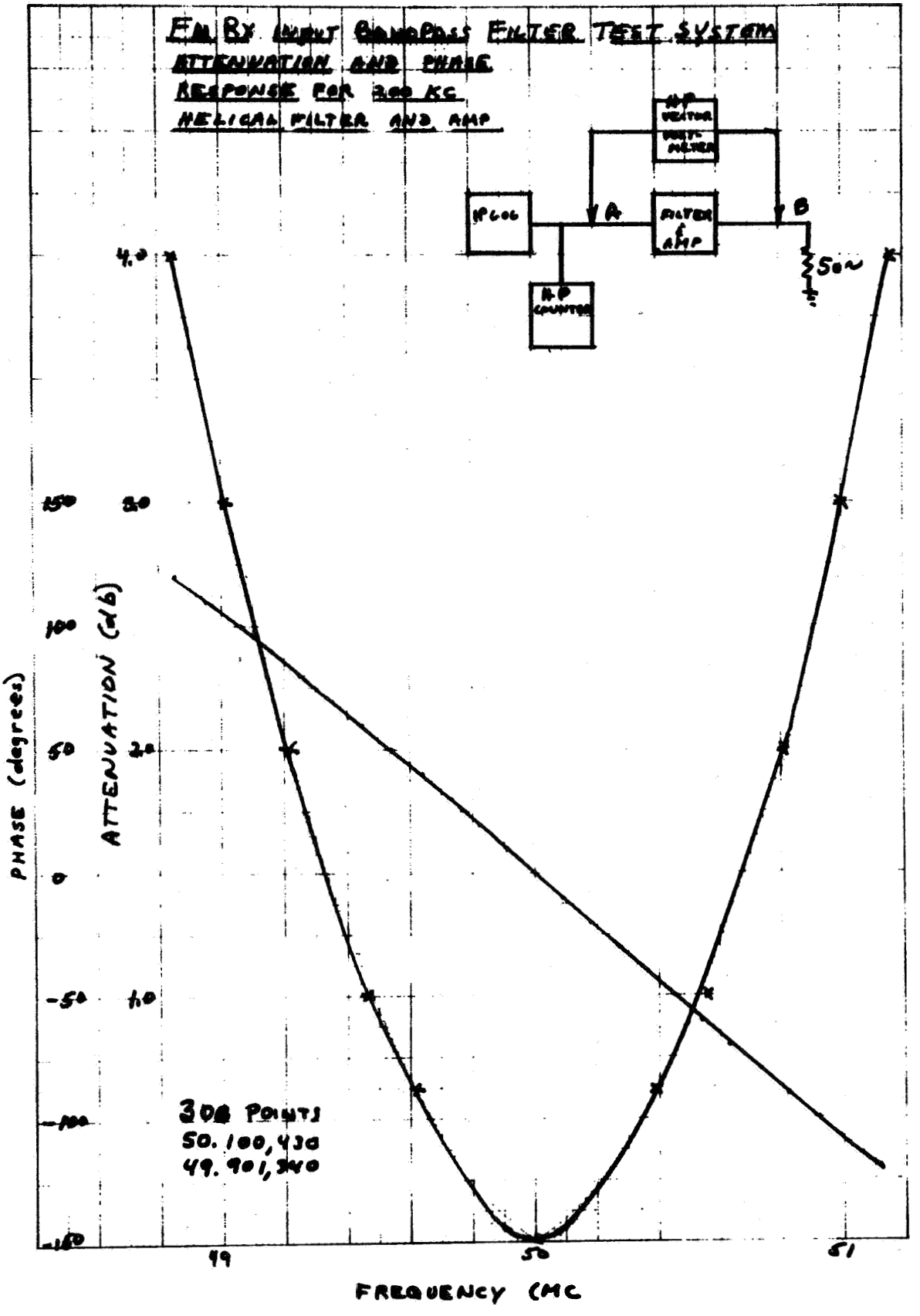


Figure 3.3.2.13. F. M. Rx Input Band Pass Filter Test System Attenuation And Phase Response For 200 Kc Helical Filter And Amp.

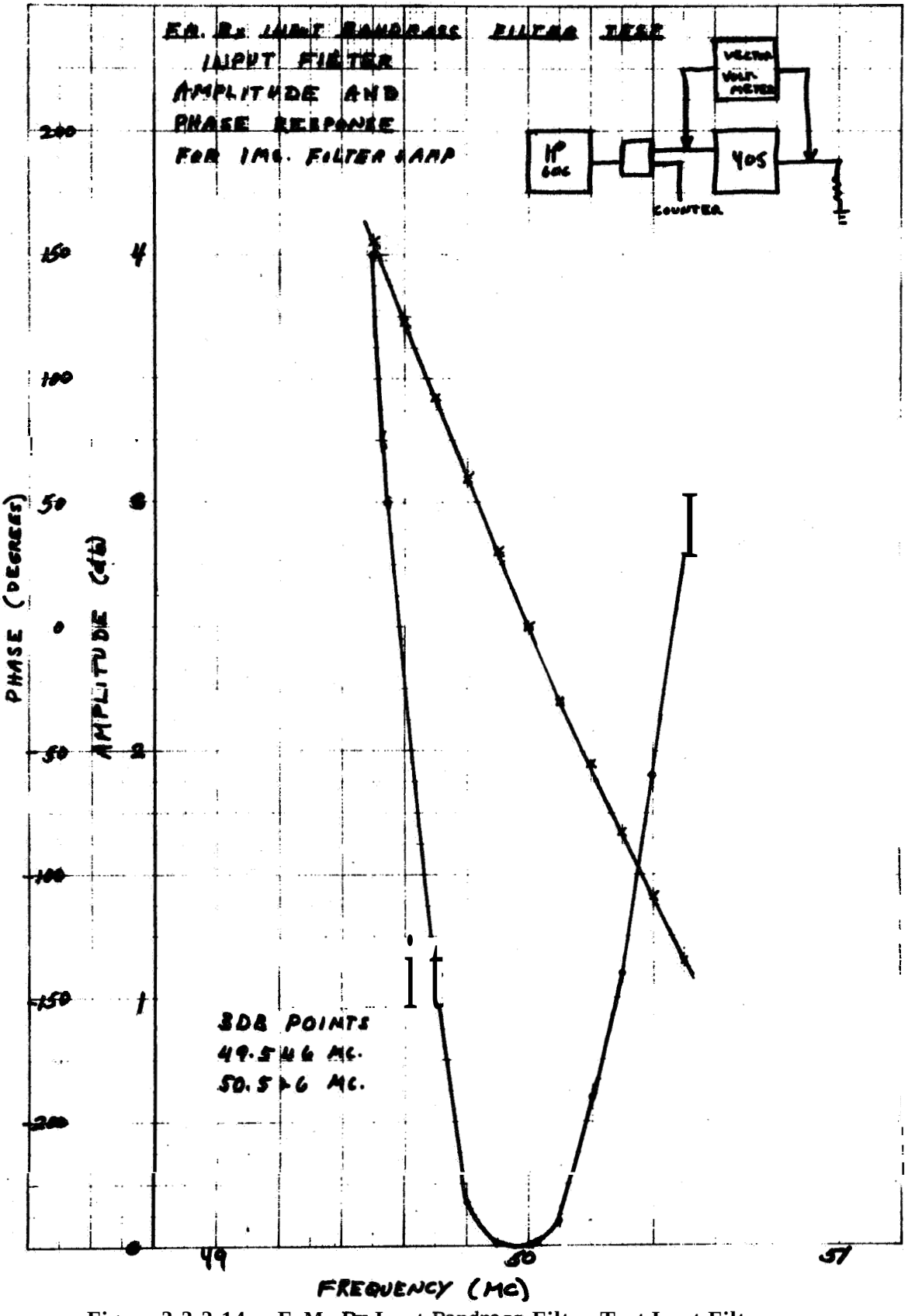


Figure 3.3.2.14. F. M. Rx Input Bandpass Filter Test Input Filter Amplitude and Phase Response for 1Mc. Filter and Amp.

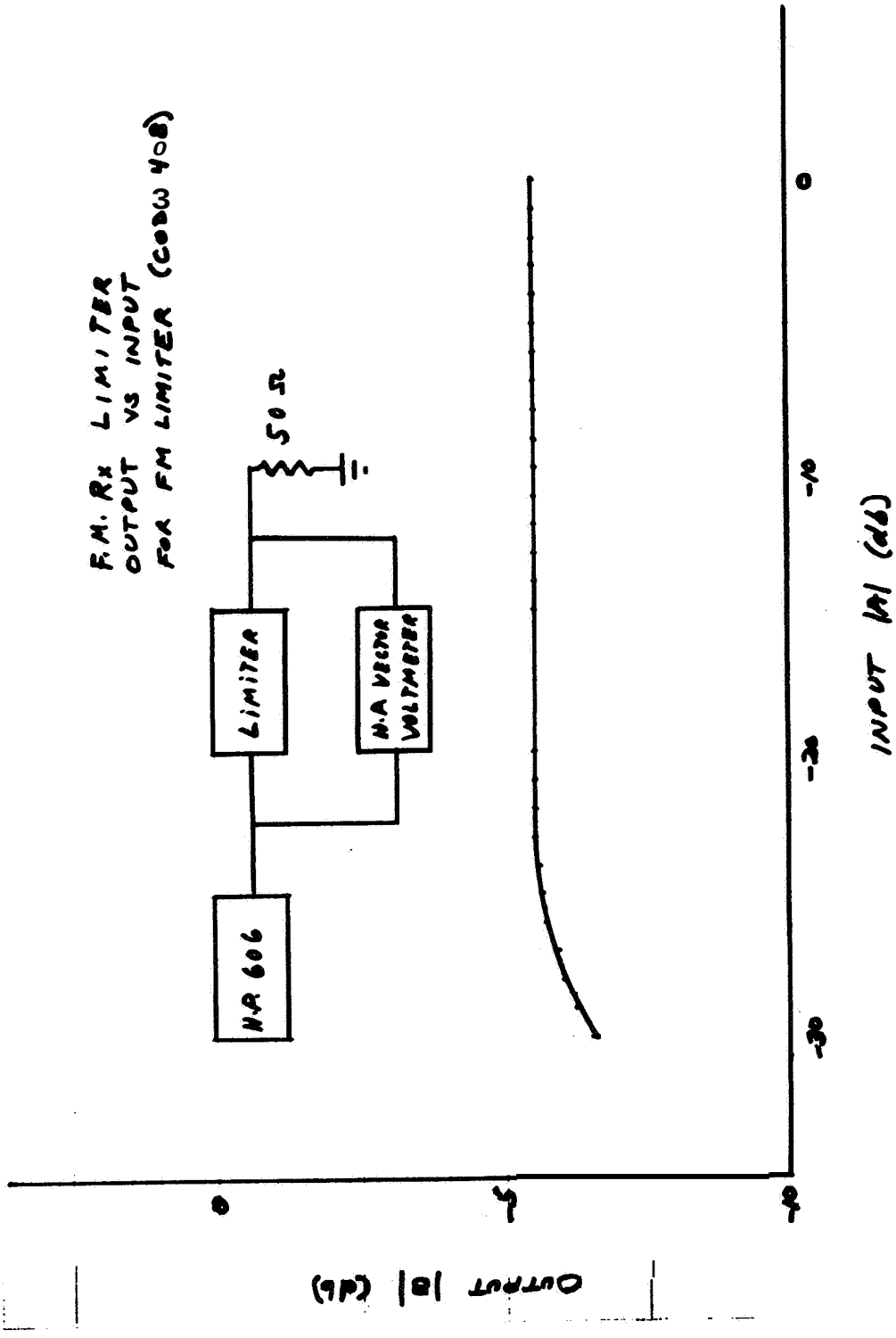


Figure 3.3.2.15. F. M. Rx Limiter Output vs. Input for F. M. Limiter (Code 408)

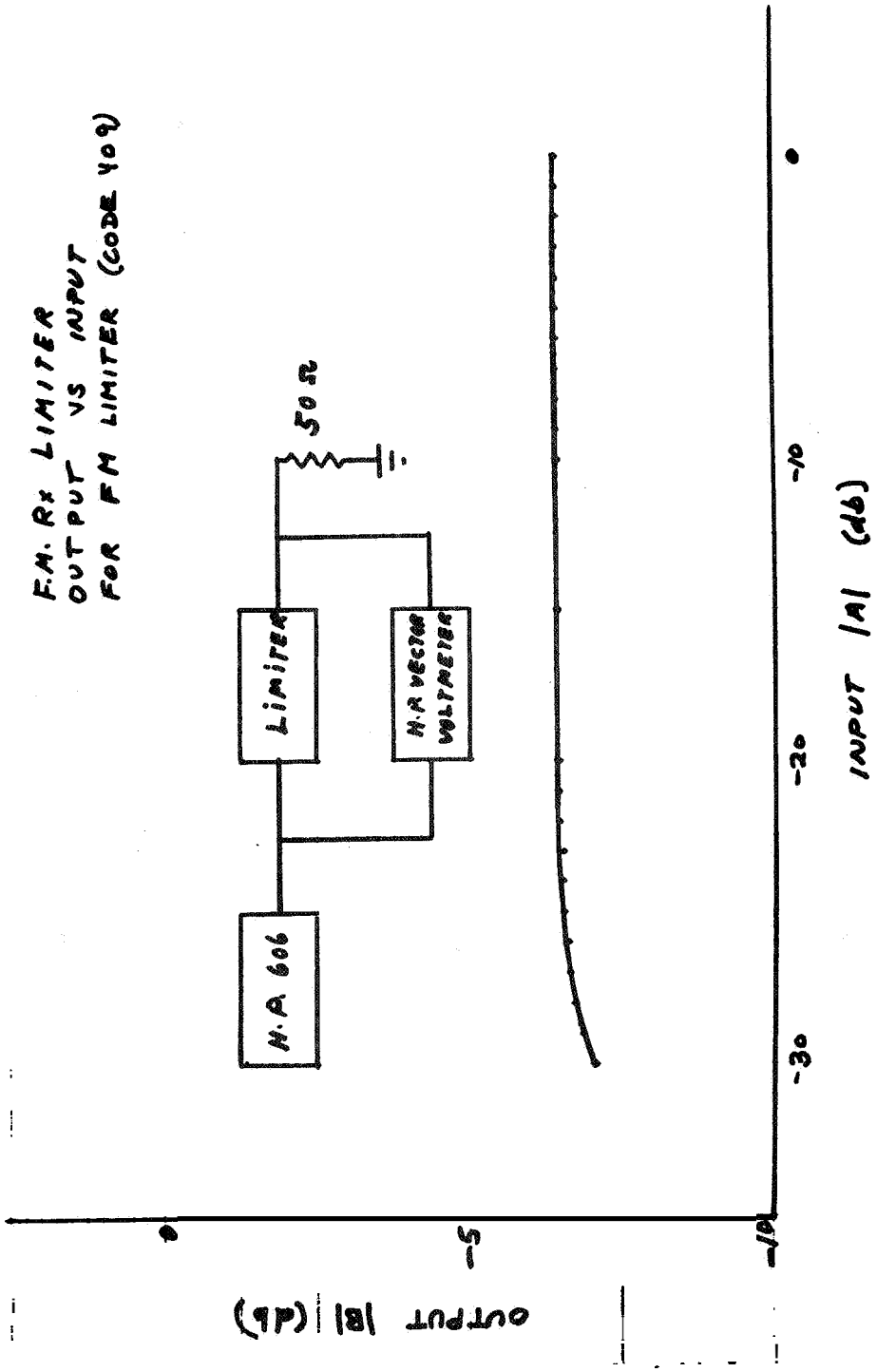


Figure 3.3.2.16. F.M. Rx Limiter Output Vs. Input for F.M. Limiter (Code 409)

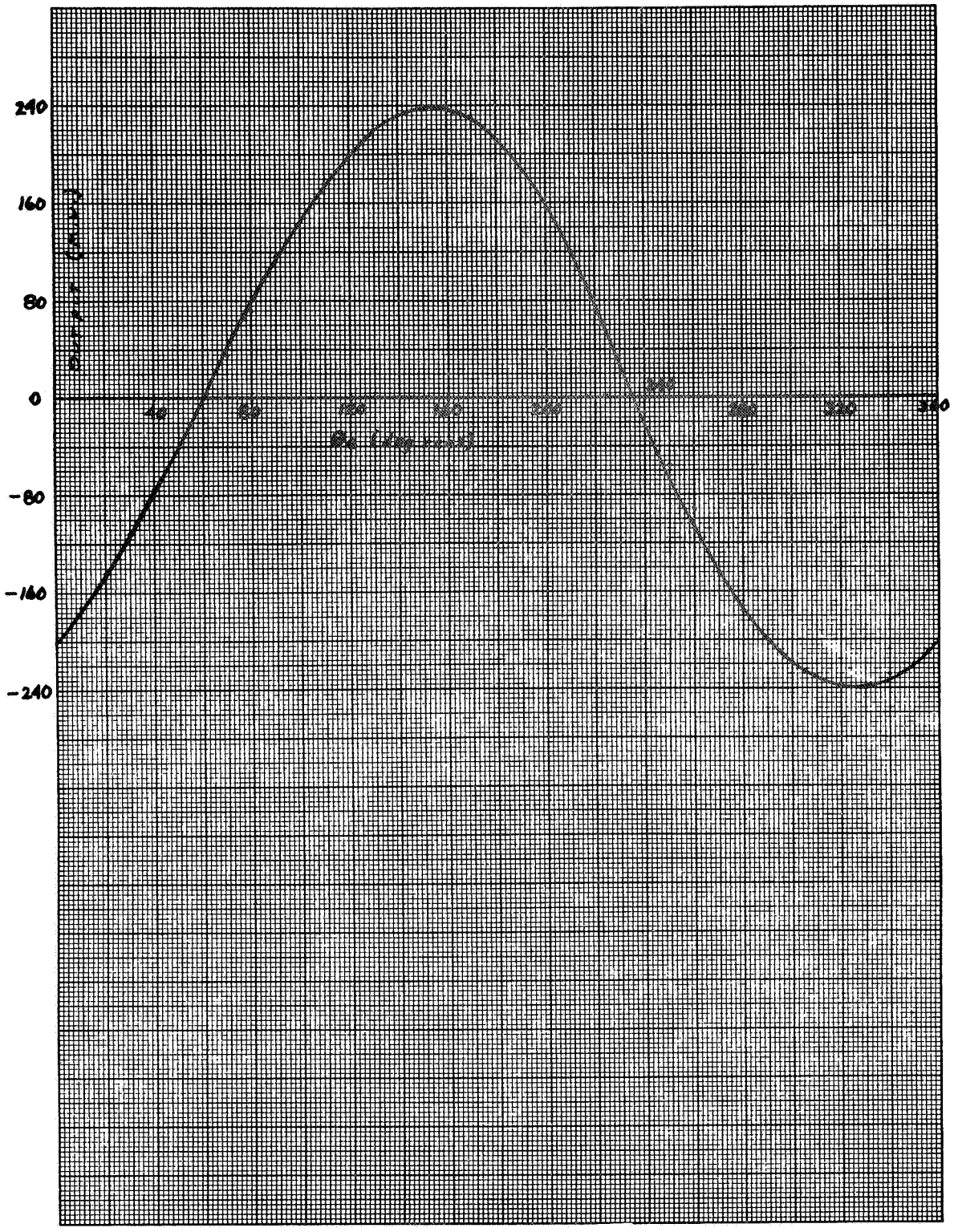


Figure 3.3.2.17. Phase Lock Discriminator
Phase Detector Characteristic

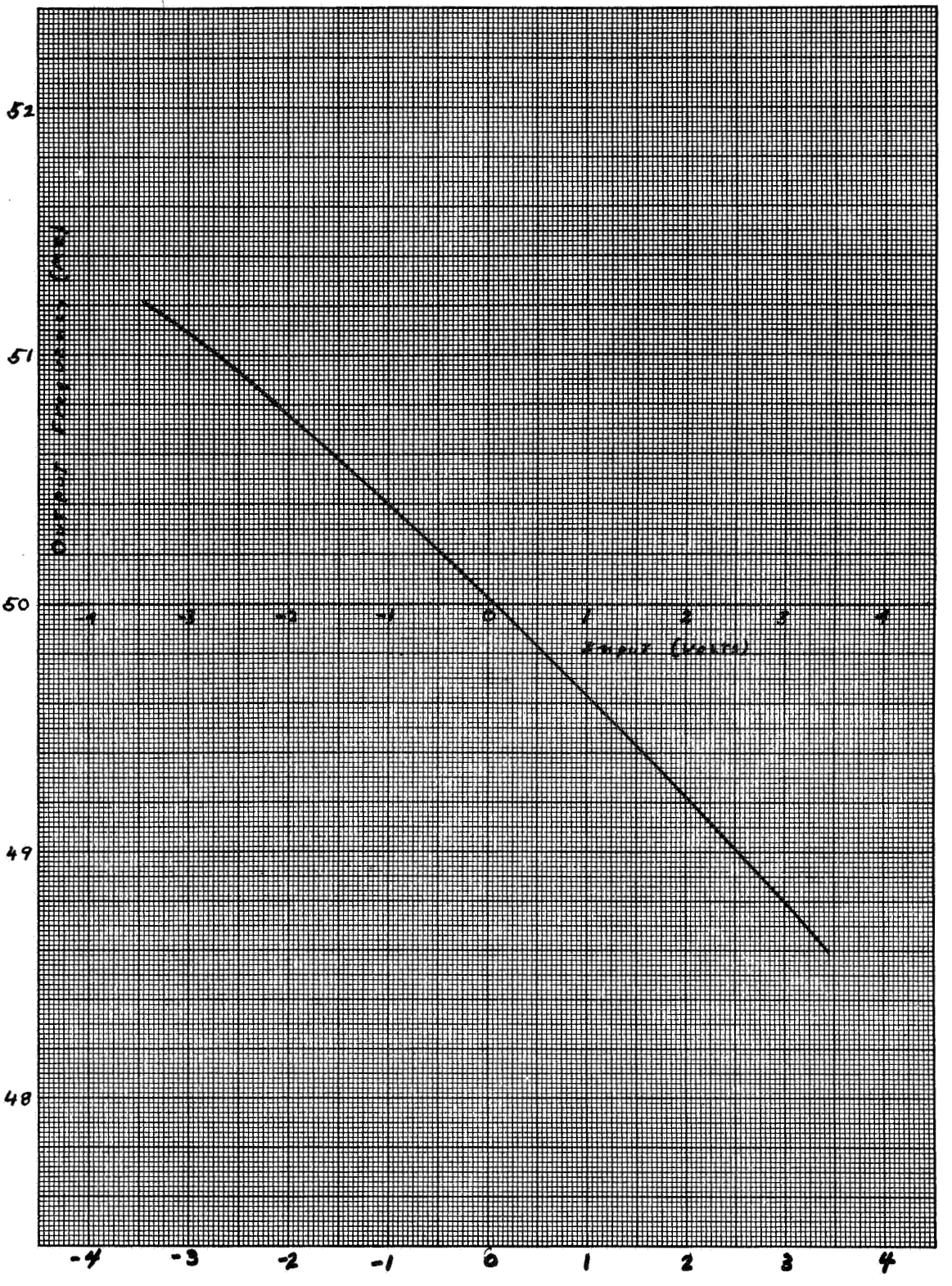


Figure 3.3.2.18. Phase Lock Discriminator VCO Characteristic (Closed Loop)

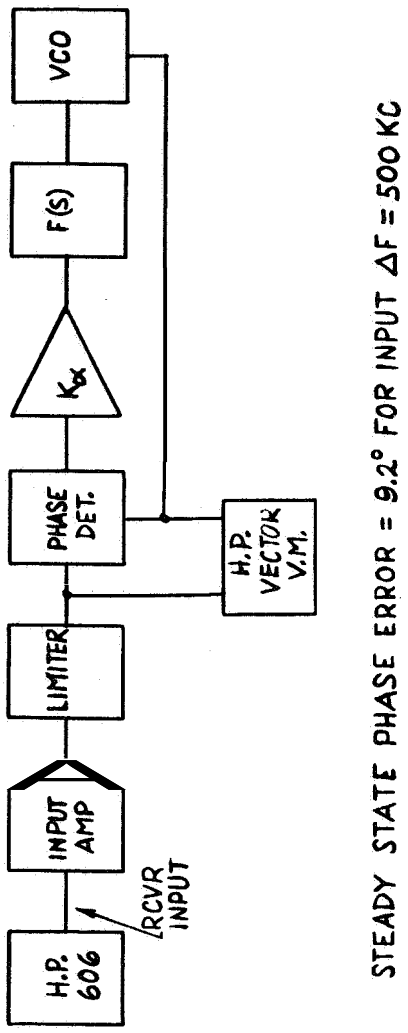


Figure 3.3.2.19. F.M. Receiver APC Loop Gain Test Set

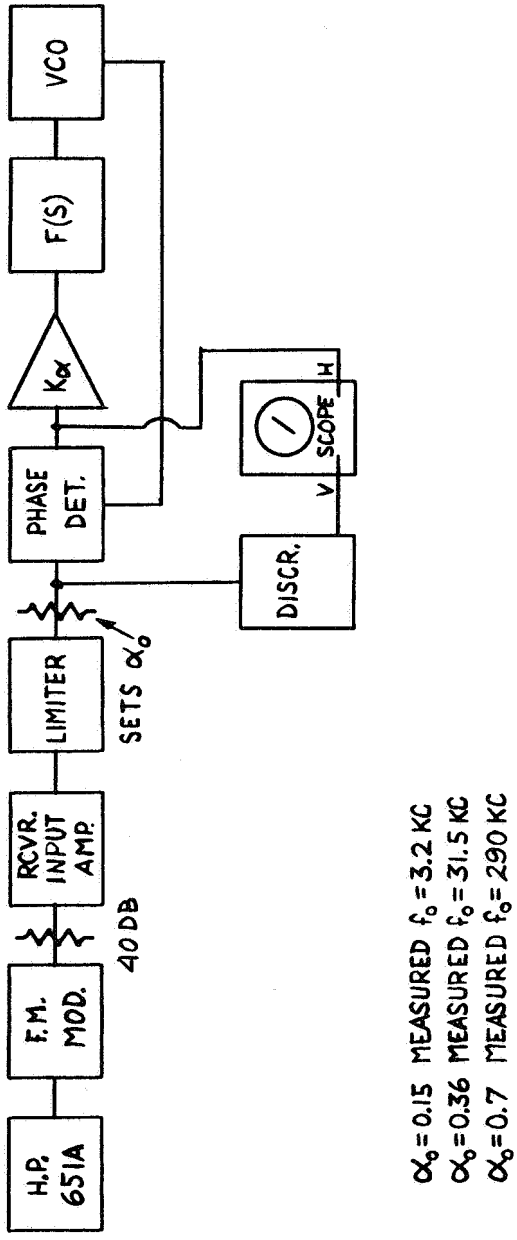


Figure 3.3.2.20. F. M. Receiver APC Loop Bandwidth Test Set

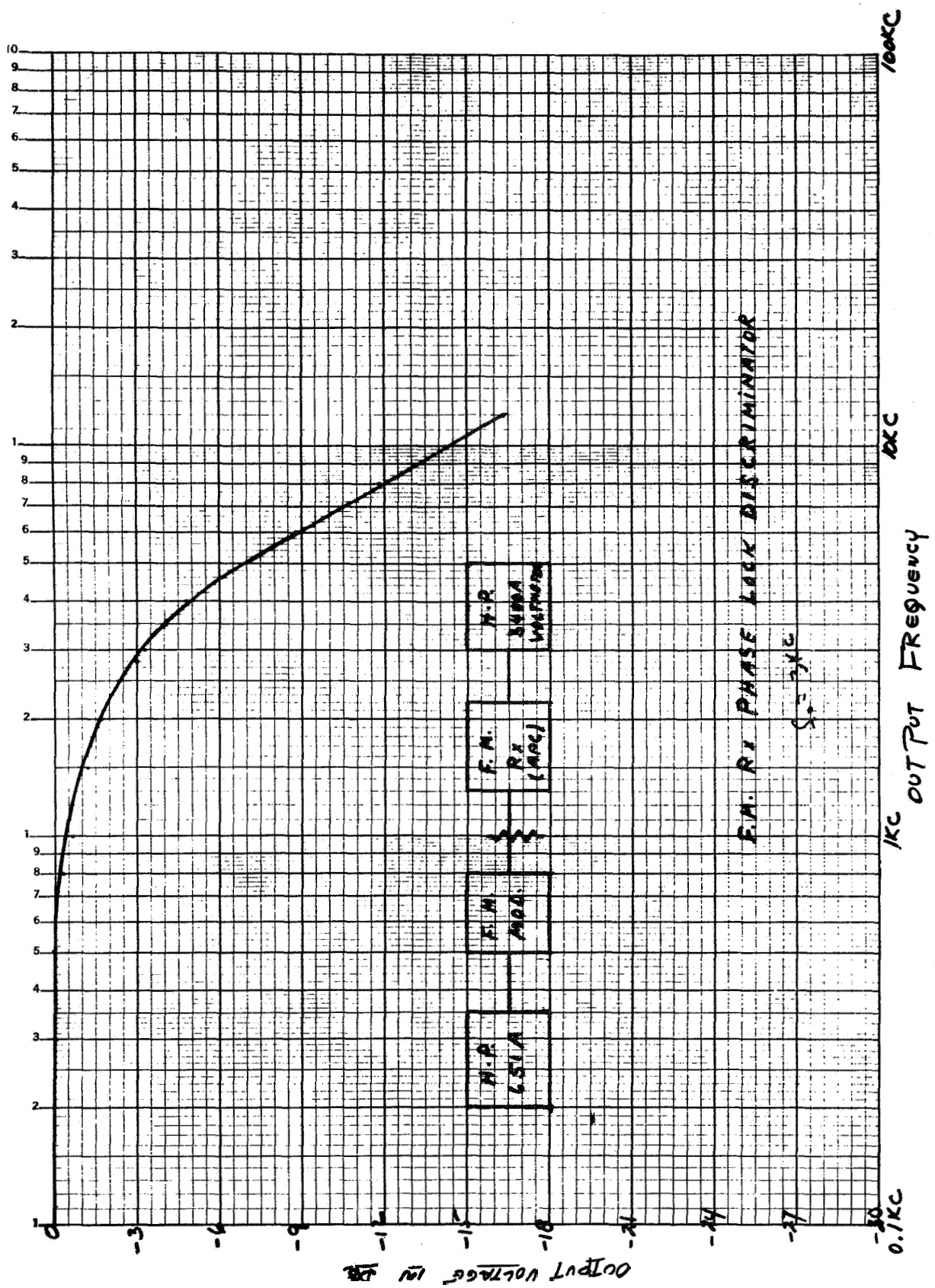


Figure 3.3.2.21. F. M. Rx Phase Lock Discriminator Amplitude Response (f_o = 3Kc)

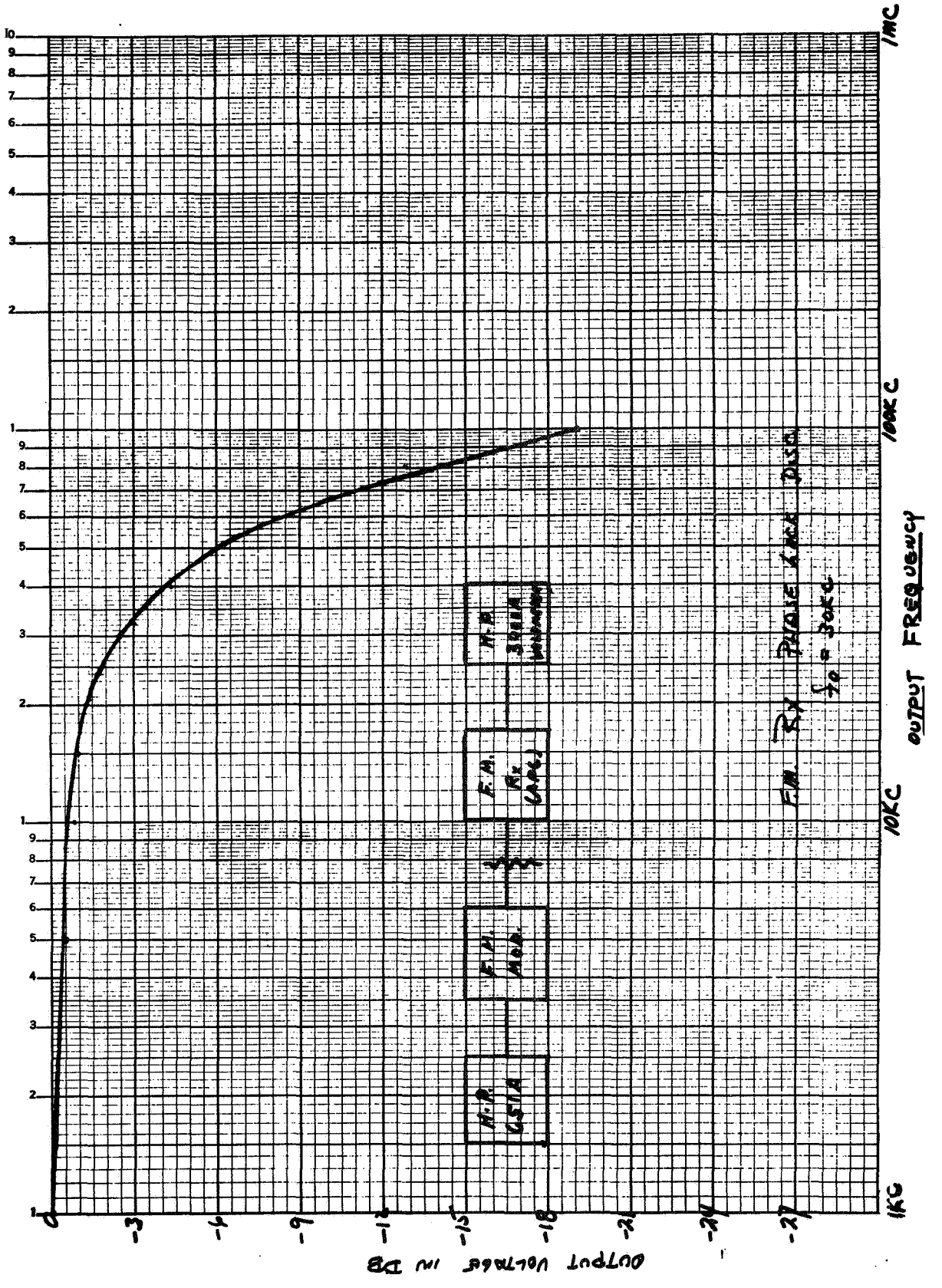


Figure 3.3.2.22. F. M. Rx Phase Lock Discriminator Amplitude Response (f_o = 30Kc)

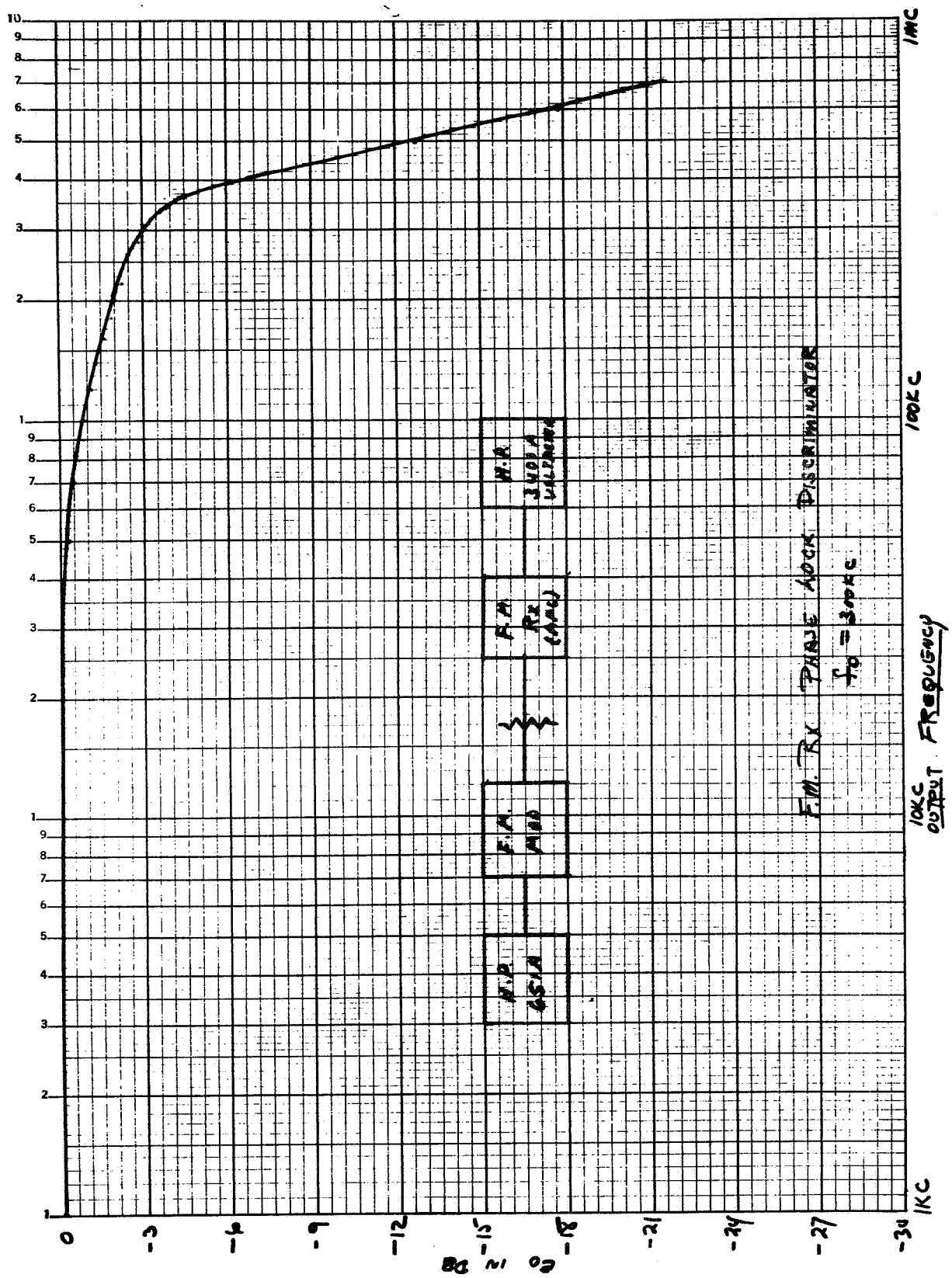


Figure 3.3.2.23. F. M. Rx Phase Lock Discriminator Amplitude Response (f_0 = 300Kc)

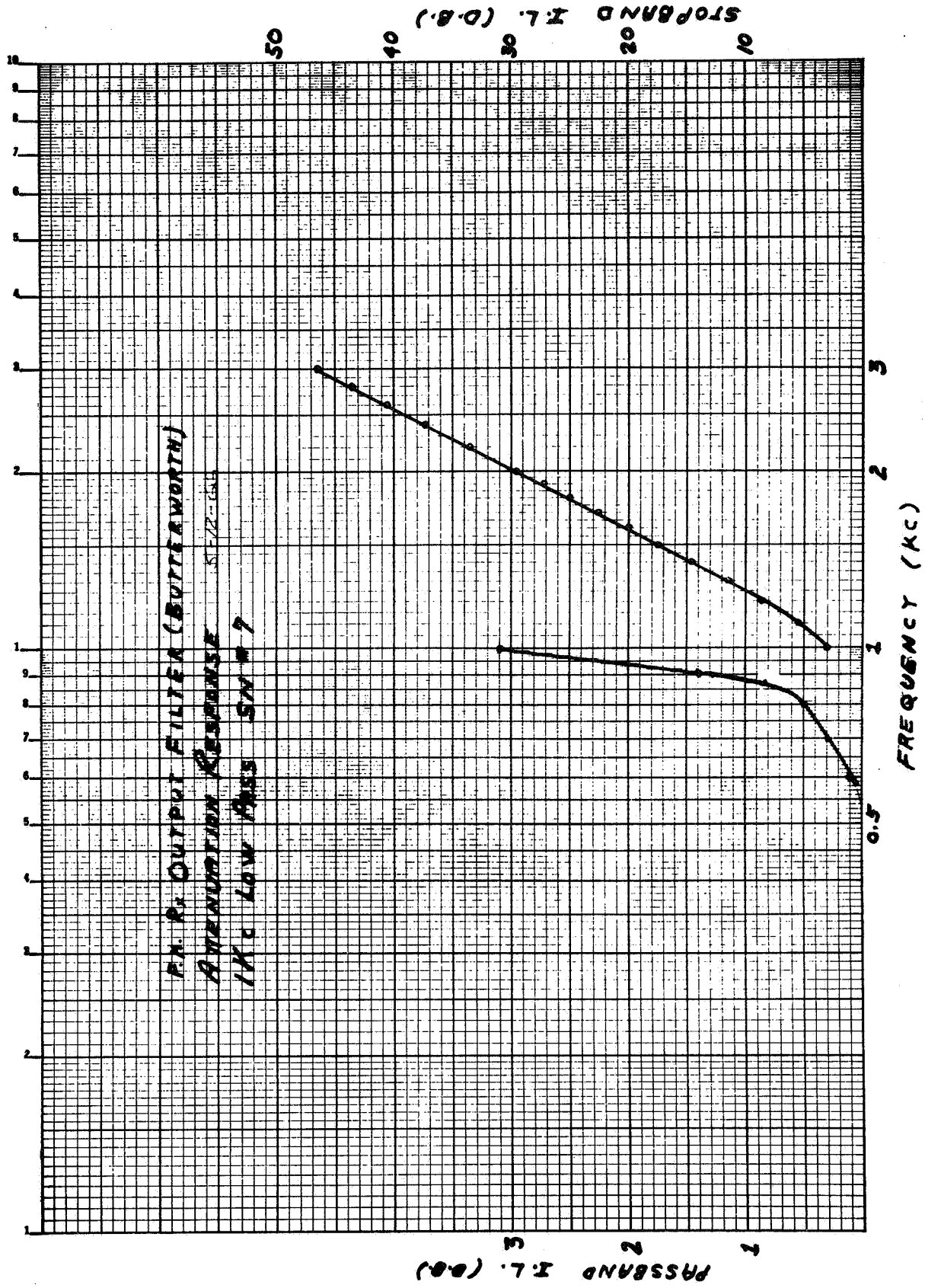


Figure 3.3.2.24. F. M. Rx Output Filter (Butterworth) Attenuation Response 1 Kc Low Pass SN #7.

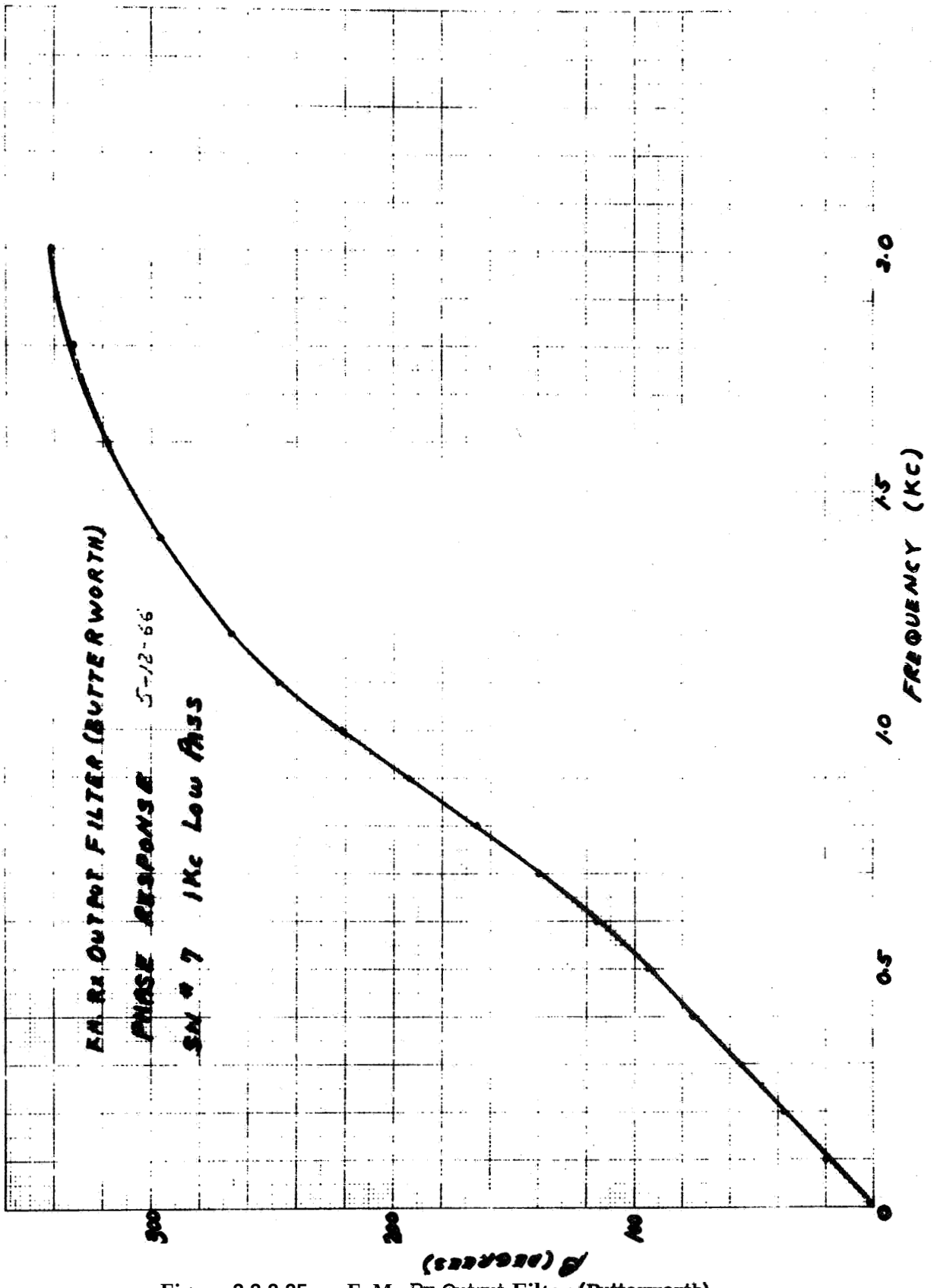


Figure 3.3.2.25. F. M. Rx Output Filter (Butterworth) Phase Response 1Kc Low Pass

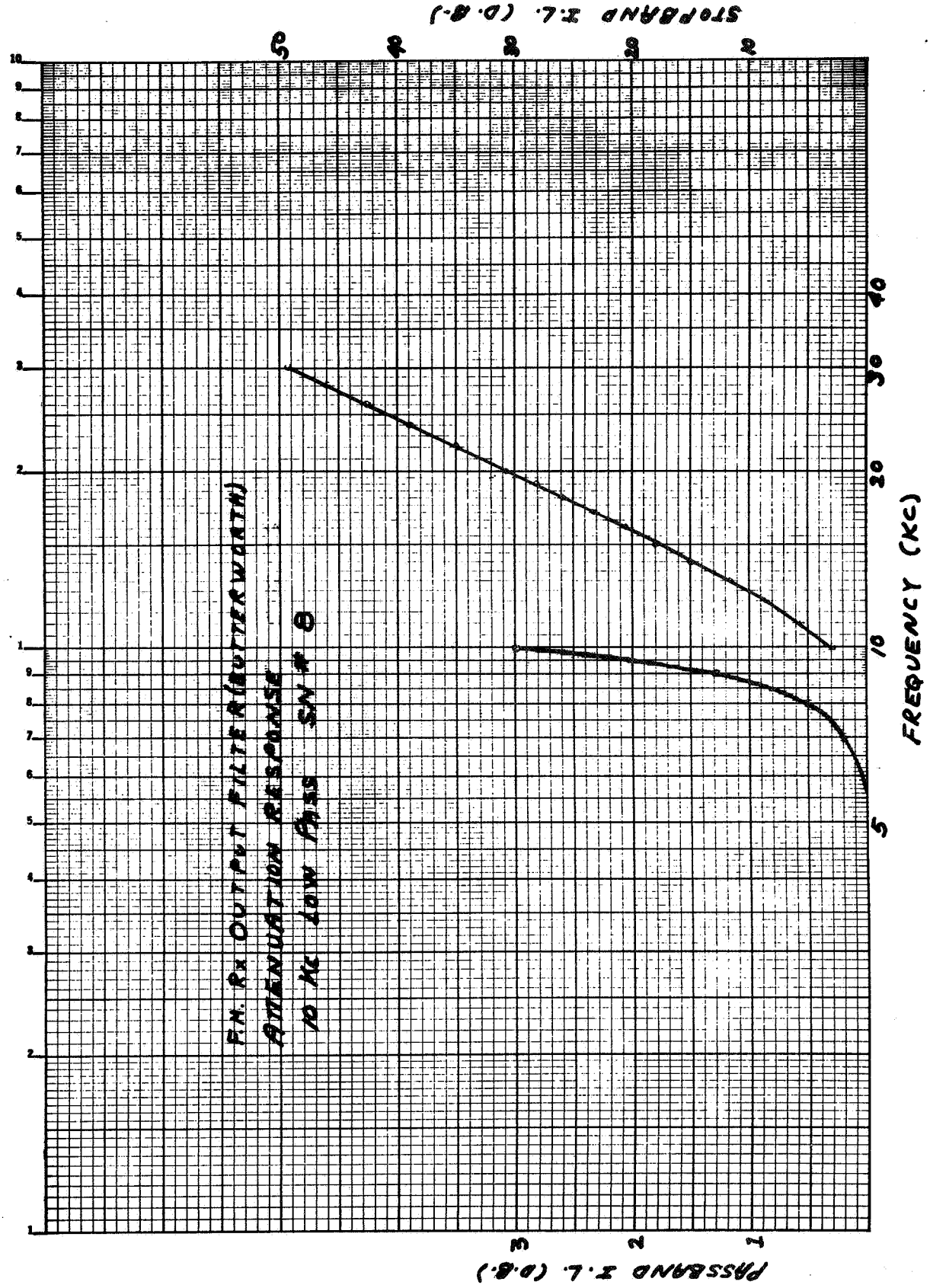


Figure 3.3.2.26. F. M. Rx Output Filter (Butterworth) Attenuation Response 10 Kc Low Pass

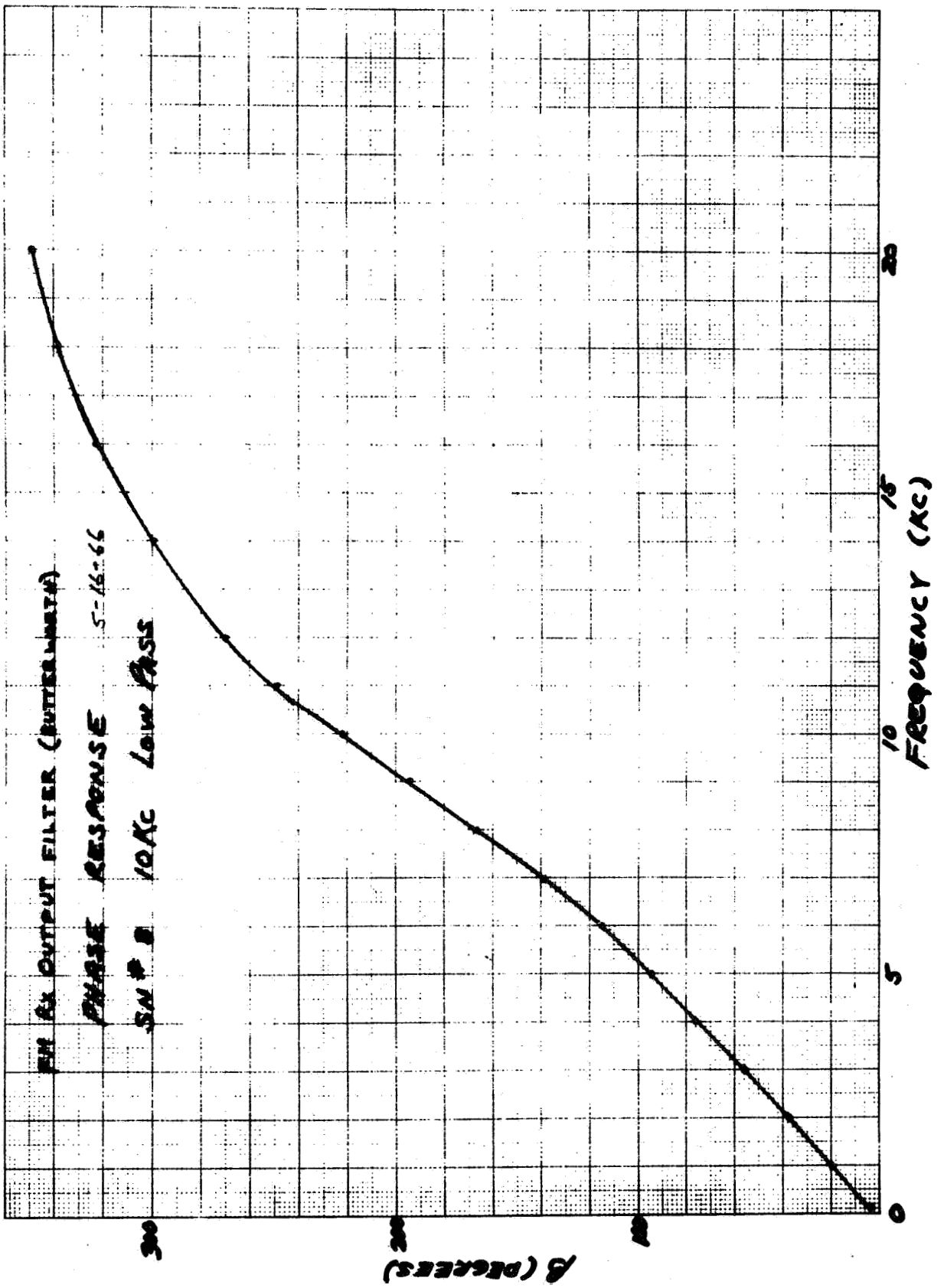


Figure 3.3.2.27. F. M. Rx output Filter (Butterworth) Phase Response 10 Kc Low Pass

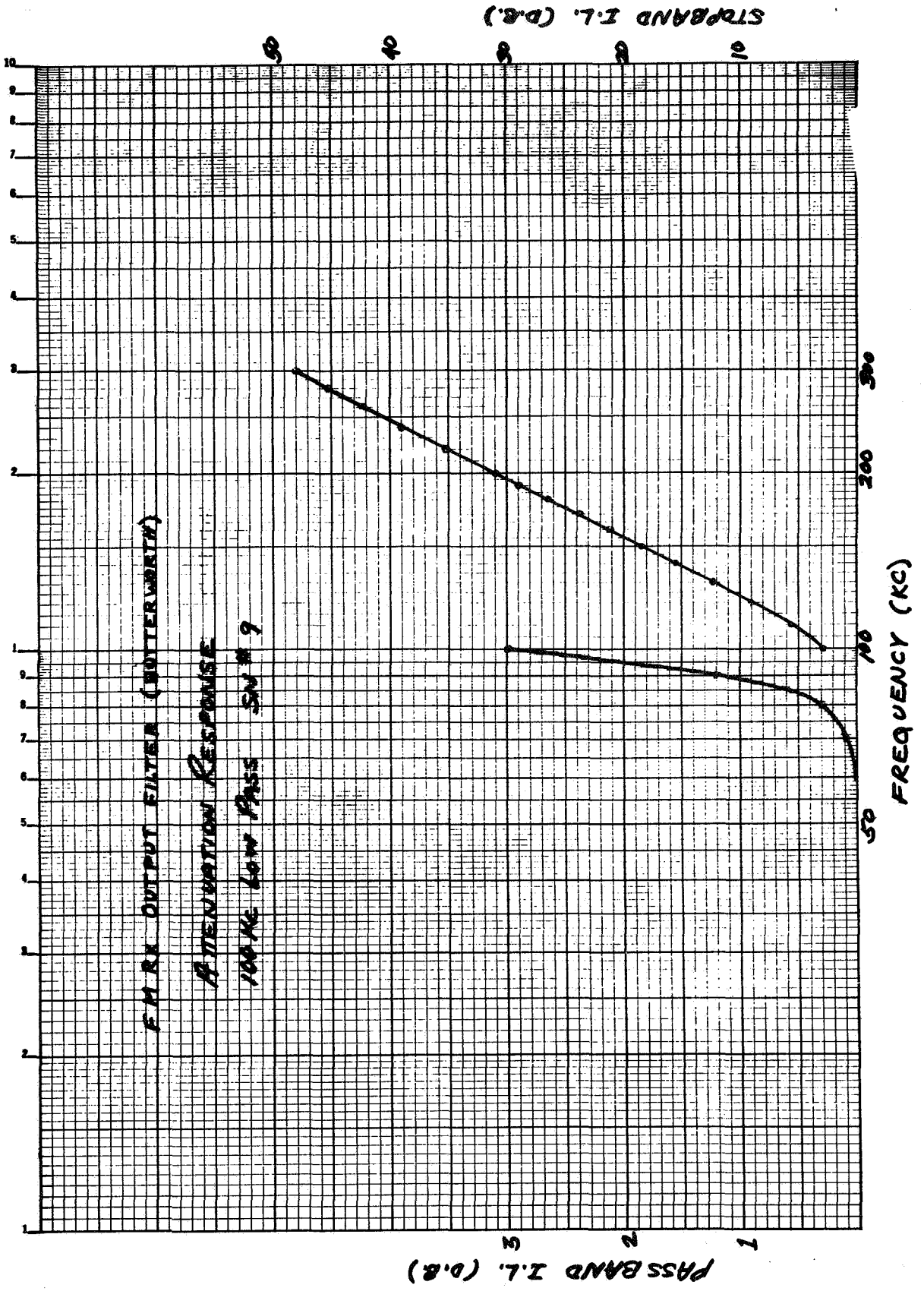


Figure 3.3.2.28. F. M. Rx Output Filter (Butterworth) Attenuation Response 100 Kc Low Pass SN #9

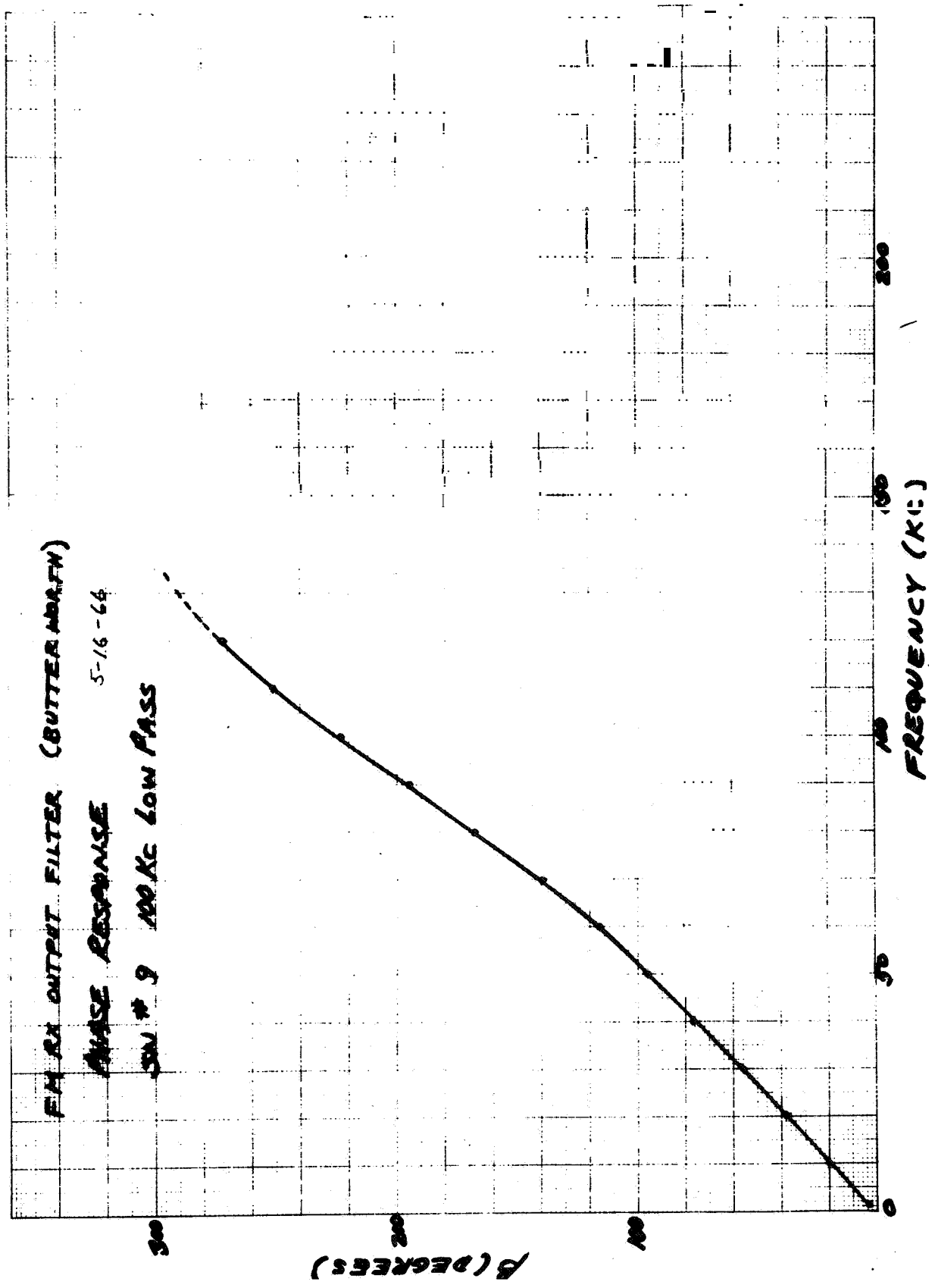


Figure 3.3.2.29. F. M. Rx Output Filter (Butterworth) Phase Response SN #9 100 Kc Low Pass

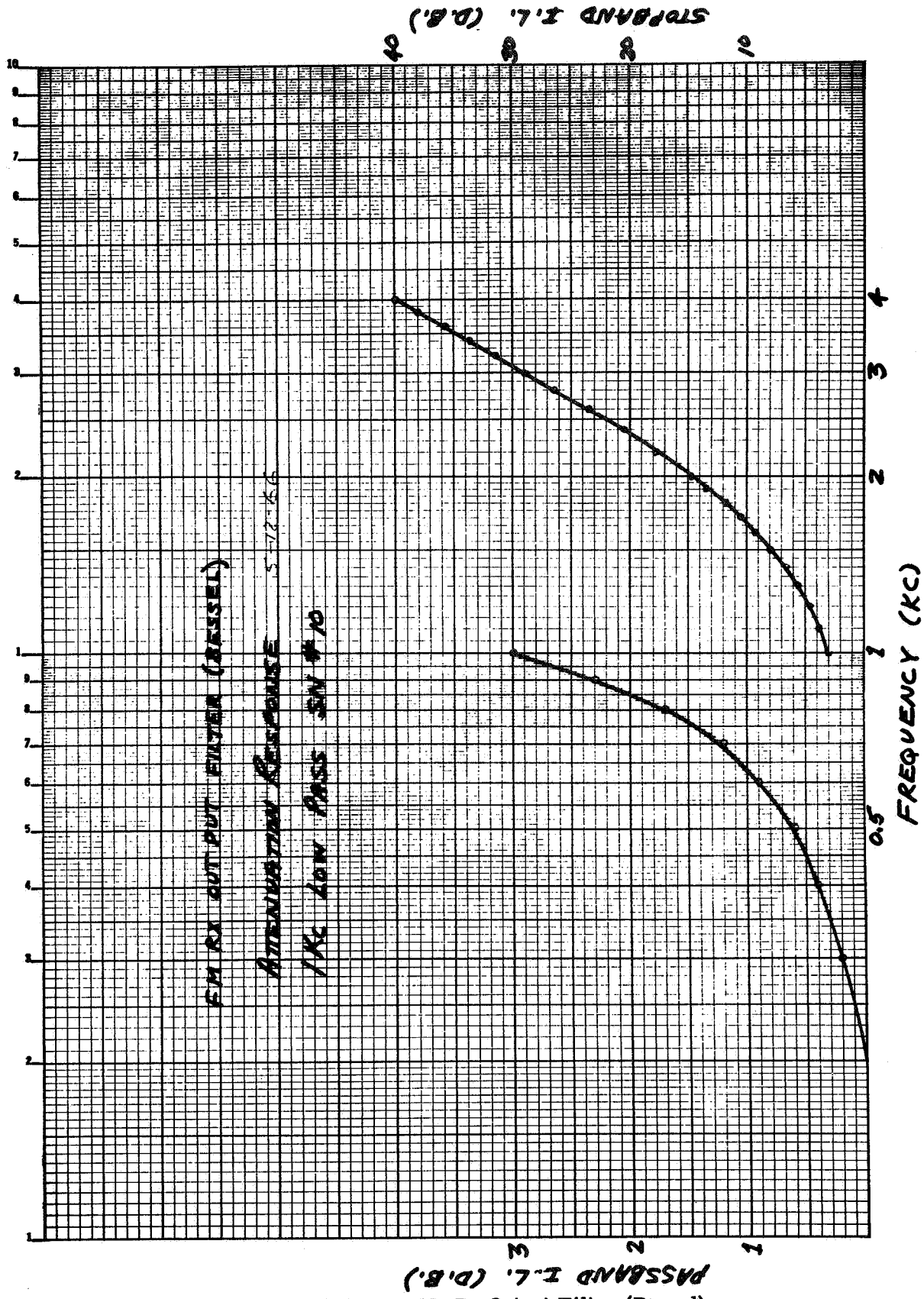


Figure 3.3.2.30. F.M. Rx Output Filter (Bessel) Attenuation Response 1Kc Low Pass SN #10

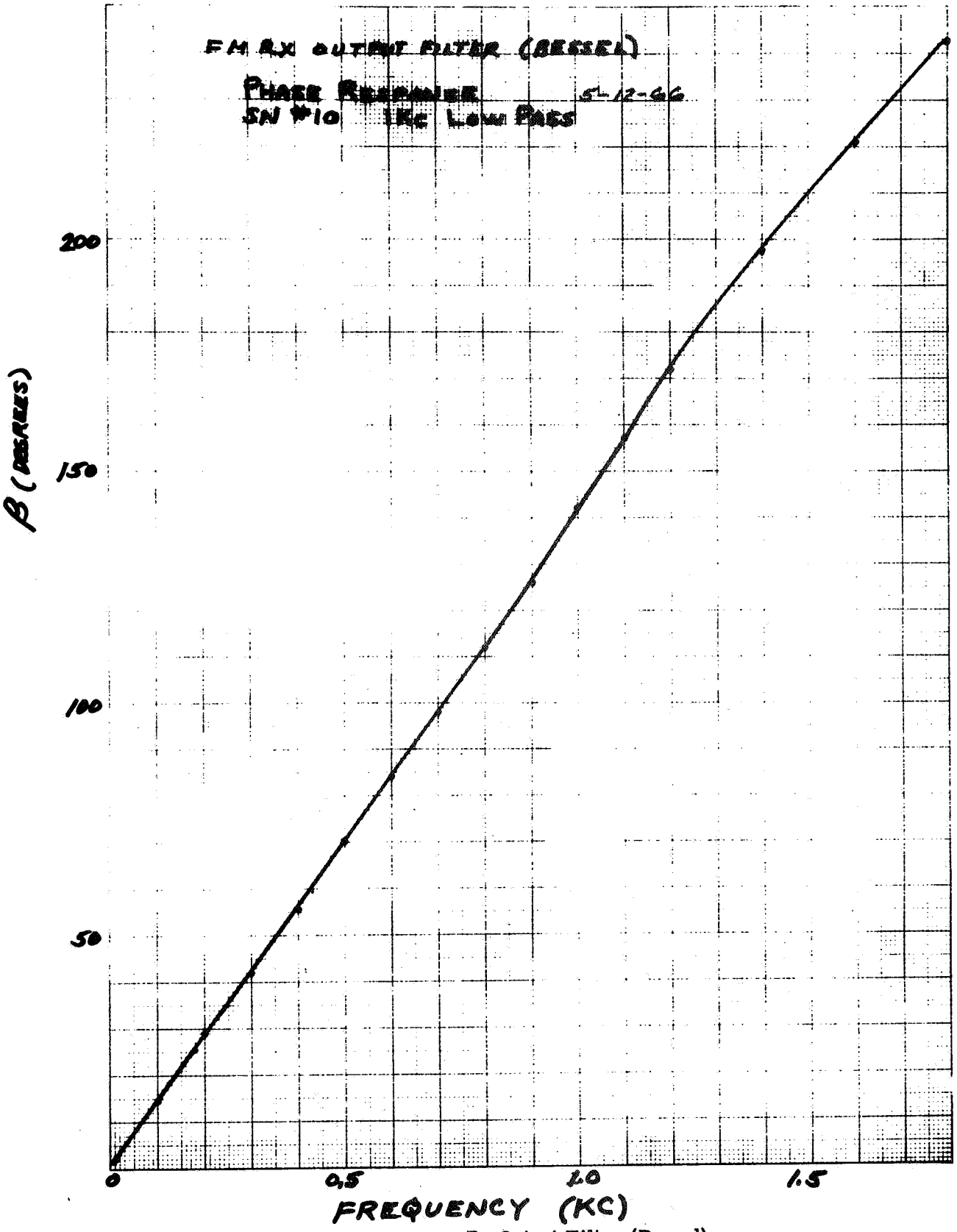


Figure 3.3.2.31. F. M. Rx Output Filter (Bessel)
Phase Response SN #10 1Kc Low Pass

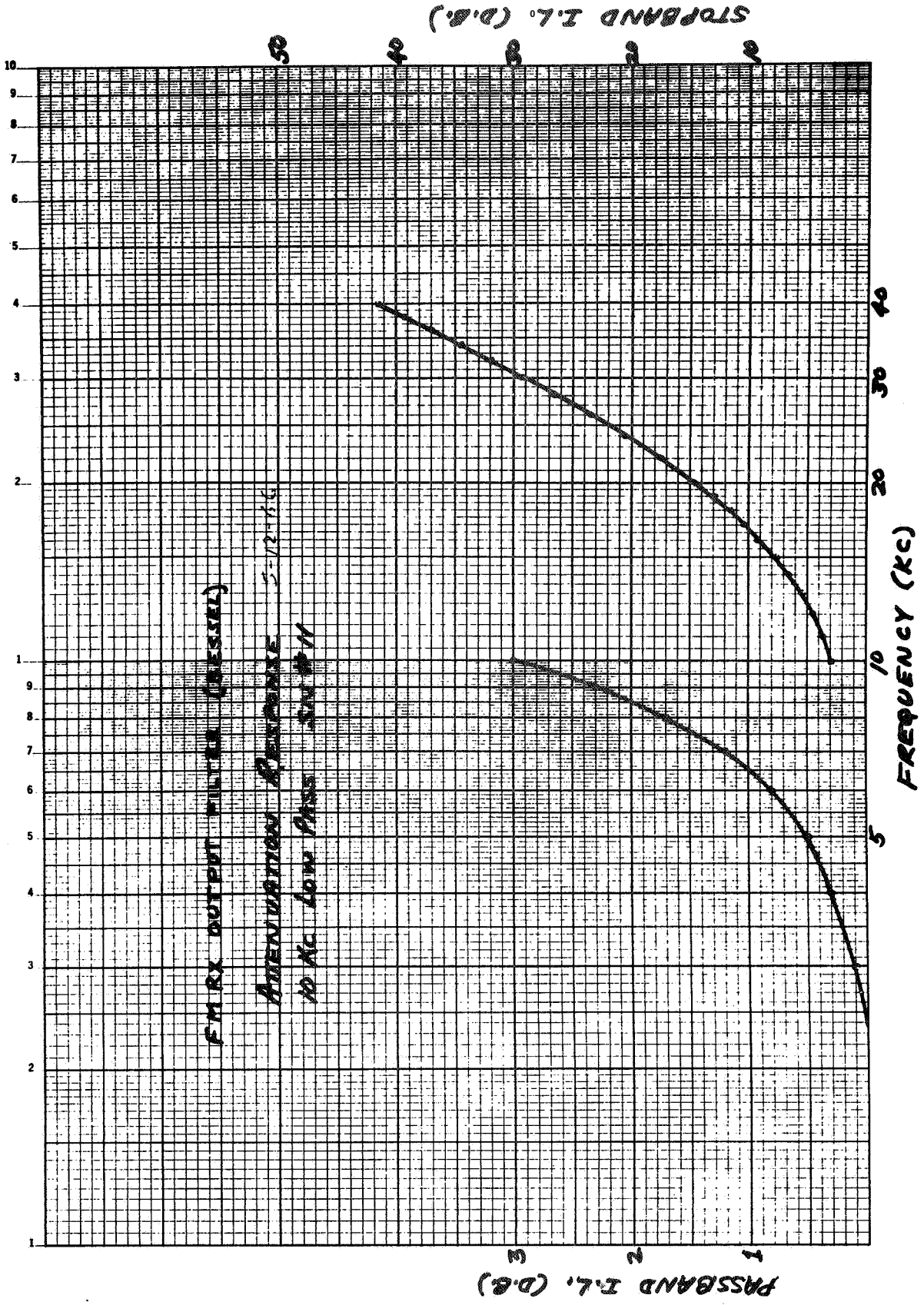


Figure 3.3.2.32. F.M. Rx Output Filter (Bessel)
Attenuation Response 10 Kc Low Pass SN #11

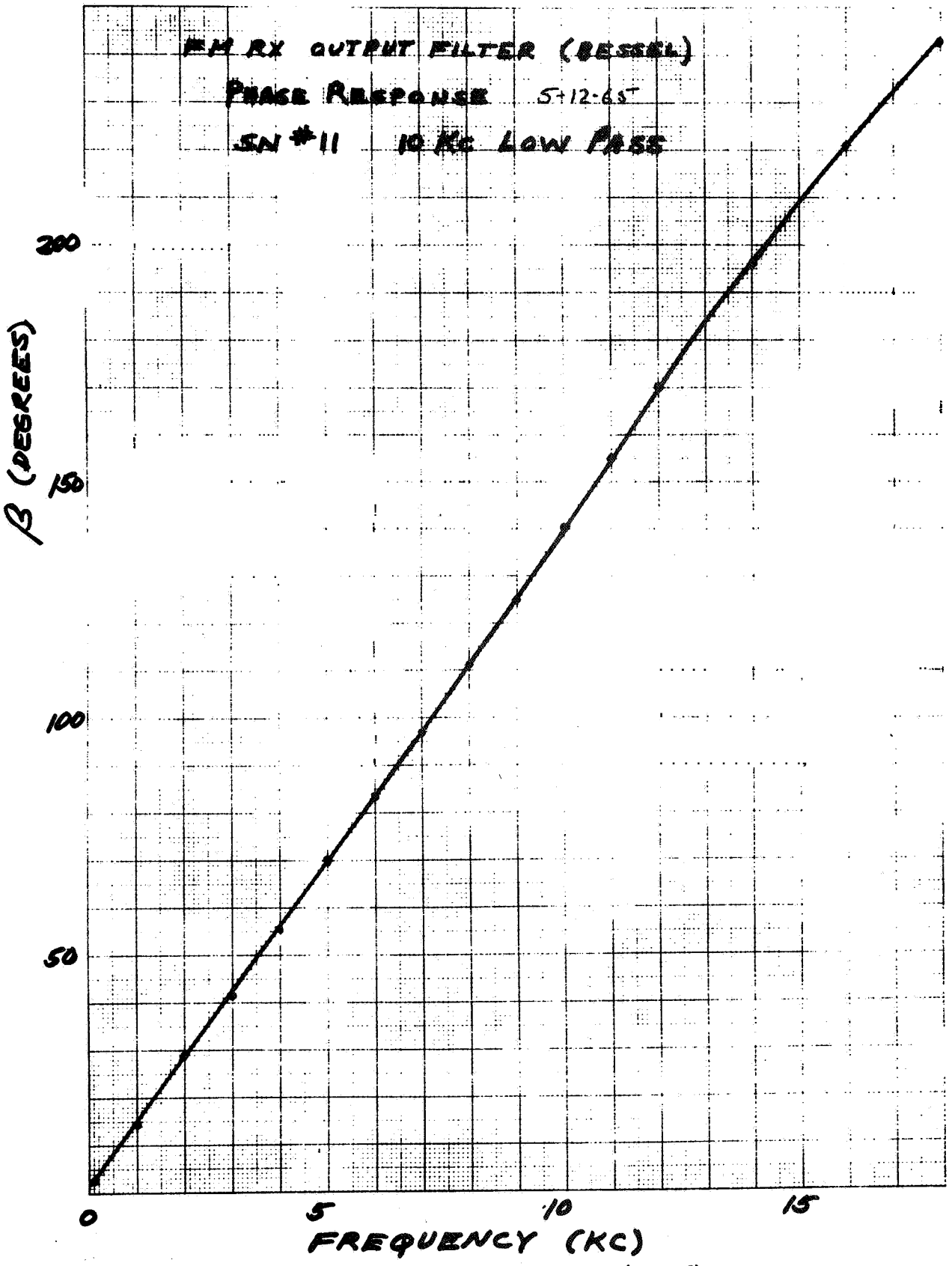


Figure 3.3.2.33. F.M. Rx Output Filter (Bessel)
Phase Response SN #11 10Kc Low Pass

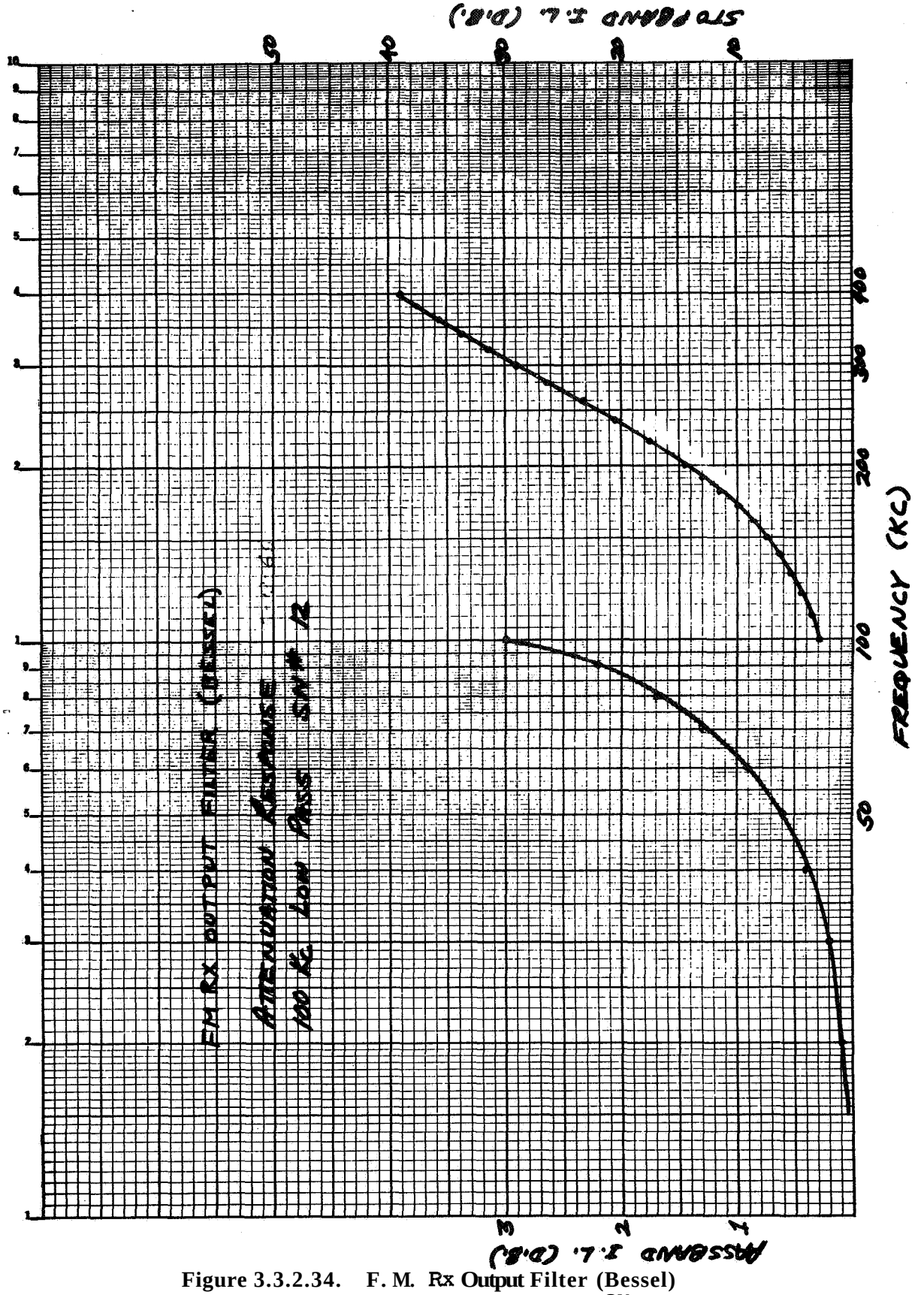


Figure 3.3.2.34. F. M. Rx Output Filter (Bessel) Attenuation Response 100Kc Low Pass SN #12

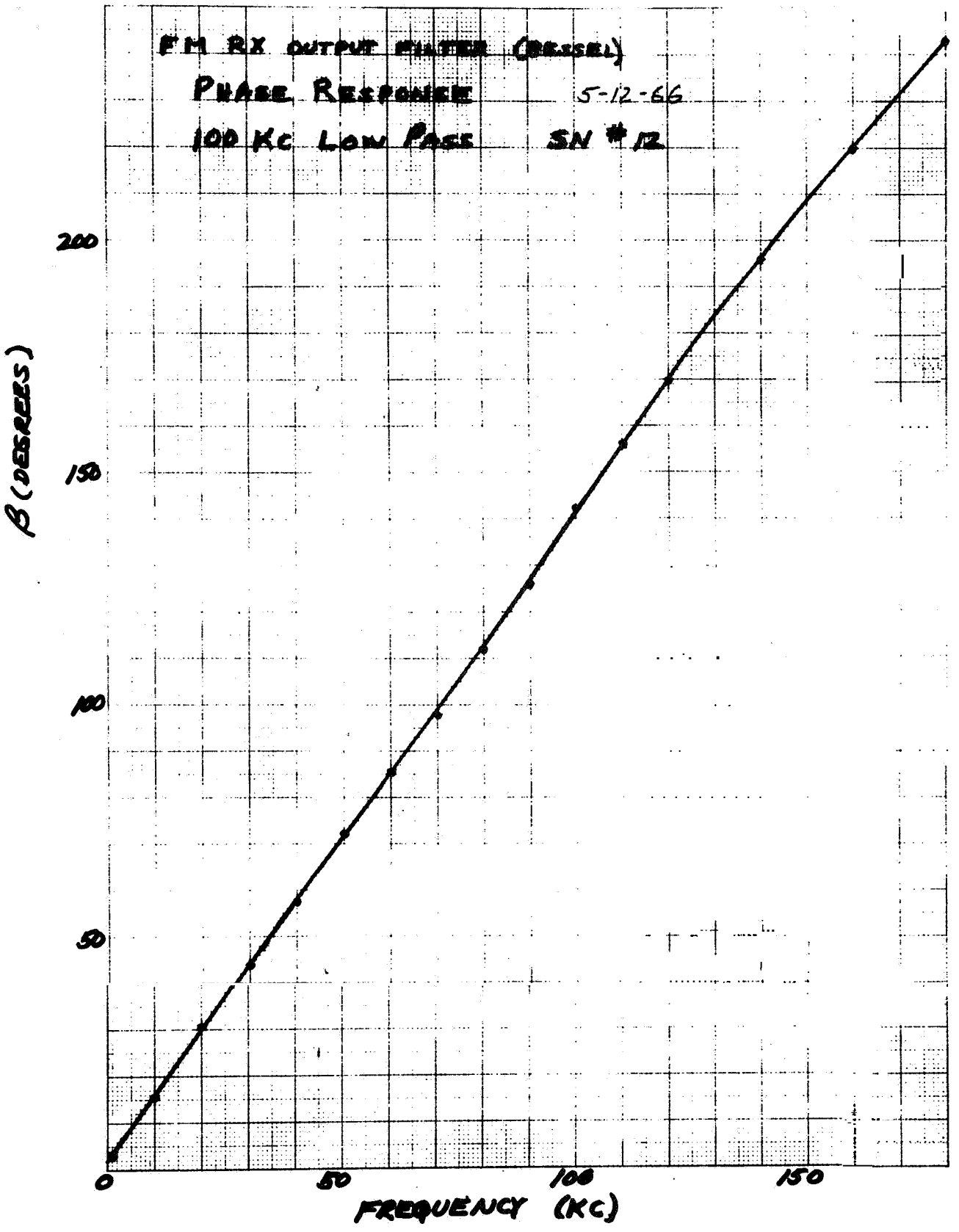


Figure 3.3.2.35. F. M. Rx Output Filter (Bessel) Phase Response 100Kc Low Pass SN #12

OUTPUT NOISE POWER / AGC

INPUT NOISE	OUTPUT NOISE POWER			
	AGC 0.0	AGC 0.5	AGC 1.0	AGC 1.5
KTB	-9.7dbm	-10.2dbm	-11.4dbm	-12.0dbm
KTB +19db	-0.6dbm	-1.0dbm	-2.0dbm	-2.6dbm

OUTPUT CARRIER POWER FOR INPUT POWER

INPUT	OUTPUT
0dbm	-19.2dbm
-3dbm	-22.2dbm
-5dbm	-29.2dbm

COMBINATIONS OF OUTPUT NOISE AND CARRIER POWERS
OVEN TEMPERATURE - 39.5°C
NOISE BANDWIDTH - 19.137 MHz

C. L. Sandy 12/13/66

Figure 3.4.1. Noise Amplifier Characteristics as a Function of Bias Voltage

The typical operating point is indicated by curve three at a "Bias Adjust" dial setting of 1.0.

Figure 3.4.2 indicates the Power Transfer of the Noise Amplifier/Filter at an oven temperature of 39.5°C. The operating point and its relationship to saturation is shown.

The noise preamplifier and power amplifier were retuned at an oven temperature of 39.5°C. Figure 3.4.3 indicates the test set used to align the noise amplifier. As shown, the dual channel insertion loss test set was used to accurately measure the noise amplifier response. This system includes two principal advantages that yield 0.01 db resolution. First, variations in the input signal are common to both the reference and signal channel and cancel. Secondly, the RF Power in both the reference and signal channels are converted to 1 Kc tones. Therefore, variations in the signal channel (as a function of frequency) are compensated by precision audio attenuators in the signal channel to achieve a null. The noise amplifier response is read off the audio attenuator setting required to achieve null. Initially, the system is calibrated with the noise amplifier replaced with a calibrated fixed pad. Figures 3.4.4 through 3.4.7 indicate the noise amplifier responses at oven temperature for various AGC operating points. Figure 3.4.8 indicates the overall noise amplifier/filter 3 db bandwidth. The 3 db bandwidth shown was measured in a manner whereby the frequency accuracy is determined by the crystal controlled frequency synthesizer and the amplitude accuracy by the Weinschel Dual Channel System.

Figure 3.4.9 indicates the Summer Noise Power Output for various "Bias Dial Settings". The measured Summer carrier power output as a function of carrier power input is also shown.

The Summer is organized such that a narrow band crystal filter centered on 50 Mc can be cabled in the noise channel. This feature is included in the Test Console such that the PM Receiver carrier tracking loop threshold tests can be made without overloading the receiver front end with wideband noise. Figure 3.4.10 indicates the test set used to measure the crystal filter bandwidth. Figure 3.4.11 indicates the filter response.

Table 3.4.1. Linear S/N Summer Test Results

1.	S/N Dynamic Range	100 DB
2.	Absolute Accuracy	±0.156 DB over 100 DB Range
3.	S/N Ratio Repeatability	±0.024 DB
4.	S/N Ratio Stability	±0.013 DB over 4 hour period
5.	Noise Power Spectral Density	±0.05 DB over, 4 MHz contered at 50 MHz.

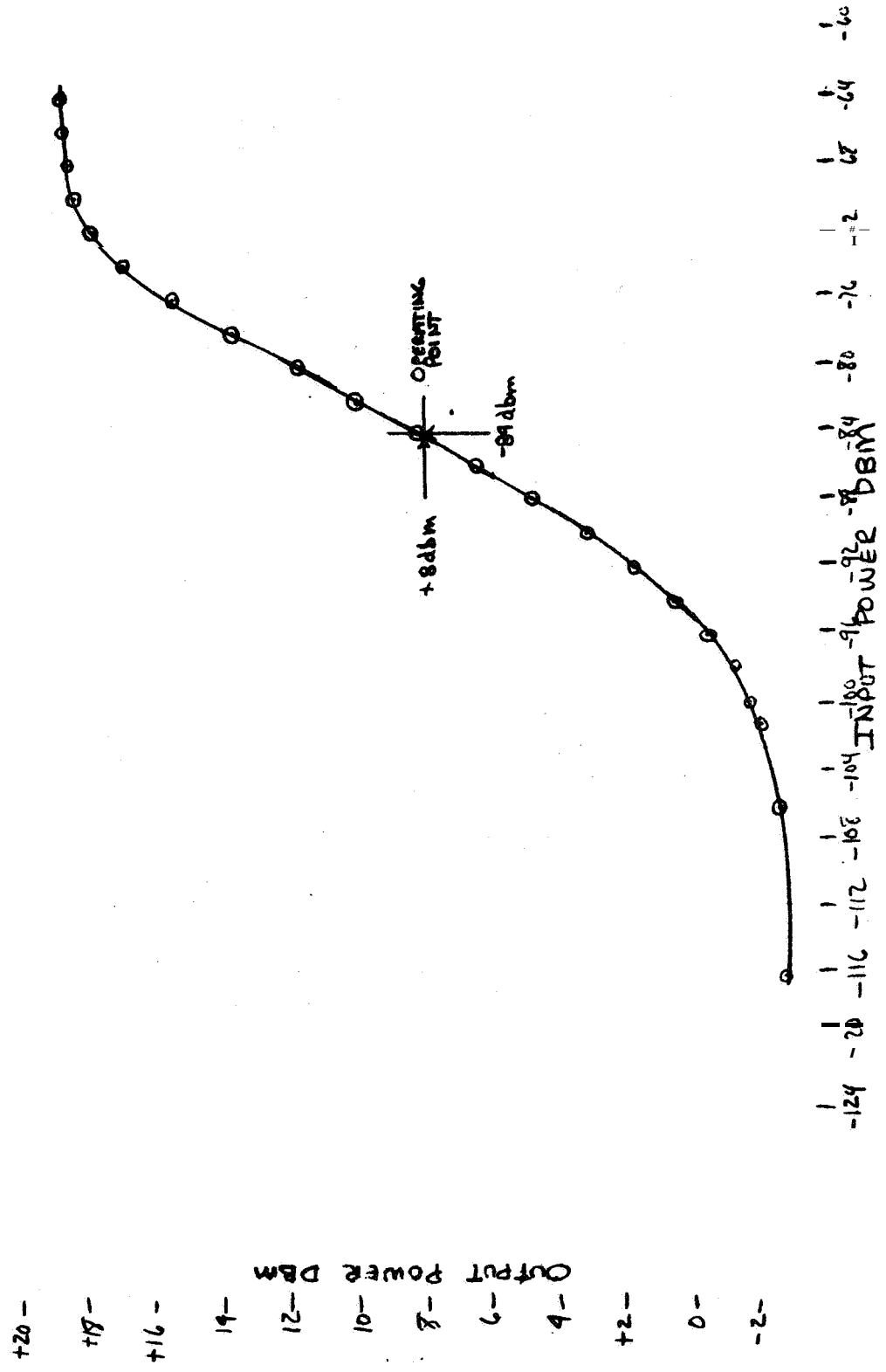


Figure 3.4.2. Power Transfer of Noise Amp./Filter Taken at Oven Temperature 39.5°C

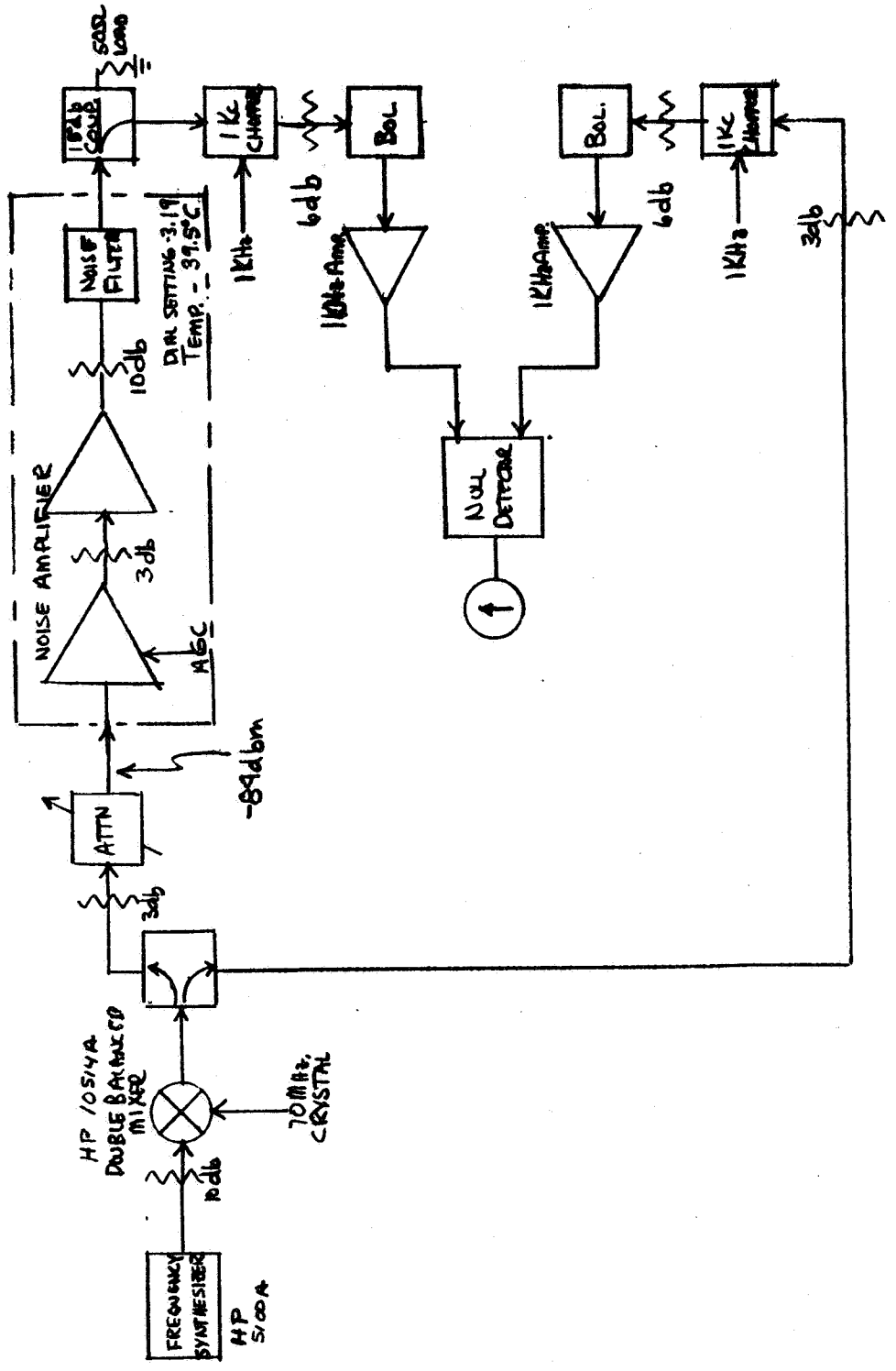


Figure 3.4.3. Block Magram of Test Set Up For Noise Amplifier Frequency Response

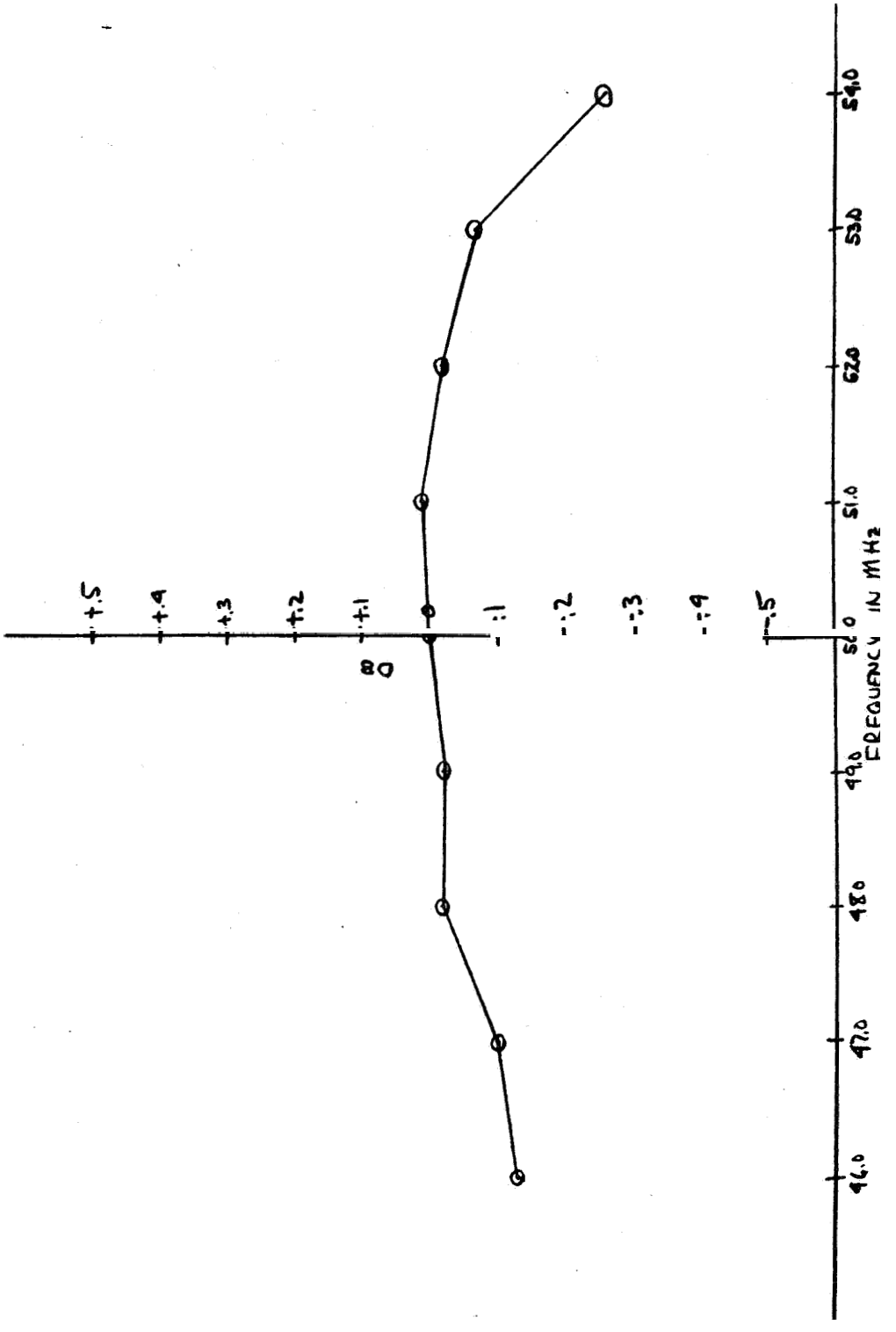


Figure 3.4.4. Pass Band Response Frequency vs. Relative Response (DB)

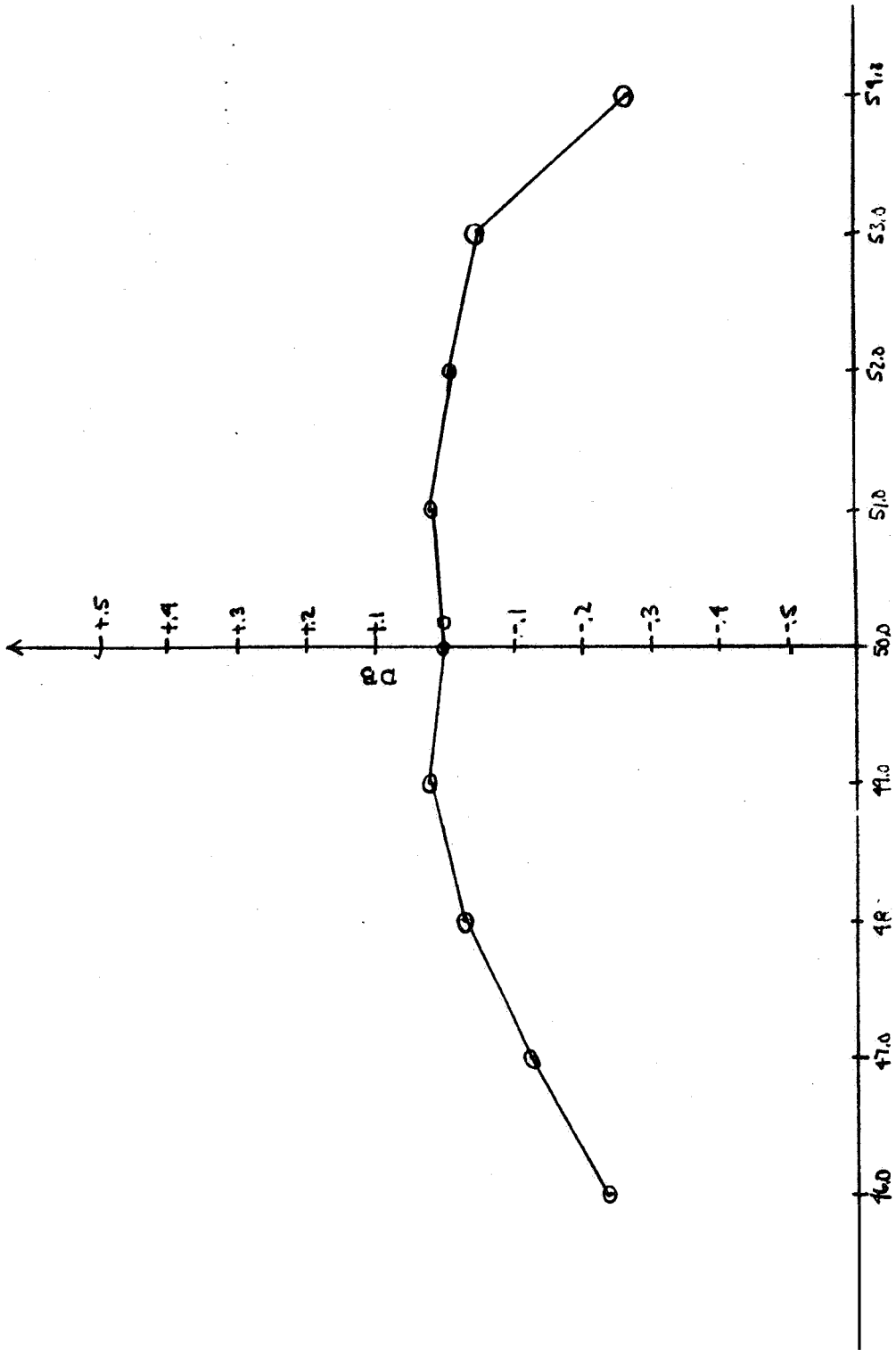


Figure 3. 4. 5. Pass Band Response Frequency vs. Relative Response in DB

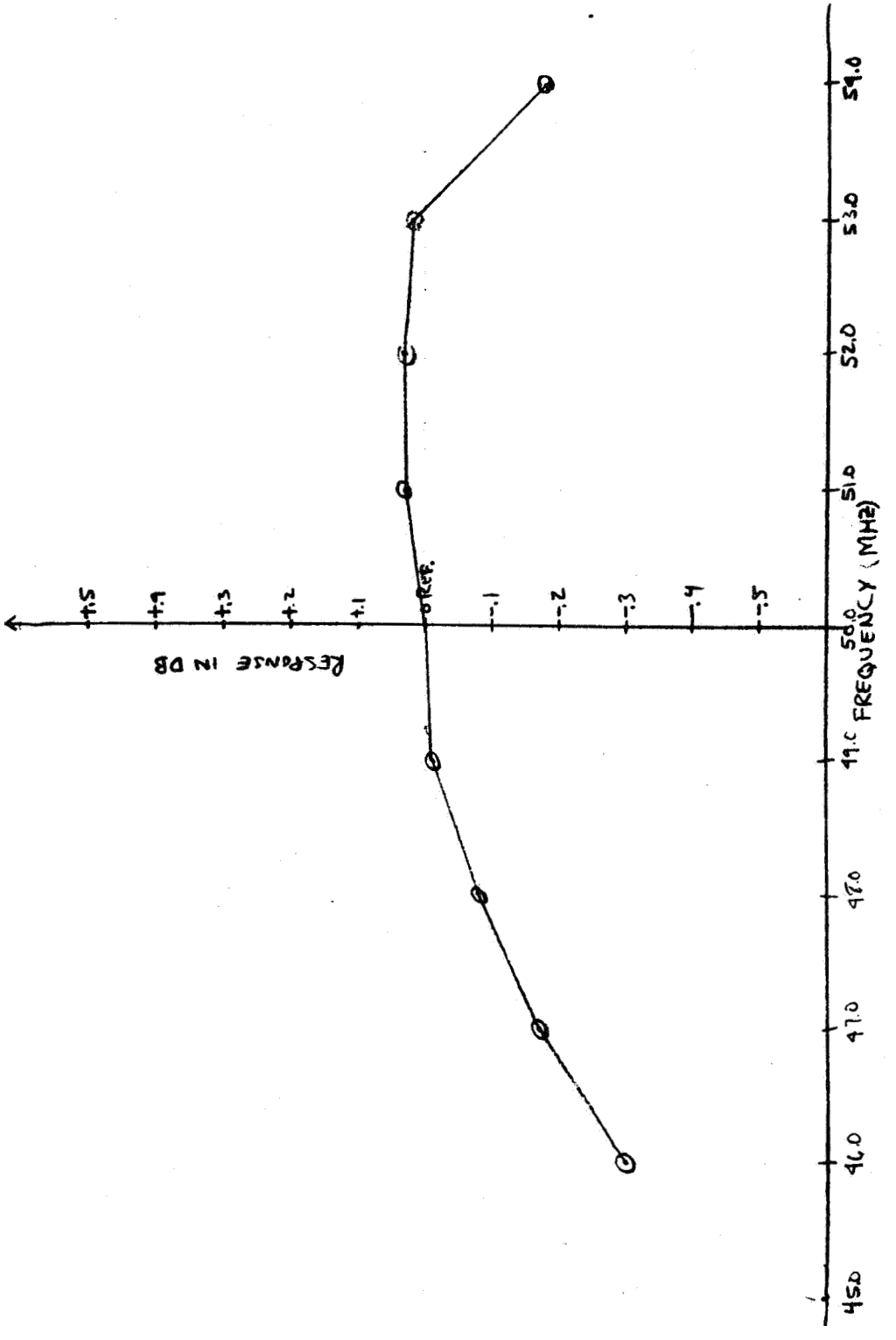


Figure 3.4.6. Pass Band Response Frequency vs. Relative Response in DB

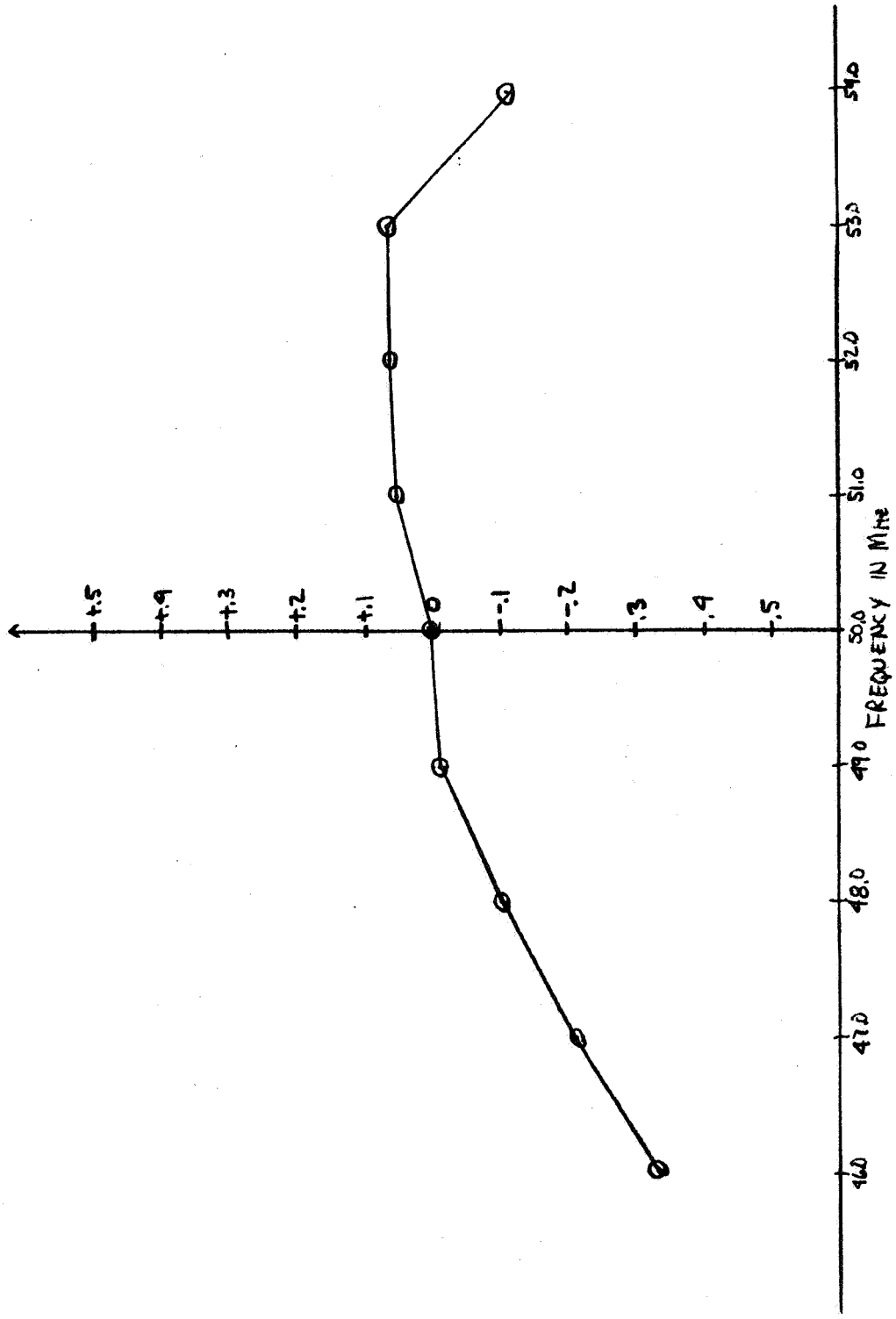


Figure 3.4.7. Pass Band Response Frequency vs. Relative Response

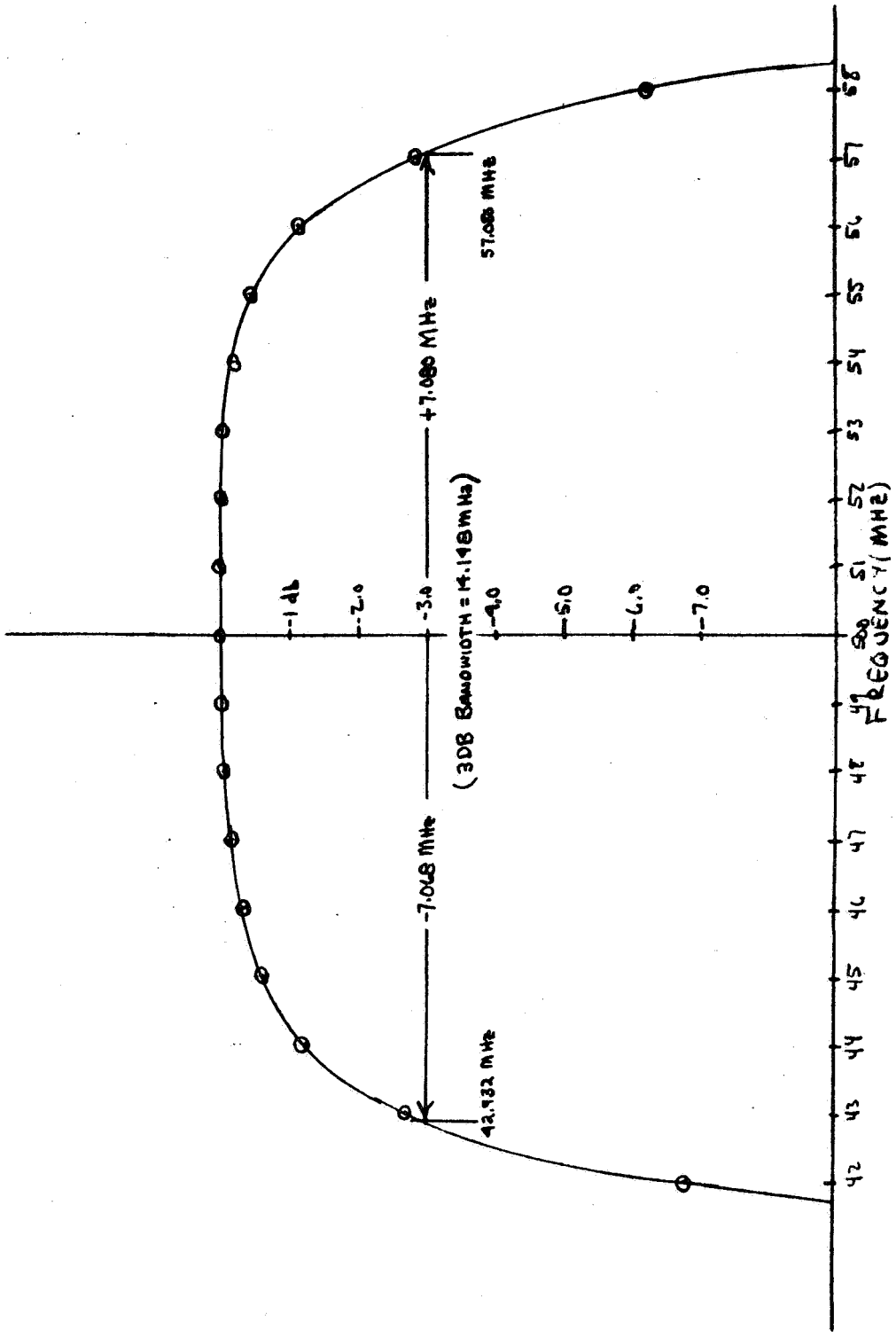


Figure 3.4.8. Noise Amplifier Freq. Response

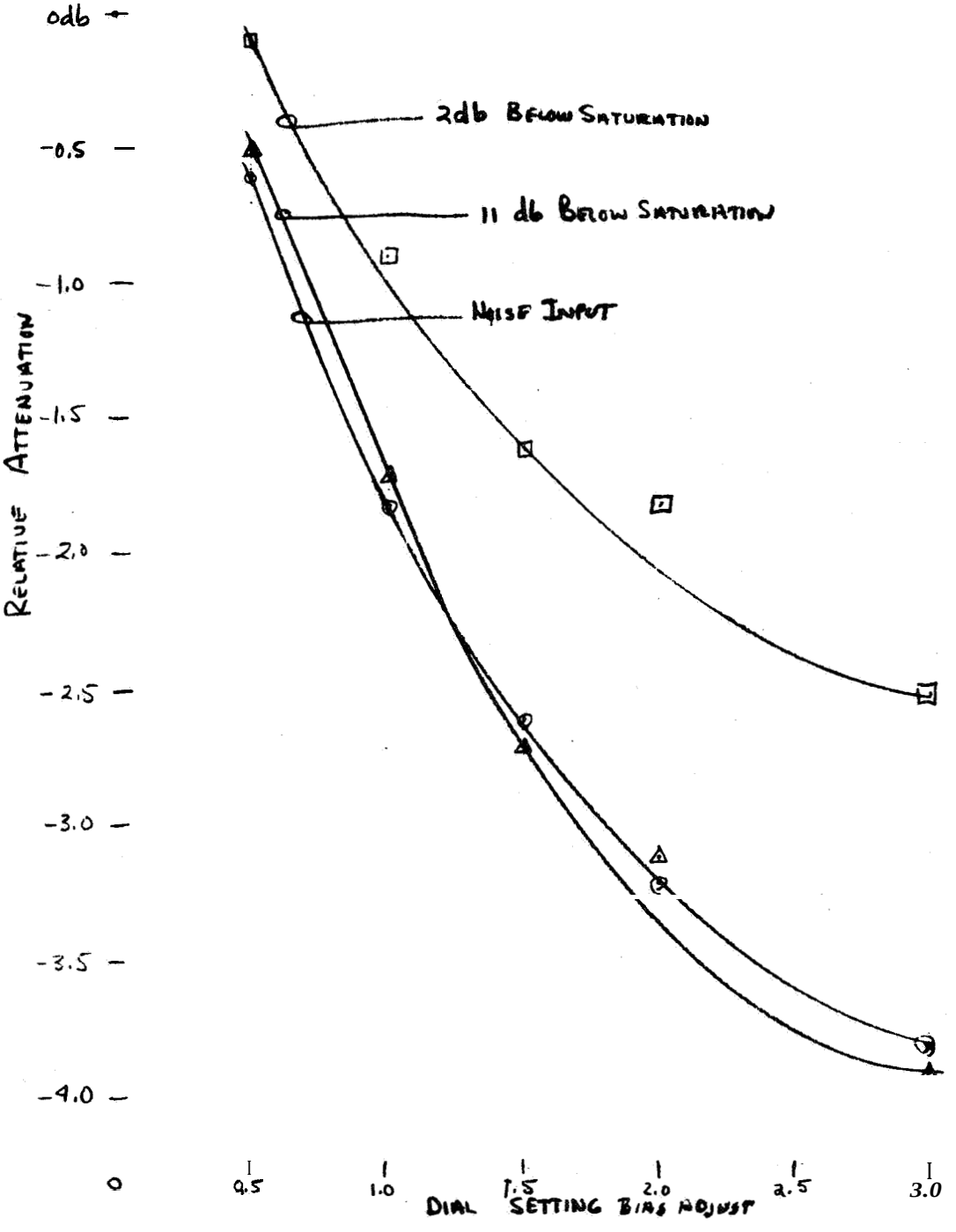


Figure 3.4.9. Summer Noise Power Output for Various "Bias Dial Settings"

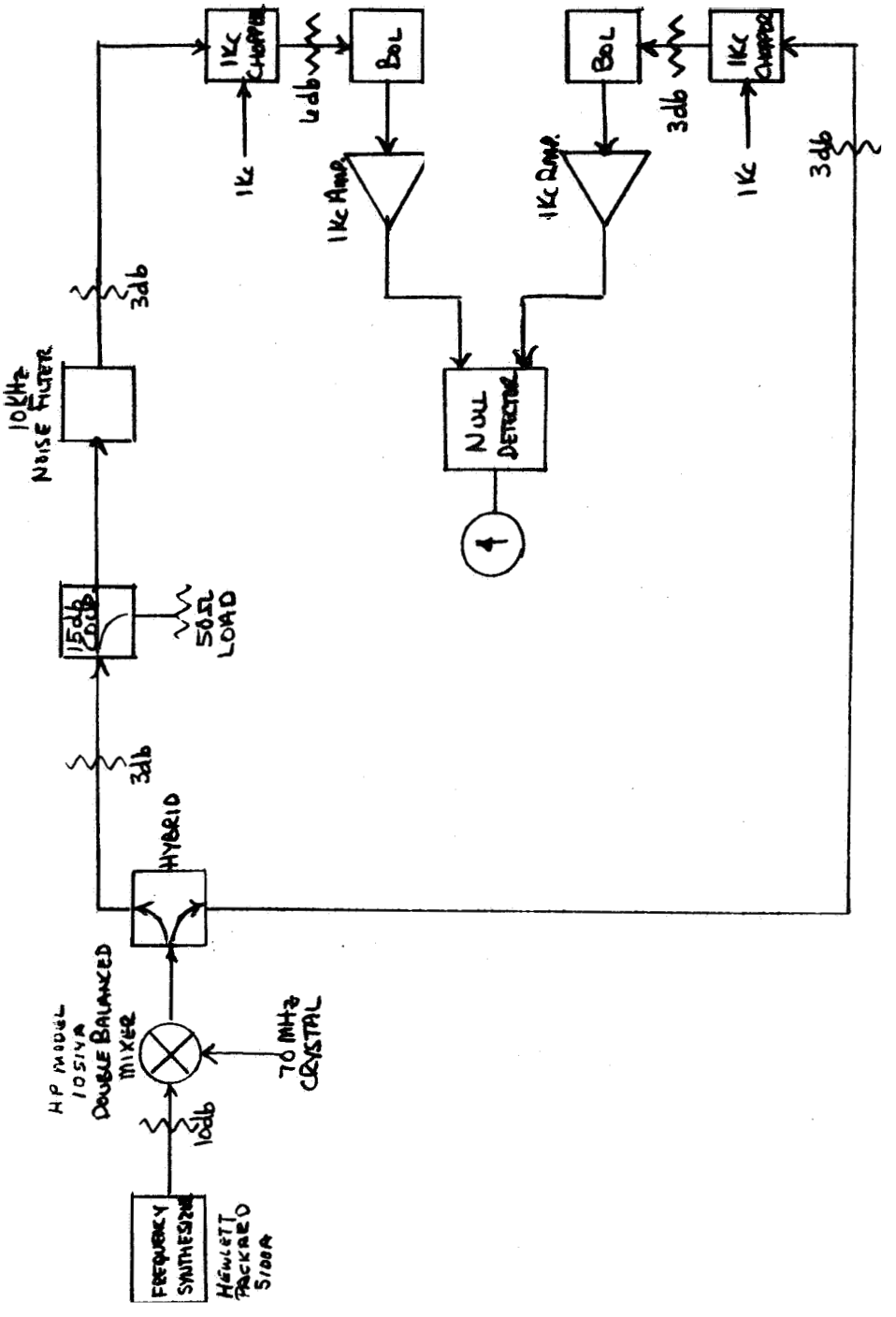


Figure 3.4.10. Block Diagram of Test Set-up For 10 KHz Noise Filter Freq. Response

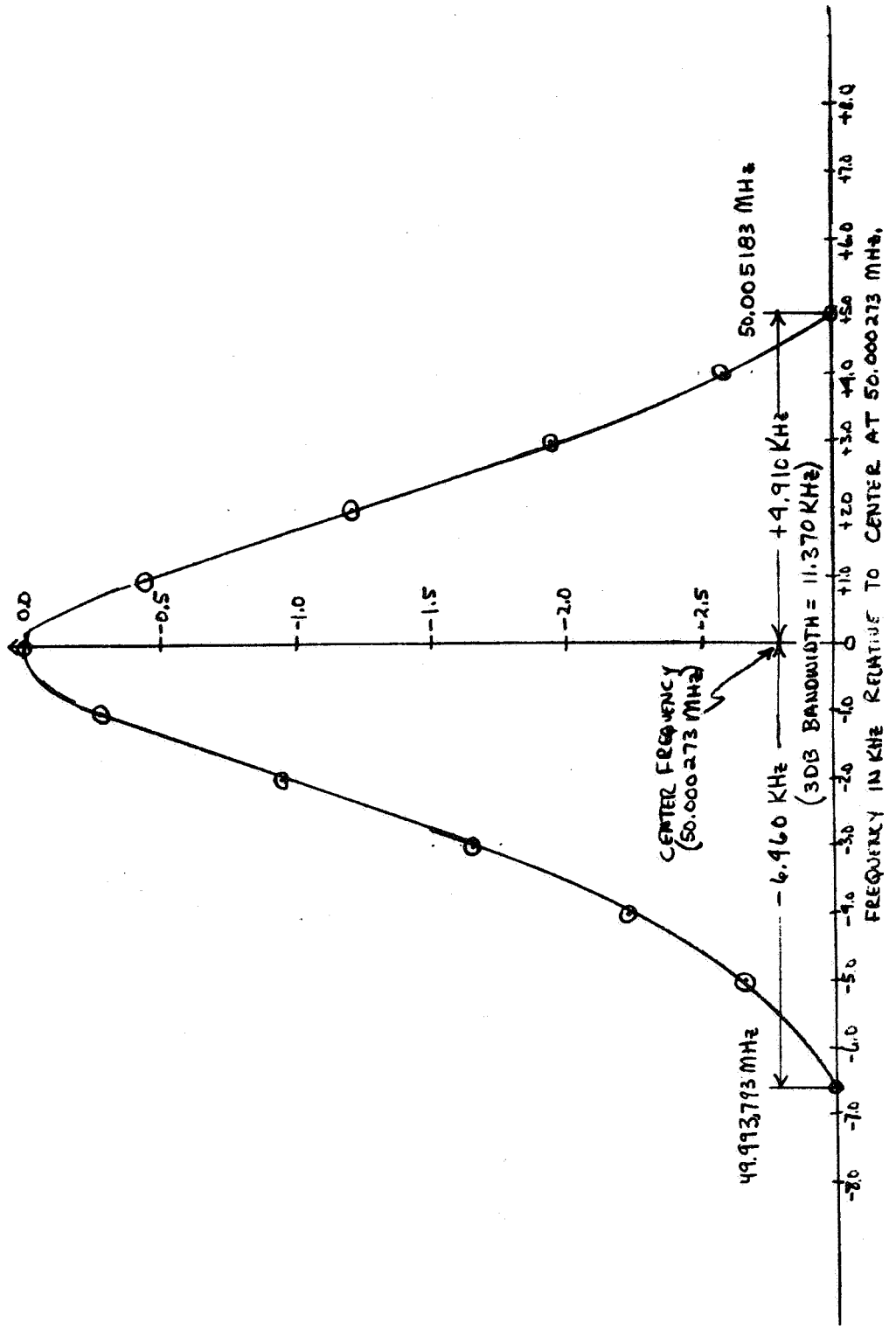


Figure 3. 4. 11. 10 KHz Noise Filter Response
Frequency vs. Relative Response in DB

3.5 PHASE NOISE AND TEST INSTRUMENTATION

In addition to the commercial test instruments included in the RF Test Console, the system includes hardware to measure the P. M. Receiver carrier tracking loop VCO phase noise and the P. M Modulator carrier suppression. Figure 2.6.1 is the block diagram of this subsystem. As shown the VCO 1 Mc output is multiplied to 60 Mc and is down converted to 10 Mc by mixing with the 50 Mc transmitter reference. The resulting 10 Mc is phase compared with a 10 Mc reference derived from the P. M Receiver reference oscillator. The Hewlett-Packard Vector Voltmeter samples the 10 Mc reference and the 10 Mc spectrum derived from the VCO. The two inputs are reconstructed at 20 Kc by a sampling technique. The information bandwidth retained is dictated by the Nyquist sampling rate. The 10 Mc spectral bandwidth (carrier plus noise) is constrained by a 2 Kc crystal filter in the 10 Mc I-F amplifier. The bandwidth determined by the sampling rate is 10 Kc. The reconstructed 20 Kc waveforms are phase compared with a linear phase detector (set-reset flip-flop and low pass filter) . The resulting phase detector characteristic is shown in figure 3.5.1.

The coherent carrier suppression measurement system shown in figure 3.5.2 provides a means of converting the 50 Mc carrier power to a D. C. voltage. The conversion is achieved by phase comparing the P. M spectrum with a coherent 50 Mc reference. The phase detector output is filtered whereby the polarity and magnitude of the D. C. term is a measure of the 50 Mc carrier power as dictated by the J_0 Bessel coefficient.

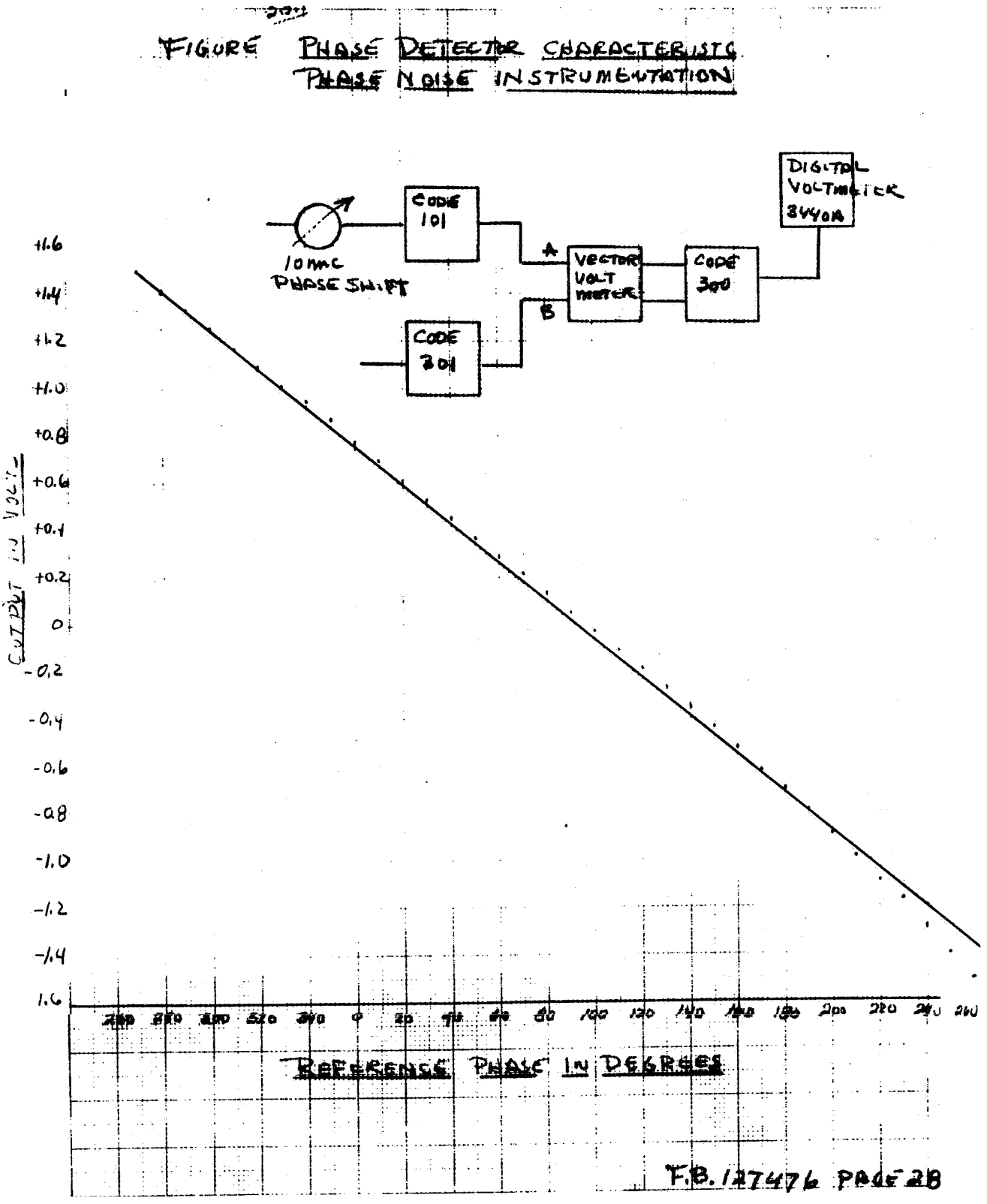


Figure 3.5.1. Phase Detector Characteristic
Phase Noise Instrumentation

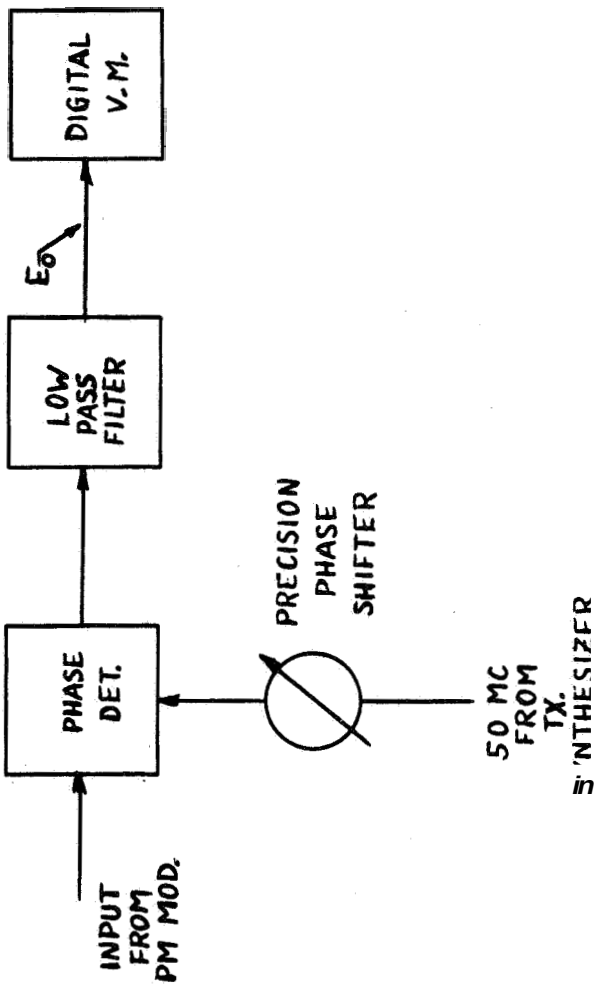


Figure 3.5.2. Carrier Suppression Measurement System

APPENDIX A

Specification

Submitted as Part of the Final Report
for RF Test Console on JPL Contract 951140

Date: 2 May 1967

Prepared by: Westinghouse Electric Corp.
Surface Division
P.O. Box 1897
Baltimore, Md. 21207

1.0 Appendix A includes the correlation between the R. F. Test Console specifications and measured data. The material is presented in order of appearance in the Specification (Third Revision). Only the specific specifications and test results are listed. The boiler plate (paint specification, etc.) and peripheral data is not included in this document. The simplified block diagrams listed in the original specification are included in Appendix D and are not repeated in this document.

P. M. SUBSYSTEM

Principal Specifications & Test Results

1. Frequency Stability

The frequency stability of both the transmitter frequency source and the receiver reference oscillator shall be as follows:

	MEASURED	SPECIFIED
a.	2.3 parts in 10^{-10}	a. Each shall have a short term stability measured over a one-minute period of 1 part in 10^7.
b.	4. 4 parts in 10^{-9}	b. Each shall have a long term stability measured over a four hour period of five (5) parts in 10^7.

2. Phase Stability — 0.25 RMS in 2 B_{LO} of 3.0 cps.

The phase stability of the unmodulated Tx/Rx pair shall be such as to cause no more than one degree rms phase error in 2BL of 3.0 cps.

3. Fidelity

$\Delta\theta$	p	q	[Combinations of p and q]
± 1 rad	10kc ODB	9kc ODB	Worst Case -46.5 DB
± 2 rad	10kc ODB	9kc ODB	-49 DB
± 4 rad	10kc ODB	9kc ODB	-44 DB
± 4 rad	100kc ODB	90kc ODB	-39 DB
± 4 rad	500kc ODB	450kc ODB	-45 DB
± 1 rad	1000kc ODB	900kc ODB	-34 DB

The fidelity of the Tx/Rx pair shall be such that all spurious sidebands within the modulation passband are 30 db (40 db design goal) below the modulated carrier or 40 db (50 db design goal) below unmodulated power when the transmitter is modulated with two pure sinusoids of any frequency and at modulation indices within the phase modulator design limits.

P. M. TRANSMITTER

Principal Specifications & Test Results

		MEASURED	SPECIFIED
1.	Carrier Frequency	50 mc/s ±500 cps	50 mcs Tunable ±500 cps
2.	Frequency Response	±0.1DB DC to 500KC/s ±0.4DB DC to 1.0MC/s	±0.1 db DC to 500 KC ±0.5 db 500 KC to 1.5 mcs
3.	Phase Deviation	k3.0 Radians DC to 500 KC ±1.0 Radian DC to 1.5 mcs	i3.0 radians D. C. to 500 KC ±1.0 radian D. C. to 1.5 mc
4.	Deviation Linearity and Incidental AM	See PM Tx/Rx Subsystem spec.	See PM Tx/Rx pair spec.

AMPLITUDE MODULATOR

Principal Specifications & Test Results

		MEASURED	SPECIFIED
1.	Frequency Response	+0. 1DB from DC to 10KC, 3DB Bandwidth greater than 1MC.	±0. 1DB from D. C. to 5. OKC.
2.	Per Cent Modulation	100 per cent	i50 per cent in voltage.
3.	Modulation Linearity	Two equal tones applied within 5KC band. One hundred per cent peak modulation index. Worst inband intermodulation -26DB with respect to either of the two equal tones.	5 per cent 1 per cent (design goal)
4.	Incidental P. M.	P. M., measured in RCVR carrier tracking loop [1-H(s)] when AM modulator 50% modulated, less than 1 degree peak to peak.	Compatible with Phase Stability Spec.

P. M. RECEIVER

Principal Specifications & Test Results

		MEASURED	SPECIFIED
1.	Carrier Frequency	50 MC	50 MC
2.	Input Amplifier		
	a. Bandwidth	3DB BW, 12 MC/S 56.20 - 44.17 mc/s 0.5DB BW, 4.35 mc/s 52.27 - 47.92 MC/S	3db B. W. 10 mcs min. flat within ± 0.25 db within ±2 mc of 50 mcs.
	b. Phase Linearity	Maximum Flat Group Delay	Compatible with P. M. Subsystem Linearity Spec.
	c. AGC Range	30 DB	30db
3.	Narrow Band IF		
	a. Center Frequency	10 mc/s	10 mcs
	b. Bandwidth	10 MC/S + 1,050 cps 10 MC/S - 1,080 cps	2 KC (3db) Centered on 10 MC
	c. Phase Symmetry	±5° Phase Symmetry ±3.5 KC of center frequency	15" for frequencies ±1 KC of center frequency (± 6 KC Design Goal)
4.	Wideband IF		
	a. Center Frequency	10 MC	10 MC
	b. Bandwidth	6.8 MC (3 DB) ±0.5DB + 2.2 MC - 1.6 MC of center frequency	6 MC (3db) ±0.5 db within 1.5 mc of center frequency.
	c. Phase Symmetry	15 Degrees over 6 mc/s passband, geometric symmetry	± 5 degrees over 6 mc passband.
5.	Wide Band Phase Detector		
	a. Video 3 db Bandwidth	5 mcs	5 mc
	b. Dynamic Range	50 DB (Min)	40 db
	c. Fidelity	See subsystem Linearity Spec.	Compatible with P. M. Subsystem Linearity Spec.

P. M. RECEIVER (Continued)

		MEASURED	SPECIFIED
6.	Carrier Tracking Loop		
	a. No Noise Loop Gain	$\Delta\theta$ = 2" for Tx detuning Δf, 1 000 cps	Constrain Static Phase Error ±1 Degree Transmitter. Detuning ±500 cps
	b. Loop Bandwidths $2 B_{LO}$	2.7, 11.3, 19.3, 48.6 cps	3.0 12.0 20.0 and38.0 cps, variable 1.0 cps = 1KCs
	c. Loop Filter	1%Res. 3% Cap.	Active and passive, 1% resistors, 3% capacitors
	d. Loop Gain Stability	±3% over Tx Tuning Range	±3% over transmitter tuning range
7.	AGC Loop		
	a. Min. Loop Gain	20	20
	b. Loop Noise Bandwidths	0.1, 1.0, 10 cps 0.1 not measured	.01, 0.1, 1.0 and 10 cps
	c. Loop Filter	1%Res. 3%Capacitors	Passive, 1%resistors 3% capacitors
8.	Predetection Record and Playback		
	a. Record	Yes	P. M. Spectrum down converted to 50 mcs
	b. Playback	Yes	Recorder spectrum up converted to 50 mcs
9.	Balanced Modulators	2fl - fr =-40DB All other products greater than 60 DB below the desired output.	All spurious and feedthru products 50DB below the desired output.

Phase Noise Instrumentation

Principal Specifications & Test Results

		MEASURED	SPECIFIED
1.	Phase Shifter	Center frequency, 10 MC continuously variable 0-360" Dial Calibration accuracy ±1 degree	Center frequency, 10 MC continuously variable 0-360" Dial Calibration Accuracy ± 1 degree
2.	Lineary Phase Detector Characteristic E_o V_s θ_{in}	One per cent over 300 degree Range[Binary dividers not used]	Binary Divider and Limiter Rise and Fall times specified not applicable to Subsystem built.

F.M. SUBSYSTEM

Principal Specifications & Test Results

		MEASURED	SPECIFIED
1.	**Frequency Stability**		The frequency stability the FMS **Tx/Rx** pair **shall** be such as to cause less than **15** cps **RMS** residual F. M. with the Tx operating in the AFC Mode and 60 cps rms residual **F.** M in non/AFC mode measured in either conventional or phase lock receiver in **a** 500 KC bandwidth.
2.	Static Linearity	Within ±0. **5** percent, Phase Lock Rx, Conv. Rx	The Tx/Rx pair shall exhibit a static linearity of ±0. **5** percent over the full-scale frequency deviation with the non/AFC Transmitter and either receiver above and beyond the inherent sinusoidal phase detection non-linearity.
3.	Dynamic Linearitv		The **Tx/Rx** pair shall exhibit a dynamic linearity of ±1. **0** percent over all combinations of modulating frequency and frequency deviation in both AFC and non/AFC transmitter modes and with either receiver above and beyond in inherent sinusoidal phase detector non-linearity

	PHASE LOCK RCVR.	CONVENTIONAL RCVR	
AFC Tx	**77. 5 cps**	**69 cps**	**100 KC BW**
Non AFC Tx	**88. 2 cps**	**69 cps**	

AFC/Tx	500 KC/s **Phase** Lock Rx	**B.** W. Conv. Rx
Non AFC Tx	**165 cps**	**195 cps**
	170 cps	**211 cps**

AFC **Tx**	-44. 5DB	-43DB
Non	-43 DB	-42DB

Noise Loading Results
RMS Deviation = **67** KC

	Phase Lock Rx	Conv. Rx
AFC **Tx**	**-41DB**	**-41DB**
Non AFC **Tx**	-41DB	-41DB
	-41DB	**-41DB**

Slot Ratio

Slot Ratio not specified

F. M. Tx

Principal Specifications & Test Results

		MEASURED	SPECIFICATIONS
1.	Frequency Response	±0.1DB,50 cps to 100 KCS. ±0.5DB, 3 cps to 50 cps and 100 KC/s to 500 KC/s	The frequency response of the frequency modulator shall be constant with ±0.1db from 50 cps to 100 KC and ± 0.5 db from 3 cps to 50 cps and 100 KC to 500 KC.
2.	Frequency Deviation	± 500 KC β = 512 in AFC	The modulator shall be capable of deviating the carrier ±500 KC about its center frequency with a maximum modulation index of 512 in the AFC mode.
3.	Deviation Linearity	Refer to FM Subsystem measurements	Refer to FM Subsystem Specifications.
4.	AFC Operation	3 cps - 500 KC AFC DC - 500 KC Non AFC	The F. M. Transmitter shall be capable of operating either with or without automatic frequency control. In the AFC mode its modulation response shall be from 3 cps to 500 KC and in non/AFC from DC to 500 KC.

F.M. RCVR

Principal Specifications & Test Results

	MEASURED	SPECIFIED
1. Input Band Pass Filters	a. 50.0 MCS + 0.526 MC/s 50. OOMCS - 0.454 MC/s b. 50.0 MCS + 0.100430 MC/s 50.00MC/s - 0.098660 MC/s c 50.00MC/s + 0.005109 MC/s 50.00MC/s - 0.005100 MC/s	The Input Filters shall have half power bandwidths within ±2 percent of 1 mc, 200 KC and 10 KC.
a. Phase Response	Max Flat Group Delay	The filter's phase response shall be linear as established by a Bessel Response.
b. Amplitude Response	Yes	The Amplitude Response shall be established by the 3 db bandwidth and the phase characteristics.
2. Limiter		
a. The Dual F. M. Rx shall contain a hard limiter following the input band-pass filter with the following characteristics:	ΔE_{IN} = 60 DB ΔE_{OUT} = 1 DB	The limiter shall have a dynamic range of 60 db.
3. Conventional F. M. Detector	See F. M. Subsystem Tests	The Dual F. M. Rx will include a conventional F. M. Detector with performance characteristics consistent with the F. M. Subsystem frequency stability and static and dynamic linearity requirements.
4. Phase Lock F. M. Detector		
a. VCO	Yes	The VCO center shall have a center frequency of 50 mc.

	MEASURED	SPECIFIED
	See Subsystem measurements	The deviation capability shall be consistent with the transmitter modulator characteristics.
	See Subsystem measurements	The static and dynamic linearity and stability shall be consistent with the F. M. Subsystem Specifications.
b. Phase Detector	3DB Video Bandwidth 4.94 MC/s	The phase detector bandwidth shall be consistent with the Tx modulator frequency response. It shall be of sufficient fidelity to meet the subsystem dynamic linearity requirements.
c. Loop Gain	9.2" for input Δf = 500 KC	Sufficient to constrain static phase error to 10 degrees when Tx deviation is maximum (500 KC).
d. Loop Filter		Three standard loop information bandwidths of 3, 30 and 300 KC shall be supplied.
e. Compensation Filter	Measured match computed except f_n = 300 KC, Transport lag introduces deviation from computed response for f_n of 300KC	A single pole R. C. low pass filter shall be employed at the loop filter output such that the overall phase-lock F. M. detector transfer function is that of a pure loop.
5. Output Low Pass Filter		
The Dual F. M. Rx shall include a single low-pass output filter with the following characteristics:	5 pole max. flat Amp. 5 pole max. flat group delay 1, 10, & 100 KC/s Supplied	The output filter shall have more than three poles and shall have either maximally flat amplitude or maximally flat phase response. Filter bandwidths of 1, 10 and 100 KC shall be supplied.

	MEASURED	SPECIFIED
6. Predetection Record and Playback		
a. Record	Yes use same hardware as in P. M. Rec.	F. M. Spectrum down converted to 5 mcs.
b. Playback	Yes use same hardware as in P. M. Rx	Recorder Spectrum up converted to 50 mcs.

202

SIGNAL TO NOISE SUMMER

Principal Specifications and Test Results

		MEASURED	SPECIFIED
1.	Dynamic Range	0-100DB	0-100DB
2.	Noise Bandwidth	Within the bounds ±0.05DB, 48 - 52 MC	±0.05DB from 48 to 52 MC
3.	Over All Abolute Accuracy Over A Four Hour Period	S/N Ratio accuracy, ±0.156DB over 100DB dynamic range, S/N Ratio repeatibility, ±0.024DB, S/N Ratio Stability, ±0.013DB over 4 hr. period	±0.3DB
4.	Noise Power Spectral Density	Within the bounds ±0.05DB From 48 to 52 MC. Measured in 500 cps B.W. in 2 KC increments from 50.01 to 49.99 MC. Measured in 5KC BW in 20 KC increments from 50.1 to 49.9 MC. Measured in 50 KC B.W. in 200 KC increments from 48 to 52 MC	±0.05DB from 48 to 52 MC