FIFTH RELIABILITY ASSESSMENT FOR THE ORBITING GEOPHYSICAL OBSERVATORIES

PRC R-621

31 OCTOBER 1964

PREPARED FOR

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GODDARD SPACE FLIGHT CENTER

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Under Contract NAS5-1692

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FOREWORD

This is the fifth of a series of reliability assessment reports on the Orbiting Geophysical Observatories. Working under prime contract NAS 5-1692, awarded by the Goddard Space Flight Center of the National Aeronautics and Space Administration, the Planning Research Corporation study team assisted NASA in the overall OGO development program by making independent estimates of OGO spacecraft system reliability, aiding in the establishment of reliability goals, and acting as technical advisor to NASA in OGO reliability matters.

The first reliability assessment was of a preliminary nature, since it was based, in some areas, on designs that were not quite finalized; limited information about the experiments to be serviced by the OGO spacecraft; and broadly defined environmental and electrical stresses. The second assessment updated and refined the work of the first assessment. Specifically, the second assessment sought to be more realistic by eliminating a number of simplifying assumptions made of necessity in the first assessment, bringing launch and POGO effects into the assessment, making individual subsystem assessments more detailed and incorporating latest design changes, revising basic failure rates on the basis of new information, and revising the reliability models to incorporate the greater depth of engineering analysis.

The third assessment further refined and updated the first two assessments. It emphasized increased engineering analysis at the subsystem level, the objective being a complete assessment of all aspects of the spacecraft. To make the assessment more complete and realistic, the mathematical models were revised to include subsystem interface considerations, and applicable data from all OGO spacecraft and subsystem tests conducted during the period were incorporated.

The fourth assessment departed from the previous efforts in two major areas: (1) It went more deeply into the engineering analysis of specific areas to provide methods of improving the reliability of the spacecraft subsystems. (2) It provided a complete reliability analysis

of the OGO radio astronomy experiment and a reliability analysis of the operational aspects of the spacecraft for the EGO mission.

The fifth assessment, reported here, has followed a three-way approach: (1) It has investigated the use of new areas of technology of possible benefit to OGO. (2) A major portion of the work assessed the effects on spacecraft reliability of the changes necessary for the polar orbit; in other words, it was essentially a reliability assessment of the POGO spacecraft. (3) It assessed the reliability status of the OGO A spacecraft.

ABSTRACT

This report presents the findings and Technical Advisement Memoranda (TAM's) of the fifth assessment and the results of additional, smaller efforts that have previously appeared only in progress reports.

Sections I and II provide an introduction and a summary of all TAM's prepared during the assessment period and the additional findings of the period. Section III is concerned with the status of OGO A as a launch-ready vehicle. Section IV describes investigations into the use of new areas of technology of possible benefit to future OGO vehicles. Section V analyzes the effects on spacecraft reliability of the changes necessary for the polar orbit.

I. INTRODUCTION

This document reports upon the fifth of a series of independent reliability assessments of the Orbiting Geophysical Observatories. These assessments are being conducted by Planning Research Corporation for the Goddard Space Flight Center, National Aeronautics and Space Administration.

The first assessment, conducted from 8 October 1961 to 5 February 1962, was, except for the assessment of the Communications and Data Handling (CDH) Subsystem, of a preliminary nature. Study of the design documentation of the CDH Subsystem revealed a high degree of complexity which required more detailed examination, from both modeling and engineering analysis viewpoints, in order to ensure a realistic preliminary assessment.

The second assessment, conducted from 5 February 1962 to 30 September 1962, essentially updated and refined the work of the preliminary assessment. To make the assessment more realistic and practical, a number of simplifying assumptions were eliminated which had been made as a matter of economic and temporal necessity in the first effort. For example, with the receipt of more complete design information, a number of assumptions regarding subsystem part complements were readily discarded. Elimination of other assumptions, however, required considerable detailed engineering analysis at the subsystem level and nontrivial changes in the preliminary assessment models.

The third assessment, 30 September 1962 to 30 April 1963, consisted primarily of increased engineering analysis at the subsystem level and further examination of subsystem interdependence. The subsystem model was developed, and the prior assessments required a modicum of revision. However, to include the subsystem interface considerations, the spacecraft model underwent considerable revision. This third effort provided a complete and realistic assessment of the Orbiting Geophysical Observatories for the EGO mission.

The fourth assessment, 30 April 1963 to 30 March 1964, departed from the previous efforts in two major areas: (1) It went more deeply than previous assessments into the engineering analysis of specific areas in order to try to provide methods of improving the reliability of the spacecraft subsystems, and (2) it provided a complete reliability analysis of the OGO radio astronomy experiment and an analysis and evaluation of the operational aspects of the spacecraft system from a reliability standpoint for the EGO mission.

The fifth and present assessment, 31 January 1964 to 31 August 1964, has, to a certain extent, followed a three-way approach. A portion of the effort was dedicated to investigating new areas of technology of possible benefit to the OGO spacecraft. The second and major portion of the work assessed the effects on the OGO spacecraft reliability of the changes in the subsystems necessary for the polar orbit; this effort, in essence, constitutes a reliability assessment of the POGO spacecraft. The third portion involved establishing the final reliability status of the OGO A spacecraft.

As before, the objectives of this study were established at the outset by NASA and, briefly, are as follows:

1. To provide NASA with objective and independent estimates of OGO spacecraft system reliability
2. To assist NASA in establishing reliability goals for the spacecraft system and major subsystems
3. To act as technical advisor to NASA in OGO reliability matters

These objectives have been carried out informally via conversations with representatives of the NASA OGO project organization and formally via Technical Advisement Memoranda (TAM's) prepared by the PRC assessment team. As with the second assessment report, because this effort has proceeded on such a time-dependent basis, most of the material covered here has already been described in previous TAM's.

With the assistance of NASA WOO representatives, PRC maintained close coordination with the OGO spacecraft development

contractor, Space Technology Laboratories, Inc., during the course of the assessment. Members of the PRC study team relied heavily on spacecraft design documents supplied by NASA and STL (via NASA); however, when documentation provided an incomplete or ambiguous description of some design aspect, consultations were held with the cognizant STL design engineers.

Section II of this report summarizes all the work conducted during preparation of this assessment and lists the major recommendations arising from the study. It also presents some of the work reported in progress reports but not covered in the TAM's themselves. The section summarizes the basis, major findings, and recommendations of each of the study areas undertaken. Conclusions and recommendations of major interest are described in detail in later sections of the report; some detailed conclusions and recommendations of lesser importance, discussed in the later sections, are not summarized in Section II.

The remaining sections of the report cover three major areas. Section III is concerned with the status of OGO A as a launch-ready vehicle. Section IV describes the investigations into the use of new technology of possible benefit to future OGO vehicles. Section V presents the results of the analyses undertaken to determine the effect on the spacecraft reliability of the changes necessary for the polar orbit.

II. SUMMARY AND RECOMMENDATIONS

During the course of the fifth OGO reliability assessment, nine Technical Advisement Memoranda (TAM's) have been prepared by PRC. Four of these were published earlier; five appear here in final form for the first time, although major findings of most of these have been discussed with members of the OGO project organization and much of the work has been covered in previous monthly progress reports. In addition to the TAM's, several smaller efforts have been conducted, which have been reported on either in the progress reports or informally in conversations with members of the OGO project organization. All of the nine TAM's arising out of the efforts of the fifth assessment are published in their entirety in subsequent sections of this report.

A. Summary of TAM's

The contents of the TAM's are as follows:

1. TAM No. 25, "Preliminary Analysis of Part Burn-In Benefits for OGO"

TAM No. 25 discusses the potential worth of a parts burn-in program for OGO. This investigation was initiated as the result of a parts parameter-drift screening (PDS) program proposed for OGO by STL. As alternatives to STL's approach, two burn-in techniques are investigated by PRC, and a simple and inexpensive parameter-drift selection method is outlined. The first burn-in technique investigated, termed "derated burn-in," is that utilized by BTL for the Telstar parts. A significant amount of data arising out of the Telstar program was analyzed, and it is concluded that a burn-in program conducted on a similar basis for OGO parts could be expected to yield a significant reduction in failure rates. The limiting factor, however, is the time required for the procedure, for the burn-in should continue at least 20 weeks.

The second technique investigated is that of burning in parts at a higher stress level than that expected in service. Essentially, this

technique attempts to accelerate the failure-rate reduction potential of the burn-in process. Empirical relationships between the stress and test time required for various percentages of failure in Minuteman-type voltage reference diodes were investigated. It is concluded that burn-in for 80-percent rated junction temperature for 2 weeks is potentially capable of providing a failure-rate reduction for OGO parts of a magnitude similar to that claimed by STL's PDS program. This approach could, of course, be realized at significantly less expense than the BTL method or the STL PDS proposal, and within a minimal time period.

A rudimentary parameter-drift screen was investigated which could be used with either of the two burn-in techniques discussed. This simple screen is easily available because, for either of the burn-in methods, it is necessary to measure the part parameters before and after the burn-in is completed. When either of these is undertaken, then, it is only necessary to plot the frequency histogram function of the parameter changes for each parameter and then eliminate the most unstable of the parts. The elimination criterion is not established and would require a study in more depth than was allowed by the scope of the TAM.

The major recommendations of the TAM are as follows:

a. The derated burn-in could result in significant part failure-rate reductions as large as those claimed for the STL PDS program and at considerably less cost if the burn-in period is at least 20 weeks.

b. Stressed burn-in could result in equivalent part failure-rate reductions and at still lower cost if the parts are burned in at stress levels over 80 percent of rated stress for 2 weeks.

c. Additional benefit may be gained from either burn-in technique at practically no increase in test cost by including a rudimentary parameter-drift screen.

2. TAM No. 26, "Recommendations for a Single Classical Reliability Model for OGO"

A previous PRC TAM[1] compared STL's and PRC's approaches to the classical prediction of OGO spacecraft system and subsystem reliability. TAM No. 26 examines further the differences in modeling approaches, points out inaccuracies where they exist, and makes recommendations concerning the modeling approach PRC believes should be utilized for continuing OGO reliability predictions. The previous TAM, which was a numerical comparison of the results of STL's and PRC's predictive models, is thoroughly reviewed, and the variations in modeling approaches and assumptions that bring about the numerical differences in the predictions are isolated.

It is pointed out that both STL and PRC agree that the five major OGO subsystems split into two classes; the Structure, Thermal Control, and Power Supply Subsystems all have relatively high predicted reliability values, whereas the Attitude Control and Stabilization (ACS) and Communications and Data Handling (CDH) Subsystems have much lower predicted reliability values. Thus, from the standpoint of apportionment of reliability improvement effort, STL and PRC would clearly agree that most of the effort should be devoted to the ACS and CDH Sybsystems. Moreover, STL and PRC would both probably recommend that the Power Supply Subsystem be next in line for reliability improvement effort, although there is a significant difference in the two reliability predictions for the Power Supply Subsystem. For the ACS and CDH Subsystems, although both models result in low predicted reliabilities, the values predicted by STL and PRC are widely variant.

At the OGO system level, STL predicts a 1-year reliability of 0.20, whereas PRC predicts 0.00026--a difference of three orders of magnitude. In order to see the effects of failure rates at the system level, one should note that the use of current STL rates in either model results in

[1] TAM No. 34-18, Comparison of Current STL and PRC OGO Classical Reliability Predictions, 18 November 1963.

approximately a hundredfold increase in predicted system reliability over that using PRC rates. This accounts for two of the three orders of magnitude difference, and, since assignment of failure rates involves a considerable amount of subjective judgment, this difference must be viewed as an "honest" difference in basic failure rates. The remaining order of magnitude, then, must be attributable to modeling differences. Unlike with the subjectively justifiable failure-rate difference, PRC feels that this difference due to modeling is not justifiable and should be resolved. More explicitly, since (1) STL and PRC use the same method of analysis and (2) the same OGO configuration is used, there is no valid reason that an order of magnitude difference in predicted system reliability should exist as a result of modeling differences.

TAM No. 26 thoroughly examines, first for the spacecraft system, and then for each of the major subsystems, the reasons for the differences in the two models and recommends a model or modeling approach that in each case can be universally used with confidence. The TAM concludes that the STL reliability model equations for the OGO spacecraft system and major subsystems are greatly oversimplified in most cases, whereas those derived by PRC take every feasible step to represent the real-life situation faithfully. In addition, it points out that the differences in basic assumptions underlying the models used for the CDH Subsystem are primarily the result of differences about the importance of the various modes of operation. It is felt that GSFC should be the rightful authority in this area.

The major recommendations are as follows:

a. The PRC models or modeling approaches should be used as the basic models in making reliability predictions or allocations and in conducting investigations into design improvement.

b. If the capability for comparison of models is considered necessary, the model differences in the CDH area should be resolved under GSFC guidance.

3. TAM No. 27, "Preliminary Review of OGO S-50 Power Control Unit"

This TAM describes a "system level" review of the OGO S-50 power control unit design and failure-switching provisions, which was conducted to form the basic modeling framework for the detailed reliability assessment of the subsystem design. The TAM discusses areas in which preliminary qualitative analysis indicates that performance and reliability can be improved by subsystem changes in the proposed design. Detailed numerical assessments are not included but are deferred to a later TAM. Subsystem functional operation and the available subsystem failure-switching provisions are described, and changes are recommended in the proposed design, including some circuit changes.

The design approach to the S-50 Power Supply Subsystem is entirely different from that used for the S-49. In addition, the S-50 uses N-on-P solar cells and silver-cadmium batteries instead of P-on-N solar cells and nickel-cadmium batteries, as are used in the S-49. The major elements of the S-50 Power Supply Subsystem can be divided functionally into the following units:

a. The solar array, which provides the basic system power and recharge of the batteries during sunlight periods
b. The batteries, which provide the basic system power during eclipse periods
c. The solar array shunt regulators, which control the solar array output current
d. The charge controls, which sense battery current, temperature, and voltage status to drive the shunt regulators
e. The series regulators, which drop the battery voltage during charge to the voltage required at the load bus
f. The discharge control, which controls the bypassing of the series regulators during discharge

g. The load bus limiter, which reduces the output of one of the "uncontrolled" array sections when the output of both "uncontrolled" sections is greater than the load requirements

h. The cycle relay controls, which control battery charge frequency during extended sunlight periods

i. The current monitor excitation oscillators

j. The capacitor quad, which filters the load bus voltage

The subsystem operates in two distinct modes, as selected from the ground by command, to correspond with the orbit of the spacecraft. Mode I is the "continuous" mode of charging the battery and will generally be used in sunlight-eclipse orbits; Mode II is the "cycle" mode of charging the batteries and will be used in extended sunlight orbits. The available failure-switching provided for in the proposed design is thoroughly discussed, and the resulting deficiencies are pointed out. Major recommendations for design changes to surmount these deficiencies are as follows:

a. The failure-switching provisions should be revised to provide (1) series regulator cross-strapping and elimination of the load bus overvoltage relays, and (2) charge control of both batteries by one cycle relay in the cycle charge mode when the charge buses are cross-strapped.

b. A ground-commanded override of the discharge control relays should be incorporated.

c. The discharge control relays logic should be revised to operate on load bus voltage sensor for both charge and discharge conditions.

The TAM makes additional, detailed recommendations on the improvement of subunit circuit elements.

4. TAM No. 28, "Use of Integrated Circuits for Increased System Reliability"

For some time, PRC has been keeping track of developments in the field of integrated circuits, primarily in the area of reliability, but also taking into account such necessary additional factors as power dissipation, availability, and cost. Due to the low predicted reliability of the present OGO design (primarily as a result of its unusual complexity), PRC feels the potential use of integrated circuitry in the implementation of some of OGO's subsystems should be given detailed consideration. Integrated circuits could provide significant gains in reliability at not too unreasonable a cost. TAM No. 28 describes the more important facts that led PRC to this conclusion.

The TAM first establishes the terminology used in this discussion and then describes the two major areas of technological development in present-day integrated circuit techniques. The first area involves thin-film circuits, which represent a two-dimensional approach to the physical realization of electronic elements. The elements are synthesized in the form of thin films deposited in a patterned relationship on a structural supporting material. The second area involves semiconductor integrated circuits, which embody a three-dimensional approach to the physical realization of electronic components. Here the bulk and junction properties of semiconductor active elements are used to produce transistor-diode functions, and wide-tolerance passive component functions are inseparably associated on or in a continuous body of semiconductor material.

Although volume and weight reductions are important, it is more important that integrated circuit techniques lead to significantly higher reliability and lower cost. Use of systematic production techniques, elimination of assembly operations, and a marked reduction of interconnections (discrete joints) will increase reliability and save costs.

The possible application of integrated circuits to OGO is discussed thoroughly. Three alternative types of integrated circuits may be used: (1) standard circuits, (2) custom circuits, or (3) something in between,

referred to as customized circuits. Standard circuits are off-the-shelf integrated circuits produced to a set of specifications developed by the vendor; custom circuits are produced to the buyer's unique specifications. The customized circuits are designed to a buyer's specifications, which, in turn, are based on a configuration of integrated circuit components already being used by the vendor for either of the other two types of circuits.

Digital circuits and linear circuits must, as is frequently the case in electronics, be considered separately. The most progress has been made in integrated digital circuits, and, because of the large amount of complex digital circuitry aboard OGO, attention has been directed toward this area. Several choices of the particular logic to use are available: direct-coupled transistor logic (DCTL), resistor-transistor logic (RTL), resistor-capacitor-transistor logic (RCTL), transistor-coupled transistor logic (TTL or T^2L), diode-transistor logic (DTL), emitter-coupled transistor logic (ECTL), etc. The TAM includes a table listing typical worst-case operating conditions for some of the logic types. Systematic study generally indicates that none of the logic types is inherently superior; each has its advantages and its disadvantages. With respect to OGO as a specific system (and in view of the preliminary nature of the effort reported here), the factors that must be considered are somewhat simplified. In other words, as an already designed and tested system, OGO is inherently unreliable. PRC feels that integrated circuits offer great promise of improving the reliability. The specific factors considered in reaching this conclusion are thoroughly discussed in the TAM.

The possibility of replacing portions of the OGO circuitry with standard integrated circuits is investigated to the depth allowed by the TAM. The TAM considers such relevant factors as operating frequency, environmental operating characteristics, power dissipation, noise immunity, and fan-out. The results indicate that, at this point, a significant improvement in reliability at a reasonable cost could be achieved through the use of integrated circuitry in portions of OGO.

Of the many apparent advantages of integrated circuitry, really significant increases in achievable reliability may prove to be the greatest.

The reliability data available at the time of writing was thoroughly analyzed and reported in the body of the TAM. From this review of the data, it is concluded that the failure rates of integrated circuits are at least 10 times less than those of similar discrete component circuits. An appropriate average semiconductor integrated-circuit failure rate for preliminary use is 0.15 to 0.2 failures per 10^6 integrated-circuit hours. Major recommendations presented in the TAM are as follows:

a. Use of integrated circuits in some portions of OGO is feasible without necessitating basic logic redesign.

b. Direct substitution of off-the-shelf integrated circuits on a one-to-one basis probably is not possible, but substitution on a basis of two or three standard integrated circuits for one discrete component circuit appears to be feasible.

c. It appears that power consumption will not be a serious problem.

d. Noise susceptibility will require care in design.

e. There is reason to believe that the benefits would outweigh the cost involved.

f. The possibility of significant increases (possibly orders of magnitude) in reliability has been definitely determined to exist.

g. A thorough and detailed analysis of the use of integrated circuits in specific areas of OGO should be carried out as soon as possible.

5. <u>TAM No. 29, "Assessment of the OGO S-50 Power Supply Subsystem"</u>

TAM No. 27 gives functional description and preliminary recommendations applicable to the OGO S-50 Power Supply Subsystem. TAM No. 29 is a quantitative assessment of the reliability of the S-50 Power Supply Subsystem for the POGO orbit. The POGO mission profile is characterized by the alternating periods of eclipse seasons and

sunlight seasons. The Power Supply Subsystem operates in two distinct operational modes corresponding to the two possible seasons. In the eclipse season, the normal mode of Power Supply Subsystem operation is referred to as the continuous charge mode. During the sunlight season, the normal mode of operation is the cycle charge mode. These two modes of operation are necessary so that the batteries will have sufficient power when they are required (eclipse season) and are not overcharged when they are not required (sunlight season).

Reliability of the Power Supply Subsystem is defined as the probability that it will operate successfully in each mode when required and for the length of time required. So that this probability can be numerically evaluated, a specific mission profile is defined, and the assessment of the Power Supply Subsystem proceeds on the basis of this profile.

The approach of this assessment involved a complete failure-effects analysis for all first-order failures, and some second-order failures, occurring in the Power Supply Subsystem. The results of this analysis are thoroughly documented in the exhibits contained in the TAM. In addition, it analyzes the output requirements of the solar array, the depth of discharge of the battery (both for when two batteries are required and for when one battery is required), and the probable output capability of the solar array as it varies with time due to degradation by radiation and other effects of the space environment. These three analyses are included as appendices to the TAM. The reliability of the Power Supply Subsystem was computed both for the case where the batteries are not considered redundant and for the case where they are considered fully redundant. This made it possible to be flexible in determining the point at which the two batteries are no longer sufficient for Power Supply Subsystem operation.

Reliability of the Power Supply Subsystem is presented as a function of time and will be found in Exhibit 11 in the TAM. As concerns the solar array output capability, it is highly improbable that the array can supply the full output required to operate the Power Supply Subsystem successfully for a full year. It is probable, however, that the array can

supply current to operate the spacecraft plus half the experiment load for a year.

In addition to assessing the reliability of the existing Power Supply Subsystem design, the TAM assesses the reliability of the design with various previous recommendations included; i.e., (1) series regulator cross-strapping, (2) revised cycle mode cross-strapping, and (3) ground-commanded discharge control override. TAM No. 29 concludes that the reliability of the Power Supply Subsystem is relatively high but could be significantly improved by including the major changes recommended in TAM No. 27.

6. TAM No. 30, "POGO Experiment Programmer Assessment"

This TAM reviews the proposed design of the POGO experiment programmer and evaluates its implications on the spacecraft and mission reliability. This review includes the experiment programmer itself, the five additional relays required, and converter 10 as a separate entity.

The experiment programmer provides variable duty cycle +28 volts to, at most, five different experiments via latching relays, each of which has been placed in series with the normal power control relay. The purpose of the experiment programmer is to provide the 28 volts to the high-power experiments so that their power consumption can be controlled on a time-share basis.

To arrive at a mathematical model for accurately predicting the reliability, a failure analysis was performed which considered not only the specific effect of a failure but also the overall effect on mission operation. The results of the analysis are tabulated in order of the criticality of failure effects, in Exhibit 3 of the TAM.

To arrive at the data presented in Exhibit 3, single component failures in each circuit element were analyzed to determine if they caused that element to fail true or false. Open input diodes in gates were considered separately, since this causes a different kind of loss by means of a change in the logic output of that gate.

Analysis of the experiment programmer revealed that failure effects could be grouped into five specific categories:

a. Those which cause +28 volts to be continously "on"

b. Those which cause +28 volts to be continuously "off"

c. Those which cause an indeterminate +28 volts to be continuously "on" or "off," depending on state of operation at time of failure

d. Those which cause altered duty cycle(s)

e. Those which have no effect

Examples of each of these types of failures are contained in the TAM. Failures previously classified as causing continuous +28 volts or 0 volts to the experiments, altered duty cycles, and no effect are shown to cause one of three effects upon the mission: (1) abort the mission, (2) cause loss of high-power experiments, or (3) have no effect on the overall mission value. The TAM points out that, in some cases, the use of backup commands may negate the effects of some of the failures, although this method requires considerable computer time.

Numerical assessment of the reliability effects of the experiment programmer on the POGO mission results in the computation of two probabilities: (1) that the entire mission will be lost (programmer providing 28 volts continuously and at least one experiment cannot be switched out), and (2) that all the high-power experiments will be lost. These two probabilities are determined to be 0.106 and 0.353, respectively.

Major recommendations arising out of this analysis are as follows:

a. The command configuration logic duty cycle relations should be studied for optimization from a reliability standpoint.

b. The continuous "on" capability should be changed to "continuous off" command for greater fail-safe capability.

c. The output of the experiment programmer should be instrumented so that its operating state can be readily determined on the ground.

7. TAM No. 31, "Review of Capacitive Tachometers for Attitude Control Reaction Wheels"

The previous OGO ACS Subsystem used a magnetic tachometer to determine the speed of the reaction wheels. This tachometer was a simple device with a reliability approaching 1, but it became a problem because of the magnetic field it created. To reduce the magnetic field, a capacitive tachometer was designed that would achieve the same pulse-train waveform characteristics. The original version of this system incorporated a single variable capacity system consisting of a rectangularly toothed capacitive plate on the stator and a sawtoothed capacitive plate on the rotor. Because of the direct relation between load resistance and output voltage, however, it was necessary to incorporate a buffer amplifier with high input impedance and low output impedance between the tachometer output resistor and the frequency-to-DC converter circuitry that receives the signal. In addition, the original single variable capacitive element tachometer was found to be susceptible to 400 cycles motor drive pickup and to electrostatic charge accumulation on the tachometer capacitor plates. To circumvent these effects, a single capacitor pattern was altered to two symmetrically balanced rotor and stator patterns. The following design necessitates a buffer amplifier consisting of three functions: (1) a high input impedance differential amplifier, (2) a gain stage to provide the pulse level and characteristics required by the frequency-to-DC converter circuitry, (3) an output emitter-follower to feed the low impedance frequency-to-DC converter. It is this buffer amplifier that interjects the inherent reliability degradation brought about by the new tachometer.

Since no low-level redundancy was incorporated into the design of the buffer amplifier, the reliability assessment of the new tachometer system proceeded on a parts count basis. The reliability of the system was computed for a period of 1 year's orbit for the total of the three reaction wheels involved in the ACS Subsystem. The resultant reliability is 0.95.

The major conclusions are as follows:

a. The reliability of the ACS Subsystem is degraded slightly.

b. From a system standpoint this degradation is practically negligible.

8. TAM No. 32, "Effects of Universal Wiring System and Command Receiver Frequency Change on OGO Spacecraft Reliability"

This TAM reviews the design and evaluates the implications on spacecraft and mission reliability of (1) the use of a "universal" wiring system and (2) a command receiver frequency change. The analysis of these two changes is explained fully in the TAM itself.

The TAM concludes that the reliability of the spacecraft is slightly increased with the universal wiring system because the number of connectors involved is reduced, and that the reliability of the command receiver remains unchanged. Thus, essentially, the net effect of these two changes upon the spacecraft system reliability is a slight increase.

9. TAM No. 33, "OGO A Reliability Critique"

This TAM reviews the failure histories of the units integrated into OGO A in order to determine if any have a failure history that would make its potential reliability questionable. OGO failure report and component summaries covering the period from 1 November 1962 to 1 May 1964 were reviewed and all OGO A unit failure reports were extracted. The unit serial numbers appearing on the Spacecraft Integration Log were used as a guide to the OGO A units.

The applicable failure reports were examined for any signs of suspicious failure patterns or repetitive failure patterns without evidence of sufficient corrective action. In addition, a similar earlier effort, previously reported in a progress report, is included in the OGO A reliability critique for completeness.

The TAM concludes that OGO A units have experienced a significant number of failures during the testing programs but that (1) those

which were repetitive have been sufficiently corrected, and (2) the remainder have not seriously degraded the reliability of the units.

B. Additional Work Areas

For completeness, this section describes additional work areas reported on in previous progress reports but not covered in TAM's in the later sections of the report. There are three specific tasks. Two are observations and reviews of tests performed on the OGO spacecraft; the third analyzes the "purple plague" problem in the PT4-7059 transistors.

An additional task was to make preliminary reviews of several proposed OGO design changes. Results of these reviews were reported in conversations with members of the OGO project organization early in the fifth assessment period.

1. Review of OGO Prototype Thermal Vacuum Test

The test procedure was reviewed and the test setup observed just before the OGO prototype thermal vacuum test was initiated. PRC believes that, within the obvious cost constraints, the test procedure and equipment are adequate to describe the spacecraft's capability to operate under space conditions. The simulation equipment is sufficient to adequately simulate the major elements of the space thermal and vacuum conditions, and the instrumentation provided and test procedure followed are sufficient to detect any significant deviations in spacecraft performance.

2. Review of OGO Prototype Spacecraft Torsional Vibration Tests

The performance of the OGO prototype spacecraft torsional vibration tests was observed. The test equipment utilized and the procedure followed were adequate. The instrumentation used was judged to be sufficient to provide the required data. During the tests, there was visual evidence of cross-coupling between solar panel lateral vibration and spacecraft torsional vibration. Solar panel tip deflection at the one visible resonance was estimated at 0.1 to 0.2 inches double amplitude. No visible damage occurred during the test.

3. Investigation of "Purple Plague"

In this connection the following documentation was reviewed:

STL Failure Reports No. 8708.

Fairchild Semiconductor Internal Correspondence to Tom Williams from J. L. Farley, 14 January 1964. Subject: TE-1341, Space Technology Laboratories.

STL IOC 9371.1-277 to J. C. Horvath from L. H. Garner, 23 January 1964. Subject: Failure Report No. 8708 and Purple Plague.

STL IOC 9371.1-292 to J. C. Horvath from L. J. Martire, 4 February 1964. Subject: Laboratory Investigation To Determine Possible Deleterious Effects of Purple Plague.

STL IOC 9371.1-317 to J. C. Horvath from L. H. Garner, 26 February 1964. Subject: Laboratory Evaluation, PT4-7059 and 2N708 Transistors.

Unless further evidence is brought to light, it is concluded that "purple plague" has no detrimental effect on the performance or failure rate of the PT4-7059 transistor. This conclusion is based on two principal factors. (1) Various statistical checks of the data presented in IOC 9371.1-317, including the performance of the signed test for paired observations on the Group V data at V_{BE} = 10 ma , all indicate that no significant difference existed in the parameters of the transistors before and after test. Group V involved the most severe environmental conditioning. (2) The failure which originated the investigation was a collector-base short which is in direct opposition to the type of failure that should be caused by "purple plague" if it were to cause failures. Since its properties include poor electrical conductivity, brittleness, and a coefficient of thermal expansion different from its constituents (gold and aluminum), it would be expected that if any failures were to be related to "purple plague" they would be open bonds rather than collector-base shorts.

TECHNICAL ADVISEMENT MEMORANDUM NO. 34-33

OGO A RELIABILITY CRITIQUE

PRC D-845

31 August 1964

Prepared by

H. Scott Watson

Approved by

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PLANNING RESEARCH CORPORATION
LOS ANGELES, CALIF. WASHINGTON, D.C.

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TECHNICAL ADVISEMENT MEMORANDUM NO. 34-33

To: Assistant OGO Project Manager, GSFC, NASA
From: PRC OGO Reliability Assessment Team
Subject: OGO A Reliability Critique

1. Introduction

This TAM reviews the failure histories of the units integrated into OGO A in order to determine their potential reliability.

The OGO Failure Report and Component Failure Summaries covering the period from 1 November 1962 through 1 May 1964 were reviewed and all OGO A unit failure reports were extracted. The unit serial numbers appearing on the Spacecraft Integration Log (undated) were used as the guide to the OGO A units. The log was, as well as could be determined, current as of about 1 August 1964. The extracted failure reports were then examined for signs of suspicious or repetitive failure patterns for which there had not been sufficient corrective action.

2. OGO A Unit Failures

The complete set of failure summaries is contained in the appendix to this TAM.

There was only one case of a potential problem. Failure Report No. 6907 of 27 January 1964 reported the detection of an open circuit between pins 40 and 41 of 4A18-J2. The result was loss of continuity through the temperature sensor thermistor. Rather than opening the unit and subjecting it to extensive rework, the corrective action taken was to modify the connector on electronics assembly serial No. E4 and then mate it with transport T7 for a spare. However, the Integration Log now indicates transport T7 is on board, and the only concern is to ensure that in a last-minute effort the electronics assembly serial No. E4 and transport T7 are not de-mated for any reason. This should not be a problem since the checkout sequence would pick up the discontinuity.

The ADHA serial No. 5 had experienced failures of triad transformers, but corrective EO's were issued requiring that all transformers be changed to OEO's. This particular unit has exhibited no more transformer failures.

Several unconfirmed failures were reported in different units. However, in all cases, efforts to duplicate the failures proved unsuccessful, and it was believed the failures were caused by test equipment or operator error. In most cases, a logical hypothesis could be found to support this conclusion.

3. Previous Investigation

The May Progress Report[1] contained a summary of a previous PRC investigation of OGO A units. For completeness, it is repeated verbatim here.

> The second area investigated concerned the failure histories of five OGO A units. The units involved were:
>
> P/N 201529 - Command Distribution Unit, S/N 3
>
> P/N 201460 - Wide Band Transmitter, 4 watt, S/N 3 and 4
>
> P/N 201441 - Low-Frequency Timing Assembly, S/N 3
>
> P/N 201140 - Analog Data Handling Assembly, S/N 5 and 10
>
> P/N 200934 - Drive Electronics Assembly, S/N 3[2]
>
> The failure summaries available (through March) were reviewed, and selected failure reports were examined to assess the possible effects of the failure histories experienced by these units. The conclusion reached was that, with three notable exceptions, the failures experienced by these units throughout their lifetime were of a random nature caused primarily by fabrication problems, poor workmanship, and overtesting (primary vibration) due to

[1] Technical Progress Report on a Reliability Study for the Orbiting Geophysical Observatories, for period ending 30 May 1964. PRC C64-2052, dated 9 July 1964.

[2] The Spacecraft Integration Log now indicates that Drive Electronics Assembly S/N 6 is installed in OGO A.

several rework cycles. It is felt that the effects of these prior failures on the reliability of the units is negligible.

The three cases in which the failures were not considered to be random are:

(1) Eight failures of STL P/N PT4-2009 diodes in the LFTA.

(2) Twenty-eight failures of transformer T3 (STL P/N 521500-1) in the ADHA.

(3) Six motor drive magnetic amplifiers (STL P/N PT6-2007) failed in the Drive Electronics Assembly.

In all three cases the cause of the failures was determined and corrective action instituted. In case (1), the problem was due to mishandling of a sensitive microdiode, which resulted in intermittent opens. Assembly procedures were refined, and additional fabrication experience apparently resolved the problem.

Case (2) involved breakage of transformer winding wires adjacent to their pin attach points during thermal cycling. The breaks were ductile tensile breaks, as indicated by the fact that the wire was necked down at the fracture. During manufacture these wires are exposed to thermal stresses when the transformer is encapsulated. The manufacturer started using their most experienced coil winders to reduce the frequency of occurrence of this failure.

The solution to case (3), which was due to inadvertent removal of -20 V bias supply from the unit during test, was accomplished by revising the test instructions, providing a plug-in protective circuit and additional control windings to prevent the magnetic amplifiers from drawing excessive current if the -20 V bias is interrupted. In addition to the fixes implemented, it is pointed out that these failures are not at all likely to slip by test without being detected.

4. General Conclusions

For the most part, the past failures of OGO A units fall into two categories:

a. The failures were repetitive; the cause has been determined, and satisfactory corrective action was instituted early enough so that sufficient testing since then indicates the problem is solved.

b. The failures were random in nature and due to a number of causes, primarily workmanship and fabrication difficulties.

It is felt that the failures exhibited previously by the various OGO A units do not, at this time, represent a threat to the reliability of these units. The number of failures experienced in some cases seems somewhat higher than might have been hoped for; however, from the information available, there is no reason to believe that the reliability of the units has been impaired significantly.

5. SUMMARY

OGO A UNITS HAVE EXPERIENCED A SIGNIFICANT NUMBER OF FAILURES DURING THE TESTING PROGRAMS; HOWEVER:

a. THOSE WHICH WERE REPETITIVE HAVE BEEN SUFFICIENTLY CORRECTED.

b. THE REMAINDER HAVE NOT SERIOUSLY DEGRADED THE RELIABILITY OF THE UNITS.

APPENDIX

FAILURE HISTORY

This listing constitutes a complete history of OGO A unit failures as extracted from the STL Failure Report Summaries for the period 1 November 1962 through 1 May 1964.

FAILURE REPORT SUMMARY, ELECTRONICS DIVISION

	Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
Received for period 23 to date 68 Completed during period 17 to date 55 Reports in process: 13 Period: 1 December 1962 through 1 January 1963 Page 1 of 14 Project: OGO System: Attitude Control	SA Shaft Transducer (F. Koehler)	C200979	3	Major	In continuity check prior to system test, rotor of transducer was found to be open.	Defect verified. Open in rotor winding. Unable to determine definite cause. Suspect mishandling.	Personnel in SA shaft assembly area were orally advised of delicacy of the transducers and requested to exercise utmost caution in handling the units. (12-20-62)		4923(1) (12-13-62)
Received for period 27 to date 455 Completed during period 36 to date 401 Reports in process: 54 Period: 1 September 1963 through 1 October 1963 Page 4 of 17 Project: OGO System: Elect. Integrat.	Wrap-Up, Solar Array (A. Eisenstein)	212674	3	Major	During acceptance bench test (OGO-3A-116), leakage was detected between pins 6, 7, and 35 of 1A2-J3 and 1A2-J11.	Wrap-up slots of solar array found to be breaking through insulation and grounding shield to frame. May have been due to handling or fatigue.	Minor design revision incorporated. Solar array wrap-up slots are now lined with Raychem sleeving material to provide additional protection for wrap-ups. (9-16-63)	Action satisfactory.	4770(1) 9-13-63
Received for period 46 to date 114 Completed during period 19 to date 72 Reports in process: 42 Period: 1 January 1963 through 1 February 1963 Page 2 of 25 Project: OGO System: Attitude Control	Attitude Control Assembly (J. Sherman)	200833-1	3		Attitude control unit exhibited out of tolerance reading on reaction wheel direction telemetry output in post vibration acceptance test. (OGO Flash Failure Report 49.)	No failure of attitude control unit. Erroneous indication of failure by test console due to degraded performance of telemetry output monitoring circuit of tester. (OGO Flash Analysis Report 49.)	None required on attitude control unit. Operation of unit satisfactory after rework and recalibration of tester.		6128(1) (1-28-63)

Note: (1) Report complete.

	Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
Received for period 46 to date 114 Completed during period 19 to date 72 Reports in process: 42 Period: 1 January 1963 through 1 February 1963 Page 20 of 25 Project: OGO System: Comm. and Data Handling (below major assembly level)	Digital Decoder Matrix Pulser Module (R. Bolman)	203231	5-13	-	Same as Failure Report 4757, below.	Same as Failure Report 4757.	Same as Failure Report 4757.	-	4756 (1) (1-15-62)
		203231	2-3-30		Pulse width of module found to be marginally out of tolerance in production test of decoder subassembly P/N 202988, S/N 2-5.	This item not considered a failure as a result of reevaluation of unit requirements and subsequent revision of specification.	A reevaluation of the "execute" pulse width requirement on the digital decoder indicated that the original tolerance allowed was too tight in that satisfactory operation is obtained over a broader range. As a result, the limits on pulse width have been expanded from 325 ± 125 microseconds to 400 ± microseconds. This change is reflected in decoder specification D 13416, Rev. C, dated 1-21-63. Under this expanded tolerance, the performance of this module is acceptable.		4757 (1) (2) (1-15-63)
Received for period 46 to date 114 Completed during period 19 to date 72 Reports in process: 42 Period: 1 January 1963 through 1 February 1963 Page 22 of 25 Project: OGO System: Comm. and Data Handling (below major assembly level)	Digital Decoder Word Command Module	203265-1	3-2		Same as Failure Report 5249, below.	Same as Failure Report 5249.	Same as Failure Report 5249.		5288 (1) (1-9-63)
	Digital Decoder Word Command Module (R. Bolman)	203265-1	2-2-10		Module pulse width excessive in production test of decoder subassembly P/N 202988, S/N 2-2.	This item not considered a failure as a result of reevaluation of unit requirements and subsequent revision of specification.	The tolerance originally allowed for "word command" pulse width was found to be insufficient in a reevaluation of decoder pulse width requirements. Satisfactory operation is obtained over a broader range. As a result, the decoder specification has been revised to change the pulse width requirement from 120 ± 30 microseconds to 130 ± 40 microseconds. (Ref. D 13416, Rev. C, dated 1-21-63). This change brings the readings on this module within tolerance.		5249 (1) (2) (1-8-63)

Notes: (1) Report complete.

(2) Does not pertain to OGO A units: included for completeness.

Received for period 80 to date 232
Completed during period 63 to date 178
Reports in process: 54
Period: 1 March 1963 through 1 May 1963
Page 18 of 40
Project: OGO
System: Comm. and Data Handling

Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
Digital Decoder (R. Bolman)	201506	3	Major	(Failure Report 5568) During thermal-vacuum portion of acceptance test, negative matrix lights were inoperative. (OGO Flash Failure Report 57.) (Failure Report 5573) Failure isolated to logic gate module P/N 203239 S/N 5-1, which developed an internal short causing absence to input to negative matrix pulsers.	The failure was initially attributed to intermittent shorting of two leads within the logic gate module. The module, however, checked good electrically after removal from the decoder. Materials and Processes Section dissected the module but no defects could be found. Cause of trouble indeterminate. The decoder has not exhibited this trouble since replacement of the module. (OGO Flash Analysis Report 57.)	None.	-	5568(1) (3) (2-11-63) 5573(1) (2-11-63)
Digital Decoder Matrix Pulser Module (R. Bolman)	203231	5-28	Major	Pulse width found to be too narrow in production test of decoder assembly P/N 202988, S/N 4.	Unknown. The failed component cannot be located.	See Failure Report 6306, below.		5571(1) (3) (2-6-63)
	203154	2-56	Major	Module (FF-3) displayed no TM2 signal during production test of LFTA S/N 2-2.	Indeterminate. The failed component was lost in transit.	Memo 8100.5-49, dated 5 March 1963, has been released defining proper methods of reporting failures and handling failed hardware. Through use of this procedure, the incidence of misplaced hardware should be minimized.		6306(1) (2) (3) (12-11-62)
Digital Decoder Timing Gate Logic Module (R. Bolman)	203285-1	3-1	Minor	Timing gate logic found to be shorted internally during production test of decoder subassembly P/N 202988, S/N 4.	Analysis by Product Engineering did not reveal any defects. The module, however, was damaged somewhat in dissection. Cause of failure unknown.	None.		4987(1) (3) (1-28-63)

Notes: (1) Report complete.
(2) Does not pertain to OGO A units: included for completeness.
(3) Carryover from last report period.

	Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
Received for period 45 to date 277 Completed during period 64 to date 243 Reports in process: 34 Period: 1 May 1963 through 1 June 1963 Page 10 of 31 Project: OGO System: Comm. and Data Handling	Digital Decoder (R. Bolman)	201506	5	Minor	During thermal-vacuum acceptance, unit marginally out of tolerance in word command tests (delay and pulse width measurements).	Discrepancy in delay measurement could not be repeated. Reading error is suspected. Pulse width discrepancy resulted from not using latest revised test procedure. Pulse width in tolerance per OGO-5A-17, Rev. D. No failure charged to unit.	None required.	-	6840(1) (5-3-63)
Received for period 37 to date 152 Completed during period 43 to date 115 Reports in process: 37 Period: 1 February 1963 through 1 March 1963 Page 30 of 32 Project: OGO System: Comm. and Data Handling (below major assembly level)	Low Frequency Timing Assembly Amplifier Driver Module (T. Galvin)	202202	3-26		In production test of LFTA S/N 2-1, module (AM-1) exhibited short to ground in normal "A" output.	Secondary failure. DDHA chassis wiring error. Output connected to power supply.	None. Wiring corrected and personnel cautioned concerning wiring chassis to print.		6307(1) (2) (11-13-62)
Received for period 45 to date 277 Completed during period 64 to date 243 Reports in process: 34 Period: 1 May 1963 through 1 June 1963 Page 29 of 31 Project: OGO System: Comm. and Data Handling (below major assembly level)	LFTA Logic Gate Module (T. Galvin)	205410	3-1	Major	CR3 and CR4 of module (LG-4) exhibited high forward resistance during production test of LFTA S/N 4. Suspect open weld or broken wire.	Failure attributed to intermittently open CR3 and CR4 diodes (PT4-2009). It appears the diodes were damaged by mishandling. These micro-diodes are extremely sensitive to handling and require utmost care during fabrication to prevent part degradation. Reference IOC 9371.2-8.	See Failure Report 6350.		6343(1) (2) (2-8-62)

Notes: (1) Report complete.

(2) Carryover from last report period.

	Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
Received for period 45 to date 277 Completed during period 64 to date 243 Reports in process: 34 Period: 1 May 1963 through 1 June 1963 Page 30 of 31 Project: OGO System: Comm. and Data Handling (below major assembly level)	LFTA Flip Flop Module (T. Galvin)	203163	3-62	Major	Module (FF-2) D10 signal lost at 60° C during production test of LFTA S/N 4.	See Failure Report 6343, above. In this case, only CR4 was involved.	See Failure Report 6350.	-	6344(1) (3) (2-15-53)
	DDHA Hi Frequency Gate Module (T. Galvin)	203163	2-5	Major	Open detected in module (HG-5) during production test of DDHA S/N 2-3.	Micro-diodes CR2, CR3, CR7 and CR8 (PT4-2009) had leads pulled apart and interconnecting ribbon fractured. Apparent mishandling either during component testing or during assembly. Reference IOC 9371.2-8.	Fabrication problems concerning these diodes stem basically from their sensitivity to handling. Refinement of assembly procedures and experience with these components has minimized these problems. This is evidenced by the fact that no failures of these diodes have been reported since 3-30-63.		6350(1) (2) (3) (2-16-63)
Received for period 80 to date 232 Completed during period 63 to date 178 Reports in process: 54 Period: 1 March 1963 through 1 May 1963 Page 16 of 40 Project: OGO System: Comm. and Data Handling	Command Receiver (R. B. Miller)	201456	3	Major	During thermal vacuum qualification, unit R. F. signal was present with R. F. input reduced to zero. (OGO Flash Failure Report 80.)	Screw which holds transistor clip was the wrong size (too long) and was found to be shorting to the case of Q4. (OGO Flash Analysis Report 80.)	Appropriate fabrication personnel informed of defect and requested to adhere to drawing call-off on clip screws. (4-11-63)	Action satisfactory.	6056(1) (4-8-63)
Received for period 37 to date 152 Completed during period 43 to date 115 Reports in process: 37 Period: 1 February 1963 through 1 March 1963 Page 2 of 32 Project: OGO System: Attitude Control	Sensor Electronics and Logic Assembly (W. Keller)	200932	3	Minor	Unit lost instrumentation for Mode II readout during vibration portion of acceptance test per OGO-4A-02. (OGO Flash Failure Report 52.)	Wire broken at TB 2 due to long run without tie-down and possible excessive flexing during fabrication of the unit. Wire connects to test point and is not required for flight operation. (OGO Flash Analysis Report 52.)	An equipment redesign has been accomplished (Dwg. 202415, E.O. B-1, Dwg. 203885, E.O. B-2, effective S/N 3 and on). Additional cable tie-downs provided.	Action satisfactory	5637(1) (3) (1-31-63)

Notes: (1) Report complete.

(2) Does not pertain to OGO A units; included for completeness.

(3) Carryover from last report period.

	Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
	Analog Data Handling Assembly First Level Gate Module (G. Marsh)	201057-1	5-4	Major	Gates X_3, X_4, X_7, and X_8 open in production test of submultiplexer S/N 4.	See Failure Report 4759, below.	See Failure Report 4759.	See Failure Report 4759.	6111(1) (2-3-63)
	Analog Data Handling Assembly First Level Gate Module (G. Marsh)	201057-1	4-50	Major	Gate X_1, X_2, X_5, and X_6 open intermittently. Production test of submultiplexer S/N 4.	Materials and Processes Section analyzed this failure and three others (see Failure Reports 4992, 4995, and 6111 below). In each case, failure was attributed to a Triad transformer (521500-1) which exhibited one or more defects (poorly soldered junctions, mangled winding and insufficient encapsulation). Three of the remaining 10 transformers from these modules had similar defects. Also, none were identified as to lot or date of manufacture. Failure of a fifth module (see Failure Report 6103 below) was also attributed to a defective transformer, although the component was not dissected.	After a sampling of these transformers from STL bins proved 10 percent defective, a production stop order on these modules was issued (E.O. C-6 Dwg. 201057). Production at Triad was halted and restarted under heavy STL surveillance. Changes instituted include use of soft solder at junctions instead of silver solder, proper date coding, and 100 percent inspection by STL prior to potting. New transformers have been obtained and rework of assemblied modules per E.O. C-7 has begun. (3-14-63) This action also applies to Failure Report 5331, page 18, of this summary.	Action satisfactory for this report. For recurrence control, it is recommended that Corporate Product Assurance (L.K. Lee) review current procurement and inspection procedures and their interfaces with Engineering to assure implementation of engineering specifications.	4759(1) (2) (3) (1-20-63)
Received for period 37 to date 152 Completed during period 43 to date 115 Reports in process: 37 Period: 1 February 1963 through 1 March 1963 Page 26 of 32 Project: OGO System: Comm. and Data Handling (below major assembly level)	Analog Data Handling Assembly First Level Gate Module (G. Marsh)	201057-1	5-16	Major	Module had +DC cross-talk on X_2 during production test of submultiplexer S/N 4.	See Failure Report 4760, below. Unhardened epoxy buildup, in this case, occurred at Q5.	See Failure Report 4760.		4994(1) (3) (1-29-63)

Notes: (1) Report complete.

(2) Does not pertain to OGO A units; included for completeness.

(3) Carryover from last report period.

	Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
		201057-1	4-7	Major	Module out of specification. (+DC crosstalk on gate X_6) during production test of sub-multiplexer P/N 202375-1, S/N 4.	Crosstalk due to electrical leakage path provided by buildup of unhardened epoxy around transistors Q13 and Q15. This apparently occurred in earlier replacement of these transistors at WEMS. Epoxy was improperly mixed or cured.	None. These modules are no longer manufactured by WEMS. WEMS, however, was notified of the discrepancy. STL potting-room personnel are indoctrinated as to critical nature of epoxy mixing and curing requirements.	-	4760(1) (2) (3) (1-22-63)
Received for period 80 to date 232 Completed during period 63 to date 178 Reports in process: 54 Period: 1 March 1963 through 1 May 1963 Page 35 of 40 Project: OGO System: Comm. and Data Handling (below major assembly level)	Analog Data Handling Assembly First Level Gate Module (G. Marsh)	201057-1	5-32	Major	Gate X_1 intermittently open in production test of sub-multiplexer S/N 4.	Under investigation.	-		4991(3) (1-20-63)
		201057-1	5-44	Major	(Same as Failure Report 4991, above, except X_7 checks open.)	Analysis by Materials and Processes revealed no defects. It was reported that R14 (PT4-7-C3481F) was intermittent when moved. This could not be verified. Dissection revealed that R14 used a conductive adhesive containing silver to attach the component leads to the body. Reference IOC 9371.2-27.	Although the failure could not be duplicated, the STL standard for this type of resistor is being revised to eliminate the conductive adhesive method of component lead attachment. The crimped-on end cap method, which is considered more reliable, is being adopted. Reference IOC 9371.2-27.		5693(1) (1-22-63)
Received for period 45 to date 277 Completed during period 64 to date 243 Reports in process: 34 Period: 1 May 1963 through 1 June 1963 Page 24 of 31 Project: OGO System: Comm. and Data Handling (below major assembly level)	Analog Data Handling Assembly First Level Gate Module (G. Marsh)	201057-1	5-32	Major	Gate X_1 intermittently open in production test of submultiplexer S/N 4.	Transformer T1 (Triad, STL P/N 521500) found to have open primary.	As a result of continued workmanship deficiencies with Triad transformers, these components will no longer be used in production. Transformers manufactured by OECO to STL P/N 521500-1 have been procured and are being installed. Reference IOC 8100.1-814.	Action satisfactory pending subsequent testing.	4991(1) (2) (3) (1-20-63)

Notes: (1) Report complete.

(2) Does not pertain to OGO A units; included for completeness.

(3) Carryover from last report period.

	Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
	Analog Data Handling Assembly Reference Module (G. Marsh)	201588	5-2	Major	Module output out of tolerance in production test of A/D converter S/N 5.	Diode CR401 (PT4-2006) zener voltage varies beyond limits of specification with temperature. Failure detected during initial thermal cycling tests.	Since the part is controlled by STL specifications and procurement is made from approved vendors, no corrective action will be taken at this time. Should failure mode recur, additional part studies will be required.	-	5386(1) (2) (3-27-63)
Received for period 18 to date 604 Completed during period 15 to date 583 Reports in process: 21 Period: 1 April 1964 through 1 May 1964 Page 9 of 12 Project: OGO System: Comm. and Data Handling	Analog Data Handling Assembly (G. Marsh)	201140	5	Major	Unit exhibited incorrect telemetry output on word 521 during system tests on S-49 Spacecraft. Indication was 016. Should be 0 ± 1.	Extensive testing of the ADHA at room temperature, +5° C and +35° C did not reproduce the defect. Cause of original indication unknown.	-		7731(1) (4-4-64)
Received for period 45 to date 277 Completed during period 64 to date 243 Reports in process: 34 Period: 1 May 1963 through 1 June 1963 Page 13 of 31 Project: OGO System: Comm. and Data Handling	Transmitter, 4W (E. B. Stewart)	201460	4	Minor	In test prior to thermal-vacuum acceptance, transmitter exhibited no output. (OGO Flash Failure Report 112.)	Transistor Q8 shorted. This was a secondary failure which resulted from a test connector working loose from a test fixture filter box which, in turn, permitted the transistor to operate unloaded. No failure charged to unit. (OGO Flash Analysis Report 112.)	The test fixture filter box circuitry has been modified to prevent inadvertent unloading of transistors. (6-5-63)	Action satisfactory.	7066(1) (5-31-63)
Received for period 47 to date 394 Completed during period 47 to date 290 Reports in process: 34 Period: 1 June 1963 through 1 July 1963 Page 11 of 27 Project: OGO System: Comm. and Data Handling	Transmitter, 4W (E. B. Stewart)	201460	3	Minor	During transition from high to low temperature (thermal-vacuum acceptance), output dropped to 1.6W Power returned to 4W after 15 minutes at low temperature.	Repeated functional tests could not duplicate the trouble. Unit was resubmitted to thermal-vacuum environment and successfully passed the test. Suspect indication may have been caused by chamber wiring. No failure charged to transmitter.			7068(1) (6-1-63)

Notes: (1) Report complete.
(2) Carryover from last report period.

	Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
Received for period 39 to date 363 Completed during period 30 to date 319 Reports in process: 44 Period: 1 July 1963 through 1 August 1963 Page 10 of 24 Project: OGO System: Comm. and Data Handling	Special-Purpose Telemetry (R. Eastman)	202650	5	Major	Unit exhibited no regulation and distortion at all frequencies during thermal-vacuum portion of acceptance test. (OGO Flash Failure Report 135.)	Analysis revealed that the weld at the ground lead to C7 on board assembly P/N 204598 was intermittently open. No evidence of pulse mark. Workmanship item. (OGO Flash Analysis Report 135.)	As part of a policy of continuous improvement of welding quality, the failure was reviewed with weld line and weld inspection personnel (OGO Flash Analysis Report 135.)	-	7083(1) (7-8-63)
Received for period 21 to date 477 Completed during period 44 to date 445 Reports in process: 32 Period: 1 October 1963 through 1 November 1963 Page 10 of 17 Project: OGO System: Comm. and Data Handling	Special-Purpose Telemetry (R. Eastman)	202650	5	Minor	During preenvironmental acceptance bench test, unit drew 19.1 ma with 42V input. Requirement is not more than 19.0 ma. (OGO Flash Failure Report 156.)	Current marginally out of tolerance. Reading was within measurement accuracy (5 percent). Extensive testing produced no further degradation and NCMR was dispositioned "use as is."	None. Overall unit operation considered satisfactory. PCR in process to permit up to 20 ma for this unit.		6426(1) (10-25-63)
Received for period 65 to date 428 Completed during period 48 to date 365 Reports in process: 63 Period: 1 August 1963 through 1 September 1963 Page 3 of 25 Project: OGO System: Attitude Control	Sun Sensor Assembly (P. Hutchings)	202384 (RTT) 202744 (-X)	5	Minor	See Failure Report 6643, below.	See Failure Report 6643.	See Failure Report 6643.		6251(1) (8-12-63)
		202384 (RTT) 202744 (-X)	4	Minor	Heat sink and mounting plate stabilization temperatures checked low during thermal-vacuum portion of acceptance test.	Studies on the OGO sun sensors have indicated that the stabilization temperature tolerance was not wide enough to permit sufficient adjustment by application of aluminized mylar tape to bring the intensity voltage up to the required 0.78 or greater. Sun sensors S/N 4 and 5 (see Failure Report 6251, below) had been adjusted prior to the thermal-vacuum test to attain the required intensity voltage.	Revision G of Test Procedure OGO-4A-06, released approximately 9-4-63, modifies the heat sink stabilization temperature tolerance from 100 = 15° F to 100 = 30° F, and the mounting plate tolerance from 130 = 15° F to 120 = 30° F. This change permits the proper intensity voltage to be attained but does not adversely affect the other electrical characteristics of the sun sensor.		6643(1) (2) (8-22-63)

Notes: (1) Report complete.

(2) Does not pertain to OGO A units; included for completeness.

	Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
						These items are not considered failures. The test procedure revision altering the stabilization temperature tolerance had not been released at the time of test. Reference IOC's 9354.3-49 and 9354.3-64.			
Received for period 65 to date 428 Completed during period 48 to date 365 Reports in process: 63 Period: 1 August 1963 through 1 September 1963 Page 16 of 25 Project: OGO System: Comm. and Data Handling	Signal Conditioner (H. Freeman)	201738	5	Minor	Capacitor C7 of Z2 module appeared to be shorted during setup phase of preenvironmental magnetic properties acceptance test. (OGO Flash Failure Report 119.)	Investigation revealed that this defect and that reported on Failure Report 7087, below, in each case resulted from an operator error in the use of an impedance bridge, which caused the capacitors to be overstressed. These defects, therefore, are not directly charged to the units. (OGO Flash Analysis Report 119.)	Test personnel cautioned orally concerning the strict adherence to written procedure required during use of impedance bridge. Warning sticker placed on bridge case to alert personnel that bridge must be in full capacitance configuration when capacity test is made. (8-30-63)	Action satisfactory.	6022(1) (2) (6-14-63)
	Digital Data Handling Assembly Buffer Analog Data Module (T. Galvin)	202582	6-1	Major	Bit 4 at 5F0261 would not get through to output at 5F0264 in lab bench test of DDHA S/N 7.	Output circuit open. Cause could not be specifically determined, since the module was damaged in removal and could not be properly checked.			7053(1) (2) (6-5-63)
Received for period 21 to date 477 Completed during period 44 to date 445 Reports in process: 32 Period: 1 October 1963 through 1 November 1963 Page 12 of 17 Project: OGO System: Comm. and Data Handling (below major assembly level)	Digital Data Handling Assembly Logical Inverter Module (T. Galvin)	202197	6-13	Major	Output on pin 50 intermittent at 63° C in production test of board number 2, P/N 205867, S/N 6.	Analysis revealed that transistor Q21 (PT4-7059, Fairchild) was shorted collector to emitter and partially shorted collector to base. Examination of the part indicated that this was probably a secondary failure caused by a test or wiring error or poor welding technique which applied a reverse bias high voltage resulting in a secondary breakdown. Reference IOC 9371.2-265.	See Failure Report 3100, below.		7882(1) (2) (6-24-63)

Notes: (1) Report complete.

(2) Carryover from last report period.

	Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
Received for period 21 to date 477 Completed during period 44 to date 445 Reports in process: 32 Period: 1 October 1963 through 1 November 1963 Page 3 of 17 Project: OGO System: Attitude Control	Sensor Electronics and Logic Assembly (W. Keller)	200932	5	Major	(Failure Report 3100) Unit would not command to mode 2C during thermal vacuum acceptance test. (OGO Flash Failure Report 147) (Failure Report 6675) Failure isolated to relay driver module Number 1 (Z 29) P/N 203708, S/N 5. Module exhibited intermittent open condition between pins 6 and 7.	Relay driver module was found to have an intermittently open weld at the ribbon to pin 6. The module was removed, the joint re-welded, and the module reinstalled. The SELA then passed the repeat environmental acceptance test cycle with no other failures. Workmanship item.	A general review of fabrication and inspection standards and procedures is presently being conducted by the Reliability Staff. Due to the long-term nature of the investigation, specific reports concerning workmanship defects will be closed and final corrective actions summarized at a later date.	-	3100(1) (2) (3) (8-30-63) 6675(1) (2) (3) (9-6-63)
Received for period 27 to date 455 Completed during period 36 to date 401 Reports in process: 54 Period: 1 September 1963 through 1 October 1963 Page 16 of 17 Project: OGO System: Comm. and Data Handling (qual./accept. test failures at vendor's facilities)	Tape Recorder Transport (W. R. Ryan)	C207464	T3	Major	Unit exhibited inoperative write motor in post-vibration acceptance bench test at RCA.	Investigation revealed that the motor mounting bracket screws had been torqued excessively, which distorted the case of the motor and caused the rotor to bind.	Procedure concerning torque requirements clarified and all flight units rechecked.		149(1) (3) (8-29-63)
Received for period 30 to date 543 Completed during period 28 to date 504 Reports in process: 39 Period: 1 December 1963 through 1 February 1964 Page 10 of 13 Project: OGO System: Comm. and Data Handling (qual./accept. test failures at vendor's facilities)	Tape Recorder Transport (W. R. Ryan)	C207464	T7	Major	Same as Failure Report 5930, below	See Failure Report 5930.	See Failure Report 5930.	Action satisfactory.	161(1) (3) (11-7-63)
		C207464	T7	Major	Unit failed leak check during acceptance test at RCA. (OGO Flash Failure Report 159.)	Excessive leakage at connectors J1 and J2. As a result of this failure and those noted on Flash Failure Reports 158, 160, 161, and 167, an intensive investigation by RCA, assisted by STL, revealed that the basic cause of the leakage problem with connectors was improper preparation of the mating surfaces prior to application of the sealant (MOCA-100).	Action instituted by RCA includes more stringent inspection during surface preparation, retaining of appropriate manufacturing personnel, and proper resealing of failed items per RCA Process Specification MEP 05-1598-1. (11-20-63)	Action satisfactory.	5930(1) (2) (3) (10-31-63)

Notes: (1) Report complete.

(2) Does not pertain to OGO A units; included for completeness.

(3) Carryover from last report period.

	Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
Received for period 23 to date 585 Completed during period 33 to date 568 Reports in process: 17 Period: 1 March 1964 through 1 April 1964 Page 10 of 16 Project: OGO System: Comm. and Data Handling	Tape Recorder Transport (W. R. Ryan)	C207464	T7	Major	During checkout on Spacecraft S-49, unit exhibited an open circuit between pins 40 and 41 of 4A18-J2. Should show continuity through temperature sensor thermistor.	Investigation indicated thermistor was wired to the wrong pins on the internal side of the noted connector. Vendor quality control item.	Vendor (RCA) contacted but no other unit was found to have this defect. This defect will not be repaired, since such a repair would require opening the unit and possibly extensive rework of the unit as a result of the repair itself. (The defect noted on Failure Report 7742, below, is repairable without opening the transport.) Instead, electronics assembly S/N E4 will be modified at the connector to provide required thermistor operation. E4 and transport T7 will then be mated and used as a spare tape recorder system.	-	6907(1) (2) (1-27-64)
	Tape Recorder Transport (W. R. Ryan)	C207464	T7	Major	Spacecraft telemetry indicated unit had low internal gas pressure during S-49 Spacecraft thermal-vacuum test. (OGO Flash Failure Report 181.)	After several days of exposure to thermal-vacuum, leakage began around the connectors apparently due to the opening of minute bubbles in the sealing epoxy. The leakage continued at various rates for a period of about 36 hours, at which time the leakage stopped completely. Vendor quality control item. (OGO Flash Analysis Report 181.)	Rework accomplished by stripping away the externally applied sealant and resealing the connectors with MOCA-100. The vendor's inspection personnel have been instructed to ascertain that the sealant is as bubble-free as possible. Retest after rework was satisfactory.		7742(1) (2) (2-24-64)

Notes: (1) Report complete.
(2) Carryover from last report period.

	Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
Received for period 23 to date 585 Completed during period 33 to date 568 Reports in process: 17 Period: 1 March 1964 through 1 April 1964 Page 6 of 16 Project: OGO System: Elect. Integrat.	Command Distribution Unit (W. McMinimy)	201529	3	Critical	(Failure Report 7745) Relay driver module appeared to be inoperative during S-49 Spacecraft thermal-vacuum test. (OGO Flash Failure Report 132.) (Failure Report 8615) Relay driver module, P/N 201799, S/N 3 replaced for failure analysis.	Module failure verified by Materials and Processes Section. Reference IOC 9371.2-453. A defective weld (leaner) was found at R1. The weld became intermittently open at high temperature resulting in no CDU command capability. Workmanship defect. Reference IOC 8100.1-1093 from P.W. Woodson to Distribution, dated 12-16-63.	Action presently being taken in the area of welding consists of revision of operator training program, replacement of magnifiers with binocular microscopics, and studies to determine whether to update or replace present equipment.	-	7745(1) (2) (2-25-64) 8615(1) (3-9-64)
Received for period 18 to date 604 Completed during period 15 to date 583 Reports in process: 21 Period: 1 April 1964 through 1 May 1964 Page 6 of 12 Project: OGO System: Elect. Integrat.	Command Distribution Unit (J. Sharp)	201529	3	Major	Bit rate appeared to be intermittent during checkout of unit on S-49 Spacecraft.	Extensive testing of unit on the bench and during temperature cycling could not reproduce the defect. Cause of original indication unknown. This unit is now a flight backup to CDU S/N 5 on S-49.			9065(1) (4-1-64)
Received for period 18 to date 604 Completed during period 15 to date 583 Reports in process: 21 Period: 1 April 1964 through 1 May 1964 Page 3 of 12 Project: OGO System: Attitude Control	Pneumatics Assembly Pressure Regulator and Relief Valve (B. Crouse)	PT2-3004	3	Minor	During qualification revibration, pressure regulator exhibited excessive internal leakage. (OGO Flash Failure Report 177.)	Investigation revealed that the excess leakage was due to a damaged valve seat which was probably caused by the high amplitude pulse or jolt imposed on the unit by the shaker during equalization of the shaker immediately after the sinusoidal sweep. At that time the unit was being serviced and the unit engineer indicates that the ball check was probably not seated. Leakage rate was in tolerance just prior to the severe pulse but a recheck right	This unit has previously passed the complete qualification test successfully and was being requalified due to introduction of a new orifice size. Regulator S/N 8, with the design change incorporated, has since passed the complete qualification test successfully.		6680(1) (2) (2-10-64)

Notes: (1) Report complete.

(2) Carryover from last report period.

Assembly Name and Responsible Engineer	Part Number	Serial Number	Severity	Description of Failure	Cause of Failure	Corrective Action (Other Than Repair or Replace Failed Item) and Effectivity	Recommended Corrective Action and Action Agency	Failure Report Number
					after the incident revealed the out-of-tolerance condition. This defect is therefore attributed to faulty test equipments. (OGO Flash Analysis Report 177.)			
Junction Box, OPEP End (3A7) (A. Eisenstein)	213078	3	Major	Pins 8 and 9 of J-23 appeared to be shorted to ground during integration of unit into Spacecraft S-50.	Several screws found to be cutting through insulation of two wires in adjacent bundle. Excessive screw length.	E.O. B5 to Drawing 213078 released specifying shorter screws in the questionable areas to prevent recurrence.	Action satisfactory.	9828[1] (4-13-64)

Note: (1) Report complete.

TECHNICAL ADVISEMENT MEMORANDUM NO. 34-25

PRELIMINARY ANALYSIS OF PART BURN-IN BENEFITS FOR OGO

PRC D-743

21 February 1964

Prepared by

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PLANNING RESEARCH CORPORATION

LOS ANGELES, CALIF. WASHINGTON, D.C.

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TECHNICAL ADVISEMENT MEMORANDUM NO. 34-25

To: Assistant OGO Project Manager, GSFC, NASA

From: PRC OGO Assessment Team

Subject: Preliminary Analysis of Part Burn-In Benefits for OGO

1. Introduction

This effort was undertaken in order to provide timely assistance in determining the potential worth of a parts burn-in program for OGO. Two burn-in techniques were investigated, and a preliminary estimate of the potential benefits of each to the OGO program is presented.

In addition, a very simple and inexpensive parameter-drift selection method is outlined which is felt to be of significant potential value to OGO if either of the burn-in techniques discussed is utilized.

Due to the limited time available, this investigation was restricted primarily to semiconductor devices.

2. Derated Burn-In

The first burn-in technique investigated was that utilized by BTL for the Telstar parts. It must be understood that the complete part selection program invoked by BTL for Telstar was much more complex than that particular facet herein termed "derated burn-in." The complete selection program entailed first subjecting the parts to mechanical inspection and quality control tests, during which approximately 3 percent were rejected, and then performing "life tests and selection." The "life tests" consisted of placing the devices in operation at circuit (approximately 10 percent of rated for Telstar) and temperature conditions similar to those expected in actual performance. The tests were conducted for periods of 2 to 20 weeks, with the average duration being 15 weeks. Parameter limits were determined for the parts such that a parameter reading outside these limits was considered a failure (as well as catastrophic failures, of course). These parameter limits were fairly tight due to the circuit applications of some of the parts.

In addition to the burn-in or "life test," the parts were screened for parameter drift as discussed in TAM 34-24. Discussion of burn-in techniques herein is limited to the burn-in test and the catastrophic and out-of-limits failures.

Exhibit 1 presents the results for 29,644 transistors and 28,525 diodes subjected to the described testing for the Telstar program. The results of Exhibit 1 indicate that a burn-in program conducted on a similar basis for OGO parts could be expected to yield a reduction in failure rate similar to the reduction factors of from 2 to 18 claimed for the PDS program, and at considerably less cost. The limiting factor, however, is the time required for the procedure. The burn-in should continue for at least 20 weeks, especially since transistors apparently experience a significantly higher reduction at some point between 10 and 20 weeks.

It should be remembered that the parts actually used in Telstar were only those passing both rigorous parameter-drift analyses and the "life test," during which approximately 60 percent of the parts were eliminated. Also, it is felt that the failure-rate reductions may be somewhat smaller than those appearing in Exhibit 1, since OGO parts are procured to relatively tight specifications.

3. Stressed Burn-In

The second technique investigated was that of burning in parts at higher stress levels than those expected in service. This technique is an attempt to achieve acceleration of the failure-rate reduction potential of the burn-in principle. It is well to emphasize that the relationships utilized and the conclusions drawn in this discussion are not based on an impressive mass of data. It is felt, however, that the relationships are essentially valid and that the conclusions are sufficiently accurate to indicate order-of-magnitude effects.

H. T. Go[1] has derived empirical relationships between the stress (current) and test time required for various percentages of failure in Minuteman-type voltage reference diodes. These relationships are

[1] "Accelerated Life Testing," Proceedings of the 10th National Symposium on Reliability and Quality Control in Electronics, January 1964.

EXHIBIT 1 - BURN-IN DURATION

Duration	Failure Rate Per 10^6 Part Hours	
	Transistors	Diodes
1 week	150	4.5
2 weeks	100	3.0
5 weeks	7.0	1.0
10 weeks	4.0	0.4
20 weeks	0.8	0.1

	Failure-Rate Reduction (Percent of 1-Week Failure Rate)	
	Transistors	Diodes
2 weeks	0.67	0.67
5 weeks	0.47	0.22
10 weeks	0.27	0.09
20 weeks	0.05	0.03

	Reduction Factor (Times Reduced From 1-Week Failure Rate)	
	Transistors	Diodes
2 weeks	1.5	1.5
5 weeks	2.1	4.6
10 weeks	3.7	11.2
20 weeks	20.0	32.2

utilized for all the computations involved in analyzing the possible benefits of this technique.

The data presented by Go included 2-percent and 5-percent failure plots of stress versus time. In order to allow a direct comparison of this technique with the derated burn-in, a plot of 1.25-percent failure (approximate Telstar experience) was extrapolated from the 2-percent and 5-percent plots.

Since GSFC is proposing a burn-in based on consideration of the rated junction temperatures of the devices, power ratios were utilized in this analysis because they are sufficiently linearly related to temperature for the purpose. This is based on the fact that the devices will be tested in controlled hot environments, and the heat lost to ambient will be slight and depend very little on the junction temperature. Therefore, since Power = I^2R for these devices, the ratio of test current to rated current can be expressed as

$$\frac{\text{I, use}}{\text{I, rated}} = \sqrt{\frac{\text{Power, use}}{\text{Power, rated}}}$$

and, for the Telstar parts,

$$\text{I ratio} = \sqrt{0.1} = 0.316 \ .$$

For OGO parts burned in at 80 percent of rated junction temperature,

$$\text{I ratio} \cong \sqrt{0.8} = 0.895 \ .$$

Assuming an 80-ma. rated current for both devices,

$$\text{I, test (Telstar)} = 25.3 \text{ ma.}$$

and

$$\text{I, test (OGO)} = 71.6 \text{ ma.}$$

Returning to the 1.25-percent failure plot of current stress versus test time mentioned previously, the burn-in time required to accumulate 1.25-percent failure is

$$\text{Telstar parts (25.3 ma.)} = 2.6 \times 10^3 \text{ hours or 15.5 weeks}$$

$$\text{OGO parts (71.6 ma.)} = 1.7 \times 10^2 \text{ hours or 1.01 weeks}$$

and the test time acceleration factor is

$$\text{Time acceleration factor} = \frac{2.6 \times 10^3}{1.7 \times 10^2} = 15.3 \quad .$$

The 15.5 weeks' burn-in time indicated for Telstar parts is essentially equivalent to the 15-week average time on test reported for the Telstar program, and therefore provides a substantial check on the accuracy and applicability of the method used.

It may be inferred, then, that the burn-in proposed by GSFC at 80-percent rated junction temperature for 2 weeks is potentially capable of providing a failure-rate reduction for OGO parts of a magnitude similar to that claimed for the PDS program. The GSFC approach could, of course, be realized at significantly less expense and within a minimal time period. It is to be emphasized, however, that the estimates made herein are very rough and no guarantee can be made that failure-rate reductions of this degree actually will be realized.

4. Rudimentary Parameter-Drift Screen

If one of the two burn-in techniques discussed is applied to OGO parts, a very simple parameter-drift screen which may be of significant benefit can be included at practically no increase in testing cost. Cost of additional parts required, however, may be nonnegligible.

With either of the burn-in techniques, it is necessary to measure the device's parameters both prior to and after completing the burn-in period in order to eliminate those that are failed either catastrophically or out of tolerance limits. Since this is the case, two points are available from which parameter drift occurring during the burn-in can be determined.

The proposed technique consists of plotting the frequency histogram function of the parameter changes for each parameter and then eliminating the most unstable of the parts. The elimination criterion can be established in any number of ways, and should be determined by an analysis of more depth than is allowable here.

One method of establishing this criterion, however, would be to eliminate the same percentage of parts as was screened out due to each of the same critical parameters in the Telstar programs. If this criterion were established, it could be stated that the expected reduction in failure rate would differ from that achieved by the Telstar parameter-drift screening program only by that percentage of parts which displays nonmonotonic parameter drifts. It can generally be expected that the percentage displaying nonmonotonic drifts would be low. This method, of course, would require a significant expenditure for additional parts.

From the foregoing, it is obvious that more serious study should be given to the screening criterion before the criterion could be selected with high confidence in its applicability.

5. SUMMARY

THE PURPOSE OF THIS TAM IS TO DISCUSS METHODS OF, AND POTENTIAL BENEFITS FROM, BURN-IN OF OGO SEMICONDUCTORS. TWO BURN-IN TECHNIQUES ARE DISCUSSED.

a. THE DERATED BURN-IN (I.E., PARTS ARE BURNED IN AT EXPECTED OPERATING CONDITIONS) COULD RESULT IN PART-FAILURE-RATE REDUCTION AS LARGE AS THE FACTORS OF 2 TO 18 CLAIMED FOR THE STL PDS PROGRAM AT CONSIDERABLY LESS COST IF THE BURN-IN PERIOD IS AT LEAST 20 WEEKS.

b. THE STRESSED BURN-IN (I.E., PARTS ARE BURNED IN AT HIGHER-THAN-EXPECTED STRESS CONDITIONS) COULD RESULT IN EQUIVALENT PART-FAILURE-RATE REDUCTIONS, AND AT STILL LOWER COST, IF THE PARTS ARE BURNED IN AT STRESS LEVELS OF 80 PERCENT OF RATED STRESS FOR 2 WEEKS, AS PROPOSED BY GSFC.

c. ADDITIONAL BENEFIT MAY BE GAINED FROM EITHER BURN-IN TECHNIQUE AT PRACTICALLY NO INCREASE IN TEST COST BY INCLUDING A RUDIMENTARY PARAMETER-DRIFT SCREEN (RPDS) AS PROPOSED IN THIS TAM.

d. AN ANALYSIS IN GREATER DEPTH THAN WAS ALLOWED HEREIN IS NECESSARY TO ESTABLISH THE SCREENING CRITERION FOR THE PROPOSED RPDS IF IT IS TO BE UTILIZED.

TECHNICAL ADVISEMENT MEMORANDUM NO. 34-26

RECOMMENDATIONS FOR A SINGLE CLASSICAL RELIABILITY MODEL FOR OGO

PRC D-764

15 May 1964

Prepared by

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TECHNICAL ADVISEMENT MEMORANDUM NO. 34-26

To: Assistant OGO Project Manager, GSFC, NASA

From: PRC OGO Reliability Assessment Team

Subject: Recommendations for a Single Classical Reliability Model for OGO

1. Introduction

The purpose of a recent PRC TAM (Reference 1) was to compare STL's and PRC's approaches to the classical prediction of OGO spacecraft system and subsystem reliability. Hopefully, GSFC can use the recent predictions made independently by STL and PRC (cf. References 2 and 3) to assess where the OGO development stands, reliability-wise, and to identify which OGO equipment should receive the greatest effort toward reliability improvement. More explicitly, in areas where the two predictions agree, GSFC can feel safe in taking whatever action is indicated. For example, if both predictions indicate that a given subsystem's reliability is approximately the same high value, GSFC can safely place reliability improvement effort elsewhere in the spacecraft. But, when the two predictions do not agree, even approximately, GSFC understandably has difficulty in deciding which more accurately predicts current reliability and, consequently, must use considerable guesswork in determining where effort should be placed in seeking reliability improvement.

So that the reader can better appreciate the magnitude of the differences between the STL and PRC reliability predictions, Exhibit 22 of Reference 1 is presented on the following page. The reliability values given in the exhibit represent the predicted reliability for a one-year OGO mission. Note also that one of the exhibit's purposes is to allow rapid examination of the effect of using various failure rates[1] in each of the two classical reliability models.

[1] PDS failure rates are those predicted by STL to result from the application of parameter-drift screening (PDS) to component parts.

EXHIBIT 22 - OGO SYSTEM AND SUBSYSTEM RELIABILITIES USING STL AND PRC MODELS AND STL, PRC, AND PDS FAILURE RATES

	Classical Reliability Estimates					
	STL Model			PRC Model		
	STL Failure Rates	PRC Failure Rates	PDS Failure Rates	STL Failure Rates	PRC Failure Rates	PDS Failure Rates
Structure	0.987	0.982	0.987	0.9897	0.982	0.9900
Thermal Control	0.983	0.849	0.983	0.9995	0.944	0.9995
Power Supply	0.915	0.879	0.936	0.7721	0.686	0.8470
Attitude Control and Stabilization	0.606	0.104	0.744	0.2008	0.0224	0.5883
Communications and Data Handling	0.373	0.035	0.919	0.2033	0.0203	0.7886
Digital Command (PRC only)	(1)	(1)	(1)	0.7834	0.3912	0.9605
Spacecraft System	0.20	0.00267	0.62	0.0316	0.000258	0.3925

Note: (1) Included in CDH model.

It is immediately evident from the exhibit that both STL and PRC find that the five major OGO subsystems split into two classes, each defined by a range of predicted reliability values. That is, the Structure, Thermal Control, and Power Supply Subsystems all have relatively high predicted reliability values, whereas the ACS and CDH Subsystems have much lower predicted reliability values. From the standpoint of apportionment of reliability improvement effort, then, it is clear that STL and PRC would agree that the major portion of such effort should be devoted to the ACS and CDH Subsystems. Moreover, it is likely that both STL and PRC would recommend that the Power Supply Subsystem be next in line for reliability improvement effort. Indeed, in view of GSFC's one-year spacecraft reliability goal of 0.7 and the PRC prediction of 0.686 for the Power Supply Subsystem, PRC unquestionably recommends[1] application of a significant portion of the total reliability improvement effort to the Power Supply Subsystem, whereas, in view of the 0.915 value predicted by STL, it is conceivable that STL might recommend that all of the reliability improvement effort be used in improving the two weakest subsystems.

It is well to note that the preceding conclusions can be generally drawn regardless of model or failure rates used; however, as regards differences in absolute values of the predictions, it is seen that wide variations exist. For example, at the system level, STL predicts a one-year reliability of 0.20, whereas PRC predicts 0.00026, a difference of three orders of magnitude. To see the effect of failure rates at the system level, one notes that use of current STL rates (i.e., non-PDS rates) in either model results in approximately a hundredfold increase in predicted system reliability over that using PRC rates. This accounts for two of the three orders of magnitude difference, and, since assignment of failure rates involves a considerable amount of subjective judgment, this difference must be viewed as an "honest" difference in basic failure rates.

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[1] Assuming that the 0.7 requirement is not relaxed.

The remaining order of magnitude difference, then, must be attributable to modeling differences. That this is true can be seen by comparing corresponding columns in the "system" row of Exhibit 22 (e.g., using PRC rates in the STL and PRC models yields 0.00267 and 0.00026, respectively). Unlike the subjectively justifiable failure-rate differences, PRC feels that this difference due to modeling is not justifiable and should be resolved. More explicitly, as pointed out in Reference 1, since (1) STL and PRC use the same general method of analysis and (2) the same OGO configuration is used, there is no valid reason that an order of magnitude difference in predicted system reliability should exist as a result of modeling differences.

Since Reference 1 has identified the modeling (and other) differences, the purpose of this TAM is to take the next step; that is, to examine further the reasons for such differences and to recommend, for the spacecraft system as well as for each major subsystem, a model or modeling approach which can be universally used with confidence. As will be seen, it is possible in some cases to state "this model is recommended," whereas in other cases, because differences in basic assumptions must be resolved first, only a general modeling approach can be recommended.

As in Reference 1, the spacecraft system models will be examined first, followed by an examination of the models of each major subsystem in the same order as that of Reference 1. To avoid needless repetition and use of models out of context, references to portions (e.g., equations or sections) of Reference 1 will be liberally made. Accordingly, it is important that the reader have a copy of Reference 1 at hand as he reads the remaining sections of this TAM.

2. Overall OGO System

Two of the prerequisites to realistic mathematical modeling of a complex system such as the OGO spacecraft are (1) a reliability block diagram of the system and (2) a mission profile. The former identifies the "in series" and "in parallel" elements[1] within the system,

[1] Used here in the sense of major "black boxes."

or, more generally, describes how the system elements relate reliability-wise, so that proper mathematical relationships can be written. The latter allows the model developer to identify the point in time when each system element is required. Some elements, for example, may be inoperative and/or in a quiescent state during certain portions of the mission and fully operable otherwise. Thus, the first prerequisite helps to ensure that all elements are considered, whereas the second ensures that they are considered only when they should be.

In addition to these two modeling prerequisites, it is also important that the model developer understand the effects of various types of failures and the system's remaining capabilities in the face of failures. He must, in short, be able to catalog all alternative configurations that the system can assume (as a result of failures and/or human or automatic reconfiguration decisions) which retain some or all of the system's capability. Thus, the failure-free system configuration or state and all the useful alternative states, together with appropriate nominal and alternative mission profiles, are all that is needed to develop the appropriate basic probability relationships expressing system and/or subsystem reliability.

Now, since the number of such alternative states may easily be untenably large for a complex system (such as a spacecraft system), the model developer is forced to make simplifying assumptions. He may, for example, assume that all system elements are "in series," so that only the failure-free state is of interest and the system reliability model routinely follows the well-known product rule. As regards the mission profile, note that this assumption also implies that every element must be fully operable for the entire duration of the mission. In general, each simplifying assumption amounts to ignoring the existence of certain alternative states that might exist and contribute to useful system capability. Dropping them and their associated probabilities of occurrence, therefore, yields pessimistic reliability predictions, the degree of such pessimism depending on the total probability of occurrence of such states and their useful contributions.

It is incumbent upon the model developer, therefore, to assess numerically the degree of pessimism that each simplifying assumption introduces into the model. He can--and it is often done--drop from the model any major element whose reliability is very nearly unity or, equivalently, whose contribution to unreliability is negligible relative to that of other elements. Unless he has a good quantitative appreciation for the degree of pessimism in his model, he cannot expect to achieve meaningful numerical predictions, nor can he confidently utilize the model to assist in reliability improvement analyses.

Returning now to the OGO system reliability modeling and predictions, the reader will note that Reference 1 points out that both PRC and STL were forced to make simplifying assumptions. At the system level STL utilized the product rule (cf. Equation (1) of Reference 1), taking into account "in series" and "in parallel" relationships at the subsystem level. PRC, on the other hand, recognized that, with the single exception of the Thermal Control Subsystem, all subsystems assume two distinct hardware configurations, each depending on whether or not the digital command portions (elevated to subsystem rank by PRC) of the system are operable. The difference in the approaches, therefore, is that PRC feels that the STL approach is an oversimplification which introduces too much pessimism into the predictions.

Accordingly, it is recommended that the PRC system model, Equation (2) of Reference 1, be adopted as the basic OGO system reliability model ("basic" in the sense that it be employed whenever a prediction of OGO system reliability is desired). For the reader's convenience and later reference, this basic model[1] is repeated below.

$$R_A = R_G R_B^{(1)} R_C R_D^{(1)} R_E^{(1)} \sum_i R_F^{(1)}(i) + (1 - R_G) R_B^{(2)} R_C R_D^{(2)} R_E^{(2)} \sum_i R_F^{(2)}(i) \qquad \text{(I)}$$

Recall that the superscript (1) indicates subsystem reliability given an operable Digital Command Subsystem, and the superscript (2) implies

[1] Dropping the second subscript "P," since it is no longer necessary.

that the Digital Command Subsystem is inoperable. The subscripts are to be interpreted as follows:

Subscript	Interpretation
A	OGO Spacecraft
B	Structure Subsystem
C	Thermal Control Subsystem
D	Power Supply Subsystem
E	Attitude Control and Stabilization Subsystem
F	Communications and Data Handling Subsystem
G	Digital Command Subsystem
S	Space Technology Laboratories
P	Planning Research Corporation

Note also that the above equation is now Equation (I); that is, for ease of reference all equations herein will be numbered with Roman numerals, eliminating the need for statements such as "Equation (8) of Reference 1." Finally, recall that it is understood that each factor in Equation (I) is a function of operating time, t.

Before going on to the next sections, which treat the subsystems individually, it is important to note that the philosophy underlying Equation (I) carries over--again with the exception of the Thermal Control Subsystem--to the subsystem level. That is, it is recommended that the basic reliability model for each subsystem be as follows:

$$R_X = R_G \, R_X^{(1)} + (1 - R_G) \, R_X^{(2)} \quad , \qquad \text{(II)}$$

where the subscript X can be any one of B, D, E, or F (i.e., excluding only C , the Thermal Control Subsystem). As in Equation (I), operating time, t , is implicit in Equation (II). Written explicitly as a function of operating time, Equation (II) becomes

$$R_X(t) = R_G(t) \, R_X^{(1)}(t) + \left[1 - R_G(t) \right] R_X^{(2)}(t) \quad . \qquad \text{(III)}$$

3. Structure Subsystem

As can be seen from Reference 1, STL and PRC have different reliability block diagrams for the Structure Subsystem. More explicitly, as seen from Exhibits 3 and 4 of Reference 1, the major difference in the reliability block diagrams is that STL assumes that deployment initiation will take place with certainty, whereas PRC believes that the probability of successful deployment initiation must be assessed, with and without an operable Digital Command Subsystem. Other differences occur in the interstaging function and in the hinge/spring portions of the deployment function. In addition, PRC considered the appendages, but further examination of their reliability (cf. Reference 3) yielded a predicted value of very nearly unity; hence, no factor for the appendages appears in the reliability equations.

Except for easily correctable errors in two reliability equations (Equations (11) and (17)), the STL equations accurately represent the configuration given in Exhibit 3.[1] Similarly,[2] PRC's equations faithfully represent the situation in Exhibit 4. An immediate problem, then, is how one is to resolve the dilemma of having two accurate sets of equations for the Structure Subsystem. Fortunately, resolution is very straightforward; there should be only one "true" reliability block diagram for the subsystem, and, once this is established, the appropriate reliability equations can rather routinely (because of the subsystem's relative simplicity) be written.

PRC wishes to go one step further. Specifically, since the reliability block diagram of Exhibit 4 was derived after considerable detailed

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[1] It is to be understood hereafter that all exhibits referred to are in Reference 1.

[2] At this juncture, some minor typographical oversights in Reference 1 should be pointed out. Specifically, P_{BS} in Equations (5) and (17) should have been written as R_{BS} to be consistent with Equation (1). Similarly, $P_{BP}^{(1)}$ and $P_{BP}^{(2)}$ of Equations (18) and (19) should have been written as $R_{BP}^{(1)}$ and $R_{BP}^{(2)}$, respectively, to be consistent with Equation (2). Finally, P_{BP} of Equation (5) should have been written as R_{BP}.

study of the actual design, it is believed that this is in fact the "true" reliability block diagram. Accordingly, it is recommended that GSFC adopt[1] Equations (15), (16), (18), and (19) as the basic reliability model equations for the Structure Subsystem. Of course, the effects of any subsystem design changes that have taken place subsequent to the development of these equations should be accounted for by appropriate revision of the equations.

It may be of interest to the reader to observe that Equation (6) can be put in the form of Equation (II). To see this, one need only combine Equations (6), (8), (10), (13), (14), (15), (16), (17), and (18) and then factor the result appropriately. In Equation (10), P(command) is equal to R_G in Equation (II), while P(no command) equals $1 - R_G$.

4. Thermal Control Subsystem

Since the STL model for the Thermal Control Subsystem is known to be in error (cf. Reference 1) in that 36 failure modes considered are not mutually exclusive, it is recommended that the PRC model given by Equation (21) be adopted as the basic reliability model for the Thermal Control Subsystem. Since the reliability P_{TS} of the thermal shield and the reliability P_{EP} of the thermal control equipment of the experiment packages can be shown to equal unity for all practical purposes, one can equivalently adopt Equation (23) as the basic model.

Further refinements of these equations may be desirable as a result of the heat balance analyses conducted by STL. Such refinements, if found necessary, would possibly affect the definition of failure from the standpoint of the number of louvers involved in each case and might modify the proportions of the failure rates assigned to "stuck open" and "stuck closed" conditions.

5. Power Supply Subsystem

In the case of the Power Supply Subsystem, STL has not been in consonance with the two fundamental prerequisites essential to realistic modeling; specifically, it has (1) oversimplified the basic reliability block

[1] As before, omitting the second subscript, "P."

diagram and (2) generally ignored the mission profile. That STL recognizes the importance of mission profile to the model is evident from its introduction of the concept of "criticality" of component parts. That is, all Power Supply Subsystem component parts are categorized as to the percentage of time that a failure is "critical" to the subsystem. The percentages used are 100, 50, 20, and 0. The overall effect of this concept is to reduce the total number of component parts that enter into the reliability prediction calculations. As shown in Exhibit 10, only 318 of the 499 parts comprising the subsystem enter into the calculations, with 181 being considered noncritical.

Now the question can be asked, "If such parts are noncritical, why fly them at all?" The answer, of course, is that their criticality is mission-time-dependent, and the notion of criticality is introduced more or less as a type of averaging process to avoid the necessity of looking in detail at a number of distinct, useful subsystem states. In short, it simplifies the analysis. PRC contends, however, that in order to ensure that the notion of criticality gives acceptable results one must "check it out" by carefully examining the alternative states that might occur during the mission. In this event, the detailed analysis might well be used and the criticality notion disregarded. Even the argument that "If the criticality approach works for one subsystem, it can be applied to others," appears questionable, since the subsystem configurations and functions differ greatly.

On the other hand, the PRC analysis considers every component part,[1] the detailed interrelationships among subsystem elements, the mission profile (including solar cell and battery degradation), the command backup capability, and a number of likely failure modes. As a result the model equations developed by PRC are felt to represent real life faithfully. Accordingly, it is recommended that GSFC adopt Equations (25) and (26) and their supporting equations as the basic reliability model equations for the Power Supply Subsystem for EGO missions.

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[1]The Power Supply Subsystem as defined by PRC contains fewer total component parts (232) than that defined by STL (499). This difference can be localized to the charge control units, but further resolution is impossible without the details of STL's parts count methods.

6. Attitude Control and Stabilization Subsystem

PRC's initial assessment (cf. Reference 4) of the ACS Subsystem essentially considered the subsystem as consisting of a relatively large number of "in series" elements and a few "in parallel" elements. As a result, the reliability model equations were rather straightforward, primarily involving the product rule. In the second and third assessments, however, PRC analyzed the ACS Subsystem in much more detail. It is unique among the subsystems in the sense that it must automatically (with minimal command backup) cycle itself through several modes of operation during the mission, each such mode involving, in effect, a reconfiguration of the ACS Subsystem components that must be active. Thus, PRC's preliminary reliability assessment was too gross, since it essentially assumed that the majority of component parts must be fully energized throughout the entire duration of the missions. To overcome this lack of realism, PRC's later reliability assessments of the subsystem were based on the functional approach of describing subsystem reliability in terms of the reliability of the four (non-independent) servo channels comprising the subsystem, carefully keeping track of the configuration of actively operating components in each of the operating modes that the subsystem passes through during the mission. In addition, the revised models accounted for the increase in subsystem reliability associated with the command backup capability (cf. Equation (II) with X = E).

STL's current model (cf. Reference 2), on the other hand, is very similar in concept to PRC's preliminary model and consequently possesses the same limitations. Mission profile effects are partially considered by STL via introduction of duty cycles for some of the parts. It is also interesting to note that the criticality concept is used very little by STL for this subsystem. Finally, STL's component parts count of the subsystem is 1,188 versus 1,467 by PRC.[1] Not counting 279, or 19 percent,

[1] The parts count difference is primarily a result of the handling of the sensor electronics and logic assembly (SELA), although the difference in approach also accounts for numerous discrepancies. Resolution of the differences would require a knowledge of the details of STL's parts count method.

of the parts effectively "buys" more reliability; however, this practice is justifiable only if the reliability of these parts is near-perfect or they are noncritical.

To sum up the preceding discussions of the two approaches, it is evident that STL has again oversimplified the situation with a concomitant loss in realism. PRC, on the other hand, has emphasized inculcation of realism wherever possible and consequently again feels obliged to recommend adoption of the PRC model equations as the basic reliability models for the ACS Subsystem. Equation (37) is a highly simplified version of the recommended PRC model equation, and the exact version is given by the set of equations on pages III. B-65 and III. B-66 of Reference 3.

It is well to note that neither STL nor PRC has as yet included the OPEP subsystem in either the overall spacecraft system or the ACS Subsystem reliability models and predictions. As will be seen in the next section, it is best to consider the effect of OPEP reliability (or, more precisely, OPEP unreliability) in conjunction with the assessment of the reliability of the CDH Subsystem.

7. Communications and Data Handling Subsystem

As in the case of the other subsystems, Reference 1 shows that the STL approach to reliability assessment of the CDH Subsystem is overly simplified. From the table on page 58 of Reference 1, for example, it is clear that STL uses the criticality notion to an unreasonably great extent. Furthermore, some of STL's basic assumptions are inconsistent (see, for example, item 2 on page 55 of Reference 1). It is well to note that the table on page 58 of Reference 1 might be interpreted to indicate that PRC also adopted the criticality concept, but to a lesser degree. Actually, PRC's reduction from 17,373 to 12,999 parts results from the number of simplifying assumptions regarding the CDU, the DDHA, and the tracking system. STL further oversimplifies the situation by not accounting for the backup capability of the Digital Command Subsystem.

Again, because PRC's model provides a much closer approach to realism than does STL's, there is no alternative to recommending that PRC's model be adopted. A simplified version is presented in Equations

(48), (50), and (51), and the exact equations are Equations III.A-16 through III.A-22 of Reference 3.

It is recognized that one of the main causes of divergence of the STL and PRC models stems from the fact that the assumptions underlying the two assessments differ greatly (cf. page 55 of Reference 1 for specifics). As a result, comparisons of the models in this area tend toward comparisons of "apples and oranges." It is felt that the assumptions utilized in the formulation of the PRC model are by far the more realistic. If, however, GSFC desires to make direct comparison between the models, resolution of the differences should be guided by GSFC clarifications as to which CDH Subsystem functions are felt to be of greater importance to the mission.

In addition, it has been recognized that model adjustments at the system and/or subsystem level to account for OPEP reliability are essential in order to increase modeling realism further. As to where this added consideration might most appropriately be introduced, PRC has concluded that it fits best as a factor in the CDH Subsystem models. The reason for this is that "operable states" are defined in the classical approach to be those with relative value equal to or greater than two-thirds, or, equivalently, those for which at least two-thirds of the experiments can still be "serviced" by the spacecraft. Loss of OPEP orientation, fully or in degrees, results in the loss of some or all of the OPEP experiments. Thus, since the CDH Subsystem is the only other subsystem whose failed states retain some experiment servicing capability, it is natural to revise the CDH Subsystem model to include combined OPEP/CDH states that are "operable" in the sense defined above.

Hence, for the CDH Subsystem it is recommended (1) that the PRC modeling approach be adopted and (2) that the concept of "operable" combined OPEP/CDH states defined in the preceding paragraph be incorporated.

8. SUMMARY

A REVIEW OF REFERENCE 1 LEADS TO THE CONCLUSION THAT THE STL RELIABILITY MODEL EQUATIONS FOR THE OGO SPACECRAFT SYSTEM AND MAJOR SUBSYSTEMS ARE GREATLY OVERSIMPLIFIED, WHEREAS THOSE DERIVED BY PRC TAKE EVERY FEASIBLE STEP TO REPRESENT THE REAL-LIFE SITUATION FAITHFULLY. ACCORDINGLY, IT IS RECOMMENDED THAT THE PRC MODELS BE ADOPTED AS THE BASIC MODELS TO BE USED IN MAKING RELIABILITY PREDICTIONS AND ALLOCATIONS AND IN CONDUCTING DESIGN IMPROVEMENT INVESTIGATIONS.

FOR GREATER REALISM, OPEP CONSIDERATIONS CAN BE INTRODUCED INTO THE CDH SUBSYSTEM MODEL.

IF CAPABILITY FOR DIRECT COMPARISON OF MODELS IS CONSIDERED NECESSARY, THE MODEL DIFFERENCES IN THE CDH AREA SHOULD BE RESOLVED UNDER GSFC GUIDANCE.

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1. Comparison of Current STL and PRC OGO Classical Reliability Predictions. Technical Advisement Memorandum No. 34-18. Planning Research Corporation, 18 November 1963.

2. OGO Reliability Assessment Report Number V. Technical Report No. 2311-6036-RU-000. Space Technology Laboratories, 30 November 1962.

3. Third Reliability Assessment for the Orbiting Geophysical Observatories. Report No. R-309. Planning Research Corporation, 15 April 1963.

4. Preliminary Reliability Assessment for the Orbiting Geophysical Observatories. Report No. R-243. Planning Research Corporation, 1 February 1962.

TECHNICAL ADVISEMENT MEMORANDUM NO. 34-27

PRELIMINARY REVIEW OF OGO S-50 POWER CONTROL UNIT

PRC D-818

10 August 1964

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TECHNICAL ADVISEMENT MEMORANDUM NO. 34-27

To: Assistant OGO Project Manager, GSFC, NASA

From: PRC OGO Reliability Assessment Team

Subject: Preliminary Review of OGO S-50 Power Control Unit

1. Introduction

A "system-level" review of the OGO S-50 power control unit design and failure-switching provisions was conducted to form the basic modeling framework for the detailed reliability assessment of the subsystem design. This TAM discusses areas in which the preliminary qualitative analysis indicates that performance and reliability can be improved by subsystem changes in the proposed design. Detailed numerical assessments are not included here, but will be given in the fifth reliability assessment of the OGO spacecraft.

Subsystem functional operation and the available failure-switching provisions are described in Section 2. Changes recommended in the proposed design, including some circuit changes, are discussed in section 3.

2. Subsystem Description

a. General

The function of the OGO S-50 Power Supply Subsystem is to furnish direct-current electrical power to the spacecraft loads at a load bus voltage regulated to be within 23.5 and 33.5 volts d-c. This is accomplished by using solar cells to furnish power to the loads and to charge the batteries when the spacecraft is in sunlight, and by using the batteries for delivering power to the loads when the spacecraft is in darkness.

The power control unit automatically controls the charge current of each battery to a constant value of 1 ampere, 5 amperes, or 10 amperes, as commanded from the ground. In addition, the power control unit reduces the battery charge current when an upper

voltage limit is reached to prevent battery overvoltage. A nominal upper voltage limit of 36.4 volts, 37.4 volts, or 38.4 volts (which are also functions of battery temperature) can be selected by ground command.

Exhibit 1 is a functional block diagram of the OGO S-50 Power Supply Subsystem and shows the two branches of the system including the major elements, which are the solar arrays, the batteries, and the power control unit. These major elements can be divided functionally into the following units:

(1) The solar array, which provides the basic system power and recharging of the batteries during the sunlight periods.

(2) The batteries, which provide the basic system power during the eclipse periods.

(3) The solar array shunt regulators, which control the solar array output current.

(4) The charge controls, which sense battery current, temperature, and voltage status to drive the shunt regulators.

(5) The series regulators, which drop the battery voltage during charge to the voltage required at the load bus.

(6) The discharge control, which controls the bypassing of the series regulators during discharge.

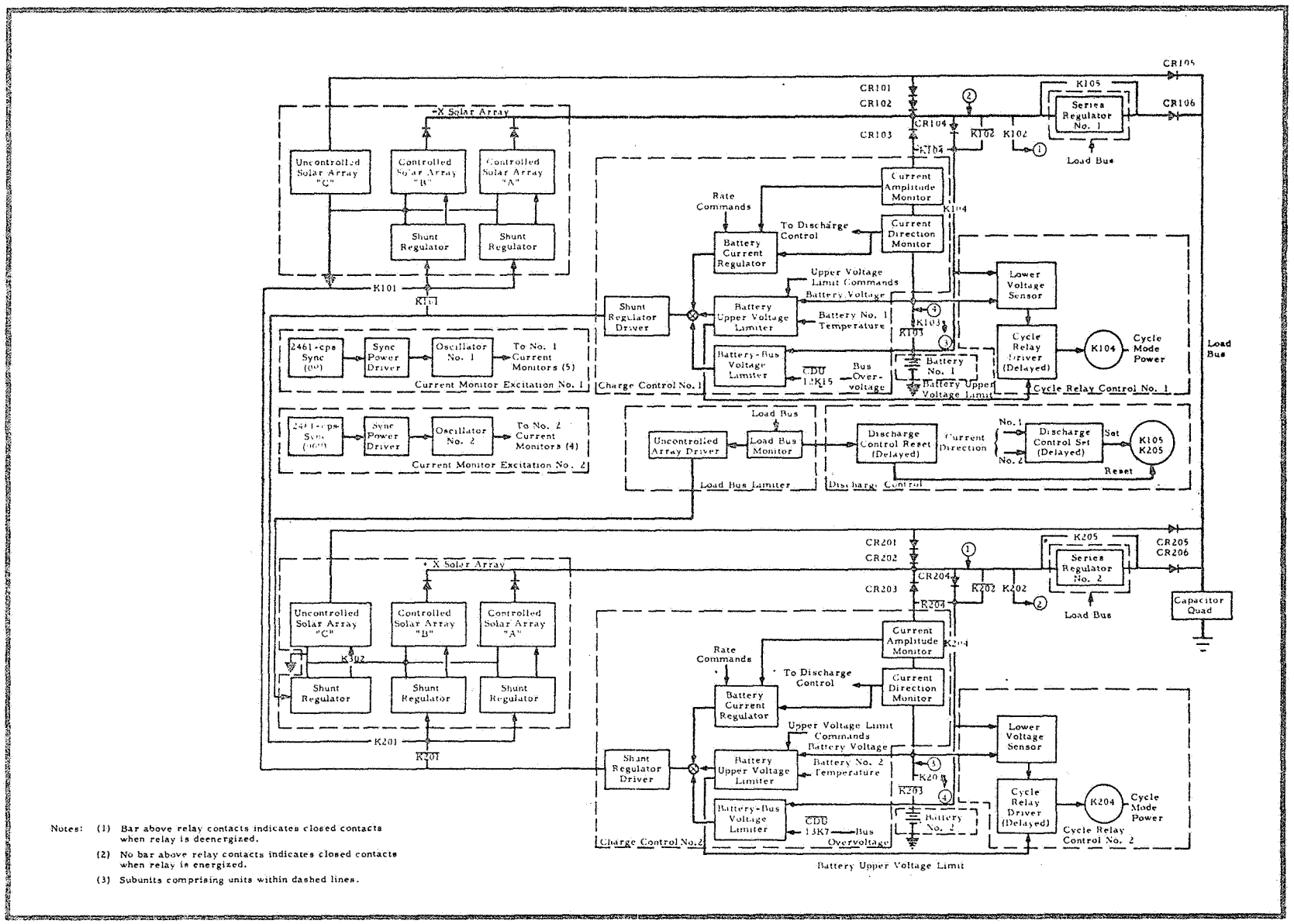
(7) The load bus limiter, which reduces the output of one of the "uncontrolled" array sections when the output of both uncontrolled sections is greater than the load requirements.

(8) The cycle relay controls, which control battery charge frequency during the extended sunlight period.

(9) The current monitor excitation oscillators.

(10) The capacitor quad, which filters the load bus voltage.

Functional operation of the Power Supply Subsystem is described in subsection 2.b. The subunits making up each of the units and the functional operation of each are described in subsection 2.c.



Notes: (1) Bar above relay contacts indicates closed contacts when relay is deenergized.

(2) No bar above relay contacts indicates closed contacts when relay is energized.

(3) Subunits comprising units within dashed lines.

EXHIBIT 1 - POWER SUPPLY SUBSYSTEM FUNCTIONAL BLOCK DIAGRAM

b. Subsystem Functional Operation[1]

The subsystem operates in two distinct modes, as selected from the ground by command to correspond with the orbit of the spacecraft. Mode I is the "continuous" mode of charging the batteries and will generally be used in sunlight-eclipse orbits; Mode II is the "cycle" mode of charging the batteries and will be used in extended sunlight orbits. The system current and voltage relationships of these two modes of operation as a function of time are illustrated in Exhibits 2, 3, and 4, which are referred to in the description of system operation below.

(1) Mode I (Continuous Charge Mode): Sunlight-Eclipse Orbit

(a) Case 1: Direct-Connected Arrays Furnish Less Power Than That Required by the Spacecraft Load

For the following discussion, reference is made to the Power Supply Subsystem functional block diagram in Exhibit 1 and the graphs in Exhibit 2, depicting the continuous mode of charging the batteries (Case 1).

Prior to T_0 in Exhibit 2, the spacecraft is in darkness, the output from the solar array is zero, the discharge control relay contacts (K105, K205) are closed, and the batteries are discharging as they furnish power to the spacecraft loads. In the case illustrated, the voltage of the batteries is approximately 25 volts, yielding a load bus voltage 0.7 volts lower, corresponding to the voltage drop through the diodes CR106 and CR206 in the respective branches. The discharge current from each battery in the case illustrated is 4 amperes.

As the spacecraft enters into sunlight (at time T_0 in Exhibit 2), the solar array is illuminated and the solar array voltage increases rapidly, reaching the battery voltage at time T_1. When the solar

[1] Much of the information concerning Power Supply Subsystem functional operation is taken directly from Reference 1.

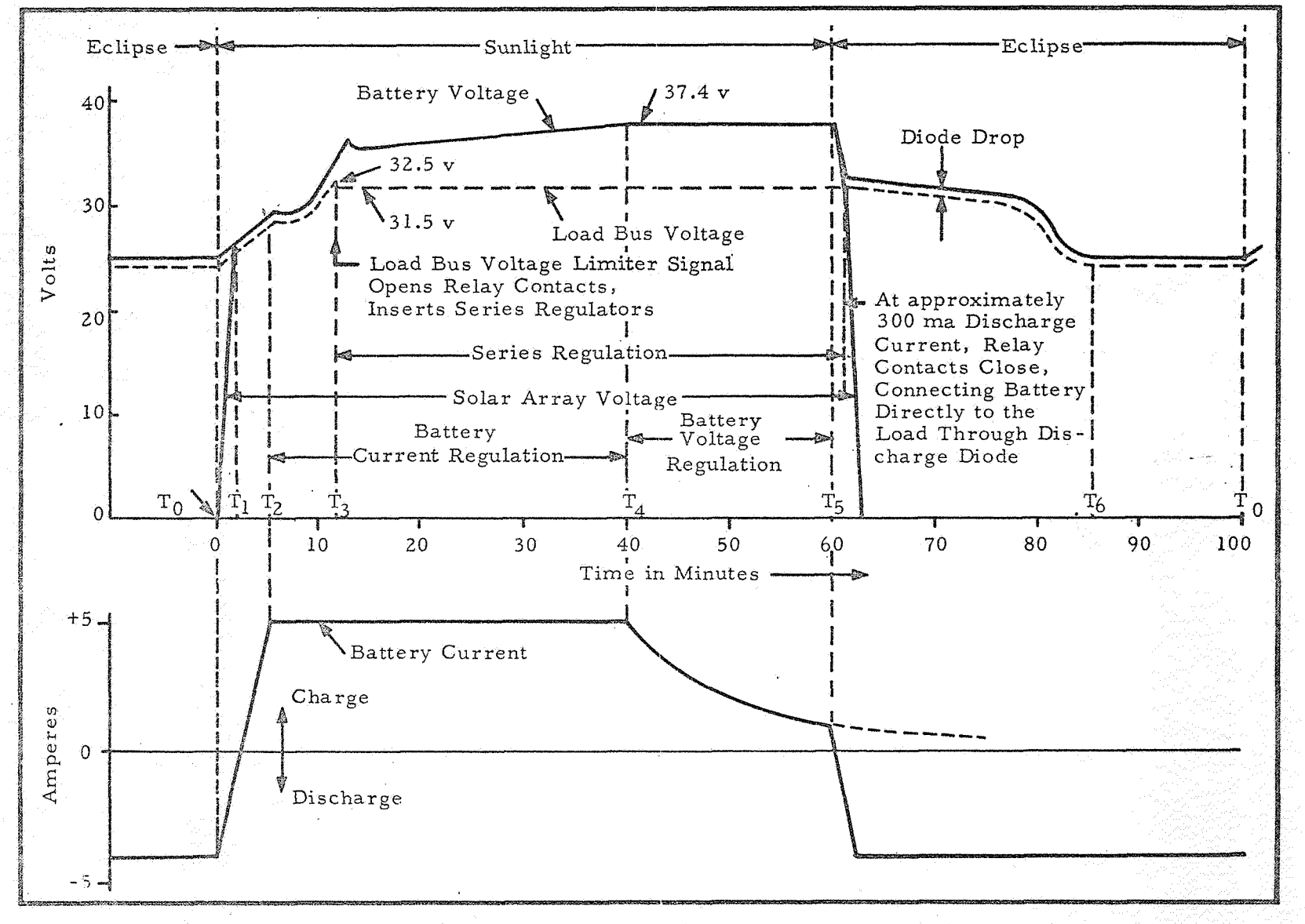


EXHIBIT 2 - MODE I (CONTINUOUS CHARGE MODE), SUNLIGHT-ECLIPSE ORBIT: UNCONTROLLED SECTIONS PROVIDING INSUFFICIENT POWER FOR SPACECRAFT LOADS

array begins to deliver power to the spacecraft loads, the solar array current increases and becomes larger than the load current, and the batteries start charging. The battery charging current continues to increase until, at T_2, it reaches the current limit commanded from the ground (i.e., 1 ampere, 5 amperes, or 10 amperes; in the case illustrated, the current limit is 5 amperes). Constant current regulation will now remain in effect until the battery voltage reaches the upper limit[1] as defined by the following equation:

$$V_B = 37.40 - 0.024\,(T_B - 30) \text{ volts}$$

where T_B is the battery temperature in degrees Fahrenheit.

When the load bus voltage reaches 32.5 volts at T_3, the discharge control relays are reset (deenergized), removing the shunts across the series regulators. For the remainder of the sunlight period, series regulation will be in effect, yielding a load bus voltage which is held to 31.5 volts ± 1 percent, while the batteries are charged to their selected upper voltage limit.

As solar array power is furnished to the load and to the batteries, each battery voltage continues to increase until (at T_4) the battery[2] voltage reaches its upper limit of 37.4 volts (for the normal upper voltage limit and 30° F battery temperature). At this time, battery voltage regulation starts and will be in effect for the remainder of the sunlight period to maintain the battery at the selected upper voltage limit. The battery charging current now decreases and continues to decrease until the end of the sunlight period. Charging the battery continuously (between

[1] Battery upper voltage limits can be decreased or increased one volt by commanding limit "A" or limit "B," respectively. The 37.4-volt limit is the normal value.

[2] The remainder of the paragraph describes the action of one branch during charge. The second branch will operate independently and in the same manner until one of the batteries indicates discharge and the discharge control relays are set.

T_4 and T_5) as described above constitutes the continuous mode of charging. (Refer to subsection 2.b(2) for the cycle mode of charging the batteries.)

As the spacecraft enters into darkness (at T_5), the solar array ceases to furnish power to the load and to the batteries. The battery voltages and the load bus voltage decrease. The battery charging currents reduce to zero and, as the battery voltages drop below 37.4 volts, battery voltage regulation ceases. When either of the battery currents reverses and reaches a value of approximately 300 milliamperes discharge, a signal is generated to set (close) the contacts of the discharge control relays, causing series regulation to cease and connecting the batteries directly to the load bus through their respective diodes in each branch.

During the sunlight-eclipse transition period, the solar array and the batteries share the load, consistent with the amount of power available from the solar array. When the solar array output goes to zero, each battery provides, in the case illustrated, 4 amperes to the load. During the period between T_5 and T_6 the battery and load bus voltages decrease, as indicated on the graph, until (at T_6) they again reach the steady values of approximately 25 and 24.3 volts, respectively. The total sunlight-eclipse sequence is completed when time T_0 is again reached.

The above discussion and Exhibit 2 are based on the premise that the two solar array sections connected directly to the load bus (not via the series regulators) combined provide less power than the spacecraft minimum load, so that the load bus limiter is not required to come into action to maintain the load bus maximum limit at 32.5 volts.

(b) Case 2: Direct-Connected Arrays Furnish More Power Than That Required by the Spacecraft Load

It should be noted that the battery voltage and current characteristics are essentially the same in Case 2 as in Case 1, but that the load bus voltage is regulated differently in Case 2, where the load bus limiter is active.

Exhibit 3 shows the voltage and current relationship when the direct-connected sections of the array can provide more power than the spacecraft load, as may be the case when the solar array is new or cold. The sequence up to the time T_3 is the same as in Case 1.

When the load bus voltage at time T_3 in Exhibit 3 reaches 32.5 volts, the load bus limiter starts regulating the load bus voltage to this value. At the same time, a signal from the load bus limiter resets the discharge control relays, removing the shunts from across the series regulators. Since, however, the load bus voltage is higher than the 31.5 volts at which the series regulator is designed to regulate, no current passes through the regulator; therefore, the series regulators have no control of the load bus voltage. The load bus voltage is regulated by the load bus limiter to 32.5 v ± 1 percent for the remainder of the sunlight period.

As in Case 1, battery current regulation takes place in the period from T_2 to T_4 and battery voltage regulation is in effect between T_4 and T_5.

When the spacecraft enters into darkness, the solar array decreases until the direct-connected sections of the array can no longer maintain the load bus at 32.5 volts, and the load bus voltage limiter drops out. Also, as the battery voltage goes below 37.4 volts, battery voltage limiting or regulation ceases, since the output from the battery charging arrays also decreases. The series regulator will regulate the load bus voltage to 31.5 volts as long as the array can put out enough power so that the battery does not discharge.

As in Case 1, when either of the battery currents reverses and reaches the value of approximately 300 ma discharge, the contacts of the discharge control relays are closed and the batteries are connected directly to the spacecraft load bus through their associated diodes.

(2) Mode II (Cycle Charge Mode): Extended Sunlight Orbit

If the Mode I method of charging were used during extended periods of sunlight, overcharging of the battery would result. Because of the inability of the battery to withstand continuous overcharge, a second charging mode, designed to prevent overcharging

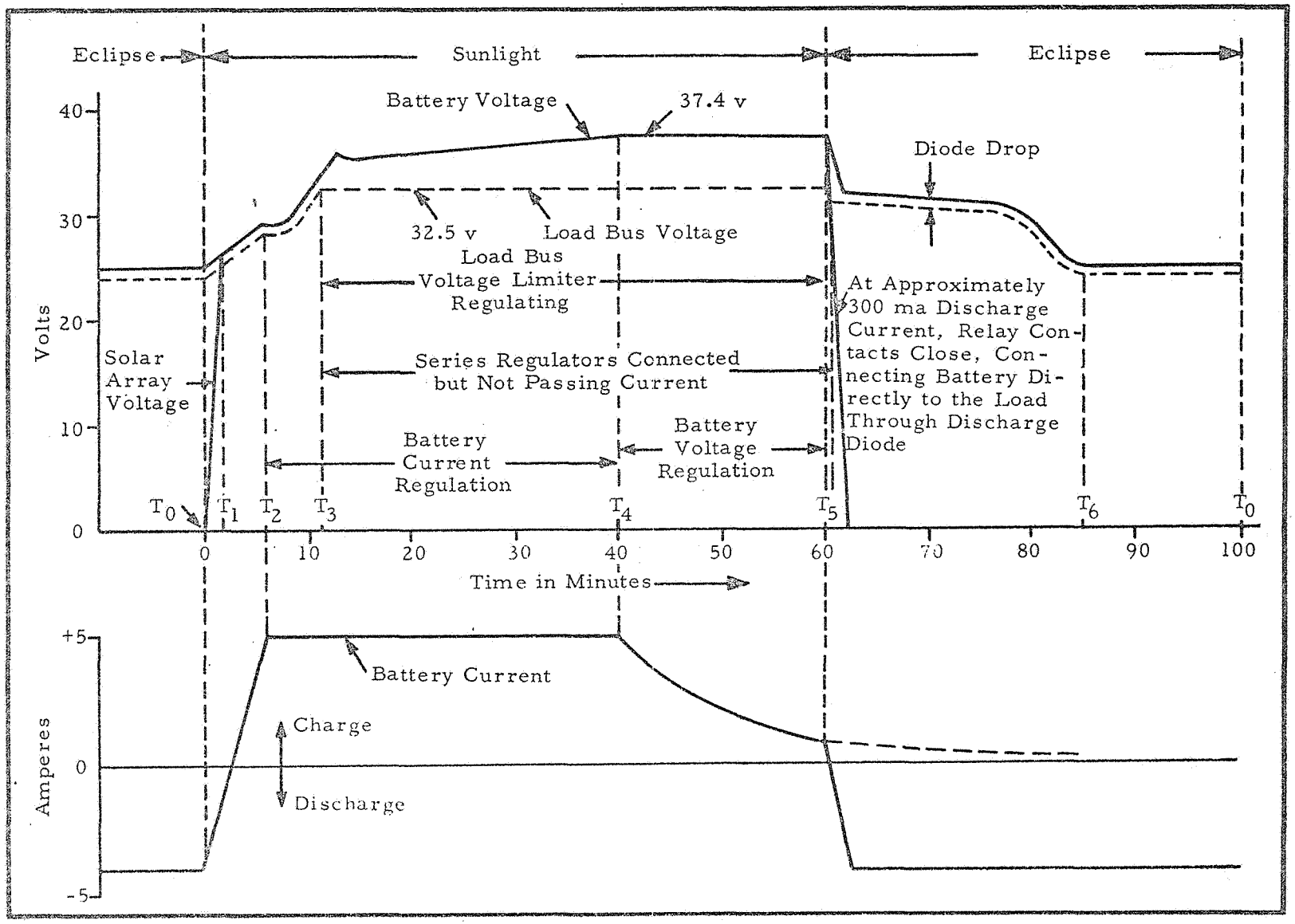


EXHIBIT 3 - MODE I (CONTINUOUS CHARGE MODE), SUNLIGHT-ECLIPSE ORBIT: UNCONTROLLED SECTIONS PROVIDING SUFFICIENT POWER FOR SPACECRAFT LOADS

of the battery, is utilized for the extended sunlight orbit. The Mode II charging method is selected by ground command and operates as described below (reference is made to Exhibit 4).

Charging of the battery[1] to the upper limit of 37.4 volts takes place in a manner similar to the continuous mode of charging; however, in the cycle charge mode relatively little time and charging power will be required for the battery to reach the upper voltage limit of 37.4 volts after reaching it the first time, since very little charge will be removed from the battery in the float cycle.

When the upper limit is reached, the charging circuit is opened by the cycle relay (K104 or K204) and the battery is allowed to float discharge down to the lower limit of 33.6 volts, as indicated in Exhibit 4. When the lower limit is reached, the cycle relay is deenergized and the battery is again placed on charge at the commanded charge rate. This cycle will repeat as long as the spacecraft is in the extended sunlight orbit, provided that the cycle command is present. The time required for charging to the upper limit and discharging to the lower limit will depend on the value of voltage selected for the lower limit.

During the period when a battery is on float discharge, its associated battery charge bus is regulated to 36 volts, as indicated in Exhibit 4, to prevent the battery from discharging rapidly and to minimize the series regulator losses.

c. Unit Functional Operation

(1) Solar Array

The solar array consists of 32,704 N-on-P solar cells, divided evenly between two paddles (+X and -X) mounted on either side of the spacecraft body. The cells are arranged in three sections per paddle, two controlled sections and one "uncontrolled" section.

The lowest level of electrical organization of the cells is a module, which consists of 7 parallel strings of 16 cells each. In turn, each controlled section consists of seven columns of seven modules each,

[1] Again, the process is described only for one branch. Each branch will operate independently and will be controlled by its associated cycle relay control logic.

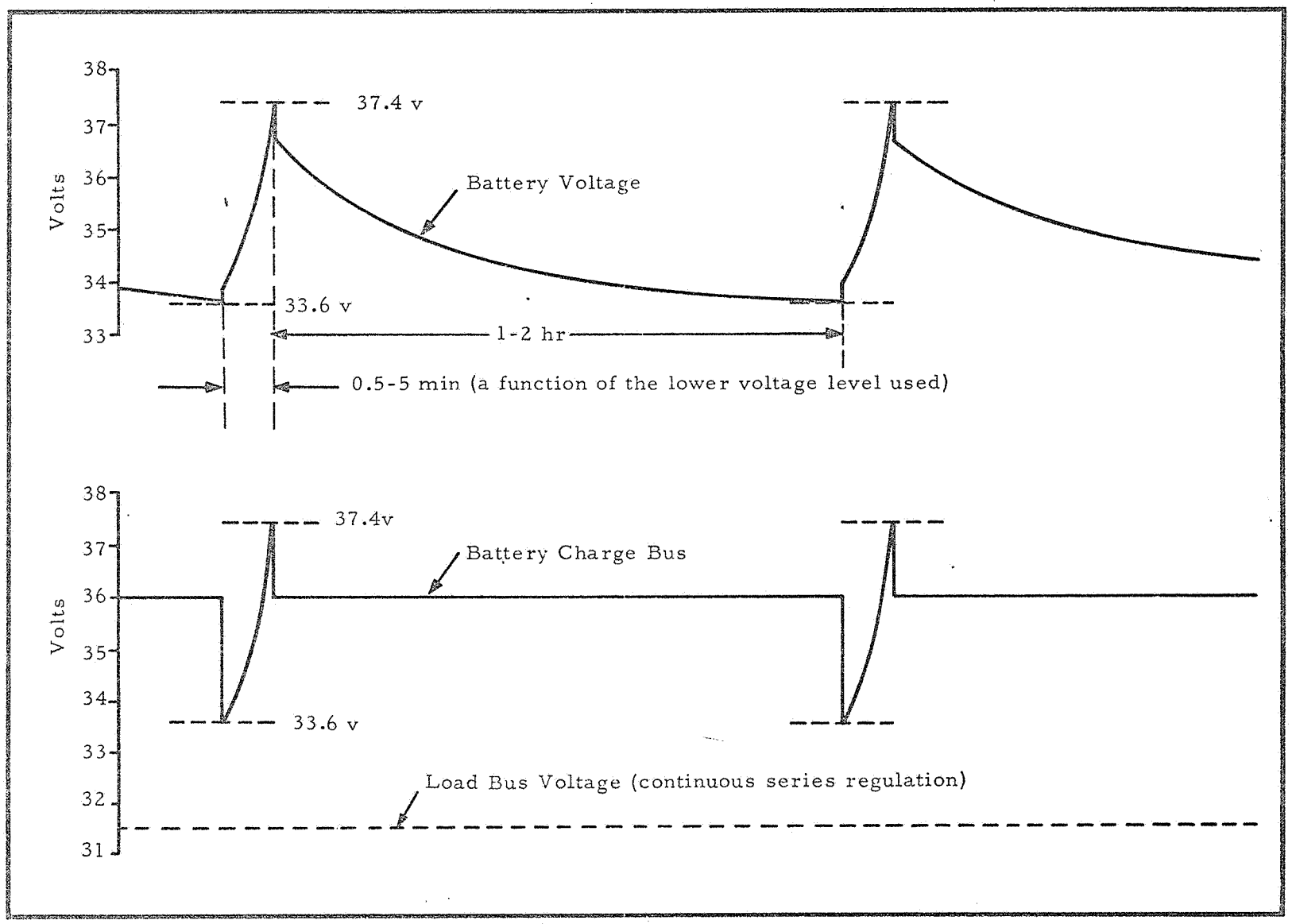


EXHIBIT 4 - MODE II (CYCLE CHARGE MODE), EXTENDED SUNLIGHT ORBIT

and each "uncontrolled" section consists of eight columns of six modules each. Thus, the controlled sections provide the voltage required to charge the batteries to full capacity, while the "uncontrolled" sections, which operate at the lower load bus voltage, provide increased current capability.

The output of each paddle is used to charge a separate battery and to supply power to the load bus. The output currents of the two "uncontrolled" sections are directly connected to their respective batteries and to the common load bus through isolating diodes. These sections are configured to supply less than the required load current (except during periods when the array is new or is extremely cold) so that a portion of the load current is normally supplied by the controlled sections through the series regulators. However, when the combined output of the two "uncontrolled" sections is greater than the load requirements, the output of the +X paddle "uncontrolled" section is reduced by the shunt regulation action of the load bus limiter to maintain the load bus voltage at 32.5 volts.

The parallel outputs of the two controlled sections of each paddle are connected directly to their respective batteries and thereafter to the common load bus through the series regulators and isolation diodes. The outputs of the controlled sections are regulated in order to provide both the remainder of the required load current (the portion not supplied by the "uncontrolled" sections) and the battery charge current as commanded by the ground. Reference is made to part (a) of Exhibit 5, which is a simplified diagram showing one section of a controlled solar array connected to the load (consisting of the load and battery current requirements). The method of controlling the solar array in the OGO S-50 system is by shunt regulation of the lower three modules of each section, as indicated in the exhibit. This method causes the lower portion of each regulated array to operate on the current-limited part of the solar array voltage-versus-current characteristic, as shown in (b) of Exhibit 5, and causes the upper portion (four-sevenths for a controlled section and one-half for the "uncontrolled" section) to operate on the voltage-limited part of the V-I characteristic, as shown in (c) of Exhibit 5.

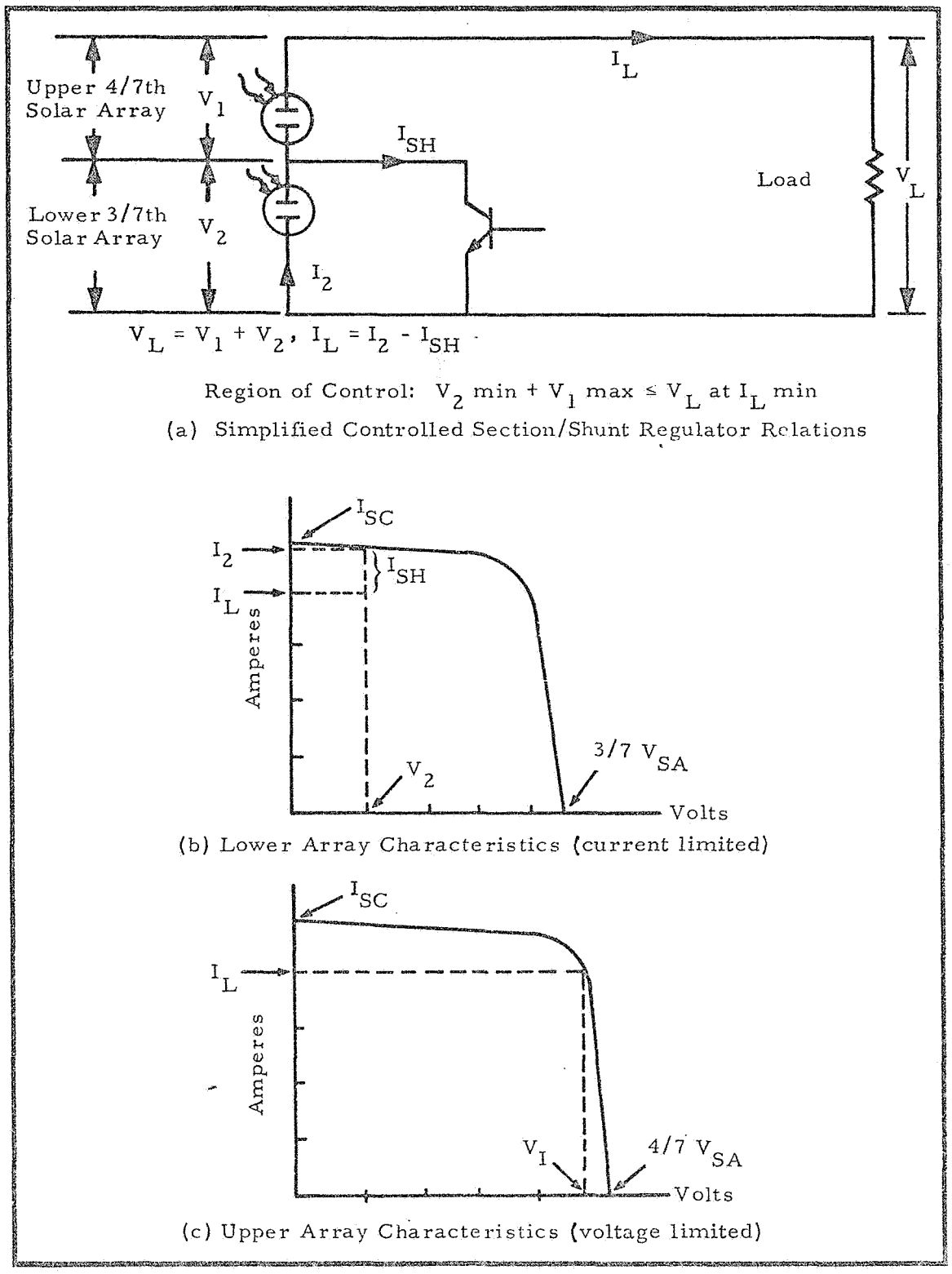


EXHIBIT 5 - METHOD OF SOLAR ARRAY CONTROL

Proper regulating control of the solar array output is effected when V_2 min + V_1 max $\leq V_L$ at I_L min (region of control), where the voltages and the current are as indicated in Exhibit 5.

(2) Batteries

The subsystem contains two batteries, one for each branch. Each battery consists of 24 Yardney YS 12S-SP, 12 ampere-hour capacity, silver-cadmium cells and is provided with a thermal switch. When the temperature of either battery exceeds 125° F, undervoltage relays 1 and 2 are activated, thereby disconnecting nonessential spacecraft loads.

During the continuous charge mode of operation, each battery supplies approximately one-half of the load requirements through its isolating diode to the load bus when no solar power is available. At the end of the eclipse (discharge) period, the two battery voltages are approximately equal and their depths of discharge are approximately equal because of the isolating diodes. During the ensuing sunlight portion of the cycle, each battery is recharged by its two associated controlled solar array sections. Charge current is regulated at the rate commanded from the ground by the charge control unit. Three charge rates (1 ampere, 5 amperes, and 10 amperes[1]) can be commanded, depending on the depth of discharge, length of available charge time, and whether one or two batteries are available. When the battery voltage reaches the upper limit (which is a function of battery temperature), the charge control unit reduces battery current to prevent overcharging. Three upper voltage limits (36.4 volts, 37.4 volts, and 38.4 volts) can be commanded, depending on the charge mode selected, the age of the batteries, and whether one or two batteries are available.

(3) Solar Array Shunt Regulators

The conductances of the power transistors shunting the lower three-sevenths of each controlled section and the lower

[1]Since the 10-ampere command actually effects current increments, a 6-ampere charge rate can be obtained if the 10-ampere rate is commanded without commanding the 5-ampere rate.

one-half of the "uncontrolled" array section are controlled by the charge control unit and load bus limiter unit, respectively. Regulation of the controlled sections is accomplished to provide the required load current plus a constant level of charge current in a closed-loop fashion. When the battery voltage reaches the selected upper limit, the charge current is further reduced to maintain the required battery voltage. The shunt resistance of the "uncontrolled" regulator is reduced by the load bus limiter when the load bus voltage exceeds 32.5 volts in order to maintain the load bus at this voltage.

(4) Charge Controls

Each charge control unit comprises the following subunits: (a) current amplitude monitor, (b) current direction monitor, (c) battery current regulator, (d) battery upper voltage limiter, (e) battery-bus voltage limiter, and (f) shunt regulator driver.

The shunt regulator driver sums the outputs of the battery current regulator, the battery upper voltage limiter, and the battery-bus voltage limiter. Regulation of the two controlled sections is effected by changing the current drain of the shunt regulators. The battery current regulator is activated by the current direction monitor when the battery is charging. In addition, an analog indication of battery current amplitude is delivered from the current amplitude monitor to the battery current regulator. Thus, the array current is regulated to maintain the required load current plus the selected battery charge current (1 ampere, 5 amperes, or 10 amperes). When the upper battery voltage limit is reached, the battery upper voltage limiter provides additional regulation to maintain the battery voltage at the upper limit. A temperature-sensitive element mounted on each battery permits the battery voltage to be limited to the following value:

$$E_B = 37.4 - 0.024\,(T_B - 30) \text{ volts}$$

where T_B is the battery temperature in degrees Fahrenheit. In addition to the analog control signal used to reduce the controlled array

current, the battery upper voltage limiter performs a second function in the cycle charge mode. At the upper voltage limit, a signal is delivered to the cycle relay control to energize the cycle relay (when power is applied by ground command).

The battery-bus voltage limiter does not function in the normal continuous charge mode unless a failure causes the bus voltage to exceed 34.1 volts. When this condition occurs, the bus overvoltage causes the battery-bus voltage limiter, which functions as a voltage regulator, to reduce the controlled array voltage and limit the battery charge bus to 34.1 volts.

The battery-bus voltage limiter does perform a normal function in the cycle charge mode. When the battery reaches the upper voltage limit, the battery upper voltage limiter causes the cycle relay to be energized. When the relay is energized, the contacts which remove the charge bus voltage from the battery apply this voltage to the battery-bus voltage limiter. The charge bus voltage thus activates the battery-bus voltage limiter and functions as the control input so that the controlled array is regulated to maintain the charge bus at 36 volts. When the cycle relay is again deenergized, the charge bus voltage is removed from the battery-bus voltage limiter (deactivating this subunit), and array output regulation is returned to the battery current regulator.

(5) Series Regulators

A series regulator is inserted between each battery and the load bus during battery charge so that the batteries can be charged as high as approximately 38.4 volts without exceeding the maximum load bus voltage of 33.5 volts. The voltage drop is accomplished by varying the resistances of two parallel power transistors which are inserted between the batteries and the load bus to maintain load bus voltage at +31.5 volts. When the output of the two "uncontrolled" array sections is sufficient to increase the load bus voltage above 32.5 volts, the series regulator will be fully open and no load current will be supplied from the controlled array sections. In this instance, the load bus limiter supplements the action of the series regulators and reduces the

output of the +X array "uncontrolled" section to maintain load bus voltage at +32.5 volts. When the battery discharges into the load during eclipse periods, the series regulators are shunted by the discharge control relays to prevent any power loss across the series transistors.

(6) Discharge Control

The discharge control unit is comprised of the following subunits: (a) discharge control relays, (b) discharge control set, and (c) discharge control reset. Input signals are also derived from the load bus monitor and the two current direction monitors. Each relay is a magnetic latching type which requires independent "set" and "reset" signals to be energized or deenergized, respectively. When the discharge control relays are set (energized), contacts shunt the power transistors of the series regulators, permitting the batteries to discharge directly into the load bus through their respective isolating diodes. A positive signal from either current direction monitor (indicating battery discharge current equal to 300 ma) will cause the discharge control set to energize both relays. The relays will remain in the energized state through the discharge period and the ensuing charge period until the solar array provides sufficient power to increase the load bus voltage to 32.5 volts. At this time, the load bus monitor subunit of the load bus limiter sends a signal to the discharge control reset to reset (deenergize) the relays, thus removing the shunts from across the series regulators.

Miller integrator circuits are incorporated into both the discharge control set and discharge control reset subunits to provide finite time delays in changing the state of the relays. The delay in the "set" circuit prevents a momentary battery discharge indication from bypassing the series regulators. The action of both delays permits the battery to discharge for short periods during the beginning of an eclipse with the load bus voltage above 32.5 volts; thus, immediate activation of the discharge control relays, which could cause an oscillatory condition, is prevented.

(7) Load Bus Limiter

The load bus limiter unit comprises the load bus monitor and the "uncontrolled" array driver subunits. When the load bus voltage increases to 32.5 volts, the load bus monitor sends a signal to the discharge control unit to deenergize the discharge control relays, thereby inserting the series regulators. Subsequently, if the two "uncontrolled" array sections provide sufficient power to increase the load bus voltage above 32.5 volts, even though the series regulators cut off all load current from the controlled sections, the "uncontrolled" array driver causes the shunt regulator associated with the +X array "uncontrolled" section to draw sufficient current to maintain the load voltage at +32.5 volts.

(8) Cycle Relay Controls

Each cycle relay control unit comprises the following subunits: (a) cycle relay, (b) lower voltage sensor, and (c) cycle relay driver. An input signal is also derived from each battery upper voltage limiter, and the relays are not activated until cycle relay power is supplied by ground command. If relay power is present, the cycle relay is energized by the cycle relay driver when the battery upper voltage limiter senses that the battery voltage has reached the commanded upper voltage limit. Energization of the cycle relay removes the associated battery from charge and applies the charge bus voltage to the lower voltage sensor (thereby activating the subunit). The lower voltage sensor, in turn, holds the cycle relay energized until the battery voltage decays to approximately 33.6 volts. At this time the cycle relay is deenergized, and the battery is charged at the selected rate until the upper voltage limit is again reached.

An additional function of the cycle relay is to provide charge bus voltage to the battery-bus voltage limiter of the charge control unit when the battery is removed from charge. In this case, since no battery current is available for solar array regulation, the battery-bus voltage limiter is utilized to regulate the output of the controlled array sections to maintain each charge bus at approximately 36 volts.

A Miller integrator time delay has also been incorporated in each cycle relay driver. This delay prevents immediate energization of the cycle relay when the battery upper voltage limit is reached and ensures several seconds of battery charge at the commanded current rate.

(9) Current Monitor Excitation

Each current monitor excitation unit is comprised of a 2461-cps sync oscillator, a sync power driver, and a power oscillator. The output of the number 1 excitation unit provides excitation power for the battery current amplitude and direction monitors and the three telemetry current amplitude monitors in the number 1 branch; the output of the number 2 excitation unit provides excitation power for the battery current amplitude and direction monitors and the two telemetry current amplitude monitors in the number 2 branch. Each power oscillator can function in a free-running mode if the 2461-cps sync oscillator fails; however, the system's noise level will be increased if the synchronization is lost.

(10) Capacitor Quad

The capacitor quad filters any load bus transients.

d. Failure Switching

The available switching which can be effected by ground command in order to alleviate the effects of equipment failure is illustrated in Exhibit 6. In addition, failure switching is automatically accomplished within the Power Supply Subsystem by (1) energizing undervoltage relays number 1 and number 2 when the temperature of either battery exceeds 125° F, thereby disconnecting nonessential spacecraft loads, and (2) causing the battery-bus voltage limiter to function as a solar array voltage limiter if the load bus voltage exceeds 34.1 volts. The failures which may be circumvented by the available switching features and the consequences of the revised configuration are discussed in the following subsections.

(1) Charge Control Failure

If a charge control unit fails such that its two associated controlled array section outputs are incorrectly regulated,

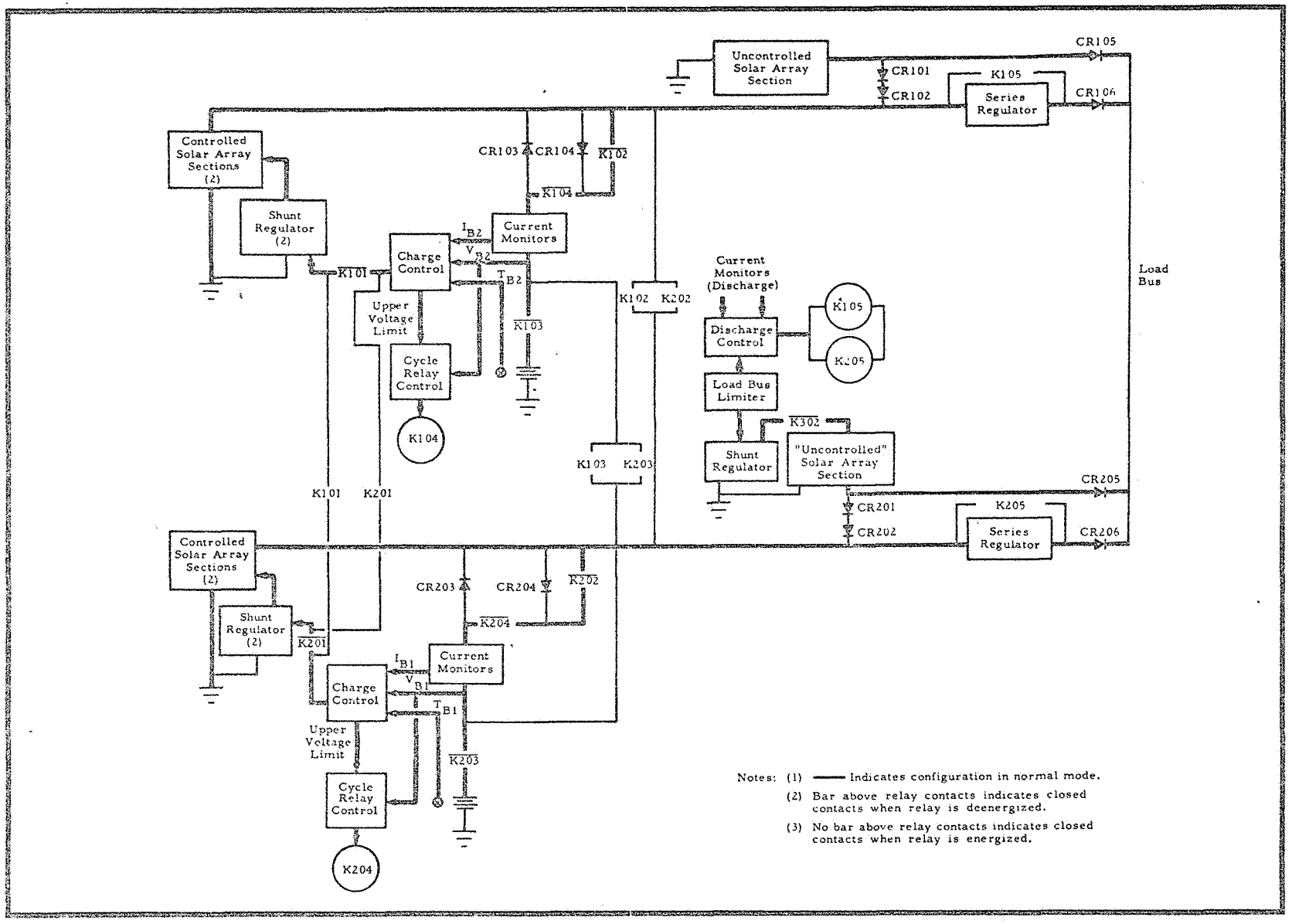


EXHIBIT 6 - FUNCTIONAL BLOCK DIAGRAM SHOWING AVAILABLE FAILURE-SWITCHING PROVISIONS

K101 and K102 (or K201 and K202) can be energized by ground command. Exhibit 7 is a functional block diagram of subsystem operation with charge control number 1 switched out.

When one of the charge control units is switched out, the outputs of the four controlled array sections are connected and supply the paralleled batteries. The four controlled array section shunt regulators are placed under the control of the operational charge control unit, and the battery charge current associated with the operational charge control unit remains controlled to the commanded value. When relay K102 (or K202) is energized, diode CR104 (or CR204) is inserted in the charging path of the other battery. By this method, the batteries are not directly paralleled and the battery associated with the failed charge control unit is supplied sufficient charge current to cause its voltage to follow that of the operational channel less the voltage drop of diode CR104 (or CR204). Charge current to both batteries is reduced when the battery of the operational branch reaches the command upper voltage limit.

In the cycle charge mode, each cycle relay effects the charging of the individual batteries as controlled by its associated control logic. If the failure in the charge control unit which has been switched out is such that the cycle relay is continuously energized (when cycle mode power is applied), the associated battery will be continuously "floated"; if the relay is energized below the commanded voltage level, the associated battery will be removed from charge below the commanded voltage level and will not reach full charge. On the other hand, even if the cycle relay function of the failed charge control unit remains operational, the "captive" battery will follow the voltage of the battery of the operational branch, less the voltage drop of the diode inserted by activation of the cross-strapping relay, K102 (or K202). When the operational branch battery reaches the upper voltage limit, its cycle relay will be energized, maintaining the common charge bus at approximately 36 volts. Thus, the captive battery will never be removed from the charge bus and will be trickle-charged through diode CR104 (or CR204) between 36 volts and the upper voltage limit of the operational charge control unit.

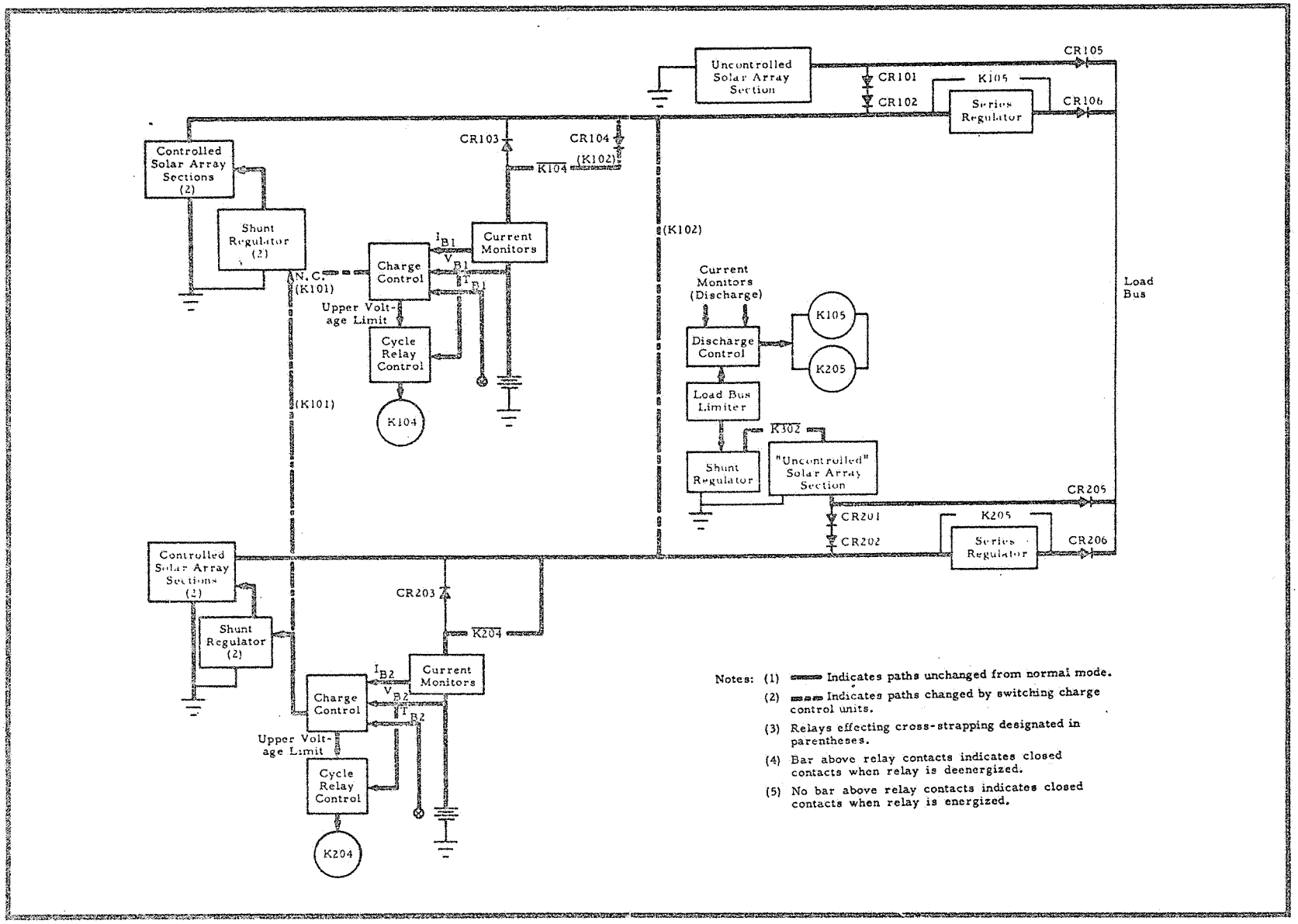


EXHIBIT 7 - FUNCTIONAL BLOCK DIAGRAM WITH ONE CHARGE CONTROL FAILED

(2) Battery Failure

If a battery fails, either by opening or shorting, K103 (or K203) can be energized to remove the battery from the circuit. The charge buses can then be connected to supply the full charging capability of the four controlled array sections to the surviving battery by energizing K101 and K102 (or K201 and K202), thereby putting the four controlled sections under the control of a single charge control unit. Exhibit 8 is a functional block diagram of subsystem operation with one battery and one charge control unit switched out.

Although the two current monitor paths are in parallel, insertion of diode CR104 (or CR204) prevents current (which could be caused by charge bus imbalance) from flowing through the "failed" charge control monitor in either direction. Thus, a continuous discharge indication from one of the current monitors, which would cause the series regulators to be bypassed, is circumvented. In addition, since only one charge control unit is controlling the combined outputs of the four controlled array sections, the battery charge current is controlled to the commanded value, rather than being approximately twice the commanded value, as would be the case if both charge control units were permitted to supply battery current in parallel.

During the eclipse when the battery discharges into the load, the single battery must supply the entire load current demand.

In the cycle charge mode, the voltage indication of each charge control unit is connected to the surviving battery, and each cycle relay will be energized at an upper voltage limit which is dependent on its individual battery temperature indication. If the cycle relay of the "failed" (switched out) charge control unit operates at the lower voltage, operation will be satisfactory since the common charge bus will not be regulated to 36 volts until the operational cycle relay is energized. However, if the cycle relay of the "failed" charge control unit is not energized or is energized at a higher voltage than the operational cycle relay, the charge path through CR104 (or CR204) will not be opened when the common charge bus is regulated to 36 volts. In this case, the battery will not discharge to the lower voltage limit to energize the operational cycle relay and will be continuously trickle-charged at 36 volts.

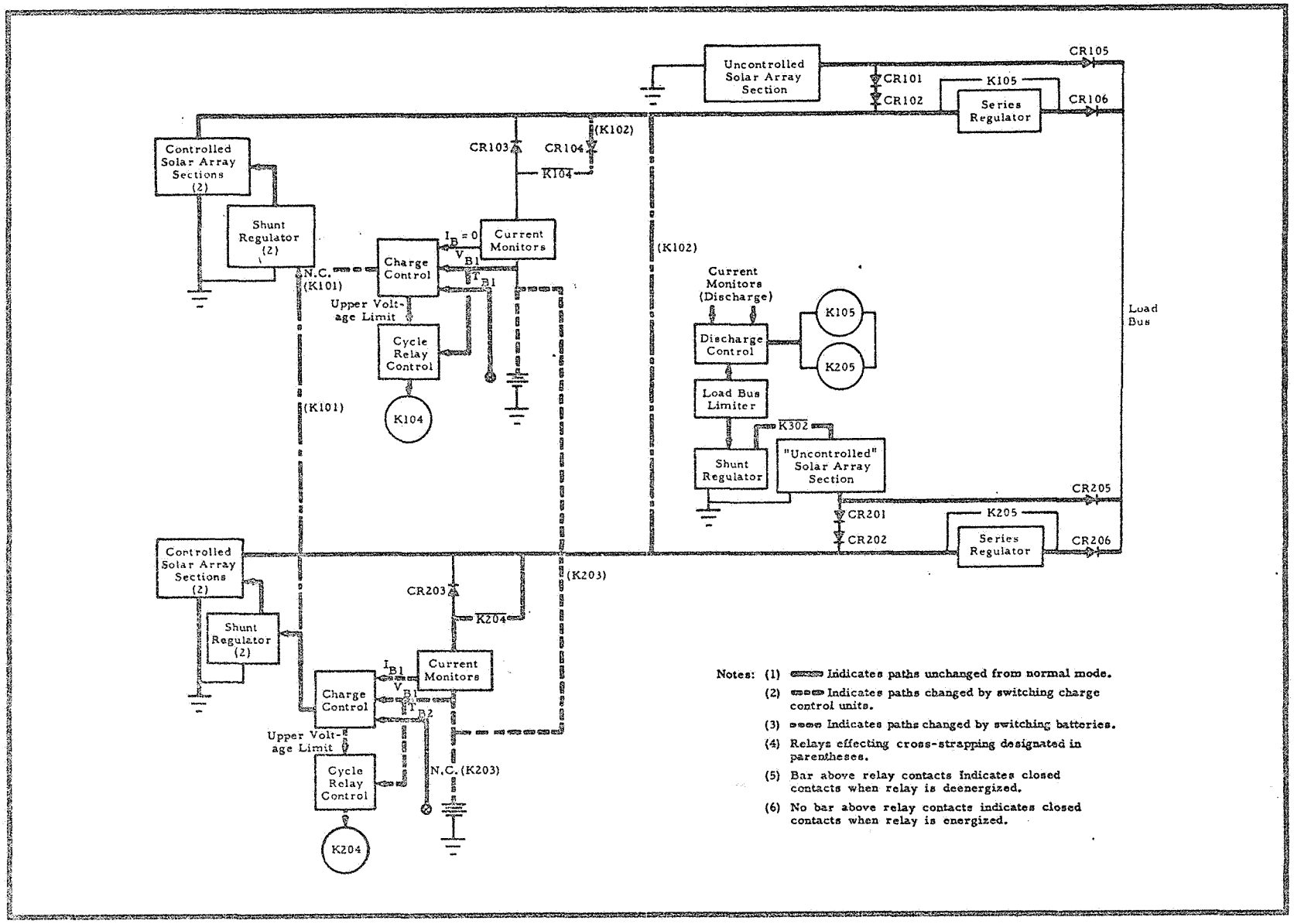


EXHIBIT 8 - FUNCTIONAL BLOCK DIAGRAM WITH BATTERY NO. 2 FAILED AND CHARGE CONTROL NO. 1 FAILED OR SWITCHED OUT

(3) Series Regulator Open

If either series regulator fails open, K101 and K102 (or K201 and K202) can be energized, configuring the controlled array sections and the batteries as illustrated in Exhibit 7.

In this case, the subsystem operation is the same as that for a charge regulator failure except that the entire controlled array load current must be carried by the operational series regulator.

(4) Series Regulator Shorted

(a) One Series Regulator Shorted

If either series regulator fails shorted or if one of the discharge control relays remains energized, the load bus will be at the battery voltage of the shorted series regulator. The charge control units will automatically reduce both controlled array outputs (and battery voltages) to approximately 34.1 volts to prevent load bus overvoltage. In this case, the bus overvoltage feedback can be removed from the charge control unit associated with the operational series regulator by energizing command distribution unit relay 12K15 (or 13K7) by ground command. The battery of the branch with the operational series regulator is then charged to its normal voltage, while the other battery charge voltage remains limited to 34.1 volts, providing approximately 25 percent of battery capacity.

In the cycle charge mode, cycle relay operation in the branch with the operational series regulator will be normal when the bus overvoltage feedback is removed. However, the battery associated with the shorted series regulator will be continuously trickle-charged at 34.1 volts, since the battery voltage will not reach the upper limit to energize the cycle relay.

(b) Both Series Regulators Shorted

If both series regulators are shorted or if the discharge control relays remain energized, the charge control units will automatically reduce both controlled array outputs (and battery voltages) to approximately 34.1 volts to prevent load bus overvoltage. The

charge voltage of both batteries will be limited to 34.1 volts, providing approximately 25 percent of battery capacity.

In the cycle charge mode, both batteries will be trickle-charged at 34.1 volts, since neither battery voltage will reach the level required to energize the cycle relays.

(5) Multiple-Unit Failures

Examination of Exhibit 6 indicates that the available failure switching is effective in circumventing any combination of single charge control, battery, and open series regulator failures in either channel. For example, if charge regulator number 1 fails, battery number 2 fails, and either series regulator fails open, then K101, K102, and K103 can be energized to configure the controlled array sections and battery as illustrated in Exhibit 8. In this case the subsystem operation is the same as that for a battery failure except that, with one series regulator open, the entire load current from the controlled arrays must be carried by the operational series regulator.

(6) "Uncontrolled" Solar Array Output Switching

If the load bus limiter fails such that its associated "uncontrolled" array section is either uncontrolled or fully shunted, the load bus limiter regulation can be removed by energizing K302.

3. Recommended Changes

The review of the OGO S-50 power control unit indicates three general areas in which improved functional reliability can be effected: (1) the failure-switching provisions, (2) the logic controlling the discharge control relays, and (3) various circuit refinements. The potential problems associated with each of these areas and the recommended changes in the proposed design are discussed below.

a. Failure-Switching Deficiencies

The available switching provisions which may be utilized to circumvent unit failures are discussed in detail in subsection 2.d. A high degree of redundancy has been incorporated into the proposed design

by providing means for cross-strapping the batteries and the charge control functions between the individual branches. It is evident from the preceding discussion, however, that the available cross-strapping provisions do not accomplish all that they could to utilize the two series regulators, nor do they provide optimum operation in the cycle charge mode. These deficiencies and recommended changes in the failure switching are discussed below. A functional block diagram incorporating all of the recommended switching provisions is included as Exhibit 9.

(1) Series Regulator Cross-Strapping

If one of the series regulators shorts, there is presently no method of removing the failed unit from the system. The battery-bus voltage limiters will automatically regulate the charge bus voltage of each channel to 34.1 volts, thereby charging each battery to approximately 25 percent of capacity. As previously discussed, the bus overvoltage feedback can be removed from the charge control unit of the branch containing the operational series regulator. This method permits normal charging of one battery; however, the battery associated with the shorted series regulator is limited to a charge voltage of 34.1 volts and is charged to only 25 percent of capacity.

In addition, since a series regulator cannot be removed from the circuit by this scheme, no failure switching can be performed if either of the series regulators is shorted. Any switching to circumvent a battery or charge control unit failure would automatically connect the charge buses. Thus, the charge voltage of both batteries (or a single battery if one has failed) would be limited to 34.1 volts, and each would be charged to 25 percent of capacity.

In order to alleviate these deficiencies, it is recommended that individual switching relays be incorporated for each series regulator which, on ground command, will remove the failed unit from the circuit and connect the charge buses. The proposed connections for these relays (designated K1 and K2) are illustrated in Exhibit 9. With the proposed failure-switching provisions, one of the charge control units must also be switched out by energizing K101 and K102 (or K201 and

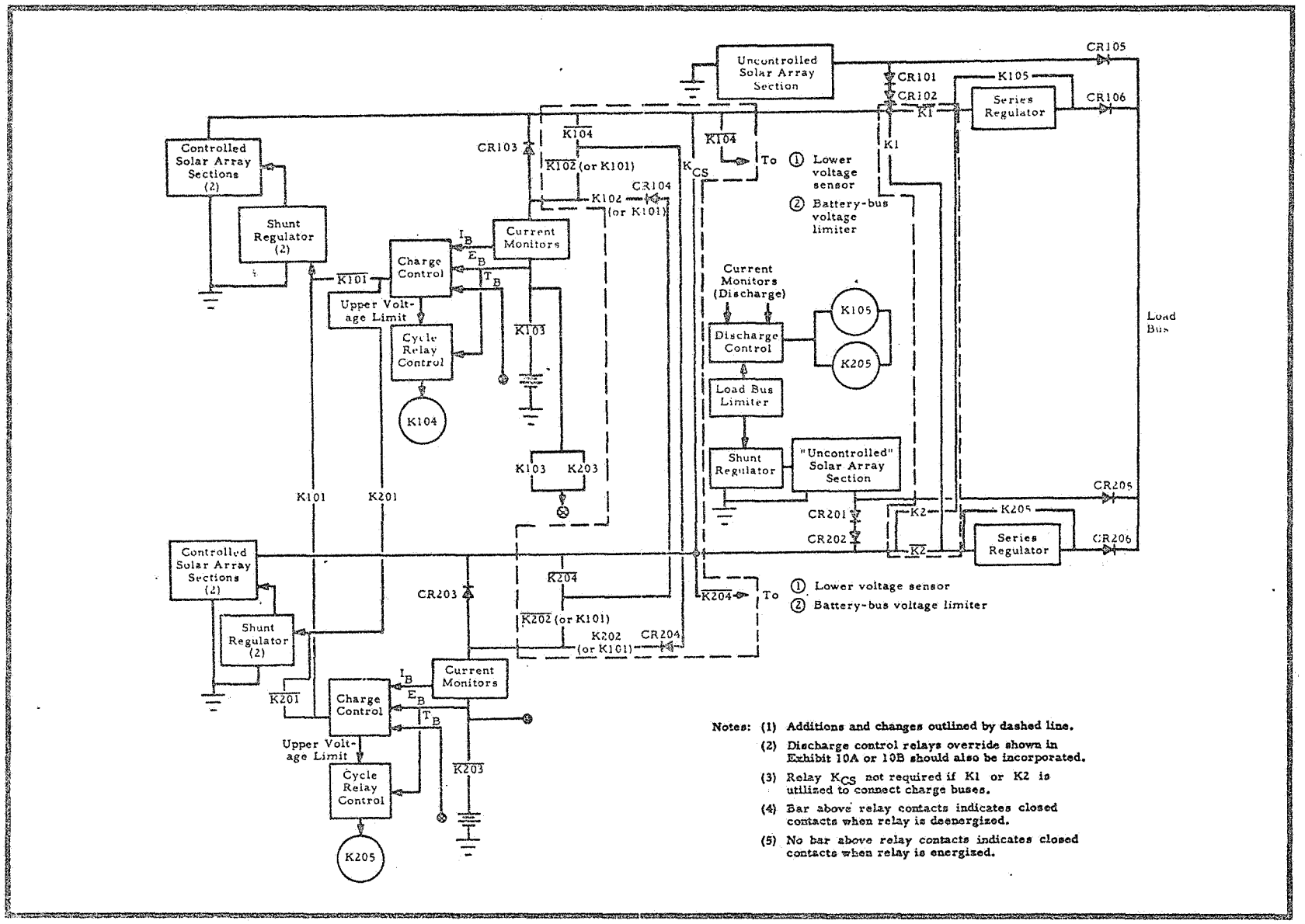


EXHIBIT 9 - PROPOSED MECHANIZATION OF OGO S-50 POWER CONTROL UNIT FAILURE-SWITCHING PROVISIONS

K202) to prevent directly paralleling the batteries except through diode CR104 (or CR204); however, addition of these relays would provide the following advantages:

a. In the event of a shorted series regulator, the operational series regulator could be commanded to carry the entire load from the connected battery charge buses. Thus, each battery could be charged to full capacity, rather than one battery being limited to a charge voltage of 34.1 volts.

b. Since a shorted series regulator can be disconnected from the system, additional failure switching can be performed to cross-strap the batteries and/or charge control units without limiting the common charge bus voltage to 34.1 volts and the charge of the batteries (or battery) to 25 percent of capacity.

c. The contacts of command distribution unit relays 12K15 and 13K7, which presently remove the load bus overvoltage feedback and allow one battery to be charged to full capacity, can be eliminated. Thus, the battery-bus voltage limiters would limit charge bus voltage to 34.1 volts only when both series regulators are shorted or when the discharge control relays remain energized.

d. Commands 11 and 13, which presently energize the load bus overvoltage feedback relays, can be utilized to control the series regulator switching relays.

(2) Cycle Charge Mode Cross-Strapping

When the cycle charge mode is commanded and the charge buses are connected by the present failure-switching provision, each cycle relay remains controlled by its associated voltage sensing circuitry. As previously discussed in subsection 2.d, the battery associated with the "failed" charge control unit will be either (1) continuously "floated" and removed from charge for the duration of the cycle charge mode or (2) continuously trickle-charged between the charge bus voltage of 36 volts and the upper voltage limit of the other battery. The effect of the cross-strapping in the cycle charge mode can be even more severe when charge bus cross-strapping is commanded because one

battery has failed. In this case, cycle mode operation will be normal for the surviving battery if the cycle relay of the "failed" charge control unit is energized at a lower voltage than the cycle relay of the controlling branch; however, if the cycle relay of the "failed" charge control unit is not energized before the cycle relay of the operational charge control unit is energized (regulating the common charge bus to 36 volts), the surviving battery will be continuously trickle-charged at 36 volts for the duration of the cycle charge mode through the deenergized cycle relay contacts.

In order to alleviate the above deficiencies, it is recommended that the battery charge paths be routed through the charge control failure-switching relays (K102 and K202) in the cycle charge mode as well as in the continuous charge mode. The proposed connections for these relays and the voltage-dropping diodes, CR104 and CR204, are illustrated in Exhibit 9.

Since all available contacts of the failure-switching relays K102 and K202 are utilized by the recommended scheme, one additional relay (designated as K_{CS} in Exhibits 10A and B) must be added to connect the charge buses. However, if the previously recommended series regulator switching relays are incorporated, the charge buses can be connected by energizing either of these relays, and the addition of relay K_{CS} is not required. If this were done, one of the series regulators would be switched out, and the other would pass the combined current from the common charge bus whenever the charge buses whenever the charge buses were connected.

In the continuous charge mode, with the recommended failure switching, failure-switching relay K102 (or K202) inserts diode CR104 (or CR204) into the battery charge path of the "failed" charge control unit effectively in the same way as in the present method. Thus, operation is unchanged in this mode.

In the cycle charge mode, however, one of the cycle relays is disconnected, and charging of both batteries (or a single battery) is controlled by the cycle relay logic of the operational charge control unit. Thus, conditions whereby a battery is continuously "floated" or trickle-charged because of a failure or imbalance of the cycle control

relay voltage sensing logic do not affect battery charging. Voltage-dropping diode CR104 (or CR204) is also inserted in the charge path of the "failed" channel to prevent overcharging the captive battery.

(3) Utilization of Failure-Switching Relays

In addition to cross-strapping the outputs of the shunt regulator drivers between the controlled solar array sections of the two branches, two sets of contacts of each failure-switching relay K101 (or K201) energize a second relay K102 (or K202). The second failure-switching relay is presently used to connect the charge buses and to insert voltage-dropping diode CR104 (or CR204) into the battery charge path of the failed charge control unit. This method requires two relays (one 4PDT and one 2PDT) in order to provide redundant contacts for each function. It is recommended that K101 and K201 each be replaced with a 4PDT relay type with contact ratings sufficient to carry the current presently carried by K102 and K202 in either the present or proposed failure-switching mechanization. Thus, two sets of contacts of K101 (or K201) could be used in place of K102 (or K202), as illustrated in Exhibit 9, eliminating the requirement for two relays.

(4) Discharge Control Relays Override

Both discharge control relays are simultaneously controlled by a single logic function consisting of the load bus monitor, the discharge control reset, the current direction monitors, and the discharge control set subunits. If a failure occurs in any of these functions such that the discharge control relays are not reset or remain energized, both series regulators will be bypassed and the batteries (or battery) will be charged to only 25 percent of capacity. The numerical probability of the occurrence of this type of failure has not been computed at this time; however, because of the number of elements controlling the relays and the consequences of this type of failure, it is recommended that one of the following alternatives be incorporated:

(a) The capability of resetting the discharge control relays by ground command.

(b) The capability of interrupting the discharge control relays bypass paths by ground command.

(c) Increased redundancy within the logic for controlling the discharge control relays.

(d) Redundant use of the battery-bus voltage limiter functions to control the discharge control relays on a voltage basis rather than on a current basis.

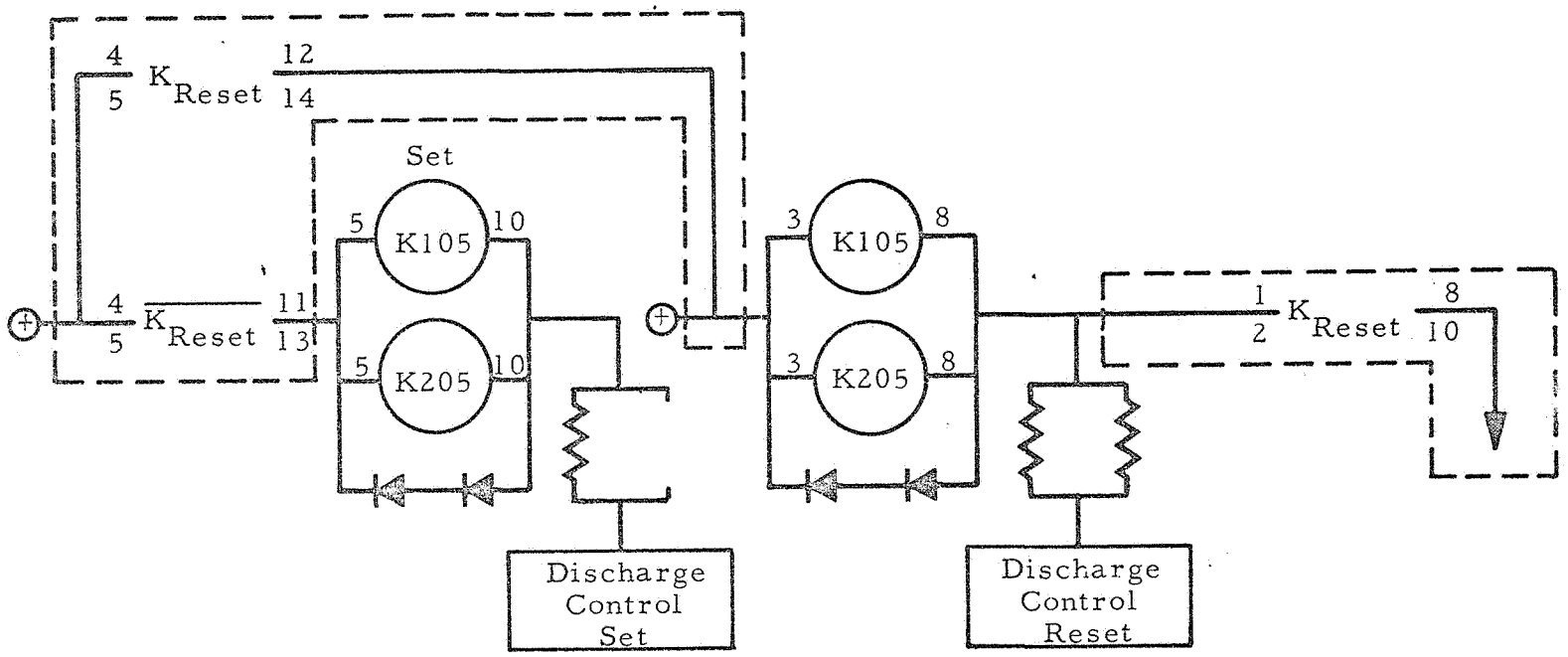
Methods of incorporating alternatives (a) and (b) are illustrated in Exhibits 10A and 10B, respectively. The addition of this capability would also require one additional ground command. If the maximum number of commands for the power control unit is firmly fixed at 13, as stated in Reference 3, it is recommended that commands 5 and 6 be combined so that both batteries would simultaneously be commanded to the 5-ampere charge rate. (It is anticipated that both batteries will be commanded to the 5-ampere charge rate at the same time in any event.)

Specific recommendations concerning alternatives (c) and (d) are beyond the scope of this TAM; however, the deficiencies of the present method of sensing current direction to activate the discharge control relays are discussed in subsection 3.b. It should also be noted concerning alternative (d) that, if the recommended cross-strapping of the series regulators is incorporated, the requirements for two individual bus overvoltage limiter functions will be deleted, since the battery charge bus must be limited to 34.1 volts only when both series regulators are bypassed or shorted.

(5) Failure-Switching Command Logic

The failure switching that would be effected for any combination of single battery, single charge control unit, or single series regulator failures with the recommended mechanization is summarized in Exhibit 11. It is evident that the charge buses must be connected for any type of failure, and the independent cross-strapping relay (K_{CS}) may be omitted if the series regulator failure-switching relays are utilized to perform this function, as discussed in subsections 3.a(1) and (2).

Based on the table in Exhibit 11, the logic for energizing the various failure-switching relays can be configured as illustrated in Exhibit 12,

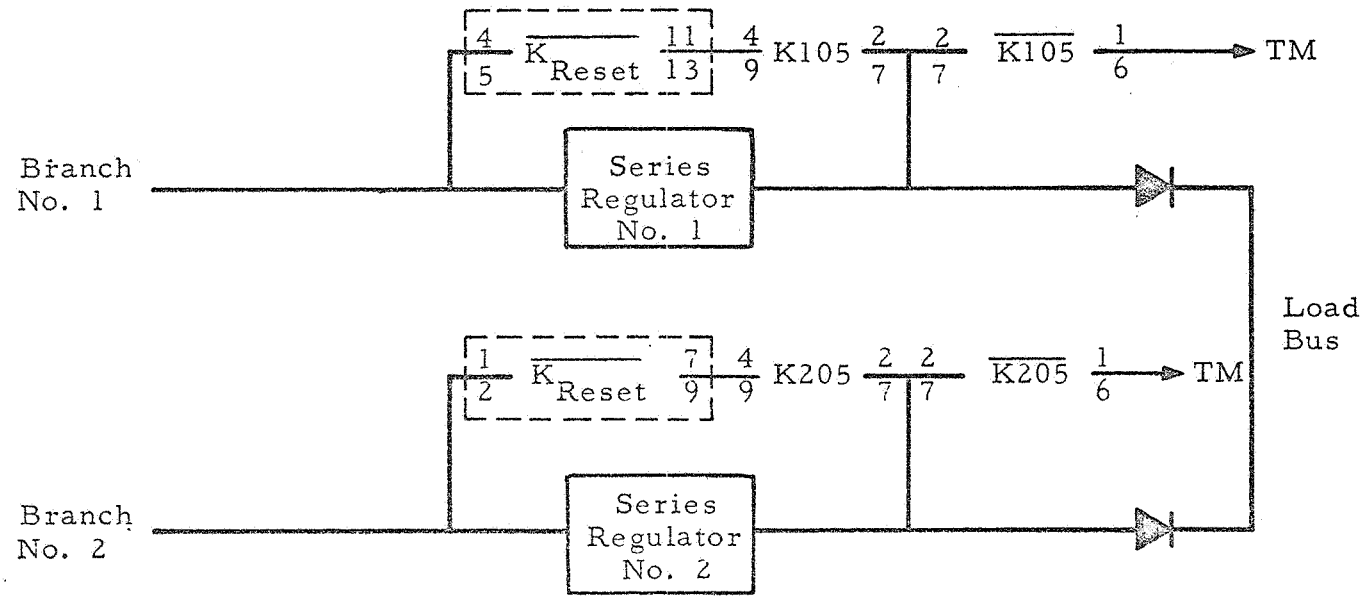


Notes: (1) Additions outlined by dashed line.

(2) Bar above relay contacts indicates closed contacts when relay is deenergized.

(3) No bar above relay contacts indicates closed contacts when relay is energized.

EXHIBIT 10A - RECOMMENDED METHOD OF RESETTING DISCHARGE CONTROL RELAYS BY GROUND COMMAND



Notes: (1) Changes outlined by dashed line.

(2) Bar above relay contacts indicates closed contacts when relay is deenergized.

(3) No bar above relay contacts indicates closed contacts when relay is energized.

EXHIBIT 10B - RECOMMENDED METHOD OF INTERRUPTING SERIES REGULATOR BYPASSES BY GROUND COMMAND

EXHIBIT 11 - RELAYS ENERGIZED BY REVISED FAILURE SWITCHING

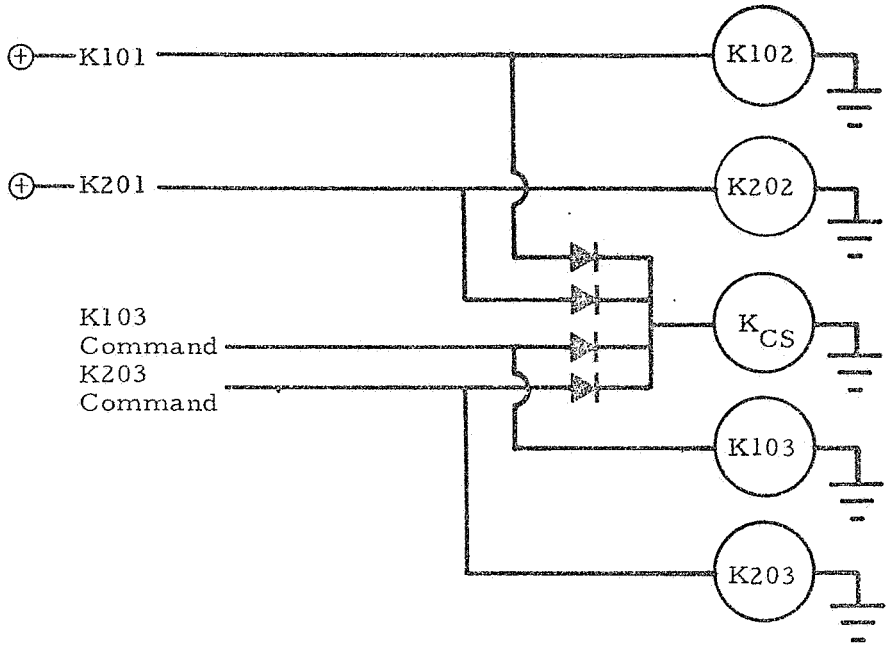
	Failure						Relays Energized							Results			
	Charge Control		Battery		Series Regulator									Connected Controlled Arrays Regulated by Charge Control	Battery Upper Charge Voltage		Controlled Array Load Current Carried by Series Regulators
	No. 1	No. 2	No. 1	No. 2	No. 1	No. 2	101 (201)	201 (202)	103	203	1	2	CS(1)		No. 1	No. 2	
1.	1	1	1	1	1	0	[+	+]				+	(+)	1 or 2	Battery of controlling branch charged normally. Captive battery charged to $E_B - V_D$.		1
2.	1	1	1	1	0	1	[+	+]			+		(+)	1 or 2			2
3.	1	x	1	0	1	1		+		+			+	1	Normal	Removed	Both
4.	1	x	1	0	1	0		+		+		+	(+)	1	Normal	Removed	1
5.	1	x	1	0	0	1		+		+	+		(+)	1	Normal	Removed	2
6.	x	1	0	1	1	1	+		+				+	2	Removed	Normal	Both
7.	x	1	0	1	1	0	+		+			+	(+)	2	Removed	Normal	1
8.	x	1	0	1	0	1	+		+		+		(+)	2	Removed	Normal	2
9.	1	0	1	1	1	1		+					+	1	Normal	$E_{B1} - V_D$	Both
10.	1	0	1	1	1	0		+				+	(+)	1	Normal	$E_{B1} - V_D$	1
11.	1	0	1	1	0	1		+					(+)	1	Normal	$E_{B1} - V_D$	2
12.	1	0	0	1	1	1		+	+				+	1	Removed	Normal(2)	Both
13.	1	0	0	1	1	0		+	+			+	(+)	1	Removed	Normal(2)	1
14.	1	0	0	1	0	1		+	+				(+)	1	Removed	Normal(2)	2
15.	0	1	1	1	1	1	+						+	2	$E_{B2} - V_D$	Normal	Both
16.	0	1	1	1	1	0	+					+	(+)	2	$E_{B2} - V_D$	Normal	1
17.	0	1	1	1	0	1	+				+		(+)	2	$E_{B2} - V_D$	Normal	2
18.	0	1	1	0	1	1	+			+			+	2	Normal(2)	Removed	Both
19.	0	1	1	0	1	0	+			+		+	(+)	2	Normal(2)	Removed	1
20.	0	1	1	0	0	1	+			+	+		(+)	2	Normal(2)	Removed	2

Notes: (1) Cross-strapping relay can be deleted if one of the series regulator switching relays is utilized to connect charge buses.

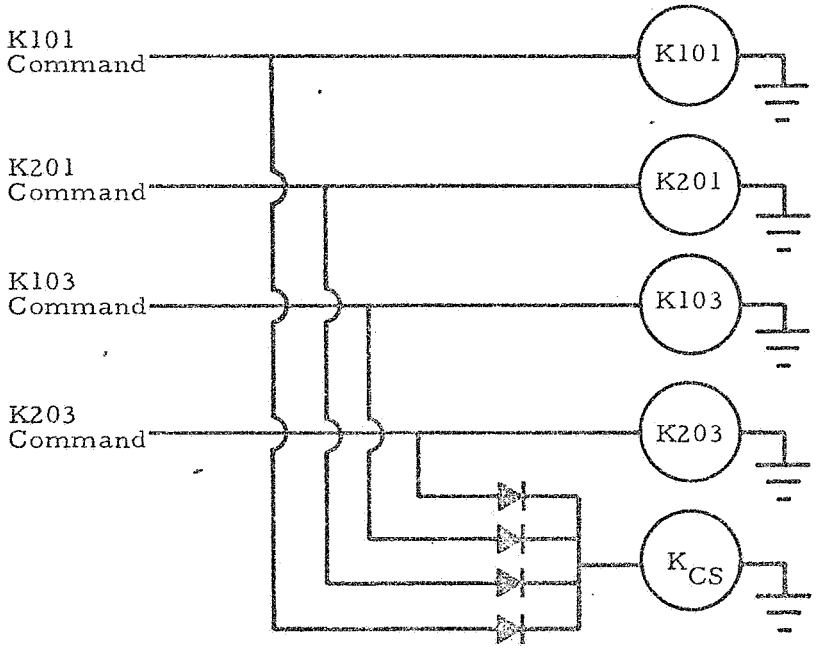
(2) Upper voltage limit depends on temperature of disconnected battery.

(3) 1 = Unit operating
0 = Unit failed
x = Status of unit does not influence failure switching
+ = Relay energized

( ) = Relay can be energized without affecting remaining failure switching
[ ] = Either relay can be energized
V_D = Voltage drop of cross-strapping diode, CR104 or CR204



(a) With Cross-Strapping Relay Added and Both K102 and K202 Retained



(b) With Cross-Strapping Relay Added and Both K102 and K202 Deleted

EXHIBIT 12 - RECOMMENDED FAILURE-SWITCHING RELAY LOGIC

depending on whether or not individual relays are retained to perform the functions of K102 and K202 (as discussed in subsection 3.a(4)). If the cross-strapping relay were not incorporated and the series regulator switching relays were utilized to connect the charge buses, the logic would also be as shown in Exhibit 12, except that the four connections to relay K_{CS} would be omitted.

b. Discharge Control Relays Logic

The discharge control relays used to bypass the series regulators are presently controlled by diverse indications; namely, they are set (series regulators bypassed) by a 300-ma discharge current from either battery and are reset (series regulators inserted) by a load bus voltage above 32.5 volts. This method has the following deficiencies:

1. Reference 4 indicates that the batteries can initially discharge at a voltage sufficient to cause load bus overvoltage. If the duration of this overvoltage condition is sufficient for the delayed load bus monitor to detect the overvoltage and attempt to reset the discharge control relays, simultaneous set and reset commands will be generated, causing an indeterminate relay condition. Simultaneous set and reset commands may also be generated because of imbalance between the two channels if, under heavy load current demand, one of the batteries indicates a discharge condition while the solar array is still in sunlight.

2. Voltage transients occur because the series regulators are saturated at 31.5 volts but are not inserted into the circuit until the load bus voltage is above 32.5 volts.

As suggested in Reference 4, it is recommended that the discharge control relays logic be controlled only by load bus voltage for both charge and discharge, and that the series regulators be inserted at a voltage below their saturated level. Also, as pointed out in subsection 3.a(5), because of the low battery capacity available when a failure causes the discharge control relays to remain energized, redundancy should be incorporated into the control logic to increase its reliability.

c. Circuit Design Reliability

During the review of the power control unit, each circuit was examined to determine if the design was based on sound reliability

practice. Cases in which increased reliability could be effected by circuit changes without degrading functional operation are discussed below.

(1) Parallel Transistors

Two 2N2124 power transistors are connected in parallel in each series regulator unit to provide the voltage drop between the battery charge bus and the load bus. A check of the specification for this type of transistor shows that it is rated at 250 watts and 30 amperes. Even if one series regulator were failed, the load current requirement would not approach the maximum rating of the transistor, and a single transistor would be sufficient. Therefore, the question of whether a single transistor or parallel transistors should be used can only be answered by determining the consequences of a given failure (short or open) and the means of circumventing the failure by the available cross-strapping provisions.

Obviously, for the series regulator unit, the probability of short is higher and the probability of open is lower for the parallel transistors than for a single transistor. With the present switching provisions, a shorted series regulator presents the greatest subsystem degradation, since one battery could only be charged to 25 percent of capacity and no failure switching can be performed; however, an open series regulator can be circumvented by connecting the charge buses via K101 and K102 (or K201 and K202). Therefore, if no additional failure switching is incorporated to remove a shorted series regulator, it is recommended that a single 2N2124 transistor be used to minimize the probability of a shorted series regulator.

On the other hand, if the recommended provisions to remove completely and cross-strap the series regulators are incorporated, the choice of a single or parallel transistor is dependent on the relative short and open failure rates, since either type of failure will have the same effect on subsystem operation (i.e., the failed series regulator will be switched out).

Letting P_s be the probability of transistor short and P_o the probability of transistor open, the probability of successful operation for a

single transistor is $1 - P_s - P_o$ while the probability of successful operation for the paralleled transistors is $(1 - P_s - P_o)^2 + 2P_o(1 - P_s - P_o)$.

Equating the two expressions and solving indicates that a single transistor would give the highest probability of series regulator operation (neither shorted or open) if $P_s > P_o$.

(2) Series Diodes

Two series diodes, rather than a single diode, are used in several circuit applications. Discussion with STL personnel indicates that this practice was followed because the ratio of diode shorts to opens was considered to be approximately three to one. In circuit applications where an open failure would cause more serious subsystem degradation than a short, however, it is contended that a single diode should be used. In particular, the functions of diodes CR8 and CR9 in the discharge control relay reset circuit and diodes CR15 and CR16 in the cycle relay driver circuits are to provide the delay of their associated Miller integrator circuits. In these instances, if a coupling diode circuit (single or dual) were to short, the time delay would be lost and the circuit operation would be more susceptible to transients; however, if the coupling diode circuit were to open in either circuit, the discharge control relays would be continuously "reset" or the associated cycle relay would be continuously energized. Since, in either case, the consequences of the open circuit failures would result in a more severely degraded consequence than if the time delay were lost, it is recommended that a single diode (or a parallel pair) be used in these applications.

(3) Current-Limiting Resistors

Parallel, 200-ohm, current-limiting resistors are used in the relay driver stages of the discharge control relay set (R19 and R20) and the discharge control relay reset (R17 and R18) circuits to reduce the power dissipation of the output transistor; however, only one 100-ohm, current-limiting resistor (R65) is used in the output stage of each cycle relay driver. Obviously, for the parallel resistors

the probability of shorting is higher and the probability of opening is lower than for a single resistor. Discussion with STL personnel indicates that, if the current-limiting function were eliminated because one of the two parallel resistors shorted, the power dissipation of the output transistors would still be well below their rated values and the circuit would continue to function satisfactorily. On the other hand, if the collector circuit were opened, such as would be the case if R65 opened, the associated cycle relay could not be energized to remove the battery from charge in the extended sunlight period. Since the consequence of an opened resistor (i.e., open transistor collector connection) is more severe than that of a shorted resistor in these cases, it is recommended that R65 be replaced by two parallel 200-ohm resistors.

(4) Extraneous Components

(a) Discharge Control Relays Reset

The relay driver stage of the discharge control relay reset circuit utilizes two series transistors (Q14 and Q15). Although this method prevents a single shorted transistor from causing a continuous reset signal, it requires the addition of three components to the circuit (R21, CR11, and Q14) and increases the probability of not resetting the relays.

The question of whether the single transistor (Q15) or the two transistors (Q14 and Q15), plus the additional diode and resistor, should be used depends on the consequences of the two types of failure and their probabilities of occurrence. If the circuit in question is open and the relays are not reset, both series regulators will be continuously bypassed and both batteries (or a single battery) can be charged to only 25 percent of capacity.[1] If the circuit is shorted, a continuous reset signal will be generated, causing the position of the relays to be indeterminate; thus the series regulators may not be bypassed during battery discharge, increasing the power drained from the batteries. Although it is recognized that the increased power dissipated across the

[1] This condition can be circumvented if a ground-commanded discharge control relay override is incorporated, as recommended in subsection 3.a(4).

series regulators if they were not bypassed during battery discharge would jeopardize mission success, it is PRC's contention that the continuously bypassed series regulator represents the more severely degraded consequence. Therefore, it is recommended[1] that components R21, CR11, and Q14 be removed from the discharge control relay reset driver and that the output stage be configured identically to those of the cycle relay drivers.

(b) 10-Ampere Charge Rate Commands

Components R18 and Q6 in each battery current regulator are used to accept the 10-ampere rate command and to insert shunting resistor R17 to ground. These two components increase both the probability of inadvertently increasing the commanded current amplitude by a 5-ampere increment (if Q6 shorts) and the probability of not being able to command the additional 5-ampere increment when desired (if Q6 or R18 opens). Correspondence from STL indicates that the spacecraft cabling from the CDU to the power control unit would have to be revised to provide two leads for satisfactory isolation of the two branches. Therefore, it is recommended that a single ground signal be sent to the power control unit when the 10-ampere rate is desired and that R17 of each branch be directly connected to this ground through isolating diodes.

4. SUMMARY

BASED ON THE "SYSTEM-LEVEL" ANALYSIS OF THE OGO S-50 POWER SUPPLY SUBSYSTEM, THE CHANGES AND/OR INVESTIGATIONS LISTED BELOW ARE RECOMMENDED.

a. REVISION OF THE FAILURE-SWITCHING PROVISIONS, AS ILLUSTRATED IN EXHIBIT 9, TO PROVIDE:

(1) SERIES REGULATOR CROSS-STRAPPING AND ELIMINATION OF THE LOAD BUS OVERVOLTAGE RELAYS.

[1] As discussed in subsection 3.b, it is also recommended that the logic for controlling the discharge control relays be investigated and made more redundant.

(2) CHARGE CONTROL OF BOTH BATTERIES BY ONE CYCLE RELAY IN THE CYCLE CHARGE MODE WHEN THE CHARGE BUSES ARE CROSS-STRAPPED.

(3) UTILIZATION OF THE CHARGE CONTROL FAILURE-SWITCHING RELAYS TO PERFORM THE FUNCTIONS OF K102 AND K202.

b. INCORPORATION OF A GROUND-COMMANDED OVERRIDE OF THE DISCHARGE CONTROL RELAYS, AS ILLUSTRATED IN EXHIBITS 10A AND 10B, OR INCREASED REDUNDANCY IN THE CONTROLLING LOGIC.

c. REVISION OF THE DISCHARGE CONTROL RELAYS LOGIC TO OPERATE ON LOAD BUS VOLTAGE SENSE FOR BOTH CHARGE AND DISCHARGE CONDITIONS.

d. INCORPORATION OF THE FOLLOWING CIRCUIT REVISIONS:

(1) ELIMINATION OF ONE OF THE PARALLEL OUTPUT POWER TRANSISTORS IN EACH SERIES REGULATOR.

(2) ELIMINATION OF ONE OF THE SERIES DIODES IN THE DISCHARGE CONTROL RELAY RESET CIRCUIT AND IN THE CYCLE RELAY DRIVER CIRCUITS.

(3) USE OF TWO PARALLEL, 200-OHM, CURRENT-LIMITING RESISTORS IN THE OUTPUT STAGE OF EACH CYCLE RELAY DRIVER.

(4) ELIMINATION OF R21, CR11, AND Q14 IN THE OUTPUT STAGE OF THE DISCHARGE CONTROL RELAY RESET CIRCUIT.

(5) UTILIZATION OF THE 10-AMPERE CHARGE CURRENT COMMAND TO GROUND R17 DIRECTLY THROUGH ISOLATING DIODES IN THE BATTERY CURRENT REGULATOR.

REFERENCES

1. Engineering Data for Design Review No. 3, OGO S-50 Power Control Unit. Space Technology Laboratories, 6 April 1964.

2. Schematic Diagram, Power Control Unit S-50. Drawing No. S214250U. Space Technology Laboratories, 9 March 1964.

3. Power Control Unit, OGO S-50 Configuration. Specification No. D-13484. Space Technology Laboratories, 6 April 1964.

4. A Brief Study of the OGO Silver Cadmium Power Subsystem. Interoffice Correspondence No. 9361.2-100. Space Technology Laboratories, 8 January 1964.

TECHNICAL ADVISEMENT MEMORANDUM NO. 34-28

USE OF INTEGRATED CIRCUITS FOR INCREASED SYSTEM RELIABILITY

PRC D-821

7 August 1964

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Approved by

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TECHNICAL ADVISEMENT MEMORANDUM NO. 34-28

To: Assistant OGO Project Manager, GSFC, NASA

From: PRC OGO Reliability Assessment Team

Subject: Use of Integrated Circuits for Increased System Reliability

1. Introduction

PRC has for some time been keeping track of developments in the field of integrated circuits. This attention has been devoted primarily to the area of reliability, taking into account such necessary additional factors as power dissipation, availability, and--contingent on the latter--cost. Because of the unusual complexity of OGO, resulting in a very low probability of success (as determined in PRC's fourth OGO reliability assessment), PRC presently feels that the use of integrated circuits should be given detailed consideration. Whereas PRC has previously made recommendations concerning the use of Minuteman-type discrete component parts in addition to parameter-drift screening, at this time it is felt that integrated circuits could provide significant gains in reliability at not too unreasonable a cost. The remainder of this TAM provides, for further consideration by GSFC, the more important facts that led PRC to the preceding conclusion.

2. Terminology

As the first point, it is important to clarify terminology. The terminology of microelectronics is in a general state of confusion. For the purpose of this TAM, however, it is only necessary to make clear the relationships among some of the often-used terms. That is, microelectronics can be considered as encompassing microminiaturization accomplished with discrete microminiature component parts or with integrated circuits. With discrete component parts, either a uniform geometry (e.g., pellets) or a random geometry (e.g, cordwood) is used. A large amount, if not all, of OGO presently makes use of the latter.

3. Technological Development Trends

With integrated circuits, either semiconductor circuits or thin-film circuits are used. There are thus two major areas of technological development in the area of integrated circuits. Thin films represent a two-dimensional approach to the physical realization of electronic elements in the form of thin films deposited in a patterned relationship on a structural supporting material. A significant advantage of thin film is that large groups of high-quality, close-tolerance, passive components and connections can be produced in one batch with a very small number of operations and materials. However, although thin-film active components have been developed using such techniques, this has not been until recently (and at great expense). Practical thin-film active components are still considered to be in the laboratory stage. Because of this, many thin-film circuits use individually attached active semiconductor devices. This total circuit, as well as other combined types, is then referred to as a hybrid (integrated) circuit.

The semiconductor integrated circuit technology is a three-dimensional approach to the physical realization of electronic elements using the bulk and junction properties of semiconductor technology to produce transistor-diode functions and wide-tolerance passive component functions inseparably associated on or within a continuous body of semiconductor material. Transistor and diode functions are stressed; however, although passive functions are limited, they are still more than satisfactory, particularly in digital circuits.

Thus, the most pronounced trend presently encountered in electronic development is the integral fabrication of many components together with their necessary interconnections for specific circuit configurations. Initially, the prime interest in microelectronics stemmed from the fantastic volume and weight reductions. This was true of the discrete component part approach, with reliability and cost remaining about the same as with any other discrete part approach. While volume and weight reductions are significant, these benefits are rapidly being overshadowed by the fact that integrated circuit techniques should ultimately lead to higher reliability and lower cost. Reliability is increased

and cost is saved by the use of systematic production techniques, elimination of assembly operations, and a marked reduction of interconnections (discrete joints).

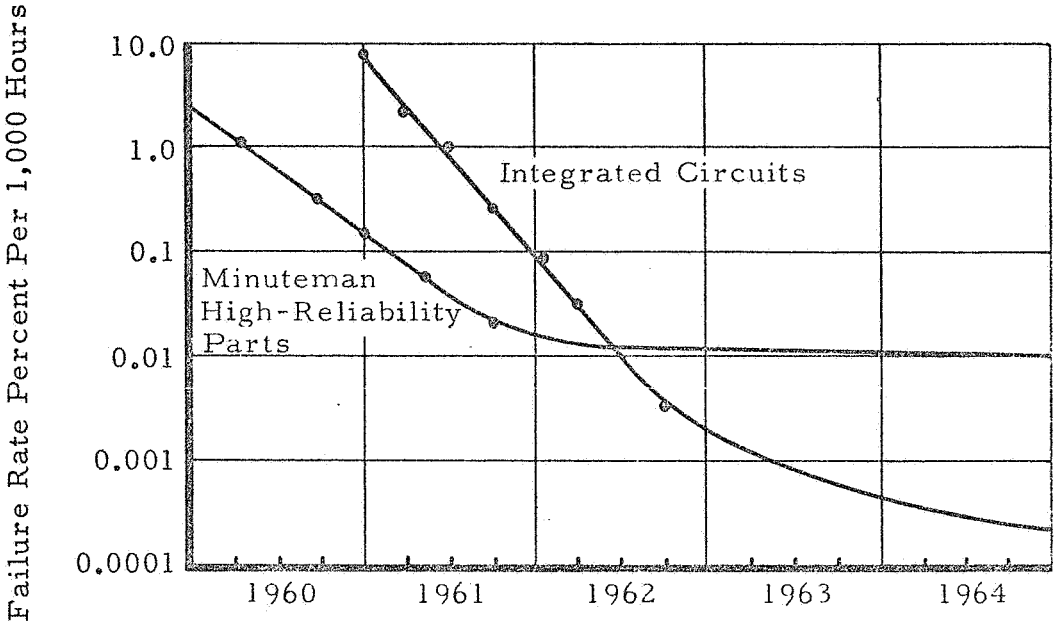
The important subject of reliability will be discussed in detail later in this TAM. At this time it should suffice to say that the reliability advantage of integrated circuits is largely unproven. Confidence has been expressed in their potential reliability, however, by their application in Advanced Minuteman, Polaris, Saturn, and Apollo. Their use in Minuteman is "based on expectations that they will be 10 to 100 times more reliable than the circuits used in the current Minuteman."[1] (See Exhibit 1.) There are several reasons for the fact that the reliability is largely unproven. Some of the most important reasons are interrelated. These include the fact that not enough hours of use have been accumulated to determine reliability and that the cost and impracticability of accelerated life-testing of statistically large numbers of circuits is unreasonable. However, data is being made available by at least the major integrated circuit vendors on their in-house testing. From this the user is able to draw his own conclusions. It is from such data, along with data from other sources, that PRC has made a preliminary investigation, the results of which will be described later in this TAM. First, however, there are other factors that must be considered in relation to OGO alone.

4. Application to OGO

When undertaking the development of an electronic system from the conceptual level, there are several alternative approaches for using integrated circuits. These approaches can be categorized as making use of (1) standard circuits, (2) custom circuits, or (3) something in between. The Signetics Corporation refers to the latter as customized circuits, and since this seems to be an appropriate term it will be used hereafter in this TAM. The standard circuits represent off-the-shelf integrated circuits produced to a set of specifications developed by the vendor.

[1] Donald Christiansen, "EEE-Specifying Guide, Microelectronics '63," Electronic Equipment Engineering, November 1963, pp. 38-51.

EXHIBIT 1 - RELIABILITY GROWTH CURVE[1]



[1] Ibid. (Fig. 1), p. 42, citing G. H. Smith, Future of On-Board Computers for Space Vehicles, Autonetics Technical Paper, June 1963. "Reliability growth curve compares integrated circuits of the form selected for Improved Minuteman against identical circuits using Minuteman high-reliability components. Data were obtained from accelerated life test measurements . . ."

Custom circuits are produced to the buyer's unique specifications, while customized circuits are designed to a buyer's specification which, in turn, must be based on a configuration of integrated circuit components already being used by the vendor for either of the other categories of circuits.

As is frequently the case in electronics, digital circuits and linear circuits require separate considerations. The most progress has been made in integrated digital circuits, and, because of the large amount of complex digital circuitry aboard OGO, attention has been directed toward this area. Even at this point, choices remain as to the particular logic to use--direct-coupled transistor logic (DCTL), resistor-transistor logic (RTL), resistor-capacitor-transistor logic (RCTL), transistor-coupled transistor logic (TTL or T^2L), diode-transistor logic (DTL), emitter-coupled transistor logic (ECTL), etc.--for the digital integrated circuits. Exhibit 2, taken from an article by Alex E. Skoures,[1] is a table listing typical worst-case operating conditions for some of the logic types. (It should be noted that this table was taken directly from the previously referenced article and that the entries for the TTL logic were misprinted in the original article. It would seem reasonable to assume that the measurements were taken at a temperature of 55° C, not -55° C.) The results of this systematic study by Skoures at the U.S. Naval Air Development Center, Johnsville, Pennsylvania, generally indicate that none of the logic types is inherently superior, although each has its advantages and its disadvantages. However, several factors require consideration in choosing a logic type for a particular application. These factors, taken from the article by Skoures, are summarized in Exhibit 3. It should be noted that these factors are not necessarily to be considered in the same manner for the preliminary design of a system and for an already designed system such as OGO. For example, OGO has been designed using a-c coupled flip-flops and therefore only requires--and uses--a single-phase clock system. The use of logic without such flip-flops would require a

[1] Skoures, "Choosing Logic for Microelectronics," Electronics, October 4, 1963, pp. 23-26.

EXHIBIT 2 - TYPICAL WORST-CASE CONDITIONS FOR LOGIC GATE TYPES

RTL Gate: T = 125 C. Fan-out (N) = 4. f = 1 Mc.

Propagation delay (T_{pd}) = 40 ns. Rise time (T_r) = 15 ns.

Fall time (T_f) = 22 ns.

Power dissipation (P_d) = 15 mw per gate and 15 mw per shift register.

RCTL Gate: T = 125 C. N = 5. V_{cc} = 3 v. f = 0.1 Mc.

T_{pd} = 200 ns. T_r = 0.3 μsec. T_f = 1.4 μsec.

P_d = (for V_{cc} = 3 v) 3 mw per gate and (for V_{cc} = 6 v) 7 mw per shift register.

DTL Gate: T = 125 C. V_{cc} = 5 v. N = 4. f = 7 Mc.

T_{pd} = 42 ns. T_r = 39 ns. T_f = 56 ns.

P_d = 6 mw per gate and 23 mw per shift register.

TTL Gate: T = -55 C. V_{cc} = 4. f = 5 Mc.

T_{pd} = 55 C. V_{cc} = 4. f = 5 Mc.

T_{pd} = 90 ns. T_r = 13 ns. T_f = 15 ns.

P_d = 12 mw per gate and 60 mw per shift register.

EXHIBIT 3 - FACTORS TO CONSIDER IN CHOOSING A LOGIC SYSTEM

Logic Capability--Fan-in; inversion capability; availability of both normal and complemented outputs

Maximum Fan-Out--Number of loads which the logic element supplies

Maximum Frequency of Operation--Determined by rise, fall, delay, storage, and recovery times

Packing Density--Power dissipation, operating temperature, heat sink temperature

Isolation--Signal propagation between channels of the same circuit

Directionality--Degree of signal propagation from output to input

Interconnection Interaction--Signal propagation from one line to another

Limiting--Restandardization of the signal extremities corresponding to logical one or zero

Threshold Level--Limits at which circuit amplifies information but rejects certain noise signals

Stability--Degree of freedom from errors resulting from regeneration within a circuit

Signal Amplitude--Minimum limits of signal level used to communicate from one circuit to another

two-phase clock and many more circuits. However, in a more detailed study of the use of integrated circuits for OGO, the use of direct-coupled logic should not be ignored.

With respect to OGO as a specific system (and in view of the preliminary nature of the effort reported herein), the factors that must be considered are somewhat simplified. That is, an already designed and tested system is inherently unreliable. In what way can reliability be improved most for the money? PRC feels that, although this question can only be definitely answered by further study, integrated circuits offer great promise. In order to reach this conclusion it was necessary to consider some specific factors.

First, what type of integrated circuits (custom, customized, or standard) would be best for OGO? The standard types, if they will perform as required for OGO, are the cheapest and should therefore be considered first. Circuits at the interfaces between integrated and non-integrated circuits would have to be redesigned. These interface circuits could be custom, or possibly customized, integrated circuits, either of which would be more expensive than standard integrated circuits. Of course, these interface circuits could be of the discrete component type at less cost and less reliability. Regardless of the final decision as to the interface circuits, there is little question that the power converters would have to be redesigned, since integrated circuits generally operate at lower voltages.

In the preceding paragraph, the use of standard integrated circuits was predicated on whether they will perform as required for OGO. It appears that the additional factors of concern in these preliminary considerations are operating frequency, environmental operating characteristics, power dissipation, noise immunity, and fan-out.

The highest frequency in the digital areas of OGO is 256 kbps. In general this is slow for integrated circuits, and is therefore no restriction whatsoever. As a matter of fact, the slow speed is advantageous with respect to power dissipation. This will be mentioned further in a later paragraph. As for environmental operating characteristics, integrated circuits generally meet the same conditions as transistors presently being

used on OGO. For example, one standard line of integrated circuits has all test procedures conforming to MIL-M-23700, MIL-S-19500, or MIL-STD-750 and sampling procedures per MIL-M-23700 or MIL-S-19500.

Power dissipation, noise immunity, speed (operating frequency), and fan-out are interrelated. For a particular choice of logic type, higher speed calls for more power. Thus the low operating frequency of OGO digital equipment indicates promise for low power dissipation. However, it appears that standard circuits designed to operate at this low frequency (and hence low power dissipation) are not available at this time. This could not be determined for certain during the course of this investigation, but this does not necessarily matter, since power dissipation may not be excessive with 1-mbps circuits.

To determine the actual difference in power requirements for an integrated circuit version of OGO equipment is difficult and not particularly meaningful at this level of consideration. Some of the numerous reasons for this are as follows: First, the choice of standard integrated circuits for such a comparison would have to be arbitrary, since this short investigation could not possibly allow justification of the selection of any particular line of integrated circuits. In addition, the various standard integrated circuits have been designed with different types of logic. This, along with other factors, has resulted in varying fan-out (load driving) capabilities. Therefore, an OGO flip-flop could not generally be replaced by an integrated circuit flip-flop because, whereas the OGO flip-flop may be able to drive 10 discrete component gates, the integrated circuit flip-flop could only drive 3 or 4 or even 8 integrated circuit gates. Thus, the OGO circuit would have to be replaced by at least two and maybe more (a flip-flop and one or more drivers) integrated circuits. However, for information, a look is taken at the problem in conjunction with costs, following further discussion of noise immunity.

The practical concern with respect to noise is whether it will cause false triggering of storage elements. The use of microcircuitry, particularly integrated circuits, has been accompanied by renewed interest in this subject of noise immunity. There are two primary reasons for the

concern. There has been a large increase in the operating frequency of integrated circuits, and the decrease in system size brings signal lines, power lines, and ground lines into closer proximity with each other. Since cross-coupling between these lines is proportional to the speed of the transitions on the lines and their proximity to each other, it is not unusual to expect that noise problems will be greater than observed in the past for systems made of discrete components. The noise problem must not be overlooked, or the advantages of integrated circuitry may fail to provide systems that operate without error.

The various logic types generally have different noise immunities. In addition, for the same logic type, increased noise immunity requires (among other things) more power, but lower operating frequencies. That is, a high-frequency, highly noise-immune circuit requires more power than if either frequency or noise immunity were low. The OGO digital circuits are generally low-power with high noise immunity by virtue of the use of diode-transistor logic (DTL) at low operating frequencies.

Since DTL is available from Motorola (and Signetics) in standard integrated circuits, including a-c coupled flip-flops as used on OGO, it is informative to make a comparison with at least one of the present OGO circuits. The OGO FF-2 dissipates 30 mw with a fan-out of 22. A Motorola MC209 (Signetics SE124) flip-flop (integrated, of course) will operate up to a frequency of 10 mc with a fan-out of 8 and power dissipation of 16 mw. Using three MC202's (SE102's) as drivers, a total drive capability of 20 can be obtained with a total dissipation of 16 + (3 x 8.5) = 41.5 mw. Considering the fact that the power dissipation is about 10 percent greater for about 10 percent less fan-out, a quick look was taken at the OGO Tab Run Loading Study to determine if a fan-out of 22 is actually required. It appeared that only seven flip-flops were required to have a fan-out greater than 16. For a fan-out of 16 or less, integrated circuits could be obtained using two MC202's (SE102's) with a dissipation of 16 + (2 x 8.5) = 33 mw maximum. Thus it can be seen, from the point of view of power dissipation versus fan-out, that integrated circuits appear adequate enough to deserve further detailed consideration. All of the gating and logic needs to be studied before a definite statement can

be made as to whether integrated circuits will perform as required for OGO.

It should be clear at this point that costs can only be considered in a very superficial manner. If the cost of present OGO modules were available to PRC, there would be some basis for comparison. To make an estimate of the cost of the presently used modules by counting components and pricing them in quantity would not be adequate, since such costs would not be of much use without the module assembly costs and the one-time redesign costs involved with using integrated circuits. In addition, only when an exact determination of performance requirements is made will the total number of integrated circuits required be known for a useful cost comparison. This is especially important because integrated circuits show greatest advantages in large numbers--particularly custom circuits where initial costs are high and must be amortized over a large number of circuits. Since the average unit cost reduces with increased quantities, the real significance of cost versus reliability requires more detailed consideration.

Another cost versus reliability factor is the package style. It is recommended that adequate consideration be given to the flat package. The reason for this is that a large amount of developmental work is being done to eliminate the fine wires that presently connect the monolithic circuit die to the external leads in both the flat and TO-5 type packages. At present these wires are generally stitch-bonded. Their elimination will eliminate the labor cost of bonding, thereby reducing the unit cost. In addition, this method would eliminate a potential source of circuit failures.

To compare the reliability of an integrated circuit flip-flop with a discrete component flip-flop is not reasonable because there is not a one-for-one replacement ratio. As pointed out earlier, it could take up to four circuits for replacement. However, an indication of the reliability improvement that can be made can be shown by the following: In the DDHA and LFTA there are, respectively, 59 and 71 discrete component flip-flops. Replacing all but 7 (those requiring a fan-out of 22) by integrated circuits equivalent to one Signetics type SE124 and two

SE102's, the probability of no failures can be improved roughly from 0.01 to 0.58 for the remaining 123 flip-flops.

5. Reliability

Of the many apparent advantages of integrated circuitry, really significant increases in achievable reliability may prove to be the greatest. Important advancements in the reliability of discrete components have taken place with rapidity in recent years. One problem, however, exists with discrete components that seems impossible to eliminate. The problem is that a discrete component circuit, by its very nature, requires a large amount of discrete connections and a large number of handling and assembly operations. It is this factor which effectively tends to limit the ultimate reliability achievable with discrete components.

In this regard, integrated circuits have three significant advantages from the outset. These are (1) fewer interconnections, (2) process-dependent fabrication steps rather than human assembly, and (3) processing controlled by one manufacturer. In addition to the reduction in numbers of interconnections, integrated circuits also offer distinctly different types of interconnections. Discrete components require that the interconnections be formed by placing dissimilar materials in physical contact and brazing, welding, or soldering them together. In integrated circuits, however, the interconnections are achieved either by depositing the dissimilar materials directly on one another or by using the same piece of material actually to form different circuit elements. The interconnections required in integrated circuits then involve close molecular association between materials or elements, and, thereby, are inherently very reliable. An additional advantage is very small circuit mass, which naturally improves inherent resistance to vibration and shock damage.

At this point in time, significant amounts of data concerning the reliability of integrated circuitry are still difficult to locate. It is gratifying, however, to note that most manufacturers are making the data freely available from their testing operations as it is compiled. This fact in itself speaks well for the reliability of integrated circuits. Of the various data collected, probably the most interesting is that recently

released by the Navy concerning operational data on three equipments utilizing integrated circuits. The equipments involved are (1) two automatic Loran-C receivers, (2) a Pathfinder electronic countermeasures receiver, and (3) an AN/ASW-21 one-way data link. The two Loran receivers employ 1,480 integrated circuits each (with converters), and the other two devices utilize 160 and 125 integrated circuits, respectively. These four items have thus far compiled 5,765,250 integrated-circuit operating hours, 224,800 of which were actual flight operating hours. During this time only one failure has occurred, and the propriety of charging it to the integrated circuits is dubious since there is some feeling that the circuit was defective prior to installation, but that testing, because of a hurried time schedule, was insufficient to catch it. Assuming, however, that this one failure is chargeable, the resulting failure rate is 0.1735 failures per 10^6 hours for an average integrated circuit. In very general terms, each of these circuits probably represents replacement of a discrete component circuit which would exhibit a total failure rate of at least 10 times that failure rate or greater. This one body of data represents the most significant proof of the high reliability expectations for integrated circuitry that has come to PRC's attention to date.

Other data compiled from manufacturers' tests of separate circuits has been analyzed, with the following results: Failure rates, computed from various groups of test data, range from 5.34 failures per 10^6 integrated-circuit hours (4.10 per active element) for circuits tested at 125° C for an approximate average of 3,000 hours to 0.084 failures per 10^6 integrated-circuit hours (0.028 per active element) for 1,271 circuits tested for more than 9,000 hours each at 125° C. The manufacturer of the first group reports data resulting in a failure-rate estimate of 0.37 failures per 10^6 integrated-circuit hours for circuits tested at 25° C, and the manufacturer of the second group reports compiled data for testing at 125° C which results in 0.15 failures per 10^6 integrated-circuit hours, with each circuit tested for more than 8,700 hours and approximately 10 percent tested for more than 14,500 hours each. It is appropriate to note that the data for the second group in both of the above cases outnumbers that for the first group by approximately three times, both in test hours per circuit and in number of circuits tested.

From this review of data, it is appropriate to conclude that the failure rates of integrated circuits are at least 10 times less than those of similar discrete component circuits. An appropriate average semiconductor integrated-circuit failure rate for preliminary use is 0.15 to 0.2 failures per 10^6 integrated-circuit hours.

6. SUMMARY

THE PURPOSE OF THIS TAM IS TO MAKE A PRELIMINARY INVESTIGATION INTO THE POSSIBILITY OF USING INTEGRATED CIRCUITRY IN PORTIONS OF OGO IN AN EFFORT TO INCREASE THE RELIABILITY OF THE SPACECRAFT. THE CONCLUSIONS DRAWN ARE AS FOLLOWS:

a. THE USE OF INTEGRATED CIRCUITS IN SOME PORTIONS OF OGO (ESPECIALLY THE DIGITAL EQUIPMENT) IS FEASIBLE WITHOUT NECESSITATING BASIC LOGIC REDESIGN.

b. DIRECT SUBSTITUTION OF OFF-THE-SHELF INTEGRATED CIRCUITS ON A ONE-TO-ONE BASIS PROBABLY IS NOT POSSIBLE, BUT SUBSTITUTION ON A BASIS OF TWO OR THREE STANDARD INTEGRATED CIRCUITS FOR ONE DISCRETE COMPONENT CIRCUIT APPEARS TO BE FEASIBLE, WITH THE USE OF SOME CUSTOMIZED CIRCUITS IN INTERFACE AREAS.

c. INSOFAR AS IS REVEALED BY THIS PRELIMINARY INVESTIGATION, IT APPEARS THAT POWER CONSUMPTION WILL NOT BE A SERIOUS PROBLEM.

d. NOISE SUSCEPTIBILITY, BECAUSE OF THE CLOSER PROXIMITY OF LEADS AND HIGHER SWITCHING SPEED OF THE INTEGRATED CIRCUITRY, WILL REQUIRE CARE IN DESIGN. THE SCOPE OF THIS INVESTIGATION DID NOT ALLOW A DETAILED DETERMINATION OF THE EXTENT OF THIS PROGRAM.

e. RELATIVE COST COULD NOT BE DETERMINED; HOWEVER, THERE IS REASON TO BELIEVE THAT THE BENEFITS WOULD OUTWEIGH THE COST.

f. THE POSSIBILITY OF SIGNIFICANT INCREASES (POSSIBLY ORDERS OF MAGNITUDE) IN RELIABILITY HAS BEEN DEFINITELY DETERMINED TO EXIST.

g. THE USE OF INTEGRATED CIRCUITRY IN OGO HAS NOT BEEN RULED OUT BY ANY OF THE CONCLUSIONS OF THIS INVESTIGATION, AND THE POSSIBILITY OF NUMEROUS ADVANTAGES--INCLUDING INCREASED RELIABILITY AND REDUCED WEIGHT--MAKES IT DESIRABLE THAT A THOROUGH AND DETAILED ANALYSIS OF THE USE OF INTEGRATED CIRCUITS IN SPECIFIC AREAS OF OGO BE CARRIED OUT AS SOON AS POSSIBLE.

TECHNICAL ADVISEMENT MEMORANDUM NO. 34-29

ASSESSMENT OF THE OGO S-50 POWER SUPPLY SUBSYSTEM

PRC D-841

31 August 1964

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TECHNICAL ADVISEMEMT MEMORANDUM NO. 34-29

To: Assistant OGO Project Manager, GSFC, NASA

From: PRC OGO Reliability Assessment Team

Subject: Assessment of the OGO S-50 Power Supply Subsystem

1. System Description and Mission Profile

A complete description of the OGO S-50 Power Supply Subsystem was given in a previous Technical Advisement Memorandum, TAM No. 34-27[1]; however, this description, although useful, is not essential to understanding the following discussion.

The S-50 (POGO) mission profile is characterized by alternating eclipse and sunlight seasons. The eclipse season, as defined here, includes all orbits during which the satellite is in eclipse for some portion of the orbit. The sunlight season includes all complete orbits for which the satellite is not eclipsed. The Power Supply Subsystem is capable of operating in two distinct modes, which correspond to the two seasons. In the eclipse season, the normal mode is the continuous charge mode; in the sunlight season, it is the cycle charge mode. These two modes of operation are necessary so that the batteries will have sufficient power when they are required in the eclipse season, and are not overcharged when they are not required in the sunlight season.

The reliability of the Power Supply Subsystem can be defined as the probability that it will successfully operate in each mode when required and for the length of time required. So that these probabilities can be numerically evaluated, a specific mission profile is defined. However, since the mission profile is a function of launch date, it is practically impossible, owing to slipped schedules, inclement weather, etc., to make precise specifications before launch. Hence, for purposes

[1] PRC D-818, Preliminary Review of OGO S-50 Power Control Unit, Technical Advisement Memorandum No. 34-27, 16 July 1964.

of this assessment, a launch date of 3.0 hours (U.T.), 16 March 1965,[1] has been assumed, although selection of other launch dates would not greatly alter the results of the assessment. Exhibit 1 shows the details of the mission profile pertinent to this numerical assessment. The additional factor of 800 hours shown on the exhibit is used to account for the accelerated failure rates anticipated during the launch portion of the mission.[2]

2. General Approach

The usual approach in deriving a reliability expression for a particular equipment configuration is to draw a reliability block diagram relating the various components to each other as a function of their failure effects. Generally, this diagram consists of a number of series and/or parallel units, from which well-known reliability expressions can be written as a function of tabulated part failure rates and time. This is essentially the procedure followed here.

However, the effects of many of the component part failures in this subsystem are not immediately clear. Therefore, a complete[3] first-order failure analysis was performed to clarify the various failure effects. This analysis consisted of determining the initial result of the failure of each individual part in either its short or open mode, assuming that all other parts operate satisfactorily.[4] Exhibits 2 and 3 summarize the results of this analysis.

The first column of Exhibit 2 lists the various subunits, in accordance with TAM No. 34-27. The second column, taken from STL's schematic

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[1] POGO Launch Window Study, Martin-Marietta Corporation, Baltimore, Maryland, June 1963.

[2] PRC R-309, Third Reliability Assessment for the Orbiting Geophysical Observatories, 15 April 1963, pp. 11-23.

[3] The solar arrays, batteries, capacitor quad, and the 2461-cps synchronous oscillator were considered separately. (See pp. 33-35.)

[4] In cases where it was evident that a particular failure of one part would cause failure of another part or parts, the consequence of this multiple failure was taken into account.

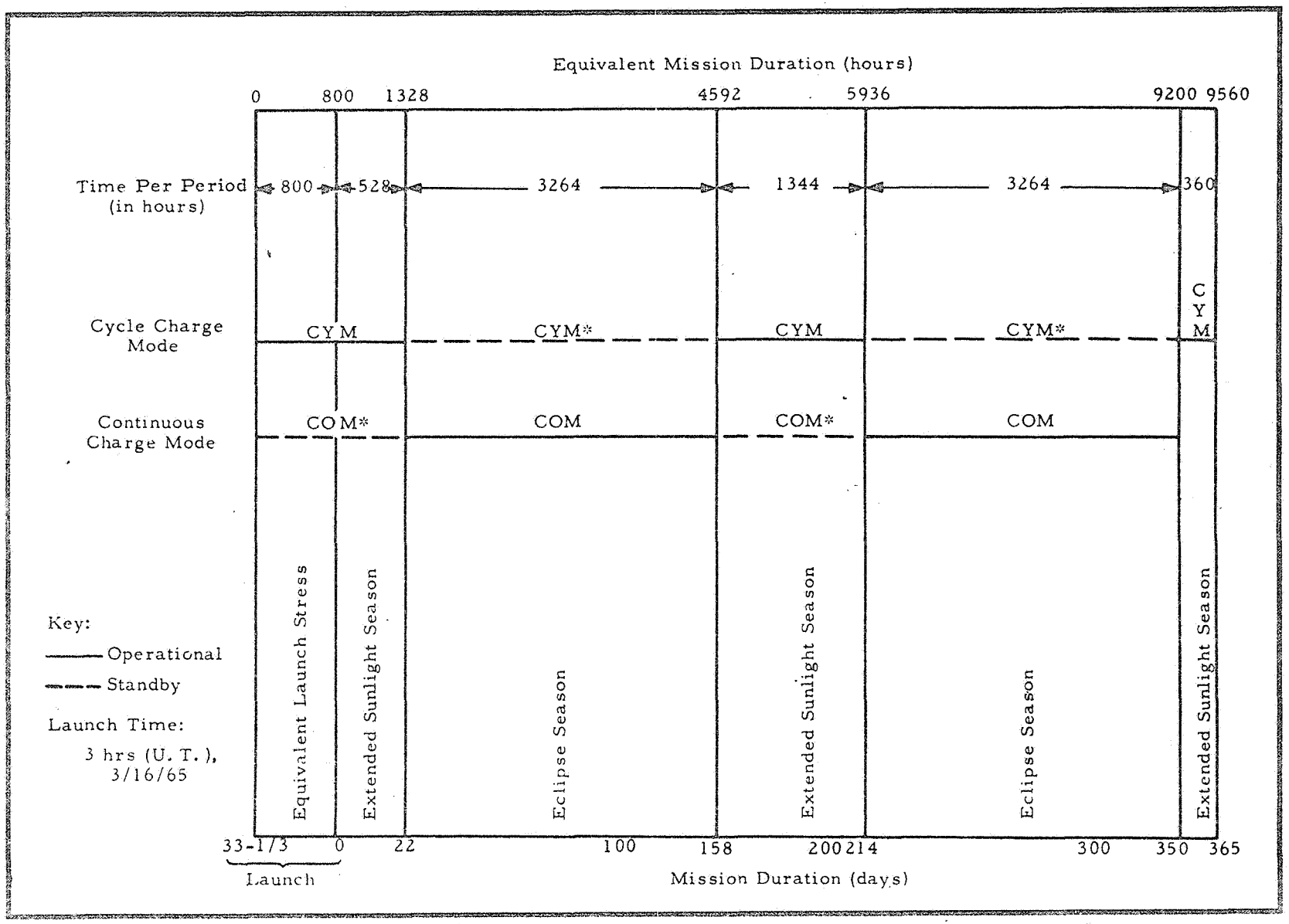


EXHIBIT 1 - POWER SUPPLY SUBSYSTEM MISSION PROFILE FOR POGO ORBIT

diagram of the S-50 power control unit,[1] identifies each component part and the power supply module upon which it is physically located. The third column identifies whether a short (S) or open (O) failure mode is under consideration. The remainder of this exhibit is dichotomized as to whether the continuous charge mode or the cycle charge mode is under consideration. For each of these modes, a numerical code, indexed in Exhibit 3, is listed which gives the initial state resulting from the failure, the indicated corrective action with regard to failure switching, and the final resulting state.

There are two configurations of the Power Supply Subsystem for each charge mode: operational and standby. In addition, there is not sufficient information to determine categorically whether one battery alone can repeatedly bear, without failing, the discharge necessary to supply the required load during the deep eclipse season or whether both batteries are necessary; consequently, both cases were considered. Thus, there are four Power Supply Subsystem configurations per charge mode, or a total of eight configurations, as follows:

a. Two Batteries Required

   (1) Continuous Charge Mode--Operational (eclipse season)

   (2) Continuous Charge Mode--Standby (sunlight season)

   (3) Cycle Charge Mode--Operational (eclipse season)

   (4) Cycle Charge Mode--Standby (sunlight season)

b. One Battery Required

   (1) Continuous Charge Mode--Operational (eclipse season)

   (2) Continuous Charge Mode--Standby (sunlight season)

[1] STL Diagram S214250 U, Schematic Diagram, Power Control Unit S-50, 6 March 1964.

EXHIBIT 2 - FIRST-ORDER FAILURE ANALYSIS SUMMARY

Subunit	Module	Component	S/O	Continuous Charge Mode			Cycle Charge Mode		
				State	Action	Result	State	Action	Result
Battery Current Regulator (2)	A1, A2	R19	S	1.8	1.2	1	1.8	OK	
			O	1.8	1.2	1	1.8	OK	
		CR7	S	1.8	1.2	1	1.8	OK	
			O	OK			OK		
		Q7	S	1.1	1.2	1	1.1	OK	
			O	1.8	1.2	1	1.8	OK	
		Q8	S	1.1	1.2	1	1.1	OK	
			O	1.8	1.2	1	1.8	OK	
		C2	S	1.1	1.2	1	1.1	OK	
			O	1.7	1.2	1	1.7	1.2	1
		CR1	S	OK			OK		
			O	D1.2			D1.2		
		CR2	S	OK			OK		
			O	D1.2			D1.2		
		R6	S	D1.2			D1.2		
			O	D1.2			D1.2		
		R10	S	1.1	1.2	1	1.1	OK	
			O	1.3/11.2	1.2	1	1.3/9.2/11.2	1.2	1
		CR4	S	D1.3			D1.3		
			O	1.1	1.2	1	1.1	OK	
		CR5	S	1.3/11.2	1.2	1	1.3/9.2/11.2	1.2	
			O	1.1	1.2	1	1.1	OK	
		R13	S	1.1	1.2	1	1.1	OK	
			O	1.3	1.2	1	1.3	1.2	1
		R15	S	1.1	1.2	1	1.1	OK	
			O	1.3	1.2	1	1.3	1.2	1

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		R14	S	10.1	5	5	10.1(1)	OK	
			O	10.1	5	5	10.1(1)	OK	
		R16	S	10.1	5	5	10.1(1)	OK	
			O	10.1	5	5	10.1(1)	OK	
		R17	S	10.2	1.2	1	10.2(1)	OK	
			O	10.5	1.2	1	10.5(1)	OK	
		R18	S	10.5	1.2	1	10.5(1)	OK	
			O	10.5	1.2	1	10.5(1)	OK	
		Q6	S	1.1	1.2	1	1.1	OK	
			O	10.5	1.2	1	10.5(1)	OK	
		R12	S	1.6	1.2	1	1.6	1.2	1
			O	1.1	1.2	1	1.1	OK	
		Q4	S	1.6	1.2	1	1.6	1.2	1
			O	1.1	1.2	1	1.1	OK	
		Q3	S	1.3/11.2	1.2	1	1.3/9.2/11.2	1.2	1
			O	1.1	1.2	1	1.1	OK	
		R11	S	1.6	1.2	1	1.6	1.2	1
			O	1.1	1.2	1	1.1	OK	
		Q5	S	1.1	1.2	1	1.1	OK	
			O	1.3/11.2	1.2	1	1.3/9.2/11.2	1.2	1
		R9	S	1.1	1.2	1	1.1	OK	
			O	1.6	1.2	1	1.6	1.2	1
		CR3	S	1.3/11.2	1.2	1	1.3/9.2/11.2	1.2	1
			O	1.1	1.2	1	1.1	OK	
Battery Upper Voltage Limiter (2)	A1, A2	R38	S	1.4/11.2	1.2	1	1.4/8.1/9.2/11.2	None	
			O	1.2	1.2	1	1.2/8.3	1.2	1

(See last page for notes)

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		R40	S	1.2	1.2	1	1.2/8.3	1.2	1
			O	1.4/11.2	1.2	1	1.4/8.1/9.2/11.2	None	
		R41	S	D6.1			D8.1		
			O	10.3	6	6	10.3/12.1	6	6
		R39	S	10.4	6	6	10.4/12.2	6	6
			O	D6.2			D8.2		
		R33	S	1.2	1.2	1	1.2/8.3	1.2	1
			O	1.4/11.2	1.2	1	1.4/8.1/9.2/11.2	None	
		R34	S	1.4/11.2	1.2	1	1.4/8.1/9.2/11.2	None	
			O	1.2	1.2	1	1.2/8.3	1.2	1
		R36	S	1.4/11.2	1.2	1	1.4/8.1/9.2/11.2	None	
			O	1.2	1.2	1	1.2/8.3	1.2	1
		R37	S	1.2	1.2	1	1.2/8.3	1.2	1
			O	1.2	1.2	1	1.2/8.3	1.2	1
		R35	S	1.2	1.2	1	1.2/8.3	1.2	1
			O	1.2	1.2	1	1.2/8.3	1.2	1
		C6	S	1.2	1.2	1	1.2/8.3	1.2	1
			O	D1.1			D1.1		
		Q12A	S	1.4/11.2	1.2	1	1.4/8.1/9.2/11.2	None	
			O	1.2	1.2	1	1.2/8.3	1.2	1
		Q12B	S	1.2	1.2	1	1.2/8.3	1.2	1
			O	1.4/11.2	1.2	1	1.4/8.1/9.2/11.2	None	
		R42	S	1.6	1.2	1	1.6/D7.2		
			O	1.2	1.2	1	1.2/8.3	1.2	1
		R55	S	1.6	1.2	1	1.6/D7.2	1.2	1
			O	1.2	1.2	1	1.2/8.3	1.2	1

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		Q13	S	1.6	1.2	1	1.6/D7.2		
			O	1.2	1.2	1	1.2/8.3	1.2	1
		Q14	S	1.6	1.2	1	1.6/D7.2		
			O	1.2	1.2	1	1.2/8.3	1.2	1
		R43	S	1.6	1.2	1	1.6/D7.2		
			O	1.2	1.2	1	1.2/8.3	1.2	1
Lower Voltage Sensor (2)	A1, A2	R53	S	OK			OK		
			O	OK			8.6	1.2	1
		R54	S	OK			8.6	1.2	1
			O	OK			8.5	None	
		Q17	S	OK			8.6	1.2	1
			O	OK			8.5	None	
		R51	S	OK			8.2	1.2	1
			O	OK			8.6	1.2	1
		R52	S	OK			8.6	1.2	1
			O	OK			8.2	1.2	1
		R49	S	OK			8.1	None	
			O	OK			8.6	1.2	1
		R44	S	OK			8.6	1.2	1
			O	OK			8.5	None	
		R45	S	OK			8.2	1.2	1
			O	OK			8.6	1.2	1
		R46	S	OK			8.6	1.2	1
			O	OK			8.2	1.2	1
		R47	S	OK			8.6	1.2	1
			O	OK			8.6	1.2	1

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		Q15A	S	OK			8.1	None	
			O	OK			8.6	1.2	1
		Q15B	S	OK			8.6	1.2	1
			O	OK			8.2	1.2	1
		Q16	S	OK			8.1	None	
			O	OK			8.6	1.2	1
		CR14	S	OK			OK		
			O	OK			8.6	1.2	1
		R50	S	OK			8.4	1.2	1
			O	OK			8.6	1.2	1
		R62	S	OK			8.4	1.2	1
			O	OK			8.2	1.2	1
Cycle Relay Driver (2)	A1, A2	Q18	S	OK			8.1	None	
			O	OK			8.4	1.2	1
		R56	S	OK			8.4	1.2	1
			O	OK			8.4	1.2	1
		R57	S	OK			8.4	1.2	1
			O	OK			8.2	1.2	1
		Q19	S	OK			8.1	None	
			O	OK			8.4	1.2	1
		R58	S	OK			8.4	1.2	1
			O	OK			8.1	None	
		CR15	S	OK			D7.1		
			O	OK			8.1	None	
		CR16	S	OK			D7.1		
			O	OK			8.1	None	

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		R59	S	OK			8.1	None	
			O	OK			8.4	1.2	1
		C7	S	OK			8.4	1.2	1
			O	OK			D7.1		
		R60	S	OK			8.1	None	
			O	OK			8.4	1.2	1
		Q20	S	OK			8.4	1.2	1
			O	OK			8.1	None	
		CR17	S	OK			8.6	1.2	1
			O	OK			8.4	1.2	1
		R61	S	OK			D7.2		
			O	OK			8.4	1.2	1
		Q21	S	OK			8.1	None	
			O	OK			8.4	1.2	1
		CR20	S	OK			D7.1		
			O	OK			8.4	1.2	1
		R63	S	OK			8.4	1.2	1
			O	OK			8.2	1.2	1
		R64	S	OK			8.4	1.2	1
			O	OK			8.4	1.2	1
		R65	S	OK			OK		
			O	OK			8.4	1.2	1
		Q22	S	OK			8.1	None	
			O	OK			8.4	1.2	1
		CR18	S	OK			OK		
			O	OK			D7.3		
		CR19	S	OK			OK		
			O	OK			D7.3		

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		K104 (Contacts)	S	OK			8.4	1.2	1
		(Coil	O	OK			8.4	1.2	1
		K204 (Contacts	S	OK			8.4	1.2	1
		(Coil)	O	OK			8.4	1.2	1
Battery-Bus Voltage Limiter (2)	A1, A2	CR12	S	OK			9.1	1.2	1
			O(1)	11.1			11.1		
		CR13	S	OK			8.5	None	
			O	OK			9.1	1.2	1
		R28	S	OK			9.2	1.2	1
			O	OK			9.1	1.2	1.1
		R29	S(1)	1.9/11.2	3.1	3.1	1.9/9.2/11.2	1.2	1
			O(1)	11.1			9.1/11.1	1.2	1
		R31	S	OK			9.2	1.2	1
			O	OK			D9.1		
		R32	S(1)	1.9/11.2	3.1	3.1	1.9/9.2/11.2	1.2	1
			O(1)	D10.2			D9.1/D10.2		
		R30	S(1)	11.1			9.1/11.1	1.2	1
			O(1)	1.9/11.2	3.1	3.1	1.9/9.2/11.2	1.2	1
		Q10	S(1)	11.1			9.1/11.1	1.2	1
			O(1)	1.4/11.2	1.2	1	1.4/9.2/11.2	1.2	1
		Q11	S(1)	1.4/11.2	1.2	1	1.4/9.2/11.2	1.2	1
			O(1)	11.1			9.1/11.1	1.2	1
		R27	S(1)	1.4/11.2	1.2	1	1.4/9.2/11.2	1.2	1
			O(1)	11.1			9.1/11.1	1.2	1
		R23	S(1)	11.1			9.1/11.1	1.2	1
			O(1)	1.4/11.2	1.2	1	1.4/9.2/11.2	1.2	1

(See last page for notes)

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		R22	S(1)	1.4/11.2	1.2	1	1.4/9.2/11.2	1.2	1
			O(1)	11.1			9.1/11.1	1.2	1
		R26	S(1)	11.3			9.3/11.3	1.2	1
			O(1)	11.1			9.1/11.1	1.2	1
		C4	S(1)	11.1			9.1/11.1	1.2	1
			O(1)	D10.1			D9.2/D10.1		
		C3	S(1)	11.1			9.1/11.1	1.2	1
			O(1)	D10.1			D9.2/D10.1		
		R20	S(1)	D10.1			D9.2/D10.1		
			O(1)	D10.1			D9.2/D10.1		
		CR6	S	D1.1			D1.1		
			O(1)	11.1			9.1/11.1	1.2	1
Shunt Regulator Driver (2)	A1, A2	R7	S	1.2/11.1	1.2	1	1.1/9.1/11.1	OK	
			O	1.3/11.2	1.2	1	1.3/9.2/11.2	1.2	1
		C1	S	1.2/11.1	1.2	1	1.1/9.1/11.1	OK	
			O	D1.1/D10.1			D1.1/D10.1		
		R8	S	D1.1/D10.1			D1.1/D10.1		
			O	D1.1/D10.1			D1.1/D10.1		
		Q2	S	1.3/11.2	1.2	1	1.3/9.2/11.2	1.2	1
			O	1.2/11.1	1.2	1	1.1/9.1/11.1	OK	
		R2	S	1.6/11.3	1.2	1	1.6/9.3/11.3	1.2	1
			O	1.2/11.1	1.2	1	1.1/9.1/11.1	OK	
		R3	S	1.2/11.1	1.2	1	1.1/9.1/11.1	OK	
			O	1.6/11.3	1.2	1	1.6/9.3/11.3	1.2	1
		R4	S	1.2/11.1	1.2	1	1.1/9.1/11.1	OK	
			O	1.6/11.3	1.2	1	1.6/9.3/11.3	1.2	1

(See last page for notes)

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		R1	S	1.6/11.3	1.2	1	1.6/9.3/11.3	1.2	1
			O	1.6/11.3	1.2	1	1.6/9.3/11.3	1.2	1
		R5	S	1.6/11.3	1.2	1	1.6/9.3/11.3	1.2	1
			O	1.6/11.3	1.2	1	1.6/9.3/11.3	1.2	1
		Q1	S	1.3/11.2	1.2	1	1.3/9.2/11.2	1.2	1
			O	1.2/11.1	1.2	1	1.1/9.1/11.1	OK	
	A7 No. 1	Q103	S	1.3/11.2	1.2	1	1.3/9.2/11.2	1.2	1
	No. 2	Q203	O	1.2/11.1	1.2	1	1.1/9.1/11.1	OK	
	No. 1	CR107	S	OK			OK		
	No. 2	CR207	O	OK			OK		
	No. 1	CR108	S	OK			OK		
	No. 2	CR208	O	OK			OK		
Controlled Section Shunt Regulator (4)	Thermal Fin A, B	R'	S	D2.1			D2.1		
			O	2.1	None		2.1 (2)		
		R''	S	2.1	None		2.1 (2)		
			O	D2.1			D2.1		
		R'''	S	D2.1			D2.1		
			O	2.1	None		2.1 (2)		
		Q'	S	2.2	None		2.2 (3)		
			O	2.1	None		2.1 (2)		
		CR'	S	OK			OK		
			O	2.3	None		2.3 (3)		
Battery Current Amplitude Monitor (2)	A6A2, A6A4	CR1	S	1.7	1.2	1	1.7	1.2	1
			O	1.7	1.2	1	1.7	1.2	1

(See last page for notes)

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		CR2	S	1.7	1.2	1	1.7	1.2	1
			O	1.7	1.2	1	1.7	1.2	1
		CR3	S	1.7	1.2	1	1.7	1.2	1
			O	1.7	1.2	1	1.7	1.2	1
		CR4	S	1.7	1.2	1	1.7	1.2	1
			O	1.7	1.2	1	1.7	1.2	1
		T1 Winding	S	1.3	1.2	1	1.3	1.2	1
			O	1.1/6.2	2.2	2	1.1/6.2	None	
	A3, A4	T1 Winding	S	1.1	1.2	1	1.1	OK	
			O	1.1	1.2	1	1.1	OK	
Battery Current Direction Monitor (2)	A6A2 No. 1, A6A3 No. 2	CR1	S	OK			OK		
			O	1.8/4.3	1.2/None	1/	1.8/4.3	OK	
		CR2	S	OK			OK		
			O	1.8/4.3	1.2/None	1/	1.8/4.3	OK	
		CR3	S	OK			OK		
			O	1.1/4.2	1.2/None	1/	1.1/4.2	None	
		CR4	S	OK			OK		
			O	1.1/4.2	1.2/None	1/	1.1/4.2	None	
		T1 Bias Winding	S	D1.8/D4.8			D1.8/D4.8		
			O	D1.8/D4.8			D1.8/D4.8		
		T1 Battery Current Winding	S	1.8/4.3	1.2/None	1/	1.8/4.3	OK	
			O	1.1/6.2	2.2	2	1.1/6.2	None	
		T1 Winding 1-2	S	1.1/4.2	1.2/None	1/	1.1/4.2		
			O	1.8/4.3	1.2/None	1/	1.8/4.3	OK	
		T1 Winding 3-4	S	1.8/4.3	1.2/None	1/	1.8/4.3	OK	
			O	1.1/4.2	1.2/None	1/	1.1/4.3	None	

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
	A3 No. 1, A4 No. 2	R10	S	1.8/4.3	1.2/None	1/	1.8/4.3	OK	
			O	D1.6/D4.6			D1.6/D4.6		
		R12	S	1.8/4.3	1.2/None	1/	1.8/4.3	OK	
			O	D1.6/D4.6			D1.6/D4.6		
		R11	S	1.1/4.2	1.2/None	1/	1.1/4.2	None	
			O	D1.7/D4.7			D1.7/D4.7		
		R13	S	1.1/4.2	1.2/None	1/	1.1/4.2	None	
			O	D1.7/D4.7			D1.7/D4.7		
		R14	S	D1.6/D4.6			D1.6/D4.6		
			O	D1.6/D4.6			D1.6/D4.6		
		R15	S	D1.6/D4.6			D1.6/D4.6		
			O	D1.6/D4.6			D1.6/D4.6		
		R16	S	D1.7/D4.7			D1.7/D4.7		
			O	D1.7/D4.7			D1.7/D4.7		
		R17	S	D1.7/D4.7			D1.7/D4.7		
			O	D1.7/D4.7			D1.7/D4.7		
		C8	S	D1.6/D4.6			D1.6/D4.6		
			O	D1.7/D4.7			D1.7/D4.7		
		C9	S	D1.6/D4.6			D1.6/D4.6		
			O	D1.7/D4.7			D1.7/D4.7		
		C10	S	D1.7/D4.7			D1.7/D4.7		
			O	D1.6/D4.6			D1.6/D4.6		
		C3	S	D1.7/D4.7			D1.7/D4.7		
			O	D1.6/D4.6			D1.6/D4.6		
	A6 No. 1, No. 2	R25	S	1.8/4.3	1.2/None	1/	1.8/4.3	OK	
		R22	O	D1.8/D4.8			D1.8/D4.8		

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
Regulated Reference Voltages (2)	A1, A2	R21	S	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
			O	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
		CR8	S	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
			O	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
		CR9	S	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
			O	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
		CR10	S	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
			O	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
		C5	S	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
			O	D1.4			D1.4		
		Q9	S	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
			O	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
		R24	S	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
			O	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
		CR11	S	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
			O	1.5/11.1	1.2	1	1.5/8.7/9.1/11.1	1.2	1
Oscillator Sync Power Driver (2)	A3, A4	T3	S	D1.5			D1.5		
			O	D1.5			D1.5		
		T4	S	D1.5			D1.5		
			O	D1.5			D1.5		
		R8	S	D1.5			D1.5		
			O	D1.5			D1.5		
		R9	S	D1.5			D1.5		
			O	D1.5			D1.5		
		R19	S	D1.5			D1.5		
			O	D1.5			D1.5		

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		C7	S	D1.5			D1.5		
			O	D1.5			D1.5		
		Q3	S	D1.5			D1.5		
			O	D1.5			D1.5		
		Q4	S	D1.5			D1.5		
			O	D1.5			D1.5		
		R7	S	4.3	1.2	1	4.3	OK	
			O	D1.5			D1.5		
Current Monitors Oscillator (2)	A3, A4	R1	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1 2	1	1.1/4.3	OK	
		R3	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
		R4	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
		R5	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
		R6	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
		R18	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
		C1	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
		C4	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
		C5	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	OK			OK		

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		C6	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	OK			OK		
		Q1	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
		Q2	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
		CR1	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
		CR2	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
		L1	S	OK			OK		
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
		T2	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
		CR3	S	1.1/4.3	1.2	1	1.1/4.3	OK	
			O	1.1/4.3	1.2	1	1.1/4.3	OK	
2461-Cycle Sync (2)	A10, A11	All Components	S	D1.5			D1.5		
			O	D1.5			D1.5		
Series Regulator (2)	A5	No. 1 / No. 2							
		R33 / R35	S	3.1	3.2	3.2	3.1	3.2	3
			O	D3.2			OK		
		CR19 / CR20	S	3.2	1.1	1	3.2	OK	
			O	3.1	3.2	3.2	3.1	3.2	3
		R34 / R53	S	3.2	1.1	1	3.2	OK	
			O	3.1	3.2	3.2	3.1	3.2	3

EXHIBIT 2 (Continued)

Subunit	Module	Component No. 1	Component No. 2	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		R48	R51	S	3.1	3.2	3.2	3.1	3.2	3
				O	3.2	1.1	1	3.2	OK	
		R49	R52	S	3.1	3.2	3.2	3.1	3.2	3
				O	3.2	1.1	1	3.2	OK	
		Q22	Q23	S	3.2	1.1	1	3.2	OK	
				O	3.1	3.2	3.2	3.1	3.2	3
		R27	R28	S	3.1	3.2	3.2	3.1	3.2	3
				O	3.2	1.1	1	3.2	OK	
		C3	C4	S	3.2	1.1	1	3.2	OK	
				O	D3.1			D3.1		
		R47	R50	S	D3.1			D3.1		
				O	D3.1			D3.1		
		Q8	Q9	S	3.1	3.2	3.2	3.1	3.2	3
				O	3.2	1.1	1	3.2	OK	
		Q2	Q3	S	3.1	3.2	3.2	3.1	3.2	3
				O	3.2	1.1	1	3.2	OK	
	A7	Q101	Q201	S	3.1	3.2	3.2	3.1	3.2	3
				O	OK			OK		
		Q102	Q202	S	3.1	3.2	3.2	3.1	3.2	3
				O	OK			OK		
Discharge Control Relays Set (1)	A5	CR17	CR15	S	OK			OK		
				O	4.3			4.3	OK	
		CR18	CR16	S	OK			OK		
				O	4.3			4.3	OK	
		R26	R22	S	4.4	None		4.4	OK	
				O	4.4	None		4.4	OK	

EXHIBIT 2 (Continued)

Subunit	Module	Component No. 1	Component No. 2	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		R46	R42	S	4.4	None		4.4	OK	
				O	OK			OK		
		CR13	CR12	S	OK			OK		
				O	4.4	None		4.4	OK	
		R24	R23	S	4.4	None		4.4	OK	
				O	4.4	None		4.4	OK	
		R44	R43	S	4.4	None		4.4	OK	
				O	OK			OK		
		C6	C5	S	4.2	None		4.2	None	
				O	D4.1			OK		
		Q17	Q16	S	OK			4.2	None	
				O	4.4	None		4.4	OK	
		Q21	Q23	S	OK			4.2	None	
				O	4.4	None		4.4	OK	
		R19		S	OK			OK		
				O	OK			OK		
		R20		S	OK			OK		
				O	OK			OK		
		CR3		S	OK			OK		
				O	D4.2			OK		
		CR5		S	OK			OK		
				O	D4.2			OK		
		K105 (Contacts)		S	4.8	None		4.8	None	
		(Coil)		O	4.5	None		4.5	OK	
		K205 (Contacts)		S	4.8	None		4.8	None	
		(Coil)		O	4.5	None		4.5	OK	

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
Load Bus Monitor (1)	A5	R2	S	4.6/5.1	None	/4	4.6/5.1	None/4	/4
			O	4.7/5.2	None/4	/4	4.7/5.2	OK/4	4
		CR7	S	D4.5/D5.6	/4	/4	D4.5/D5.6	/4	4
			O	4.6/5.1	None	/4	4.6/5.1	None	/4
		CR14	S	4.7/5.2	None/4	/4	4.7/5.2	OK/4	4
			O	4.6/5.1	None	/4	4.6/5.1	None	/4
		R14	S	4.7/5.2	None/4	/4	4.7/5.2	OK/4	4
			O	4.7/5.2	None/4	/4	4.7/5.2	OK/4	4
		R3	S	4.7/5.2	None/4	/4	4.7/5.2	OK/4	4
			O	4.6/5.1	None	/4	4.6/5.1	None	/4
		R4	S	4.6/5.1	None	/4	4.6/5.1	None	/4
			O	4.6/5.1	None	/4	4.6/5.1	None	/4
		R37	S	4.6/5.1	None	/4	4.6/5.1	None	/4
			O	4.6/5.1	None	/4	4.6/5.1	None	/4
		C2	S	4.6/5.1	None	/4	4.6/5.1	None	/4
			O	D4.4/D5.1			OK/D4.1		
		R16	S	D4.4/D5.1			OK/D4.1		
			O	D4.4/D5.1			OK/D4.1		
		R15	S	4.7/5.2	None/4	/4	4.7/5.2	OK/4	4
			O	4.6/5.1	None	/4	4.6/5.1	None	/4
		R38	S	4.6/5.1	None	/4	4.6/5.1	None	/4
			O	4.7/5.2	None/4	/4	4.7/5.2	OK/4	4
		R39	S	4.6/5.1	None	/4	4.6/5.1	None	/4
			O	4.7/5.2	None/4	/4	4.7/5.2	OK/4	4
		Q12A	S	4.6/5.1	None	/4	4.6/5.1	None	/4
			O	4.7/5.2	None/4	/4	4.7/5.2	OK/4	4

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		Q12B	S	4.7/5.2	None/4	/4	4.7/5.2	OK/4	4
			O	4.6/5.1	None	/4	4.6/5.1	None	/4
		CR1	S	OK			OK		
			O	D4.4/D5.1			OK/D4.1		
		CR2	S	OK			OK		
			O	D4.4/D5.1			OK/D4.1		
		Q1	S	D4.4/5.4	/4	/4	OK/5.4	/4	/4
			O	4.6/5.1	None	/4	4.6/5.1	None	/4
		Q6	S	D4.4/5.4	/4	/4	OK/5.4	/4	/4
			O	4.6/5.1	None	/4	4.6/5.1	None	/4
		R8	S	D4.4/5.4	/4	/4	OK/5.4	/4	/4
			O	4.6/5.1	None	/4	4.6/5.1	None	/4
Uncontrolled Array Driver (1)	A5	R12	S	5.4	4	4	5.4	4	4
			O	5.1	None	4	5.1	None	4
		Q10	S	5.4	4	4	5.4	4	4
			O	5.1	None	4	5.1	None	4
		R30	S	5.4	4	4	5.4	4	4
			O	5.1	None	4	5.1	None	4
		R29	S	5.1	None	4	5.1	None	4
			O	5.4	4	4	5.4	4	4
		Q5	S	5.2	4	4	5.2	4	4
			O	5.1	None	4	5.1	None	4
		Q4	S	5.2	4	4	5.2	4	4
			O	5.1	None	4	5.1	None	4
		Q18	S	5.2	4	4	5.2	4	4
			O	5.1	None	4	5.1	None	4

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		R1	S	5.4	4	4	5.4	4	4
			O	5.1	None	4	5.1	None	4
		R10	S	5.1	None	4	5.1	None	4
			O	5.4	4	4	5.4	4	4
		R9	S	5.1	None	4	5.1	None	4
			O	5.4	4	4	5.4	4	4
Uncontrolled Section Shunt Regulator (1)	A7	R301	S	5.4	4	4	5.4	4	4
			O	5.1	None	4	5.1	None	4
		R302	S	5.1	None	4	5.1	None	4
			O	5.4	4	4	5.4	4	4
		R303	S	5.4	4	4	5.4	4	4
			O	5.1	None	4	5.1	None	4
		Q301	S	5.2	None		5.2	None	
			O	5.1	None	4	5.1	None	4
Discharge Control Reset Driver (1)	A5	R13	S	D4.4			OK		
			O	4.6	None		4.6	None	
		Q11	S	D4.4			OK		
			O	4.6	None		4.6		
		R31	S	D4.4			OK		
			O	4.6	None		4.6	None	
		R36	S	4.6	None		4.6	None	
			O	D4.4			OK		
		Q19	S	4.7	None		4.7	OK	
			O	4.6	None		4.6	None	

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		R5	S	4.6	None		4.6	None	
			O	4.7	None		4.7	OK	
		CR8	S	OK			OK		
			O	4.7	None		4.7	None	
		CR9	S	OK			OK		
			O	4.7	None		4.7	OK	
		R40	S	4.7	None		4.7	None	
			O	4.6	None		4.6	None	
		C1	S	4.6	None		4.6	None	
			O	D4.3			OK		
		R6	S	4.7	None		4.7	None	
			O	4.6	None		4.6	None	
		Q13	S	4.6	None		4.6	None	
			O	4.7	None		4.7		
		R7	S	4.6	None		4.6	None	
			O	4.6	None		4.6	None	
		Q7	S	4.7	None		4.7	OK	
			O	4.6	None		4.6	None	
		CR10	S	D4.3	None		OK	None	
			O	4.6	None		4.6	None	
		R41	S	4.6	None		4.6	None	
			O	D4.4			OK		
		R32	S	4.6	None		4.6	None	
			O	4.6	None		4.6	None	
		R21	S	4.6	None		4.6	None	
			O	4.6	None		4.6	None	
		CR11	S	OK		OK			
			O	4.6	None		4.6	None	

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		Q14	S	OK			OK		
			O	4.6	None		4.6	None	
		Q15	S	OK			OK		
			O	4.6	None		4.6	None	
		R17	S	OK			OK		
			O	OK			OK		
		R18	S	OK			OK		
			O	OK			OK		
		CR4	S	4.6	None		4.6	None	
			O	D4.2			OK		
		CR6	S	4.6	None		4.6	None	
			O	D4.2			OK		
		K105 (Contacts)	S	OK			OK		
		(Coil)	O	4.8			4.8		
		K205 (Contacts)	S	OK			OK		
		(Coil)	O	4.8			4.8		
Miscellaneous Components	A7	CR101, CR201	S	OK			OK		
			O	OK(4)			OK(4)		
		CR102, CR202	S	OK			OK		
			O	OK(4)			OK(4)		
		CR103, CR203	S	OK(4)			8.8	None	
			O	OK(4)			OK		
		CR104, CR204	S	OK(4)			OK		
			O	OK(4)			OK(4)		
		CR105, CR205	S	OK(4)			OK(4)		
			O	5.5	OK		5.5	OK	

(See last page for notes)

EXHIBIT 2 (Continued)

Subunit	Module	Component	S/O	Continuous Charge Mode State	Continuous Charge Mode Action	Continuous Charge Mode Result	Cycle Charge Mode State	Cycle Charge Mode Action	Cycle Charge Mode Result
		CR106, CR206	S	OK(4)			OK(4)		
			O	2.4	1.1	1	2.4	None	
	Controlled Array Section--Diode (4)		S	OK(4)			OK(4)		
			O	2.3	None		2.3	OK	
	No. 1 Uncontrolled Current Monitor--Transformer Winding (A8A1)		S	OK(5)			OK(5)		
			O	5.3	None		5.3	OK	
	Array Current Monitor--Transformer Winding No. 1 (A8A2), No. 2 (A8A3)		S	OK(5)			OK(5)		
			O	7.1	None		7.1	None	
	Battery Current Amplitude Monitor (TM)--Transformer Winding No. 1 (A8A4), No. 2 (A8A5)		S	OK(5)			OK(5)		
			O	6.3	2.1		6.3	None	
	Battery No. 1 or No. 2		S	6.1	2.1	2	6.1	2.1	2
			O	6.1	2.1	2	6.1	None	

Notes: (1) Also affects operation in load bus overvoltage condition.

(2) Associated battery failure rate increased because of large charge current, but battery removed from charge by cycle relay at upper voltage limit.

(3) Surviving section provides battery current during charge.

(4) Operation affected only if another failure occurs.

(5) TM indication lost.

EXHIBIT 3 - INDEX OF FAILED STATES, DEGRADED STATES, FAILURE SWITCHING AND FINAL RESULTS

Failed States

1. Charge Control function failed in Normal limits (E_B = Normal, I_B = 1A)
   - 1.1 Battery charge current not regulated
   - 1.2 Battery upper voltage not limited
   - 1.3 Battery current minimum
   - 1.4 Battery upper charge voltage too low
   - 1.5 Regulated reference voltages incorrect
   - 1.6 Current or voltage regulation loop gain changed
   - 1.7 Incorrect current indication from Current Direction Monitor
   - 1.8 Current regulated for both charge and discharge
   - 1.9 Load Bus Overvoltage Limiter causes battery voltage to be limited at low value
   - 1.10 Battery-Bus Voltage Limiter loop gain changed
2. Controlled Array section failed
   - 2.1 One controlled section output unregulated. No battery charge regulation
   - 2.2 One controlled section output minimum
   - 2.3 One controlled section output opened
   - 2.4 No power supplied to Load Bus from one Charge Bus
3. Series Regulator function failed
   - 3.1 One Series Regulator shorted
   - 3.2 One Series Regulator open. No power supplied to Load Bus from one Charge Bus during Battery charge
4. Discharge Control function failed
   - 4.1 Discharge Control relays not set (bypass). Both Series Regulators remain inserted during battery discharge
   - 4.2 Continuous set (bypass) signal to both Discharge Control relays. Both Series Regulators bypassed, and both Charge Buses limited to 34.1 volts during charge
   - 4.3 Discharge indication from one Current Direction Monitor open
   - 4.4 No set (bypass) signal to either Discharge Control relay from one Discharge Control Set channel
   - 4.5 One Series Regulator not bypassed during battery discharge
   - 4.6 No reset signal to both Discharge Control relays. Both Series Regulators bypassed, and both Charge Buses limited to 34.1 volts during charge
   - 4.7 Continuous reset signal to both Discharge Control relays. Both Series Regulators inserted during battery discharge
   - 4.8 One Series Regulator bypassed during charge, and Charge Bus limited to 34.1 volts

EXHIBIT 3 (Continued)

Failed States (Continued)

5. "Uncontrolled" array section failed

   5.1 Output unregulated. Load Bus overvoltage if two uncontrolled sections output greater than load requirements
   5.2 Output minimum
   5.3 Output open
   5.4 Control loop gain changed
   5.5 Section voltage supplies load through Series Regulators and operates at battery charge voltage. Output reduced at high voltage

6. Battery failed

   6.1 Battery shorted or open
   6.2 Battery circuit opened. Charge Control also failed
   6.3 Battery circuit opened. Charge Control unaffected

7. Branch failed

   7.1 Output of 3 array sections open

8. Cycle relay operation failed in Normal limits (E_B = Normal, I_B = 1A) (cycle only)

   8.1 Cycle relay continuously energized, and Battery removed from charge
   8.2 Cycle relay held energized below lower voltage limit and Battery removed from charge
   8.3 Cycle relay not energized at upper voltage limit. Battery charged above upper voltage limit
   8.4 Cycle relay not energized at upper voltage limit. Battery "trickle" charged at upper voltage limit
   8.5 Cycle relay energized whenever battery voltage above lower limit. Battery cycled at high rate at lower voltage limit
   8.6 Cycle relay not held energized below upper voltage limit. Battery cycled at high rate at upper voltage limit
   8.7 Regulated reference voltages incorrect. Cycle relay not energized. Battery charged above upper voltage limit
   8.8 Battery continuously "trickle" charged at 36 volts once cycle relay is energized

9. Charge Bus regulation failed (cycle only)

   9.1 Charge Bus unregulated during battery "float"
   9.2 Charge Bus regulated to low voltage during "float"
   9.3 Charge Bus regulator loop gain changed

EXHIBIT 3 (Continued)

Failed States (Continued)

10. Charge Control function failed when non-normal current or voltage level commanded

    10.1 Current regulation failed when 5A rate commanded (Cont. only)
    10.2 Current regulation failed when 10A rate commanded (Cont. only)
    10.3 Battery voltage limited at low value when "A" commanded
    10.4 Battery voltage not limited when "B" commanded
    10.5 Battery current 5A when 10A rate commanded (Cont. only)

11. Load Bus overvoltage limiter function failed

    11.1 Load Bus voltage uncontrolled
    11.2 Controlled sections outputs minimum
    11.3 Load Bus overvoltage limiter loop gain changed

12. Cycle relay operation failed when non-normal voltage limit commanded (Cycle only)

    12.1 Cycle relay continuously energized when "A" commanded. Battery removed from charge
    12.2 Cycle relay not energized when "B" commanded. Battery overcharged

Degraded States

D1. Charge Control function degraded in Normal mode (E_B = Normal, I_B = 1A)

    D1.1 Current or voltage regulation loop frequency response changed
    D1.2 Current Regulator not clamped when Shunt Regulator Driver saturated
    D1.3 Current Regulator temperature-sensitive
    D1.4 Comparator bias voltages susceptible to transients
    D1.5 Current monitors excitation free-running. System noise level increased
    D1.6 Current Direction Monitor crossover offset. Discharge indication for discharge current of less than 300 ma or for finite charge current. Possibility of stopping associated Battery current regulation
    D1.7 Current Direction Monitor crossover offset. Discharge not indicated until discharge current greater than nominal 300 ma. Possibility of array current reduction during Battery discharge
    D1.8 Current Direction Monitor 300 ma discharge bias eliminated

EXHIBIT 3 (Continued)

Degraded States (Continued)

D2. Controlled array section degraded

D2.1 Shunt Regulator gain changed

D3. Series Regulator function degraded

D3.1 Individual regulator frequency response changed
D3.2 Individual regulator active below normal level

D4. Discharge Control function degraded

D4.1 Energization of both Discharge Control relays not delayed (Con. only)
D4.2 Relay transients dissipated through output transistors (Con. only)
D4.3 Resetting of both Discharge Control relays not delayed (Con. only)
D4.4 Loop gain and/or frequency response changed (Con. only)
D4.5 Discharge Control relays reset when Load Bus voltage less than 32.5 volts (Con. only)
D4.6 Current Direction Monitor crossover offset. Discharge indication for discharge current of less than 300 ma or for finite charge current. Possibility of generating Discharge Control Set (bypass) signal, causing both Batteries to be charged only to 34.1 volts
D4.7 Current Direction Monitor crossover offset. Discharge not indicated until discharge current greater than nominal 300 ma. Setting of Discharge Control relays delayed (Con. only)
D4.8 Current Direction Monitor crossover eliminated. Discharge Control Set (bypass) signal generated for any value of discharge current. Possibility of bypassing Series Regulators, causing both batteries to be charged only to 34.1 volts

D5. "Uncontrolled" array section degraded

D5.1 Load Bus Limiter loop frequency response changed
D5.2 "Uncontrolled" section output reduced when Load Bus voltage less than nominal 32.5 volts

D6. Battery charge voltage limit selection failed

D6.1 Charge voltage limited at Normal upper voltage limit when "A" commanded
D6.2 Charge voltage limited at Normal upper voltage limit when "B" commanded

EXHIBIT 3 (Continued)

Degraded States (Continued)

D7. Cycle relay operation degraded in Normal limits (E_B = Normal) (Cycle only)

- D7.1 Delay in energizing or deenergizing relay eliminated. Circuit operation susceptible to transients
- D7.2 Gain and/or phase shift of control loop changed
- D7.3 Relay transients dissipated through output transistors

D8. Cycle relay operating voltage limit failed (Cycle only)

- D8.1 Cycle relay energized at Normal upper voltage limit when "A" commanded
- D8.2 Cycle relay energized at Normal upper voltage limit when "B" commanded

D9. Charge Bus regulation failed (Cycle only)

- D9.1 Charge Bus regulated slightly above 36 volts during "float"
- D9.2 Charge Bus regulator loop frequency response changed

D10. Load Bus overvoltage limiter degraded

- D10.1 Load Bus overvoltage regulator loop frequency response changed
- D10.2 Load Bus limited to slightly above 34 volts

EXHIBIT 3 (Continued)

Available Switching Action

Action	Applicable CON	Applicable CYM	Results: Continuous Charge Mode	Results: Cycle Charge Mode
1. K101, K102 (or K201, K202) energized by ground command			1.1, 1.2 A. Outputs of all controlled sections connected and regulated by one Charge Control unit B. Batteries in parallel. Captive battery charged without temperature feedback to 0.7 volts less than active Battery. Active Battery charged normally C. Series Regulators in parallel. If one is open, remaining carries load current from Charge Bus	1.2 A. Output of all controlled sections connected and regulated by one charge control unit B. Batteries in parallel. Captive battery "trickle-charged" between 36 volts and active battery upper voltage limit less 0.7 volt connecting diode drop. Active battery charged normally C. Series Regulators in parallel. If one is open, remaining carries load current from charge bus
1.1 Either Charge Control unit can be used	X	NA		
1.2 Charge Control Unit of other branch must be used	X	X		
2. K103 (or K203) and K101, K102 (or K201, K202) energized by ground command			2.1, 2.2 A. Outputs of all controlled sections connected and regulated by one charge control unit B. Surviving Battery charged normally if same charge control unit is used but without temperature feedback if other Charge Control unit is used C. Series Regulators in parallel	2.1 A. Outputs of all controlled sections connected and regulated by one Charge Control during charge. Common charge bus regulated by one charge control during float B. Cycle relay operation indeterminant. Battery either cycle charged normally or continuously "trickle-charged" at 36 volts C. Series Regulators in parallel
2.1 Either Charge Control unit can be used	X	X		
2.2 Charge Control unit of other branch must be used	X	NA		
3. CDU relay 12 K15 (or 13 K7) energized by ground command			3.1 Both Batteries charged to normal limit 3.2 A. Operational branch Battery charged normally B. "Failed" branch Battery limited to 34.1 volts	3.2 A. Operational branch battery charged normally B. Failed branch battery continuously trickle charged at 34.1 volts
3.1 In same branch	X	NA		
3.2 In opposite branch	X	X		
4. K302 energized by ground command	X	X	4. Output of "uncontrolled" section not regulated if Load Bus voltage is greater than 32.5 volts. Overvoltage if uncontrolled sections output is greater than load requirement	4. Output of "uncontrolled" section not regulated if load bus voltage is greater than 32.5 volts. Overvoltage if uncontrolled sections output is greater than load requirements
5. 10 amp rate commanded without commanding 5 amp rates	X	NA	5. Both Batteries charged at 6 amps	5. N/A
6. Normal upper voltage limit commanded	X	X	6. Both Batteries charged to Normal upper voltage limit	6. Both batteries charged to normal upper voltage limit

(3) Cycle Charge Mode--Operational (eclipse season)

(4) Cycle Charge Mode--Standby (sunlight season)

For each configuration, a different reliability expression is appropriate because of the different consequences to mission reliability of each particular failure.

The approach used here is, in short, to determine a reliability expression for each configuration and then to combine these reliability expressions in an appropriate manner to arrive at an overall power supply reliability expression as a function of time.

c. Assumptions

Before proceeding with the detailed reliability modeling for each configuration, certain assumptions which apply to all configurations will be stated. These assumptions are made in order to simplify the calculations and to more clearly define the modeled system.

(1) The solar arrays exhibit only a deterministic degradation with time, which is such that all solar array sections are required during the eclipse seasons, and four of six sections are required during periods of continuous sunlight. (See Appendix A for justification of this assumption.)

(2) To fully replace the charge withdrawn from the batteries during the eclipse, the 5 ampere charge rate is required for eclipses longer than 10 minutes when both batteries are available, and the 10 ampere charge rate is required for eclipses longer than 28 minutes when one battery has failed (see Exhibit A-3, Appendix A). Since for the majority of the eclipse season the eclipse duration exceeds these times, it is assumed that the 5 ampere or 10 ampere command is required during the entire eclipse season when both batteries or one battery are available, respectively.

(3) If the 5 ampere command fails, it is assumed that the 6 ampere rate, which can be generated by commanding the 10 ampere command without the 5 ampere command, will satisfactorily limit the charge current and will not degrade battery operation.

(4) If a battery remains on continuous charge at any voltage or is continuously removed from charge during the extended sunlight period (i.e., the cycle relay is not energized or is continuously energized), the battery will fail.

(5) Because of assumptions (2), (3), and (4), the batteries and Power Supply Subsystem will fail without the command capability of increasing the charge current rate in the continuous charge mode or of energizing the cycle relays in the cycle charge mode. Thus, it is assumed for this assessment that all commands are available for enough of each orbit to perform any of their desired functions.

(6) Although STL states that approximately 25 percent of battery capacity remains when a battery charge is limited to 34.1 volts, the present assessment assumes that the battery has failed and that no capacity remains.

(7) If the battery charge bus is unregulated during cycle charge mode float, it is assumed that the increased power dissipation in a series regulator will cause the series regulator to fail open.

(8) If the battery is cycled between charge and float at an abnormally high rate in the cycle charge mode either because of incorrect cycle relay operation or because of low charge bus regulation during float, it is assumed that the battery will fail.

(9) It is assumed that the load bus limiter function is not required for mission success, since the control can be removed by ground command, and any excess uncontrolled array output can be dissipated without increasing the load bus voltage above 32.5 volts by commanding additional equipment on, such as high-power experiments.

(10) Failure rates are assumed to be constant with time in both the operational and standby configurations.

(11) Although the batteries probably have an increasing failure rate with time, insufficient data are available to quantify this effect; hence, the battery failure rate is also assumed to be a constant.

(12) It is assumed that all the degraded states shown in Exhibit 2 cause no significant reliability degradation.

(13) The load bus filter (capacitor quad) and the 2461-cps synchronous oscillator are treated as perfectly reliable in this assessment, the former because of its near unit reliability and the latter because any failure only slightly degrades system performance.

3. Model Formulation

For each of the possible equipment configurations, a reliability model is developed; a reliability diagram consisting of a number of somewhat artifical units is used. Each unit consists of all part/failure mode combinations for which the first-order failure of each yields the same effect on mission reliability for a particular configuration. The failure rate of each unit is assumed to be the sum of the failure rates of the part/failure mode combinations which constitute the unit. The failure rates used are given in Section 4.

The various units used in the assessment of the eight required configuration reliabilities are defined in Exhibit 4 in terms of Exhibit 2 "states." These units were derived by observing which states always occurred together, in the sense that any failure in the unit causes the same mission effect in any particular configuration. As Exhibit 4 shows, a total of 33 such units were required. The relationship of these units to configuration reliability is graphically demonstrated in Exhibits 5 through 9. The U_i terms in each block of the diagrams indicate which of the Exhibit 4 units are contained in that block. An exponent of any term indicates the number of such units in the block. So that the physical implications of each model can be better understood, the blocks of Exhibits 5 through 9 are further grouped into generalized functions.

a. Two Batteries Required

The reliability diagram of the operational continuous charge mode configurations, COM, is given in Exhibit 5. This is a straightforward formulation for which the reliability expression is[1]

[1] The superscript (2) is used throughout this subsection to indicate that two batteries are required.

EXHIBIT 4 - DEFINITION OF "UNITS" AND THE FAILURE RATE OF EACH

Unit Index, i	Quantity Total	Unit Definition, U_i (in terms of states)(1)	Unit Failure Rate, $\lambda \times 10^{-6}$
1	2	1.1, 1.6, 1.7, 1.8	3.99
2	1	1.1/4.2, 1.1/4.2, 4.6/5.1	2.85
3	2	1.1/4.3, 1.8/4.3	3.32
4	2	1.1/6.2	0.20
5	2	1.2	2.18
6	2	1.2/11.1	0.83
7	2	1.3	0.37
8	2	1.3/11.2	1.14
9	2	1.4/11.2	1.52
10	2	1.5/11.1	1.42
11	2	1.6/11.3	0.87
12	2	1.9/11.2	0.27
13	4	2.1	0.56
14	4	2.2, 2.3	0.42
15	2	2.4, 3.2	1.44
16	2	3.1, 4.8	1.45
17	1	4.2, 4.6	2.92
18	2	4.3	0.27
19	2	4.4	0.98
20	2	4.5	0.10
21	1	4.7, 4.7/5.2	2.18
22	1	5.3	0.04
23	2	6.1	24.00
24	2	6.3	0.04
25	2	7.1	0.08
26	2	8.1, 8.2, 8.4, 8.5, 8.6, 8.8	8.14
27	2	9.1, 9.1/11.1 CYM	1.60
28	2	9.2	0.09
29	2	10.1	0.46
30	2	10.2, 10.5	0.61
31	2	11.1	1.52
32	2	11.1 CYM	0.13
33	2	11.3	0.04

Note: (1) All states refer to the continuous charge mode except when followed by CYM, in which case they refer to the cycle charge mode.

$$R^{(2)}_{COM} = U_1 U_3 \prod_{i=5}^{11} U_i \left[U_{29} + U_{30}(1 - U_{29})\right] U_{18}$$

$$\cdot \left\{2 - U_1 U_3 \prod_{i=1}^{5} U_i \left[U_{29} + U_{30}(1 - U_{29})\right] U_{18}\right\}$$

$$\cdot\ U_{19}(2 - U_{19})\ U_{15} U_{20}(2 - U_{15} U_{20}) \tag{1}$$

$$\cdot\ U_{13}^4 U_{14}^4 U_{22} U_{25}^2 U_2 U_{17} U_{21} U_{16}^2 U_4^2 U_{23}^2 U_{24}^2$$

where U_i now denotes the reliability of unit U_i and the time notation is uniformly suppressed for ease in writing.

The standby continuous charge mode configuration, COM*, is diagrammed in Exhibit 6. This configuration expresses the probability that the continuous charge mode will survive the extended sunlight season and be operable when required for the next eclipse season. This configuration differs from the operational case in that some units may cause battery failure, and hence continuous charge mode failure, during periods of extended sunlight without, however, failing the Power Supply Subsystem during the sunlight season. The equation for this configuration is

$$R^{(2)}_{COM*} = U_1 U_3 U_6 U_{11} \left[U_{29} + U_{30}(1 - U_{29})\ U_{18}\right]$$

$$\cdot \left\{2 - U_1 U_3 U_6 U_{11} \left[U_{29} + U_{30}(1 - U_{29})\right] U_{18}\right\}$$

$$\cdot\ U_{19}(2 - U_{19})\ U_{15} U_{20} U_{27}(2 - U_{15} U_{20} U_{27}) \tag{2}$$

$$\cdot\ U_5^2 \prod_{i=7}^{10} U_i^2 U_{12}^2 U_{28}^2 U_{26}^2$$

$$\cdot\ U_{13}^4 U_{14}^4 U_{22} U_{25}^2 U_2 U_{17} U_{21} U_{16}^2 U_4^2 U_{23}^2 U_{24}^2$$

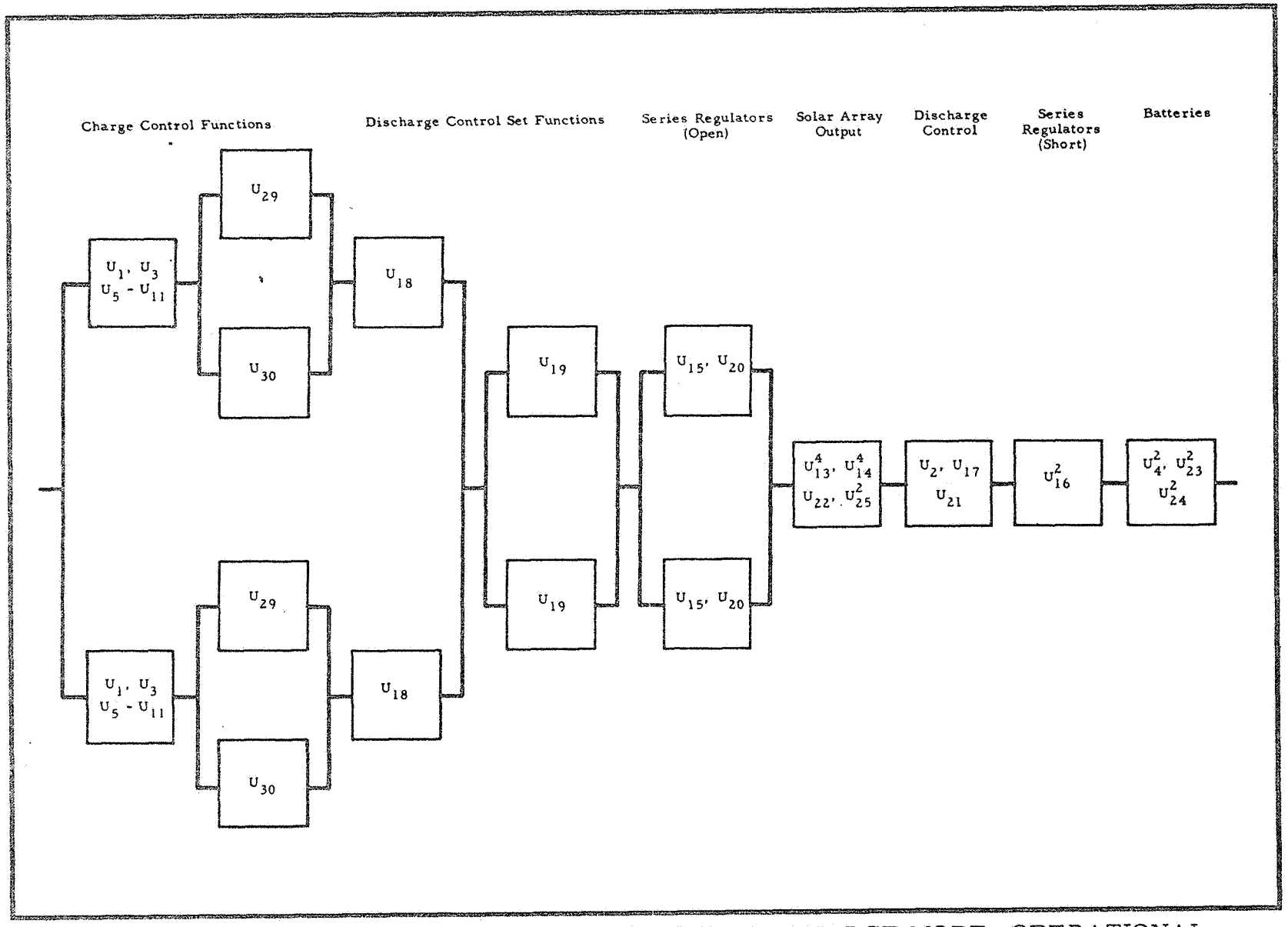


EXHIBIT 5 - RELIABILITY DIAGRAM--CONTINUOUS CHARGE MODE, OPERATIONAL (TWO BATTERIES REQUIRED)

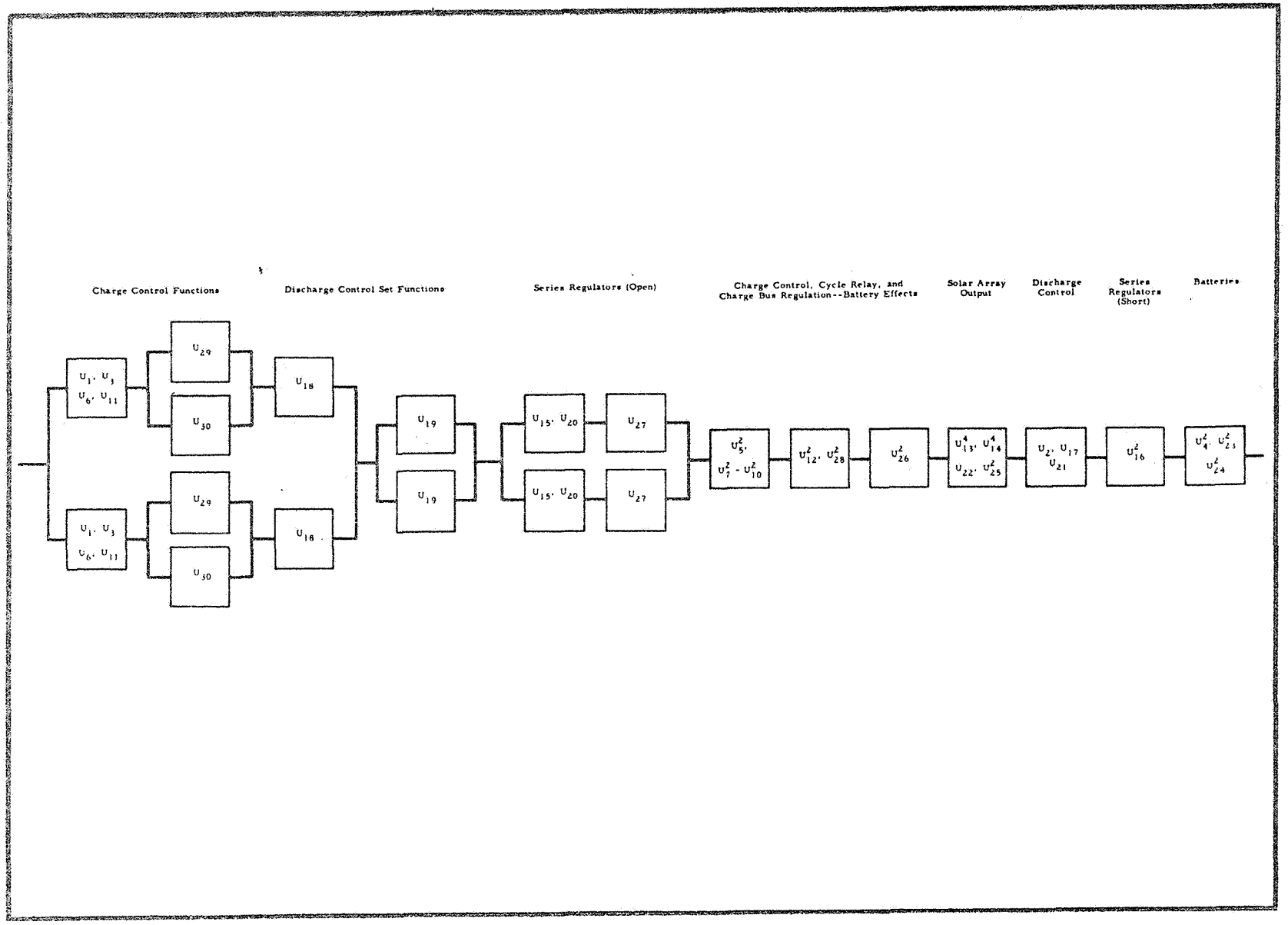


EXHIBIT 6 - RELIABILITY DIAGRAM--CONTINUOUS CHARGE MODE, STANDBY (TWO BATTERIES REQUIRED)

The reliability diagram of the operational cycle charge mode (CYM) configuration shown in Exhibit 7 is applicable to either a one- or two-battery situation, since the cycle charge mode is independent of the batteries in its operational configuration. The equation for this configuration is

$$
\begin{aligned}
R_{CYM} = & \left[U_{25}^2 U_{14}^4 + 4U_{14}^3(1 - U_{14}) + 6U_{14}^2(1 - U_{14})^2\right] \\
& \cdot \left\{U_{16}^2 U_{17} + (1 - U_{16}^2 U_{17}) \right. \\
& \cdot \left. \left[U_{13}^4 U_{11} U_{12} U_{32} U_{33}(2 - U_{11} U_{12} U_{32} U_{33})\right]\right\} \\
& \cdot U_6 U_{27} U_{15}(2 - U_6 U_{27} U_{15}) \prod_{i=7}^{10} U_i (2 - \prod_{i=7}^{10} U_i)
\end{aligned}
\qquad (3)
$$

The standby configuration of the cycle charge mode is exactly the same as the operational configuration, since there are no additional failure effects in the eclipse season which adversely affect the operational cycle charge mode. Hence, $R_{CYM*} = R_{CYM}$.

b. <u>One Battery Required</u>

The two remaining configurations are considerably more involved than those previously presented. This is to be expected, since with only one battery required for mission success a considerably higher degree of redundancy exists. The reliability diagrams representing the operational and standby configurations of the continuous charge mode are given in Exhibits 8 and 9, respectively. These diagrams are divided into a number of cases representing different conditions of the batteries and series regulators. The cases shown in Exhibit 8, together with the stated conditions, represent all successful situations in the

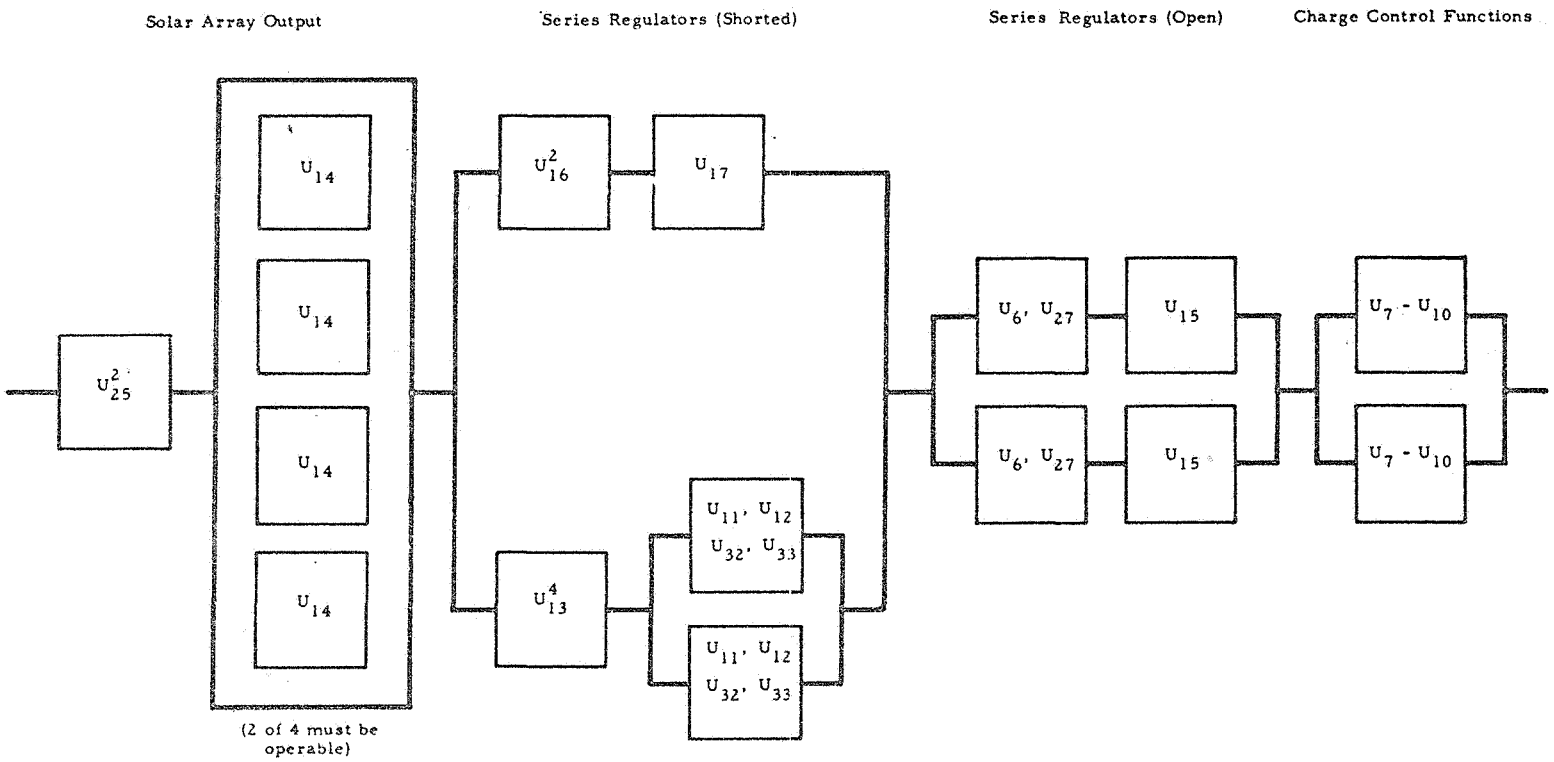
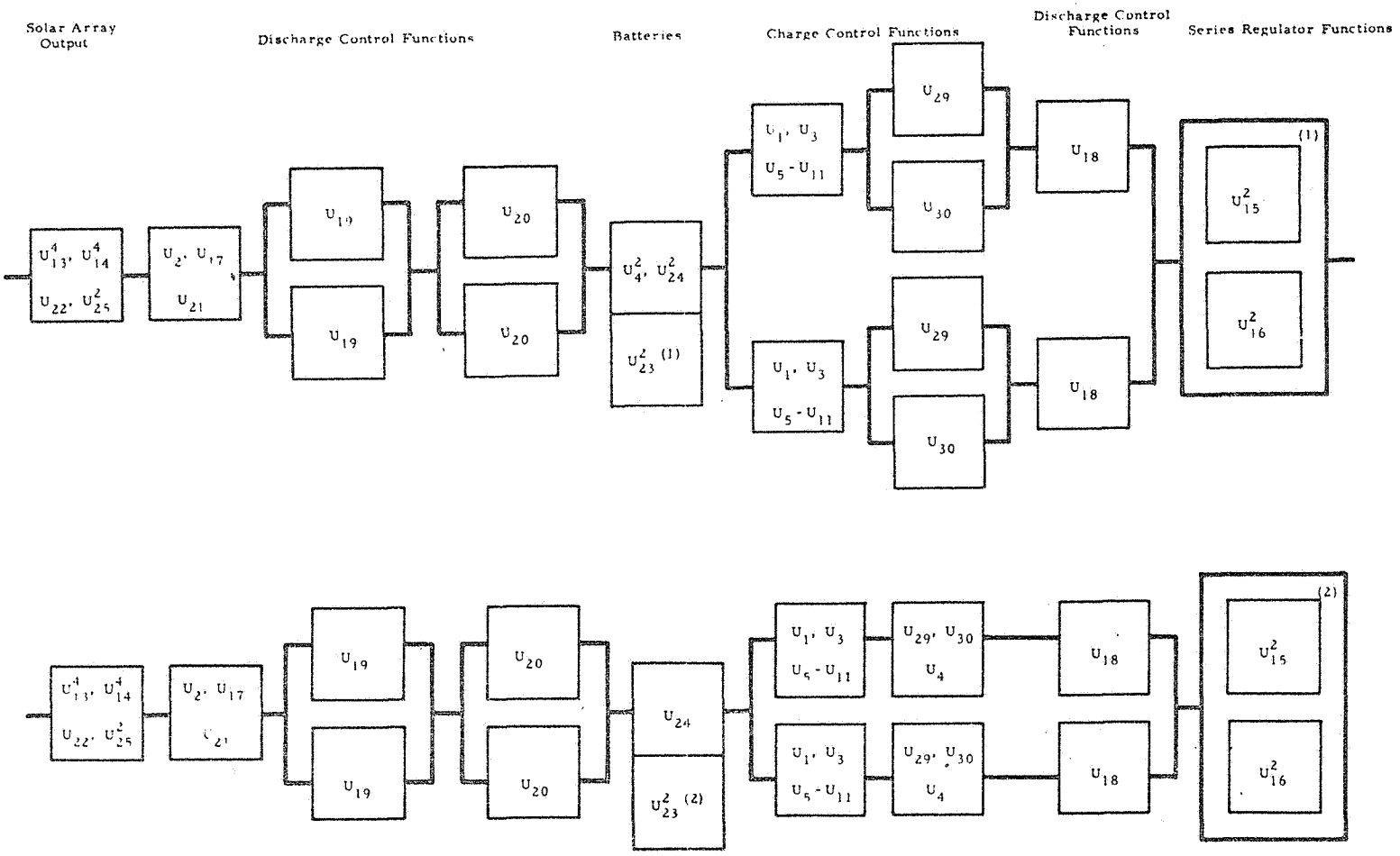
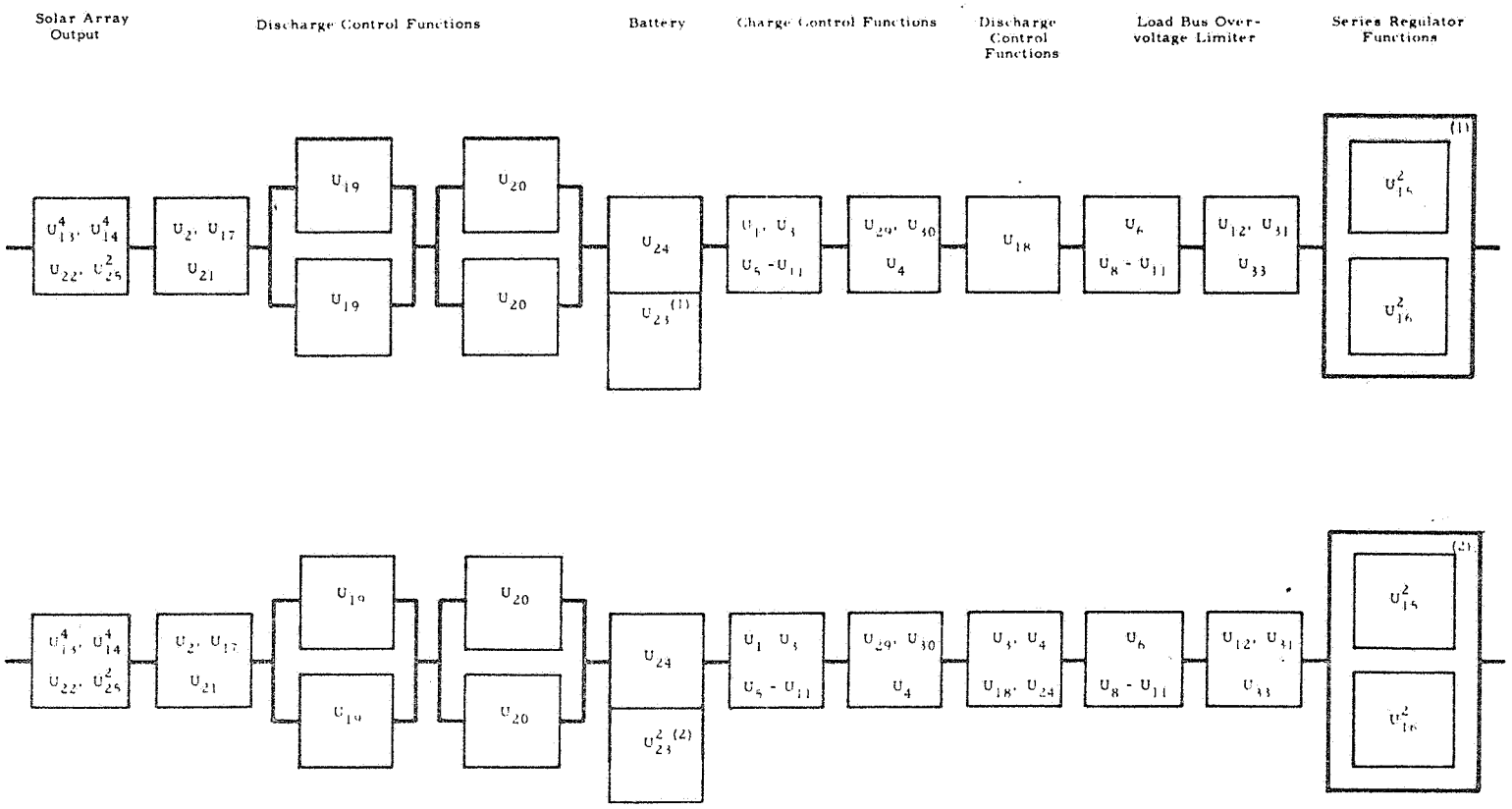


EXHIBIT 7 - RELIABILITY DIAGRAM--CYCLE CHARGE MODE, OPERATIONAL OR STANDBY (ONE OR TWO BATTERIES REQUIRED)



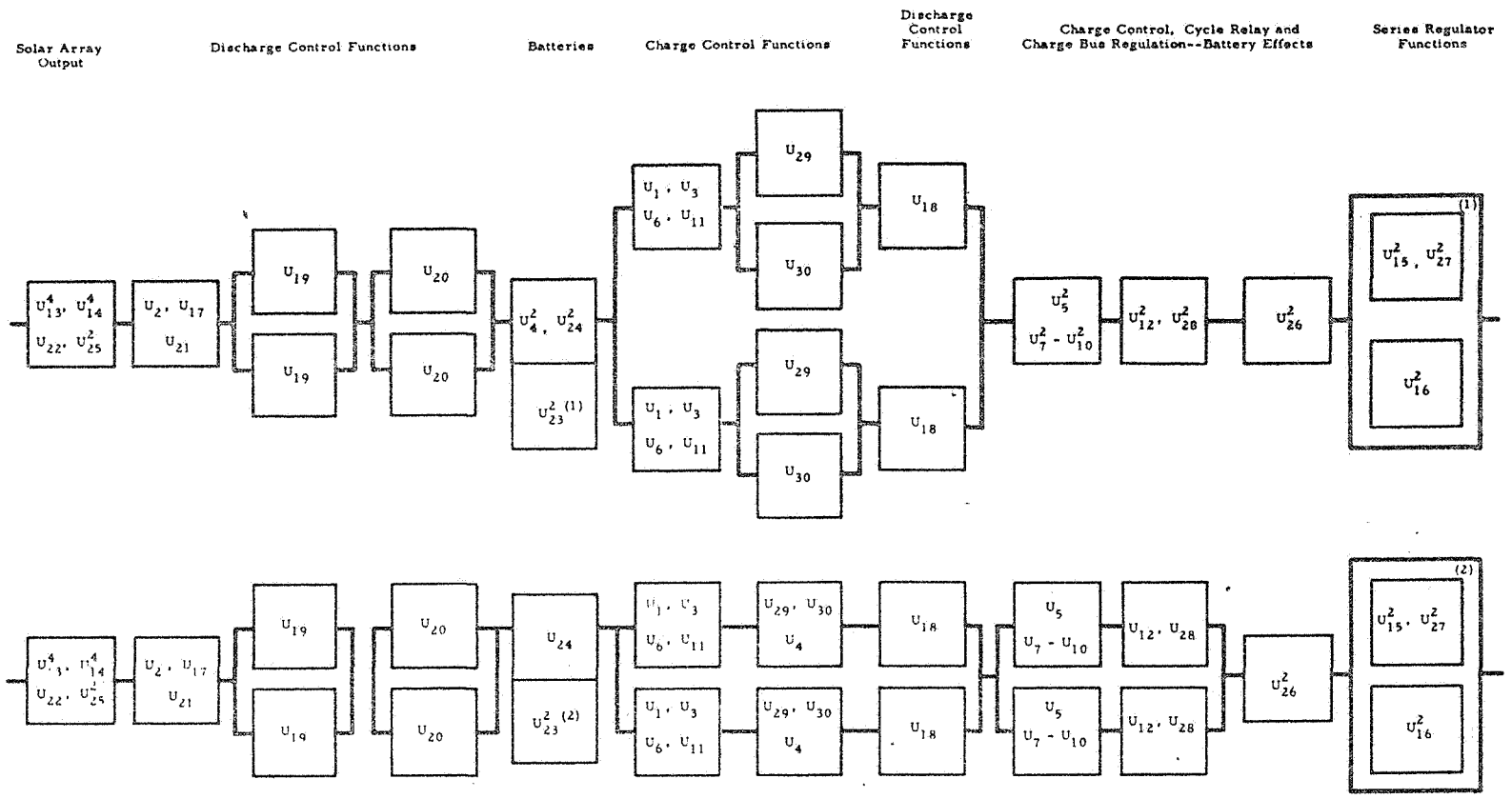
Notes: (1) Case 1: Both series regulators operable OR one series regulator operable, other opened AND both batteries operable.
(2) Case 2: Both series regulators operable OR one series regulator operable, other opened AND one battery operable, other failed.

EXHIBIT 8 - RELIABILITY DIAGRAM--CONTINUOUS CHARGE MODE, OPERATIONAL (ONE BATTERY REQUIRED)



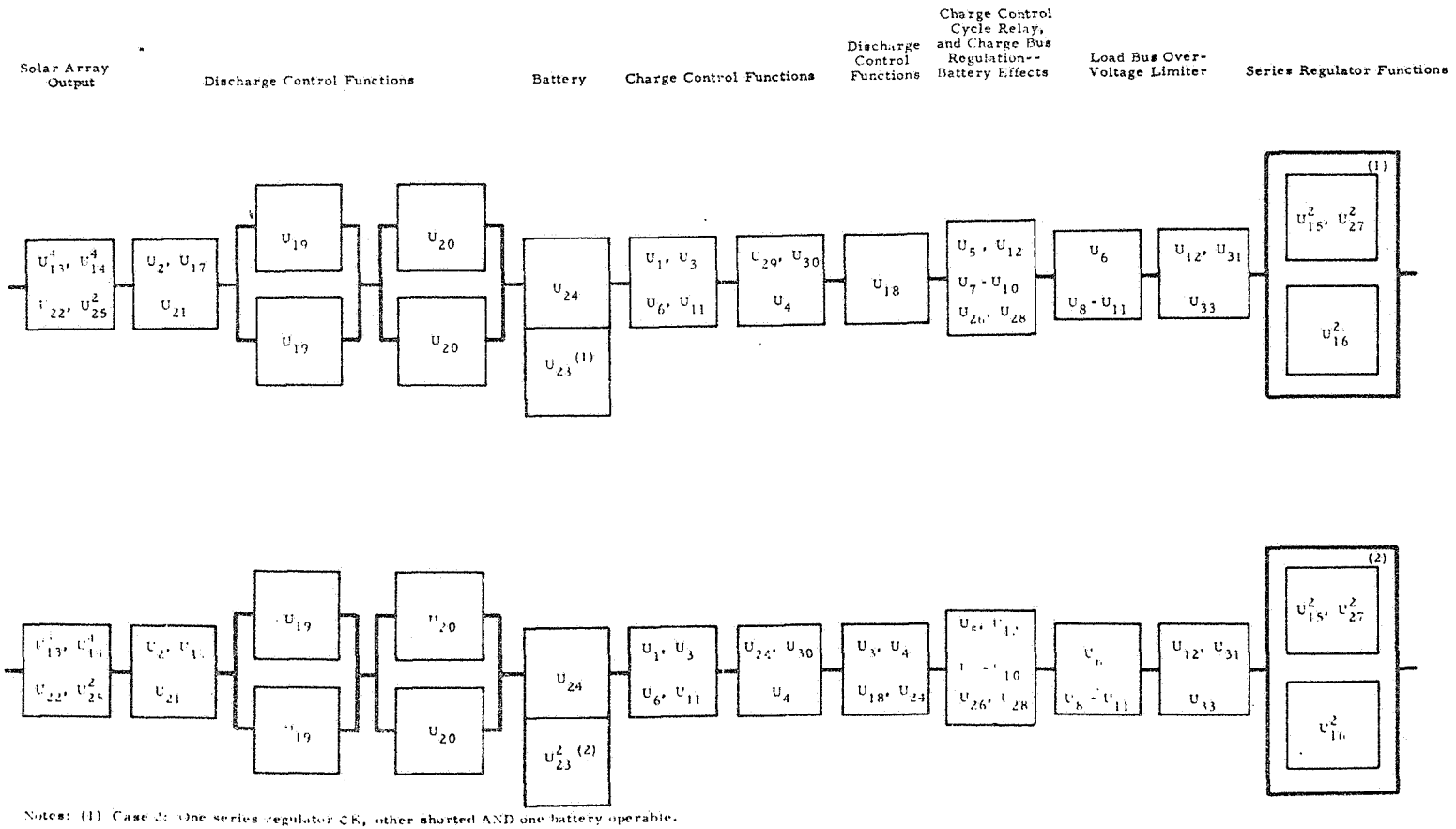
Notes: (1) Case 3: One series regulator OK, other shorted AND one battery operable.
(2) Case 4: One series regulator open, other shorted AND both batteries operable.

EXHIBIT 8 (Continued)



Notes: (1) Case 1: Both series regulators operable OR one series regulator operable, other opened AND both batteries operable.
(2) Case 2: Both series regulators operable OR one series regulator operable, other open AND one battery operable, other failed.

EXHIBIT 9 - RELIABILITY DIAGRAM--CONTINUOUS CHARGE MODE, STANDBY (ONE BATTERY REQUIRED)



Notes: (1) Case 2: One series regulator OK, other shorted AND one battery operable.
(2) Case 3: One series regulator shorted, other open AND both batteries operable.

EXHIBIT 9 (Continued)

operational continuous charge mode configuration where one battery is sufficient. The appropriate reliability expression is[1]

$$R_{COM}^{(1)} = \left[U_{23}^2 R_1 + 2(1 - U_{23})U_{23}R_2\right]\left[U_{15}^2 U_{16}^2 + (1 - U_{15})U_{15}U_{16}^2\right]$$
$$+ 2U_{23}U_{15}U_{16}\left[R_3 U_{15}(1 - U_{16}) + U_{23}R_4(1 - U_{15})(1 - U_{16})\right] \tag{4}$$

where

$$R_1 = U_{13}^4 U_{14}^4 U_{22} U_{25}^2 U_2 U_{17} U_{21} U_{19}(2 - U_{19})U_{20}(2 - U_{20})U_4^2 U_{24}$$
$$\cdot\, U_1 U_3 \prod_{i=5}^{11} U_i \left[U_{29} + U_{30}(1 - U_{29})\right] U_{18}$$
$$\cdot \left\{2 - U_1 U_3 \prod_{i=5}^{11} U_i \left[U_{29} + U_{30}(1 - U_{29})\right] U_{18}\right\}$$

$$R_2 = U_{13}^4 U_{14}^4 U_{22} U_{25}^2 U_2 U_{17} U_{21} U_{19}(2 - U_{19})U_{20}(2 - U_{20})U_4^2 U_{24}$$
$$\cdot\, U_1 U_3 \prod_{i=5}^{11} U_i U_{29} U_{30} U_4 U_{18}\left(2 - U_1 U_3 \prod_{i=5}^{11} U_i U_{29} U_{30} U_4 U_{18}\right)$$

$$R_3 = U_{13}^4 U_{14}^4 U_{22} U_{25}^2 U_2 U_{17} U_{21} U_{19}(2 - U_{19})U_{20}(2 - U_{20})U_4^2 U_{24}$$
$$\cdot\, U_1 U_3 \prod_{i=5}^{11} U_i U_{29} U_{30} U_4 U_{18} U_6 \prod_{i=8}^{11} U_i U_{12} U_{31} U_{33}$$

$$R_4 = R_3 U_3 U_4 U_{24}$$

[1] The superscript (1) is used throughout this subsection to indicate that only one battery is required.

For the standby configuration of Exhibit 9, the appropriate expression is

$$
\begin{aligned}
R^{(1)}_{COM*} = {} & \left[U_{23}^2 R_1^* + 2(1 - U_{23})U_{23}R_2^*\right] \left[U_{15}^2 U_{27}^2 U_{16}^2\right. \\
& \left. + (1 - U_{15}U_{27})U_{15}U_{27}U_{16}^2\right] \\
& + 2U_{23}U_{15}U_{27}U_{16}\left[R_3^* U_{15}U_{27}(1 - U_{16})\right. \\
& \left. + U_{23}R_4^*(1 - U_{15}U_{27})(1 - U_{16})\right]
\end{aligned}
\tag{5}
$$

where

$$
\begin{aligned}
R_1^* = {} & U_{13}^4 U_{14}^4 U_{22} U_{25}^2 U_2 U_{17} U_{21} U_{19}(2 - U_{19})U_{20}(2 - U_{20}) \\
& \cdot U_4^2 U_{24}^2 U_1 U_3 U_6 U_{11}\left[U_{29} + U_{30}(1 - U_{29})\right]U_{18} \\
& \cdot \left[2 - U_1 U_3 U_6 U_{11}\left[U_{29} + U_{30}(1 - U_{29})\right]U_{18}\right] \\
& \cdot U_5^2 \prod_{i=7}^{10} U_i^2 U_{12}^2 U_{28}^2 U_{26}^2
\end{aligned}
$$

$$
\begin{aligned}
R_2^* = {} & U_{13}^4 U_{14}^4 U_{22} U_{25}^2 U_2 U_{17} U_{21} U_{19}(2 - U_{19})U_{20}(2 - U_{20})U_{24} \\
& \cdot U_1 U_3 U_6 U_{11} U_{29} U_{30} U_4 U_{18}(2 - U_1 U_3 U_6 U_{11} U_{29} U_{30} U_4 U_{18}) \\
& \cdot U_5 \prod_{i=7}^{10} U_i U_{12} U_{28}(2 - U_5 \prod_{i=7}^{10} U_i U_{12} U_{28})U_{26}^2
\end{aligned}
$$

$$R_3^* = U_{13}^4 U_{14}^4 U_{22} U_{25}^2 U_2 U_{17} U_{21} U_{19}(2 - U_{19}) U_{20}(2 - U_{20}) U_{24}$$

$$\cdot\ U_1 U_3 U_6 U_{11} U_{29} U_{30} U_4 U_{18} U_5 U_{12} \prod_{i=7}^{10} U_i U_{26} U_{28}$$

$$\cdot\ U_6 \prod_{i=8}^{11} U_i U_{12} U_{31} U_{33}$$

$$R_4^* = R_3^* U_3 U_4 U_{24}$$

Having now derived a reliability equation for each of the eight possible configurations, there remains the problem of combining these expressions to determine the overall subsystem reliability. As Exhibit 1 shows, the cycle charge mode is the normal mode of operation up to 1328 hours. Thus,

$$R_{PSS}(t) = R_{CYM}(t) \qquad 0 \le t \le 1328$$

where PSS = Power Supply Subsystem

t = time (hours) in equivalent mission duration

For the PSS to survive beyond the 1328 hours, the units contained in the standby continuous charge mode (COM*) configuration must be operable for the first 1328 hours as well as those elements contained in the operational cycle charge mode. However, the two are not independent; in fact, the COM* configuration contains essentially all elements found in the CYM configuration. Thus,

$$R_{PSS}(t) = R_{COM*}(t) R_{COM}(t - 1328) \qquad 1328 < t \le 4592$$

Again, for the PSS to survive beyond 4592 hours, the units contained in the standby cycle charge mode (CYM*) configuration must be operable during the eclipse season. However, these units are essentially

all contained in the COM configuration. Thus, the entire PSS reliability expression for the case where two batteries are assumed to be necessary is as follows:

$$
\begin{aligned}
R^{(2)}_{PSS}(t) &= R_{CYM}(t) && 0 \le t \le 1328 \text{ hours} \\
&= R^{(2)}_{COM*}(1328) R^{(2)}_{COM}(t - 1328) && 1328 < t \le 4592 \text{ hours} \\
&= R^{(2)}_{COM*}(1328) R^{(2)}_{COM}(3264) R_{CYM}(t - 4592) && 4592 < t \le 5936 \text{ hours} \\
&= R^{(2)}_{COM*}(2672) R^{(2)}_{COM}(3264) R^{(2)}_{COM}(t - 5936) && 5936 < t \le 9200 \text{ hours} \\
&= R^{(2)}_{COM*}(2672) R^{(2)}_{COM}(6528) R_{CYM}(t - 9200) && 9200 < t \le 9560 \text{ hours}
\end{aligned}
\tag{6}
$$

If it is assumed that one operable battery is sufficient for subsystem operation, Equation (6) is identical to that given above with the superscript (2) replaced with the superscript (1) to denote the different battery assumptions used.

4. Calculations

The failure rates associated with each unit have been given in Exhibit 4. These were derived by simply counting each part/failure mode combination associated with a unit and multiplying it by the following set of failure rates:

Part/Failure Mode	Failure Rate, $\lambda \times 10^{-6}$
Resistor	0.230
Short	0.184
Open	0.046
Diode	0.150
Short	0.015
Open	0.135

Part/Failure Mode	Failure Rate, $\lambda \times 10^{-6}$
Transistor	0.300
Short	0.150
Open	0.150
Capacitor	0.080
Short	0.064
Open	0.016
Winding (transformer, coil, etc.)	0.050
Short	0.010
Open	0.040
Relay	0.200
Contacts Short	0.100
Coil Open	0.100
Battery[1]	24.000

A summary of the failure rate computations is given in Exhibit 10.

Using these values in Equations (1) through (5) results in numerical values of the individual terms of the system reliability expression given in Equation (6). These numerical values are shown in the table below for various time durations of interest.

	Time (Hours of Equivalent Mission Duration)					
	360	1328	1344	2672	3264	6578
$R^{(2)}_{COM}(t)$					0.81	0.65
$R^{(2)}_{COM*}(t)$		0.88	0.88	0.77		
$R_{CYM}(t)$	1.00	0.99	0.99			
$R^{(1)}_{COM*}(t)$					0.94	0.89
$R^{(1)}_{COM*}(t)$		0.93	0.92	0.86		

[1] Battery failure rate is taken as one failure per million hours per cell.

EXHIBIT 10 - UNIT FAILURE RATE CALCULATIONS

Unit Index, U_i	Part/Failure Mode Quantities													Failure Rate, $\lambda_i \times 10^{-6}$
	R		CR		Q		C		T		K		Battery	
	S	O	S	O	S	O	S	O	S	O	S	O	All	
1	10	4	5	7	7	4	1	1	1	1				3.99
2	9	5		6	1	3	1		1	1				2.85
3	10	6	3	5	2	2	4	2	3	3				3.32
4												2		0.20
5	5	7			1	3	1							2.18
6	3	1				3	1							0.83
7		2							1					0.37
8		2	2		4	1								1.14
9	4	4			2	2								1.52
10	2	2	4	4	1	1	1							1.42
11	3	4												0.87
12	2	1												0.27
13	1	2				1								0.56
14				2	1									0.42
15	1	4	1	1	1	2	1							1.44
16	4	1		1	4	1					1	1		1.45
17	6	7		2	1	5	3							2.92
18				2										0.27
19	4	2		1		2								0.98
20												1		0.10
21	5	5	1	2	3	2								2.18
22										1				0.04
23													1	24.00
24										1				0.04
25										2				0.08
26	17	20	3	5	9	9	1				1	1		8.14
27	2	5	2	1	1	1	2							1.60
28	2													0.09
29	2	2												0.46
30	2	2				1								0.61
31	2	4		2	1	1	2							1.52
32				1										0.13
33	1													0.04

Combining these individual terms in accordance with Equation (6) results in numerical values from the Power Supply Subsystem reliability as a function of time. These values are plotted in Exhibit 11 for both the one- and two-battery assumptions.

5. Recommended Power Supply Subsystem Changes

a. General

The functional "system-level" review of the OGO S-50 Power Supply Subsystem reported in TAM No. 34-27 (Reference 1) resulted in several changes which PRC believes would increase the subsystem reliability. The most significant functional changes[1] recommended in TAM No. 34-27 are as follows:

(1) Provide series regulator cross-strapping relays, so that a shorted series regulator can be removed by ground command and additional failure switching can be performed.

(2) Revise the cycle mode cross-strapping provisions, so that only one cycle relay controls the charging of both batteries when the charge buses are connected.

(3) Provide the capability to override[2] the discharge control relays by ground command.

In this section, the predicted reliability of the Power Supply Subsystem, with all three recommended changes incorporated for the case

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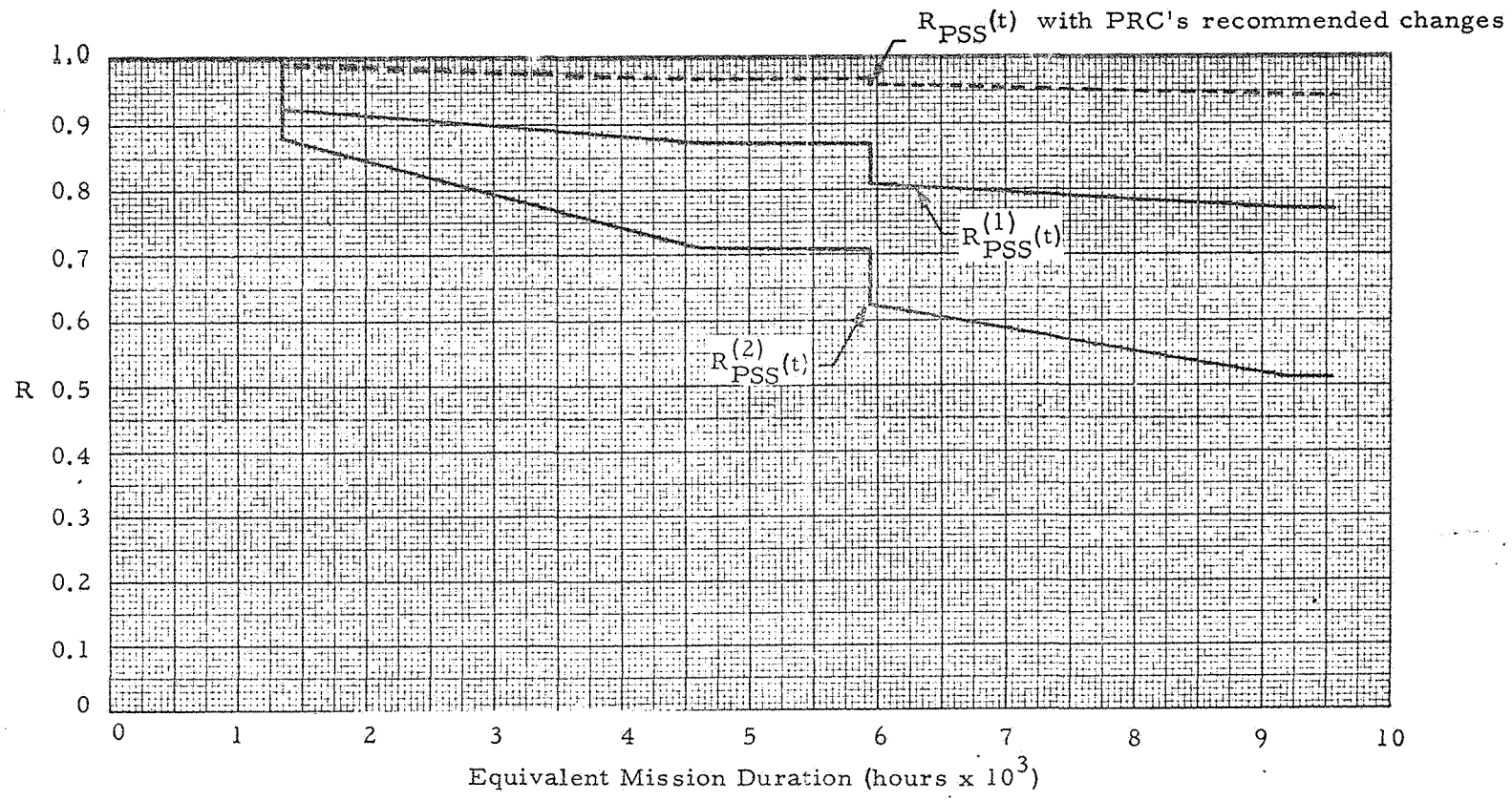
[1] Details of these recommended changes are included in TAM No. 34-27.

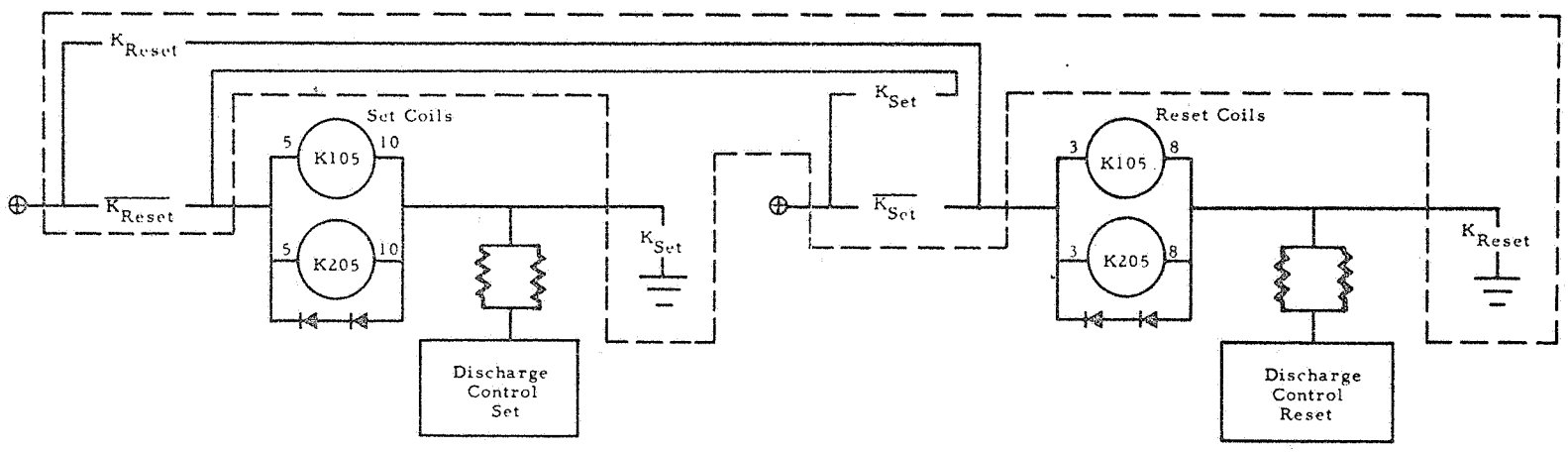
[2] At the time TAM No. 34-27 was written, it was believed that the most significant discharge control consequence would be caused by the failure of the discharge control reset function to deenergize the relays and cause the series regulators to be continuously bypassed. However, subsequent correspondence from STL indicates that subsystem failure will also occur if the series regulators are not bypassed during battery discharge. Therefore, for this portion of this assessment, it is assumed that the capability to both set and reset the discharge control relays by ground command is available. Alternate methods by which both of these features could be incorporated are shown in Exhibits 12 and 13, which are revised versions of the discharge control unit override mechanizations recommended in Exhibits 10A and 10B, respectively, of TAM No. 34-27.



Notes: (1) $R^{(1)}_{PSS}(t)$ = Reliability assuming one battery is sufficient for mission success.

(2) $R^{(2)}_{PSS}(t)$ = Reliability assuming both batteries are required for mission success.

EXHIBIT 11 - POWER SUPPLY SUBSYSTEM RELIABILITY



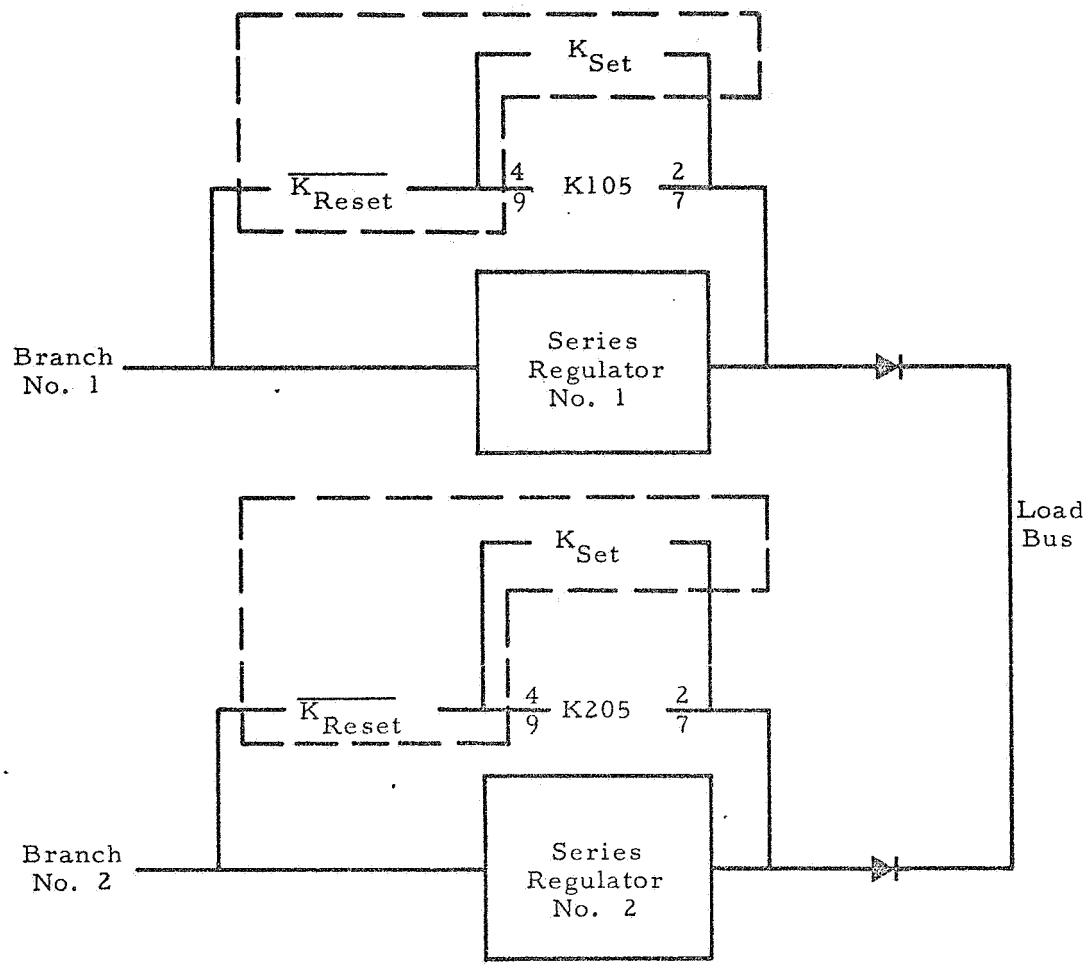
Notes: (1) Additions outlined by dashed lines.

(2) Bar above relay contacts indicates closed contacts when relay is deenergized.

(3) No bar above relay contacts indicates closed contacts when relay is energized.

(4) One additional 4PDT relay and one additional command required for each override function.

EXHIBIT 12 - RECOMMENDED METHOD OF SETTING OR RESETTING DISCHARGE CONTROL RELAYS BY GROUND COMMAND



Notes: (1) Additions outlined by dashed lines.

(2) Bar above relay contacts indicates closed contacts when relay is deenergized.

(3) No bar above relay contacts indicates closed contacts when relay is energized.

(4) One additional 4PDT relay and one additional command required for each override function.

EXHIBIT 13 - RECOMMENDED METHOD OF INTERRUPTING SERIES REGULATORS BYPASS OR MANUALLY BYPASSING SERIES REGULATORS BY GROUND COMMAND

where one battery is required, is calculated for comparison with the predicted reliability of the present configuration.

It should be noted that all of these recommended changes require the command capability since they involve failure switching. Therefore, the Power Supply Subsystem reliability will not be affected by these changes if the command capability has failed.

b. Effects of Recommended Changes on Reliability Prediction

The effects of the recommended changes on the previous reliability predictions are discussed below. The discussion is centered on the redundant battery situation (one battery required), since this assumption allows the greatest latitude in use of the available redundancies. The numerical calculations are not computed for the increased reliability gains effected by the recommended changes for the case where both batteries are required; however, PRC believes the reliability increase for this case would also be significant, since recommendations (1) and (2) are aimed at "saving" the batteries, and recommendation (3) directly affects the "series" elements of all reliability diagrams.

(1) Series Regulator Cross-Strapping

The first recommended change permits a series regulator to be removed from the system whether it is shorted or open. This capability provides two advantages in the operational continuous charge mode in the event a series regulator has shorted (or if one bypass relay is shorted or continuously energized). First, the battery of the associated branch can be "saved" and charged to full capacity in the same manner as if one series regulator had opened. Second, the charge buses can be connected without limiting both batteries to an upper voltage of 34.1 volts. Thus, the charge control functions are now redundant even though a series regulator is shorted, and either charge control function can be used to control the charging of either or both batteries.

In the standby continuous charge mode, this added capability does not "buy" as much unless recommendation (2) is also incorporated.

Without the revised cycle mode configuration, even if a shorted series regulator could be removed, the charge buses would be connected, and one battery would remain on continuous charge at approximately 36 to 37 volts through the deenergized contacts of its cycle relay. For this condition, it is assumed that the battery on continuous charge for the duration of the cycle mode would fail.

(2) Revised Cycle Mode Cross-Strapping

This change will have no effect on subsystem reliability in the operational continuous charge mode, since it only affects the cycle relay function. However, in the standby continuous charge mode the charging of both batteries could be placed under the control of a single cycle relay without causing one of the batteries to remain on continuous charge and fail. Thus, the charge control functions that could cause battery failure, the cycle relay controls, and the charge bus regulation function during battery float are redundant, and either charge control/cycle relay combination can be used to regulate the connected charge buses and to control the charging frequency of both or either of the batteries.

Again, it is emphasized that the charge buses can be connected, thereby making the charge control/cycle relay functions redundant if a series regulator is shorted only if recommendation (1) is also incorporated. However, if both series regulators are operational, or if one is operational and one is open, recommendation (2) alone will provide this capability.

(3) Ground-Commanded Discharge Control Override

This change will permit the discharge control relays to be either set (bypassing the series regulators) or reset (inserting the series regulators) by ground command. Thus, ground command can circumvent failures in the current direction monitors, discharge control set, load bus monitor, and discharge control reset functions in which the discharge control relays are incorrectly set or reset. The elimination of these failure modes applies identically to the series (reliability-wise) elements of both the operational continuous charge and the standby continuous charge mode.

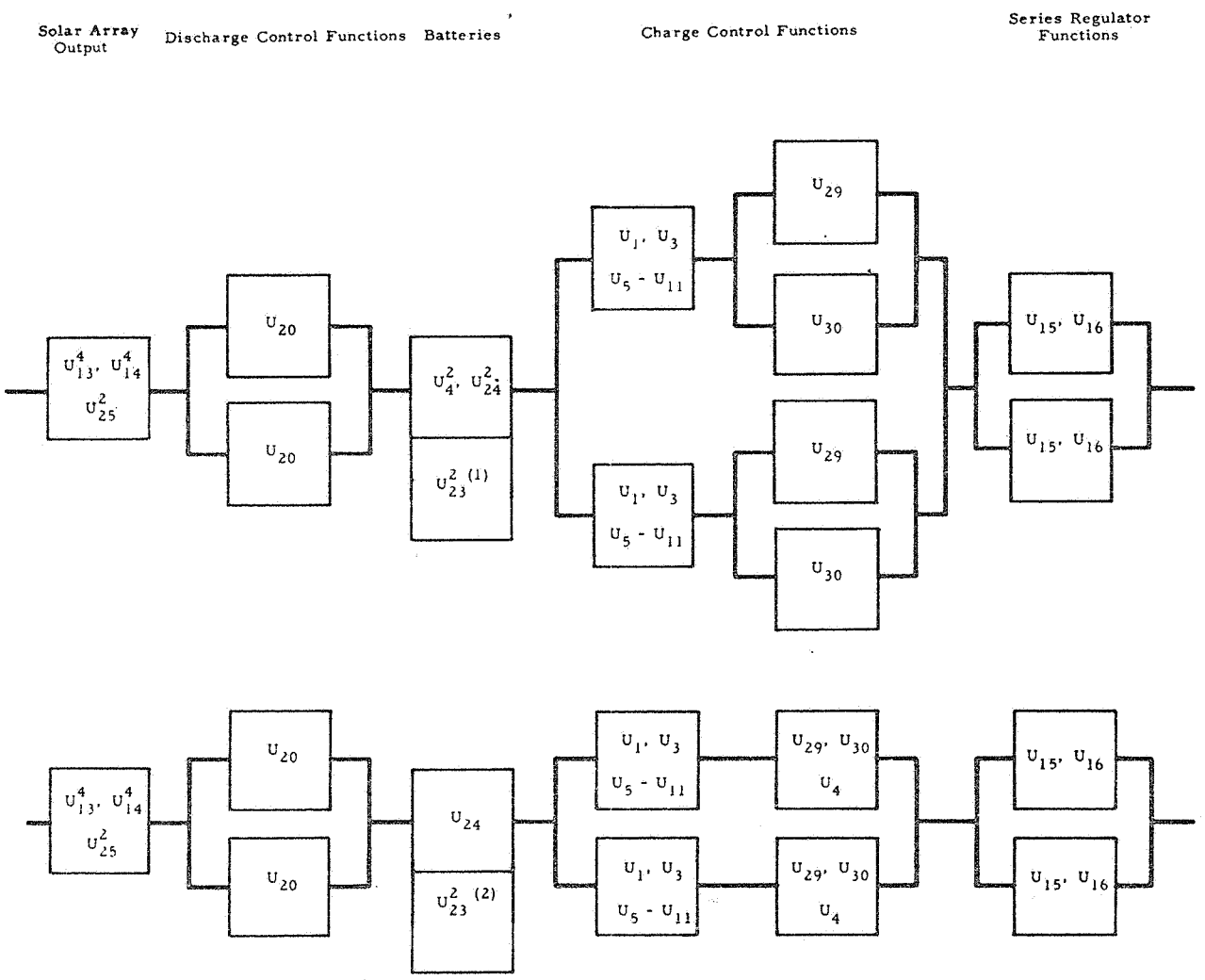
c. Calculations

Exhibits 14 and 15 show the reliability diagrams of the Power Supply Subsystem with the recommended changes included for the continuous charge mode for the case where one battery is required. This is the only configuration analyzed, since no significant mission effects would be noted in the cycle charge mode.

The first of the recommended changes essentially makes the series regulators completely redundant. The only exception would be the situation where one series regulator is shorted and the other is open. The calculations of the previous design, however, showed the probability of this event to be negligible. Hence, this case is omitted from the reliability diagram.

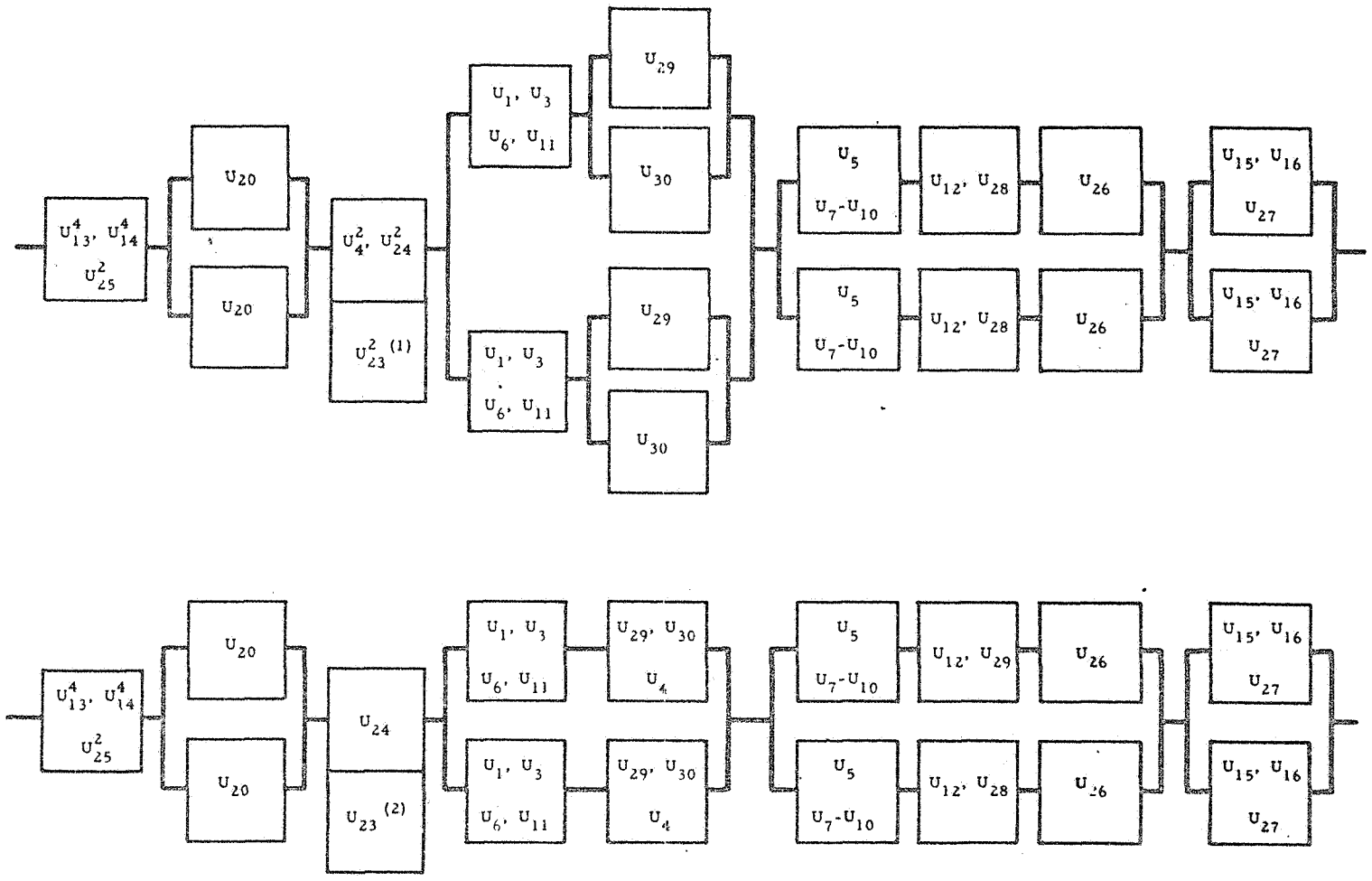
The various terms of the power supply reliability expression given in Equation (6) are listed in the table on page 61 for the time periods of interest. Expressions for the COM and COM* terms are

$$
\begin{aligned}
R_{COM} = {} & U_{23}^2\left(U_{13}^4 U_{14}^4 U_{25}^2 U_{20}(2 - U_{20})U_4^2 U_{24}^2\right) \\
& \cdot \left[U_1 U_3 \prod_{i=5}^{11} U_i \left[U_{29} + U_{30}(1 - U_{29})\right]\right] \\
& \cdot \left\{2 - U_1 U_3 \prod_{i=5}^{11} U_i \left[U_{29} + U_{30}(1 - U_{29})\right]\right\} \\
& \cdot U_{15}U_{16}(2 - U_{15}U_{16}) + 2U_{23}(1 - U_{23}) \\
& \cdot \left[U_{13}^4 U_{14}^4 U_{25}^2 U_{20}(2 - U_{20})U_{24}U_1 U_3 \prod_{i=5}^{11} U_i U_{29} U_{30} U_4\right. \\
& \left. \cdot (2 - U_1 U_3 \prod_{i=5}^{11} U_i U_{29} U_{30} U_4)U_{15}U_{16}(2 - U_{15}U_{16})\right]
\end{aligned}
$$



Notes: (1) Case 1: Both batteries operable.
(2) Case 2: One battery operable, other failed.

EXHIBIT 14 - RELIABILITY DIAGRAM (SUGGESTED)--CONTINUOUS CHARGE MODE, OPERATIONAL (ONE BATTERY REQUIRED)



Notes: (1) Case 1: Both batteries operable.
(2) Case 2: One battery operable, other failed.

EXHIBIT 15 - RELIABILITY DIAGRAM (SUGGESTED)--CONTINUOUS CHARGE MODE, STANDBY (ONE BATTERY REQUIRED)

$$
\begin{aligned}
R_{COM*} = U_{23}^2 \Big(& U_{13}^4 U_{14}^4 U_{25}^2 U_{20}(2 - U_{20}) U_4^2 U_{24}^2 U_1 U_3 U_6 U_{11} \\
& \cdot \left[U_{29} + U_{30}(1 - U_{29})\right] \\
& \cdot \left\{2 - U_1 U_3 U_6 U_{11} \left[U_{29} + U_{30}(1 - U_{29})\right]\right\} \\
& \cdot U_5 \prod_{i=7}^{10} U_i U_{12} U_{28} U_{26} \\
& \cdot (2 - U_5 \prod_{i=7}^{10} U_i U_{12} U_{28} U_{26}) U_{15} U_{16} U_{27} (2 - U_{15} U_{16} U_{27}) \Big) \\
& + 2U_{23} \left[1 - U_{23}\right] \Big[U_{13}^4 U_{14}^4 U_{25}^2 U_{20}(2 - U_{20}) \\
& \cdot U_{24} U_1 U_3 U_6 U_{11} U_{29} U_{30} U_4 \\
& \cdot (2 - U_1 U_3 U_6 U_{11} U_{29} U_{30} U_4) U_5 \prod_{i=7}^{10} U_i U_{12} U_{28} U_{26} \\
& \cdot (2 - U_5 \prod_{i=7}^{10} U_i U_{12} U_{28} U_{26}) U_{15} U_{16} U_{27} (2 - U_{15} U_{16} U_{27}) \Big]
\end{aligned}
$$

where again the U_i's represent the reliabilities of the respective units and the time notation has been uniformly suppressed.

	Time (Hours of Equivalent Mission Duration)					
	360	1328	1344	2672	3264	6578
$R_{COM}(t)$					0.98	0.96
$R_{COM*}(t)$		0.99	0.99	0.98		
$R_{CYM}(t)$	1.00	0.99	0.99			

A curve of power supply reliability versus time is given for this recommended configuration in Exhibit 11.

APPENDIX A

SOLAR ARRAY REQUIREMENTS AND BATTERY DEPTH OF DISCHARGE

1. Solar Array Requirements

a. General

An exact calculation of the required solar array current requirements depends on numerous interdependent parameters of the OGO Power Supply Subsystem equipment. Examples of these are as follows:

(1) Solar Array Characteristics

The precise output of the array is a function of cell degradation, number and distribution of cell failures, temperature, sun incidence angle, and the operating voltage of the various sections (the controlled sections operate at battery voltage whereas the "uncontrolled" sections operate at the limited load bus voltage).

(2) Battery Characteristics

The battery available capacity, current-voltage relation, depth of discharge, and charge efficiency are functions of the load requirements, battery temperature, battery age, depth of discharge history, charge and discharge current rates, upper charge voltage limit, number and frequency of discharge/charge cycles, and number of batteries available.

(3) Solar Array Regulation

The maximum current available for battery recharge and the upper voltage limit are affected by the efficiency and accuracy of the shunt regulators and charge control unit.

(4) Load Current Requirement

Since the total load is composed of a diverse mix of "constant power" and "constant current" devices, the required load current is not a direct function of load bus voltage.

b. Assumptions

Many of the relations cited in the examples above have not been precisely determined; however, even if they were available, inclusion of all interrelated parameters would involve a program which is beyond the scope and accuracy requirements of this assessment. Therefore, for the purpose of calculating a first-order approximation of the minimum solar array current required to supply the load demand and fully recharge the battery during a single sunlight interval following an eclipse, the following simplifying assumptions are made:

(1) Solar Array Output

(a) The total solar array output current capability is a deterministic quantity and diminishes only as a function of time in orbit, but is constant during any sunlight period. The output capability of the solar array is treated in Appendix B. The individual array section configuration,[1] probabilistic cell failures, and radiation degradation are accounted for.

(b) The total solar array current is available for both load requirements and battery recharge (i.e., the uncontrolled sections do not supply the total load requirement and are not regulated by the load bus limiter function).

(2) Battery

(a) The battery voltage profile is a function of discharge and charge times only. The voltage profile used and illustrated in Exhibit A-2B was derived directly from Figure 8, Revision A, Reference 3 (which assumed a discharge current of 4 amperes, and a charge current limit of 5 amperes).

(b) The battery voltage profile is as shown in Exhibit A-2B for one or two batteries.

(c) The battery charge efficiency, η, is constant and equals 0.92 (Reference 4).

---

[1] Each uncontrolled section contains eight parallel strings of six modules each; each controlled section contains seven parallel strings of seven modules each.

(d) The battery charge current can remain at the commanded value for the duration of the sunlight period, rather than decrease as the battery upper voltage is reached.

(3) Solar Array Regulation

The shunt regulators will maintain the battery charge current at the commanded value as long as the array output is sufficient to provide both the load requirement and the charge current. If this condition cannot be met, the charge current will be equal to the array current less the load current.

(4) Load Current Requirements

(a) The load current requirements for eclipse operation, eclipse turn, sunlight operation, and noon turn as a function of load bus voltage were derived from STL engineering sketch, Power Data--POGO-OGO (Reference 5), by dividing the power requirement for each condition by the corresponding voltage level. The average power levels given in this sketch are also assumed to be the load power requirements for the operating periods considered. The resultant current demand curves are plotted in Exhibit A-1.

(b) The load bus voltage is limited at 31.5 volts.

(c) The assumed sequence of events during an orbit is as shown in Exhibit A-2A (taken from Reference 6).

(d) The load current profile during an orbit derived in Exhibit A-2C is representative of all orbits during the eclipse season.[1]

(e) The load current demand for each turn during extended sunlight orbits is the same as that during the eclipse season noon turn.

(f) When both batteries are available, they share the load equally.

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[1] Although this assumption leads to slightly erroneous results for short eclipse orbits, valid results are obtained for the longer eclipse duration orbits, which produce the most demanding array current requirements.

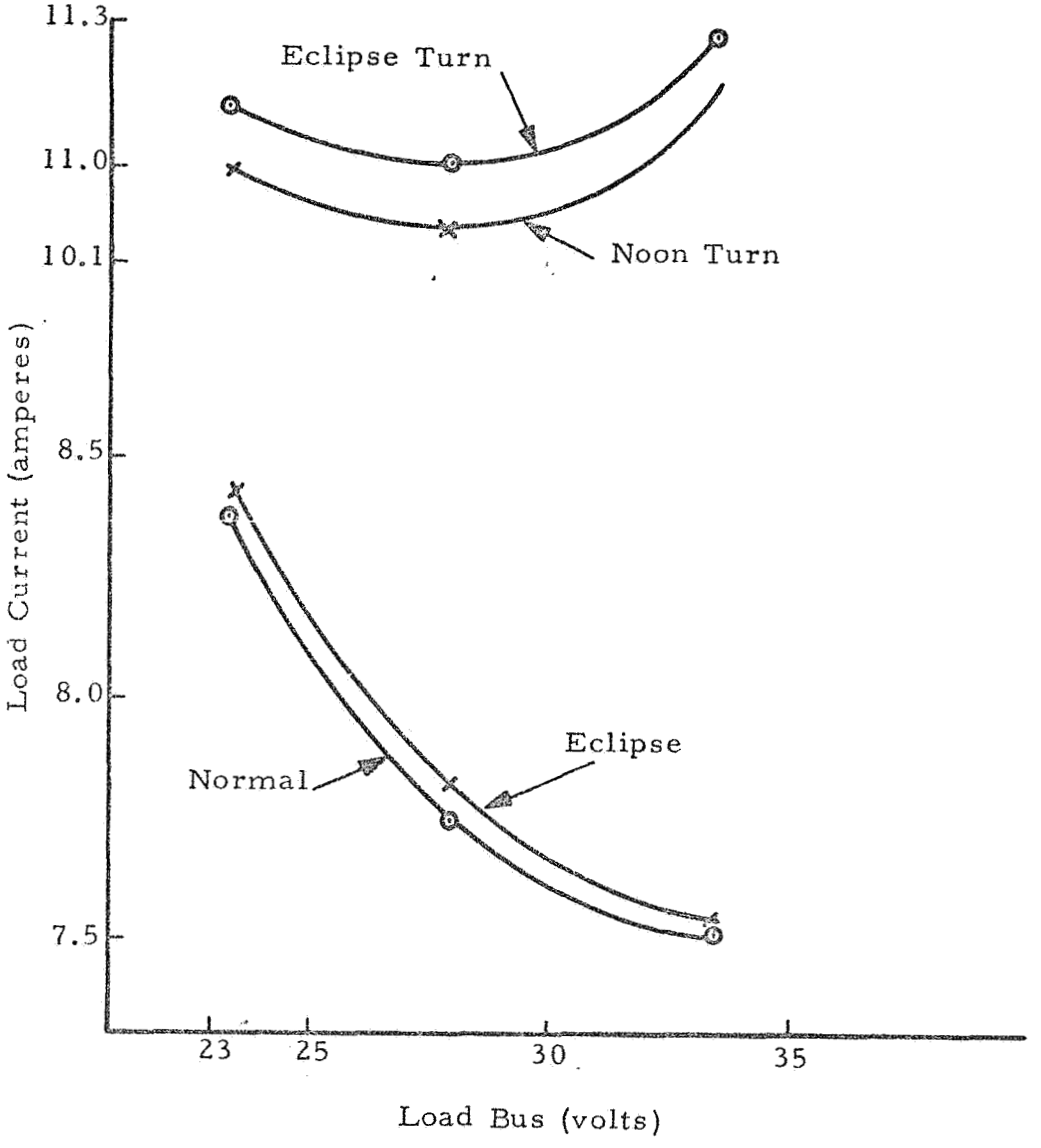

EXHIBIT A-1 LOAD CURRENT REQUIREMENTS AS A FUNCTION OF LOAD BUS VOLTAGE

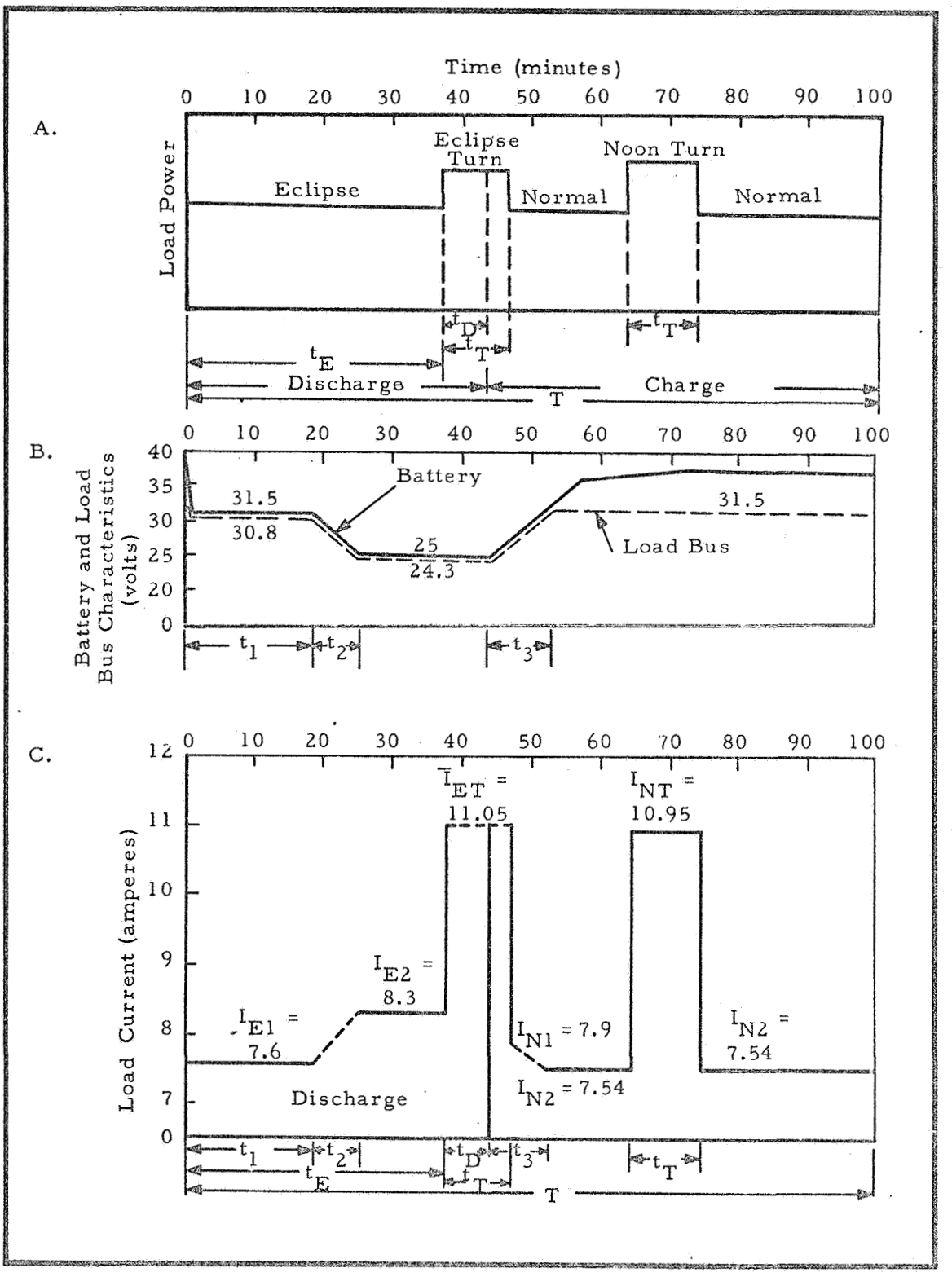

EXHIBIT A-2 BATTERY/LOAD BUS VOLTAGE AND LOW CURRENT DEMAND PROFILES AS A FUNCTION OF ECLIPSE DURATION

EXHIBIT A-2 (Continued)

Notes:

I_{E1} = Load current with battery voltage at first discharge plateau = 7.6 A

I_{E2} = Load current with battery voltage at second discharge plateau = 8.3 A

$\bar{I}_{ET}$ = Average load current during eclipse turn = 11.05 A

I_{N1} = Load current during normal sunlight operation with battery voltage at second discharge plateau = 7.9 A

I_{N2} = Load current during normal sunlight operation with load bus limited at 31.5 volts = 7.54 A

I_{NT} = Load current during noon turn with load bus limited at 31.5 volts = 10.95 A

t_T = Turn time = 10 minutes

t_D = Integrated dark time after eclipse turn = 6.5 minutes

t_1 = Time during discharge battery voltage remains at 31.5 volts = 18 minutes

t_2 = Time during discharge for battery voltage to decay from 31.5 to 25 volts = 7 minutes

t_3 = Time during charge for load bus to reach 31.5 volt limit = 11 minutes

T = Orbital period = 96.5 minutes

(5) General

(a) The solar array continues to face the sun during the noon turn, and the load bus remains limited at 31.5 volts.

(b) The voltage drop across diodes CR106 and CR206 is 0.7 volts.

(c) The integrated dark time during all eclipse turns is 6.5 minutes (as given in Reference 7).

(d) The orbital period is 96.5 minutes.

(e) The maximum eclipse duration is 36 minutes.

(f) Time required for either an eclipse turn or noon turn is 10 minutes.

c. Methodology--Solar Array

The basic condition that must be satisfied to determine the minimum solar array current required to fully recharge the batteries is expressed by the following equation:

$$C = \frac{1}{\eta}(D) \qquad (1)$$

where C = the total charge in ampere hours

D = the total discharge in ampere hours

η = the battery charge efficiency

That is, the total charge withdrawn from the battery during discharge (even if the discharge occurs because the load current is greater than the array current during portions of the sunlight period) must be replaced during the available charge period.

To determine the amount of charge withdrawn from the batteries as a function of eclipse duration, the load current requirement as a function of load voltage was calculated from the data of STL's Power Data--POGO-OGO (Reference 5) and plotted as Exhibit A-1. Secondly, the battery voltage profile as a function of the time during the orbit was taken from preliminary engineering data for design review (Reference 3), as shown in Exhibit A-2B. Then, for each inflection point of the

battery/load bus voltage profile, the corresponding load current was taken from Exhibit A-1 to form the load current profile of Exhibit A-2C. Once this demand current profile was formulated, it was a straightforward matter to calculate the required array current to satisfy Equation (1)[1] for any value of eclipse duration and for any value of commanded maximum charge current. The details of the calculations are included in the next section.

d. Solar Array Requirements

(1) Assumptions

(a) Load current requirements of Exhibit A-1 derived from Reference 5.

(b) Battery voltage profile shown in Exhibit A-2B derived from Figure 8, Revision A, of Reference 3.

(c) Load current profile shown in Exhibit A-2C representative of all orbits during eclipse season.

(d) Load current for both turns during continuous sunlight orbit same as for noon turn.

(e) No dark time during noon turn.

(f) Integrated dark time during all eclipse turns obtained from Reference 7 is approximately 6.5 minutes.

(g) Battery charge efficiency, $\eta = 0.92$.

(h) Orbital period, $T = 96.5$ minutes.

(i) Maximum eclipse duration, $t_E = 36$ minutes.

(2) Calculations

(a) Two Batteries, 5-Ampere Charge Rate

[1] $I_{SA} \leq 10.95$ (batteries discharge during turns)

[1] Both C and D in Equation (1) are a function of the eclipse time, and both can be a function of the array current if the array current is not always greater than the load demand plus the commanded charge rate.

[a] $t_E = 0$ (continuous sunlight)

Total discharge, $D = (I_{NT} - I_{SA})(2\ t_T) = 219 - 20\ I_{SA}$ amp-min.

Available charge, $C_{52} = (I_{SA} - I_{N2})(T - 2\ t_T) = 76.5 I_{SA} - 577$ amp-min.

$$C_{52} = \frac{1}{\eta} D$$

$$76.5 I_{SA} - 577 = \frac{1}{0.92}\left[219 - 20 I_{SA}\right] = 238 - 21.7\ I_{SA}$$

$$I_{SA(min)} = 8.3 \text{ amps}$$

[b] $0 < t_E \leq t \left(I_{SA} = 10.95\right)$

$$D = I_{E1}(t_E) + I_{ET}(t_D) + (I_{ET} - I_{SA})(t_T - t_D) + (I_{NT} - I_{SA})(t_T)$$

$$= 7.6 t_E + 220 - 13.5 I_{SA} \text{ amp-min.}$$

$$C_{52} = \frac{1}{2}(2 I_{SA} - I_{N1} - I_{N2})(t_D + t_3 - t_T) + (I_{SA} - I_{N2})(T - t_E - t_D - t_3 - t_T)$$

$$= 7.54 t_E - 577.6 + (76.5 - t_E) I_{SA} \text{ amp-min.}$$

$$7.54 t_E - 577.6 + (76.5 - t_E) I_{SA} = \frac{1}{0.92}\left[7.6 t_E + 220 - 13.5 I_{SA}\right]$$

$$(91.2 - t_E) I_{SA} = 817 + 0.72 t_E$$

t_E	0+	5	10	15	15.5
I_{SA}	9.0	9.5	10.1	10.8	10.95

[2] $11.05 \leq I_{SA} \leq I_{N2} + 10 = 17.54$

[a] $15.5 < t_E \leq 18$

$$D = I_{E1}(t_E) + I_{ET} + t_D$$

$$= 7.6 t_E + 71.8 \text{ amp-min.}$$

$$C_{52} = (I_{SA} - I_{ET})(t_T - t_D) + \frac{1}{2}(2I_{SA} - I_{N1} - I_{N2})(t_D + t_3 - t_T)$$

$$+ (I_{SA} - I_{N2})(T - t_E - t_D - t_3 - t_T) + (I_{SA} - I_{NT})t_T$$

$$= 7.54t_E - 726 + (90 - t_E)I_{SA} \text{ amp-min.}$$

$$7.54t_E - 726 + (90 - t_E)I_{SA} = \frac{1}{0.92}\left[7.6t_E + 71.8\right]$$

$$(90 - t_E)I_{SA} = 804 + 0.72t_E$$

t_E	16	18
I_{SA}	11.05	11.35

[b] $18 \le t_E \le 25$

$$D = I_{E1}(t_E) + \frac{1}{2}\left[\frac{(I_{E2} - I_{E1})}{t_2}(t_E - t_1)\right](t_E - t_1) + I_{ET}(t_D)$$

$$= 7.6t_E + 71.8 + 0.05(t_E - 18)^2 \text{ amp-min.}$$

C_{52} = Same as d(2)(a)[2][a] = $7.54t_E - 726 + (90 - t_E)I_{SA}$ amp-min.

$$7.54t_E - 726 + (90 - t_E)I_{SA} = \frac{1}{0.92}\left[7.6t_E + 71.8 + 0.05(t_E - 18)^2\right]$$

$$(90 - t_E)I_{SA} = 0.72t_E + 804 + 0.0544(t_E - 18)^2$$

t_E	18	20	22	24	25
I_{SA}	11.35	11.7	12.1	12.5	12.7

[c] $25 \le t_E \le 36$

$$D = I_{E1}(t_1) + \frac{1}{2}(I_{E1} + I_{E2})(t_2) + I_{E2}(t_E - t_1 - t_2) + I_{ET}(t_D)$$

$$= 8.3t_E + 56.8 \text{ amp-min.}$$

C_{52} = Same as d(2)(a)[2] [a] = $7.54t_E - 726 + (90 - t_E)I_{SA}$ amp-min.

$$7.54t_E - 726 + (90 - t_E)I_{SA} = \frac{1}{0.92}\left[8.3t_E + 56.8\right]$$

$$(90 - t_E)I_{SA} = 788 + 1.48t_E$$

t_E	25	30	36
I_{SA}	12.7	13.9	15.3

(b) Two Batteries, 1-Ampere Charge Rate

[1] $I_{SA} \le 10.95$ (batteries discharge during turns)

[a] $t_E = 0$ (continuous sunlight)

$$D = 2(I_{NT} - I_{SA})(t_T) = 219 - 20I_{SA} \text{ amp-min.}$$

$$C_{12} = (I_{SA} - I_{N2})(T - 2t_T), \quad \text{for } I_{SA} \le I_{N2} + 2 = 9.54$$

$$= 76.5I_{SA} - 576.8$$

$$76.5I_{SA} - 576.8 = \frac{1}{0.92}\left[219 - 20I_{SA}\right], \quad I_{SA} = 8.3 \text{ amps}$$

[b] $0 < t_E \le t_{(I_{SA} = 10.95)}$

[i] $I_{SA} \le 9.54$ amps

D = Same as d(2)(a)[1][b] = $7.6t_E + 220 - 13.5I_{SA}$ amp-min.

$$C_{12} = \frac{1}{2}(2I_{SA} - I_{N1} - I_{N2})(t_D + t_3 - t_T) + (I_{SA} - I_{N2})(T - t_E - t_D - t_3 - t_T)$$

$$= 7.54t_E - 578.3 + (76.5 - t_E)I_{SA} \text{ amp-min.}$$

$$7.54t_E - 578.3 + (76.5 - t_E)I_{SA} = \frac{1}{0.92}\left[7.6t_E + 220 - 13.5I_{SA}\right]$$

$$(91.2 - t_E)I_{SA} = 817 + 0.72t_E$$

$$I_{SA} = 9.54, \quad t_E = 5.6 \text{ min.}$$

$$t_E = 0+, \quad I_{SA} = 8.95 \text{ amps}$$

[ii] $9.9 \le I_{SA} \le 10.95$ amps

D = Same as d(2)(a) [1] [b] = $7.6t_E + 220 - 13.5I_{SA}$ amp-min.

$$C_{12} = 2(T - t_E - 2t_T) = 153 - 2t_E \text{ amp-min.}$$

$$153 - 2t_E = \frac{1}{0.92}\left[7.6t_E + 200 - 13.5I_{SA}\right]$$

$$10.26t_E = 14.7I_{SA} - 83$$

$$I_{SA} = 10.95, \quad t_E = 7.5 \text{ min.}$$

[c] $11.05 \le I_{SA} \le I_{NT} + 2 = 12.95$

$7.5 < t_E \le t_{E(max)}$

D = Same as d(2)(a) [2][a] = $7.6t_E + 71.8$ amp-min.

$$C_{12} = (I_{SA} - I_{ET})(t_T - t_D) + (I_{SA} - I_{NT})(t_T) + 2(T - t_E - 2t)$$

$$= 4.8 - 2t_E + 13.5I_{SA}$$

$$4.8 - 2t_E + 13.5I_{SA} = \frac{1}{0.92}\left[7.6t_E + 71.8\right]$$

$$10.26t_E = 13.5I_{SA} - 73.2$$

$$I_{SA} = 12.95 \ , \ t_E = 9.8$$

$$\text{Max charge} \quad C_{12} = 2(T - t_E - t_D) = 180 - 2t_E$$

$$180 - 2t_E = \frac{1}{0.92}\left[7.6t_E + 71.8\right]$$

$$t_{E(max)} = 10.0$$

(c) <u>One Battery, 5-Ampere Charge Rate</u>

[1] $I_{SA} \leq 10.95$ (battery discharges during turns)

[a] $t_E = 0$ (continuous sunlight)

Same as d(2)(a)

$I_{SA} = 8.3$ amps

[b] $0 < t_E \leq t_{(I_{SA} = 10.95)}$

Same as d(2)(a)[2]

$t_{E_{(I_{SA} = 10.95)}} = 15.5$

[2] $11.05 \leq I_{SA} \leq I_{N2} + 5 = 12.54$

[a] $15.5 \leq t_E \leq t_{(I_{SA} = 12.54)}$

Same as d(2)(a)

[b] $18 \le t_E \le 25$

Same as d(2)(a)[2]

$$(90 - t_E)I_{SA} = 0.72t_E + 804 + 0.0544(t_E - 18)^2$$

$$I_{SA} = 12.54t_E = 24.5 \text{ min.}$$

[3] $I_{SA} \ge I_{N1} + 5 = 12.9$, for $25 \le t_E \le t_{E(max)}$

[a] $t_{E_{max}}$

D = Same as d(2)(a)[2] = $8.3t_E + 56.8$ amp-min.

$$C_{51(max)} = 5(T - t_E - t_D) = 450 - 5t_E, \quad \text{for } I_{SA} \ge 16.05$$

$$450 - 5t_E = \frac{1}{0.92}\left[8.3t_E + 56.8\right]$$

$$t_{E(max)} = 27.7$$

[b] $25 \le t_E \le 27.7$

$$C_{51} = (I_{SA} - I_{ET})(t_T - t_D) + (I_{SA} - I_{NT})(t_T) + 5(T - t_E - 2t_T)$$

$$= 234 - 5t_E + 13.5I_{SA}$$

$$234 - 5t_E + 13.5I_{SA} = \frac{1}{0.92}\left[8.3t_E - 56.8\right]$$

$$13.5I_{SA} = 14.02t_E - 172$$

t_E	25	26	27	27.7
I_{SA}	13.2	14.2	15.3	16.05

e. Depth of Discharge

(1) Assumptions

(a) $I_{SA} \geq I$ required for full battery recharge in one sunlight period.

(b) No dark time during noon turn.

(c) Integrated dark time during all eclipse turns, $t_D = 6.5$ minutes.

(d) Average load current during eclipse turn, $I_{ET} = 11.05$ amperes.

(e) Battery voltage and current profiles as shown in Exhibit A-2 for all configurations (i.e., one or two batteries and 1, 5, or 10 ampere charge rate commanded, as required).

(f) Maximum eclipse duration, $t_{E_M} = 36$ minutes.

(2)

(a) $0 < t_E \leq 18$

$$D_1 = \frac{1}{60}\left[7.6t_E + 71.8\right] \text{amp-hours}; \quad D_2 = \frac{1}{2} D_1 .$$

(b) $18 \leq t_E \leq 25$

$$D_1 = \frac{1}{60}\left[7.6t_E + .05(t_E - 18)^2 + 71.8\right]$$

(c) $25 \leq t_E \leq 36$

$$D_1 = \frac{1}{60}\left[8.3t_E + 56.8\right] \text{amp-hours}; \quad D_2 = \frac{1}{2} D_1 .$$

t_E	0	18	25	36
D_1	1.2	3.5	4.6	5.9
D_2	0.6	1.7	2.3	3.0

f. Results

The results of the calculations are presented in Exhibit A-3, which shows both the minimum array current requirement to fully recharge the batteries as a function of eclipse duration for any power supply status, and the maximum eclipse duration that can be tolerated for a given battery charge current limit. The following conclusions are evident from Exhibit A-3:

(1) When the charge current is limited to 1 ampere, the batteries can be recharged only if the eclipse is less than 10 minutes. For longer eclipses, the 5-ampere charge rate is required.

(2) When one battery has failed, the 5-ampere charge rate provides sufficient recharge capability only for eclipse durations of less than 27.7 minutes. Thus, for longer eclipses when one battery is failed, the 10-ampere charge rate is required.

(3) For the normal operating case (i.e., where the 5-ampere charge rate is commanded with both batteries available, and the 10-ampere charge rate is commanded with one battery failed), the minimum array current requirement for a 36-minute eclipse duration is 15.3 amperes.

(4) During the extended sunlight period, the minimum array current requirements is 8.3 amperes.

2. Battery Depth of Discharge

a. General Methodology and Assumptions

The battery depth of discharge is a function of the same interacting battery characteristics and load current demands as previously discussed for determining the solar array current requirements. Thus, the battery and load current assumptions listed in the previous section were followed in computing the depth of discharge as a function of eclipse duration. For brevity, these assumptions[1] are

[1] It should be noted that the previously cited assumptions state that the voltage profile is the same for either the one or two battery case; thus, the depth of discharge for a single battery is precisely twice that for each battery when both are available to share the load.

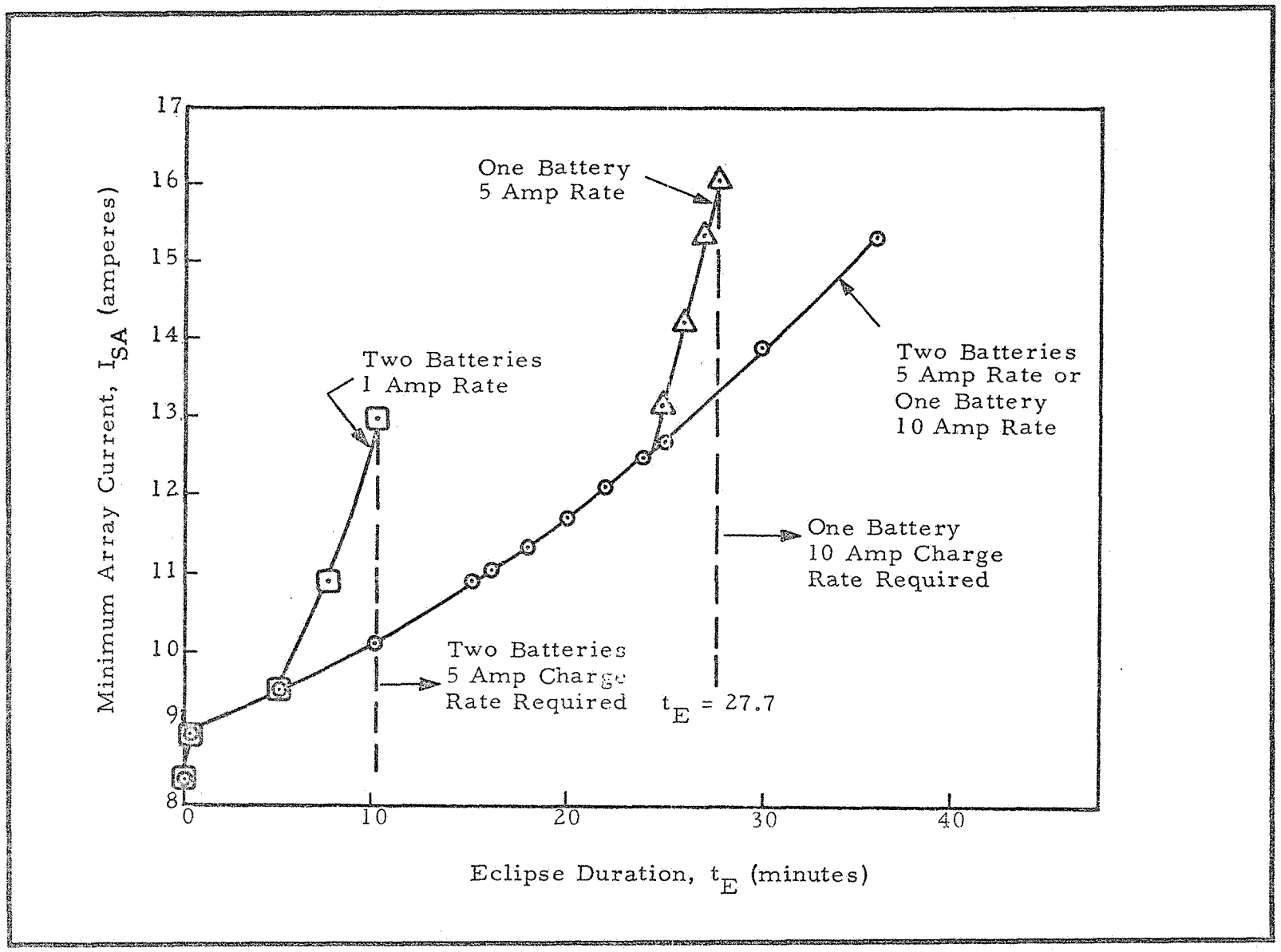

EXHIBIT A-3 MINIMUM ARRAY CURRENT REQUIREMENTS

not repeated here. In addition, to simplify the calculations, it was assumed that the array current during sunlight is always greater than the load current demand (i.e., the batteries discharge only during the eclipse and the first 6.5 minutes of the eclipse turn, but not during any of the ensuing sunlight time).

In essence, the charge supplied by the batteries or battery is the time integral of the discharge current shown in Exhibit A-2C during the total dark time. Thus, the equations for calculating the battery depth of discharge are identical to those used to calculate the "D" term of Equation (1).[1] The details for the calculations are included in 1.d.(2) of this appendix.

b. Results

The results of the calculations are presented in Exhibit A-4, which shows the battery depth of discharge as a function of eclipse duration.

With both batteries available to supply the load, the maximum discharge is approximately 3 ampere hours. Thus, the maximum depth of discharge will only reach 25 to 30 percent, depending on the available capacity of the batteries.

On the other hand, with one battery failed, the maximum discharge is twice as great, or approximately 5.9 ampere hours. This discharge calculation is considered conservative, since it was assumed that the voltage profile of a single battery would be the same as that shown in Exhibit A-2B for the two-battery case, even though the load current demand would be twice as high. However, even this conservative calculation will produce a depth of discharge of 50 to 60 percent--again depending on the available battery capacity. Without test data to prove that a battery will not fail when subjected to repeated discharges of 50 to 60 percent, it is imprudent to believe that a single battery will survive the deep-eclipse season if the other battery has failed. Therefore, it

[1] Recall it is assumed that the batteries discharge only during the dark time and not during any of the high current demand times of the sunlight period.

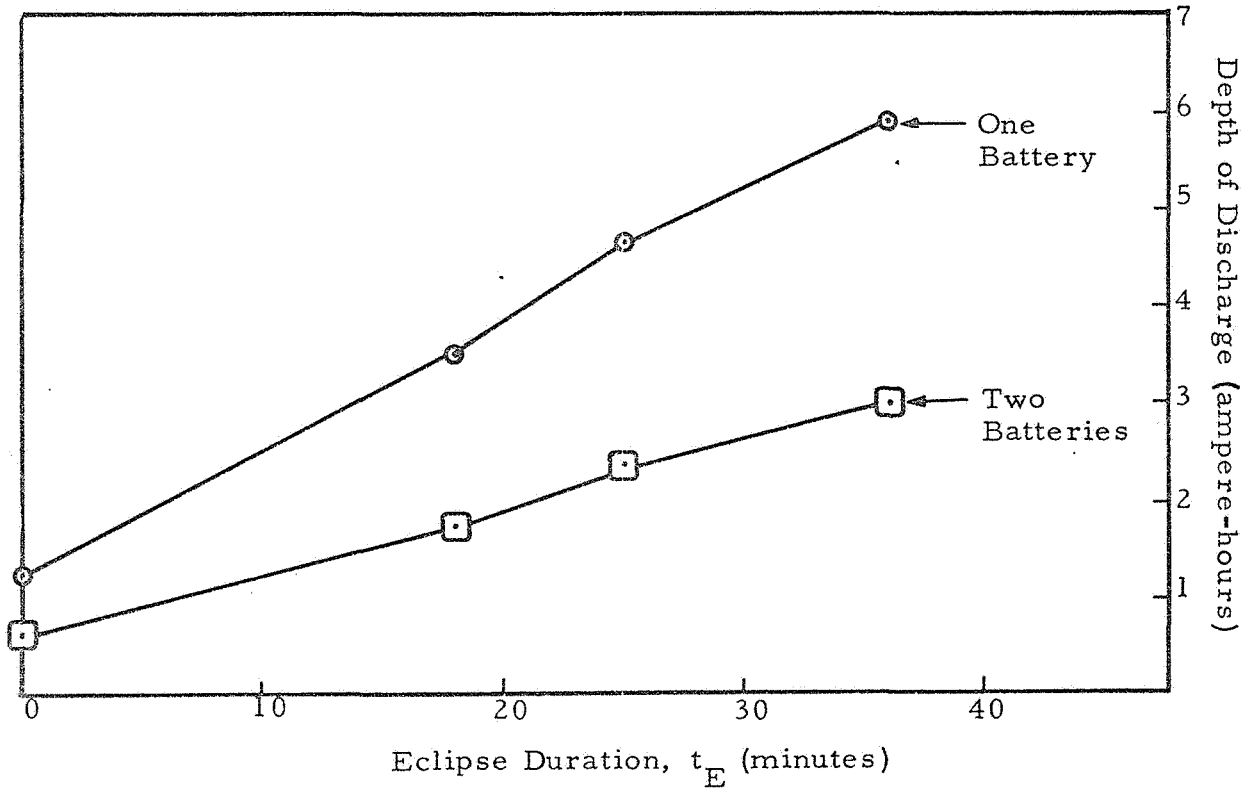

EXHIBIT A-4 BATTERY DEPTH OF DISCHARGE

is PRC's contention that there is a significant likelihood that the batteries are not truly redundant and that both batteries are required for mission success during the eclipse season.

APPENDIX B

SOLAR ARRAY CAPABILITY

1. General

The solar array as presently configured is not expected to provide the current necessary for full operation of the spacecraft and experiments for a full year. This situation is the result of the radiation to the solar cells due to solar protons and the products of the Starfish nuclear test.

Two analyses of the expected lifetime of the array have been prepared by STL for several proposed configurations (References 4 and 6). Neither of these, however, is directly applicable to the present array configuration or the array output requirements as determined by PRC. For these reasons, an analysis has been conducted, using the radiation fluxes and damage curves derived by STL, for the present array configuration and the output requirements determined by PRC.

2. Array Output Determination

The radiation fluxes used by STL in their analyses are consistent with the conclusions reached by most investigators. The damage curves were obtained under NASA contracts and are adequately substantiated in References 8 to 10. An array temperature of 70° C is assumed.

As determined in Appendix A, the total array output requirement is 15.3 amperes during battery charging periods.

The degradation factors used for this computation are as follows:

Electron flux = 8.9×10^{13} equivalent 1-Mev electrons/flat cm^2-year

Proton flux = 1.1×10^{13} equivalent 1-Mev electrons/flat cm^2-year

Cover glass and adhesive transmission loss (initial-constant) = 6 percent

Transmission loss from radiation (linear) = 2 percent

Transmission loss from UV radiation (linear) = 1 percent

Random cell failures and micrometeorite damage (linear) = 5 percent

Solar intensity variation (earth at aphelion-constant) = 3.5 percent

The operating voltage points used for the solar array sections are as follows:

Controlled sections = 37.5 volts

Uncontrolled sections = 33.5 volts

The cell voltages corresponding to these conditions are

Controlled sections = 37.5/112 = 0.335 volts

Uncontrolled sections = 33.5/96 = 0.349 volts

The cell current capability at these operating voltage points for new cells and for cells radiated with 10^{14} 1-Mev electrons per square centimeter are

Controlled Sections

Cell current (new-bare) = 62.5 ma

Cell current (radiated-bare) = 57 ma

Uncontrolled Sections

Cell current (new-bare) = 61 ma

Cell current (radiated-bare) = 54 ma

Array section currents corresponding to the specified operating conditions for two paddles are

Controlled Sections

Section current (new-bare) = $62.5 \times 10^{-3} \times 49 \times 4$ = 12.44 amp

Section current (radiated-bare) = $57 \times 10^{-3} \times 49 \times 4$ = 11.16 amp

Uncontrolled Sections

Section current (new-bare) = $61 \times 10^{-3} \times 56 \times 2$ = 6.82 amp

Section current (radiated-bare) = $54 \times 10^{-3} \times 56 \times 2$ = 6.04 amp

By degrading the currents derived by the appropriate factors for the new and the 1-year-old conditions, the expected array current capability can be determined at those points in time. For a new array, the applicable initial degradation factors are the cover glass and adhesive transmission

loss of 6 percent, and the solar intensity variation of 3.5 percent, yielding a total degradation of 9.5 percent. For a 1-year-old array, the maximum value of the remaining linear degradation factors is applicable, in addition to those applied to a new array, yielding a total degradation factor of 17.5 percent. The section currents can be determined as follows:

Controlled section (new) = 12.44 x 0.905 = 11.26 amp

Controlled section (after 1 year) = 11.6 x 0.825 = 9.21 amp

Uncontrolled section (new) = 6.82 x 0.905 = 6.17 amp

Uncontrolled section (after 1 year) = 6.04 x 0.825 = 4.98 amp

The total array current then is

Array current (new) = 11.26 + 6.17 = 17.43 amp

Array current (after 1 year) = 9.21 + 4.98 = 14.19 amp

Exhibit B-1 shows a curve of array current versus time. On the basis of these values of array current capability, the array could supply the current necessary for spacecraft and full experiment operation for 215 days, and for spacecraft and half experiment operation for approximately 385 days. The latter condition could be accomplished by operating the experiments on a duty cycle basis for the last 5 months of the mission.

3. Additional Considerations

The array current distribution of the preceding paragraphs is an approximation based on several assumptions. The array temperature of 70° C assumed for the calculations is very close for the majority of the time that the array is in sunlight. Just after eclipse, however, the array temperature rises from approximately 10° C to 70° C in approximately 24 minutes. During this period, the current-voltage characteristic of the solar cell shifts from lower current at higher voltage to higher current at lower voltage, as shown in Exhibit B-2. This results in a slightly pessimistic overall effect, owing to the assumptions of 70° C, since the battery voltage at the beginning of the charge period is approximately 25 volts instead of approaching 37.4 volts (see Exhibit 2 in Reference 1).

In addition to the temperature factor, some experimenters think that the low-altitude artificial electron belt injected by Starfish is

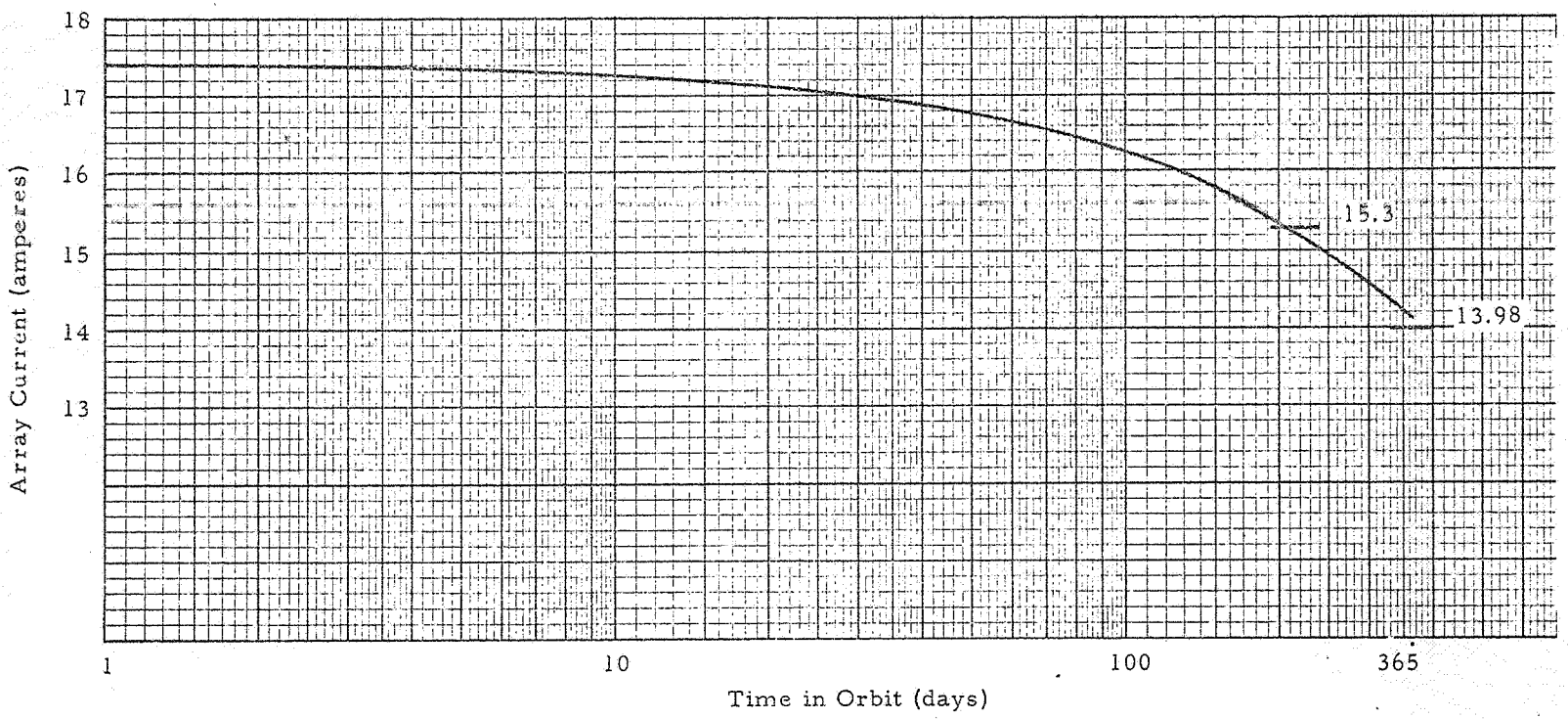

EXHIBIT B-1 ARRAY CURRENT VERSUS TIME IN ORBIT

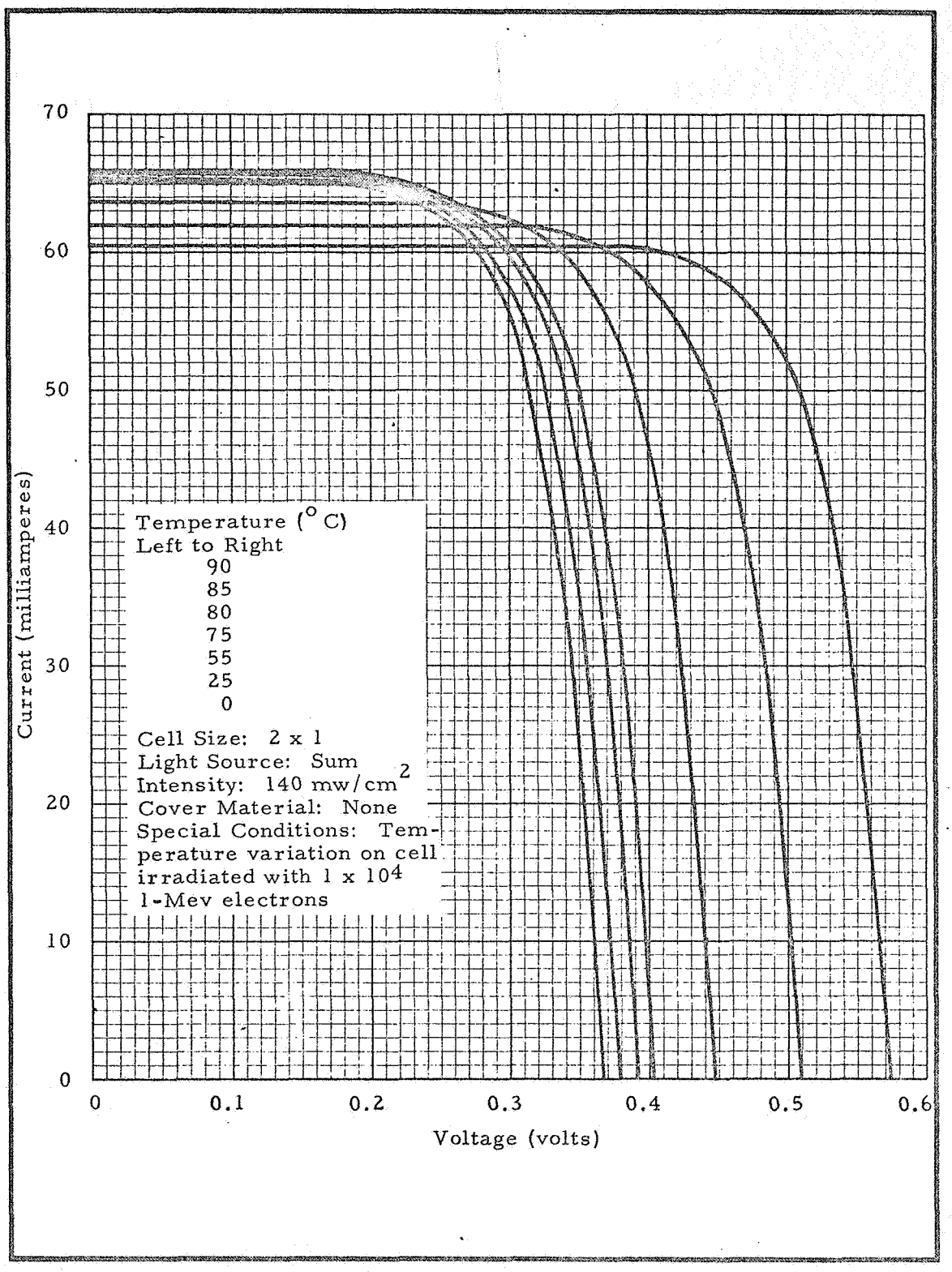

EXHIBIT B-2 SOLAR CELL CURRENT-VOLTAGE CHARACTERISTICS

somewhat less intense than indicated by the STL reference (see Reference 12). If this is true, this factor would also cause the results of this analysis to be slightly pessimistic.

This may be offset, however; STL has stated (Reference 6) that some of their more recent data indicates that the transmission loss of cover glass and adhesive from particle radiation may reach 11 percent rather than the 2 percent used here, and that the uncertainty in solar intensity may be 2 percent rather than none. At the same time, the new data indicates an initial transmission loss, owing to the cover glass and adhesive, of 2 percent instead of the 6 percent used. These factors would result in an optimism of the present results at the end of 1 year. The new data, however, is based on a few data points and is not yet considered statistically sound.

The overall effect of these considerations, then, is that there is a possibility that the present estimate of the solar array is slightly pessimistic. In this event it is improbable but not impossible that the array might in fact be just capable of supporting the spacecraft and the full experiment load for a full year, so long as the rest of the power supply continues to operate in an efficient fashion.

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TECHNICAL ADVISEMENT MEMORANDUM NO. 34-30

POGO EXPERIMENT PROGRAMMER ASSESSMENT

PRC D-842

31 August 1964

Prepared by

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Winifred C. Graham

Approved by

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TECHNICAL ADVISEMENT MEMORANDUM NO. 34-30

To: Assistant OGO Project Manager
From: PRC OGO Reliability Assessment Team
Subject: POGO Experiment Programmer Assessment

1. Introduction

This Technical Advisement Memorandum (TAM) reviews the proposed design of the POGO experiment programmer and evaluates its implications on spacecraft and mission reliability. Converter 10, which powers the experiment programmer, is considered separately here, and the experiment programmer is considered as including only those circuits shown on STL Drawing EG214499. However, the five additional latching relays required, but not shown on EG214499, are included in the analysis.

2. Programmer Operation

The experiment programmer can be viewed (Exhibit 1) as a black box requiring +16, +9, and -6 volts from converter 10 to power the digital modules, and +28 volts from the +28 volt bus for powering the latching relay and for switching at various duty cycles to selected experiments. According to the Specification for an Experiment Programmer Assembly for the S-50 Spacecraft, the inputs required to control this +28 volts with a variable duty cycle are the 0.01-pps signal from the low-frequency timing assembly (LFTA) and three command lines from the command distribution unit (CDU). The variable duty cycle +28 volts can then go to, at most, five different experiments via latching relays, each of which has been placed in series with the normal power control relay. For simplicity, the latching relays are shown in Exhibit 1 as simple switches with no coils.

In STL Drawing EG214499 (Exhibit 2, based on EG214499), the portion of the experiment programmer called the four-stage counter counts the number of 0.01-pps input signals through 16 (binary 0 through binary

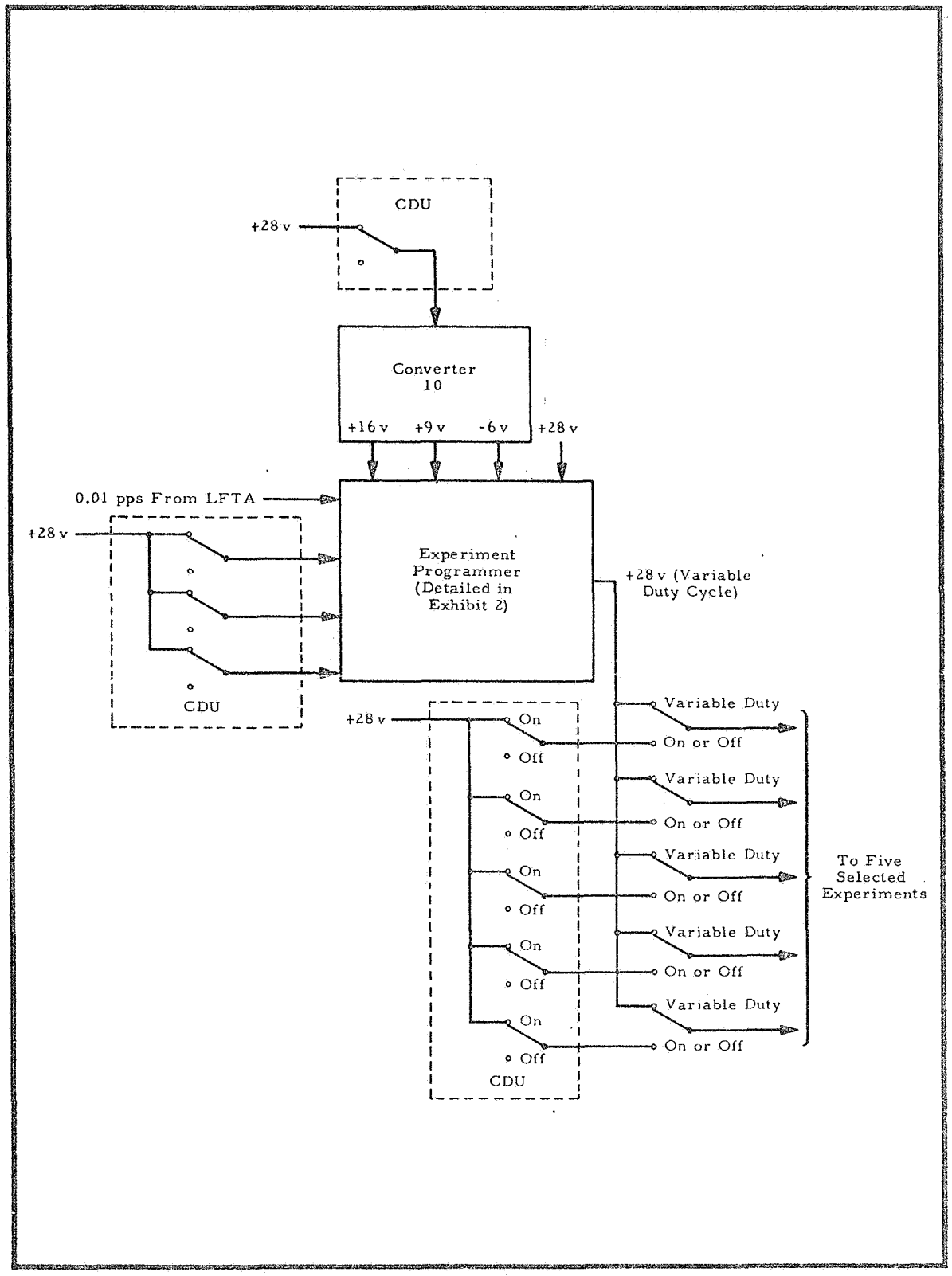


EXHIBIT 1 - FUNCTIONAL DIAGRAM, POGO EXPERIMENT PROGRAMMER AND ASSOCIATED CIRCUITS

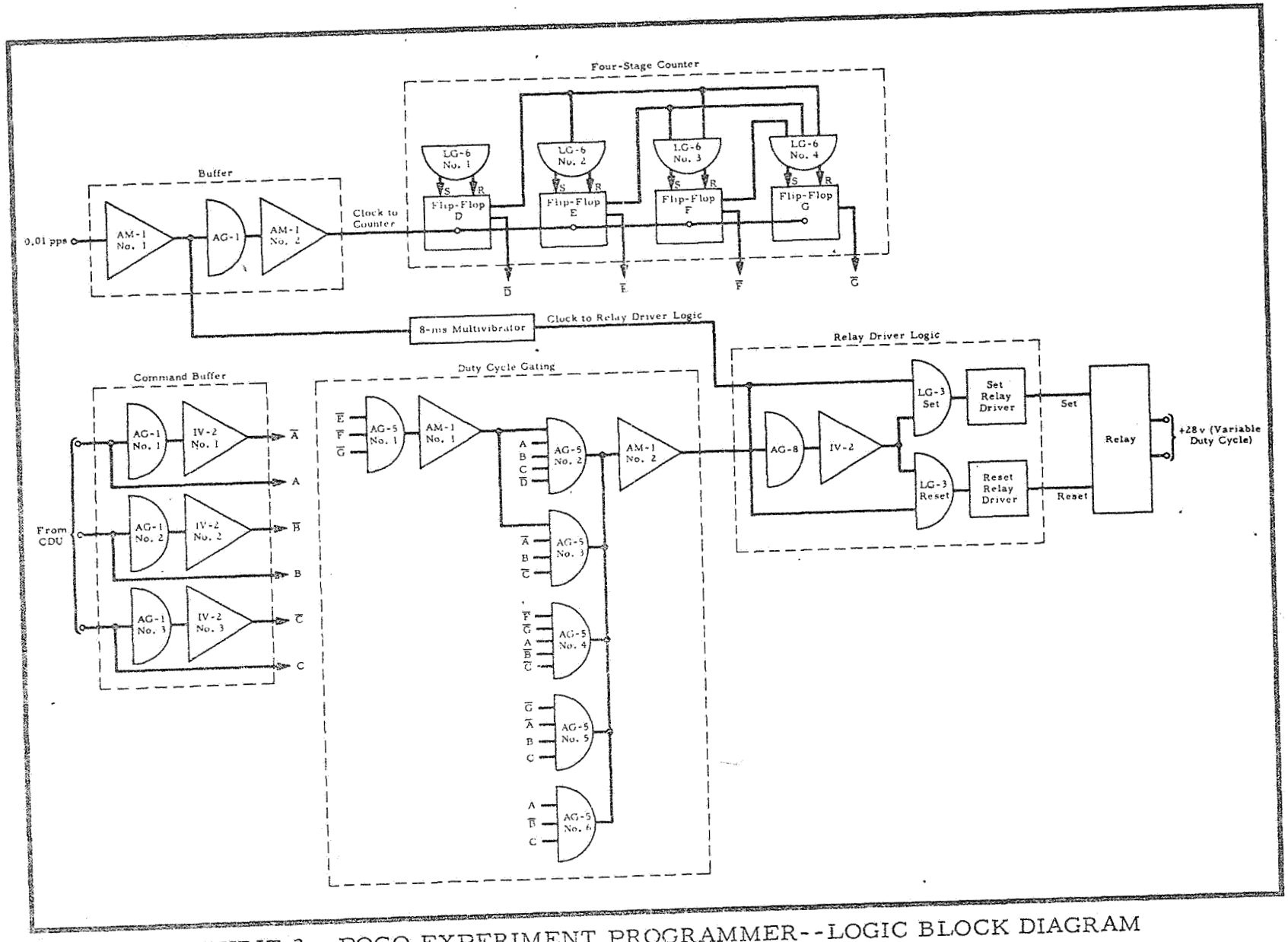


EXHIBIT 2 - POGO EXPERIMENT PROGRAMMER--LOGIC BLOCK DIAGRAM

15), and then starts over again. This causes D to be true for 100 seconds, E for 200, F for 400, and G for 800.

From combinations of these signals in conjunction with AND gates, the duty cycle gating (see Exhibit 2) derives four different duty cycles and one continuously On signal. The particular combination is selected by the signals A, B, and C, and their complements, generated in the command buffer. The logical states of these signals are completely dependent upon the command system (including the CDU), as indicated in Exhibits 1 and 2. Of the eight possible combinations available with these signals, five are used to apply power as described above, and three are used to completely remove the +28 volts that can be applied to the high-power experiments via the experiment programmer.

The 8-ms monostable multivibrator merely provides a delay in the 0.01-pps signal coming from the low-frequency timing unit via the buffer, which buffers this signal for use here and in the four-stage counter. The remainder of the programmer, excluding the one relay which is a magnetic latching type, provides the logic for driving one or the other of the latching relay coils (as determined by the previously described logic) 8 ms after the 0.01-pps signal occurs.

Thus, at the line indicated +28v (variable duty cycle) in Exhibits 1 and 2, +28 volts either exists continually for some fixed duty cycle (changeable by command), or not at all. As the experiment programmer, converter 10, and the five latching relays (variable duty--On or Off) in Exhibit 1 are presently configured, certain failure effects may thus present themselves at the power input to one or more of the high-powered experiments.

3. Failure Effects

a. General

These effects can be most easily explained by first considering the failure effects present at the output of the programmer. If one or more of the component parts in the programmer fails, the output can either be a continuous +28 volts, a continuous open circuit, or a periodic

+28 volts with an incorrect duty cycle. (It is assumed that any failure of the converter would result in one or the other of the first two effects.) The first two failure effects are both normal operating modes; that is, if the programmer had been commanded to the continuously On mode, and a failure occurred that resulted in a continuously On effect, such a failure would be unnoticeable until another proper operating mode was commanded.

To arrive at a mathematical model for accurately predicting the reliability, a failure analysis was performed which considered both the specific effect of a failure and the overall effect on mission operation. The results of the analysis are tabulated in Exhibit 4 in order of the criticality of their effects. Group 1 failures cause loss of experiments, group 2 failures cause altered duty cycles, and group 3 failures have no effect.

In arriving at the data presented in Exhibit 4, single component failures in each circuit element were examined to determine if they caused that element to fail true or false. Open input diodes in gates were considered separately, since this causes a different kind of loss by means of a change in the logic output of that gate. The assumptions utilized in the analysis are presented in Exhibit 3.

Analysis of the experiment programmer revealed that failure effects could be grouped into five specific categories:

(1) Those which cause +28 volts to be continuously On

(2) Those which cause +28 volts to be continuously Off

(3) Those which cause an indeterminate +28 volts to be continuously On or Off, depending on state of operation at time of failure

(4) Those which cause altered duty cycles

(5) Those which have no effect

Exhibit 3 lists all failures, their results, and comments where appropriate. In many cases, the effect of a failure depends upon the normal mode of operation previously commanded; the exhibit also indicates these cases.

EXHIBIT 3 - POGO EXPERIMENT PROGRAMMER--KEY TO FAILURE ANALYSIS CHART

1. Correct Command Operation

State	Time (sec) On	Time (sec) Off	Logic
S1	100	1500	$(ABC)\ (\overline{DEFG})$
S2	200	1400	$(\overline{A}B\overline{C})\ (\overline{EFG})$
S3	400	1200	$(A\overline{B}\overline{C})\ (\overline{F}\overline{G})$
S4	800	800	$(\overline{A}BC)\ (\overline{G})$
S5	Cont.		$A\overline{B}C$
S6		Cont.	$AB\overline{C}$
S7		Cont.	$\overline{A}\overline{B}C$
S8		Cont.	$\overline{A}\overline{B}\overline{C}$

Symbols, Notes, and Assumptions for Interpreting Failure Analysis Chart

2. Symbols

T = True or "1" state

F = False or "0" state

1 = Short (as applied to diodes) or true

0 = Open (as applied to diodes) or false

Sn = State selection; see above table for correct operation

(100/1500) = Duty cycle; 100 would be time On (in seconds) and 1500 would be time Off (in seconds)

3. Notes and Assumptions

a. When a flip-flop fails true, its set output is always 1, its reset output always 0.

b. When a flip-flop fails false, its reset output is always 1, its set output always 0.

EXHIBIT 3 (Continued)

c. When the flip-flop internal emitter-follower associated with the flip-flop set or reset output fails, its effects are as follows:

(1) Set side emitter-follower fails true--flip-flop set output always true; flip-flop reset output unaffected.

(2) Set side emitter-follower fails false--flip-flop set output always false, flip-flop reset output unaffected.

(3) Reset side emitter-follower fails true--flip-flop reset output always true, flip-flop set output unaffected.

(4) Reset side emitter-follower fails false--flip-flop reset output always false, flip-flop set output unaffected.

d. A failure that causes a different effect for various command selections appears in Exhibit 4 in each applicable group with a notation in the cross reference column. For instance, if the No. 1 AM-1 in the duty cycle gating fails true, S2 puts the programmer in group 1B, S1 in group 2A, S3 and S4 in group 3A. Therefore, the notation in the cross reference column for this failure in group 1B would indicate 2A and 3A; this failure shown in group 2A would refer to 1B and 3A, etc.

e. Diodes used as a logic input to a gate are considered separately in the "fail open" case. All other failures in the gate are included in the case of the gate failing "true" or "false."

f. Unless S5, S6, S7, S8 are shown specifically as being affected, or, all commands are shown as being affected, then S5 through S8 operate normally.

Group Number	Result of Failure	Circuit Element and Location	Failure Mode	Comments	Cross Reference
1A	Continuous +28 v to experiments, all commands inoperable	Duty Cycle Gating			
		AG-5 Nos. 2-6	T		
		AM-1 No. 2	T		
		Relay	T		
		Relay Driver Logic			
		AG-8	T		
		IV-2	F		
		Reset LG-3	F		
		Set LG-3	T	Relay coils continuously draw current	
		Reset Relay Driver	F		
		Set Relay Driver	T	Relay coils continuously draw current	
1B	Continuous +28 v to experiments only when in command selection shown in "Comments" column	Counter			
		Emitter Follower $\overline{G}$	T	S4	2A
		Flip-Flop G	F	S4	2A
		Duty Cycle Gating			
		AG-5 No. 1	T	S2	3A, 2A
		AG-5 No. 3, $\overline{E}\overline{F}\overline{G}$	0	S2	3A
		AG-5 No. 5, $\overline{G}$	0	S4	3A
		AG-5 No. 6, $\underline{A}$	0	S7	3A
		AG-5 No. 6, $\overline{B}$	0	S1	3A
		AG-5 No. 6, C	0	S3	3A
		AM-1 No. 1	T	S2	2A, 3A
1C	Continuous 0 v to experiments, all commands inoperable	Duty Cycle Gating, AM-1 No. 2	F		
		Relay	F		
		Relay Driver Logic			
		Reset LG-3	T	Relay coils continuously draw current	
		Set LG-3	F		
		Reset Relay Driver	T	Relay coils continuously draw current	
		Set Relay Driver	F		
1D	Continuous 0 v to experiments, S5, S6, S7, and S8 operable	Counter		Going to 0 v state with S6, S7, or S8 would decrease power consumption	
		Emitter Follower $\overline{G}$	F		
		Flip-Flop G	T		
1E	Continuous 0 v to experiments only when in command selection shown in "Comments" column	Command Buffer			
		AG-1 No. 1	T	S2, S4	3A
		AG-1 No. 2	T	S3, S5	3A
		AG-1 No. 3	T	S2, S3	3A
		IV-2 No. 1	F	S2, S4	3A
		IV-2 No. 2	F	S3, S5	3A
		IV-2 No. 3	F	S2, S3	3A

EXHIBIT 4 - POGO EXPERIMENT PROGRAMMER--FAILURE ANALYSIS CHART

Group Number	Result of Failure	Circuit Element and Location	Failure Mode	Comments	Cross Reference
1E (Cont.)		Counter			
		Emitter Follower $\overline{D}$	F	S1	3A
		Emitter Follower $\overline{E}$	F	S1, S2	3A
		Emitter Follower $\overline{F}$	F	S1, S2, S3	3A
		Flip-Flop D	T	S1	2A
		Flip-Flop E	T	S1, S2	2A
		Flip-Flop F	T	S1, S2, S3	2A
		Duty Cycle Gating			
		AG-5 No. 1	F	S1, S2	3A
		AG-5 No. 2	F	S1	3A
		AG-5 No. 3	F	S2	3A
		AG-5 No. 4	F	S3	3A
		AG-5 No. 5	F	S4	3A
		AG-5 No. 6	F	S5	3A
		AM-1 No. 1	F	S1, S2	3A
1F	Indeterminate steady state to experiments, all commands inoperable	Buffer, AM-1 No. 1	T or F	Probability of relay failing to "on" or "off" state dependent on duty cycle at time of failure or length of time spent in one state	
		Multivibrator	F		
		Relay Driver Logic			
		AG-8	F		
		IV-2	T		
		Either LG-3, Set or Reset Diode	0		
1G	Indeterminate steady state to experiments, S5, S6, S7, and S8 operable	Buffer, AG-1 and AM-1 No. 2	Any	See comment under 1F	
		Counter			
		Any Input Gate	T or F		
		Emitter Follower D, E, or F	F		
		Flip-Flop D, E, or F	F		
2A	Altered duty cycle, new duty cycle shown in "Comments" column	Command Buffer			
		AG-1 No. 1	F	S1 (800/800), S6 (200/1400)	3A
		AG-1 No. 2	F	S6 (400/1200)	3A
		AG-1 No. 3	F	S6 (100/1500)	3A
		IV-2 No. 1	T	S1 (800/800), S6 (200/1400)	3A
		IV-2 No. 2	T	S6 (400/1200)	3A
		IV-2 No. 3	T	S6 (100/1500)	3A
		Counter			
		Emitter Follower D	T	S1 (100/700), S2 (100/700), S3 (200/600), S4 (400/400)	
		Emitter Follower $\overline{D}$	T	S1 (200/1400)	3A
		Emitter Follower E	T	S1 (100/700), S2 (200/600), S3 (200/600), S4 (400/400)	
		Emitter Follower $\overline{E}$	T	S1 (100/100 - 100/1300), S2 (400/1200)	3A
		Emitter Follower F	T	S1 (100/700), S2 (200/600), S3 (400/400), S4 (400/400)	
		Emitter Follower $\overline{F}$	T	S1 (100/300 - 100/1100), S2 (200/200 - 200/1000)	3A
		Emitter Follower $\overline{G}$	T	S1 (100/700), S2 (200/600), S3 (400/400)	1B

EXHIBIT 4 (CONTINUED)

Group Number	Result of Failure	Circuit Element and Location	Failure Mode	Comments	Reference
2A (Cont.)		Counter			
		Flip-Flop D	T	S2(100/700), S3(200/600), S4(400/400)	1E
		Flip-Flop E	T	S3(200/600), S4(400/400)	1E
		Flip-Flop F	T	S4(400/400)	1E
		Flip-Flop G	F	S1(100/700), S2(200/600), S3(400/400)	1B
		Counter Input Gating			
		Flip-Flop E, D Input	0	S1(100/700), S2(100/700), S3(200/600), S4(400/400)	
		Flip-Flop F, D Input	0	S1(100/700), S2(200/600), S3(300/500), S4(400/400)	
		Flip-Flop F, E Input	0	S1(100/700), S2(200/600), S3(200/600), S4(400/400)	
		Flip-Flop G, D Input	0	S1(100/700), S2(200/600), S3(400/400), S4(700/100)	
		Flip-Flop G, E Input	0	S1(100/700), S2(200/600), S3(400/400), S4(600/200)	
		Flip-Flop G, F Input	0	S1(100/700), S2(200/600), S3(400/400), S4(400/400)	
		Duty Cycle Gating			
		AG-5 No. 1	T	S1(100/100)	3A, 1B
		AG-5 No. 1, $\overline{E}$	0	S1(100/100 - 100/1300), S2(400/1200)	3A
		AG-5 No. 1, $\overline{F}$	0	S1(100/300 - 100/1100), S2(200/200 - 200/1000)	3A
		AG-5 No. 1, $\overline{G}$	0	S1(100/700), S2(200/600)	3A
		AG-5 No. 2, C	0	S6(100/1500)	3A
		AG-5 No. 2, $\overline{D}$	0	S1(200/1400)	3A
		AG-5 No. 2, $\overline{E}\,\overline{F}\,\overline{G}$	0	S1(100/100)	3A
		AG-5 No. 3, $\overline{A}$	0	S6(200/1400)	3A
		AG-5 No. 3, B	0	S8(200/1400)	3A
		AG-5 No. 4, A	0	S8(400/1200)	3A
		AG-5 No. 4, $\overline{B}$	0	S6(400/1200)	3A
		AG-5 No. 4, $\overline{F}$	0	S3(800/800)	3A
		AG-5 No. 4, $\overline{G}$	0	S3(400/400)	3A
		AG-5 No. 5, $\overline{A}$	0	S1(800/800)	3A
		AG-5 No. 5, B	0	S7(800/800)	3A
		AG-5 No. 5, C	0	S2(800/800)	3A
		AM-1 No. 1	T	S1(100/100)	3A, 1B
3A	No effect when in command selection shown in "Comments" column	Command Buffer			
		AG-1 No. 1	T	S1, S3	1E
		AG-1 No. 1	0 or F	S2, S3, S4	2A
		AG-1 No. 2	T	S1, S2, S4	1E
		AG-1 No. 2	0 or F	S1, S2, S3, S4	2A
		AG-1 No. 3	T	S1, S4	1E
		AG-1 No. 3	0 or F	S1, S2, S3, S4	2A
		IV-2 No. 1	T	S2, S3, S4	2A
		IV-2 No. 1	F	S1, S3	1E
		IV-2 No. 2	T	S1, S2, S3, S4	2A
		IV-2 No. 2	F	S1, S2, S4	1E
		IV-2 No. 3	T	S1, S2, S3, S4	2A
		IV-2 No. 3	F	S1, S4	1E

EXHIBIT 4 (CONTINUED)

Group Number	Result of Failure	Circuit Element and Location	Failure Mode	Comments	Cross Reference
3A (Cont.)		Counter			
		Emitter Follower $\overline{D}$	T	S2, S3, S4	2A
		Emitter Follower $\overline{D}$	F	S2, S3, S4	1E
		Emitter Follower $\overline{E}$	T	S3, S4	2A
		Emitter Follower $\overline{E}$	F	S3, S4	1E
		Emitter Follower $\overline{F}$	T	S3, S4	2A
		Emitter Follower $\overline{F}$	F	S4	1E
		Emitter Follower G	T	All	
		Emitter Follower G	F	All	
		Duty Cycle Gating			
		AG-5 No. 1	T	S3, S4	2A, 1B
		AG-5 No. 1	F	S3, S4	1E
		AG-5 No. 1, $\overline{E}$	0	S3, S4	2A
		AG-5 No. 1, $\overline{F}$	0	S3, S4	2A
		AG-5 No. 1, $\overline{G}$	0	S3, S4	2A
		AG-5 No. 2	F	S2, S3, S4	1E
		AG-5 No. 2, A	0	All	
		AG-5 No. 2, B	0	All	
		AG-5 No. 2, $\overline{C}$	0	S1, S2, S3, S4	2A
		AG-5 No. 2, $\overline{D}$	0	S2, S3, S4	2A
		AG-5 No. 2, $\overline{E}\,\overline{F}\,\overline{G}$	0	S2, S3, S4	2A
		AG-5 No. 3	F	S1, S3, S4	1E
		AG-5 No. 3, $\overline{A}$	0	S1, S2, S3, S4	2A
		AG-5 No. 3, $\overline{B}$	0	S1, S2, S3, S4	2A
		AG-5 No. 3, $\overline{C}$	0	All	
		AG-5 No. 3, $\overline{E}\,\overline{F}\,\overline{G}$	0	S1, S3, S4	
		AG-5 No. 4	F	S1, S2, S4	1E
		AG-5 No. 4, $\overline{A}$	0	S1, S2, S3, S4	2A
		AG-5 No. 4, $\overline{B}$	0	S1, S2, S3, S4	2A
		AG-5 No. 4, $\overline{C}$	0	All	
		AG-5 No. 4, $\overline{F}$	0	S1, S2, S4	2A
		AG-5 No. 4, $\overline{G}$	0	S1, S2, S4	2A
		AG-5 No. 5	F	S1, S2, S3	1E
		AG-5 No. 5, $\overline{A}$	0	S2, S3, S4	2A
		AG-5 No. 5, B	0	S1, S2, S3, S4	2A
		AG-5 No. 5, $\overline{C}$	0	S1, S3, S4	2A
		AG-5 No. 5, $\overline{G}$	0	S1, S2, S3	1B
		AG-5 No. 6	F	S1, S2, S3, S4	1E
		AG-5 No. 6, $\overline{A}$	0	S1, S2, S3, S4	1B
		AG-5 No. 6, $\overline{B}$	0	S2, S3, S4	1B
		AG-5 No. 6, C	0	S1, S2, S4	1B
		AM-1 No. 1	T	S3, S4	2A, 1B
		AM-1 No. 1	F	S3, S4	1E
		Multivibrator	T	All commands, relay coils draw increased current	
		Relay Driver Logic			
		Either LG-3, Clock Diodes	0	All commands, relay coils draw increased current	

EXHIBIT 4 (CONTINUED)

The following section presents examples of failure effects and their consequences to mission value.

b. Examples (Refer to Exhibit 2)

(1) Category 1

If any of the five AG-5 gates that are "OR-ed" in the duty cycle gating failed true, the relay would receive a set signal each clock pulse, the Off commands would be invalid to the programmer, and +28 volts would be continuously On regardless of the command selection.

(2) Category 2

If the output of AM-1 No. 2 in the duty cycle gating failed false, a true signal would be present at the relay driver reset gate, the relay driver would receive a reset signal each clock pulse, and the +28 volt output would be Off regardless of the command selection.

(3) Category 3

An example of the experiment programmer failing in an indeterminate steady state is the first AM-1 in the clock buffer failing either true or false. The counter would hang up, since it would no longer receive count pulses and the multivibrator would produce no pulses. The probability of failing with either a continuous +28 volts or a continuous open circuit is related to the amount of time spent in either state when operating normally. For example, with the 50 percent duty cycle (800 seconds On, 800 seconds Off), either of these two failure effects would be equally likely to result from a particular failure of this type. With the 33-1/3 percent duty cycle (400 seconds On, 1,200 seconds Off), it is more probable that the same failure would result in the output being a continuous open circuit, and so forth.

(4) Category 4

Before an illustration is given of a failure that causes altered duty cycles, the effect of the selected command on the failure results should be considered. In the case of an indeterminate

steady-state failure the effect of the selected command is especially important in causing altered duty cycles, as is shown below.

There are some failures which, with certain commands, will cause the output to remain a continuous +28 volts or 0 volts and, with other commands, will have some other effect. A good example is if the "G" flip-flop in the counter fails false, or if the "$\overline{G}$" emitter-follower in the "G" flip-flop fails true when command S4 (800/800) is selected. For either of the failures, the $\overline{G}$ term in the duty cycle gating will be true all the time instead of providing the 800 seconds On/800 seconds Off pulses, so that command S4 will produce a continuously On signal. Commands S1 through S3 will have altered duty cycles, and commands S5 through S8 will be unaffected.

Thus, it follows that a large number of single failures cause various duty cycles to be altered and some duty cycles to be lost, but leave the experiment programmer in a satisfactory operating condition. For example, if the $\overline{EFG}$ amplifier circuit in the duty cycle gating block fails true, this goes only to the two gates that select duty cycles 100/1500 and 200/1400; hence, the other two duty cycles and the commanded Off and On states remain completely operable. The command that should select 100/1500 now selects 100/100, since only D is left to generate the timing pulses. The command that should select 200/1400 has nothing left to generate a timing pulse, and so it causes the +28 volts to be applied continuously.

(5) Category 5

There are few failures that do not affect the operation of the experiment programmer. With two exceptions, the failure is an open selection diode in the duty cycle gating. An example is the "A" diode opening in the ABC combination which selects 100/1500. Since "A" is no longer qualifying the gate, whenever a command is given that contains "B" and "C" true, this gate will be free to open and close. The only other command that has "B" and "C" true is the 800/800 selection command. Giving this command will cause the outputs of the two gates

to be "OR-ed," but since the 800/800 duty cycle overlaps the 100/1500, the output will be correct. On the other hand, giving the 100/1500 command will allow only its gate to go. This effect is illustrated below:

With no failures:

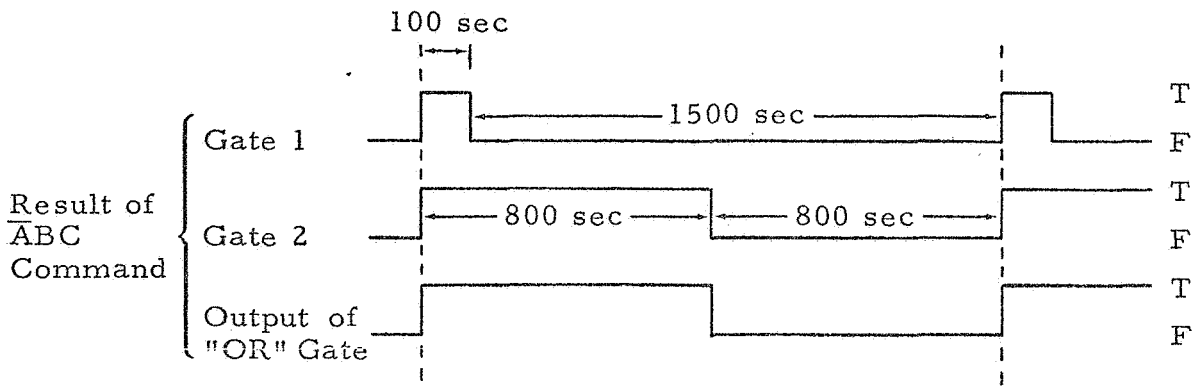
Gate 1 = ABC (100/1500 timing pulse)

Gate 2 = $\overline{A}$BC (800/800 timing pulse)

With "A" diode in gate 1 open:

Gate 1 = BC (100/1500 timing pulse)

Gate 2 = $\overline{A}$BC (800/800 timing pulse)



4. Failure Consequences

Hitherto, failures have been classified as causing continuous +28 volts or 0 volts to the experiments, altered duty cycles, and no effect. This subsection shows that, mission-wise, these failures will (1) abort the mission, (2) cause loss of the high-powered experiments, or (3) have no effect on the overall mission value.

As the failure effects have been previously classified, it is clear that they would present themselves to one or more of the high-powered experiments if any one or more of the associated relays was switched to variable duty. For any of these relays, a failure will cause the associated experiment either to receive its +28 volts in an improper timing sequence all of the time or not to receive it at all. The total result of such failure effects is complicated by the fact that the results depend significantly upon the subtleties of the particular operating state(s) at the time of failure. It is important that these total results be considered.

Exhibit 4 shows that type 1A failures are the most critical, especially because backup will be available only when the spacecraft is within communications sight of a ground station. If the +28 volts is applied continuously to all experiments (including high-powered ones), excess power consumption would be disastrous to the mission. This assumption is supported by the fact that experiments not using the programmer on S-50 require approximately 51.3 watts, whereas an additional 10.4 watts, at minimum, would be required to save at least one of the associated high-power experiments. This would mean a 20 percent additional requirement in experiment power, which seems unreasonable.

As noted, the result of a failure often depends not only on the component that failed but also on the present command configuration. Thus, if the programmer has a failure of the group 1B type, and is also out of communications sight of a ground station, the failure actually becomes one of the group 1A type for some time period. This should be kept in mind when the duty cycle is being selected for the present command configuration. Three different failures cause command state S4 to exhibit this property, and three failures for command state S2, as opposed to only one failure each for command states S1 and S3. It is interesting to note that the Off command, state S7, also falls into the latter category. At this point, it is normal to assume that, for these types of failure, the backup mode commands would be used to remove power from some or all of the experiments to prevent their excess power consumption from jeopardizing the entire mission.

Now, consider the case of a failure that causes a continuous open circuit, and one or more of the five latching relays are switched to variable duty. Again, it is normal to assume that backup mode commands would be used to provide power to at least a portion of the experiments.

If the variable duty, On or Off latching relay could not be switched back to the On or Off position, because it or the associated portion of the command system had failed, there would be no opportunity to program power by command, and the associated experiments would indeed be lost or else excess power consumption would probably abort the mission.

However, since these relays probably would not be operated frequently, their failure rates would be quite low.

The use of manual generation and radio transmission for backup mode commands would probably be impossible, although computer-generated commands might be used. However, intermittent power by command is possible only with certain types of failures, and its use is questionable because of the amount of computer usage required and the fact that the spacecraft would often be out of communications sight of the ground stations. This type of operation is conceivable for certain failures and for short periods of carefully selected time; however, from the viewpoint of overall mission results, a failure that would necessitate this type of operation would virtually cause loss of the mission or loss of the experiments powered by the experiment programmer.

It will now be shown that any failures that do not fall into either of the two previously discussed "loss" categories (mission or high-power experiments) have no effect on mission value.

With any one or more of the relays switched to variable duty and the programmer failing to provide +28 volts with an incorrect duty cycle, the final result would depend on whether the incorrect duty cycle exceeded 50 percent (the maximum duty cycle available in normal operation) and, if it did not, whether the power period was so long as to be a power problem during eclipse period. If the duty cycle exceeded 50 percent, the situation would be the same as that stated for continuous +28 volts. Exhibit 4 shows this only occurs for two failures, both when the commanded state is S4. One causes a 600 seconds On/200 seconds Off cycle and the other 700 seconds On/100 seconds Off. The worst possible result would be that the associated experiment(s) might have to be commanded Off during eclipse periods, since the erroneous duty cycles shown in Exhibit 4 (with the exception of the two mentioned above) indicate no other cause for alarm.

It can be seen that failures in the programmer or converter cause no loss of mission value if the associated experiments can be cycled by command or if there is power capability to keep them energized continually. It has been assumed, however, that a commanded duty cycle is impractical and that there is inadequate power available to keep them

energized continually. In the following section, the mathematical model considers those cases that cause mission failure, those that cause loss of the high-powered experiments, and those that have no effect. Two numbers are calculated for the reliability (or unreliability) of this area: (1) the probability that the entire mission will be lost (programmer providing +28 volts continuously when at least one experiment cannot be switched away), and (2) the probability that all of the high-power experiments will be lost.

5. Numerical Assessment

The following subsections quantitatively evaluate the probability that the POGO experiment programmer will (1) abort the overall OGO mission and (2) cause the loss of the high-power experiments with which it is associated. Each evaluation assumes that all other subsystems are operable (i. e., command, power, LFTA, etc.), thus restricting consideration to the five variable duty, On or Off relays; the experiment programmer proper; and converter 10, as shown in Exhibit 1.

a. Probability of Mission Abort

Mission abort is assumed to result whenever continuous power is drawn through the variable duty contacts of one or more of the five associated relays shown in Exhibit 1. If the satellite is in communications sight of a ground station, this can occur only if one or more of the relays fails in the variable duty position and a failure occurs in the experiment programmer such that its output is continuously at +28 volts.[1] On the other hand, if the satellite is out of communication range of a ground station, there are two possible results of an experiment programmer failure that yields a continuous +28 volt output. If the orbit is such that there is no eclipse, no damage is assumed to occur to the spacecraft. However, if part of the orbit is in eclipse, the drain on the batteries is assumed to be sufficient to abort the mission. Thus, in order to abort the mission, either (1) the satellite must be out of range of a ground station and in an eclipse "season" and the programmer or converter must

[1] See Exhibit 4 for a complete listing of possible failure modes.

fail so as to yield a continuous +28 volt output, or (2) the experiment programmer or converter must fail so as to yield +28 volts continuous output and at least one of the five relays must fail. That is,

$$P\ (\text{Mission Abort}) = \{Q_A(C) + Q_A(E.\ P.)\}\ \{P(\overline{G.\ S.})P(E) + Q(R)\} \qquad (1)$$

where $Q_A(C)$ = probability converter 10 fails providing +28 volts continuous output to experiments

$Q_A(E.\ P.)$ = probability experiment programmer fails providing +28 volts continuous output

$P(\overline{G.\ S.})$ = probability satellite is out of range of ground station

$P(E)$ = probability satellite is in eclipse season

$Q(R)$ = probability at least one of five variable duty relays fails

The probability that the satellite will be within view of a ground station at any randomly selected time is estimated to be approximately 20 percent; this is based on outdated but hopefully typical orbit calculations utilized in previous OGO assessments. P(G. S.) is thus 0.8. On the basis of a launch time of 1 January 1963 at 1800 GMT and an 82° orbit, the satellite will be in an eclipse season approximately 80 percent of the mission.[1] Thus, P(E) will also be assumed to be typically 0.8.

The Q(R) term of Equation (1) is evaluated on the basis of the following considerations. First, the average failure rate of 0.2×10^{-6} failures per hour generally used in PRC OGO assessments refers to relays that have a substantial duty cycle. Single relays such as the five considered here are generally assumed to have a negligible probability of failure because of the extremely low number of expected actuations. For the failure probability for the five relays considered together, a failure rate for an individual relay is derived from Mil-Hdbk 217[2] and used in Equation (2):

[1] See Exhibit III.C.3 of PRC R-309, Third Reliability Assessment for the Orbiting Geophysical Observatories, 15 April 1963.

[2] Proposed Mil-Hdbk 217 (Weps), Reliability Stress Analysis for Electronic Equipment, 31 December 1961.

$$Q(R) = 1 - (e^{-5\lambda_R t}) \tag{2}$$

where λ_R = individual relay failure rate

t = effective mission time (9560 hours, including 800 hours to compensate for launch stress)

The relays under consideration are similar to the Mil-Hdbk 217 type I relay. The incremental additions therein are assumed to be zero and the multiplying factors unity. The average number of actuations is taken to be 0.01 per hour. Using the procedures of the handbook, the failure rate then becomes 0.052 failures per million hours. Evaluating Equation (2) with $\lambda_R = 0.052 \times 10^{-6}$ gives a value of 0.0025 for Q(R).

The evaluation of Q_A(E. P.) and Q_A(C) is deferred to the following subsection. These values are 0.1213 and 0.0431, respectively. Inserting these values in Equation (1) results in a probability of mission abort of 0.1056 for a 1-year mission.

b. Probability of Loss of High-Power Experiments

The high-power experiments are assumed to be lost if either +28 volts or 0 volts is continuously provided to the variable duty relays.[1] This effect can result from certain failures either in converter 10 or in the experiment programmer itself. Thus, with respect to failures of this type, the overall model equation giving the probability of losing the high-power experiments is

$$Q(H.\ P.) = 1 - P(C)P(E.\ P.) \tag{3}$$

where Q(H. P.) = probability of loss of high-power experiment

P(C) = probability of no failure in the converter, resulting in +28 or 0 volts to the experiments

P(E. P.) = probability of no failure in the experiment programmer, resulting in +28 or 0 volts to the experiments

[1] Failures resulting in an incorrect duty cycle are generally such that the resultant duty cycle is ≤ 50 percent; thus, these failures are assumed to be noncritical in the numerical analysis.

Derivations of the final two terms in Equation (3) are discussed below for the experiment programmer and for converter 10; other probabilities of interest are also considered.

The results of a failure analysis of the experiment programmer are given in Exhibit 4. The effects of all singular failures are tabulated where the experiment programmer is assumed to consist of a number of "independent" element/mode combinations. The elements are subunits such as relay drivers, AM-1 circuit cards, etc., and the modes are either "fail true" or "fail false" or "fail open" in the case of some singular diodes under consideration. Exhibit 5 lists all subunits contained in the experiment programmer and their estimated failure rates.[1] In general, any singular failure may cause one of four possible results: (1) +28 volts continuously supplied to the high-power experiments, (2) 0 volts continuously supplied to the experiments, (3) an incorrect duty cycle supplied to the experiments, and (4) no effect. Some of these failures always yield the same results; for others, the result is a function of which of the possible duty cycles is being used when the failure occurs. For still others, the result is a function of which portion of the duty cycle the failure occurs in; i.e., whether the experiment programmer is On or Off at the instant of failure.

In this analysis, it is assumed that the experiment programmer will be in one of the four duty cycles at all times during normal (non-failed) operation and that any one duty cycle is as likely to be in use at a particular time as any other. That is, the probability that the experiment programmer is operating in S1, S2, S3, or S4 is 1/4, and the probability that position S5, S6, S7, or S8 is commanded is 0. This accounts for fractional entries in Exhibit 5 which are multiples of 0.250. For instance, element IV-2(T) has an apportioned quantity of 0.250, causing an "incorrect duty cycle," and 2.750, causing "no effect." This results because only if the experiment programmer is in S1 when IV-2 No. 1 fails true will an incorrect duty cycle result, whereas, if either

[1] The derivation of these failure rates is described in the appendix.

EXHIBIT 5 - LIST OF FIRST-ORDER FAILURES, THEIR EFFECTS AND PROBABILITIES AT THE END OF A ONE-YEAR POGO MISSION

Subunit	Failure Mode	Failure Rate $\lambda \times 10^{-6}$	Apportionment of Total Subunit/Failure Mode Quantity Causing: (A) 28 Volts Continuous	(B) 0 Volts Continuous	(C) Incorrect Duty Cycle	(D) No Effect	Total Subunit/ Failure Mode Quantity (E.P.)
Relay Driver	T	0.553	1	1			2
	F	0.917	1	1			2
IV-2	T	0.861	0.234	0.766	0.250	2.750	4
	F	0.540	1	1.250		1.750	4
Relay	T	0.1	1				1
	F	0.1		1			1
AM-1	T	1.322	1.718	1.532	0.250	0.500	4
	F	0.954	0.468	3.032		0.500	4
AG-8	T	0.214	1				1
	F	0.546	0.234	0.766			1
LG-3	T	0.290	1	1			2
	F	0.500	1	1			2
F/F	T	0.652		2.500	1.500		4
	F	0.652	0.952	2.298	0.750		4
EF	T	0.380	0.250		5	2.750	8
	F	0.380	0.702	4.798		2.500	8
AG-1	T	0.214	0.234	2.016		1.750	4
	F	0.546	0.234	0.766	0.250	2.750	4
AG-5 No. 2-6	T	0.574	5.000				5
	F	1.871		1.000		4.000	5

EXHIBIT 5 (Continued)

Subunit	Failure Mode	Failure Rate $\lambda \times 10^{-6}$	Apportionment of Total Subunit/Failure Mode Quantity Causing: (A) 28 Volts Continuous	(B) 0 Volts Continuous	(C) Incorrect Duty Cycle	(D) No Effect	Total Subunit/ Failure Mode Quantity (E.P.)
AG-5 No. 1	T	0.259	0.250		0.250	0.500	1
	F	0.546		0.500		0.500	1
Multivibrator	T	1.953				1.000	1
	F	3.669	0.234	0.766			1
Counter Gates (Lumped)	T	0.210	0.234	0.766			1
	F	2.000	0.234	0.766			1
Diodes	Open	0.135	1.468	1.532	9.500	23.500	36
Total Column Failure Rate			11.830	21.686	5.396	21.334	60.246
Total Column "Parts"			19.446	30.054	17.750	44.750	112
$P_0(\ ) = P(f = 0) =$			0.89	0.81	0.95	0.82	0.56
$P_1(\ ) = P(f = 1) =$			0.10	0.17	0.05	0.17	0.32
$P_2(\ ) = P(f \geq 2) =$			0.01	0.02	0	0.01	0.12

where f = number of failures

Note: Time is taken to be 9560 hours, which includes a factor of 800 hours to account for launch stress.

IV-2 No. 2 or 3 fails true, no effect results, nor is there any effect if IV-2 No. 1 fails true in command state S2, S3, or S4. However, the failure, IV-2(T), associated with the relay driver logic results in either +28 volts or 0 volts being continuously supplied to the experiments. As Exhibit 5 shows, this failure is apportioned as 0.234 and 0.766. This apportionment arises as follows. It has been assumed that any of the four duty cycles is equally likely under normal operation. Since each cycle is 1600 seconds long, the expected proportion of On time is[1]

$$\frac{100 + 200 + 400 + 800}{4(1600)} = 0.234$$

and the expected proportion of Off time is

$$\frac{1500 + 1400 + 1200 + 800}{4(1600)} = 0.766$$

Thus, for those failure modes listed in Exhibit 3 resulting in an indeterminate steady state, the ratio of 0.234 On and 0.766 Off is used to apportion failure results between continuously On and continuously Off. The apportionment of all failures among the four possible results is shown in Exhibit 5, as well as the total failure rate associated with each result.

Thus far, only the effects of first-order failures have been considered. Of course, double or multiple failures may occur; however, the probability associated with all possible high-order failures in the experiment programmer is 0.115, utilizing the usual exponential law and the failure rates shown in Exhibit 5. Since there are in excess of 6000 "second-order" failures alone, the analysis of higher order failures on a case basis is clearly intractable. Thus, for simplicity, it will be conservatively assumed that all higher order failures cause loss of the high-power experiments.[2] The probability of a "successful" experiment programmer is, then, under the assumptions made,

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[1] See Exhibit 3.

[2] For use in the mission analysis, half the higher order failures are assumed to cause continuous +28 volt input to the experiment.

$$P(E.\ P.) = P_0(A)P_0(B)\ \{P_0(C)P_0(E) + P_0(C)P_1(E) + P_1(C)P_0(D)\} \qquad (4)$$

where $P_0(A)$ = probability of no failures in column A

$P_1(A)$ = probability of exactly one failure in column A

A, B, C, D = the four columns so designated in Exhibit 5

The requisite probabilities have been calculated directly from Exhibit 5 and are listed there. Inserting these probabilities in the above expression yields

$$P(E.\ P.) = 0.71$$

The term $Q_A(E.\ P.)$ of Equation (1) can now be calculated as

$$Q_A(E.\ P.) = P_1(A)P_0(B)P_0(C)P_0(D) + \frac{P_2(E.\ P.)}{2} \qquad (5)$$

where $P_2(E.\ P.)$ = probability of two or more failures in the experiment programmers

which, from the inputs of Exhibit 5, is seen to be, numerically,

$$Q_A(E.\ P.) = 0.12$$

The analysis of converter 10 was not carried out to the depth of that performed for the experiment programmer; i.e., a part-by-part failure analysis was not performed. However, sufficient analysis was performed to indicate that any singular part failure in the converter will result in either a continuously On or Off state to the variable duty relays, assuming there are no failures in the experiment programmer. Either resultant state is assumed to be equiprobable. Multiple failures either within the converter or between the converter and the experiment programmer result, on the basis of previous assumptions, in a continuous +28 or 0 volts output with equal probabilities.

The term $Q_A(C)$ in Equation (1) can thus be written

$$Q_A(C) = \frac{(1 - e^{-\lambda_c t})}{2} \qquad (6)$$

where λ_c = the total converter failure rate

t = 9560 hours (1 year, plus 800 hours to account for launch stress)

Using the value for λ_c in Exhibit 6 gives a value of 0.04 for Equation (6).

The P(C) term of Equation (3) is simply $\exp\left\{-\lambda_c t\right\}$, where λ_c and t are as above. The result is 0.91.

Thus, the probability of losing the high-power experiments, from Equation (3), is equal to 0.35.

6. Conclusions and Recommendations

The experiment programmer, converter 10, and five latching relays were added to the OGO spacecraft in order to accomodate four POGO mission experiments having high-power requirements. The added circuitry will control the total power consumption of these four experiments to a satisfactory amount when it is operating properly. However, it is possible that the added circuitry will fail. The probability that such failure will cause the entire mission to abort during a 1-year mission is 0.10. The probability that such failure will cause loss of all of the high-power experiments is 0.35. These numbers should be interpreted in the light of the assumptions made throughout the previous portions of this TAM.

Attention is directed to the following facts:

a. 1B failures can become 1A failures when certain commands are selected.

b. Some failures, such as certain open selection diodes in the duty cycle gating, have no effect.

Because of these facts it is possible for one command configuration to be better than another. For example, it was found that command state S4 would develop into a type 1A (as opposed to 1B) failure as the result of any one of three failures, if the spacecraft was out of communications sight. However, states S1 and S3 develop in this manner only if one particular failure occurs. Thus, PRC recommends that further attention be given to the command configuration/logic/duty cycle relations. That

EXHIBIT 6 - PARTS COMPLEMENT AND FAILURE RATES FOR CONVERTER NUMBER 10

Part Type	Number of Parts	Individual Part Failure Rate x 10^{-6}
Resistors, Carbon Composition	25	0.01
Resistors, Wirewound	10	0.07
Capacitors	2	0.01
Capacitors, Tantalum	10	0.08
Transistors	10	0.30
Diodes, Zener	6	0.26
Diodes	12	0.15
Transformers	4	0.25
Choke	1	0.05
Coils	3	0.05
Fusable Link	1	0.10
Totals	84	9.43

is, S4 selects the highest duty cycle; instead, perhaps it would be better if this were done by S1, and vice versa.

It should also be noted that including the capability of providing the high-power experiments with a continuous +28 volts via the experiment programmer creates a hazard, since failures can occur. Such a "redundant" capability would seem inappropriate, since the same function can be accomplished by normal commands, and the requirement for continuous power to the high-power experiments is obscure. Thus, PRC recommends that the continuous On capability (S5) be changed to a continuous Off command, thereby omitting it from the duty cycle gating.

Finally, PRC recommends that some consideration be given to instrumenting the experiment programmer output so that its operating state can be readily determined on the ground. With such instrumentation a "quick look" capability would also be available.

7. SUMMARY

THIS TAM ASSESSES THE RELIABILITY OF THE EXPERIMENT PROGRAMMER AND ITS EFFECTS ON THE POGO SPACECRAFT.

a. THE PROBABILITY OF MISSION ABORT DUE TO EXPERIMENT PROGRAMMER FAILURE IS 0.10.

b. THE PROBABILITY OF LOSS OF THE HIGH-POWER EXPERIMENTS DUE TO EXPERIMENT PROGRAMMER FAILURE IS 0.35.

c. PRC RECOMMENDS THAT THE COMMAND CONFIGURATION/LOGIC/DUTY CYCLE RELATIONS BE STUDIED FOR OPTIMIZATION FROM THE RELIABILITY STANDPOINT.

d. PRC RECOMMENDS THAT THE "CONTINUOUS ON" CAPABILITY BE CHANGED TO A "CONTINUOUS OFF" COMMAND FOR GREATER FAIL-SAFE CAPABILITY.

e. PRC RECOMMENDS THAT THE OUTPUT OF THE EXPERIMENT PROGRAMMER BE INSTRUMENTED SO THAT ITS OPERATING STATE CAN BE READILY DETERMINED ON THE GROUND.

APPENDIX

EXPERIMENT PROGRAMMER FAILURE RATE DERIVATION

The electronic parts in the experiment programmer consist essentially of the following six classes of parts: transistors, Q; resistors, R; diodes, D; capacitors, C; relays, Ry; and zener diodes, Dz. In the failure analysis, it is necessary to consider both the open and short modes for each part type. The table below summarizes the failure rates assigned, which are those used in the third OGO assessment.

	Failure Rate (failures/million hours)		
	Open	Short	Total
Transistor	0.150	0.150	0.30
Diode	0.135	0.015	0.15
Resistor	0.184	0.046	0.23
Capacitor	0.002	0.008	0.01
Relay	0.100	0.100	0.20
Diode, Zener	0.234	0.026	0.26

In addition, the failure rates of two of the modules used herein were previously calculated in the third OGO assessment. These are the IV-2 and AM-1 modules. The F/F modules are similar to those used previously, except that for this analysis the emitter-follower sections were treated separately. Exhibit A-1 presents the failure-rate calculations and parts complements for each multiple part subunit used in the experiment programmer assessment.

EXHIBIT A-1 FAILURE-RATE DERIVATIONS FOR THE EXPERIMENT PROGRAMMER

Subunit		Failure Contributors	Failure Rate (failures/million hours)
Relay Driver	T	D-O, 2 Q-S, 2 R-S, Dz-S	0.553
	F	D-S, 2 Q-O, 2 R-O, Dz-O	0.917
IV-2	T	See PRC R-309	0.861
	F	See PRC R-309	0.540
AM-1	T	See PRC R-309	1.322
	F	See PRC R-309	0.954
AG-8	T	2 D-S, R-O	0.214
	F	2 D-O, R-O, 2 R-S	0.546
LG-3	T	4 D-S, R-O, R-S	0.290
	F	2 D-O, R-O, R-S	0.500
AG-1	T	2 D-S, R-O	0.214
	F	2 D-O, R-O, 2 R-S	0.546
AG-5 Nos. 2-6	T	26 D-S, R-O	0.574
	F	5 D-O, 5 R-O, 6 R-S	1.871
AG-5 No. 1	T	5 D-S, R-O	0.259
	F	2 D-O, R-O, 2 R-S	0.546

EXHIBIT A-1 (Continued)

Subunit		Failure Contributors	Failure Rate (failures/million hours)
F/F (with 2 EF)	T	See PRC R-309	1.412
	F	See PRC R-309	1.412
EF	T	Q-S, R-O, R-S	0.380
	F	Q-O, R-O, R-S	0.380
F/F (minus 2 EF)	T		0.652
	F		0.652
Multivibrator	T	4 D-O, 2 R, 2 R-S, IV-2-T	1.953
	F	4 D, 3 R, IV-2, C, 4 D-S, 2 R-O, IV-2-F	3.669
Counter Gates (Lumped)	T	14 D-S	0.210
	F	8 D-O, 4 R	2.000

Notes: "O" indicates failure open.

"S" indicates failure short.

TECHNICAL ADVISEMENT MEMORANDUM NO. 34-31

REVIEW OF CAPACITIVE TACHOMETERS FOR ATTITUDE CONTROL REACTION WHEELS

PRC D-843

31 August 1964

Prepared by

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Approved by

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PLANNING RESEARCH CORPORATION

LOS ANGELES, CALIF. WASHINGTON, D.C.

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TECHNICAL ADVISEMENT MEMORANDUM NO. 34-31

To: Assistant OGO Project Manager, GSFC, NASA

From: PRC OGO Reliability Assessment Team

Subject: Review of Capacitive Tachometers for Attitude Control Reaction Wheels

1. Magnetic Tachometer

The original magnetic tachometer components consisted of a stationary permanent magnetic slug and an output coil mounted on the reaction wheel stator and a permeable steel cam ring mounted on the rotor. Rotation of the cam with respect to the stationary magnet resulted in a change in flux distribution, thereby inducing a voltage across the output coil terminals. Due to the cam contour, the flux variation was triangular with rotation; hence, the output versus angular velocity was a pulse train having a repetition rate and pulse amplitude proportional to speed, and a pulse polarity dependent upon sense of rotation. The output pulses were delivered to the STL speed and direction converter circuitry to derive an analog indication of speed and a digital indication of direction.

2. Capacitive Tachometer

A capacitive tachometer is proposed to replace the magnetic tachometer in order to achieve the same pulse-train waveform characteristics while reducing the magnetic field of the reaction wheel assembly. Originally, a single variable capacitive system was proposed consisting of a rectangularly toothed capacitive plate on the stator and a sawtoothed capacitive plate on the rotor. In this approach, the charge across a capacitor (supplied by an external DC source) was permitted to vary linearly with rotation by varying the capacitance in a triangular manner, analogous to the flux variation characteristics of the magnetic tachometer. The rate of change of charge across the capacitor, or current, was then read out by monitoring the voltage across a series output resistor.

Because of the direct relation between load resistance and output voltage, it was necessary to incorporate a buffer amplifier with a high input impedance and a low output impedance between the tachometer output and the frequency-to-DC converter circuitry. The single variable capacitive element tachometer was also found to be susceptible to 400-cycle motor drive pickup and to electrostatic charge accumulation on the tachometer capacitor plates. To circumvent these effects, the single capacitive pattern was altered to two symmetrically balanced rotor and stator patterns. This design consists of two variable capacitors of equal value at any instant of time and changing at equal rates; it is illustrated in Exhibit 1, with the equivalent electrical circuit shown in Exhibit 2. The voltages E_1 and E_2 are fed to a differential amplifier stage in the buffer amplifier so that the 400-cycle pickup and electrostatic charge accumulation effects cancel, while the useful tachometer signal is amplified. To reduce the noise further, the differential amplifier must cancel; the capacitance of the rotor plates to ground is made large, thereby shunting a portion of the noise in the tachometer to ground. Thus, the final buffer amplifier consists of three functions:

a. A high input impedance differential amplifier

b. A gain stage to provide the pulse level and characteristics required by the frequency-to-DC converter circuitry

c. An output emitter-follower to feed the low impedance frequency-to-DC converter

The buffer amplifier circuitry is shown in Exhibit 3. The differential input stages are connected in Darlington configurations to provide input impedances of 750 K ohms. Variable shunt feedback is provided in the gain stage to stabilize the loop gain and to permit adjustment of gains from 3 to 11. Low pass filter networks are also provided in this stage to obtain cutoff frequencies of 250 cps and 800 cps. The output impedance of the emitter follower is 100 ohms, and it can drive loads of from 3,000 ohms to infinity.

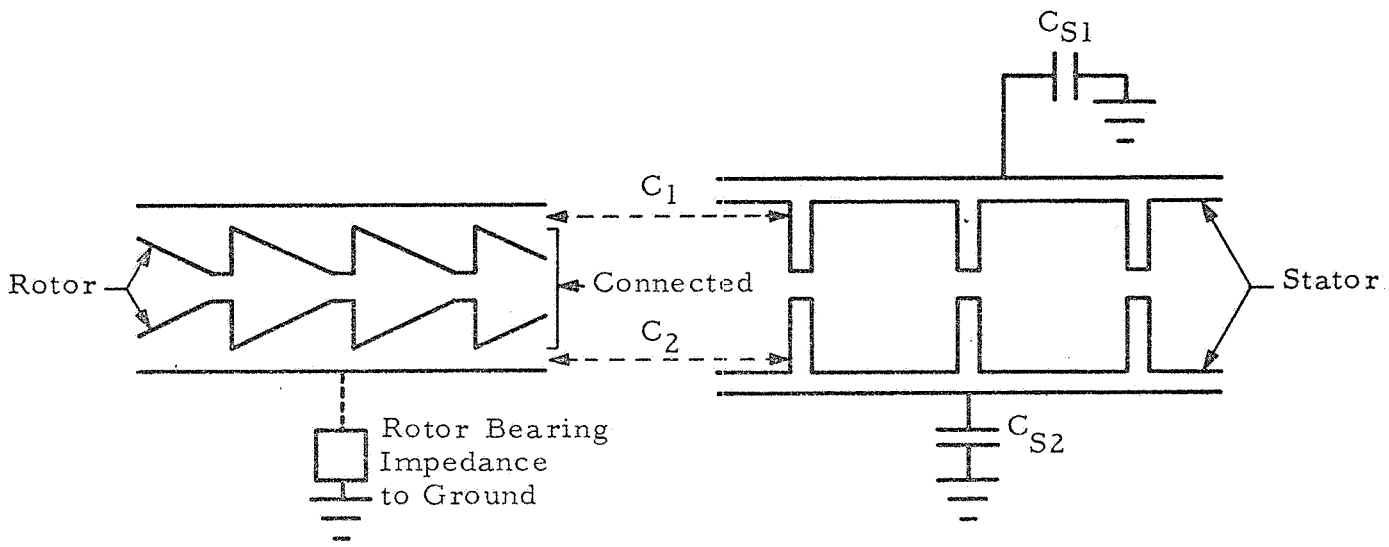

EXHIBIT 1 - ROTOR AND STATOR PATTERNS OF SYMMETRICAL-CAPACITANCE TACHOMETER

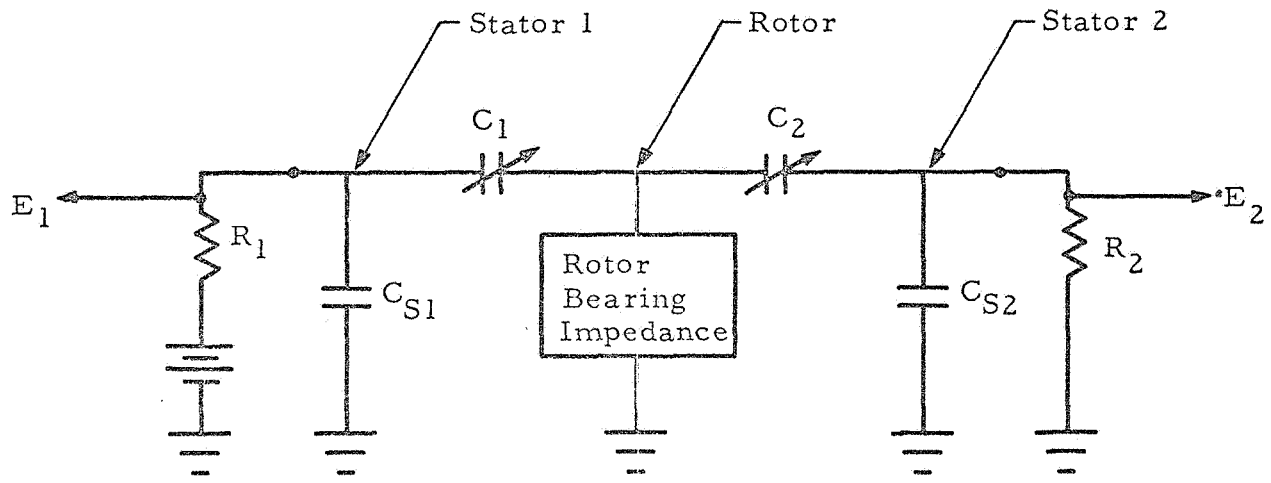

EXHIBIT 2 - EQUIVALENT CIRCUIT OF SYMMETRICAL-CAPACITANCE TACHOMETER

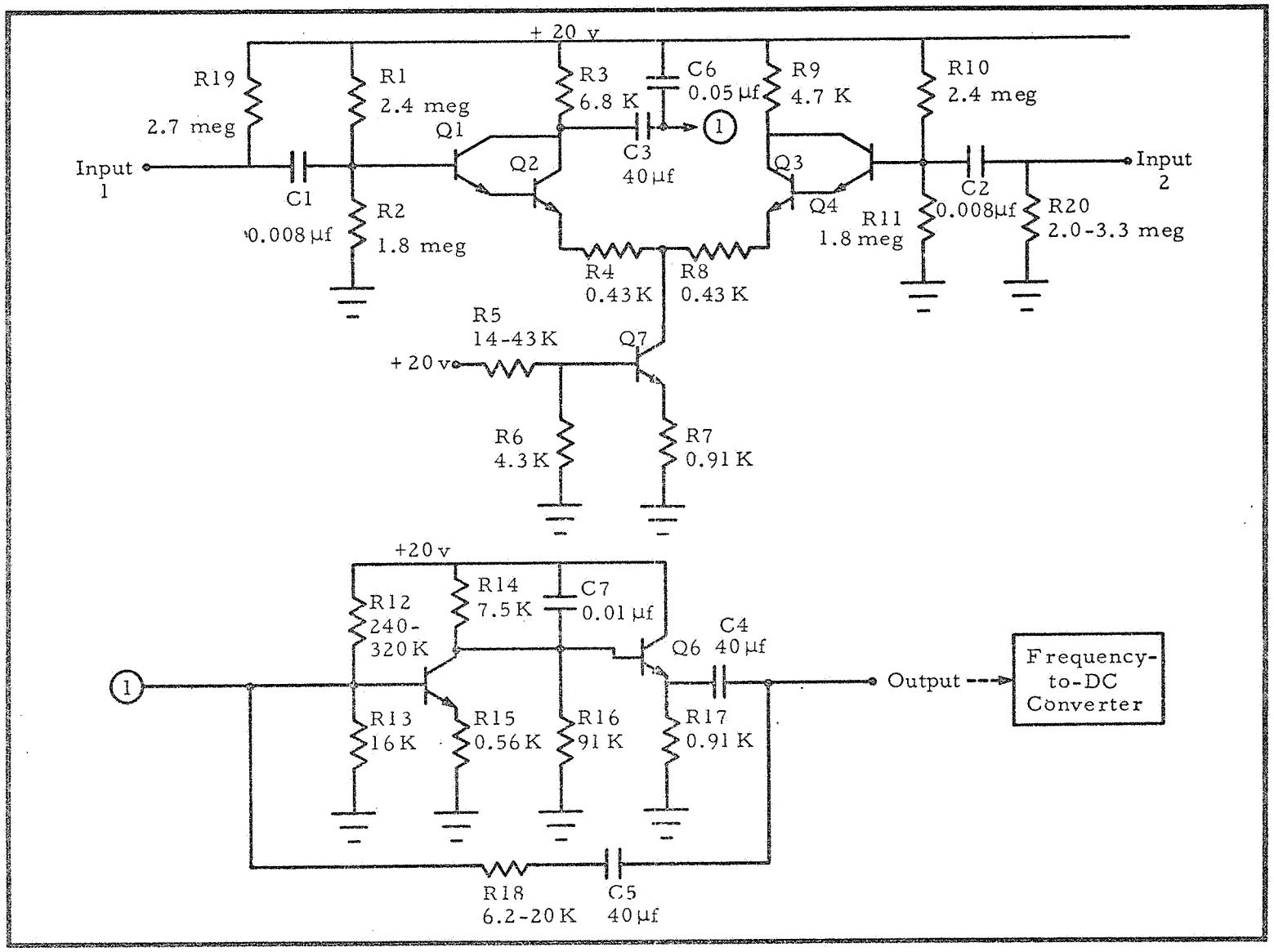

EXHIBIT 3 - BUFFER AMPLIFIER FOR SYMMETRICAL-CAPACITANCE TACHOMETER

3. Reliability Effects

As originally conceived, the tachometer pulse-train output was fed directly to the frequency-to-DC converter circuitry. However, the capacitive tachometer requires a buffer amplifier between its outputs and the frequency-to-DC converter to provide consistent pulse shape and amplitude and to prevent loading effects. Because of the feedback around the gain and emitter-follower stages, some degradation of performance within these stages can be tolerated without functional operation being affected. However, no direct redundancy has been incorporated in the buffer amplifier; therefore, operation is assumed to fail if any of the individual parts fail. The components used in the proposed buffer amplifier (plus the two resistors that are the voltage sensing elements of the tachometer) are listed in Exhibit 4. The exhibit also includes the parts-count reliability computations for all three channels (pitch, yaw, and roll) combined for periods of 3, 6, 9, and 12 months (including the launch period represented by 800 hours[1]), using the parts failure rates of Reference 4.

The computed reliability of the electronic components after 1 year in orbit is 0.95. Since no electronic parts were required between the magnetic tachometer and the frequency-to-DC converter, the capacitive tachometer adds a series block with a reliability of 0.95 to the reliability of the Reaction Control Subsystem, if it is assumed that the tachometers must be unfailed for mission success. Thus, if the reliabilities of the two tachometer systems (exclusive of the buffer) are assumed equal and approximately one because of their simplicity, the relative reliability of the Reaction Control Subsystem with the proposed capacitive tachometer is 95 percent of that utilizing the magnetic tachometer, or 0.95. The effect of this reliability degradation on the overall ACS Subsystem is insignificant.

[1] The representation of the launch stresses by 800 hours is derived in Reference 4.

EXHIBIT 4 - RELIABILITY CALCULATION FOR CAPACITOR TACHOMETER AND BUFFER AMPLIFIER

Components	Number	λ (x 10^{-6})	Total λ (x 10^{-6})
Tachometer Resistors	2	0.01	0.02
Amplifier Resistors	20	0.01	0.20
Capacitors	7	0.01	0.07
Transistors	7	0.30	2.10
Electronics			2.39

Time (hours)	R (electronics)
2990	$e^{-(0.00715)3} = 0.979$
5180	$e^{-(0.0124)3} = 0.976$
7370	$e^{-(0.0176)3} = 0.966$
9560	$e^{-(0.0228)3} = 0.954$

Therefore, Reliability (1 year) = (0.95) (Capacitive Tachometer Reliability)

4. SUMMARY

THE PURPOSE OF THIS TAM IS TO INVESTIGATE THE EFFECTS ON THE RELIABILITY OF THE SPACECRAFT OF REPLACING THE MAGNETIC TACHOMETER WITH THE CAPACITIVE TACHOMETER.

a. RELIABILITY OF THE THREE CAPACITIVE TACHOMETERS INVOLVED IS 0.95, AS OPPOSED TO APPROXIMATELY ONE FOR THE ORIGINAL MAGNETIC TACHOMETERS.

b. THE RELIABILITY OF THE ATTITUDE CONTROL SUBSYSTEM IS DEGRADED SLIGHTLY.

c. FROM A SYSTEM STANDPOINT THIS DEGRADATION IS PRACTICALLY NEGLIGIBLE.

REFERENCES

1. Some Electrostatic Tachometer Design Considerations. Technical Note ED63-N-177. Eclipse-Pioneer Division, Bendix Corporation. 7 February 1963.

2. Second Interim Report for Attitude Control Reaction Wheel (OGO Yaw) Reliability and Performance Requirements (1 June 1963-31 August 1963). Eclipse-Pioneer Division, Bendix Corporation.

3. Monthly Progress Report, Attitude Control Reaction Wheel (OGO Yaw) Reliability and Performance Improvements. Eclipse-Pioneer Division, Bendix Corporation. 15 August 1964.

4. Third Reliability Assessment for the Orbiting Geophysical Observatories. PRC R-309. 15 April 1963.

TECHNICAL ADVISEMENT MEMORANDUM NO. 34-32

EFFECTS OF UNIVERSAL WIRING SYSTEM AND COMMAND RECEIVER FREQUENCY CHANGE ON OGO SPACECRAFT RELIABILITY

PRC D-844

31 August 1964

Prepared by

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TECHNICAL ADVISEMENT MEMORANDUM NO. 34-32

To: Assistant OGO Project Manager, GSFC, NASA

From: PRC OGO Reliability Assessment Team

Subject: Effects of Universal Wiring System and Command Receiver Frequency Change on OGO Spacecraft Reliability

1. Introduction

The purpose of this memorandum is to review the proposed design and to evaluate the implications on spacecraft and mission reliability of (1) the use of a "universal" wiring system and (2) the command receiver frequency change.

2. Universal Wiring System

It appears that the OGO cabling has proceeded through three iterations. The original, very flexible system of patch panels and J-boxes was discarded in favor of what was referred to as a more tailored cable system. This iteration was primarily for weight reduction, and the system was used on S-49.

Primarily because improvement in the spacecraft boosters somewhat lifted the weight restrictions with respect to the cabling, the tailored cable system was changed to the universal wiring system. This system is used on S-50 and is expected to be used hereafter.

It would appear that the only recognizable effect such changes could have on reliability would be the result of increases and/or decreases in connections. The exact number of connections was not available; and the number of connectors used in the first system was not available, perhaps because it was never completely finished. However, it is known that, not including those for experiments, S-49 requires 554 connectors and S-50 only requires 428.

Thus, on the basis of the number of connectors (assuming the percentage of used pins is equal for both spacecraft), the universal system used on S-50 would tend to have lower probability of failure than the

tailored system used on S-49. However, if the total number of pins is the same for both S-49 and S-50, the reduction in connectors would tend to improve reliability. This is due to the reduction in physical points at which disturbances could occur by virtue of the existence of connectors. Therefore, despite the missing details, PRC does not feel that the reliability was hindered in this area.

3. Command Receiver Frequency

The command receiver frequency was changed from 120 mc to 148.9 mc either because it was interfering with or being interfered with by some other 120-mc signals. The frequency change resulted in a change of the first r-f transistor from a Philco 2N2398 to a Texas Instruments 2N2415 in order to lower the noise. The only other changes were a higher frequency crystal and tuned circuit component values. Therefore, it is felt that the reliability of the command receiver remains unchanged.

4. SUMMARY

THE EFFECTS OF THE UNIVERSAL WIRING SYSTEM AND THE COMMAND RECEIVER FREQUENCY ON RELIABILITY OF THE OGO S-50 SPACECRAFT ARE AS FOLLOWS:

a. SPACECRAFT RELIABILITY IS IMPROVED SLIGHTLY THROUGH THE USE OF FEWER CONNECTORS IN THE UNIVERSAL WIRING SYSTEM.

b. SPACECRAFT RELIABILITY IS UNCHANGED DUE TO THE COMMAND RECEIVER FREQUENCY CHANGE.