A Reproduced Copy

OF

Reproduced for NASA

by the

NASA Scientific and Technical Information Facility

MAR 1971
RECEIVED
NASA STI FACILITY
INPUT BRANCH

N71-19790

RECONFIGURABLE G & C COMPUTER STUDY FOR SPACE STATION USE

FINAL REPORT

VOLUME III

APPENDIX 1

31 January 1971

J. Jurison
Program Manager

Distribution of this report is provided in the interest of information exchange and should not be construed as an endorsement by NASA of the material presented.

Prepared Under Contract No. NAS9-10416

Autonetics Division of North American Rockwell
for
Manned Spacecraft Center
National Aeronautics and Space Administration

FOREWORD

This final report covers the work performed by Autonetics Division of North American Rockwell Corporation under a study contract entitled Reconfigurable G&C computer Study for Space Station Use. The report is submitted to the National Aeronautics and Space Administration Manned Spacecraft Center under the requirements of Contract NAS 9-10416. The study program covered the period from December 29, 1969 through January 31, 1971. The NASA Technical Monitor was Mr. E. S. Chevers.

The final report consists of seven (7) volumes:

Volume I	Technical Summary	
Volume II	Final Technical Report	
➧Volume III	Appendix I.	Model Specification
Volume IV	Appendix 2.	IOP - VCS Detailed Design
Volume V	Appendix 3.	System Analysis and Trade-Offs
Volume VI	Appendix 4.	Software and Simulation Description and Results
Volume VII	Appendix 5.	D-200 Computer Family
	Appendix 6.	System Error Analysis
	Appendix 7.	Reliability Derivation for Candidate Computers
	Appendix 8.	Power Converter Design Data
	Appendix 9.	Data Transmission Medium Design

➧YOU ARE READING THIS VOLUME

VOLUME III
APPENDIX I
TABLE OF CONTENTS

		Page
1.0	Scope	1-1
2.0	Requirements	1-1
	2.1 Item Definition	1-1
	2.2 Characteristics	1-3

VOLUME III
APPENDIX 1
LIST OF ILLUSTRATIONS

Figure		Page
1.	Computer Interface Diagram	1-2
2.	Computer Block Diagram	1-4
3.	IOP Block Diagram	1-11
4.	IOP Command Formats	1-12
5.	Control Word Formats	1-15

1.0 SCOPE

This document establishes the requirements for the performance of a reconfigurable computer for application in multiple computer and fault tolerant systems.

2.0 REQUIREMENTS

The computer consists of a central processing unit (CPU), a memory system, an input/output processor (IOP), a clock section, a memory data bus and a power converter. The computer shall provide program storage and necessary circuitry to act as a general purpose computer.

2.1 Item Definition

The computer shall be a general purpose digital machine capable of executing an internally stored program. The computer shall be capable of communicating with other computers and external devices over digital data buses. The computer shall consist of one CPU, a modular memory system of one to four memory modules, one memory data bus, one power converter, one IOP and one clock generator.

2.1.1 Item Diagram

The relationship of the computer to other equipment is shown in Figure 1.

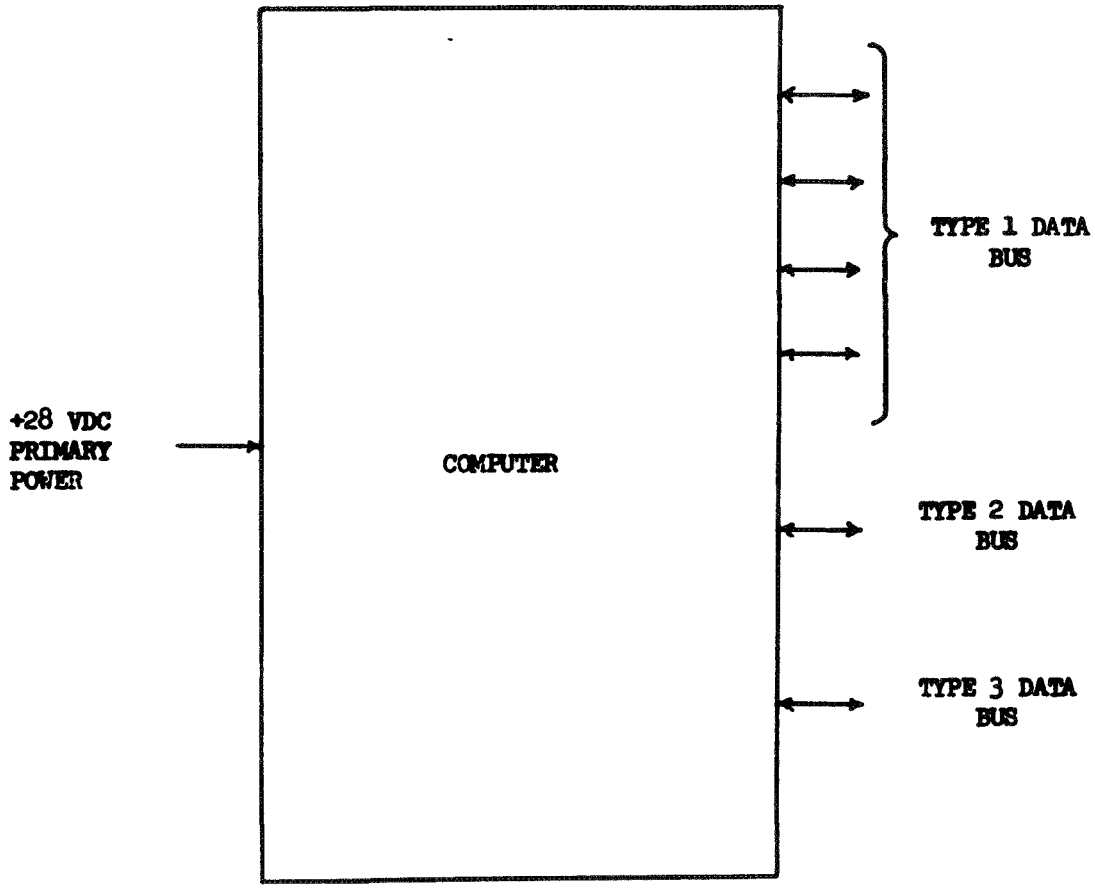
2.1.2 Interface Definition

2.1.2.1 Input Power

The computer shall be designed to comply with the requirements of MIL-STD-704A in the utilization of electric power. The computer shall provide specified performance when supplied with electric power having the characteristics described in paragraph 5.2 and in accordance with paragraphs 6.3 and 6.4 of MIL-STD-704A. The power input shall be from a +28 VDC source.

2.1.2.1.1 Power Interruption

The computer shall not be damaged by the interruption of the input power for any time period. During application of power to the computer, all computer outputs shall be held in the off state. When power is applied after a power shutdown or transient, the computer shall automatically execute a restart routine and resume operation in an orderly manner.



COMPUTER INTERFACE DIAGRAM

FIGURE 1.

2.1.2.2 Signal Interface

The signal interface with other equipment shall have the following characteristics:

a. All signals shall be complementary (two lines per signal).

b. Connecting cables will be twisted pair shielded transmission cable with controlled impedance.

c. A true signal shall be represented as a ground potential on the primary line and a positive potential on the complement line.

d. Data rates on the type 1 and 2 data buses shall be one megahertz.

e. Data rates on the type 3 data bus shall be 250,000 words per second.

f. Signals on the type 1 and 2 data buses shall be Manchester encoded.

g. Signals on the type 3 data bus shall be straight binary.

2.2 Characteristics

2.2.1 Functional Block Diagram

A functional block diagram of the computer is shown in Figure 2.

2.2.2 Central Processing Unit

The CPU shall be capable of performing logical and arithmetic operations in 16 or 32 bit word formats. All operations shall be done in parallel.

2.2.2.1 Data Formats

2.2.2.1.1 Fixed Point

The data words for fixed point operations shall be either 16 or 32 bits in length including sign. Data shall be represented in true binary with two's complement for negative numbers.

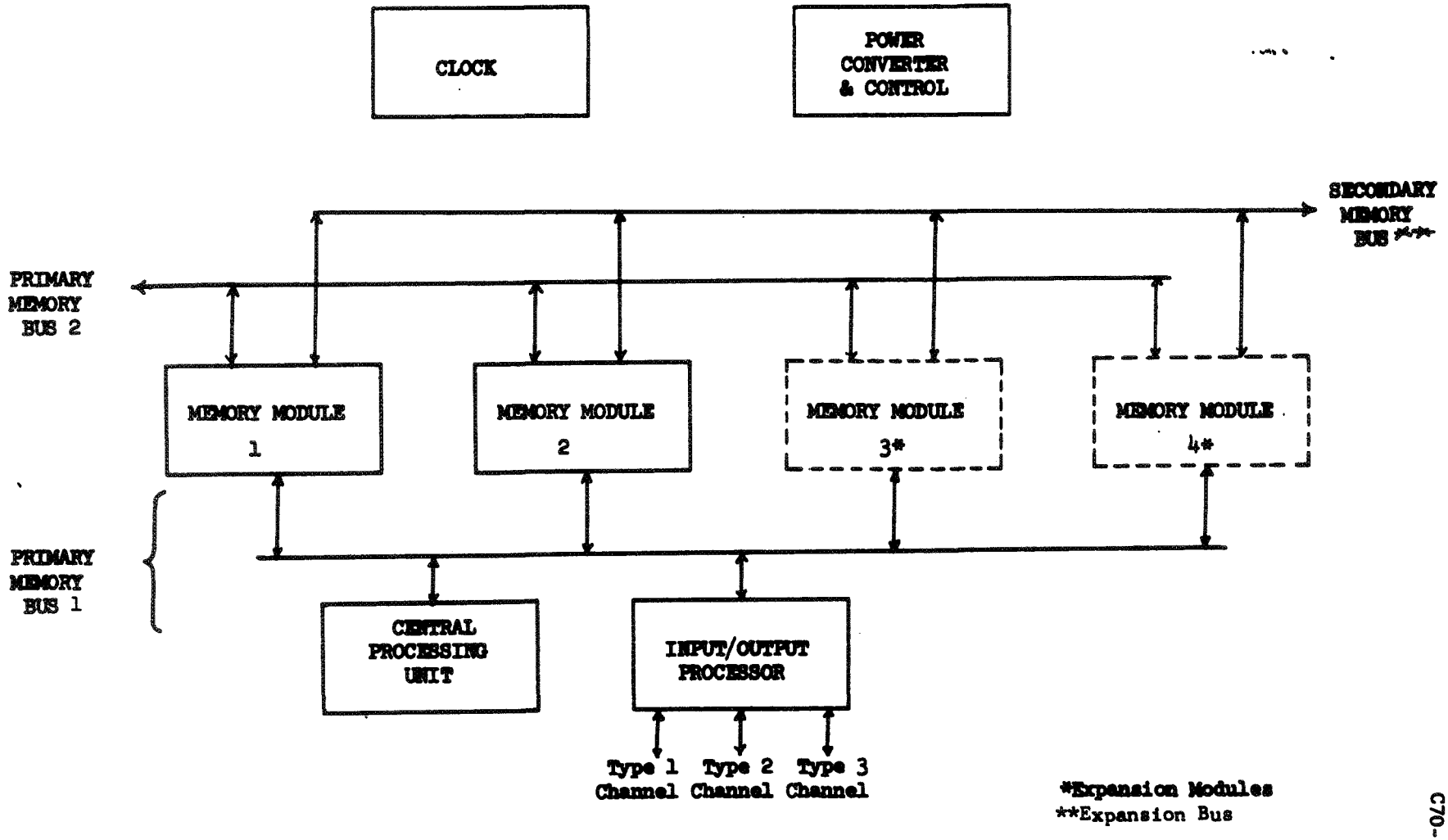
2.2.2.1.2 Floating Point

The data words for floating point operation shall be 32 bits long as follows:

a. Sign - The most significant bit

b. Characteristic - The next seven most significant bits

c. Mantissa - The 24 least significant bits



COMPUTER BLOCK DIAGRAM

FIGURE 2

2.2.2.2 Registers

The CPU shall contain sufficient registers to perform the following functions as a minimum:

a) Program Counting
b) Indexing
c) Memory Addressing
d) Arithmetic Operations
e) Logical Operations
f) Shifting Operations
g) Instruction Decoding
h) Masking
i) Control
j) Status Storage
k) Buffering

2.2.2.3 Interrupts

The CPU shall have the capability of executing interrupts generated internally or externally. There shall be a minimum of four internal and four external interrupts. The interrupts shall be capable of being masked under program control. The interrupts shall have a cyclic priority build into the hardware.

2.2.2.4 Instructions

The computer shall have a flexible instruction repertoire utilizing nine basic formats:

a) Register to register operations
b) Register operations
c) Shift operations
d) Program counter operations
e) Register to storage operations
f) Register to storage indexed operations
g) Register-register-storage operations
h) Storage and immediate operand operations
i) Floating point operations

Instructions shall be in half or full word formats and shall be capable of operating on half and full word data.

2.2.2.5 Read Only Memory

The CPU shall have a read only semiconductor memory for performing self-diagnostic and reconfiguration routines after a computer failure has been detected. This memory shall have a capacity of 8192 bits organized into 32 bit words. The ROM shall contain all addressing and readout circuitry internally.

2.2.2.6 Memory Interface

The CPU shall interface with up to 12 memory modules by means of the memory data bus.

2.2.3 Memory

The computer memory shall consist of up to four memory modules. Each module shall be independent of the others.

2.2.3.1 Memory Module

The memory module shall be a random access NDRO type

2.2.3.1.1 Word Length

The word length in the memory module shall be 34 bits (32 bits of data and two parity bits).

2.2.3.1.2 Capacity

The module shall have a capacity of 16,384 words.

2.2.3.1.3 Speed

The effective memory cycle time shall be less than or equal to 1.25 microseconds.

2.2.3.1.4 Data Protection

Data in the memory module shall be protected against alteration due to power fluctuations or unauthorized writing. Data changed during reading operations due to noise or circuit failure shall be detected and not sent out on the memory data bus.

2.2.3.1.4.1 Power Fluctuation Protection

The memory module shall finish the operation in progress when a power fluctuation is sensed. All further operation shall be inhibited until the power has returned to within normal operating limits.

2.2.3.1.4.2 Parity

A parity bit shall be generated and attached to each half word stored in memory. This parity bit shall make the number of ones in the 17 bit half word an odd number. The parity shall be checked when the half word is read from the array. Data having incorrect parity shall not be placed on the memory data bus. Detection of parity errors shall be reported to the CPU requesting the data.

2.2.3.1.4.3 Write Protection

The memory module shall be capable of assigning protected status to locations in the memory. The assignment of this status shall be under program control. Any attempt to write into protected locations shall be inhibited and an indication of the attempt reported to the CPU.

2.2.3.1.5 Memory Data Bus Interface

The memory module shall be capable of interfacing with up to three memory data buses. Each bus shall be connected to a different combination of CPU and IOP. Two of these buses shall be considered primary and equal and the third bus shall be considered a secondary bus. The module address for each bus shall be set independently of the other buses.

2.2.3.1.6 Memory Module Control

2.2.3.1.6.1 Module Address

Each memory module shall have a four bit address code associated with each memory data bus that can be changed under program control by the CPU on that bus. These address codes shall be stored in dedicated locations in the memory. Only data accompanied by the proper address code shall be accepted by the module. A special address code (same for all three data buses) that is mechanically set into the module shall be provided to permit initial startup operation.

2.2.3.1.6.1.1 Address Restoration

When the computer recovers from a temporary loss of power, the memory module shall restore all addresses by reading the contents of dedicated memory locations into the three address registers.

2.2.3.1.6.2 Control Codes

The memory module shall be capable of executing the following control codes codes:

a. Read data word
b. Write full word
c. Write left half word
d. Write right half word
e. Mode command present
f. Read module mode
g. Restore module address
h. Read module address
i. Store module address

Codes a. through g. shall be honored when they are accompanied by the program determined address code. Codes h. and i. shall be honored when accompanied by the mechanically determined address code.

2.2.3.1.6.3 Mode Control

The module mode of operation shall be determined by the mode commands received from the CPU. With no computer failures, identical commands must be received over both primary busses before the module mode can be changed. A failure of a computer on a primary bus shall cause the module to honor mode commands received over the remaining primary bus. Failures of the computers on both primary buses shall cause the module to honor mode commands received over either primary bus. No mode commands received over the secondary bus shall be honored by the module. One mode command shall determine the mode for the primary buses. A second mode command shall determine the mode for the secondary bus. The following modes shall be possible for all buses:

a. Full operation
b. No operation
c. Read only operation
d. Scratch pad operation
e. Read only and scratch pad operation

Scratch pad operation shall be defined as read and write capability for a specified set of locations in memory.

2.2.3.1.6.3.1 Primary Bus Mode Commands

The memory module shall be capable of setting up modes for the primary buses according to the following commands:

a. Full operation on both primary buses
b. Full operation on bus 1; no operation on bus 2
c. Full operation on bus 1; read only operation on bus 2
d. Full operation on bus 1; scratch pad operation on bus 2
e. Full operation on bus 1; read only and scratch pad operation on bus 2
f. Full operation on bus 2; no operation on bus 1
g. Full operation on bus 2; read only operation on bus 1
h. Full operation on bus 2; scratch pad operation on bus 1
i. Full operation on bus 2; read only and scratch pad operation on bus 1

2.2.3.1.6.3.2 Secondary Bus Mode Commands

The memory module shall be capable of setting up modes for the secondary bus according to the following mode commands:

a. No operation
b. Full operation
c. Read only operation
d. Scratch pad operation
e. Read only and scratch pad operation

2.2.4 Memory Data Bus

All communications with the memory modules shall be over a memory data bus. Each memory data bus shall connect to one CPU, one IOP, and up to 12 memory modules. The data flow over the bus shall be between the CPU and the memory and between the IOP and the memory. Memory data bus operations shall be initiated by either the CPU or the IOP. Simultaneous requests for data bus access by the CPU and IOP shall be resolved in favor of the IOP. Data on the bus shall be handled in bit parallel and word serial fashion. The bus word length shall be 16 bits.

2.2.4.1 Data Rate

The memory data bus shall be operated at a ten megahertz rate when data are being transferred.

2.2.4.2 Data Bus

The data shall be made up of the following:

a.	Address lines	18
b.	Control lines	6
c.	Data in lines	16
d.	Data out lines	16

2.2.5 Input/Output Processor

The IOP of the computer shall perform the following functions:

a. Communication with external devices
b. Program time synchronization
c. Computer fault detection
d. Majority voting on data

The IOP shall perform according to an internally stored program, control words received from external devices or signals generated by computer hardware.

The IOP shall consist of the following functional areas:

a. Type 1 data bus
b. Type 2 data bus
c. Type 3 data bus
d. Voter-Comparator-Switch (VCS)
e. Built-in test equipment (BITE) counter
f. Real time counter (RTC)
g. Master sync controller (MSC)

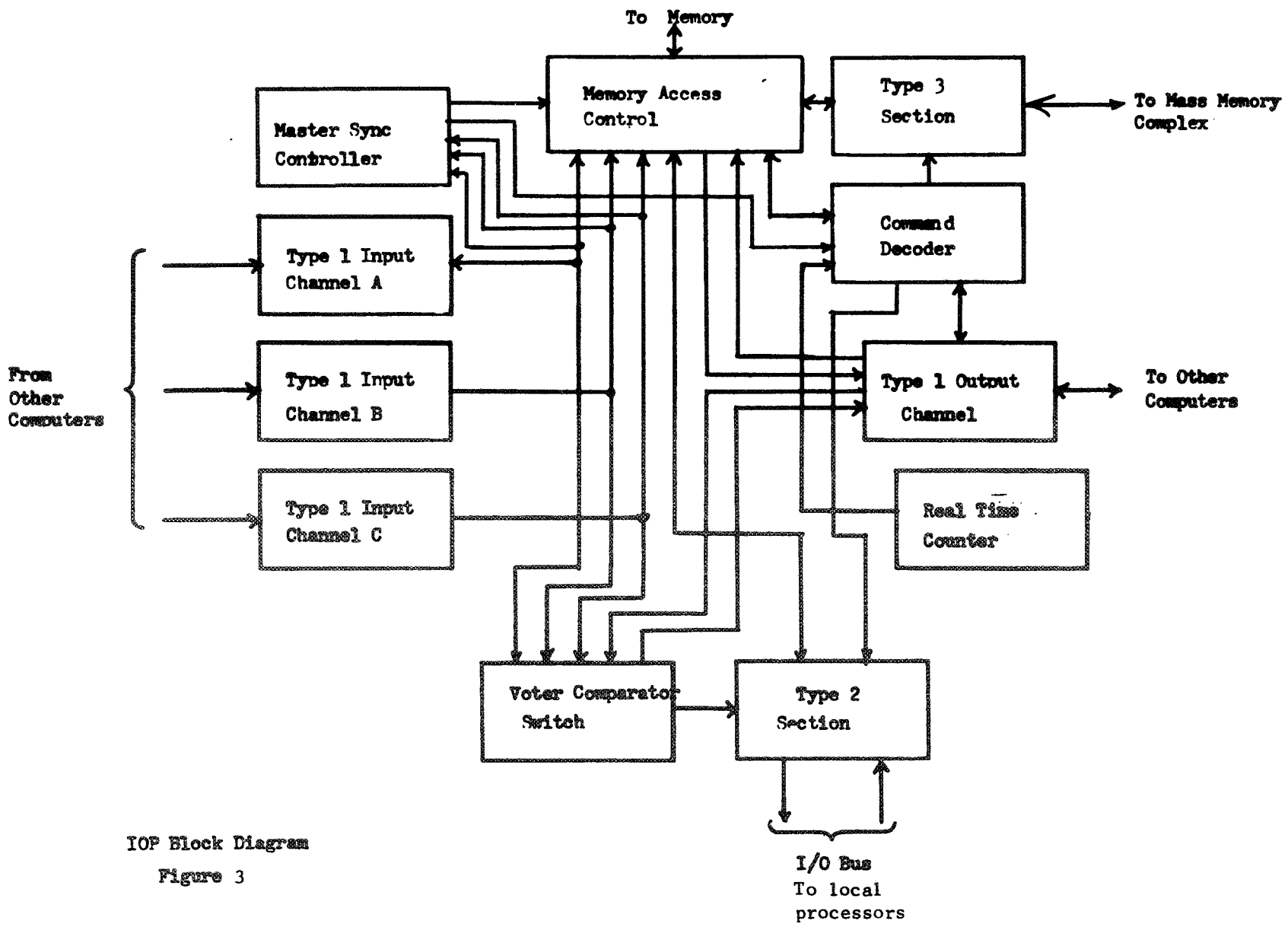
A block diagram of the IOP is shown in Figure 3.

2.2.5.1 Program Commands

The IOP shall be capable of executing four program commands. The commands are:

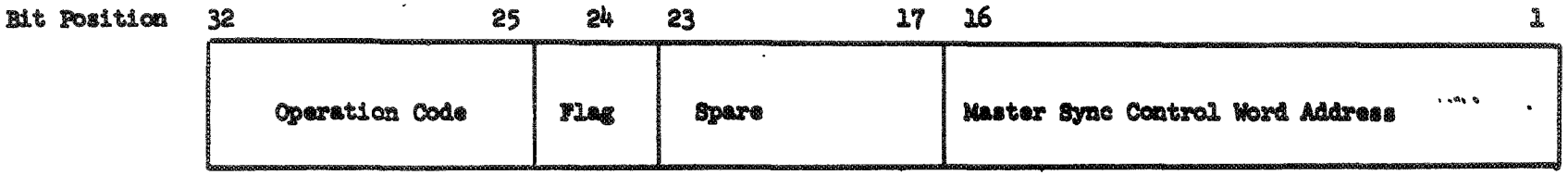
a. Halt and proceed
b. Jump
c. Conditional skip
d. Fetch control word

The command formats are shown in Figure 4.

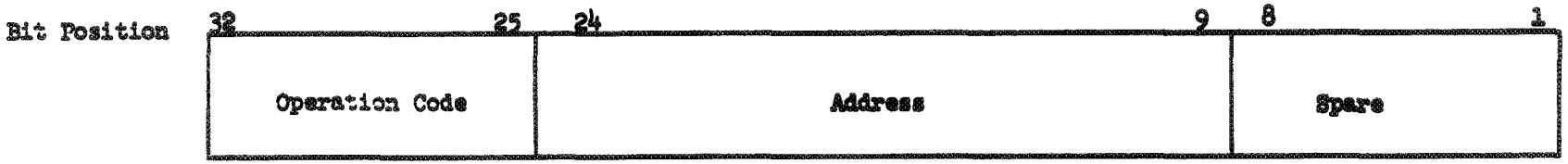


IOP Block Diagram

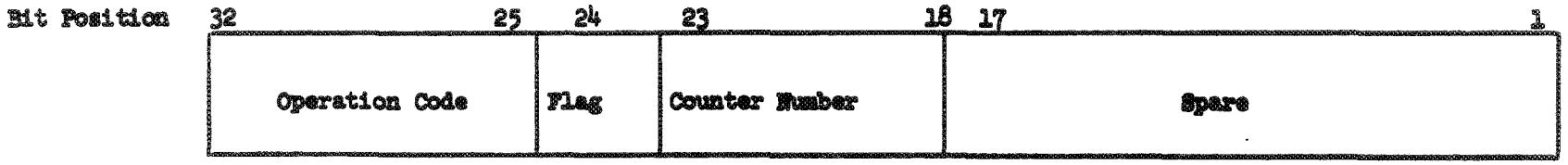
Figure 3



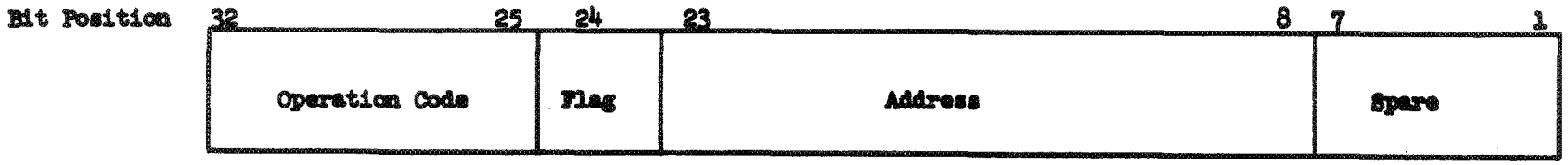
Halt and Proceed



Jump



Conditional Skip



Fetch Control Word

IOP COMMAND FORMATS

FIGURE 4

2.2.5.1.1 Halt and Proceed

The command shall cause the IOP to enter an idle state where no other commands are executed. The IOP shall respond to control words received from an external device. The flag bit of the command shall have the following meaning:

a. Flag bit is zero - The IOP shall exit the idle mode upon receipt of the real time counter interrupt.
b. Flag bit is one - The IOP shall execute a master sync operation when the real time counter reaches 72. The IOP shall exit the idle mode upon receipt of the cycle start interrupt from the master sync controller.

2.2.5.1.2 Jump

This command shall cause the IOP to use the address field as the location of the next command to be executed.

2.2.5.1.3 Conditional Skip

This command shall cause the IOP to increment the IOP program counter according to the condition of a counter and the state of the flag bit. The execution of the command shall be as follows:

a. A counter is accessed from memory
b. The counter is incremented once
c. If an overflow occurs, the counter is re-initialized and stored back in memory. The IOP program counter is incremented once.
d. If there is no overflow, the flag bit is checked.
e. If the flag bit is a zero, the incremented counter is stored back in memory and the IOP program counter is incremented twice.
f. If the flag bit is a one, the IOP program counter is incremented twice.

2.2.5.1.4 Fetch Control Word

This command shall cause the IOP to access the memory location specified by the address field. The flag bit shall have the following meaning:

a. Flag bit is zero - All data buses are operational
b. Flag bit is one - The type 3 bus is masked out - All other buses are operational

2.2.5.2 Control Words

The IOP shall be capable of executing control words accessed from memory or received from other devices. The control words are:

a. Computer to local processor

b. Computer to computer (memory)

c. Computer to computer (IOP)

d. Acknowledge

The control word formats are shown in figure 5.

2.2.5.2.1 Computer to Local Processor Control Word

This control word is used when data are to be sent to or requested from a local processor. The fields of control word are defined as follows:

Field	Bits	Definition
*Computer Address	4	Indicates which computers are to receive the control word. Any combination of computers may be addressed by setting the appropriate bits to ONE.
Type	2	Identifies control word type.
Retransmit	1	ONE: Message is to be sent again if an error is detected in the transmission. ZERO: Message is to be sent once.
LP Address	5	Identifies the local processor being accessed by the computer.
I/O	1	ONE: Data are to be input to the computer. ZERO: Data are to be output from the computer.
Data Location	6	Identifies the address of the first data word of the message in the local processor memory.
*Reply Buses	4	Identifies the buses over which data are to be transmitted from the local processor to the computer.
Number of Words	6	Indicates the number of data words in the message.

Bit Position	32 29	28 27	26	25 21	20	19 17	16 11	10 7	6 1
	Computer Address	Type	Re-xmit	L P Address	I/O	Spare	Data Location	Reply Buses	Number of Words

Computer to Local Processor Control Word

Bit Position	32 29	28 27	26 21	20	19 17	16 13	12 7	6 1
	Computer Address	Type	Memory Address	I/O	Spare	Return Address	Return Store Address	Number of Words

Computer to Computer (Memory) Control Word

Bit Position	32 29	28 27	26 23	22 19	18 17	16 13	12 7	6 1
	Computer Address	Type	Operation Code	Data Address	Spare	Return Address	Return Store Address	Spare

Computer to Computer (IOP) Control Word

Bit Position	32 29	28 27	26 21	20	19 17	16 12	11 7	6 1
	Reply Buses	Type	Data Location	I/O	Spare	L P Address	L P Status	Number of Words

Acknowledge Control Word

CONTROL WORD FORMATS

FIGURE 5

2.2.5.2.1 Computer to Local Processor Control Word (Cont)

When the control word is first accessed from memory, the fields marked by an asterisk in the above list are not the codes having the meaning given in the definition column. The initial value of these fields is used as an address to get the actual codes to be used in the control word. The IOP places the initial values in the least significant bit positions of the operand program counter, sets the upper bits to a fixed code and accesses the memory. The word accessed from memory contains the true codes which are inserted into the register holding the control word. The control word is ready to be transmitted.

2.2.5.2.2 Computer to Computer (Memory) Control Word

This control word is used when data are to be sent between computer memories over the inter-computer bus. The field of the control word are defined as follows:

Field	Bits	Definition
Computer Address	4	Same as Para. 2.2.5.2.1
Type	2	Same as Para. 2.2.5.2.1
Memory Address	6	Identifies a location in the memory of the computer receiving the control word.
I/O	1	Same as Para. 2.2.5.2.1
Return Address	4	Identifies the computer sending the control word.
Return Store Address	6	Identifies a location in the memory of the computer sending the control word.
Number of Words	6	Same as Para. 2.2.5.2.1

2.2.5.2.3 Computer to Computer (IOP) Control Word

This control word is used when the R, P and S matrices of the VCS of the other computer are to be sampled or set and when a master synch operation is to be performed. The fields of the control word are defined as follows:

Field	Bits	Definition
Computer Address	4	Same as Para. 2.2.5.2.1
Type	2	Same as Para. 2.2.5.2.1
Operation Code	4	Identifies the operation to be performed by the receiving IOP.

2.2.5.2.3 Computer to Computer (IOP) Control Word (Cont)

Field	Bits	Definition
Data Address	4	Identifies the location in the memory of the transmitting computer of the data to be used in setting the matrices.
Return Address	4	Same as Para. 2.2.5.2.2
Return Store Address	6	Same as Para. 2.2.5.2.2

The data address field of the control word, when read from memory, forms the least significant bits of the location of the actual address to be used for accessing the data to be sent.

The operation field codes are as follows:

Bits	26	25	24	23	Operation
	0	0	0	0	Set R and P matrices to value; Set S matrix to zero
	0	0	0	1	Set R matrix to value
	0	0	1	0	Set P matrix to value
	0	0	1	1	Set S matrix to zero
	0	1	0	0	Sample R, P and S matrices
	0	1	0	1	Sample R matrix
	0	1	1	0	Sample P matrix
	0	1	1	1	Sample S matrix
	1	0	0	0	Master Sync

2.2.5.2.4 Acknowledge Control Word

The control word is generated by the local processors and sent to the computer. The control word is sent to acknowledge the receipt of data by the local processor or to start the transmission of data by the local processor. The fields of the control word are defined as follows:

Field	Bits	Definition
Reply Buses	4	Same as Para. 2.2.5.2.1
Type	2	Same as Para. 2.2.5.2.1
Data Location	6	Same as Para. 2.2.5.2.1
I/O	1	Same as Para. 2.2.5.2.1
LP Address	5	Same as Para. 2.2.5.2.1
LP Status	5	Identifies the operational status of the local processor and errors in data received by the local processor.
Number of Words	6	Same as Para. 2.2.5.2.1

2.2.5.3 Type 1 Data Bus

The type 1 data bus shall consist of four input channels and one output channel. This data bus shall be used for computer to computer communications. Data rates on the bus shall be one megahertz. Data words shall be 17 bits long including parity. Data transfer shall be serial by bit and serial by word. Data messages shall consist of one control word followed by up to 63 data words.

2.2.5.3.1 Input Channel

Data received over the input channel shall be sent to the memory, VCS, or MSC according to the control word. During certain voting modes, the input channel shall compare the data sent out by the IOP against the data sent out by the voter (the voter being used is external to the computer). The results of this comparison shall be stored in memory and shall be used to generate a go or no-go code for output messages. All operations over the input channel shall be initiated by control words.

2.2.5.3.2 Output Channel

Data sent out on the output channel shall come from either the memory or the type 2 input channel. Operation over this channel shall be initiated by a control word from memory or by the receipt of data on the type 2 input channel. The type 2 input channel shall have priority for outputting on this channel.

2.2.5.4 Type 2 Data Bus

The type 2 data bus shall consist of one input channel and one output channel. This data bus shall be used for communications with all external devices other than the computers. Data rates on the bus shall be one megahertz. Data words shall be 17 bits long including parity. Data transfer shall be serial by bit and serial by word. Data messages shall consist of one control word followed by up to 63 data words.

2.2.5.4.1 Input Channel

The input channel operations shall be initiated by the receipt of a control word. Data received over the channel shall be sent to the memory and/or the type 1 output channel. During voting modes using the internal VCS, data received on this channel shall be compared with the data sent to the VCS. The results of this

2.2.5.4.1 Input Channel (Cont)

comparison shall be stored in memory and shall be used to generate a go or no-go code for output messages.

2.2.5.4.2 Output Channel

The output channel operation shall be initiated by a control word from memory. Data sent out over this channel shall be from the memory in a non-voting mode and from the VCS during voting or comparison modes using the internal VCS.

2.2.5.5 Type 3 Data Bus

The type 3 data bus shall consist of a bi-directional parallel channel between the computer and the data management system. Data shall be transmitted in bit parallel, word serial fashion. Data words on this bus shall be 16 bits long. Data rates on this bus shall be 250,000 words per second. Messages shall consist of one control word and up to 127 data words. This bus shall be capable of being masked off by program control. Operations over this bus shall be initiated by the data management system and shall be on a "ready-read" basis. The data bus shall consist of the following:

a.	Data lines	16
b.	Control lines	2
c.	Parity line	1

2.2.5.6 Real Time Counter

The real time counter shall be capable of measuring a specified time interval by decrementing a counter at the logic clock rate. The counter shall be 15 bits long. The counter shall autometically re-initialize when it reaches zero. The initializing constant shall be held in a buffer register which can be loaded by the program. An interrupt shall be issued when the RTC reaches zero.

2.2.5.7 BITE Counter

The BITE counter shall be a counter that is decremented at the logic clock rate. The counter shall be initialized by reading a number from memory into the counter. The counter shall issue a load counter discrete at the count of 1024. The counter shall issue a computer no-go discrete if the counter is not initialized before reaching zero. The counter shall be 15 bits long. The initializing constant shall be placed in memory by the CPU program. When the initializing constant is read out of memory, the memory location shall be set to zero.

2.2.5.8 Voter-Comparator-Switch

The VCS shall perform the voting or comparison function according to the modes as determined by two computers. The functional areas of the VCS are:

a. R matrix
b. P matrix
c. S matrix
d. Voter /Comparator
e. Input channel

2.2.5.8.1 R Matrix

The R matrix shall consist of 16 data bits, four bits set by each computer in the complex. These 16 bits shall determine the operating mode of the VCS and which computers are involved. The mode determining logic shall be modified by the P matrix. A mode shall be entered if a majority of the non-failed computers input identical four bit codes to the R matrix. The modes are:

a. Four way voting - data from all four computers must be compared in the voter to determine a majority.
b. Three way voting - data from three computers shall be compared in the voter. The computers involved shall be indicated by the presence of ones in the matrix.
c. Two way comparison in data from two computers shall be compared in the voter. The computers involved shall be indicated by the presence of ones in the matrix.
d. No voting - The VCS is not used.

2.2.5.8.2 P Matrix

The P matrix shall consist of 16 bits, three set by each computer. These bits shall represent the operating conditions of all computers as determined by each computer. A binary zero in any position of the matrix shall indicate a failed computer as determined by another computer. The matrix takes the form as follows:

2.2.5.8.2 P Matrix (Cont)

Computer Doing the Fault Determination

		I	II	III	IV
Computers	I	*			
Being	II		*		
Studied	III			*	
	IV				*

* Indicate the diagonal positions

A binary zero in a diagonal position as shown shall indicate that that computer is failed and its outputs should be disregarded. The failed computer's entry in the R matrix shall be ignored in the mode determination. The diagonal terms shall be set to zero as follows:

a. The computer no go discrete is true
b. A majority of the non-failed computers have indicated the computer is bad by the entries in the P matrix.

2.2.5.8.3 S Matrix

The S matrix shall consist of 16 bits, four for each computer. This matrix shall indicate the status of the data received by the VCS according to the voting process. Binary ones shall be placed in the matrix to indicate that a computer's data did not agree with the majority data from the voter.

2.2.5.8.4 Voter/Comparator

The voter shall compare the data according to the P and R matrices. The majority data shall be sent to the type 2 output channel for transmission. If no majority is found, no data shall be sent to the type 2 output channel and the operation shall be terminated.

2.2.5.8.5 Input Channel

The VCS shall have four input channels. The input channel shall buffer the data being received from the various computers to remove time variations in the data up to $\pm \frac{1}{2}$ word time.

2.2.5.9 Master Sync Controller

The master sync controller shall receive master sync control words over the type 1 input channels from all other computers. The time of arrival of each control with respect to the time of arrival of the first one shall be determined and stored. A cycle start discrete shall be issued eight logic times after arrival of the second master sync control word.

2.2.6 Secondary Power

2.2.6.1 Power Converter

The computer shall have a power converter that provides the regulated dc voltage levels from the unregulated +28 Vdc primary power. The converter shall be capable of powering the maximum computer configuration.

2.2.6.2 Power Control

The computer shall have power control circuitry to:

a. Insure the preservation of memory contents during turn on, turn off and input power transients.

b. Sense internal computer operating temperatures so that an orderly shut down of regulated levels may occur without any loss of memory contents when the temperature is too high.

c. Return the computer to the operating condition starting at a pre-determined instruction location after the power or temperature condition that caused the shut down has been removed.

2.2.7 Clock

The computer shall contain a crystal controlled oscillator to perform the clocking function. The logic clock frequency shall be one megahertz $\pm$ 0.01 percent.

A single phase 10 megahertz clock shall be provided for the memory data bus.

NASA — MSC — Coml., Houston, Texas