N71-19794

RECONFIGURABLE G & C COMPUTER STUDY FOR SPACE STATION USE

FINAL REPORT

VOLUME VII

APPENDICES 5,6,7,8 & 9

31 January 1971

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Prepared Under Contract No. NAS9-10416

Autonetics Division of North American Rockwell
for
Manned Spacecraft Center
National Aeronautics and Space Administration

FOREWORD

This final report covers the work performed by Autonetics Division of North American Rockwell Corporation under a study contract entitled Reconfigurable G&C computer Study for Space Station Use. The report is submitted to the National Aeronautics and Space Administration Manned Spacecraft Center under the requirements of Contract NAS 9-10416. The study program covered the period from December 29, 1969 through January 31, 1971. The NASA Technical Monitor was Mr. E. S. Chevers.

The final report consists of seven (7) volumes:

Volume I	Technical Summary	
Volume II	Final Technical Report	
Volume III	Appendix I.	Model Specification
Volume IV	Appendix 2.	IOP - VCS Detailed Design
Volume V	Appendix 3.	System Analysis and Trade-Offs
Volume VI	Appendix 4.	Software and Simulation Description and Results
➧Volume VII	Appendix 5.	D-200 Computer Family
	Appendix 6.	System Error Analysis
	Appendix 7.	Reliability Derivation for Candidate Computers
	Appendix 8.	Power Converter Design Data
	Appendix 9.	Data Transmission Medium Design

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APPENDIX 5

C70-171/301

1. D200 BUILDING BLOCKS

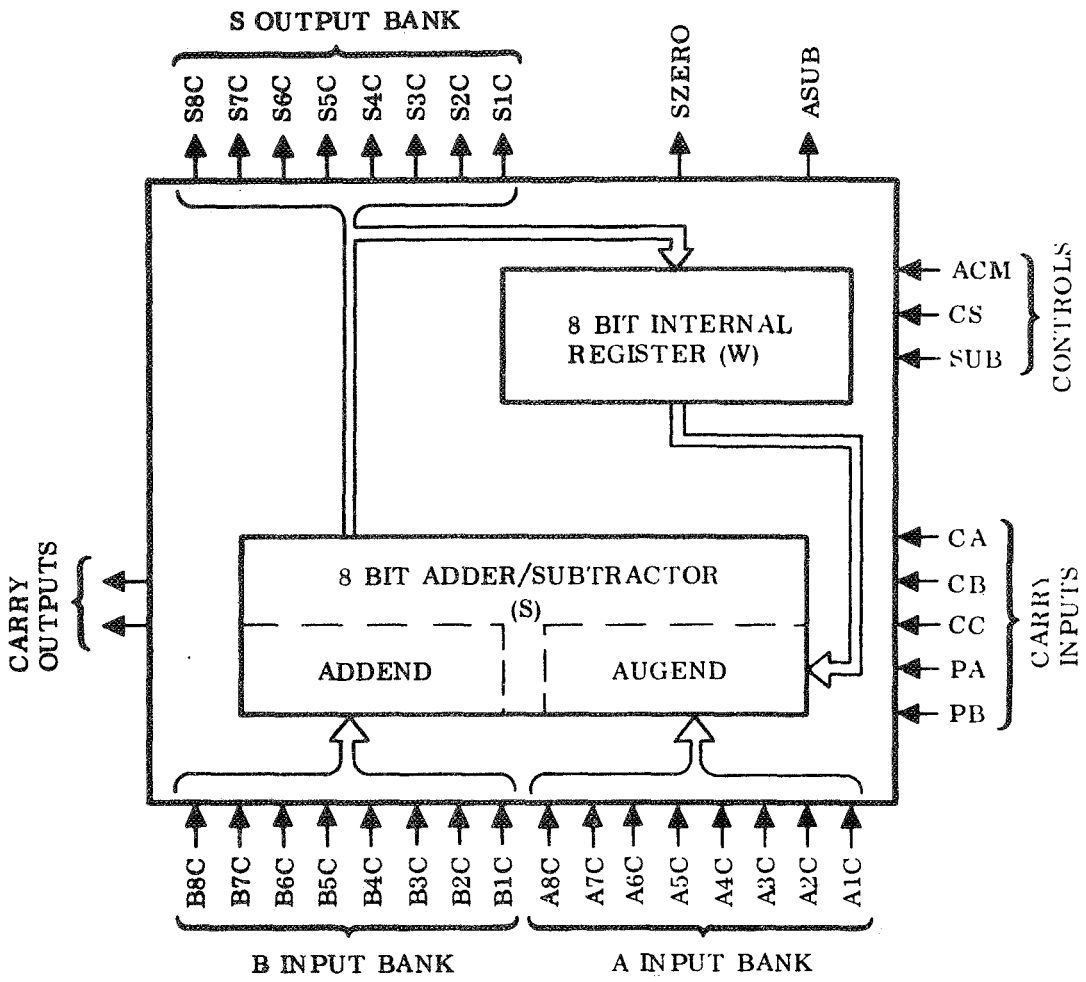
Autonetics recently undertook an advanced computer development program to define their next generation of computers. Presently, prototypes are being assembled. The computer family is based on a family of building block MOS/LSI devices. The following sections discuss the modularity in the design of the processor for the D-200 family.

The basic arithmetic unit element is an 8 bit parallel adder/subtractor and accumulator register section. The 42 pin configuration of the A chip, as illustrated in Figure 1. provides for two independent parallel input banks of eight bits each. These two banks may be added or subtracted, and the result is available on the S output bank one bit time later. The A chip, as all other basic elements of the D200 family, is presently designed to operate at a bit rate of one megahertz.

Another mode of operation for the A chip enables one of the input banks to be added to the 8 bit internal register with the result replacing the contents of the 8 bit internal register and also appearing on the output bank. A list of the total modes of operation for the A chip appears in the figure. When the two input banks are being added together and the internal register retains its values the A chip can be used for indexing in a general purpose computer arithmetic section. During this indexing operation, the accumulator remains in the W flip flops of the A chips.

When an input bank is added or subtracted from the internal register W, this is for the purposes of adding or subtracting to the accumulator.

The carry inputs and outputs illustrated in the figure enable a maximum of four A chips to be interconnected to mechanize a maximum 32 bit arithmetic unit whose register to register add time is 1 microsecond. Two A chips are used for the 16 bit arithmetic unit and accumulator for the 16 bit D200 computers. Three A chips are used for the 24 bit D200 computers. All add times for the various bit lengths are one microsecond.



CONTROL STATES	OPERATION
0	A + B → S, W → W
1	A - B → S, W → W
2	A + B → S & W
3	A - B → S & W
4	B → S & W
5	A → S & W
6	W + B → S & W
7	W - B → S & W

A MAXIMUM OF 4 IC'S MAY BE USED TO YIELD A 32 BIT ADDER/SUBTRACTOR

1 BIT TIME DELAY FROM INPUT TO OUTPUT

Figure 1. "A" Chip

Registers, Interface, and Boolean Function Element - The B Chip

With the exception of shifting paths to be discussed in the next paragraph, the B chip and the previously discussed A chip comprise the complete mechanization of a wide variety of arithmetic processors for the D200 family of computers. The B chip serves three important functions: (1) to house all registers necessary for computer operations, with the exception of the accumulator which is housed in the A chip, as discussed above, (2) to furnish the interface between the memory and the arithmetic processor, this interface consists of both a time and storage buffer, and (3) the extensive list of Boolean functions available in the D200 family of computers is mechanized in the B chip.

The B chip (Figure 2) is a 4 bit wide element. Two B chips are used with one A chip. In a 16 bit computer two A chips would furnish the accumulator and basic arithmetic, and four B chips would then complete the requirements for registers, interface, and Boolean functions shown in Table 1.

Ten registers are provided in each B chip. Being 4 bits wide, the B chip, therefore, contains the equivalent of 40 flip-flops plus the logic for the operations described below. The registers are organized into the following groupings:

1. A lower accumulator register sometimes known as the extension to an accumulator register which houses the lesser significant half of the product resulting from a multiply operation or the remainder resulting from the divide operation.

2. A register for holding the index register selected by the instruction word for use in modifying the address of the instruction word.

3. A buffer register for housing the operand for arithmetic operations, and serving as a time and storage buffer between the arithmetic processor and memory.

4. A general register file of seven registers which may be used according to the design of the control chips and the various requirements of the instruction set in the particular mechanization within the D200 family of computers. Many uses mechanized so far have spelled out six of these seven registers as index registers, and one of these as a temporary storage register for the accumulator and operand for accumulative multiply instructions.

Shifting paths for the registers provided in the B chip are built into the B chip. This enables left and right shifting paths for both shift operations and the multiply and divide operations. Sufficient shifting paths are built in to enable an arithmetic processor to be configured with either a 2 bit or a 4 bit at a time multiply algorithm.

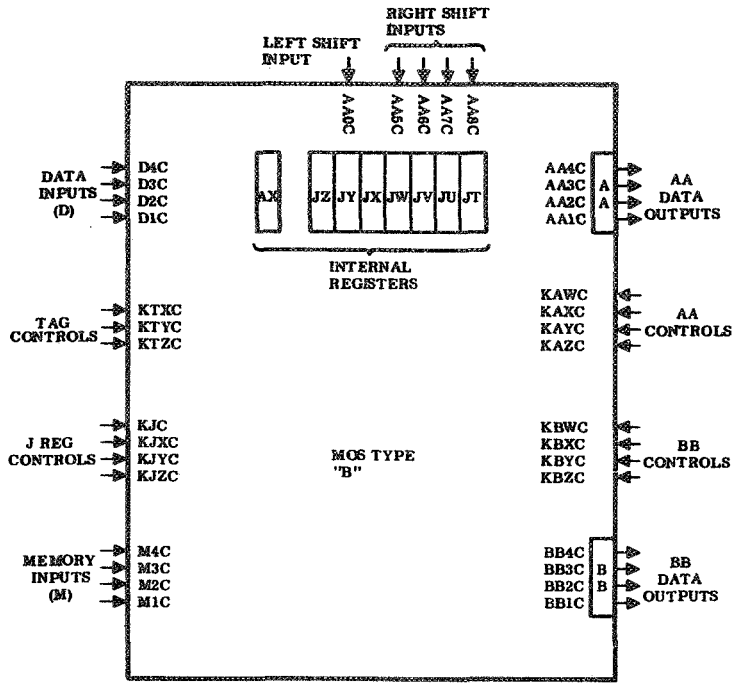


Figure 2. "B" Chip

Table 1. Independent Control States for MOS Type "B" IC

BB Control States	Operation
1	BB → BB
2	AX → BB
3	$\overline{D}$ → BB
4	$\overline{D}$ → BB
5	M → BB
6	D · M → BB
7	AX · M → BB
8	BB · M → BB
9	D + M → BB
10	BB + M → BB
11	AX · D + $\overline{AX}$ · M → BB
12	AX · BB + $\overline{AX}$ · M → BB
13	ZERO → BB
14	D + BB → BB
15	D · BB → BB
16	D ⊕ BB → BB

AA Control States	Operation
1	AX → AX, AA
2	BB → AX, AA
3	D → AX, AA
4	M → AX, AA
5	2AA → AX, AA
6	1/2AA → AX, AA
7	1/4AA → AX, AA
8	1/16AA → AX, AA
9	AX → AX } Tag controls
10	BB → AX } Determine
11	D → AX } Contents of AA
12	AX → AX, AA → AA
13	2AA → AX } Tag controls
14	1/2AA → AX } Determine
15	1/4AA → AX } Contents of AA
16	1/16AA → AX }

J Register Control States	Operation
1	None
2	BB → JT
3	BB → JU
4	BB → JV
5	BB → JW
6	BB → JX
7	BB → JY
8	BB → JZ
9	None
10	D → JT
11	D → JU
12	D → JV
13	D → JW
14	D → JX
15	D → JY
16	D → JZ

Tag Control States	Operation: Only Performed for States 9 - 11 and 13 - 16 of AA Controls
1	Value placed in AX is also placed in AA
2	JT → AA } FOR J REGISTER CONTROL STATES 2 - 8 AND 10 - 16 THE APPROPRIATE VALUE, BB OR D, IS PLACED IN AA (i.e., AFTER THE OPERATION, AA AND THE SELECTED INDEX REGISTER WILL BE EQUAL)
3	JU → AA
4	JV → AA
5	JW → AA
6	JX → AA
7	JY → AA
8	JZ → AA

The Steering Logic Element - The ST Chip

The ST chip. Figure 3. is a three to one. 8 bit byte multiplexer which is used extensively within the D200 family. It includes three banks of 8 bit input lines and one bank of 8 bit output lines. The function of the ST chip is to select one of the eight input banks according to the signals on its control lines and present the information on the output bank. A crucial feature in the operation of the ST chip is its speed. It is intended to operate between bit times. Information processed, say, in a B chip will be steered through an ST chip and be available for an operation in an A chip at the next bit time. The ST chip is designed to perform its function in 200 nanoseconds. This steering logic element is basic to the modularity scheme in the D200 family of computers and enables a wide variety of processor configurations. It is used in all basic arithmetic processor configurations to mechanize shifting paths into the accumulator (the B chip has shifting paths built into it).

Basic Counter Element - The P Chip

The P chip is a basic 16 bit up/down counter logic element. It has a wide variety of uses reflected in its mode of operations in Figure 4. It can be used merely as a 16 bit register. Internal shifting paths are incorporated into the P chip so it can be used as a serial-to-parallel and parallel-to-serial converter. Its basic function is as an up/down counter, and because of this it is used as the program counter (hence, the name P chip) in all arithmetic processor configurations of the D200 family of computers. It is used in many of the real time clock configurations associated with the various computer I/O's and processors. as well as control, address, and conversion registers in I/O processors.

Other Chips

The PI chip mechanizes eight parallel and independent program interrupt channels. It is an example of a modular element which mechanizes control functions. It is a standard control element. a widely used IC which controls to some degree the operation of the entire processor.

A goal in the D200 family of computers is to design modular arithmetic control IC's that are independent of the bit length. The same control IC (C_L) may mechanize two bit-at-a-time multiply and other basic arithmetic operations for 16, 24, or 32 bit processors, while another control type (C_M) may mechanize a four bit-at-a-time multiply for 16, 24. or 32 bit processors.

Each computer in the D200 family will have at least one control type unique to itself. This will house the particular instruction set that was judged best for the computer's application.

The R chip. whose design has been completed, is an example of a special purpose modular element. The R chip can be added to the design of an existing processor for a square root instruction. A 16 bit processor requires two R chips; a 24 bit processor three R chips; and a 32 bit processor four R chips.

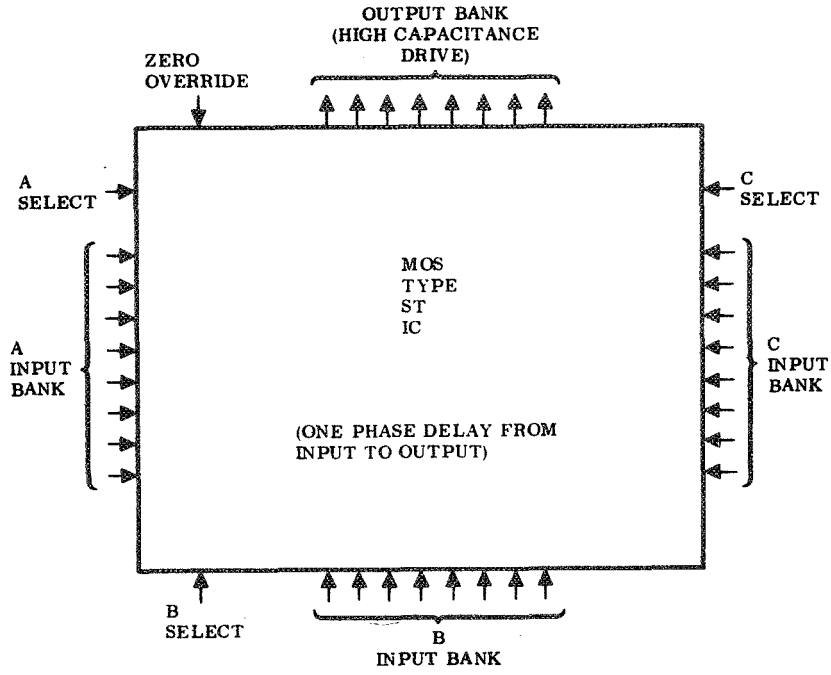
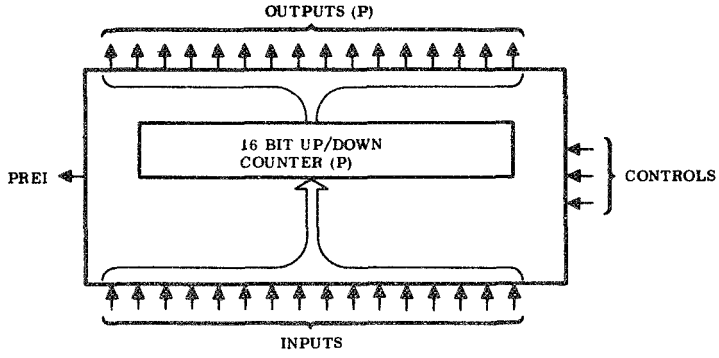


Figure 3. ST Chip



CONTROL STATES	OPERATION
1	MAINTAIN VALUE (P → P)
2	RIGHT SHIFT P — INPUT BITS FOR SHIFTING ARE RIGHT & LEFT INPUT BITS RESPECTIVELY
3	LEFT SHIFT P
4	LOAD INPUTS IN P
5	DECREMENT (P - 1 → P)
6	INCREMENT (P + 1 → P)
7	LOAD INPUTS MINUS 1 IN P
8	LOAD INPUTS PLUS 1 IN P

Figure 4. P Chip

2. D200 COMPUTERS

The use of the MOS large scale building blocks to implement a variety of arithmetic and control centers is described by the next series of figures. First, a 16 bit arithmetic center is shown in Figure 5. It consists of two 8-bit slices with each slice containing one A device, two B devices, and four ST devices. Next, Figure 6 shows a complete arithmetic and control center. Two additional ST devices have been added to interface with the memory. A P device is added for use as a program counter. A PI device is added for eight channels of program interrupt. The CL device is added for control of length operations and finally C1 has been added to implement a minimal instruction set in the 16 bit arithmetic center. Figure 7 shows an extended arithmetic and control center where two R devices have been added for a built-in square root. Additional PI devices are added for increasing the interrupt capability and C1 has been replaced by C2 and C3 for an extended instruction repertoire.

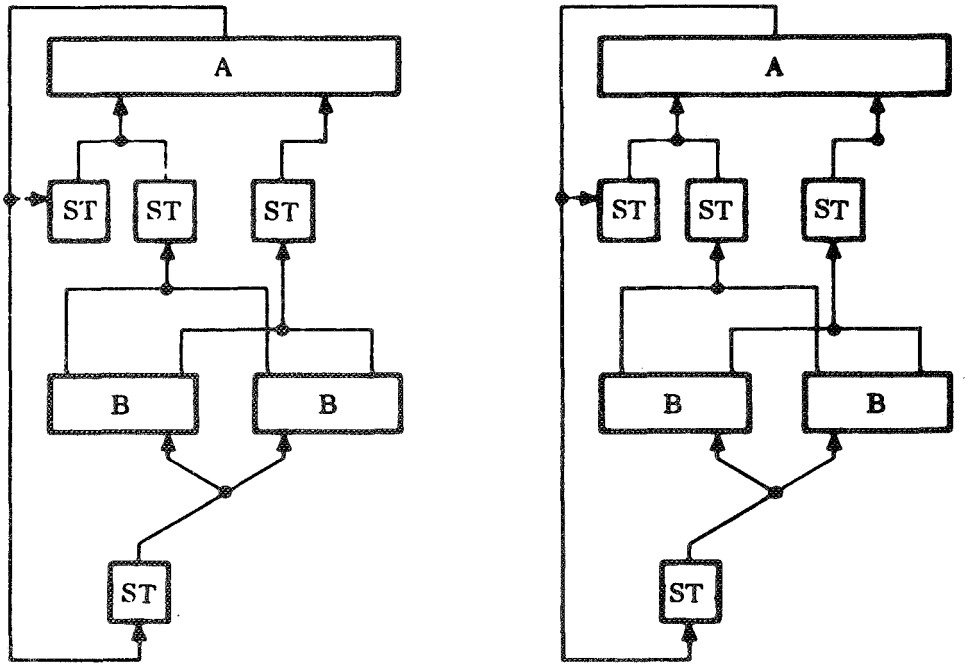


Figure 5. Basic Arithmetic and Control

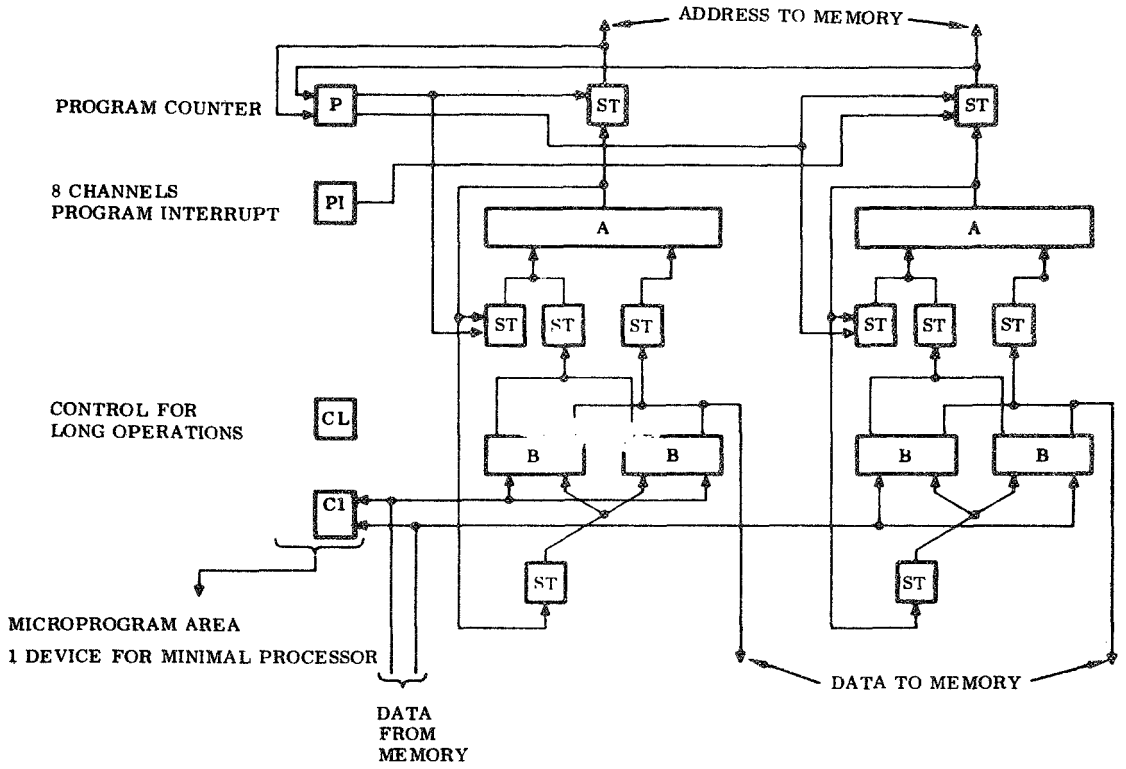


Figure 6. Complete Arithmetic and Control Center

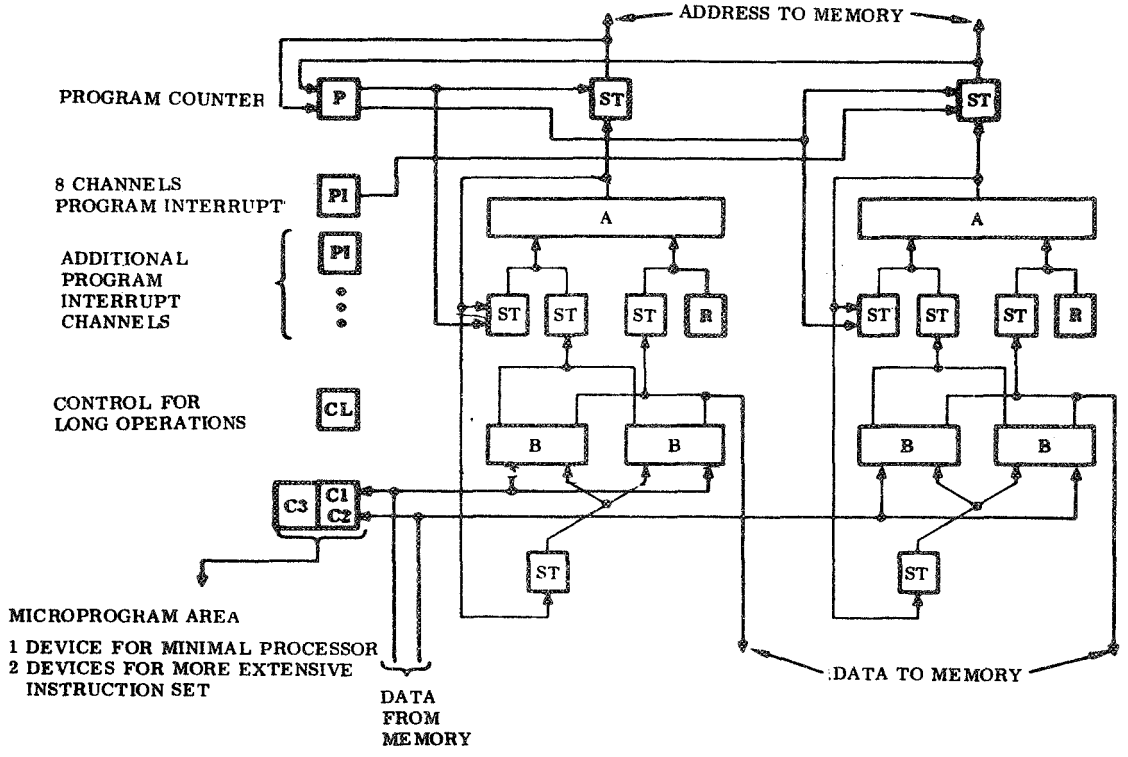


Figure 7. Extended Arithmetic and Control Section

The next set of figures will be used to show modularity with respect to word length. Figure 8 is a repeat of the basic 16 bit arithmetic center. Figure 9 shows the addition of an 8-bit slice to the arithmetic center giving a 24 bit arithmetic center while C1 has been replaced by C5 and C6 to provide for an extended instruction repertoire compatible with applications where 24 bit words are used. Again, additional program interrupt capability has been provided for by the addition of PI devices. Finally, Figure 10 shows a 32 bit arithmetic center with the only new devices required being C6 and C7 which implement the instruction set for this arithmetic and control center.

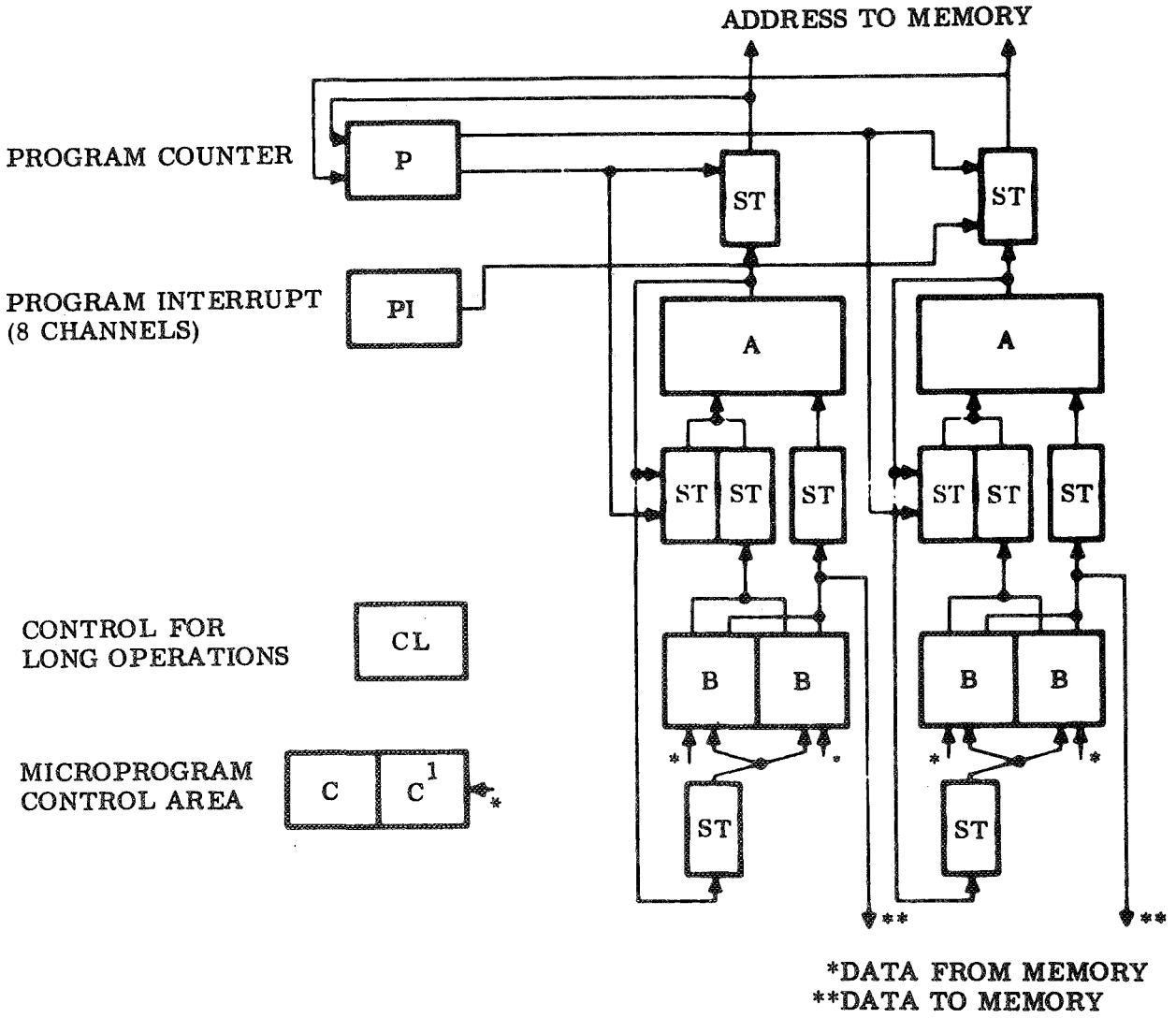


Figure 8. Basic 16 Bit A and C

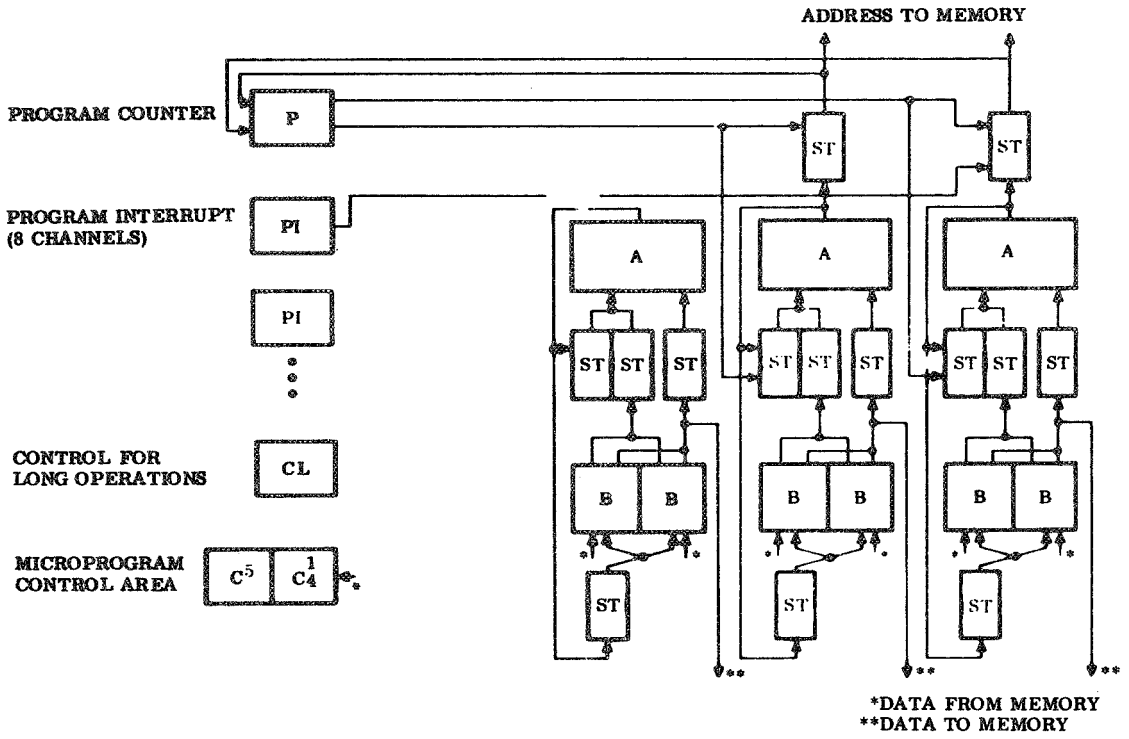


Figure 9. 24 Bit A and C

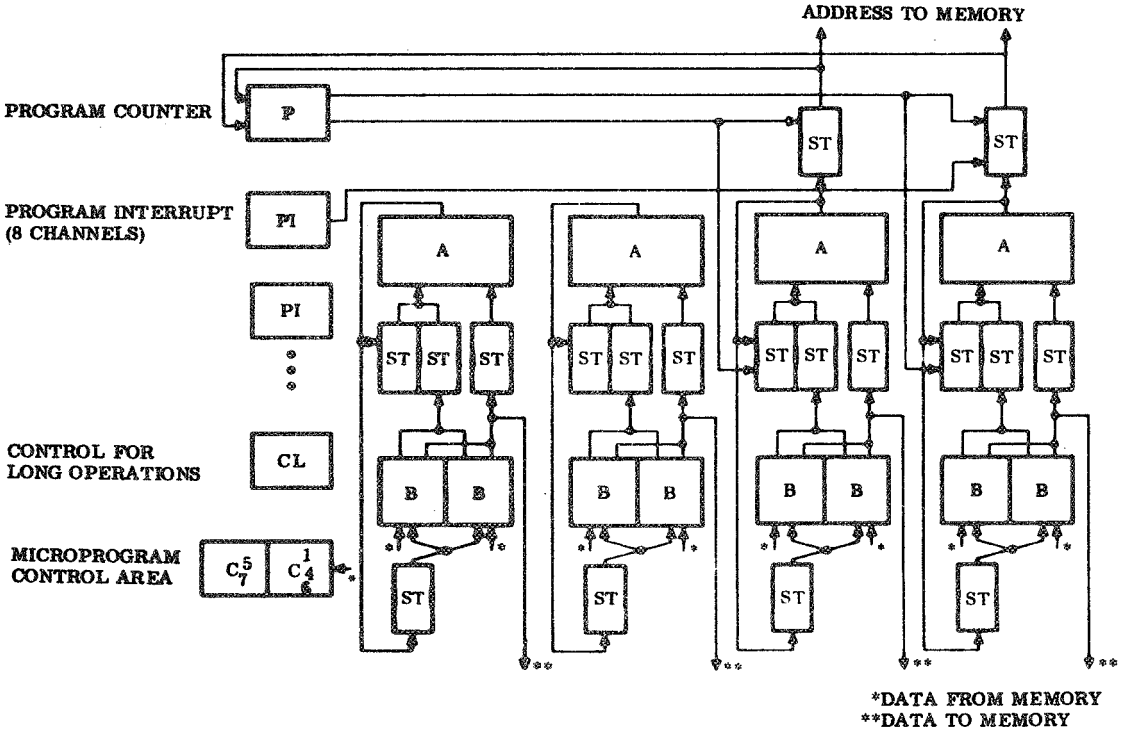


Figure 10. 32 Bit A and C

APPENDIX 6

1.0 INTRODUCTION AND SUMMARY

The purpose of this Appendix is to describe the results of a brief study of orbit determination using correlated horizon sensor measurements. The measurements consist of the angle between the line of sight from the spacecraft to the earth's horizon and a fixed line in inertial space such as the line to an appropriately chosen star. The plane defined by these two lines must be perpendicular to the earth's horizon at the point of intersection of this plane and the horizon. The difference between the observed value of this angle and the value computed based on the estimated spacecraft position provides information for updating the state (position and velocity) of the spacecraft.

It is assumed that the value of the observed angle is the true value of this angle plus a noise term which has a gaussian probability density function and an exponential autocorrelation function which is a function of the distance (as measured over the surface of the earth) between successive horizon points. Section 2.0 contains more details and descriptions of the error analysis and mechanization equations. Equations were formulated for both a linear covariance error analysis and a Monte Carlo simulation of the orbit determination process. An optimal estimation or Kalman filtering technique was used to correct the estimate of the spacecraft state.

The only error source modeled was the uncertainty in the apparent horizon. This uncertainty is on the order of 0.75-1.3 km (Reference 1) and corresponds to an angular error of approximately 0.02° when viewed from an altitude of 270 nm. Assuming accurate star trackers are used for attitude determination, the attitude errors should be on the order of 0.001-0.005° and thus negligible. It is assumed that horizon sensor instrument errors are small, and that sufficiently complex computational techniques are used so that numerical errors are also small.

The equations were incorporated into a computer program which was prepared to determine the navigation errors (position and velocity) as a function of several parameters. Section 3 discusses this program.

1.0 INTRODUCTION AND SUMMARY (Continued)

Section 4 presents data describing the effect several parameters have on the accuracy of the orbit determination process. A nominal set of environmental and mechanization parameters was chosen and variations made in these parameters to determine the resulting effect on navigational accuracy. The orbit assumed was circular with an altitude of 270 nm and an inclination of 55° although this latter parameter is superfluous since two body dynamics with an inverse square central force field were assumed (oblateness and higher order gravity terms as well as atmospheric drag were neglected). The parameters that were varied were the error in the apparent horizon, the correlation distance constant for the measurement errors, the number of and time between horizon measurements, the azimuth angles (measured in a locally level coordinate system) at which the measurements were made, and the initial position and velocity errors.

All of the results reported were obtained using the linearized covariance analysis portions of the program because of the reduction in required running time. A single Monte Carlo simulation was made with every covariance run for limited verification. Comparisons using up to 100 Monte Carlo simulations were made in one case to verify the results of the linearized analysis. Good agreement was obtained.

The data obtained shows a significant relationship between the horizon sensor field-of-view, and the azimuth angles at which measurements are made, and the navigation errors. Because of the linearized error analysis, the navigation errors are a linear function of the only error source considered, the horizon uncertainty. Varying the correlation distance constant has an interesting effect on the resulting navigation accuracy. Horizontal errors (cross track and down range) tend to decrease with increasing correlation distance constants. The opposite is true with vertical errors up to the point where the "bias" error caused by the correlation can be estimated and corrected. For correlation distance constants of less than 3000 nm, (actual horizon correlation distance constants are estimated to be on the order of 2500 nm, see reference 1) the error results, for the most part, are within 20% of those for a white noise measurement error (zero correlation distance).

Large initial position and velocity errors (up to 50 nm, 1000 fps initial uncertainties) have little if any effect on final navigation errors after a sufficient number (on the order of 20) measurements have been made. The number of and time between measurements was shown to have a significant effect on the final accuracy and is related to the correlation distance.

2.0 ERROR ANALYSIS AND MECHANIZATION EQUATIONS

A linearized covariance matrix approach was used for the error analysis with optimal estimation or Kalman filtering used to determine the correction or weighting coefficients. A brief description of the particular form of the equations used follows:

Let X_a and X_c be state vectors representing the actual state (3 position and 3 velocity components) and the computed state of the spacecraft respectively. The navigation errors are then

$$\bar{\mathcal{E}}_a = \bar{X}_a - \bar{X}_c \qquad (2.1)$$

Let y_o and y_c be the observed and computed values of the measurement (angle from star to horizon) respectively. Then

$$y_o = f(\bar{X}_a) + \eta \qquad (2.2)$$

$$y_c = f(\bar{X}_c) \qquad (2.3)$$

where η is the error in the measurement.

Based on the measurement, the computed state is corrected by the equation

$$\bar{X}_c^+ = \bar{X}_c^- + \hat{\mathcal{E}}_c \qquad (2.4)$$

where $\bar{X}_c^+$ = computed state after correction

$\bar{X}_c^-$ = computed state before correction

and $\hat{\mathcal{E}}_c$ = best estimate of correction based on measurement y_o and computed measurement y_c.

assume $\hat{\mathcal{E}}_c$ is of the form

$$\hat{\mathcal{E}}_c = B(y_o - y_c) \qquad (2.5)$$

where B is an appropriately dimensioned matrix (6 x 1 for this case) of weighting coefficients.

2.0 ERROR ANALYSIS AND MECHANIZATION EQUATIONS (Continued)

Substituting from equation 2.5 into 2.4 gives the equation for updating the computed state based on the weighting coefficients, B, and the observed and computed measurements:

$$\bar{X}_c^+ = \bar{X}_c^- + B(y_o - y_c) \qquad (2.6)$$

Using a Taylor series expansion of y_o about $\bar{X}_c$ and dropping all second order and higher terms,

$$y_o - y_c = f(\bar{X}_a) - f(\bar{X}_c) + \eta$$

$$= M(\bar{X}_a - \bar{X}_c) + \eta \qquad (2.7)$$

where $M = \left.\frac{\partial f(\bar{X})}{\partial \bar{X}}\right|_{\bar{X} = \bar{X}_c}$

The covariance matrix describing the estimation errors after the measurement can be computed as

$$C_\varepsilon^+ = E\left[\varepsilon_a^+ \varepsilon_a^{+T}\right] = E\left[(\bar{X}_a - \bar{X}_c^+)(\bar{X}_a - \bar{X}_c^+)^T\right]$$

$$= E\left[\left\{\bar{X}_a - (X_c^- + B(M(\bar{X}_a - \bar{X}_c^-) + \eta))\right\}\left\{\bar{X}_a - (X_c^- + B(M(X_a - X_c^-) + \eta))\right\}^T\right] \qquad (2.8)$$

If η is assumed to be zero mean and uncorrelated with any other variable, equation 2.8 can be reduced to

$$C_\varepsilon^+ = (I-BM)C_\varepsilon^- (I-B^T M^T) + B\, C_\eta\, B^T \qquad (2.9)$$

where $C_\eta = E\left[\eta\eta\right]$ is the covariance matrix of the measurement error.

Using Kalman optimal estimation and assuming ε_a and η are zero mean gaussian, the weighting coefficients can be determined as

$$B = C_\varepsilon^- M^T (MC_\varepsilon^- M^T + C_\eta)^{-1} \qquad (2.10)$$

Using this value of B, equation 2.9 can be reduced to

$$C_\varepsilon^+ = (I-BM)C_\varepsilon^- \qquad (2.11)$$

2.0 ERROR ANALYSIS AND MECHANIZATION EQUATIONS (Continued)

The dynamics governing spacecraft motion were assumed to be those associated with a two body inverse square central force field. The resulting differential equations can be integrated to propagate the spacecraft state and covariance matrix from one time to another. An analytic solution based on Kepler's equations as incorporated in a subroutine entitled TBODY was used; however, a state sensitivity matrix, $\Phi(t-t_o)$ was also obtained from this routine so that the covariance matrix $C_\varepsilon(t_1)$ at time t_1 can be determined from the covariance matrix $C_\varepsilon(t_o)$ at time t_o by the expression

$$C_\varepsilon(t_1) = \Phi(t_1-t_o)C_\varepsilon(t_o)\Phi(t_1-t_o)^T + Q_w \qquad (2.12)$$

where Q_w is the covariance matrix of noise added during propogation of the state.

The above equations assume the measurement error is white noise with zero mean. If instead the measurement error is correlated such that

$$\eta_{i+1} = A\eta_i + u_i$$

where η_k is the error at the kth measurement time, A is the correlation coefficient and u_i is white noise, some of the above equations need to be modified. Equation 2.3 should contain an estimate of the measurement error:

$$y_c = f(\bar{X}_c) + \hat{\eta} \qquad (2.14)$$

where $\hat{\eta}$ = best estimate of the measurement error. For zero mean white noise, $\hat{\eta}$ would be zero. Using (2.14), (2.7) becomes

$$y_o - y_c = M(\bar{X}_a - \bar{X}_c) + \eta - \hat{\eta} \qquad (2.15)$$

If the $\bar{X}_a$, $\bar{X}_c$, and M matrices are augmented as

$$\bar{X}_a^a = \begin{bmatrix} \bar{X}_a \\ \eta \end{bmatrix} \quad , \quad \bar{X}_c^a = \begin{bmatrix} \bar{X}_c \\ \hat{\eta} \end{bmatrix} \quad , \quad M^a = \begin{bmatrix} M & 1 \end{bmatrix}$$

then (2.14) becomes

$$y_o - y_c = M^a(\bar{X}_a^a - \bar{X}_c^a)$$

2.0 ERROR ANALYSIS AND MECHANIZATION EQUATIONS (Continued)

Equation 2.9 becomes

$$C_{\varepsilon}^{a+} = (I - B^{a}M^{a}) \; C_{\varepsilon}^{a-} \; (I - B^{aT}M^{aT}) \qquad (2.16)$$

where $C_{\varepsilon}^{a+} = E\left[\varepsilon_a^+ \, \varepsilon_a^{+T}\right] = E\left[(\bar{X}_a^a - \bar{X}_c^{a+})(\bar{X}_a^a - \bar{X}_c^{a+})^T\right]$

Equation 2.10 then becomes

$$B^a = C_{\varepsilon}^{a-} \; M^{aT} \; (M^a \; C_{\varepsilon}^{a-} \; M^{aT})^{-1}$$

and using this value of B^a, equations (2.6) and (2.16) become

$$\bar{X}_c^{a+} = \bar{X}_c^{a-} + B^a(y_o - Y_c) \qquad (2.18)$$

$$C_{\varepsilon}^{a+} = (I - B^aM^a) \; C_{\varepsilon}^{a-} \qquad (2.19)$$

Defining an augmented transition matrix

$$\Phi^a = \begin{bmatrix} \Phi & o \\ o & A \end{bmatrix}$$

and an augmented noise covariance matrix

$$Q_w^a = \begin{bmatrix} Q_w & o \\ o & Q_u \end{bmatrix}$$

where $Q_u = E\left[u \; u^T\right] = \sigma_u^2$,

then equation (2.12) becomes

$$C_{\varepsilon}^{a}(t_1) = \Phi^a \; C_{\varepsilon}^{a}(t_o) \; \Phi^{aT} + Q_w^a \qquad (2.20)$$

This augmented state approach (the measurement error becomes a component of the state vector) for handling correlated noise (see reference 2) results in a system where the measurement error is estimated at each measurement time, and where the white noise now enters the system only through the dynamics.

2.0 ERROR ANALYSIS AND MECHANIZATION EQUATIONS (Continued)

If η is a stationary random process, the variance of the additive white noise, σ_u^2, can be expressed as a function of the variance of η as follows: For a stationary process

$$E(\eta_{i+1}\,\eta_{i+1}) = E[\eta_i\,\eta_i] \triangleq \sigma_\eta^2$$

But $E[\eta_{i+1}\,\eta_{i+1}] = E[(A\eta_i + u_i)\,(A\eta_i + u_i)]$

$$= A^2\sigma_\eta^2 + \sigma_u^2$$

so that $$\sigma_u^2 = \sigma_\eta^2(1-A^2) \qquad (2.21)$$

The autocorrelation function of η as defined by (2.13) is an exponential function and can be derived as follows:

$$R_{\eta\eta}(\tau) = E[\eta_i\,\eta_{i+\tau}]$$

$$R_{\eta\eta}(0) = E[\eta_i\eta_i] = \sigma_\eta^2$$

$$R_{\eta\eta}(1) = E[\eta_i\,\eta_{i+1}] = E[\eta_i(A\eta_i + u_i)] = A\sigma_\eta^2$$

$$R_{\eta\eta}(2) = E[\eta_i\,\eta_{i+2}] = E[\eta_i(A\eta_{i+1} + u_{i+1})] = E[\eta_i(A(A\eta_i + u_i) + u_{i+1})]$$

$$= A^2\sigma_\eta^2$$

$$\vdots$$

$$R_{\eta\eta}(\tau) = A^{|\tau|}\sigma_\eta^2$$

Choose a constant D such that $A = e^{-\frac{1}{D}}$. Then

$$R_{\eta\eta}(\tau) = \sigma_\eta^2 e^{-|\tau|/D} \qquad (2.22)$$

Equations 2.21, 2.13, 2.2, 2.14, 2.17, 2.18, 2.19, and 2.20 are the essential mechanization equations. Figure 1 is a flow diagram of the computer program used, and these equations are shown in part of the blocks of the flow diagram. Some other equations and quantities are also shown and are discussed in the next section where the computer program is described.

3.0 COMPUTER PROGRAM

In order to determine the performance of the horizon sensor orbit determination mechanization, a computer program was prepared to perform the computations defined by the mechanization equations of the previous section for certain sets of system parameters. The computations for both a linearized covariance error analysis and a simulation of the onboard orbit determination process were programmed. Figure 1 is a flow diagram illustrating the basic program structure and computations. Table 1 defines the symbols used in figure 1.

Measurements are made with a fixed interval of time (TBM seconds) between measurements and at a sequence of azimuth angles (as measured in the locally level coordinate system) specified by input parameters. The input parameters ALLB, ALUB, ALINC, define this sequence. The first azimuth angle in a sequence is ALLB, the second ALLB + ALINC, the third ALLB + (2) (ALINC), etc., until the angle ALUB is exceeded. When this happens, the sequence is repeated. Thus, specifying the azimuth angles such that the velocity vector of the spacecraft is at an azimuth angle of zero degrees, with a clockwise orientation, a sequence of measurements to be made at angles of 30°, 60°, 90°, 120°, would be specified by ALLB = 30°, ALUB = 120°, ALINC = 30°.

The spacecraft is computed to be in a circular orbit as defined by input parameters specifying orbital altitude, inclination, and initial longitude and latitude.

The correlation coefficient, as determined by the third block in figure 1, is a function of the distance between the points on the horizon at which measurements are made (called the correlation distance). Because of the measurement sequence and the orbital motion, this correlation distance changes from measurement to measurement and has a sequence of values correlated with the sequence of measurement azimuth angles. This results in the need to compute a value of the variance of the additive white noise at each measurement time to be used as an input to the random number generator. These computations could be avoided if the measurements are correlated with time, but a distance correlation is more representative of horizon phenomenon. The other equations of figure 1 were discussed in the previous section.

Table 2 lists the required program input parameters. A namelist format is used. Output consists essentially of various CRT plots and printed tabulations of errors in the computed spacecraft state (both RMS from the covariance matrix and actual for a Monte Carlo simulation with a given random number sequence) as a function of the measurements made. Some other parameters can currently be printed out during a simulation run under control of certain input parameters.

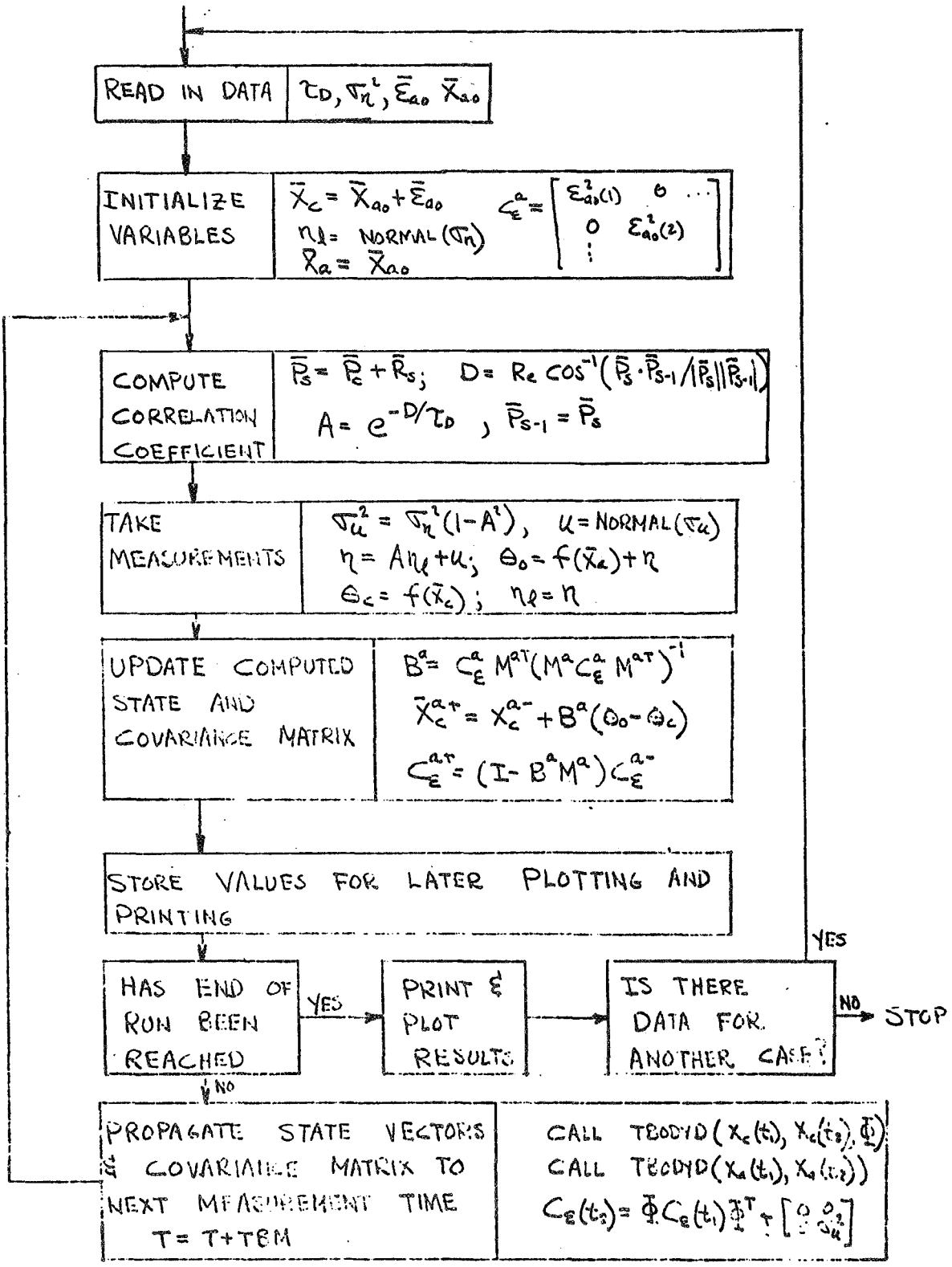


FIGURE 1: COMPUTER FLOW DIAGRAM

TABLE 1

SYMBOL DEFINITION FOR FIGURE 1

τ_D	- Distance constant for exponential correlation function
σ_η^2	- Variance of measurement error
$\bar{\varepsilon}_{ao}$	- A six vector giving initial uncertainties in spacecraft state
$\bar{X}_{ao}$	- A six vector giving the initial state of the spacecraft
$\bar{X}_c$	- The computed state of the spacecraft including the estimate of the measurement error
$\bar{X}_a$	- The actual state of the spacecraft
NORMAL (σ)	- A subroutine which generates a random number with a zero mean, gaussian probability density function, and standard deviation σ.
η_ℓ	- The "last" (i-1) random measurement error
C_ε^a	- The covariance matrix of $\bar{X}_c - \bar{X}_a$
$\bar{P}_s$	- The vector from the center of the earth to the point on the horizon where the measurement is made
$\bar{P}_{s-1}$	- The value of $\bar{P}_s$ for the previous measurement
$\bar{P}_c$	- The computed position vector (first three components of $\bar{X}_c$)
$\bar{R}_s$	- The vector from the spacecraft to the point on the horizon where the measurement is made
R_e	- Radius of earth
A	- Correlation coefficient
D	- The distance measured over the surface of the earth between successive points on the horizon where measurements are made

TABLE 1 (Continued)

SYMBOL DEFINITION FOR FIGURE 1

σ_u^2	- Variance of white noise added to correlated measurement error
u	- White noise error added to correlated measurement error
η	- Measurement error
θ_o	- Observed value of measurement
θ_c	- Computed value of measurement
M^{aT}	- Augmented matrix relating measurement error to state errors.
I	- Identity matrix
Φ	- Transition matrix relating state errors at time t_1 to time t_2.
T	- Time of current measurement
TBM	- Time between measurements

TABLE 2

PROGRAM INPUT PARAMETERS

SYMBOL	UNITS	NOMINAL VALUES	DESCRIPTION
TBM	Minutes	5	Time between measurements
TEND	Minutes	500	Time of last measurement
SIGP	nm	10	Standard deviation of initial position error
SIGV	fps	50	Standard deviation of initial velocity error
SIGE	degrees	.02	Standard deviation of measurement error
ALT	nm	270	Altitude of orbit
ALONG	degrees	0	Initial longitude of trajectory
ALAT	degrees	0	Initial latitude of trajectory
AINC	degrees	55	Inclination of orbit
CDTC	nm	2500	Correlation distance constant
ALLB	degrees	0	Smallest azimuth angle for measurements
ALUB	degrees	360	Largest azimuth angle for measurements
ALINC	degrees	90	Amount azimuth angle is incremented for each measurement
NMCR	-	1	Number of Monte Carlo runs to be made. If < 0, no runs are to be made.
NPL	-		Plot control parameter. No CRT plots if < 0.
NPR, NPIMC, NPMNM	-		Print control parameters, No print out until end of run if < 0.

3.0 COMPUTER PROGRAM (Continued)

The program, when used for more than one Monte Carlo run, has a slightly different structure from that shown in figure 1. During the first run, certain computed quantities which are independent of the random number sequence (such as X_a, B^a) are stored for each measurement. During subsequent "Monte Carlo" runs, these numbers are retrieved from storage rather than recomputed in order to save computer execution time.

4.0 RESULTS

To determine the effect of variations in certain parameters on spacecraft navigation accuracy, the computer program described in the previous section was run for various parameter values. Repeated Monte Carlo runs were made for only two cases and then only to verify the results as given by the covariance analysis. Figures 2 and 3 show a comparison of results for these two types of analysis. In figure 2, the three components of position error (expressed in locally level coordinates) are shown for a Monte Carlo simulation of 100 runs (dashed lines) and for a covariance analysis (solid lines) as a function of time. In all the results that follow, the simulation run starts at zero time with the first measurement made TBM minutes later, and with subsequent measurements made every TBM (time between measurements) minutes. The errors shown for a given time are after the correction has been applied based on the measurement made at that time. The other parameter values for the curves of figures 2 and 3 are the nominal set shown in table 2, with the exception of SIGE = 0.05. As can be seen, the results for the two analysis types are very close, the maximum difference being less than 20%. Figure 3 shows a comparison of results for different numbers of Monte Carlo runs. As expected, the larger the number of runs, the better the agreement between the covariance and Monte Carlo results.

Figures 2 and 3 show only position errors. Velocity computations are based on "position" measurements (no rates are measured) and velocity errors, hence, are similar in their behavior to position errors. Therefore, in this report, plots of velocity errors are not given, although some tabulated velocity errors are shown. Also, where all components of position errors (downrange, crossrange, and vertical) are similar in behavior, results for only one, the downrange component (which is dominant) are shown.

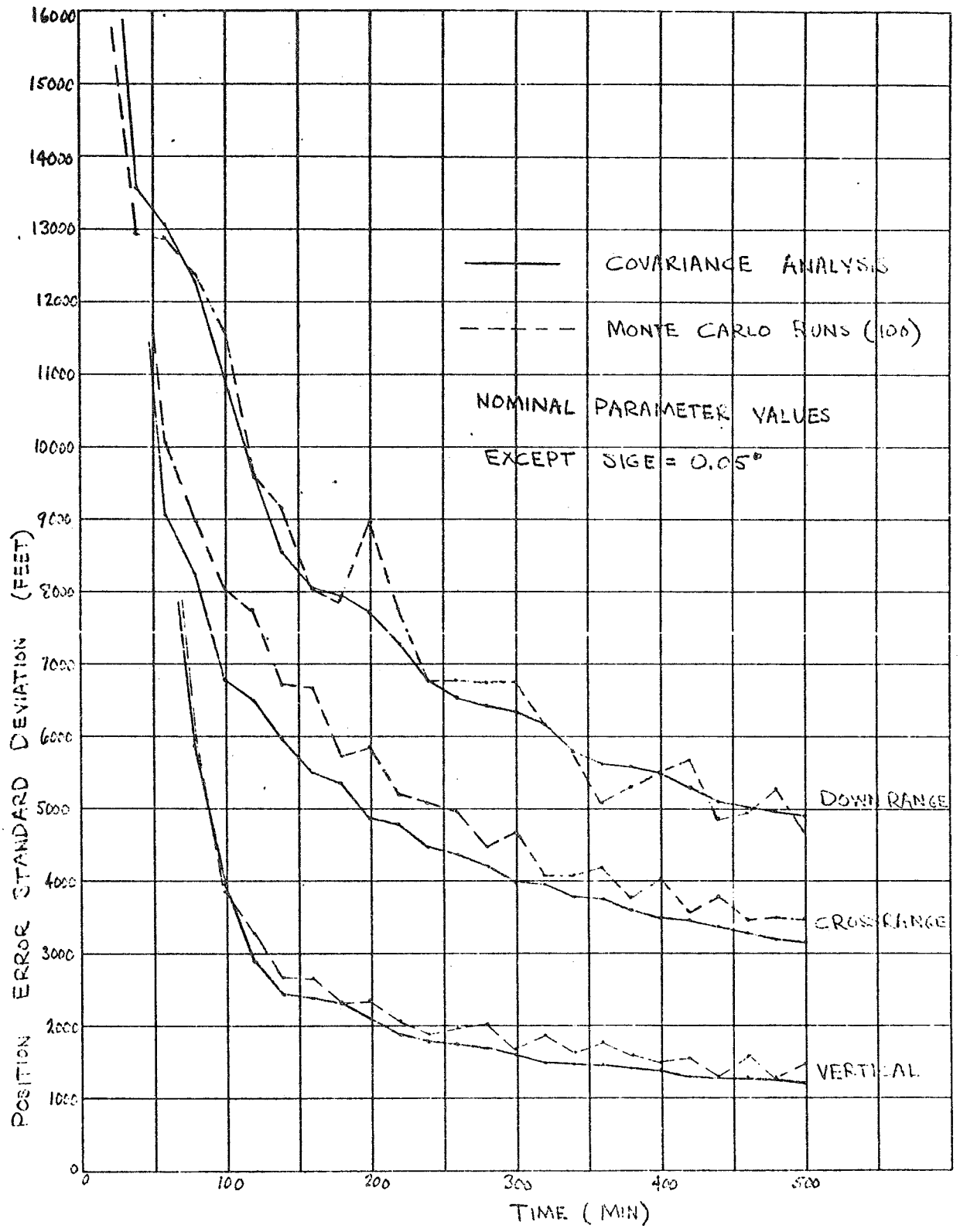


FIGURE 2: POSITION ERROR STANDARD DEVIATION FROM COVARIANCE ANALYSIS AND 100 MONTE CARLO RUNS

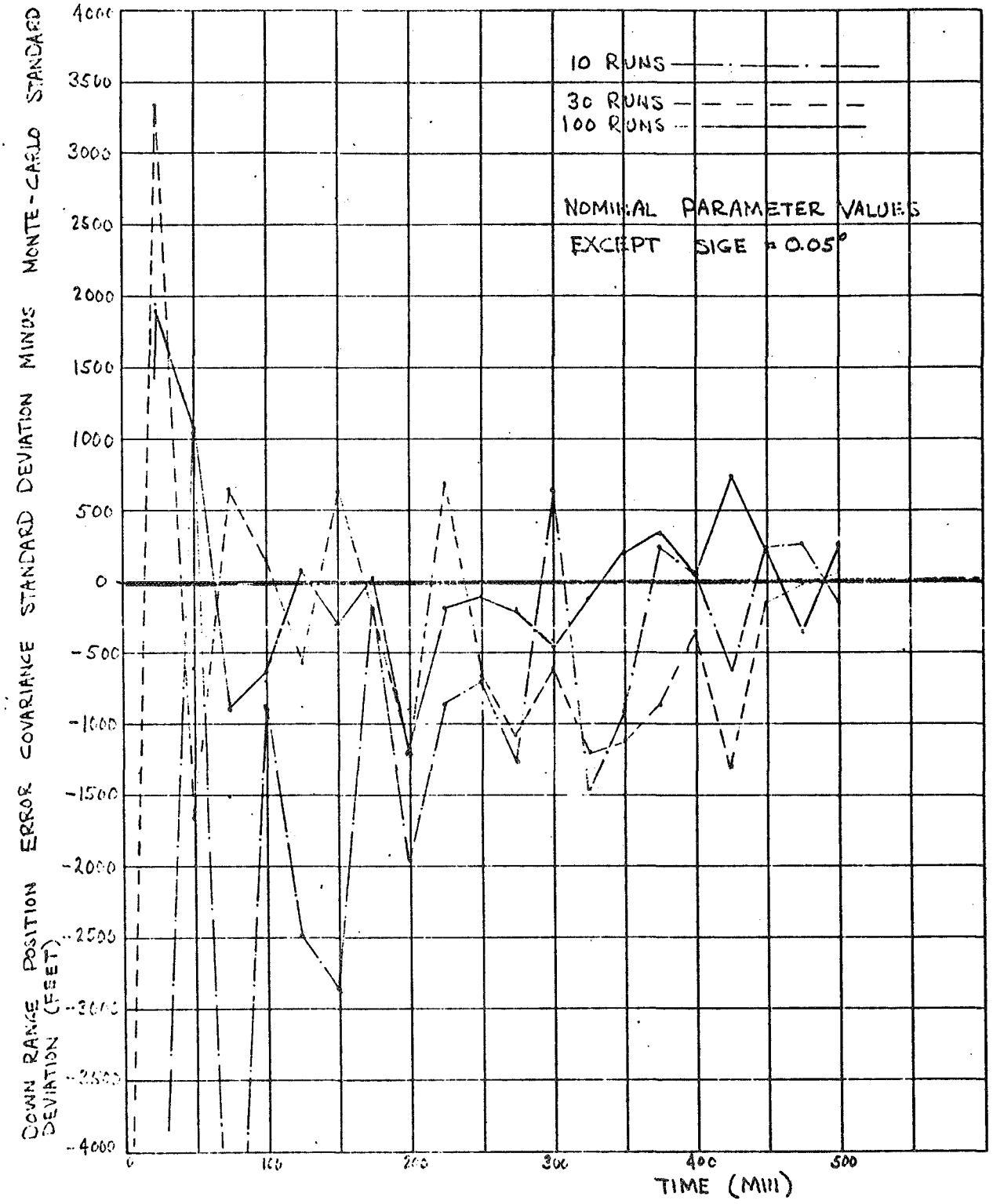


FIGURE 3: COMPARISON OF COVARIANCE ANALYSIS RESULTS & MONTE CARLO RESULTS

4.0 RESULTS (Continued)

Error results were obtained for variations of ten different parameters. These parameters are (symbol shown in parenthesis):

1. Standard deviation of horizon measurement error (SIGE)
2. Azimuth field-of-view magnitude (ALUB-ALLB)
3. Azimuth field-of-view location (ALLB)
4. Change of azimuth angle per measurement (ALINC)
5. Correlation distance (CDTC)
6. Time between measurements (TBM)
7. Time of last measurement (TEND)
8. Standard deviation of initial position error (SIGP)
9. Standard deviation of initial velocity error (SIGV)
10. Number of Monte Carlo runs (NMCR)

The spacecraft orbit was not varied but was assumed to be circular at an altitude of 270 nm with an inclination of 55, although, changes in this inclination as well as initial longitude and latitude for a circular orbit will have no effect because of the two body, inverse square central force field gravity model used.

The number of cases that result from all combinations of various parameter values for the above 10 parameters can be very large (10^n, where n is number of values each parameter assumes). To limit the number of possible cases and to provide understanding of the effect of variation of a given parameter, a nominal set of parameter values was chosen and variations made in individual parameters about the nominal value. Where the effect of a second or third parameter appeared to be important, corresponding variations were made in that parameter also. The nominal parameter values chosen are listed in table 2. The following sections discuss the results of individual parameter variations from this nominal. Unless otherwise stated, the parameter values for the data presented in the curves and tables of this section are those listed as nominal in table 2.

The effect of variation in number of Monte Carlo runs is shown in figure 3. Also, the good comparison between covariance analysis and Monte Carlo simulation shown in figure 2, justifies use of the covariance analysis upon which the following results are based.

4.0 RESULTS (Continued)

4.1 Variations of Measurement Error (SIGE) - Table 3 tabulates data relating state errors to measurement errors and the number of measurements (defined by the measurement time, T, and TBM. Thus, the number of measurements = $T/_{TBM}$). Curves relating downrange position error to these parameters are shown in figure 4, which shows the linear relationship between state and measurement errors.

4.2 Variations in Correlation Distance - Figures 5 through 9 indicate results for variations of correlation distance. The intent of figure 5 is to indicate the effect horizon measurement errors will have on corrections made in the spacecraft location. Referring to the figure, the solid lines show actual lines-of-sight to the horizon at two different measurement points. ε_1, ε_2 and ε_3 indicate possible errors in these measurements where the corresponding lines-of-sight are shown by the dashed lines. The distance h_1, h_2, and h_3 correspond to horizontal "corrections" that need to be made in the spacecraft location for errors ε_1, ε_2 and ε_3 respectively, to make the measured horizon lines-of-sight correspond to actual lines from the spacecraft to the horizon (indicated by broken lines). The distances V_1, V_2, and V_3 are corresponding vertical "corrections".

A pair of measurements that are correlated will appear as the pair $(\varepsilon_1, \varepsilon_2)$ rather than the pair $(\varepsilon_1, \varepsilon_3)$ since both errors ε_1 and ε_2 give a smaller observed angle than the actual angle. Uncorrelated errors will regularly appear as the pair $(\varepsilon_1, \varepsilon_3)$ (the observed angle is both larger and smaller than the actual angle). Now assume that a pair of horizon measurements have been made 180° apart in azimuth and the resulting apparent horizontal and vertical "corrections" averaged to give a new "correction" for the spacecraft location. A correlated pair such as $(\varepsilon_1, \varepsilon_2)$ will tend to give a zero horizontal correction but a non-zero vertical correction. The reverse is true for an uncorrelated pair of measurements - vertical errors will tend to average to zero while a non-zero horizontal error will appear.

Figure 7 and 8 show crossrange and vertical errors as a function of time and correlation distance. The results of figure 7 are as expected based on the above discussion - any correlation results in smaller crossrange errors. Figure 8 shows larger vertical errors for correlated measurement errors for the

NUMBER OF MEASURE-MENTS	σ_ε MEASUREMENT STANDARD DEVIATION (DEG)	RMS POSITION ERROR (FEET)			RMS VELOCITY ERROR (FPS)		
		DOWN RANGE	CROSS RANGE	VERTICAL	DOWN RANGE	CROSS RANGE	VERTICAL
20	0.01	2214	1368	819	0.8	1.6	2.3
	0.02	4401	2720	1594	1.5	3.2	4.5
	0.03	6612	4078	2411	2.3	4.8	6.7
	0.05	10966	6750	3958	3.7	7.9	11.2
	0.10	21474	13391	7478	7.1	15.2	21.6
	0.20	41552	24652	12801	12.5	27.0	42.1
40	0.01	1557	973	425	0.4	1.1	1.6
	0.02	3100	1939	842	0.9	2.2	3.1
	0.03	4653	2907	1270	1.3	3.3	4.7
	0.05	7758	4824	2093	2.2	5.6	7.8
	0.10	15527	9595	4141	4.3	11.0	15.7
	0.20	30080	18164	7590	8.1	20.7	30.3
60	0.01	1271	802	320	0.3	0.9	1.3
	0.02	2536	1600	635	0.7	1.8	2.6
	0.03	3818	2399	957	1.0	2.7	3.9
	0.05	6362	3987	1592	1.7	4.5	6.4
	0.10	12669	7920	3150	3.4	9.0	12.8
	0.20	24357	15144	5904	6.5	17.3	24.6
80	0.01	1101	700	268	0.3	0.8	1.1
	0.02	2197	1398	533	0.6	1.6	2.2
	0.03	3321	2097	802	0.9	2.3	3.4
	0.05	5479	3488	1308	1.4	3.8	5.6
	0.10	10923	6925	2654	2.9	7.7	11.0
	0.20	21147	13352	5091	5.6	15.1	21.3
100	0.01	985	629	235	0.3	0.7	1.0
	0.02	1963	1258	469	0.5	1.4	2.0
	0.03	2967	1886	705	0.8	2.1	3.0
	0.05	4904	3140	1178	1.3	3.4	4.9
	0.10	9824	6238	2347	2.6	6.9	9.9
	0.20	18750	12130	4561	5.1	13.5	18.9

TABLE 3: POSITION & VELOCITY ERRORS AS A FUNCTION OF MEASUREMENT ERRORS & NUMBER OF MEASUREMENTS (NOMINAL PARAMETER VALUES)

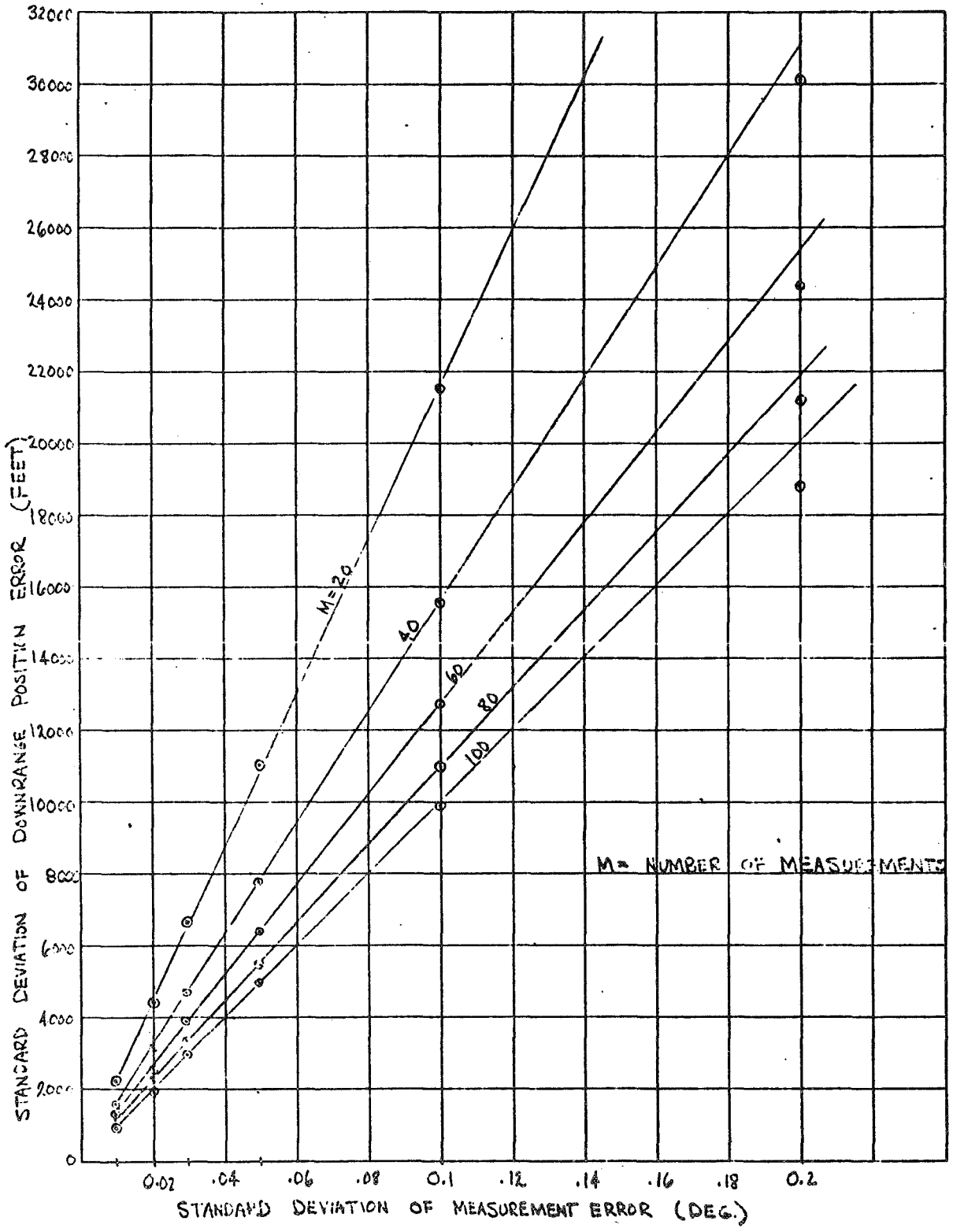
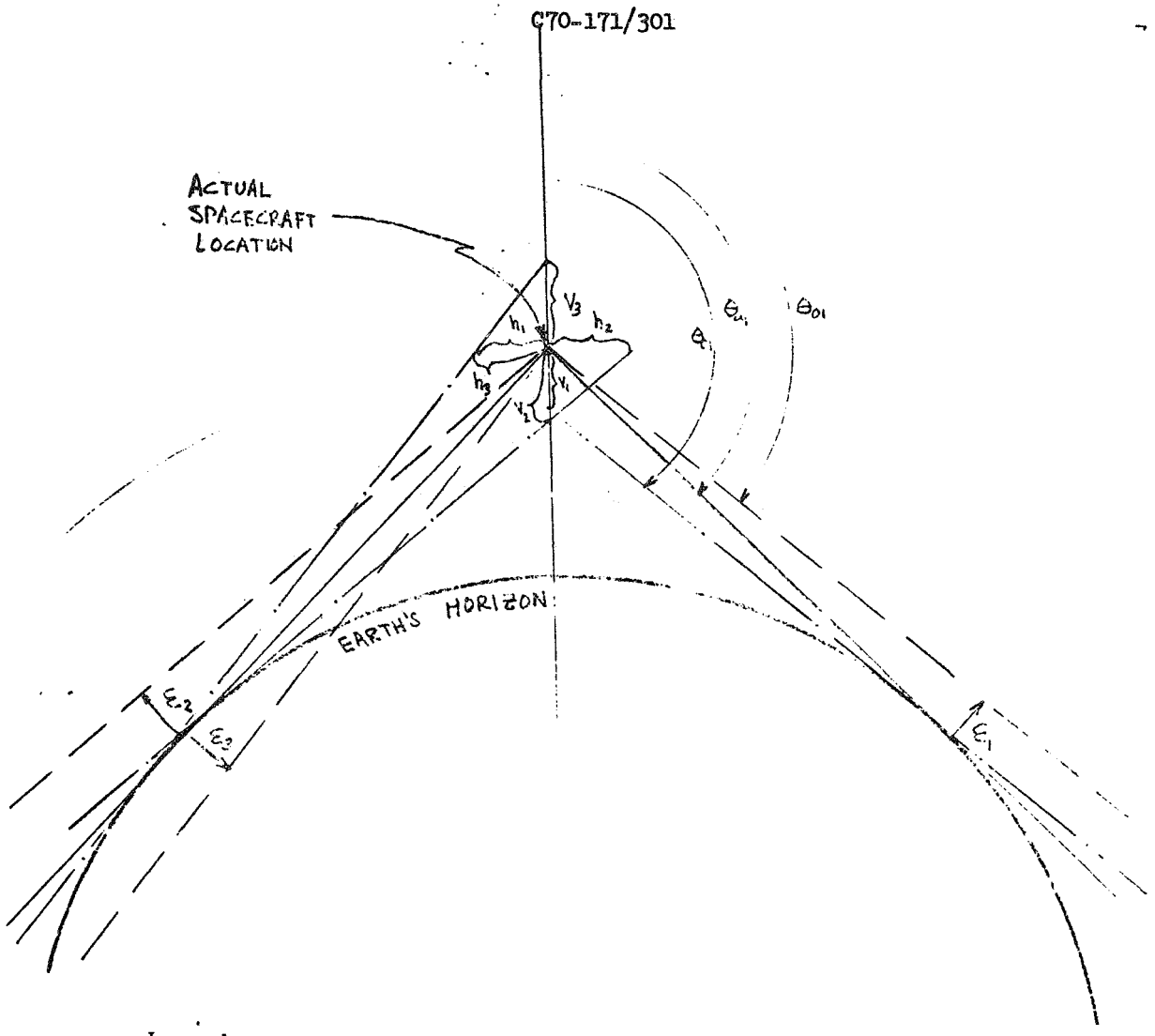


FIGURE 4: DOWNRANGE POSITION ERROR AS A FUNCTION OF MEASUREMENT ERRORS & NUMBER OF MEASUREMENTS



Legend

E_1, E_2, E_3:	Horizon Measurement Errors
θ_{ar}:	Actual Angle from Reference to Horizon
θ_{01}:	Observed Angle from Reference to Horizon
h_1, h_2, h_3:	Apparent Horizontal Spacecraft Location Corrections Based on Measurements 1, 2, and 3
V_1, V_2, V_3:	Apparent Vertical Spacecraft Location Corrections Based on Measurements 1, 2, and 3
	Actual line-of-sight from spacecraft to horizon
	Measured line-of-sight from spacecraft to horizon
	Line-of-sight from "corrected" spacecraft location to horizon

Figure 5: Effect of Horizon Measurement Errors on "Correction" to Spacecraft Location

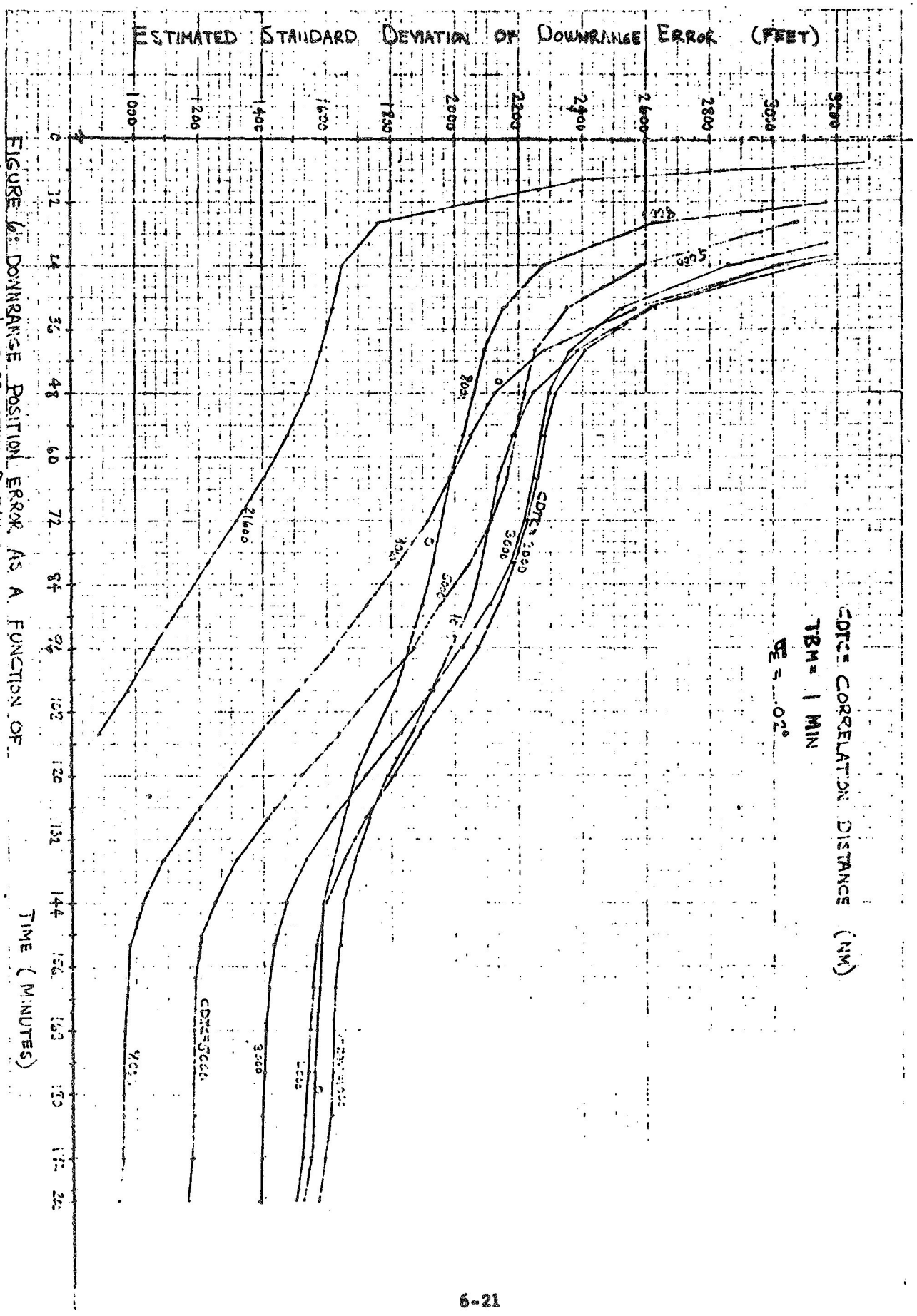


FIGURE 6: DOWNRANGE POSITION ERROR, AS A FUNCTION OF TIME & CORRELATION DISTANCE

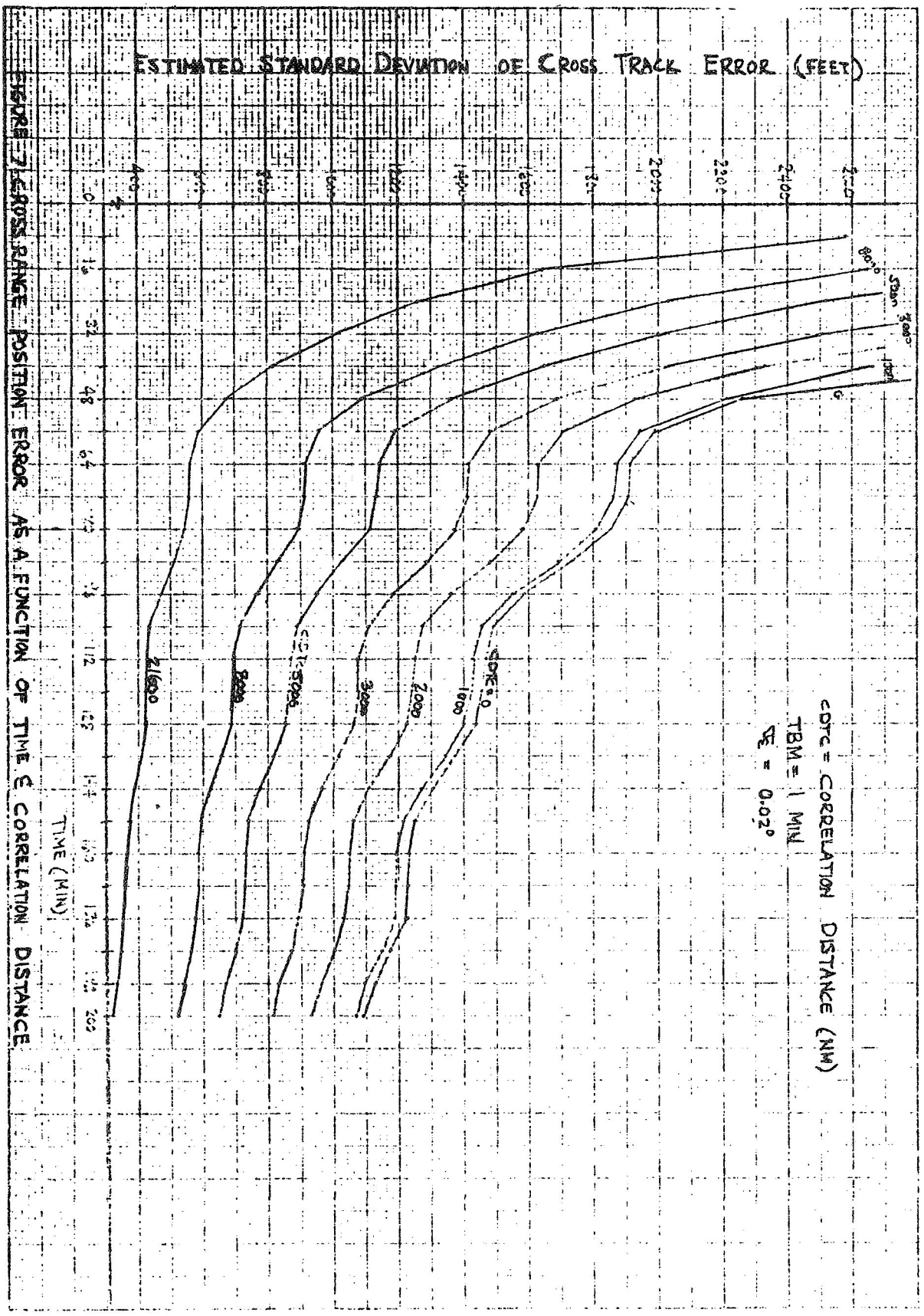


FIGURE 7 CROSS RANGE POSITION ERROR AS A FUNCTION OF TIME & CORRELATION DISTANCE

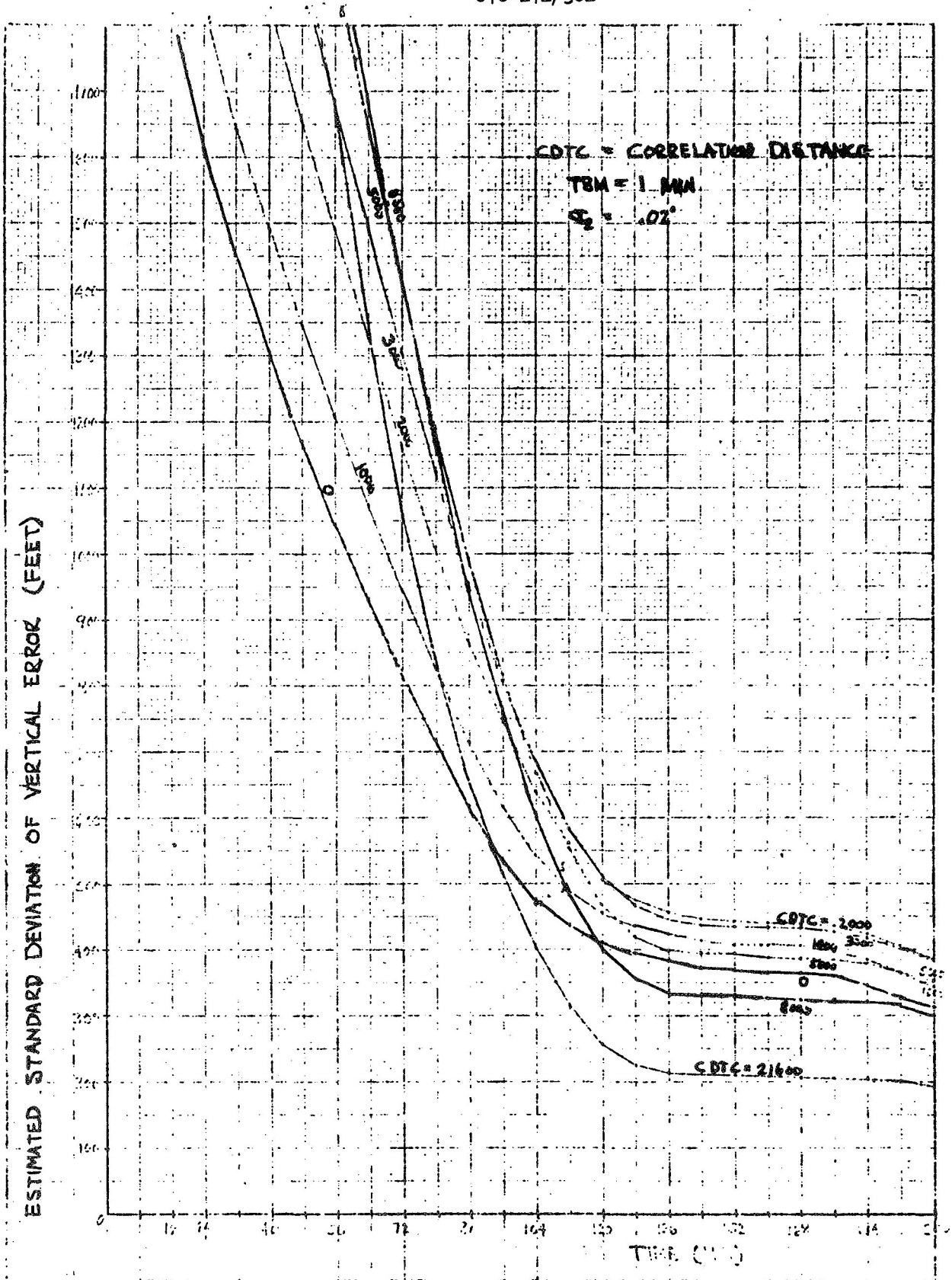


FIGURE 5: VERTICAL POSITION ERROR AS A FUNCTION OF TIME & CORRELATION DISTANCE

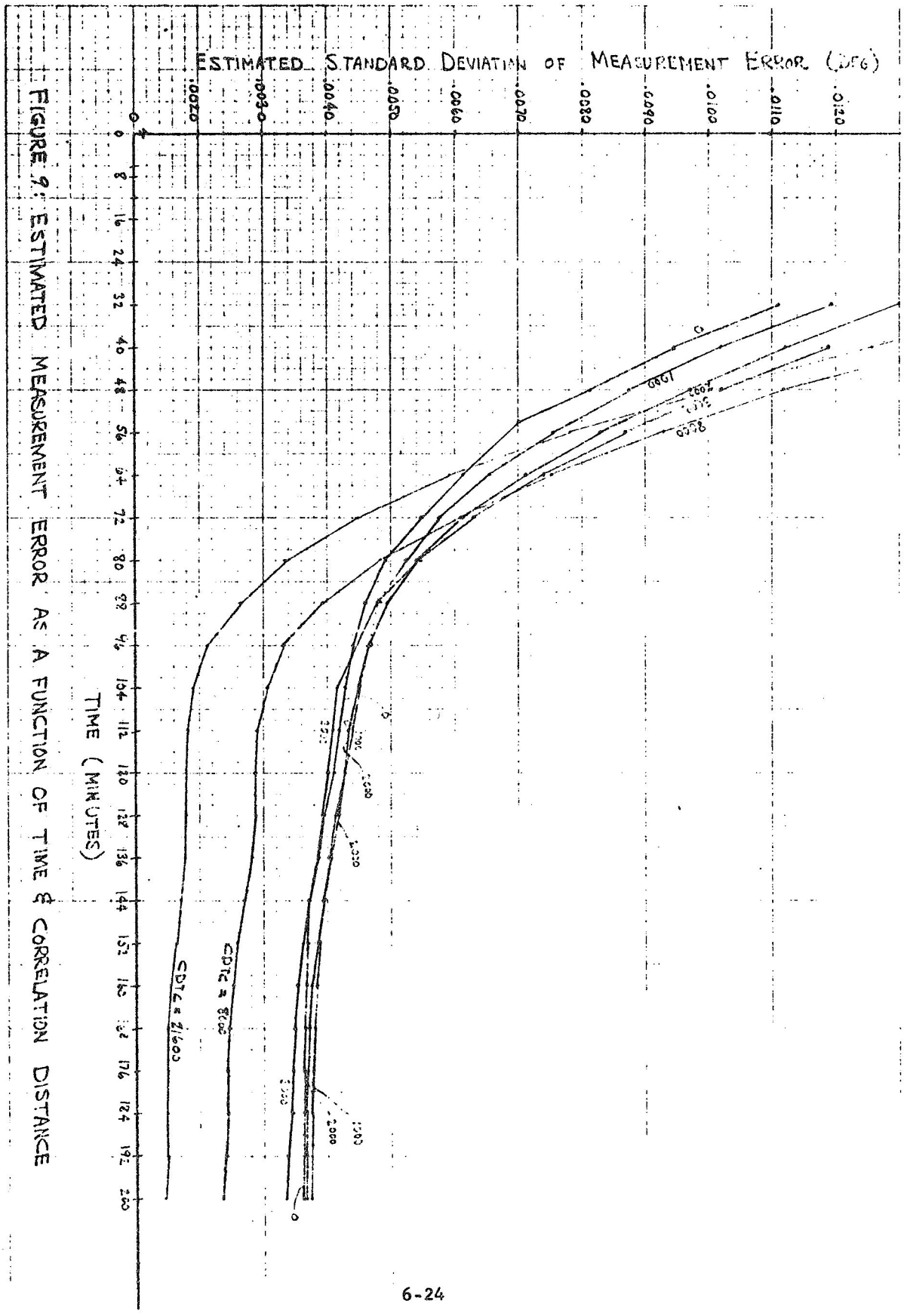


FIGURE 9: ESTIMATED MEASUREMENT ERROR AS A FUNCTION OF TIME & CORRELATION DISTANCE

4.0 RESULTS (Continued)

4.2 shorter correlation distance. Another effect is exhibited by figure 8, wherein the errors decrease for the long correlation distances after many measurements have been made. The reason for this is that the correlation between measurements is one of the variables in the state estimation process and after sufficient measurements have been made and for a large enough correlation, the "bias" exhibited by the correlation can be estimated and appropriate corrections made. Figure 9 shows the error in estimating the measurement error as a function of time (essentially the number of measurements) and the correlation distance. As expected, for the larger correlation distances (large correlation between successive measurements) the error in the estimate of the measurement error decreases after several measurements have been made.

Figure 6 shows downrange position error as a function of time and correlation distance. As expected, for the longer correlation distance (> 8000 nm), the errors decrease with increasing time and correlation distance. For short correlation distances (1000 nm), the errors are larger than for the white noise case (zero correlation distance). There is probably a strong interaction of several parameters which causes this phenomena. These effects have not been fully investigated due to time and funding constraints. One factor to be considered is the strong coupling between the downrange and vertical position and velocity errors.

4.3 Variations in Number of Measurements and Time Between Measurements - The effect of variations in the number of measurements and time between measurements is shown in figure 10 and tables 4 and 5. Earlier figures have shown errors as a function of time which, for a given time between measurements, corresponds to the number of measurements made. There is a significant difference in the results depending on the number of measurements made, with errors decreasing monotonically with increasing number of measurements. Referring to table 5, the time between measurements (TBM) for a given number of measurements, while significant, doesn't seem to have too large an effect on the position and velocity errors. There does appear to be for the data of table 5, an optimum time between measurements (as determined from rss position errors) of about five minutes. TBM is directly related to the correlation between

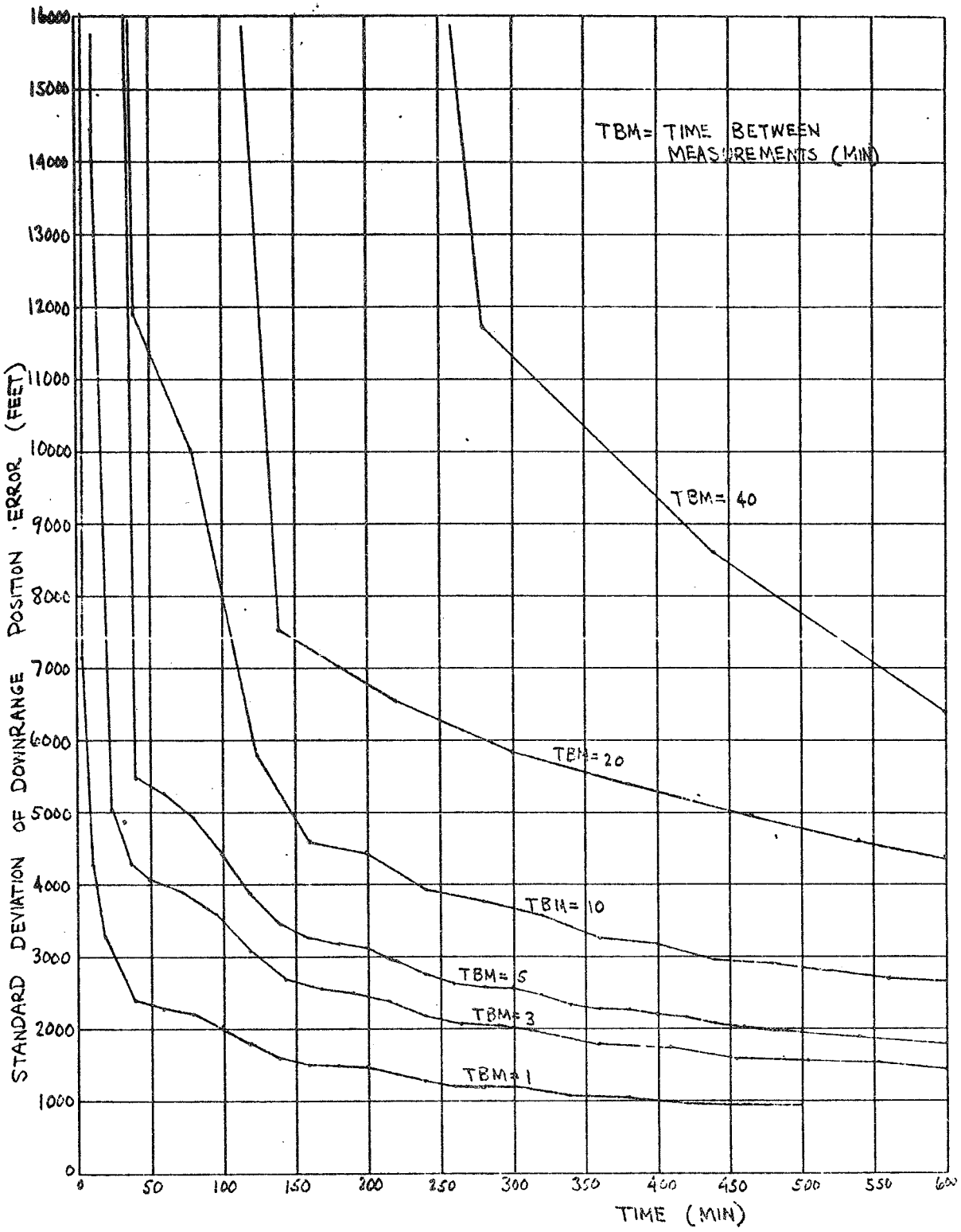


FIGURE 10: DOWNRANGE POSITION ERROR AS A FUNCTION OF NUMBER OF MEASUREMENTS & TIME BETWEEN MEASUREMENTS

CORRELATION DISTANCE (NM)	NUMBER OF MEASURE-MENTS	RMS POSITION ERROR*(FEET)			RMS VELOCITY ERROR*(FPS)		
		DOWN RANGE	CROSS RANGE	VERTICAL	DOWN RANGE	CROSS RANGE	VERTICAL
2500	600	910	560	220	0.2	0.6	0.9
	200	1410	880	340	0.4	1.0	1.4
	120	1790	1150	430	0.5	1.3	1.8
	60	2620	1820	600	0.7	1.9	2.7
	30	4390	2930	750	0.8	3.0	4.5
	15	6370	3740	1090	1.2	4.7	6.8
216000	600	115	65	33	0.0	0.1	0.1
	200	180	100	51	0.1	0.1	0.2
	120	230	140	65	0.1	0.2	0.2
	60	350	250	100	0.1	0.3	0.3
	30	810	515	140	0.2	0.5	0.8
	15	1240	850	195	0.2	1.0	1.3

*TEND (Time of last measurement) = 600 min.

TABLE 4: POSITION & VELOCITY ERRORS AS A FUNCTION OF NUMBER OF MEASUREMENTS AND CORRELATION DISTANCE

CORRELATION DISTANCE (NM)	TIME BETWEEN MEASURE-MENTS (MIN)	RMS POSITION ERROR*(FEET)			RMS VELOCITY ERROR*(FPS)		
		DOWN RANGE	CROSS RANGE	VERTICAL	DOWN RANGE	CROSS RANGE	VERTICAL
2500	1	1440	870	390	0.4	1.0	1.4
	3	1410	880	340	0.4	1.0	1.4
	5	1380	880	330	0.4	1.0	1.4
	10	1440	980	320	0.4	1.1	1.5
	20	1580	1100	280	0.3	1.2	1.7
	40	1620	1110	270	0.3	1.2	1.7
216000	1	190	100	60	0.1	0.1	0.2
	3	180	100	50	0.1	0.1	0.2
	5	170	110	50	0.1	0.1	0.2
	10	190	140	50	0.1	0.1	0.2
	20	240	190	50	0.1	0.2	0.3
	40	230	220	50	0.1	0.2	0.2

*After 200 measurements

TABLE 5: POSITION & VELOCITY ERRORS AS A FUNCTION OF TIME BETWEEN MEASUREMENTS AND CORRELATION DISTANCE

4.0 RESULTS (Continued)

4.3 measurements and as TBM increases, the correlation decreases which should, in general, degrade performance as discussed in the previous section. This is evident for the TBM values of 20 and 40 as shown in table 5.

4.4 Variation in Azimuth Measurement Angles - Table 6 tabulates position and velocity errors after 500 minutes (100 measurements) for various combinations of ALUB, ALLB, and ALINC, which define the azimuth angle field-of-view (FOV) over which measurements are taken and the azimuth angle between these measurements. The results are interesting in that they indicate a significant change in errors as a function of these parameters. Cases 6 and 13 have unreasonably large errors because essentially no cross track measurements are made.

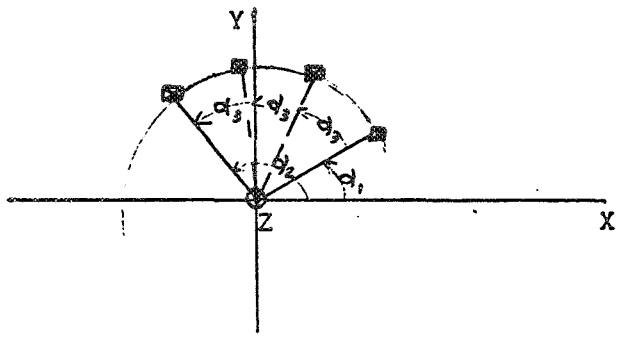
The smallest rss position error (case 4) occurs, interestingly enough, not with the largest FOV but for only a 180° FOV with measurements made 90° apart. Reducing the FOV to only 90° (cases 8 and 9) increases the rss position error only some 400 feet.

Ideally, one would like to make all measurements using the set of different azimuth angles, at the same time. Such sets of measurements should permit the best estimate of "biases" due to correlated errors and reduce the effect of velocity errors propagating into position errors. One comes closest to this by making ALINC large so that the entire FOV is covered quickly but not so large so that important components are not measured. Thus, case 3 is better than cases 1 or 2 in that the 90° between azimuth angles permits the entire FOV to be covered in four measurements as compared to 8 and 36 for cases 1 and 2 respectively. In case 6, the 180° FOV is covered in first two measurements made 180° apart, but no cross track measurement is made and hence, this component of the position error is very large - limited essentially by its initial value. The downrange position error for case 6 is smaller than for any other case however.

4.5 Variations in Initial Position and Velocity Errors - Figure 11 shows the downrange position error as a function of time for several different initial position and velocity uncertainties. Other components of position and velocity exhibited similar behavior. As can be seen from figure 11, after the first 20 measurements (100 minutes), the errors are essentially the same regardless of the initial uncertainties for values up to those shown.

These results are from a covariance analysis. A single Monte Carlo run was made for each case, and the results appeared consistent with the covariance results.

TABLE 6: VARIATIONS IN MEASUREMENT ANGLES & FIELD-OF-VIEW



- Orbit is in X-Z Plane
- Measurements are made every $\alpha_3°$ in azimuth starting at α_1 until α_2 is reached. Sequence is then repeated.

α_1 = ALLB
α_2 = ALUB
α_3 = ALINC

	CASE #	(ALUB-ALLB) FIELD-OF-VIEW (DEG)	ANGLE BETWEEN MEASUREMENTS (DEG) (ALINC)	ALLB (DEG)	ALUB (DEG)	POSITION ERRORS AFTER 500 MIN (FEET)				VELOCITY ERRORS AFTER 500 MIN (FEET)			
						RSS	X (DOWN RANGE)	Y (CROSS RANGE)	Z (VERTICAL)	RSS	$\dot{X}$ (DOWN RANGE)	$\dot{Y}$ (CROSS RANGE)	$\dot{Z}$ (VERTICAL)
	1	360	45	0	360	3080	2517	1647	640	3.2	0.7	1.8	2.5
	2	360	10	0	360	5930	5220	2734	725	6.5	0.8	3.5	5.4
*	3	360	90	0	360	2380	1969	1258	470	2.5	0.5	1.4	2.0
*	4	180	90	-45	135	2060	1564	1260	456	2.1	0.5	1.4	1.5
	5	180	90	0	180	2210	1397	1547	352	2.2	0.4	1.7	1.4
	6	180	180	0	180	46387	1166	46387	367	66.	0.4	66.	1.2
	7	90	45	-45	45	3730	3500	1150	585	3.9	0.6	1.3	3.6
*	8	90	45	0	90	2470	1810	1583	543	2.5	0.6	1.8	1.7
	9	90	45	45	135	2450	1220	1973	335	2.5	0.4	2.2	1.2
	10	90	45	90	180	2570	2235	1180	522	2.7	0.6	1.3	2.3
	11	90	90	0	90	2730	2125	1647	562	2.8	0.6	1.8	2.1
	12	20	10	-10	10	5570	3462	4340	604	6.1	0.7	4.8	3.7
	13	6	3	-3	3	14200	3600	13700	602	16.0	0.7	15.5	3.8

* Best measurement schedule for given field-of-view

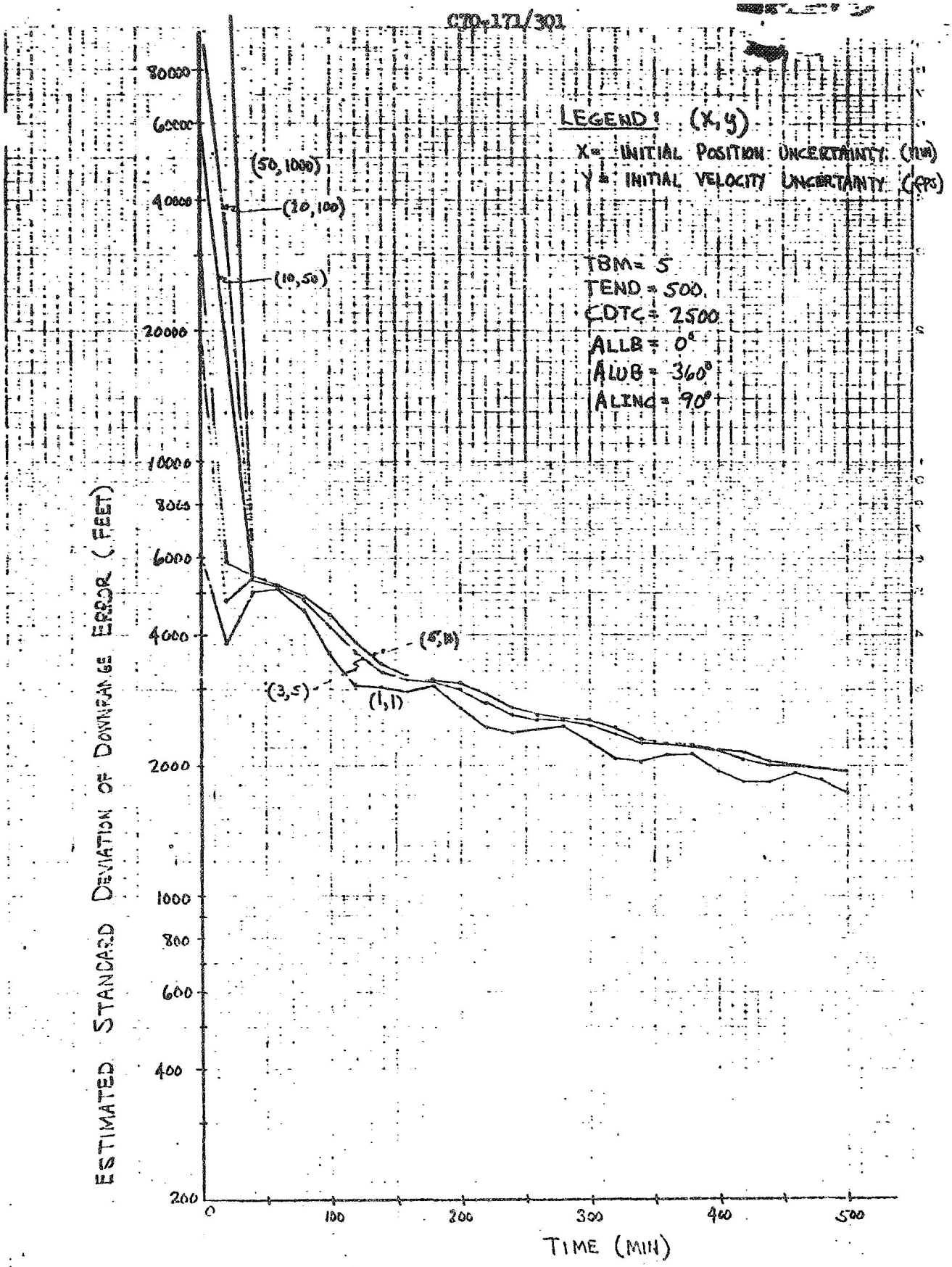


FIGURE 11: DOWNRANGE POSITION ERROR FOR VARIOUS INITIAL POSITION & VELOCITY UNCERTAINTIES.

5.0 CONCLUSION

From the data of the previous section, the following conclusions can be drawn:

1. The position and velocity errors are essentially linear functions of the measurement error for measurement errors up to 0.2°.

2. The azimuth angles at which measurements are made can have a significant effect (factors of 2 or more) on state errors. A 180° FOV gives better performance than a 360° FOV and only a 20% improvement over a 90° FOV.

3. The correlation distance (exponential correlation) affects various error components in different ways. For correlation distances in excess of 8000 nm, the errors decrease with increasing correlation distance. For distances less than 3000 nm (actual horizon correlation distances are estimated to be on the order of 2500 nm), the state errors for most cases are within 20% of the state errors from the white noise case (zero correlation distance).

4. The errors are strongly related to the number of measurements made and only slightly dependent on the time between measurements (TBM) for values of TBM $\leq$ 10 min. Increasing the number of measurements, even for large correlations and short times between measurements (table 4), decreases significantly the errors.

5. Initial position and velocity uncertainties up to 50 nm and 1000 fps respectively on each axis produces very slight differences in state errors after 20 or more measurements have been made.

6. The linearized covariance analysis was verified by Monte Carlo simulation.

REFERENCES

1. "Filtering Horizon Sensor Measurements for Orbital Navigation" by Robert J. Fitzgerald, Proceedings of AIAA/JACC Guidance and Control Conference, Seattle, Washington, August 15, 1966 - August 17, 1966. pp. 500-509.

2. "Estimation Using Sampled Data Containing Sequentially Correlated Noise", A. E. Bryson, Jr. and L. J. Henrikson, Journal of Spacecraft and Rockets, Volume 5, No. 6, June, 1968.

APPENDIX 7

1.0 INTRODUCTION

This appendix contains the detailed reliability data used for candidate computer evaluation. Section 2 presents the failure rate calculations for the modules and Section 3.0 contains the reliability models and resultant probability of success calculations.

2.0 PREDICTED FAILURE RATES

2.1 INTRODUCTION

Reliability was considered a critical design tradeoff parameter at all equipment levels throughout the GN&C reconfigurable computer study. The lowest and most critical stage of equipment design is at the device level. This section contains the development of the device and module failure rates that were used to generate the system predicted probability of success levels shown in Section 3 of this appendix.

The data in this section is largely based upon Autonetics' experience in the design, development and manufacturing of high reliability equipments. Related experience covers a broad spectrum of activities of complete electronic systems. This unusual background of systems experience is based on several major programs where effectiveness and reliability were among the primary requirements. Autonetics experience includes such major programs as Minuteman I, Minuteman II, Minuteman III, and F-111.

With the initiation of the Minuteman I program, which required a one-hundred fold increase in reliability from the state-of-the-art at that time, it was necessary to become involved in design and production problems of component parts. Autonetics, therefore, designed and managed a reliability improvement program for electronic parts that made achievement of Minuteman reliability goals possible. The reliability improvement program was a coordinated program involving electronic parts that established suppliers, procedures, controls and tests necessary for the production of high reliability parts. In addition, under Air Force Contract (AF04(647)-923), Autonetics used the Minuteman parts specifications as the basis to prepare MIL-R38100 for established reliability parts. This effort is continuing with technical and management support to RADC in the implementation of these specifications.

The Minuteman II and III programs contain state-of-the-art advances beyond those of Minuteman I. The reliability requirement is higher, the functional capabilities are significantly increased, and the weight is reduced. This achievement is being realized in production hardware for these programs. The integrated circuits are designed to Autonetics specifications and produced by parts suppliers. To ensure the production of reliable parts of all types, Autonetics developed and is managing a component quality assurance program which includes a physics-of-failure program (conducted by Autonetics) that delves deeply into failure mechanisms.

Autonetics is presently involved in advancing the state-of-the-art through MOS technology. Overall system reliability is enhanced by the use of MOS technology, since fewer devices are required to perform a particular function with less weight, less current and power. The higher complexity

MOS chips have predicted failure rates higher than that of an average bipolar IC, whereas each of these MOS devices can functionally replace many bipolar devices resulting in a substantial net gain in reliability.

Plated wire memory was also a prime consideration for the Reconfigurable G&C Computer Study. Autonetics has developed and demonstrated all the materials and process technology necessary to produce longer lifetime, NDRO plated wire and plated wire stacks. A complete pilot production capability has been established for the production of plated wire.

2.2 ORBITAL FAILURE RATES

It has been assumed that the space environment for the computer is relatively benign. A factor of 1.0 was applied to the device failure rates in accordance with MIL-STD-756A for an orbit phase environment: operating temperature approximately 25°C, minimum power on-off cycling, minimum vibration, and minimum handling. No additional degradation factors are required since the device failure rates were derived and extrapolated basically from Minuteman II strategic field operation environment.

2.3 BIPOLAR AND DISCRETE DEVICE RELIABILITY

Table 2-1 is the achieved generic part reliability from the Minuteman II production program. These achieved operational failure rates were extrapolated in this study to 1972 for bipolar IC and discrete devices. Since the silo environment is benign, it closely resembles an orbital benign space environment and requires no additional degradation or reliability usage factors.

TABLE 2-1 ACHIEVED MINUTEMAN II FAILURE RATES DATA TO 3-1-69 (FAILURES/10^6 HRS.)

Device	Failure Rate (60% Confidence)	Part Hrs. ($X10^9$)	Failures (Statistically Evaluated)
Bipolar IC	.0140	2.420	31.5
Transistor	.0072	1.118	6.5
Resistor	.00024	3.823	0
Diode	.0039	2.552	8.4
Capacitor	.0047	1.398	5.2
MLB	.0850	.024	1
MIB	.3100	.003	0
Solder	.00001	336.	3

The uncased part failure rates are reduced from the discrete device failure rate because individual packaging problems are eliminated and the number of lead bonds are reduced. The following are failure rate reduction factors based upon failure mode apportionment from Minuteman II achieved data.

Part	Failure Rate Reduction
Transistors	21 percent
Diodes	28 percent
Capacitors	28 percent
I.C.'s	16 percent
MOS	10.4 percent

2.4 MOS RELIABILITY

To analytically predict the reliability of MOS devices, a study was conducted to develop a reliability transfer model from a present day device with sufficient data and similarities in process, materials and screens as found in MOS devices. Bipolar technology was found to employ these similarities as well as an accumulation of device hours and failures from tracked field operation in a high reliability program. Post mortem analysis was done on removed devices from in-house and field operation for a statistically valid failure rate. (Reference 1) Table 2-2 is the prediction for the average MOS failure rate derivation.

TABLE 2-2 MOS FAILURE RATE PREDICTION

E-R GRADE CHIP AREA: 21.472 K SQ. MILS LEADS: 42

FAILURE MECHANISM	NORMALIZED F/R (FAIL/10^6 HOURS)	FAILURE RATE CONTRIBUTION (FAIL/10^6 HOURS)
1. Passivation	.00177/10^3 Sq. MILS of metal minus critical passivation	.008728
2. Metalization	.00295/10^3 Sq. MILS of metal (minus pads)	.012985
3. Leads	.00011/Lead	.004620
4. Faulty Diffusion	.00104/10^3 Sq. MILS of diffusion area	.003409
5. Die Bonding	.00217/DIE	.002170
6. Foreign Material	.000021/10^3 Sq. MILS of internal package area	.002639
7. Package Discrepancy	.00002/Lead (42)	.000840
8. Contamination	.00150/10^3 Sq. MILS of gate area + .25 of crossover area	.001346
9. Material Descrepancy	.00006/Package	.000060
MOS Unique		
1. Critical Passivation	.008855/10^3 Sq. MILS of gate area	.008694
2. Undetermined MOS Unique	10% of subtotal	.004549
	TOTAL	.050040

2.5 PLATED WIRE MEMORY ARRAY

A reliability model was developed for the plated wire memory (PWM) array based on in-house and field data. The areas that were considered were solder joints, fabrication techniques between multi-layer circuit boards and memory mats and planes, plated wire constituents, and the ability to detect defects prior to shipments vs normally distributed (in time) failure mechanisms. Table 2-3 is the result of the above which yields the model for the plated wire memory array extrapolated to 1972. Figure 2.1 is the predicted growth expected for the plated wire memory plane.

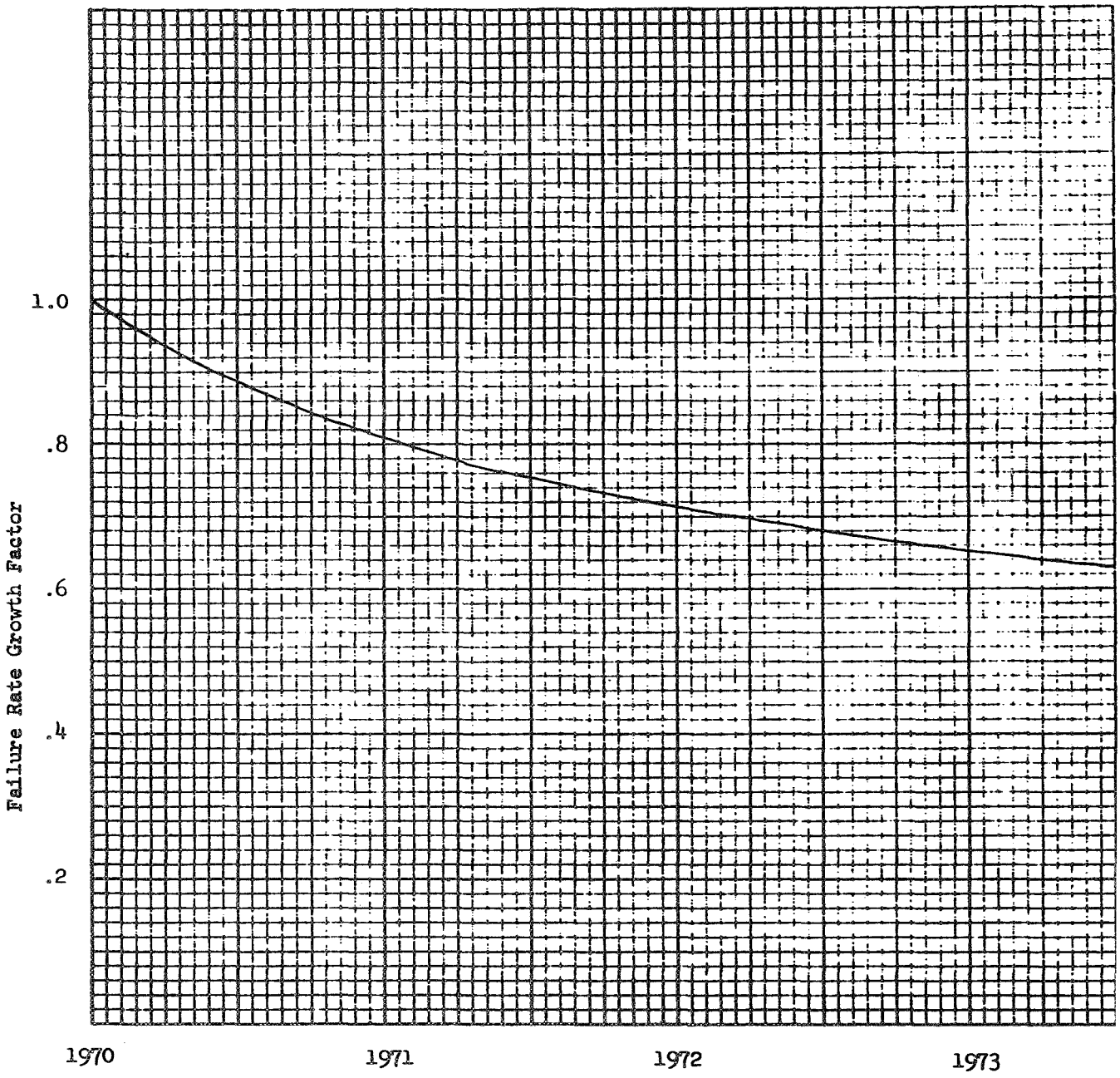
TABLE 2-3 PLATED WIRE MEMORY PLANE PREDICTION (16K) 1972

Elements	Qty	Failure Rate (Fail/10^6 Hrs.)	Failure Rate Contribution (Fail/10^6 Hrs.)
Bit Cable	2	.0001	.0002
Bit Wire (Solder)	2448	.0001	.2448
Interstituals (Solder)	136	.00001	.0014
Board Plane	2	.0400	.0800
Cable (Solder)	2448	.00001	.0245
Word Straps (Solder)	288	.00001	.0029
Connectors	4	.0020	.0080
		TOTAL	.3618

2.6 ADVANCED PACKAGING

The advanced packaging concept where uncased devices are ultrasonically bonded to a ceramic substrate will enhance the reliability of the equipment. A substantial reduction of solder connections, attachment of the due, individual package discrepancies, and foreign materials were the failure mechanisms which were considered to be the primary sources of failure rate reductions. The packaged substrate reliability consists of the failure rate of the uncased devices, the substrate, number of leads which go to the external pins, foreign material and die bond contribution (10% of the failure rate of the uncased devices).

Figure 2.1 Predicted vs Time Reliability (Failure Rate) Growth Factor For MOS and Plated Wire Memory Planes



2.7 DEVICE FAILURE RATES

Table 2-4 shows the device failure rates by generic families for both cased and uncased devices extrapolated to 1972. Figure 2.1 is the predicted failure rate growth curve vs time for MOS devices and plated wire memory planes.

TABLE 2-4 DEVICE FAILURE RATES (1972)

DEVICE	FAILURE RATE (FAIL/10^6 HRS.)	
	Cased	Uncased
MNOS (24.3 Sq. MILS)	.053042	.042773
MOS (29.9 Sq. MILS)	.063778	.053509
MOS (21.45 Sq. MILS)	.050040	.039771
MOS-All Others	.0500	.0398
IC	.0080	.0067
Transistor	.0050	.0039
Diode	.0025	.0018
Resistor	.0002	N/A
Capacitor	.0030	.0022
Substrate	.0050	.0050
MLB	.0400	N/A
MIB	.1000	N/A
Connector	.0020	N/A
Solder	.00001	N/A
PCB	.0100	N/A
Lead & Pkg. Disc.	N/A	.0001
Bonds & Foreign Mtl	N/A	10%
Transformer	.0010	N/A
Delay Line	.0050	N/A
Variable Resistor	.0020	N/A
RFI	.0015	N/A

2.8 MODULE FAILURE RATE PREDICTIONS

Tables 2-5 through 2-11 are the orbital operational failure rate predictions for each type of module that may be used in the computer organizations. These tables were used in deriving tables 4-9 and 4-10 of Volume II.

TABLE 2-5 MOS MEMORY PREDICTION (FAIL/10^6 HRS.) ADVANCED PACKAGING

COMPONENT	FAILURE RATE	QTY	FAILURE RATE CONTRIBUTION	QUANTITY		FAILURE RATE CONTRIBUTION	
				2X16K	32K	2X16K	32K
RWMD SUBSTRATE	1.4140			10	9	14.1400	12.7260
Uncased MOS (21.45 Sq. MILS)	.039771	32	1.272672				
Leads & Pkg.	.000130	70	.009100				
Foreign Mtl' & Die Bond			.127267				
Substrate	.005000	1	.005000				
MNOS SUBSTRATE	1.5197			18	17	27.3546	25.8349
Uncased MNOS	.042773	32	1.368736				
Leads and Pkg	.000130	70	.009100				
Foreign Mtl & Die Bond			.136874				
Substrate	.005000	1	.005000				
MOS MIS SUBSTRATE	1.0467			6	4	6.2802	4.1868
Uncased MOS (29.9 Sq. MILS)	.053509	14	.749126				
Uncased IC	.006720	25	.168000				
Uncased Capacitors	.002160	10	.021600				
Leads & Pkg.	.000130	70	.009100				
Foreign MTL & Die Bond			.093872				
Substrate	.005000	1	.005000				
NON MOS SUBSTRATE	.1519			4	2	.6076	.3038
Uncased Capacitor	.00216	10	.02160				
Uncased IC	.00672	1	.00672				
Uncased Transistor	.00395	20	.07900				
Uncased Diode	.00180	10	.01800				
Leads & Pkg	.00013	70	.00910				
Foreign MTL & Die Bond			.01250				
Substrate	.00500	1	.00500				
MLB	.0400			4	3	.1600	.1200
Connectors	.0020			4	3	.0080	.0060

TABLE 2-5 MOS MEMORY PREDICTION (FAIL/10^6 HRS.) ADVANCED PACKAGING (CONTINUED)

COMPONENT	FAILURE RATE	QTY	FAILURE RATE CONTRIBUTION	QUANTITY		FAILURE RATE CONTRIBUTION	
				2X16K	32K	2X16K	32K
Solder	.0001			2660	2240	.0266	.0224
Org. #1 & Sub Total #3							43.1999
Org. #2 & Sub Total #4						48.5770	
△SUBSTRATE	.3098			6	2	1.8588	.6196
Uncased IC	.00672	40	.26880				
Lead and Pkg	.00013	70					
Foreign Mtl & Die Bond			.02688				
Substrate	.00500	1	.00500				
△Solder	.00001			420	140	.0042	.0014
Org. #3							43.8209
Org. #4						50.4200	

TABLE 2-6 PLATED WIRE MEMORY (FAIL/10^6 HRS.) CONVENTIONAL PACKAGING

COMPONENT OR MODULE	FAILURE RATE	QTY	FAILURE RATE CONTRIBUTION	QUANTITY		FAILURE RATE CONTRIBUTION	
				2X16K	32K	2X16K	32K
Selection Module	.6599			2	2	1.3198	1.3198
Transformer	.0010	17	.0170				
Transistor	.0050	17	.0850				
IC	.0080	13	.1040				
Diode	.0025	143	.3575				
Resistor	.0002	154	.0308				
Capacitor	.0030	4	.0120				
MLB	.0400	1	.0400				
Connector	.0020	1	.0020				
Solder	.00001	1160	.0116				
Digit Module	1.1176			4	2	4.4704	2.2352
IC	.0080	73	.5840				
Transformer	.0010	17	.0170				
Transistor	.0050	41	.2050				
Diode	.0025	34	.0850				
Resistor	.0002	84	.0168				
Capacitor	.0030	48	.1440				
Connector	.0020	1	.0020				
Delay Line	.0050	1	.0050				
Var. Resistor	.0020	1	.0020				
MLB	.0400	1	.0400				
Solder	.00001	1680	.0168				
Timing & Control Module	.5958			2	1	1.1916	.5958
Delay Line	.0050	1	.0050				
Transformer	.0010	2	.0020				
IC	.0080	59	.4720				
Transistor	.0050	2	.0100				
Diode	.0025	9	.0225				
Resistor	.0002	29	.0058				
Capacitor	.0030	9	.0270				
Connector	.0020	1	.0020				
MLB	.0400	1	.0400				

TABLE 2-6 PLATED WIRE MEMORY (FAIL/10^6 HRS.) CONVENTIONAL PACKAGING (CONTINUED)

COMPONENT OR MODULE	FAILURE RATE	QTY	FAILURE RATE CONTRIBUTION	QUANTITY		FAILURE RATE CONTRIBUTION	
				2X16K	32K	2X16K	32K
Solder	.00001	950	.0095				
Array Module	3.7250			2	2	7.4500	7.4500
IC	.0080	145	1.1600				
MOS	.0500	34	1.7000				
Transistor	.0050	114	.5700				
Resistor	.0002	270	.0540				
Capacitor	.0030	17	.0510				
Diode	.0025	40	.1000				
MLB	.0400	1	.0400				
Connector	.0020	1	.0020				
Solder	.00001	4800	.0480				
Memory Plane	.3618			2	2	.7236	.7236
Bit Cable	.0001	2	.0002				
Bit Wire (Solder)	.0001	2448	.2448				
Interstitual (Solder)	.00001	136	.0014				
Planes	.0400	2	.0800				
Cable (Solder)	.00001	2448	.0245				
Word Strap (Solder)	.00001	288	.0029				
Connector	.0020	4	.0080				
Org. #1 & Sub-Total #3							12.3244
Org. #2 & Sub-Total #4						15.1554	
△For #3	.7012				1		.7012
IC	.0080	80	.6400				
Solder	.00001	1120	.0112				
MLB	.0400	1	.0400				
Connector	.0020	1	.0020				
Org. #3							13.0256
△For #4	1.0188			2		2.0376	
IC	.0080	120	.9600				
Solder	.00001	1680	.0168				
MLB	.0400	1	.0400				
Connector	.0020	1	.0200				
Org. #4						17.1930	

TABLE 2-7 VCS PREDICTION (FAIL/10^6 HRS.)

COMPONENT	FAILURE RATE	QTY.	FAILURE RATE CONTRIBUTION	QUANTITY		FAILURE RATE CONTRIBUTION	
				CONVENTIONAL	ADVANCED	CONVENTIONAL	ADVANCED
HTF - Clock Buffer	.1152			1		.1152	
Uncased IC	.0067	1	.0067				
Uncased Transistor	.0039	12	.0468				
Uncased Diode	.0018	20	.0360				
Uncased Capacitor	.0022	4	.0088				
Substrate	.0050	1	.0050				
Leads & Pkg.	.0001	14	.0014				
Foreign MTL & Die Bond			.0105				
MOS	.0500			4		.2000	
MLB	.0400			1		.0400	
Solder	.00001			100	100	.0010	.0010
MOS Substrate	.2957				1		.2959
Uncased MOS	.0398	4	.1592				
Lead & Pkg	.0001	70	.0070				
Die Bond & Foreign Mtl.			.0262				
Substrate	.0050	1	.0050				
HTF Clock Buffer Devices			.0983				
PCB	.0100				1		.0100
TOTAL						.3562	.3067

TABLE 2-8 IOP PREDICTION (FAIL/10^6 HRS.)

COMPONENT	FAILURE RATES		QTY.	FAILURE RATE CONTRIBUTION	
	CASED	UNCASED		CONVENTIONAL PKG.	ADVANCED PKG.
MOS	.0500	.0398	24	1.2000	.9552
HTF Clock Buffer (See Table 10)	.1152	.0983	1	.1152	.0983
IC	.0080	.0067	35	.2800	.2345
Transformer	.0010	N/A	6	.0060	.0060
Resistor	.0002	N/A	60	.0120	.0120
Capacitor	.0030	N/A	33	.0990	.0990
MLB	.0400		1	.0400	
Connector	.0020	N/A	1	.0020	.0020
Solder	.00001	450	1760	.0176	.0045
Substrate		.0050	3		.0150
Leads & Pkg.		.0001	210		.0210
Foreign Mtl. & Die Bond					.1324
PCB	.0100		1		.0100
TOTAL ORG. # 1 and #3				1.65666	1.5899
IC	.0080	.0067	16	.1280	.1072
Solder	.00001		220	.0022	
Foreign Mtl. & Die Bond					.0107
TOTAL ORG. # 2 & #4				1.7868	1.6971

TABLE 2-9 PROCESSOR PREDICTION (FAIL/10^6 HRS.)

COMPONENT	FAILURE RATES		QTY.	FAILURE RATE CONTRIBUTION	
	CASED	UNCASED		CONVENTIONAL PKG.	ADVANCE PKG.
HTF Clock Driver & Osc.					
Transistor		.0039	4	.0156	.0156
Diode		.0018	1	.0018	.0018
Capacitor		.0022	6	.0132	.0132
Substrate		.0050	1	.0050	
Leads & Pkg.		.0001	14	.0014	
Foreign Mtl. & Die Bond				.0036	
HTF Buffer (See Table 10)	.1152	.0983	1	.1152	.0983
MOS	.0500	.0398	46	2.3000	1.8308
IC	.0080		23	.1840	
Resistor	.0002		12	.0024	
Leads & Pkg.		.0001	350		.0350
Foreign Mtl. & Die Bond					.2174
Substrate		.0050	5		.0250
MLB	.0400			.0400	.0400
Connector	.0020		1	.0020	.0020
Solder	.00001		2330(Con) 450(Adv)	.0233	.0045
TOTAL ORG. #1 & #3				2.7075	2.2836
△IC	.0080	.0067	16	.1280	.1072
△SOLDER	.00001		220	.0022	
△FOR MT. & DIE BOND					.0107
TOTAL ORG. #2 and #4				2.8377	2.4015

TABLE 2-10 POWER CONVERTER PREDICTION (FAIL/10^6 HRS.)

COMPONENT	FAILURE RATES		QTY	FAILURE RATE CONTRIBUTION	
	CASED	UNCASED		CONVENTIONAL PKG.	ADVANCE PKG.
Transistor	.0050	.0039	35	.1750	.1365
Diode	.0025	.0018	35	.0875	.0630
Capacitor	.0030		28	.0840	.0840
Resistor	.0002		70	.0140	.0140
Transformer	.0010		7	.0070	.0070
Substrate	.0050		2		.0100
Leads & Pkg.		.0001	20		.0020
Foreign Mtl. & Die Bond					.0209
PCB	.0100		1	.0100	.0100
Connector	.0020		1	.0020	.0020
Solder	.00001		700(Conv) 600(Adv.)	.0070	.0060
TOTAL ORGS. #1, #2, #3 and #4 →				.3865	.3554

TABLE 2-11 CHASSIS PREDICTION (FAIL/10^6 HRS.)

		CANDIDATE															
COMPONENT	FAILURE RATE	1.1A		1.2A		2.1A		2.2A		3.1A		3.2A		4.1A		4.2A	
		QTY.	F/R	QTY.	F/R	QTY.	F/R	QTY.	F/R	QTY.	F/R	QTY.	F/R	QTY.	F/R	QTY.	F/R
Connector	.0020	10	.0200	12	.0240	11	.0220	13	.0260	11	.0220	13	.0260	12	.0240	15	.0300
MLB	.1000	1	.1000	1	.1000	1	.1000	1	.1000	1	.1000	1	.1000	1	.1000	1	.1000
RFI	.0115	1	.0015	1	.0015	1	.0015	1	.0015	1	.0015	1	.0015	1	.0015	1	.0015
TOTAL			.1215		.1255		.1235	.	.1275		.1235		.1275		.1255		.1315

		CANDIDATE															
COMPONENT	FAILURE RATE	1.1C		1.2C		2.1 C		2.2C		3.1C		3.2C		4.1C		4.2C	
		QTY.	F/R	QTY.	F/R	QTY.	F/R	QTY.	F/R	QTY.	F/R	QTY.	F/R	QTY.	F/R	QTY.	F/R
Connector		22	.0440	24	.0480	27	.0540	29	.0580	24	.0480	25	.0500	31	.0620	32	.0640
MLB		1	.1000	1	.1000	1	.1000	1	.1000	1	.1000	1	.1000	1	.1000	1	.1000
FRI		1	.0015	1	.0015	1	.0015	1	.0015	1	.0015	1	.0015	1	.0015	1	.0015
TOTAL			.1455		.1495		.1555		.1595		.1495		.1515		.1635		.1655

3.0 RELIABILITY MODELS AND CALCULATIONS

3.1 RELIABILITY DEFINITIONS AND RELATIONSHIPS

3.1.1 Definitions

In this analysis the following definitions and relationships will be used.

Let

$f(t)$ = failure density function

$F(t)$ = Failure distribution function

$R(t)$ = reliability distribution function or reliability function

$z(t)$ = hazard rate or instantaneous failure rate

θ = mean time to failure

Then

$$F(t) = \int_0^t f(\tau)d\tau \tag{3-1}$$

$$R(t) = 1 - F(t) = \int_t^\infty f(\tau)d\tau \tag{3-2}$$

$$z(t) = -\frac{1}{R(t)}\frac{dR(t)}{dt} = \frac{f(t)}{R(t)} \tag{3-3}$$

$$\theta = \int_0^\infty t\ f(t)dt = \int_0^\infty R(t)dt \tag{3-4}$$

3.1.2 Exponential Functions

The failure density function is often represented by an exponential function

$$f = \lambda e^{-\lambda t} \tag{3-5}$$

where λ is constant hazard rate, see Eq (3-8).

Substituting Eq (3-5) into (3-1) - (3-4) results in, respectively:

$$F(t) = 1 - e^{-\lambda t} \tag{3-6}$$

$$R(t) = e^{-\lambda t} \tag{3-7}$$

$$z(t) = \lambda \tag{3-8}$$

$$\theta = \frac{1}{\lambda} \tag{3-9}$$

3.1.3 Basic Reliability Models

A computer system model can be made generally of basic reliability models for the following configurations:

1. Series-parallel
2. Parallel-series
3. Partial redundancy
4. Standby

Expressions for these models are readily available (Reference 2) and will not be given here.

3.2 CANDIDATE RELIABILITY MODELS AND FUNCTIONS

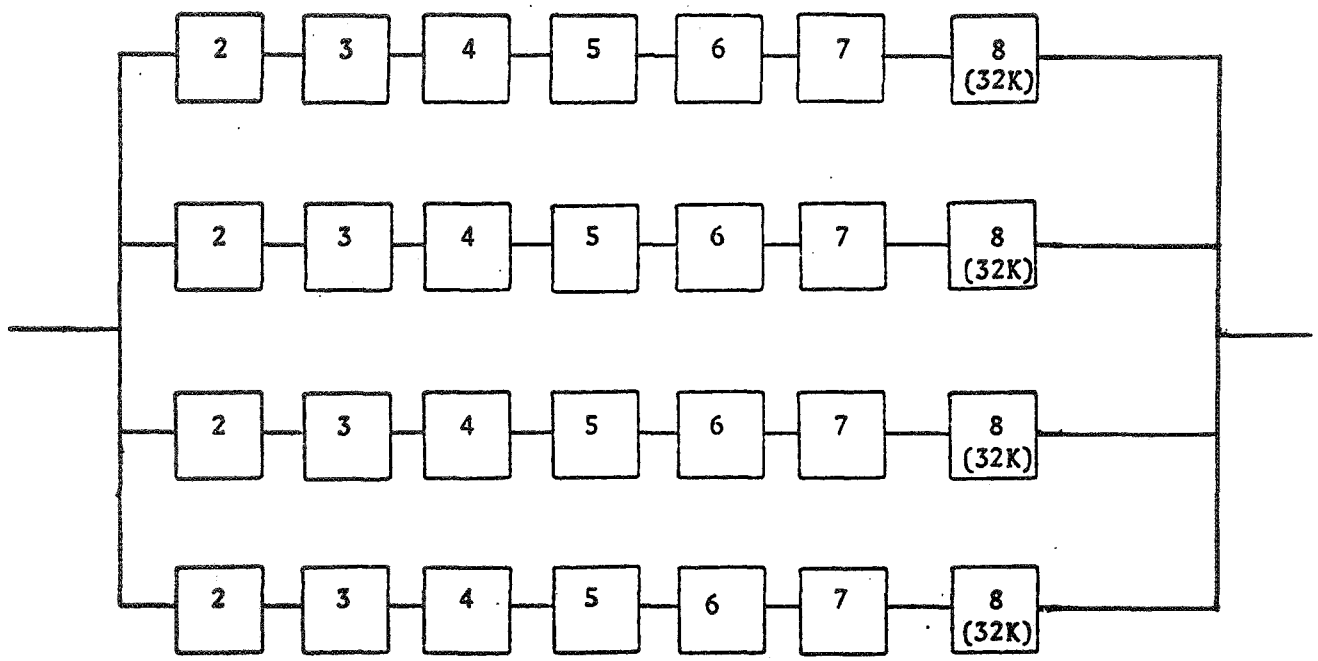
Figures 3-1 through 3-8 give the following eight candidate reliability models and functions:

Candidates Models	Figure
1. Non-modular Multicomputer without VCS (1_{1C} & 1_{1A})	3-1
2. Non-modular Multicomputer with VCS (1_{2C} & 1_{2A})	3-2
3. Modular Multicomputer without VCS (2_{1L} & 2_{1A})	3-3
4. Modular Multicomputer with VCS (2_{2C} & 2_{2A})	3-4
5. Non-modular Multiprocessor without VCS (3_{1C} & 3_{1A})	3-5
6. Non-modular Multiprocessor with VCS (3_{2C} & 3_{2A})	3-6
7. Modular Multiprocessor without VCS (4_{1C} & 4_{1A})	3-7
8. Modular Multiprocessor with VCS (4_{2C}, 4_{2C}*, & 4_{2A})	3-8

The symbols which represent their respective units in Figures 3-1 through 3-8 are defined as follows:

Symbols	Units
1	VCS
2	Power Converter
3	Chassis
4	I/O Serial Switch
5	I/O Parallel Switch
6	Processor
7	Input/Output Processor
8	Memory (32K or 16K words)

These reliability models were developed based on the candidate computer characteristics presented in Vol. II, see 4.5.2. For this analysis no spares were present in the candidates and each computer simply had 32K of memory.



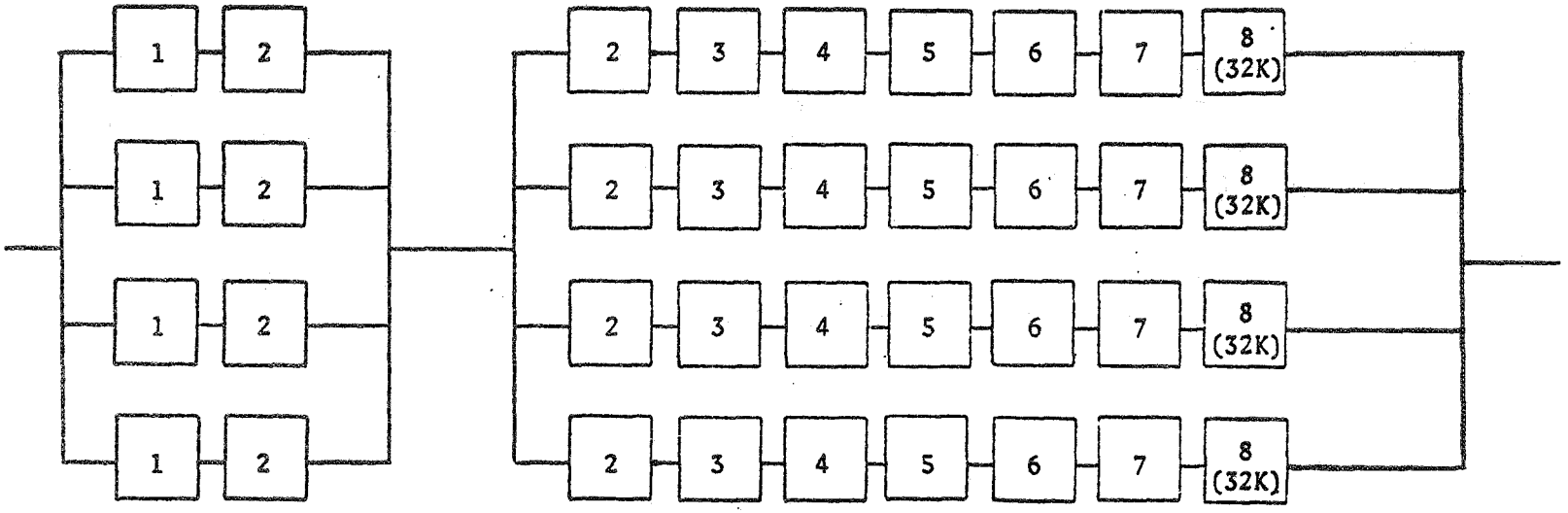
$$R = [1 - (1 - \prod_{j=2}^{8} R_j)^4]$$

where

$R = R(t)$ = Candidate reliability function

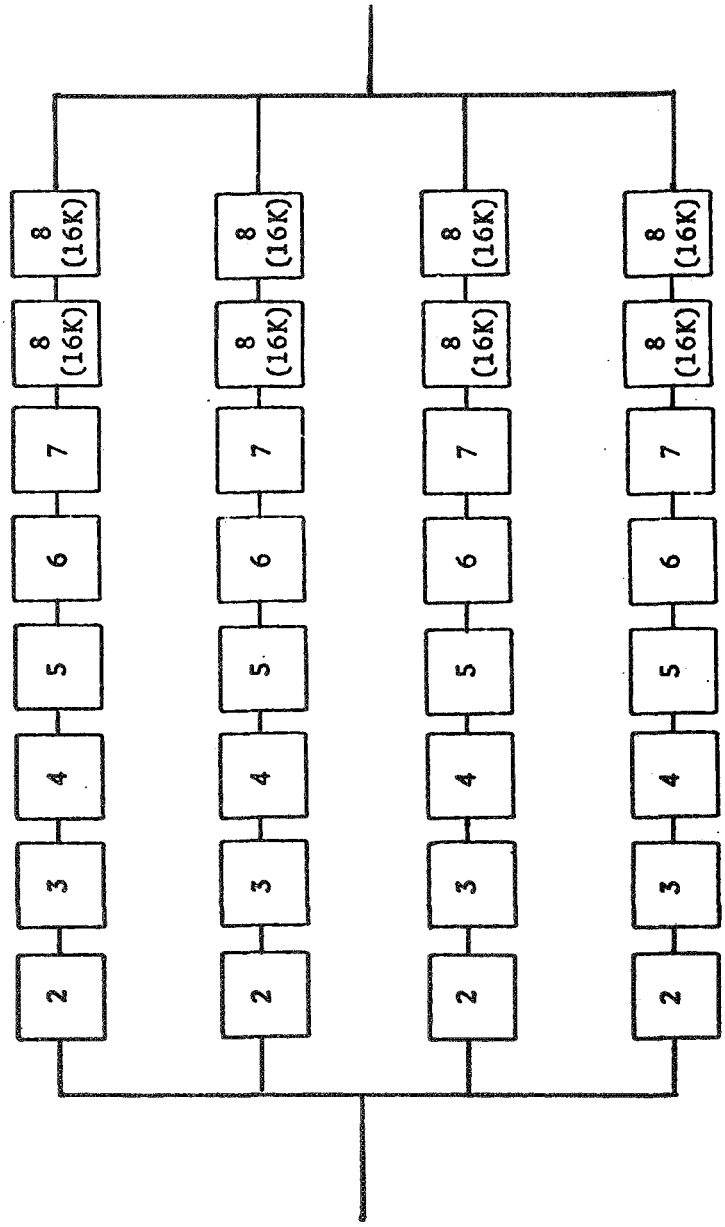
$R_j = R_j(t)$ = jth unit reliability function

Figure 3-1 Non-modular Multicomputer (without VCS) Reliability Model and Function



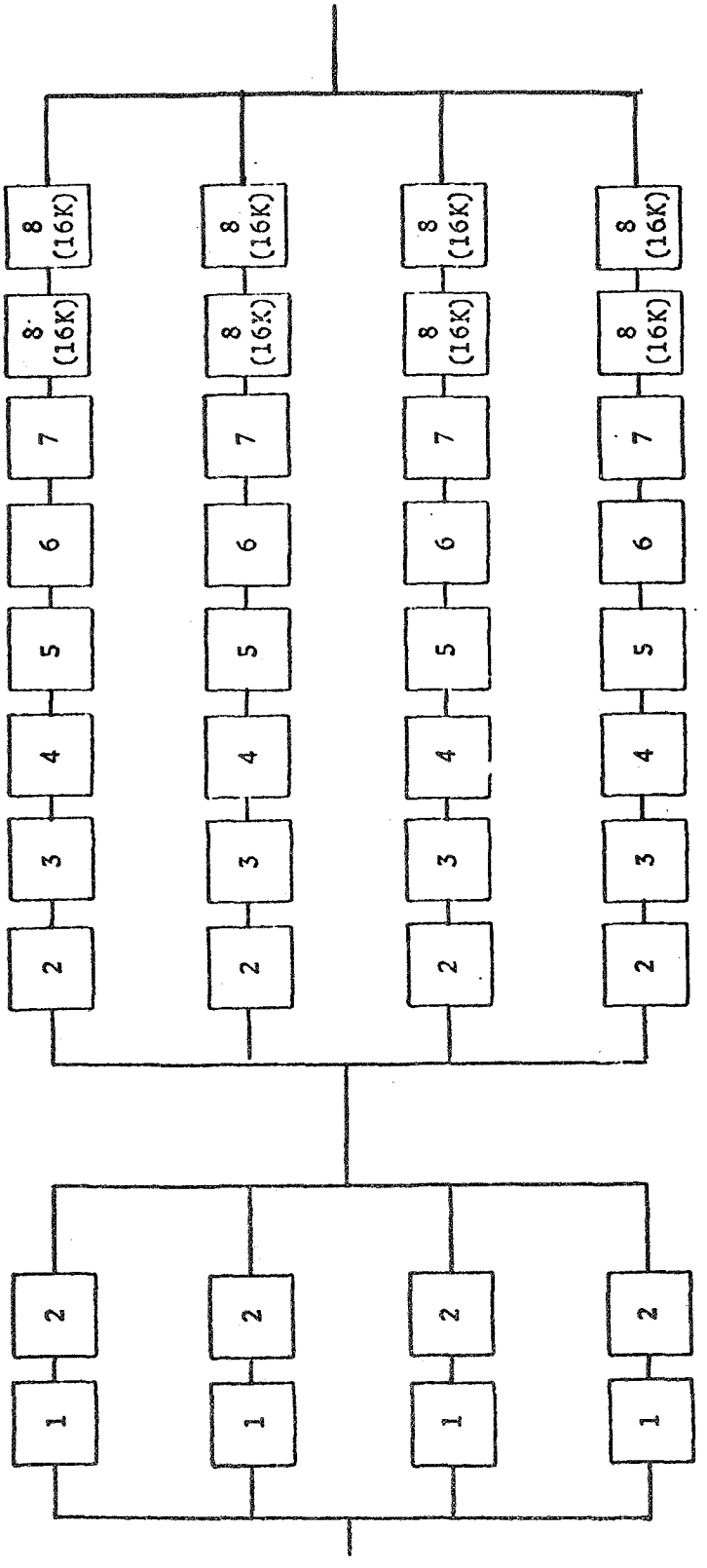
$$R = [1 - (1 - R_1 R_2)^4][1 - (1 - \prod_{j=2}^{8} R_j)^4]$$

Figure 3-2 Non-modular Multicomputer (with VCS) Reliability Model and Function



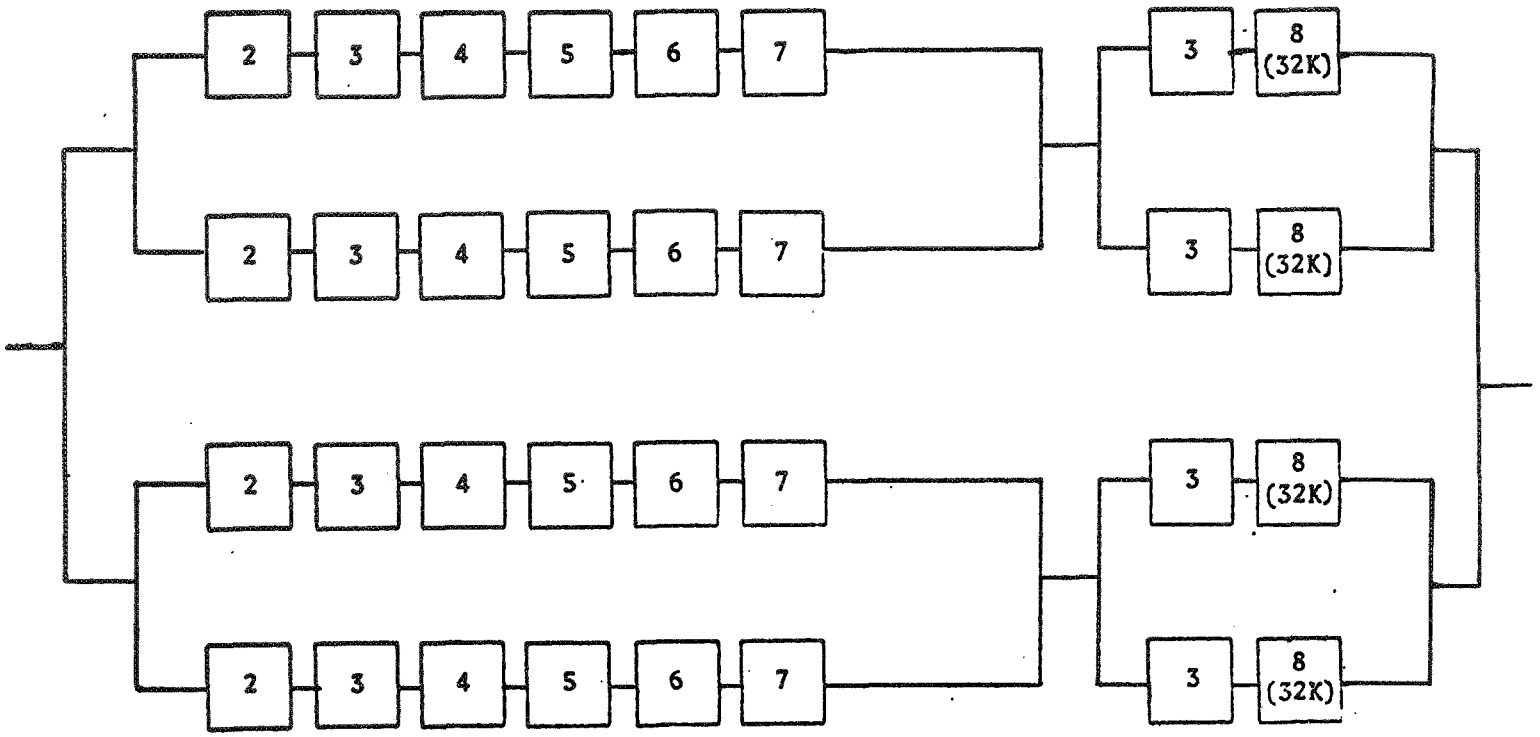
$$R = [1 - (1 - R_8 \prod_{j=2}^{8} R_j)^4]$$

Figure 3-3 Modular Multicomputer (without VCS) Reliability Model and Function



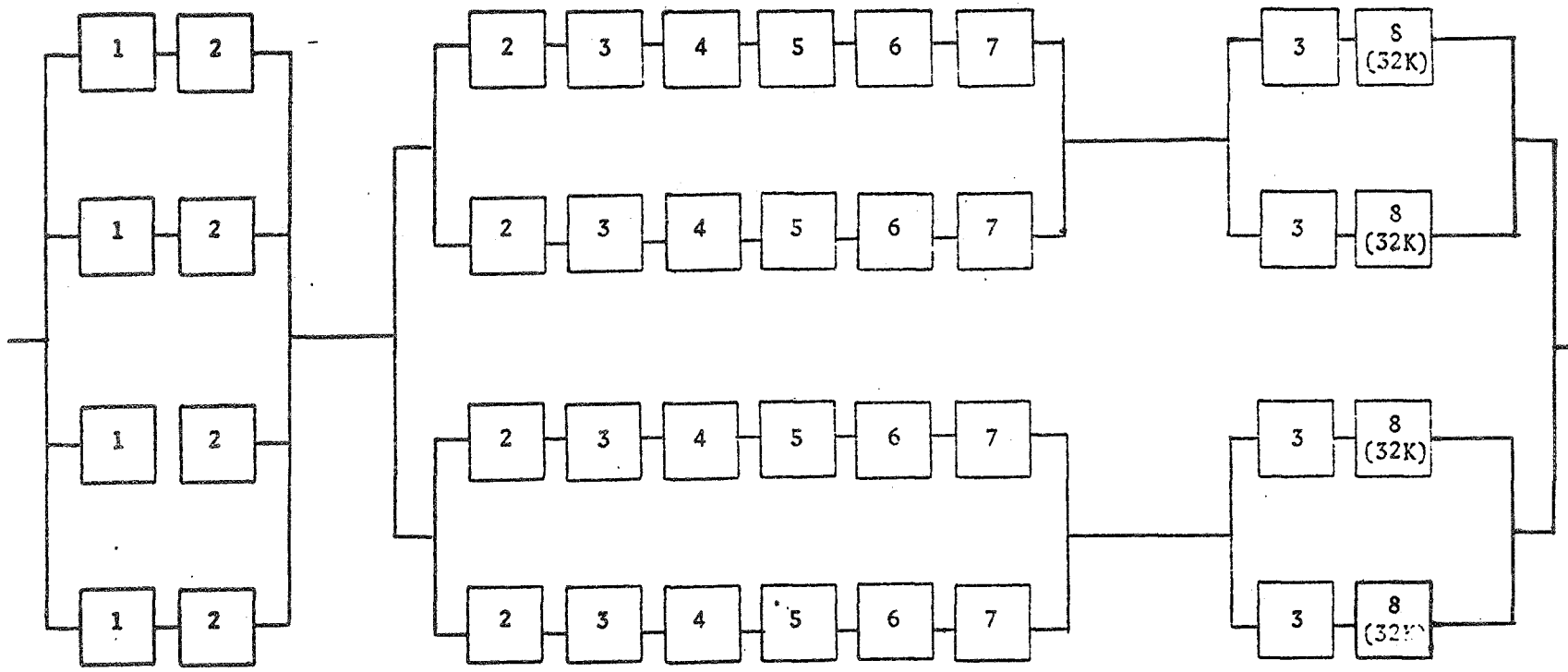
$$R = [1 - (1 - R_1 R_2)^4][1 - (1 - R_8 \prod_{j=2}^{8} R_j)^4]$$

Figure 3-4 Modular Multicomputer (with VCS) Reliability Model and Function



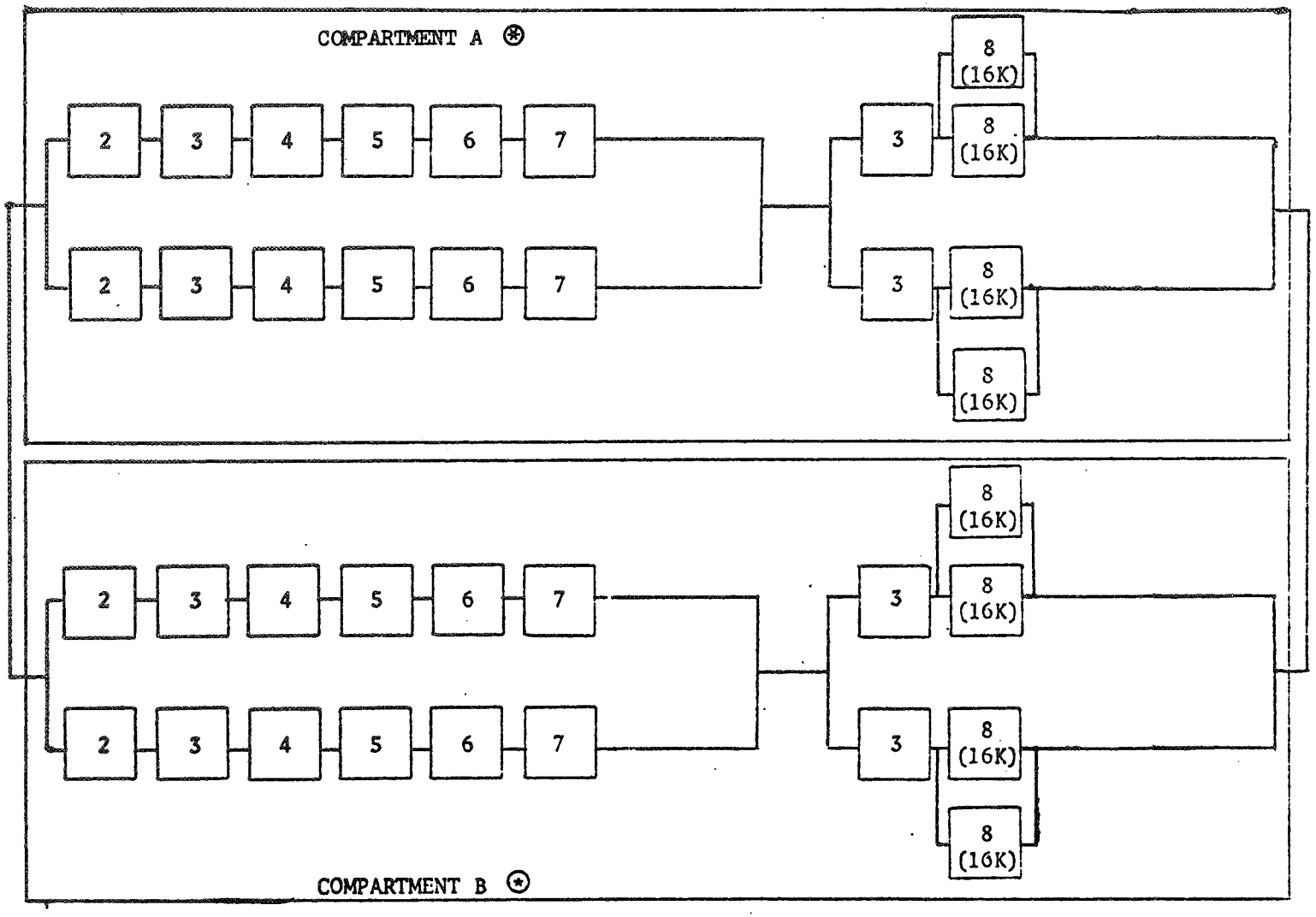
$$R = 1 - \{ 1 - [1 - (1 - \prod_{j=2}^{7} R_j)^2][1 - (1 - R_3R_8)^2] \}^2$$

Figure 3-5 Non-modular Multiprocessor (without VCS) Reliability Model and Function



$$R = [1 - (1 - R_1R_2)^4]\left[1 - \{1 - [1 - (1 - \prod_{j=2}^{7} R_j)^2][1 - (1 - R_3R_8)^2]\}^2\right]$$

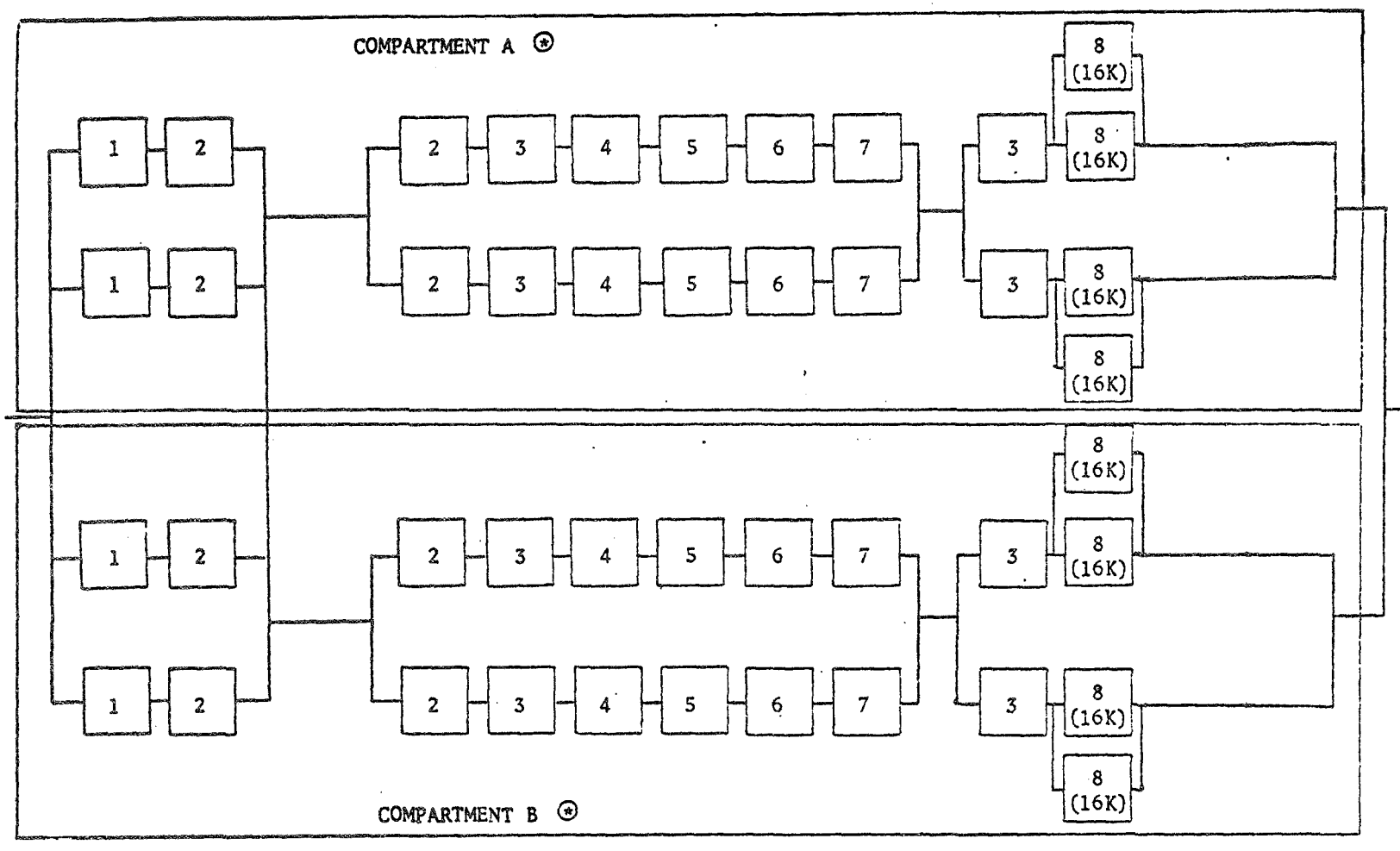
Figure 3-6 Non-modular Multiprocessor (with VCS) Reliability Model and Function



⊛ Minimum requirement for Memory in Compartment A or B is 32K words.

$$R = 1 - \{1 - [1 - (1 - \prod_{j=2}^{7} R_j)^2][R_3^2][1 - 4R_8(1 - R_8)^3 - (1 - R_8)^4 + 2R_8^2(1-R_8)^2(\frac{1}{R_3} - 1)]\}^2$$

Figure 3-7 Modular Multiprocessor (without VCS) Reliability Model and Function



⊛ Minimum requirement for Memory in Compartment A or B is 32K words.

$$R = [1 - (1 - R_1R_2)^4]\left[1 - \{1-[1 - (1 - \prod_{j=2}^{7} R_j)^2][R_3^2][1 - 4R_8(1 - R_8)^3 - (1 - R_8)^4 + 2R_8^2(1 - R_8)^2(\frac{1}{R_3} - 1)]\}^2\right]$$

Figure 3-8 Modular Multiprocessor (with VCS) Reliability Model and Function

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3.3 CANDIDATE RELIABILITY VALUES AND EQUIVALENT MEAN TIME TO FAILURE

Table 4-10 of Volume II and Figure 3-1 give the reliability values and equivalent mean time to failure for the sixteen candidates, respectively. They were computed using:

1. The candidate reliability models and functions given in Figure 3-1 through 3-8,

2. The exponential unit reliability function; i.e.,

$$R_j = e^{-\lambda_j t}$$

3. The numerical values of the unit failure rates (λ_j) for the conventional and advanced computer design technology given in Tables 3-2 and 3-3, respectively,

4. The space station mission duration (T_m) of 6 months, and

5. Equivalent mean time to failure:

$$\theta_e = \frac{T_m}{\ln\left[\frac{1}{R(T_m)}\right]}$$

where

$R(T_m)$ = computer reliability for the mission.

TABLE 3-1 COMPUTER SYSTEM CANDIDATES EQUIVALENT MEAN TIME TO FAILURE (HOURS)

CANDIDATES DESCRIPTION	CONVENTIONAL TECHNOLOGY		ADVANCED TECHNOLOGY	
	Without VCS	With VCS	Without VCS	With VCS
Non-modular Multicomputer	135×10^6	135×10^6	2.30×10^6	2.30×10^6
Modular Multicomputer	69.7	69.7	1.47	1.47
Non-modular Multiprocessor	304	304	3.12	3.12
Modular Multiprocessor	946	940	105	103

TABLE 3-2 COMPUTER UNITS FAILURE RATE (λ_j in No. of Failures per 10^6 Hours) - CONVENTIONAL TECHNOLOGY

Units	Non-modular Multicomputer		Modular Multicomputer		Non-modular Multiprocessor		Modular Multiprocessor	
j. Name	W/O VCS	W/VCS	W/O VCS	W/VCS	W/O VCS	W/VCS	W/O VCS	W/VCS
1. VCS	0	.3562	0	.3562	0	.3562	0	.3562
2. Power Converter	.3865	.3865	.3865	.3865	.3865	.3865	.3865	.3865
3. Chassis	.1455	.1495	.1555	.1595	.1495	.1515	.1635	.1655
4. I/O Serial Switch*	0	0	0	0	0	0	0	0
5. I/O Parallel Switch*	0	0	0	0	0	0	0	0
6. Processor	2.7075	2.7075	2.8377	2.8377	2.7075	2.7075	2.8377	2.8377
7. Input/Output	1.6566	1.6566	1.7868	1.7868	1.6566	1.6566	1.7868	1.7868
8. Memory	12.3244 (32K x 32 bits)	12.3244 (32K x 32 bits)	7.5777 (16K x 32 bits)	7.5777 (16K x 32 bits)	13.0256 (32K x 32 bits)	13.0256 (32K x 32 bits)	8.5965 (16K x 32 bits)	8.5965 (16K x 32 bits)

*Failure rate is included as part of Unit 7, Input/Output, since no spares were used in calculation.

TABLE 3-3 COMPUTER UNITS FAILURE RATE (λ_j in No. of Failures per 10^6 Hours) - ADVANCED TECHNOLOGY

Units	Non-modular Multicomputer		Modular Multicomputer		Non-modular Multiprocessor		Modular Multiprocessor	
j. Name	W/O VCS	W/VCS	W/O VCS	W/VCS	W/O VCS	W/VCS	W/O VCS	W/VCS
1. VCS	0	.3067	0	.3067	0	.3067	0	.3067
2. Power Converter	.3554	.3554	.3554	.3554	.3554	.3554	.3554	.3554
3. Chassis	.1215	.1255	.1235	.1275	.1235	.1275	.1255	.1315
4. I/O Serial Switch*	0	0	0	0	0	0	0	0
5. I/O Parallel Switch*	0	0	0	0	0	0	0	0
6. Processor	2.2836	2.2836	2.4015	2.4015	2.2836	2.2836	2.4015	2.4015
7. Input/Output	1.5899	1.5899	1.6971	1.6971	1.5899	1.5899	1.6971	1.6971
8. Memory	43.1999 (32K x 32 bits)	43.1999 (32K x 32 bits)	24.2885 (16K x 32 bits)	24.2855 (16K x 32 bits)	43.8209 (32K x 32 bits)	43.8209 (32K x 32 bits)	25.2100 (16K x 32 bits)	25.2100 (16K x 32 bits)

* Failure rate is included as part of Unit 7, Input/Output, since no spares were used in calculation.

4.0 REFERENCES

1. M. F. Adam and D. M. Aaron, MOS Reliability Prediction Model, Ninth Reliability and Maintainability Conference, July, 1970.

2. Barlow, R. E. and Proschon, F., Mathematical Theory of Reliability, 1965.

APPENDIX 8

1.0 INTRODUCTION

This appendix provides detailed description of isolator devices considered during a power distribution study. In addition to the description of the devices and their operation, the failure modes and the effects on the power distribution system are discussed. The following isolator devices are described in this appendix: diodes (computer, ion implantation, and Schottky barrier hot carrier), magnetic devices (simple magnetic amplifiers, four aperture magnetic switches, and paraformers), solid state controllers, and electromechanical relays.

The second half of this appendix provides some additional information on power converter design constraints which are useful in determining the impact of power converter design options on the overall system design.

2.0 ISOLATOR DESCRIPTION

2.1 DIODES

Diodes can be used in DC systems by oring two or more DC busses to one load. They will protect the load and other busses against a shorted bus or one connected with the polarity reversed. They protect other busses from a high bus but do not protect the load. They provide no protection to the busses for a shorted load. They are also used to rectify AC voltages. The conventional diffused silicon diode junction usually fails short due to overstress. The interconnection may then fuse open or the diode may originally fail open due to fusing or mechanically opening of the interconnections. Their main disadvantage is the power dissipation and voltage variation introduced by the forward voltage drop.

Both ion implantation diodes and Schottky Barrier Hot Carrier Diodes can be designed to reduce the forward voltage drop and power dissipation by 50 to 70%, usually at the cost of increased reverse leakage current, lower breakdown voltages and reduced temperature rating.

Table 2-1 compares the characteristics of the three types of diodes for a similar 1 ma computer diode application. Table 2-2 summarizes the characteristics for a 35A diffused diode, a 30A ion implantation diode and a 50A hot carrier diode.

DEVICE	BV Volts		I_R (50V) Nano Amps		FORWARD VOLTAGE V_F 1 ma MV		10 ma MV		100 ma MV	
	Range	Limit	Range	Limit	Range	Limit	Range	Limit	Range	Limit
Diffused Continental Device CD 9002 (65 samples)	94-134	75	4-6	30	608-626	630	702-750	760	871-902	920
Schottky Barrier Hewlett Packard 2861 (141 Samples)	80-95	70	11-63	200	370-398	410	672-722	NS	2350-3800	NS
Ion Implanted Isofilm 7824 (99 samples)	63-170	75	700-7000	20,000	200-263	275	318-344	NS	513-652	NS

Data Source: Autonetics Component Technical Report CTR 70-563-033-105

NS = Not Specified

TABLE 2-1 COMPUTER DIODE COMPARISON

Device	Current Rating	Tj Max.	Typical Forward Voltage				V_R	I_R
			1.0A	10.0A	30.0A	100A		
	A	oC	V	V	V	V	V	ma
Diffused 1N1183	35A	190	0.75	0.85	1.0	1.2	50V	1.0
Ion Implantation 5R5	30A	175	0.41	0.63	0.87	---	50V	0.2
Hot Carrier MBD5500	50A	100	0.22	0.30	0.38	0.58	20V	200

Data from Specification Sheets from Motorola, ISO Film and Motorola

TABLE 2-2 POWER DIODE COMPARISON

2.2 MAGNETIC ISOLATORS

Magnetic isolators of three types are discussed. These are a simple magnetic amplifier, a four aperture magnetic switch developed by Stanford Research Institute for Jet Propulsion Labs on a NASA contract, and the parametric magnetic device called a Paraformer TM, a product of Wanlass Electric Company.

2.2.1 Magnetic Amplifier

Figures 2-1 through 2-4 show the schematic, hysteresis loops, timing diagram and transfer characteristic for a magnetic amplifier configuration. The magnetic amplifier consists of two square loop cores. The windings in the load side are reversed to induce opposite voltages in the two control windings which are driven with a current source. Since the usual current source consists of a low DC voltage and a fairly large inductor to give a high AC impedance, this configuration is shown for the current source.

The description is for a square wave source voltage; however, the operation is similar for a sinusoidal source. With no control current, the hysteresis loops of the two cores are superimposed and the cores absorb the full volt-seconds of the source and the load sees the small magnetizing current of the cores.

When control current flows a current flows in the load up to a value determined by the product of the control current and the turns ratio of the control and load windings. From the diagrams of Figures 2-1 through 2-4 and the magnetic equation

$$\text{Volt-Seconds} = KN\phi$$

the following observations can be made:

1. With no control current most of the source voltage is dropped across the core windings and the switch is off.

2. The control current can be set so the load receives full current but no more. Both cores are fully saturated and the source voltage and load current are in phase.

3. If the load tries to draw additional current (overload or short) the cores alternately come out of saturation and absorb sufficient voltage so that a fixed power is delivered to the load. This is accomplished in a non-dissipative manner by shifting the phase of the load current and source voltage. This means current flows back into the source.

4. If the volt-second rating of the cores are exceeded by exceeding the design limits for upper voltage and lower frequency, the load current is limited only by the load impedance. Under those conditions there is no current limitation for a short circuit load. These design constraints have a significant effect on the size, weight, and power losses of the magnetics.

An additional observation from design experience is that the inductor in the control circuit is a significant contributor to size and weight.

The failure characteristics of the device are as follows:

1. Shorted load: The power taken from the source is limited to some preset value automatically. It can be shut off by shutting off the control current.

2. Shorted Source: The circuit is bilateral and will pass power from the load to the shorted source up to the preset value. It can be shut off by removing the control current.

3. Open Control Winding: Fails open.

4. Shorted Control Windings: Fails closed.

5. Excessive Control Current: Preset power limiting point is raised.

6. Excessive source voltage or low frequency (including DC): Load effectively tied to source after core voltsecond rating is exceeded.

7. Dielectric Failure: Most transformer failures are due to failures of the insulation system and the voltage stress seen by the insulation is important. If the control winding to load winding ratio is ten, the induced voltage is ten times the source voltage or 2,550 peak volts for a MIL-STD-704A, 115VAC high-line transient (180 VACRMS).

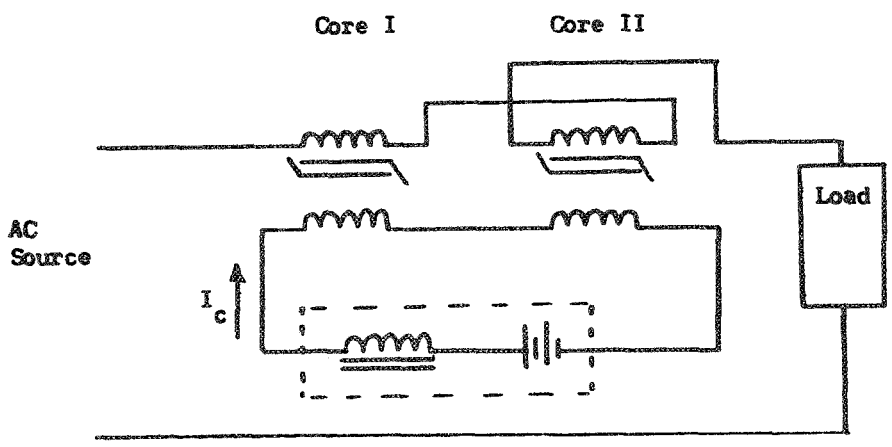


FIGURE 2-1. MAGNETIC AMPLIFIER SCHEMATIC

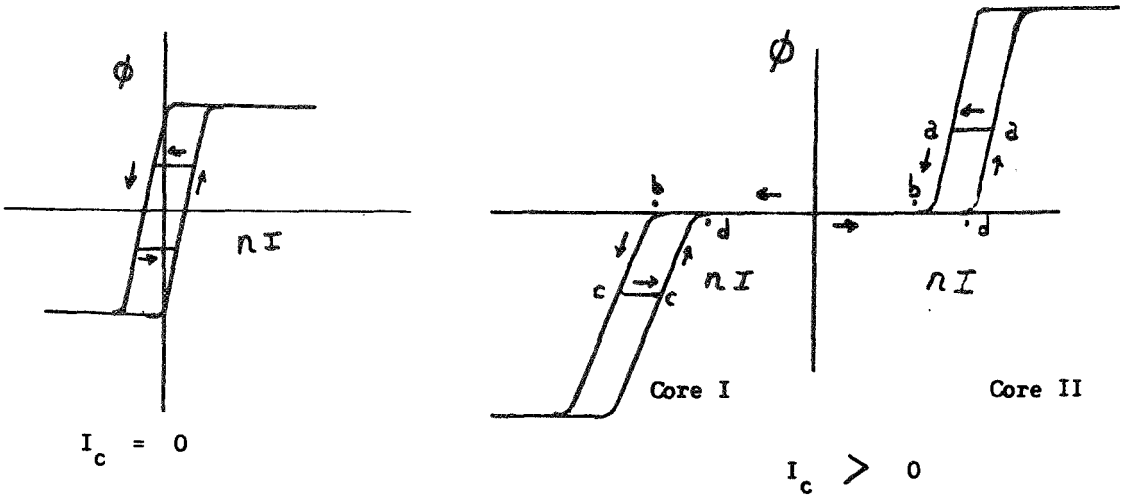


FIGURE 2-2. MAGNETIC AMPLIFIER HYSTERESIS LOOPS

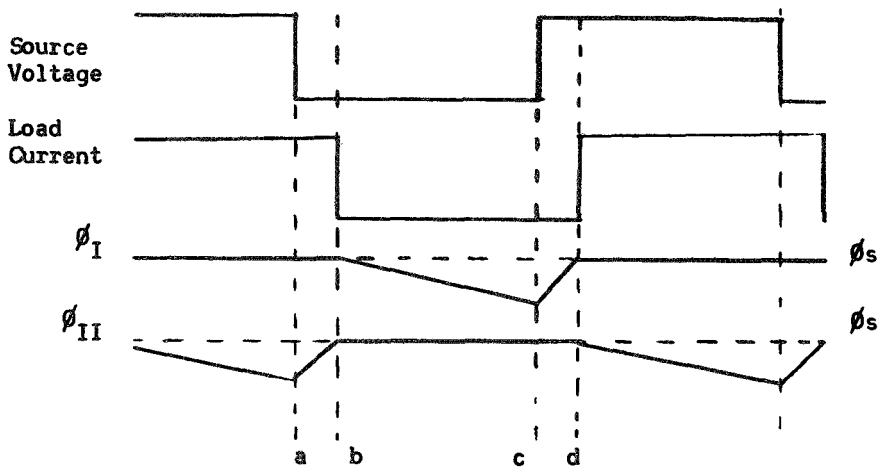


FIGURE 2-3. MAGNETIC AMPLIFIER TIMING DIAGRAM

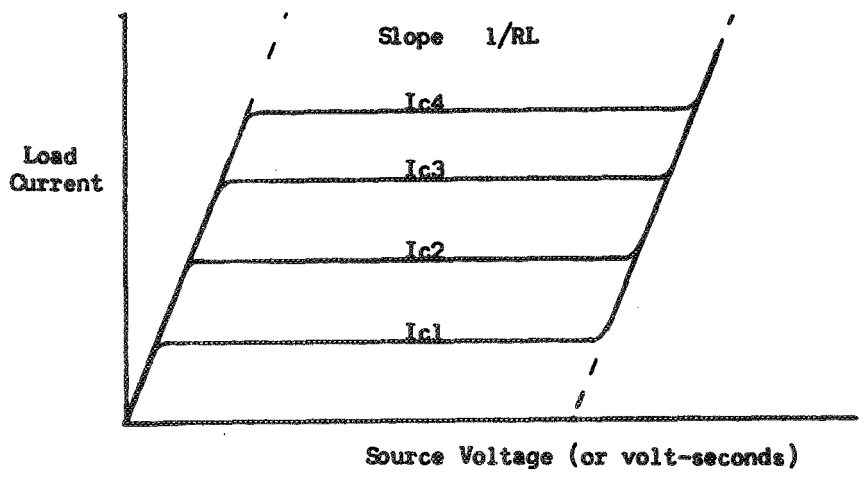


FIGURE 2-4. MAGNETIC AMPLIFIER TRANSFER CHARACTERISTICS

2.2.2 SRI Magnetic Connection Switch

Reference 8-1 describes a four aperture core with multiple windings that is used as an off-on switch for a 2.4KHz, 50V square wave source. A design requirement is that the switch fails open for either a load or switch failure. The switch contains a voter circuit such that two or more of five inputs are necessary to turn it on. No single input can either turn the circuit on or hold it on.

Figure 2-5 is taken from the reference and has been simplified to show conceptually how it operates. To connect the load to the source, the inductor is caused to saturate and the transformer to operate in its unsaturated region. To disconnect the load from the source, the transformer is caused to saturate and the inductor is operated in its unsaturated region.

The reference describes the power, control, and voter circuits in detail, the failure modes, and how to do an actual design. It should be noted the report recommends transformer drive to ensure critical volt-second balance. This transformer should be included in any comparison with alternative switches if it is not otherwise required. Also, the loss in the control circuitry is apparently not considered in the report and should be included in comparison of efficiencies since it may be substantial. Since the reference is assumed to be readily available to readers of this report, the concept will not be expanded further.

The failure characteristics of the device are as follows:

1. Shorted Loads: The current to the load overpowers the control signals limiting or removing the current to the load.

2. Shorted Source: Uncertain; circuit appears bilateral, passing power to the source from the load up to a value allowed by the control circuit with the ability of the control circuit to turn the switch off.

3. Open Control Windings:

   Voter Windings: Fails open

   Source Bias: Fails open - can be made fail-op with one or more redundant parallel windings.

   Voter Bias: Fail open with no voter input. Will turn on with one or more voter inputs.

4. Shorted Control Windings: There is no AC flux through any control windings so shorting them has no loading effect on the source. Failure modes would be same as opening the windings.

5. Excessive Control Current:

   Source Bias: No effect

   Voters and Voter Bias: The ratio is the critical parameter. The ratio is made fail-op or fail safe by using no external resistors in series with these windings and driving them from the same voltage source.

6. Excessive Source Voltage or Low Frequency: Load effectively tied to source after core volt-second rating is exceeded.

7. Dielectric Failure: Winding methods and winding resistance minimize the effect of shorted terms. Any single short to the core can be tolerated.

8. Other: The switch is extremely sensitive to the volt-second balance of the driving source and relies on a transformer drive to assure this balance. Any inbalance has a cumulative effective and results in heavy surges of current being drawn from the source.

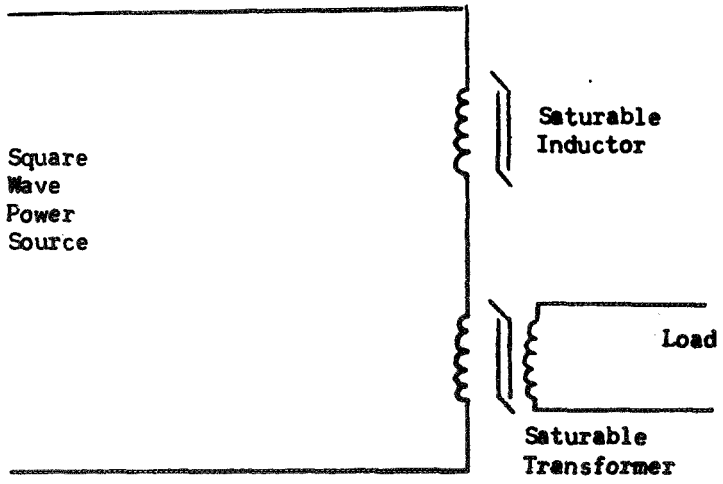
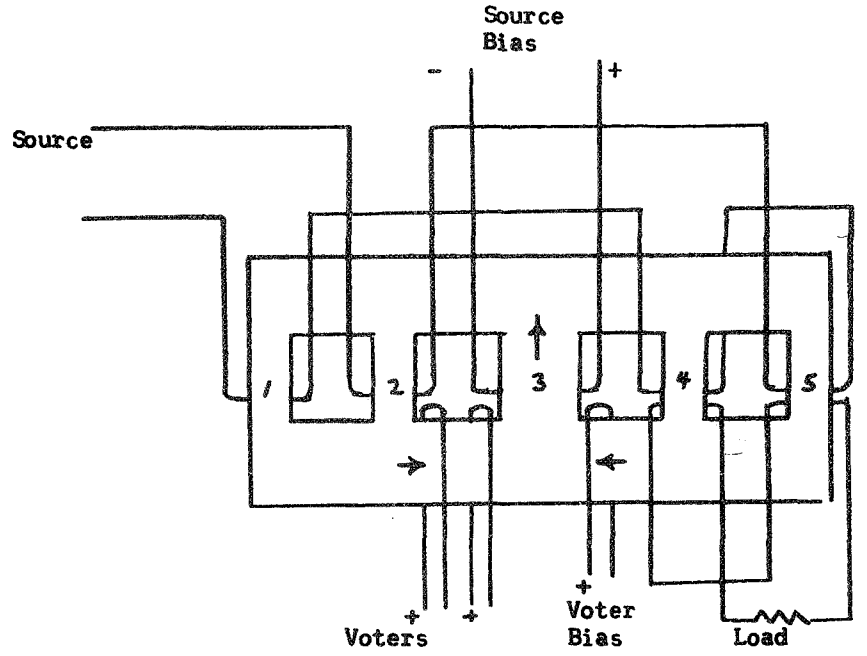


Figure 2-5

Inductor/Transformer Circuit



ON: The two voters are energized. One voter almost overcomes the voter bias mmf and the second voter overcomes it and saturates legs 1 and 2 downward with the flux returning in leg 3. With the saturable inductor saturated and all flux accounted for, legs 4 and 5 act as a conventional two coil shell type transformer that connects the source to the load.

OFF: The two voters are not energized. The voter bias winding saturates legs 4 and 5 downward with the flux returning in leg 3. With the saturable transformer saturated it can couple no power to the load. Legs 1 and 2 are unsaturated and free to act as an inductor in series with the saturated transformer and keeps it from shorting the source. Bias is not essential in leg 3 since the load will provide a bias that insures the voltage is dropped across the unbiased saturable inductor.

Figure 2-6

SRI Switch

2.2.3 Wanlass Paraformer ™

Reference 8-2 describes a parametric transformer that has characteristics that can be used to make an AC switch. The following description is abstracted for the most part from the reference. Figure 2-7 shows the schematic, configuration and governing equation for the device.

Assume that an AC voltage is applied to the input terminals of the device. A flux path is established that flows in the primary and secondary core, but none of this flux links the secondary winding and there is no output. The secondary circuit is an LC tank circuit and if it is excited, it will oscillate at its characteristic frequency. This oscillation can be sustained if the circuit is parametrically pumped by varying the inductance with time at twice the resonant frequency of the tank. This is exactly what the input does as can be seen by following the waveforms of Figure 2-8. The input voltage is shown as a square wave; however, it can be sinusoidal or anything between. The output is always sinusoidal because of the LC tank, and is always shifted 90° since for parametric pumping the voltage magnitude is maximum when the secondary inductance is minimum and vice versa.

Some of the device's interesting characteristics are noted.

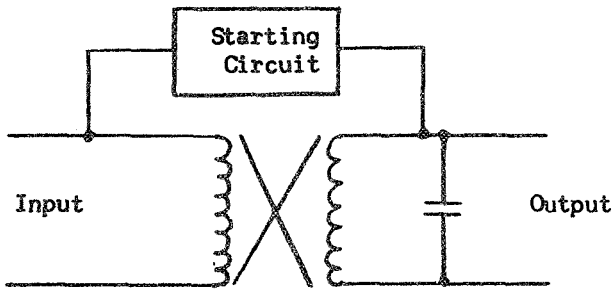
1. It can be seen from the governing equation that no voltage can be coupled unless some secondary current is present. This must be supplied by a starting circuit. Without initial current from this starting circuit, there is no output even with the input present.

2. The device is marketed as a line stabilizer or regulator, the regulating mechanism being similar to that of a constant voltage or ferro-resonant transformer. As such, the output voltage changes as a function of input frequency (a 1% change in input frequency gives about a 1.5% change in output voltage) and load power factor (a change from 0.5 to 1.0 in power factor gives about 1.25% change in output voltage). Also the input power factor is highly inductive varying from about 0.2 to 0.5 depending on load.

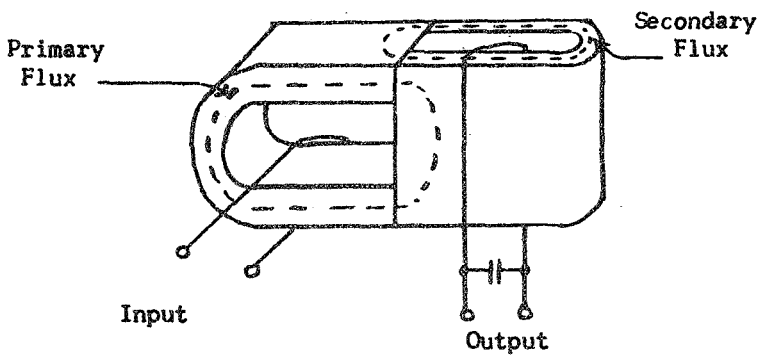
3. The output circuit is a LCR oscillator circuit and will stop oscillating if overloaded by a shorted output, or too low a value of R (overload) that spoils the Q, or a shorted or open capacitor or inductor. This gives the device desirable failure modes and a method of turning it off. Oscillations also cease if the input frequency and resonant frequency are not within a few percent.

4. An AC (or DC) voltage applied to the output will not couple to the input. It can modulate the primary reluctance but since there is no flux coupling or input capacitor their is no coupling mechanism. The device is unilateral in operation. It can be made bilateral by adding an input capacitor.

5. Typical efficiencies for a 500W unit would be 88 percent at full load and 75 percent at half load.



a) Schematic



b) Physical Configuration

$$E = \frac{d}{dt}(Li) = \underbrace{L\frac{di}{dt}}_{\substack{\text{Flux coupling}\\ \text{Term} = 0}} + \underbrace{i\frac{dL}{dt}}_{\substack{\text{Parametric}\\ \text{Coupling Term}}}$$

c) Governing equation

Figure 2-7

Paraformer Characteristics

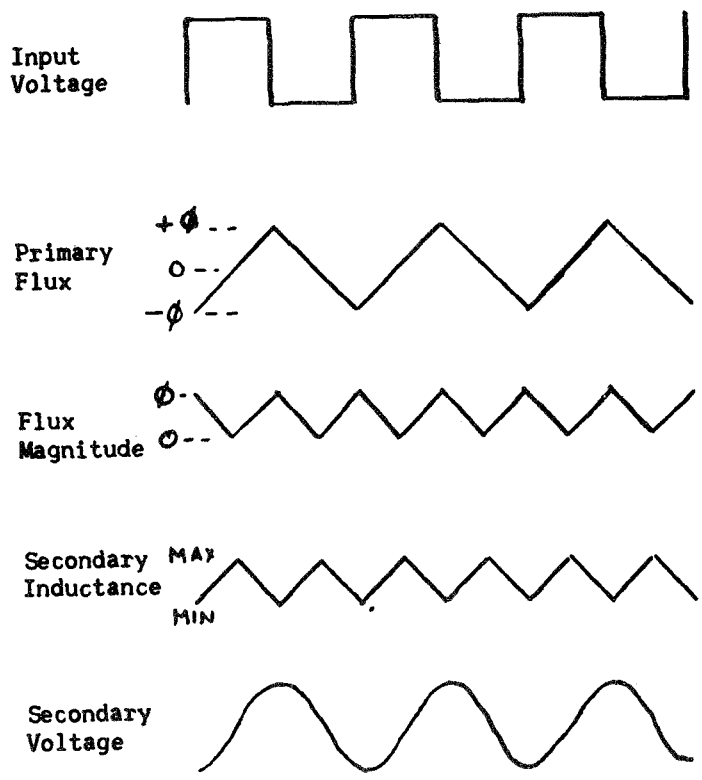


Figure 2-8

Paraformer waveform relations

6. The magnetic structure is typically about twice the size of a conventional transformer of the same frequency, VA, and temperature rating. To this must be added the resonant capacitor which must be stable with temperature and age. The total size penalty is about 3 times that of a conventional transformer with a weight penalty of about 2.5 times.

The failure characteristics are as follows:

1. When the circuit stops oscillating, it draws little power from the source and delivers none to the load. The circuit stops oscillating if:

   a. Capacitor opens or shorts or drifts excessively

   b. Input voltage increases or decreases excessively from nominal

   c. Input frequency increases or decreases moderately from nominal

   d. Load shorts or becomes excessive

   e. Secondary turns short to each other

   f. Core characteristics change radically.

2. The circuit passes no energy from an active load to a shorted input bus.

3. The probability of a primary to secondary short are very much less than in a conventional transformer since they are separated by inches rather than mils. Also an insulated core gap can provide one more barrier for primary to core to secondary shorts. A primary to secondary short can occur through the starting circuit, but since this can be low power and short duty cycle, a large measure of redundancy is practical.

2.3 SOLID STATE CONTROL

Reference 8-3 reports on an LTV contract to prove the feasibility of solid state switching for an entire aircraft electrical distribution control network. The following is abstracted from the reference.

Solid state devices cannot be efficiently employed on a part-for-part replacement basis; therefore, the entire electrical system is redesigned. For comparison purposes, two complete simulators are built for observation and test, one with production A-7B electrical hardware and the other with solid state components and a high density harness. The solid state components are being built on LTV contracts to Texas Instruments for signal sources and to Leach for indicator drivers and power controllers. (References 8-4 and 8-5).

Figure 2-9 is a block diagram of the solid state power distribution system from Reference 8-3. The system is composed of three basic building blocks. These are: (1) Signal Sources, (2) Control Logic, and (3) Power Controllers (bus switching and load switching). Signal sources are transducers which provide digital output. They are used to sense controlling functions such as temperature, pressure, mechanical motion, etc. Their output signals are fed into the control logic unit where they are correlated in a prescribed method to provide a signal to control the power controllers. The logic switching is performed by standard integrated circuit gates. The fan out capability normally provided by multiple pole switches and relays is provided by the integrated circuits. The flow of power from the power sources to the bus and from the bus to the loads is controlled by power controllers.

The characteristics of the LTV power controllers are listed in Tables 2-3, 2-4, and 2-5.

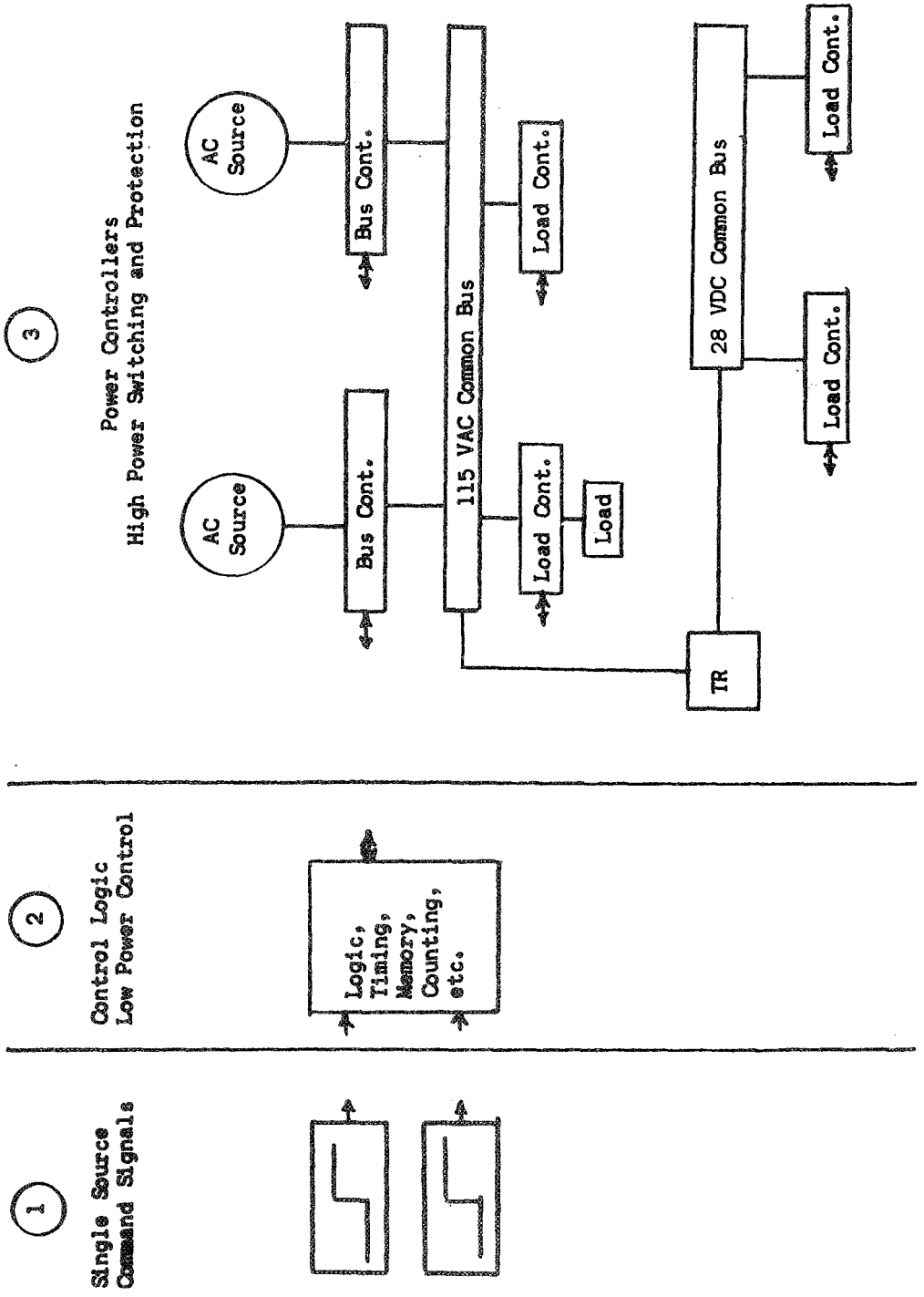


Figure 2-9

LTV Solid State Power Control System

TABLE 2-3 AC LOAD CONTROLLER CHARACTERISTICS

Normally Open SPST

Voltage: 115/200 VAC ± 5% with Mil-Std-704 transients

Frequency: 400 Hz ± 5% No transients specified

Control voltage: OFF -10V to 2.5V ± 100V transients
ON 3.5 to +10V ± 100V transients

ON-OFF response time: One Cycle

Typical trip characteristic: 130% Overload, 5.12 sec; 2000% Overload, 1.25 msec.

Temperature: -54°c to 120°c Case

Wire list:
Power In
Power Out
Control
Trip Indicator
Reset
Signal GRD
Power GRD

Voltage drop: 1.5 VRMS Max.

Physical - 1-10 Amp rating: 1.015 x 1.015 x 1.015 inches with mounting studs and terminals extending 0.375 inches: 2.0 oz max. wt. 0.5° c/w thermal resistance.

- 15-35 Amp rating: 2.5 x 1.515 x 1.3 inches plus 0.375 for studs and terminals: 5 ox max. wt. 0.25° c/w thermal resistance.

Electrical -

Current Rating amps	Fail Safe Current amps	ON Power Watts	OFF Power Watts
1	10	1.75	0.311
2	30	3.25	0.311
3	30	4.75	0.311
5	30	8	0.311
7.5	60	11.75	0.311
10	60	16	0.311
15	90	25	0.311
25	150	40	0.311
35	210	50	0.311

TABLE 2-4 AC BUS CONTROLLER CHARACTERISTICS

Normally Open SPST

Conditions not stated are the same as the load controllers.

Trip characteristic (overload): 200% for 10 sec. maximum

Wire list:
Power In
Power Out
Control
Lookout
Signal GRD
Power GRD

Current Rating amps	ON Power Watts	OFF Power Watts	Thermal Resistors °c/w	Oz. Weight	Size
10	15.1	0.31	0.25	5	2.5 x 1.515 x 1.3 in +0.375
75	120	0.50	0.10	10	2.5 x 1.0 x 3.8 in Total

TABLE 2-5 DC LOAD CONTROLLERS

Normally Open SPST

Voltage: 21-29 VDC with Mil-Std-704 transients.

Control voltage: OFF -10V to +2.5 VDC ± 100V transients
+3.5V to +10V ± 100V transients

Turn on time: 1 ms max.

Turn off time: 6 ms max.

Voltage drop: 0.5V max.

Current limiting: 130 to 150% rated current

Trip out time: 3 sec. max. 1 sec. minimum at 28 VDC

Temperature: -54°c to +120°c case

Wire list: Power In
Power Out
Control
Trip Indicator
Reset
Signal GRD
Power GRD

Current Rating	Fail Safe Current	Power	Power	Leakage MA	
1	10				1.075 x 0.710 x 1.015 + 0.375: 1.803 oz
2	30	2.0	0.156	0.5	1.075 x 0.710 x 1.015 + 0.375 in
3	30	2.5	0.158	0.5	2 oz max.
5	30	4.5	0.164	0.5	0.5°c/w
7.5	60	6.5	0.174	1.0	
15	90	12.5	0.192	1.5	1.515 x 7.3 x 1.515 + 0.375 in.
25	150	22	0.220	2.5	5 oz max.
35	210	31	0.248	3.5	0.25°c/w

The use of solid state controllers has been proposed for F-111, SST, F-15 and B1 aircraft with the result that several specifications have been written for these devices (Ref. 8-4, 8-6) and some hardware is available and being qualified. The technology should be well developed within the time frame of the space station.

The failure characteristics are as follows:

AC controllers usually use solid state thyristors (silicon controlled rectifier, SCR) as the control element. DC controllers usually use transistors. Since the normal catastrophic failure mode of both junctions is a short, a series fuse link is often included that opens at several times the rated current. This is essential in the space station application. Besides the main control element, the controllers contain a rather large amount of additional circuitry for logic, timing, current limiting, switch drive, and bias. The failure characteristics of the total controller is highly dependent on this circuitry. It is doubtful if any presently designed controller would meet the failure requirements of the space station guidance and control subsystem. It is highly probable that they could be modified or redesigned to meet the desired characteristics.

The AC devices are bilateral; they will pass power from an active load to a shorted bus if on. The DC devices are partially bilateral; they will pass power from an energized load to a bus after a breakdown threshold is reached.

2.4 ELECTROMECHANICAL CONTROLLER

Electromechanical relays with demonstrated MCBF (Mean Cycles Before Failure) of 10 million cycles at a confidence level of 90% are available (Ref. 8-7), but are limited by rated life to 100,000 cycles or less at which time they must be replaced. The emphasis of this study has been on solid state devices that are capable of a million or more operations. Since the design goal of the programs developing solid state controllers is to increase reliability and maintainability by an order of magnitude and reduce weight and volume by 50% (Ref. 8-8), this emphasis seems valid.

3.0 SYSTEM ASPECTS OF POWER CONVERTER DESIGN

3.1 INTRODUCTION

Power converters are simply buffer circuits that provide power with characteristics required by the load from primary power sources with characteristics imcompatible with the load.

Good system design consists of trying to eliminate the power converter by matching primary power and load characteristics by modifying one or the other or by providing the required conversion with the least impact on power consumption, size and weight, reliability, dollar cost, program risk and schedule. How to assess the system impact of a power converter is discussed.

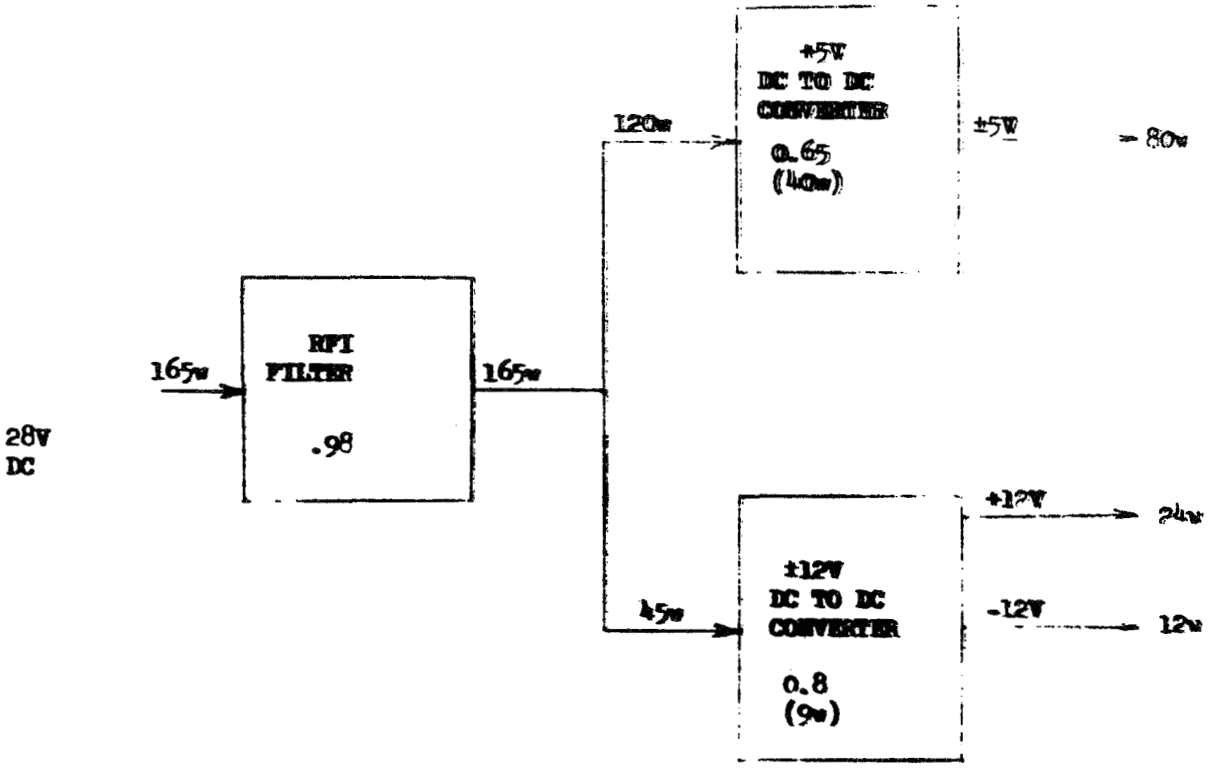
3.2 ASSESSING THE NEED

Almost any experienced power supply designer or system engineer can recall instances of a system design where unnecessary power conversion was provided such as an AC to DC conversion followed by a DC to AC conversion or cases where the required characteristics were grossly over-specified. Eliminating unnecessary power conversion and unnecessary features on the necessary power converters can contribute greatly to overall system design improvement.

3.3 EFFICIENCY MODELS

Figures 3-1, 3-2, and 3-3 show simplified efficiency models. Figure 3-1 is for a DC to DC converter providing three DC levels from a 28 VDC source. Figure 3-2 converts this to an AC to DC converter by adding a transformer rectifier set that converts 115 VAC to 28 VDC. Figure 3-3 shows a high voltage AC to DC converter where the transformer is eliminated and rectification is at a higher voltage. Weight, volume and efficiency are all improved. The figures illustrate the use of such models to determine the overall efficiency of a system, the input power, and the distribution of power dissipation needed for thermal design. Am important effect to notice is the reduction in efficiency as more elements are added in series, even if these elements themselves are reasonably efficient.

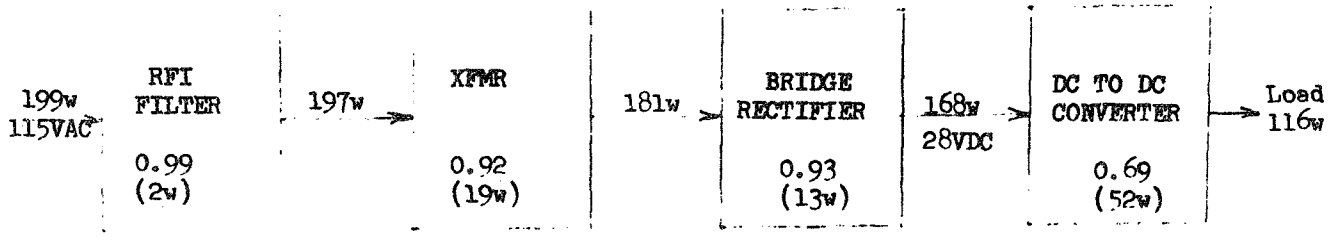
These series elements are multiplying factors and quickly reduce the efficiency of a system. Other losses, such as housekeeping circuits are added in at the appropriate point in the model and are pure losses since they contribute nothing to output power. Efficiency is calculated at nominal input and output voltage and full rated load. The model may have to be calculated for other conditions such as high line input voltage to determine the maximum thermal load in each block.



$$P_{in} = \frac{\left[\frac{80w}{0.65} + \frac{36w}{0.8}\right]}{0.98} = \frac{120w + 45w}{0.98} = 168w$$

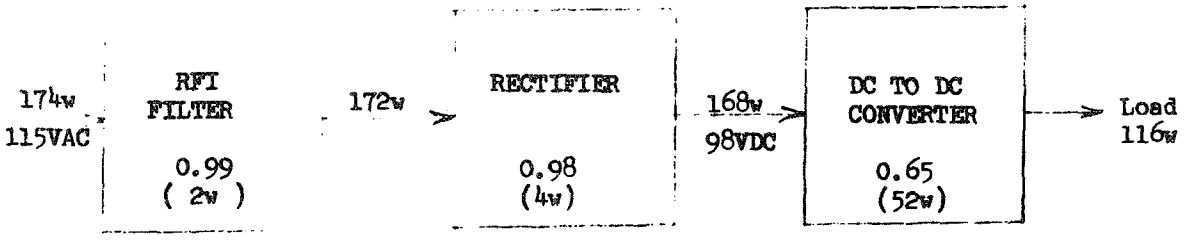
$$\eta = \frac{P_o}{P_I} \; 100 = \frac{116w}{168w} \; 100 = 69\%$$

Figure 3-1 DC to DC Converter



$$\eta = (100)\ (0.99)\ (0.92)\ (0.93)\ (0.69) = 58.5\%$$

Figure 3-2 AC to DC Converter



$$\eta = \frac{116w}{174w}\ 100 = 66.5\%$$

Figure 3-3 AC to DC Converter

3.4 EFFICIENCY MODEL PARAMETERS

3.4.1 Switching Regulators

Figure 3-4 is a plot of the equation

$$\text{Efficiency} = \frac{E_o}{X + E_o} \qquad \text{Versus } E_o$$

where E_o is the output of the regulator and X is a voltage in the range of one to four volts. For switching regulators in the low to 500W range and frequencies between 5KHz and 25KHz the efficiencies seem to fall between the lines determined by X = 2 to 3 volts. If it falls outside the X = 3V line, the designer usually didn't pay sufficient attention to power losses or traded off efficiency for some other parameter. While you might expect a good design to approach the X = 1V line, the 1 volt being the drop across the switching transistor or commutating diode, in practice it seldom penetrates the X = 2V line. The losses occur as switching losses, core losses, series IR drops and power required for the control and drive circuitry.

3.4.2 Series Dissipative Regulators

Basic efficiency is estimated by multiplying the value obtained from Figure 3-4 with X between 1 and 2 volts by the following factor

$$a = \frac{\text{Minimum Input Voltage}}{\text{Nominal Input Voltage}}$$

For example, if the input voltage has a tolerance of +10% and -20%

$$a = \frac{\text{Vnom} - 0.2\ \text{Vnom}}{\text{Vnom}} = 0.8$$

and the efficiency for a five volt regulator would be

$$(0.75)(0.8)(100) = 60\%$$

3.4.3 Shunt Dissipative Regulator

For maximum efficiency, the input voltage to the regulator is determined by the equation (reference 8-9).

$$E = v\,\frac{1 + \sqrt{1-a}}{a}$$

where v is the output voltage and a is defined as before. The maximum efficiency is then

$$N = \frac{v}{E}\ 100 = \frac{a}{1 + \sqrt{1-a}}\ 100$$

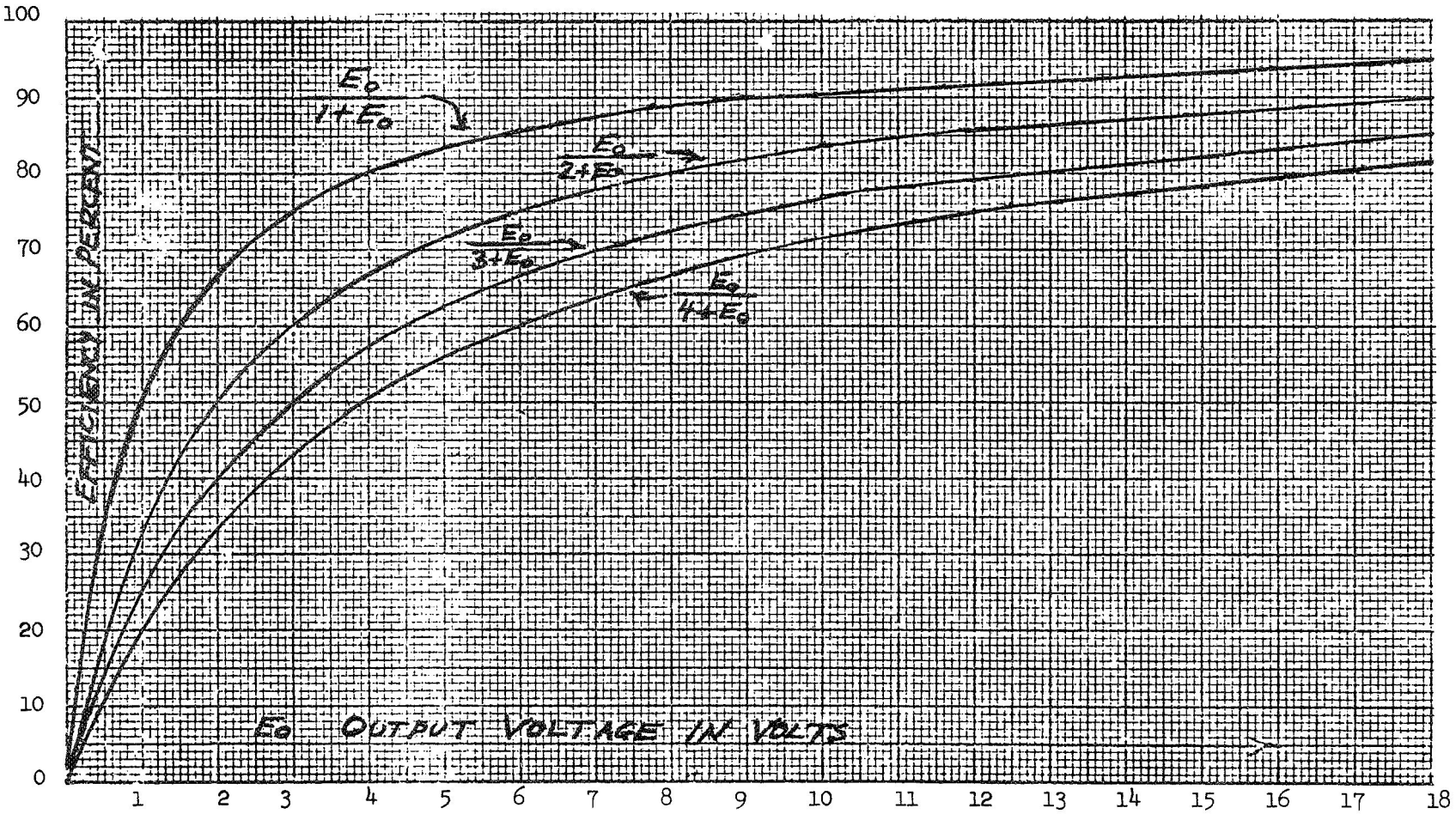


FIGURE 3-4. EFFICIENCY VS. OUTPUT VOLTAGE

which must be modified by an estimate of control losses. In practice, a shunt regulator is always less efficient than a series regulator or at best the same efficiency.

3.4.4 RFI Filter

$$N = 100 \frac{E_{in}}{X + E_{in}} \quad \text{where } X = 0.5V \text{ to } 2.0V$$

Within the limits of X there is a size-weight trade-off with efficiency, with the more efficient filter being larger.

3.4.5 Marginal Test Capability

Some computers incorporate a trouble shooting scheme in which the secondary output voltage is varied high and low by some percentage as an aid in locating marginal logic circuits. If dissipative regulators are used, the efficiency is lowered by

$$N = a \quad \text{where a is defined as before.}$$

For example, if $\pm$ 5% marginal test is desired, $a = 0.95$

3.4.6 Remote Sensing

The need for remote sensing usually indicates a poorly designed or unknown distribution system. If used with switching regulators, the efficiency loss is only that in the actual bus, if used with dissipative regulators the maximum bus drop must be designed for and is always lost, either in the bus or regulator.

$$N = a = 0.95 \quad \text{for a 5\% drop in the bus.}$$

3.4.7 Overcurrent Protection

Assuming that current is sensed by a series resistor, use Figure 3-4 with $X = 1.0 \pm 0.5V$. Losses can be lowered with the use of a current sensing transformer or other devices.

3.4.8 Power Sequencing

The need for this should serve as a warning flag to the system engineer that he may have a problem. It usually means that either circuitry will be destroyed or information lost if not sequenced properly. Since electronic sequencing circuitry can often be thrown out of kilter by randomly turning the input voltage on and off (for instance, relay chatter), it is highly likely that it will occasionally happen. Another problem is that different loads may require different, and totally incompatible, sequencing. The efficiency cost is usually only in the housekeeping circuitry needed.

3.4.9 Isolation of Grounds

Ground isolation can be obtained for no efficiency loss if transformers are needed anyway. If not, the isolation losses must be considered. For an unregulated DC to DC converter, they can be estimated from Figure 3-4, using X = 1 volt for each series switching transistor on the primary side, multiplying by the transformer efficiency, and using X = 1 volt for each series rectifying diode on the secondary side. For example, a 28V to 28V parallel inverter with center tapped secondary and a 96% efficient transformer would be N = (0.965)(0.96)(0.965) 100 = 89% efficient. A bridge inverter with a bridge output and the same transformer would be N = (0.93)(0.96)(0.93) 100 = 82% efficient.

3.4.10 Transformers

Transformer efficiencies can be estimated from the curves in reference 8-10 Figure 3-5 in the reference gives size versus regulation and temperature rise for 60 Hz transformers. Figure 3-6 is for 400 Hz transformers.

A conservative estimate of power losses can be made by assuming the copper losses equal the regulation, and core losses equal the copper losses. A transformer with 4% regulation would be 92% efficient. Power losses for transformers in the 5KHz to 25KHz range can be estimated as about half those of a 400 Hz transformer.

3.4.11 Input Voltage Tolerance

For input voltage tolerances of ± 10% or less, dissipative regulators are usually preferred because they provide high quality power with no EMI problems and at reasonable efficiency. When the voltage range exceeds this, efficiency considerations make switching regulators more and more attractive in spite of their EMI problems and higher output ripple. Whichever type is chosen, sufficient information has been provided to estimate the efficiency.

3.5 SIZE ESTIMATING

3.5.1 Thermal Constraint

The volume of a power converter should be compatible with its efficiency, i.e., a 65% efficient power converter should occupy 35% of the volume of the package containing the converter and its load. While it is true that the thermal design for a power converter is usually better than for most loads, it often receives the cooling last which negates this advantage.

3.5.2 Output Power Per Cubic Inch Figure of Merit

Often a figure of merit can be used as a guideline to estimate size. One such figure of merit is output power per cubic inch. Table 3-1 lists this figure of merit for several computer power supplies done over a period of eight years by different designers in the same company. All are DC to DC converters operating at 20KHz with output power ranges of 25 to 350 watts. All are conduction cooled with a 71°c upper heat sink limit except the last whose heat sink is less than 40°c.

A reasonable figure of merit for estimating size for this approach seems to be one watt output power per cubic inch. This allows for sufficient component derating and working room to allow for good workmanship and inspection, all of which are necessary for achieving a reliable design.

3.5.3 Component Density

Reliable regulator design requires resistors in two out of three transistor leads and several protection diodes. This requires about twenty to thirty parts per regulator even when IC regulators with booster transistors are used. If many low powered output levels are required, component density may require more volume than the other figure of merits indicate.

3.5.4 Redundancy

Brute force dual redundancy would be expected to double the volume, however, if heat sinking can be shared, substantial savings may be made in required volume.

3.5.5 Transformers

Transformer size can be estimated from Chapter 5 of Reference 8-10.

3.5.6 Rectifier and Filters

These almost have to be rough designed to get a semi-accurate answer. A very conservative estimate is to assume they occupy a volume similar to the transformer. If the filter must provide energy storage for transients, it can become quite large in comparison to what is required for pure ripple reduction.

TABLE 3-1. OUTPUT POWER PER CUBIC INCH FIGURE OF MERIT

Computer	Output Power Per Cubic Inch	Efficiency	Comments
A	0.53	65-82%	Low cost demonstrator Adjustable outputs Seven levels including 200V for Nixies.
B	1.32	73%	Production - Some Producibility Problem due to part density Six levels
C	1.41	76%	Production - Some Producibility Problems due to part density Five levels
D	1.76	72%	Production - Some Producibility Problems due to part density Four Levels
E	0.6	75%	Production - Loose Output Tolerance - Seven Levels Low power
F	6.0	86%	Two pre-production units Cordwood construction Four levels, most power on 28V level.
G	2.88	71%	Production - Two levels Cordwood
H, I	0.87 - 0.97	44%	Production - Twelve levels DC to DC with series regulators Radiation Hardened.

3.6 WEIGHT

A good rule of thumb for power levels less than 500 watts is to assume the power supply has the same density as aluminum - 0.1 lbs/cubic inch. This is perfect for the aluminum heat sinking and chassis and a good average for the heavier copper, iron, and tantalum and the lighter plastics and open air spaces. If it gives a heavier weight than 0.1 lb. per watt of output power, the latter is usually a better estimate.

3.7 RELIABILITY

Power converters have a poor reputation for reliability but they can be designed so that they contribute less than one out of every ten system failures. Reliability is achieved by proper application and derating of components (what are the forward and reverse secondary breakdown traces? - what's the ripple current through that capacitor? - does that include the load?), adequate protection components (i.e., are all source to source or source to ground paths through semi-conductor interrupted with discrete resistors? - were blocking and bypass diodes used, etc?), good thermal design (including minimizing effects of thermal expansion and contraction), and good mechanical design (adequate clearances during vibration and shock as well as statically, not trying to hold down capacitors with their insulating sleeves during vibration, no burrs under that mica washer, were the dimensions of that solder pad designed or guessed at?). Also, good follow-up with ability to change the design to eliminate failure modes is essential. The usual addition of failure rates of components has little to do with actual power converter failure rates. Another factor often overlooked is designing the converter so it can be produced with good workmanship, inspected (can you see every solder joint clearly from several angles, etc.) and reworked without goofing up the original workmanship.

3.8 INTERFACE PRECAUTIONS

Often, power converters are designed without proper consideration of the actual system loads or source characteristics they see. Some common problems are discussed.

3.8.1 Entrainment of Switching Regulators with Switching Loads

If the frequency of a switching regulator is allowed to vary and it drives a load that is also switching at some frequency (i.e., a core memory or I/O bus under software control) and the load frequency approaches that of the regulator switching frequency, the regulator can lock in on the load frequency. The effect is that the peak-to-peak output ripple goes from some reasonable level to an unacceptable level (i.e., 100 mv p-p ripple on +12VDC may go to 8 volts p-p). This can cause havoc with the load and fail power converter components such as output capacitors. The effect is amplitude sensitive, a 100 ma switching load may not entrain while a 200 ma load may. It is interesting to note that most published switching regulator designs have this characteristic.

3.8.2 More Than One Stable Operating Point

Figure 3-5 shows the block diagram of a pre-regulator, with current limiting, driving a switching regulator. The voltage versus current diagram at the interface is shown for both blocks. The two points of intersection are the two stable operating points. One is the desired one and the other is undesired. When the system is first energized, it will come up and latch into the undesired mode.

3.8.3 Voltage Overshoot

Figure 3-6 shows the LC network used on most switching regulators. If a load has established a DC current in the inductor and the load is abruptly removed, all the energy stored as $E = \frac{I^2L}{2}$ in the inductor is dumped into the capacitor as $E = \frac{V^2C}{2}$ energy and the output voltage is

$$V = I \frac{L}{C} = I Z_o$$

Some published designs of switching regulators give an 80 volt overshoot on a 5 volt regulator when the load goes from rated load to no load. The situation is compounded when the inductor current has been established by a short circuit on the output that suddenly burns open. Every IC in some large scale computers has been burned out this way.

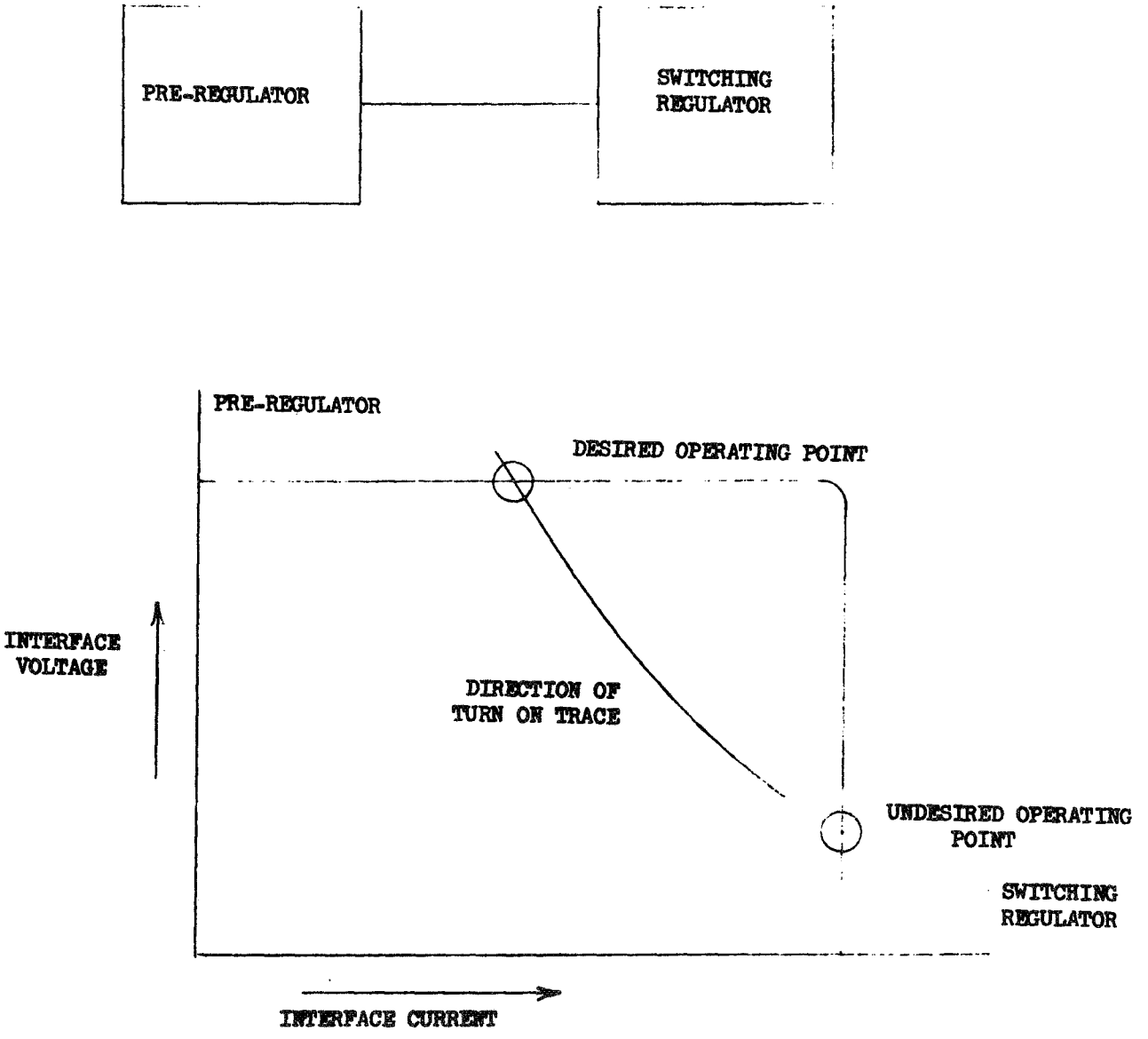


Figure 3-5 Regulator Interaction

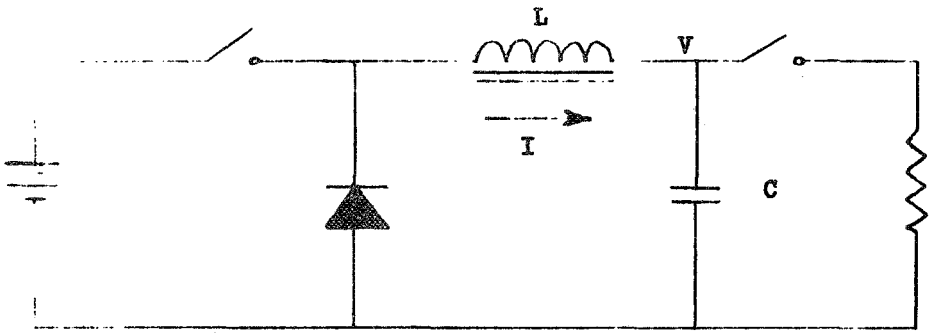


Figure 3.6 LC NETWORK

4.0 REFERENCES

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APPENDIX 9

1.0 DATA TRANSMISSION MEDIUM DESIGN

1.1 GENERAL

1.1.1 Design Considerations

The design considerations for the data transmission system were guided by factors such as reliability, cost, noise environment, etc. Some of these considerations are discussed in subsequent paragraphs as well as the descriptions of the Driver/Receiver mechanizations, data link, and equipment interfaces.

1.1.2 Data Format

The information exchange over the data link consists of data, housekeeping and spare bits and employs the processes of multiplexing, timing, storage and switching. The data exchange between major system elements employs bi-phase (Manchester) encoded data to allow AC coupling and enhance noise immunity.

Long paths (100 feet is considered long) are handled by an AC coupled (transformer) system which features high noise rejection, and DC isolation. Party line, half-duplex operation is employed where all receivers are active but only one transmitter is using the line for any given interval. Two-way transmission is thereby established by time sharing the line.

1.1.3 Noise Environment

The noise environment of the spacecraft is one of the major considerations affecting the design of the system. Noise within the transmission system inside the spacecraft constitute interference in the form of undesirable electrical signals induced from sources which may be either external or internal to the system. Random noise and impulsive noise are two categories. In addition, there is cross-talk running from other parallel electrical circuits.

At this time very little is known about electrical noise conditions inside the spacecraft, particularly short-term statistical data. Some fundamental assumptions have been made during studies and accordingly, Figure 1-1 has been drawn for a typical environment. It is presumed that the noise measured on a line spanned through the spacecraft might have magnitudes of noise power spectral density lying within the darkened area of the figure.

For purposes of calculations and mechanization, a noise power density of -130 dbw/Hz is assumed. It is likely that the -130 dbw/Hz signal may be in excess of actual noise induced in a well shielded-balanced cable. Using this figure, however, allows an adequate design for signal to noise.

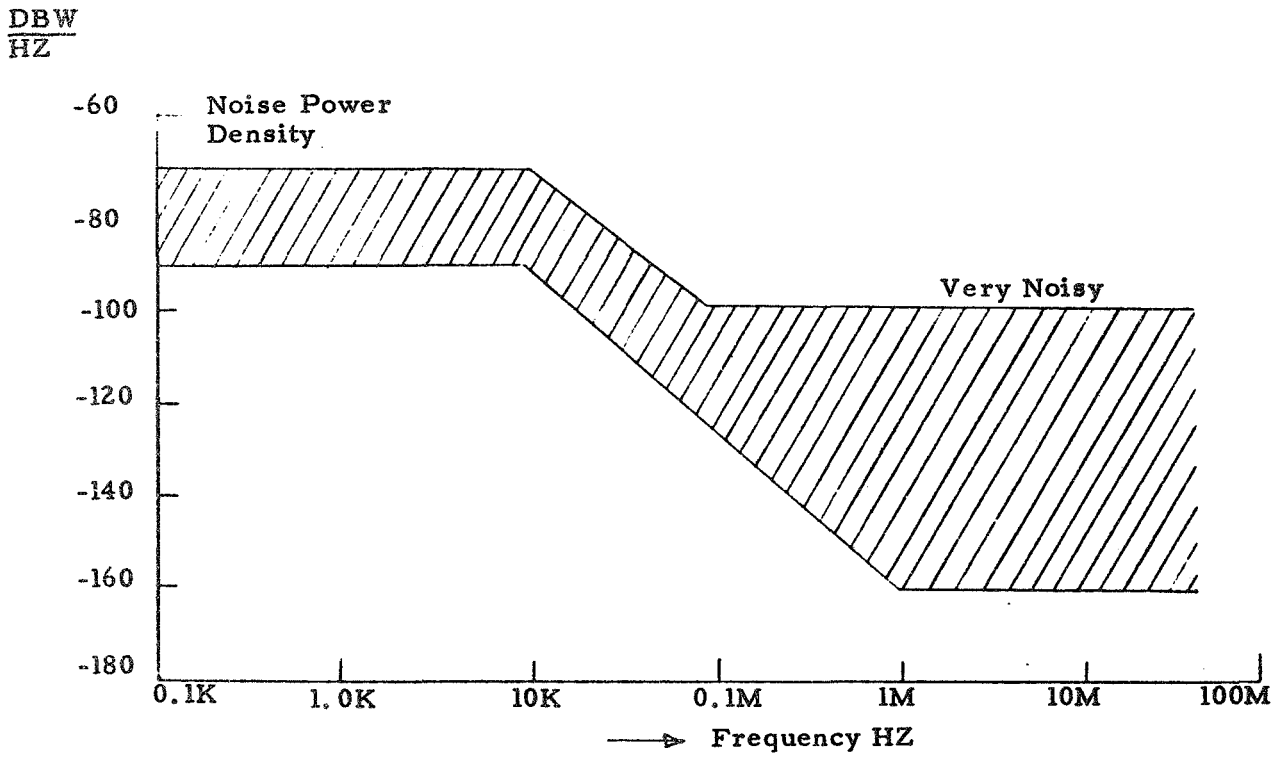

FIGURE 1-1 ASSUMED RANGE OF NOISE SPECTRUM

1.1.4 Bi-Phase Modulation

Bi-phase (Manchester) encoding is employed for the AC coupled signals. Figure 1-2 shows various encoding techniques as well as the one employed. Bi-phase Manchester was chosen because it is simple to generate and decode by using the clock signals.

Baseband bi-phase encoded data features inherent signal-to-noise enhancement over nonsynchronous encodings or transmission of basic data formats such as NRZ. Moreover, encoding to bi-phase allows the channel band to be located above the high noise environment band which is found on all types of modern vehicles. Tests have shown (as depicted in Figure 1-1) that the interfering noise on a transmission path within a vehicle increases inversely with frequency at 40 db/decade, and flattens out below 10 KHz. The knee of the noise curve is discernible at or near 1 MHz. Therefore, the operating band for the nominal 1.0 MHz bi-phase encoded data rate is located in a less hostile frequency spectrum.

Bi-phase modulation also requires less power on the transmission line, for a given error rate, over other systems with data formats utilizing low frequency or direct current band pass response. Bi-phase encoded signals may be isolated from the transmission line by transformer coupling since no DC or low frequency components need be passed. Bi-phase encoding/decoding can be digitally mechanized, and since the use of transformer isolation is allowed, superior common-mode noise rejection results.

1.1.5 Transmission Power Schedule

The power required on the line is dependent on various factors of environmental conditions, coupling losses, noise margins, bandwidth, etc. They are related by the following equation:

$$S = No + BW + E/No + Margins + Losses$$

where;

S = Signal power on line
No = Noise power density
BW = Bandwidth required
E/No = Energy contrast at a given error probability (Pe)

The noise power density is -130 dbw/Hz, taken from Figure 1-1 assuming a medium noisy system at 1 Mhz. The bandwidth required is twice the digit rate because of bi-phase encoding;(or) 10 log (bit rate) + 10 log $(\frac{2 \text{ cycles}}{\text{bit}})$. At an effective bi-phase bit rate of 1 Mhz, the bandwidth required is 10 log 2 MHz = + 63 dB. At a given error probability of 10^{-10} for a bi-phase encoded system, the required energy contrast is + 17 dB. A design margin against impulse noise is assumed at +16 dB.

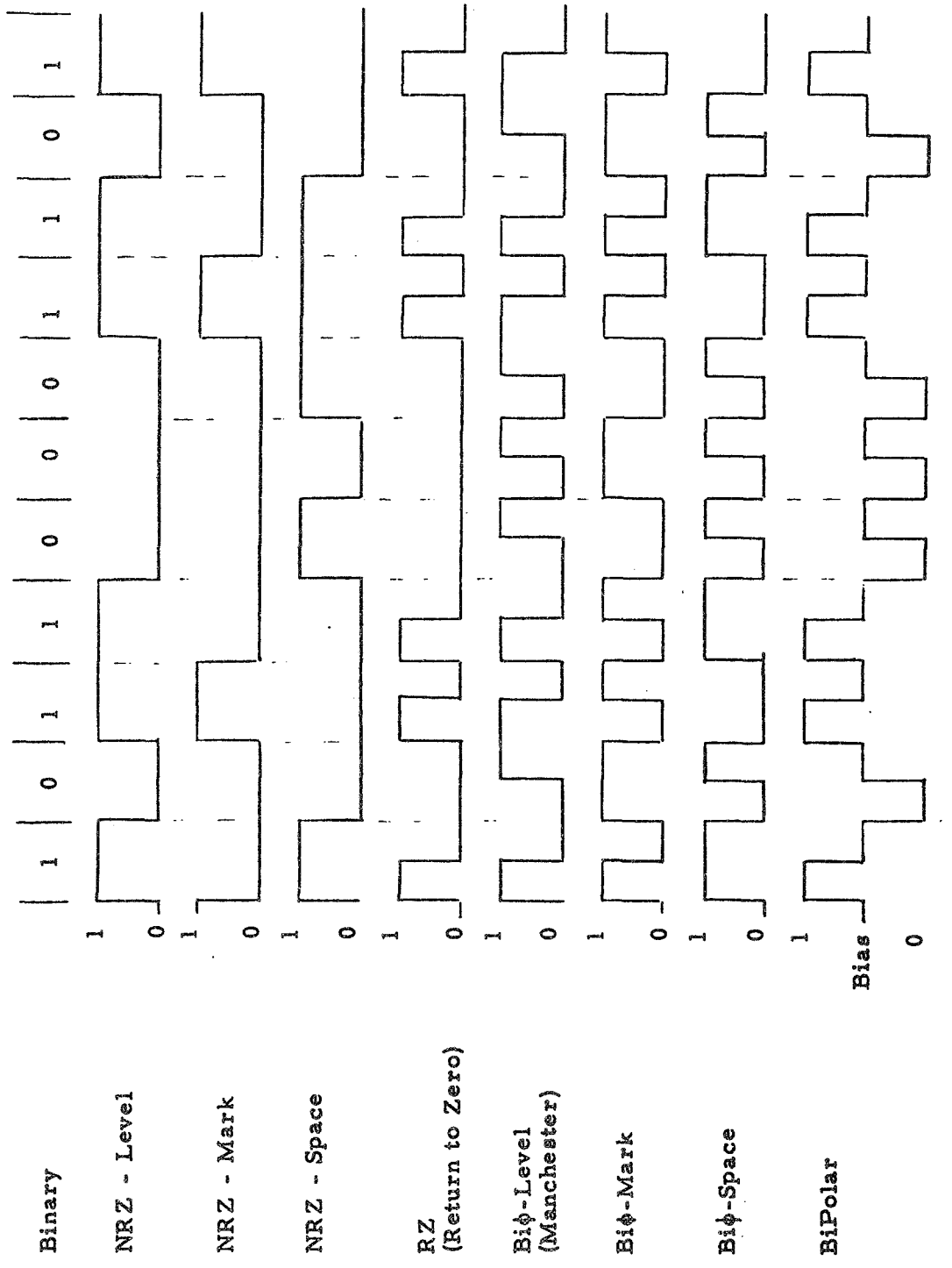

FIGURE 1-2 ENCODING/MODULATION TECHNIQUES

1.1.5 (continued)

Equipment degradation losses are found in the drivers/receivers, connectors, data link, etc. Worst case cable losses are assumed to be +2 dB and connector attenuation losses +3.2 dB (0.1 dB times up to 32 connectors). The driver/receiver and coupler losses are set at +4.8 dB. The total required power on line then is as follows:

$$S = -130 + 63 + 17 + 16 + 10 = -14 \text{ dBw}$$

$$S = -14 \text{ dBw} + 30 \text{ dBm/dBw} = +16 \text{ dBm}$$

This is equivalent to about 40 m watts power required on line.

1.2 MECHANIZATION

1.2.1 Introduction

The mechanization of the data transmission system is treated in two parts including the data link and AC coupled systems.

1.2.2 Data Link

The noise spectrum influences the design of a data transmission system concerning frequency and band allocation as well as the system of modulation. Since crosstalk is principally an inductive effect, the magnitude of this noise problem increases with the length of adjacent electrical circuits, the field-strength of the crosstalk energy, and the frequency of the transmitted signal. Crosstalk interference is greater in carrier systems since high frequencies are used, and induced EMI is a function of frequency.

The crosstalk problem is greatest for long wire circuits consisting of several adjacent paired conductors, since there exists a long path of parallel electrical circuits, unless there is shielding between them. Shielding methods and isolation techniques for electrical conductors greatly reduce the problem of crosstalk.

A good cable is a two-conductor twisted and balanced transmission line with an overall shield around both conductors. Twisting the two balanced signal carrying wires provides high common mode noise rejection thereby protecting against a low frequency magnetic noise field. When used properly it also provides protection against ground loops and capacitive fields.

The selected transmission cable has maximum impedance of about 110 ohms, is well-balanced, has twin-twisted and shielded conductors, and is small and lightweight. Both terminal ends of the cable are loaded in the cables' characteristic impedance resulting in low VSWR. The loads are center-tapped and grounded for noise drain. Low VSWR, with

1.2.2 (continued) - good balance maintained for drain, results in minimal susceptance and emission of EMI for the transmission cable. Moreover, all data transmit/receive equipments are differential high impedance bridging taps along the cable. Minimum bridged loading is maintained for each tapped element, thereby, the cable retains good drain balance and low VSWR as equipments are added or reduced from the line.

The attenuation of the cable is less than 1 db/100' at 1 Mhz and the propogation delay is less than 2 nanoseconds/foot.

1.2.3 AC Coupled Transmit/Receive (Figure 1-3)

1.2.3.1 Transmitter - The transmitter is a signal current source, which exhibits a 1500 ohm or greater bridging load at a transmission cable tap. A well-balanced, isolation transformer couples the transmitter output stage to the cable tap and bridging is maintained for either the operate or inhibit mode of the transmitter. Current drive allows the secondary of the transformer, feeding the line, to have some additional physical bridging resistors placed in series with the signal path without deleterious signal loss. Upon catastriphic failure of any one transmitter output circuit, signal paths for the remaining data communication elements are not seriously impaired.

The transmitter output stage is an IC consisting of a balanced differential transistor pair, fed by a DC current source. Current source biasing is derived within the IC. Differential bi-phase data is AC coupled to the transistor pair whose output collectors couple the line and series bridging resistors via a wide-band, well-balanced, isolation transformer. The transmission is inhibited by placing a data level low to the current source section of the IC. High bridging impedance is derived for operate or inhibit mode. Bi-phase data is differentially, AC coupled to two data inputs. Differential data coupling and inhibiting eliminates unwanted transients coupling to the transmission cable. The transmitter is capable of 1.0 MHz bi-phase encoded data rates and +16 dBm into a 60 ohm resistive load.

1.2.3.2 Receiver - The receive elements are bridged from a line tap, using mechanization similar to the transmitter. The receive isolation transformer which features high common mode noise rejection feeds a signal band-pass filter. This element rejects the out-of-band noise which is not common mode. The filter has sufficient pass to include the significant bi-phase spectural components along with a delay distortion characteristic sufficiently low to cause a low data error rate in the vehicle noise environment.

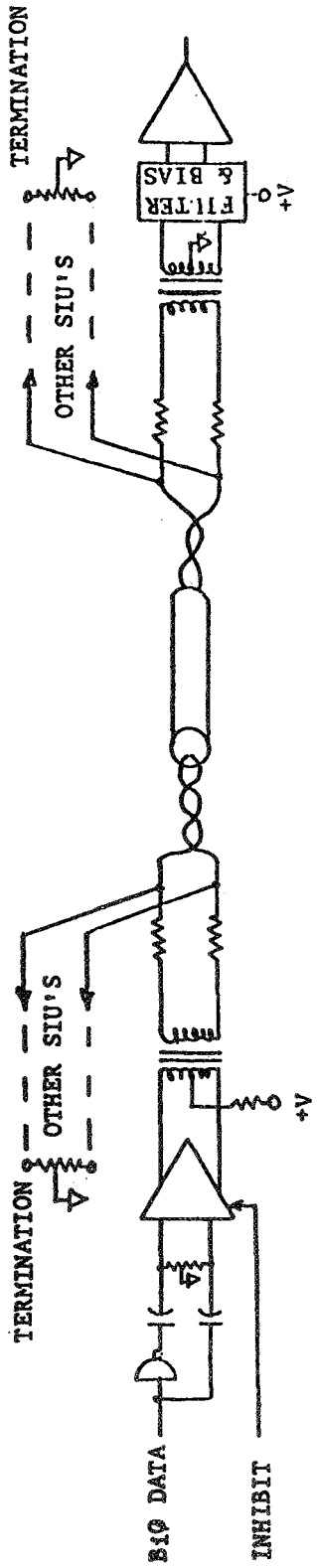

FIGURE 1-3. AC COUPLED PARTY LINE MECHANIZATION

1.2.3.2 (continued)

The filter output is connected to the input of an IC, which has a high impedance input differential transistor pair fed by a current source. Signal amplification is performed and then it is converted to the data level which appears at the IC output.

The receiver is capable of responding to 30 mv levels (crest-to-crest) from a balanced signal source and provide a bi-phase encoded data rate of 1.0 MHz. The fan out is one gate.