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SHUTTLE BIT RATE SYNCHRONIZER

FINAL REPORT

DECEMBER 1974

Prepared For

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
LYNDON B. JOHNSON SPACE CENTER
HOUSTON, TEXAS

Under Contract No. NAS 9-14021

TRW

ONE SPACE PARK, REDONDO BEACH, CALIFORNIA 90278

TRW No. 7333.3-360

SHUTTLE BIT RATE SYNCHRONIZER

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by

D. C. Huey

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ABSTRACT

A Shuttle bit rate synchronizer brassboard unit has been designed, fabricated, and tested that meets or exceeds the contractual specifications. The bit rate synchronizer operates at signal-to-noise ratios (in a bit rate bandwidth) down to -5 dB while exhibiting less than 0.6 dB bit error rate degradation. The mean acquisition time has been measured to be less than 2 seconds. The synchronizer is designed around a digital data transition tracking loop whose phase and data detectors are integrate-and-dump filters matched to the Manchester encoded bits specified. It meets the reliability (no adjustments or tweaking) and versatility (multiple bit rates) of the Shuttle S-band communication system through an implementation which is all digital after the initial stage of analog AGC and A/D conversion.

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ACKNOWLEDGEMENT

We wish to acknowledge the contributions of Mr. Harold Vang, the NASA technical monitor, and also extend our appreciation to Dr. Bart Batson and Mr. Jack Johnson of NASA for their interest, encouragement, and on-going comments during the program.

The basic design and implementation techniques of the Shuttle bit rate synchronizer were derived from a previous digital bit synchronizer project at TRW Systems which was managed by Mr. Al Cellier. Mr. Cellier provided much of the technical guidance to the development of both bit synchronizers. Mr. Lit Ma, the project engineer, conducted the day-to-day technical and project management for both bit synchronizers, and Mr. Mike Wiedner was responsible for the systems analysis of the TRW bit synchronizer and initiated the analytical effort for this project.

Special acknowledgement is due to Prof. William C. Lindsey of USC and LinCom, Inc. Dr. Lindsey was consultant to TRW on this project and contributed heavily in the formulation of the system concepts.

Other members of TRW Systems contributing to the success of this project include Dr. G. Fultz, who was responsible for the system analysis, and also Mr. Don Secor; Mr. Doug Huey who performed the integration and test as well as leading the logic and circuit designers, Mr. Harry Keches and Mr. Tom Cooper; and Mr. Ray Cheung who developed the test set with the assistance of Mr. Dan Eddow.

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1. INTRODUCTION

This final report summarizes the design, development, and test of a bit rate synchronizer brassboard model for the Shuttle program. The unit is designed for repackaging with minimum effort into a flight model for use in the uplink on-board portion of the Shuttle communications and tracking system as shown in Figure 1-1.

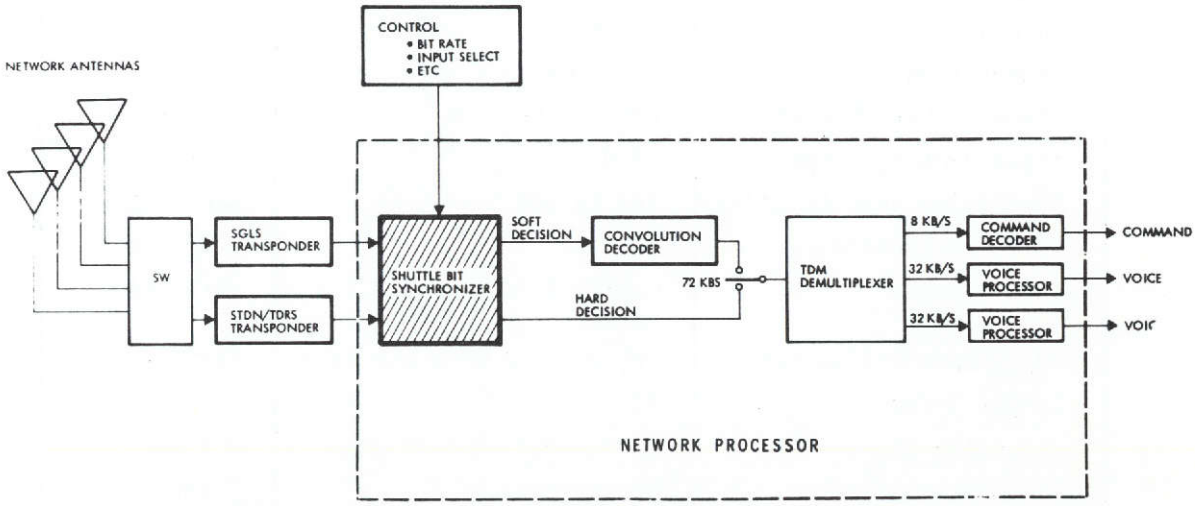


Figure 1-1. Bit Synchronizer Interface with Shuttle

The bit synchronizer brassboard unit is shown in Figure 1-2. The performance requirements and the measured results are summarized in Table 1-1. The test set used to establish performance is shown in Figure 1-3. Each is packaged in a standard 19-inch rackmount type drawer for testing and evaluation convenience in the laboratory.

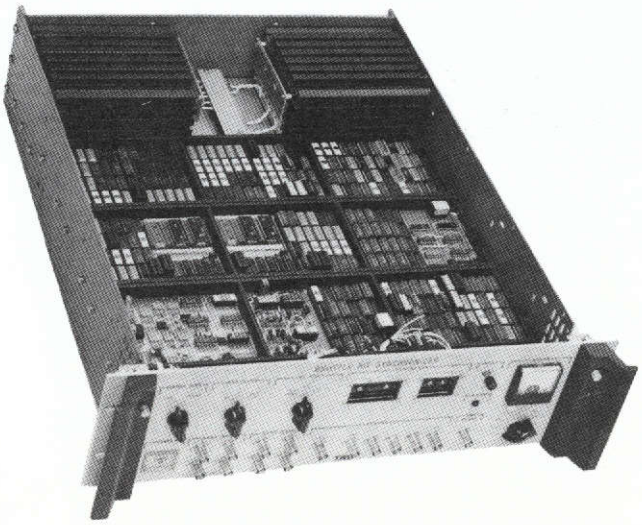


Figure 1-2.
Shuttle Bit Synchronizer
Brassboard Model

Table 1-1. Requirements vs Measured Performance

Parameter	Requirement	Measured
Symbol rate	216K bits per second	Verified
Symbol waveform	Biphase-L (Manchester)	Verified
Threshold SNR (E_b/N_o)	-5 dB	-7 dB
Video bandwidth	Ten times bit rate	Verified
Channel characteristic	White, Gaussian	Verified
Input dynamic range	20 dB	Verified
Transition density (MHz)	10% to 90%	Verified
Rate uncertainty	500 ppm	1000 ppm
Input jitter	0.01%, 1 Hz to 0.1 x bit rate	Verified
Input baseline variation	1%, dc to 0.01 x bit rate	Verified
Output jitter	1%	0.9%
Detection degradation	0.8 dB max (0.5 dB goal)	0.6 dB
Acquisition time	10 sec max	2 sec

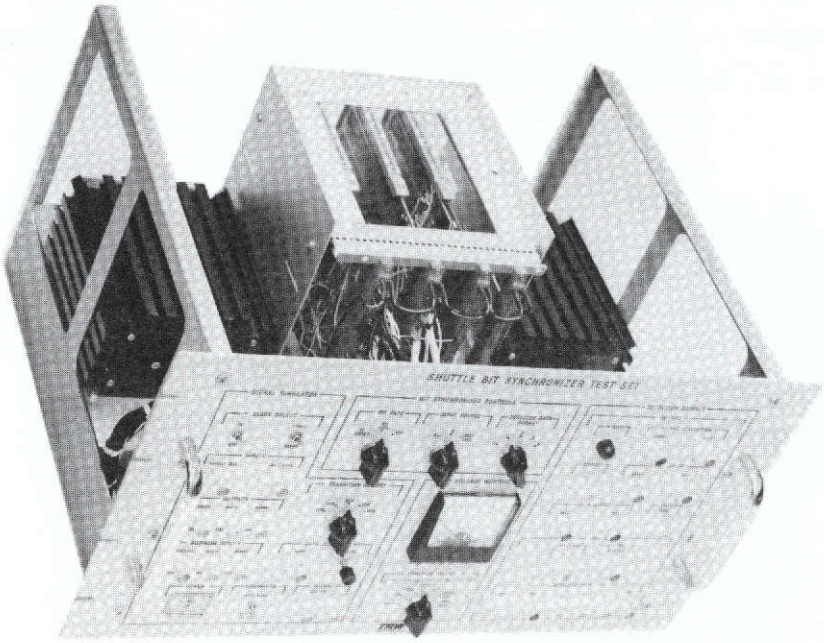


Figure 1-3. Bit Synchronizer Test Set

The primary objective of the program has been fully realized with the design and implementation of a symbol synchronizer which acquires and detects coded Manchester symbols at 216K samples per second, with hard-decision bit error rate degradation of typically 0.6 dB from theoretical, at signal-to-noise ratios in the bit rate bandwidth (E_b/N_0) as low as -7 dB. The design is readily adapted to flight applications, as it is largely digital and features a high proportion of low power MSI CMOS logic. The soft-decision data output (with switch-selectable format, quantization, and thresholds) has been tested with a TRW-built convolutional decoder (rate 1/3, K = 7). An overall synchronizer-decoder coding gain of 4.2 dB (0.7 dB from theoretical) has been demonstrated. Figure 1-4 (discussed in Section 4.3.8) summarizes this significant result.

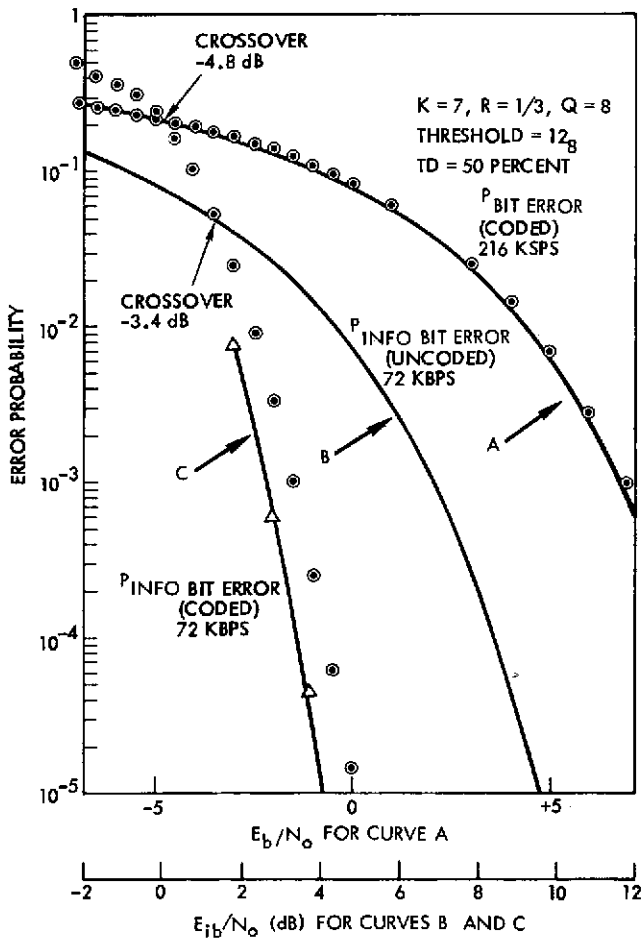


Figure 1-4. Bit Error Rate Performance of Combined Bit Synchronizer-Convolutional Decoder

The capability of this bit synchronizer represents a new benchmark of performance for units operating in this range of SNR's, bit rates, and frequency uncertainties. The application of modern digital processing technology is the key to these achievements. After analog AGC, the signal is sampled and quantized by an A/D converter; all subsequent processing occurs as digital computations. Traditionally, bit synchronizers have been designed for uncoded systems and have operated at reasonably high SNR's, e.g., 7 dB or higher. Even these conventional units require great care in design and packaging in order to achieve near-optimum performance, because analog components suffer from inaccuracies, drift, offsets, leakage, and nonlinearities which vary as a function of SNR, input level, supply voltage, and temperature. Further, operation over wide ranges of data rates requires programmed switching of numerous components, which is both cumbersome and susceptible to the introduction of errors. The all digital technique affords parameter stability, accuracy, and programmability. The freedom from analog inaccuracies permits detection at extremely negative SNR's unachievable with practical analog circuits. A high degree of producibility, with freedom from tweaking and trimming, is also a feature of digital processing hardware.

Synchronization at highly negative SNR's demands accurate estimation of the timing of the received symbols. The minimal processing errors realized with digital techniques are a primary key to successful low SNR operation. Additionally, it is desirable to optimize phase detection and sync-indication algorithms to permit use of maximally wide bandwidths which minimize acquisition time. The synchronizer described in this report features a unique new Manchester transition tracking loop (MTTL), developed from fundamental properties of the Manchester signal. The principles applied are analogous to those of the classical data transition tracking loop (DTTL) originally reported by Dr. Lindsey. The generic MTTL process provides the most efficient phase detection SNR of any sync process identified to date and includes optimization of processing of both midsymbol and potential between-symbol transitions. A further sophistication of the synchronizer brassboard is the application of a separate phase detection algorithm optimized for acquisition; the programmed acquisition-to-track handover sequence includes automatic loop bandwidth switching. Once again, the benefits of digital signal processing are manifested in minimization of stochastic transients in this switching.

The contents of the report include a detailed functional description of each module of the delivered unit and a rationale for the selected approach. A physical description is also included as well as a discussion of the results of the extensive testing performed. This testing established that the contractual performance requirements were met or exceeded.

Additional documents applicable to the work performed under this contract are as follows:

- "Test Set, Shuttle Bit Rate Synchronizer Brassboard," TRW No. 7333.3-354.
- "Shuttle Bit Rate Synchronizer Brassboard Design and Analysis," TRW No. 7333.3-355.
- "Shuttle Bit Rate Synchronizer Operating Manual," TRW No. 7333.3-356.
- "Acceptance Test, Shuttle Bit Rate Synchronizer Brassboard," TRW No. 7333.3-357.

2. FUNCTIONAL DESCRIPTION

The Shuttle bit rate synchronizer has two basic modes of operation: the signal or sync acquisition mode and the synchronous or tracking mode. Each mode has fundamental physical restrictions and characteristics, and the best overall performance is achieved when these two modes of operation are independently processed. The performance measures used in the design include acquisition performance (sync acquisition range and acquisition time) and tracking performance (rms bit sync jitter, bit slippage rate, and bit error probability degradation). The functional elements of the synchronizer considered include phase detector characteristics, lock detector characteristics, and ambiguity resolution circuits, while the basic synchronizer parameters include loop damping, loop bandwidth, and implementation approach.

Figure 2-1 shows a simplified block diagram of the bit synchronizer. The A/D converter samples the incoming signal plus noise 32 times during each bit interval. Subsequent to the A/D converter, all functions are digitally implemented. The top channel is a matched filter for Manchester encoded input from which soft decision outputs are provided to the convolutional decoder. The soft decision can be controlled to provide 3, 4, or 5 bits, quantized with variable step sizes in the scaler. The remaining portion of Figure 2-1 provides for clock recovery with the DTTL phase detector used to extract the transition energy. The data transition detector uses the output of the data channel to remove the data ambiguity. The digital loop filter and digital VCO complete the phase-locked loop which develops a "clean" reference clock for data detection.

A block diagram of the brassboard synchronizer is shown in Figure 2-2. The synchronizer is broken down into four major functional units: the front end, the clock recovery channel, the data recovery channel, and the lock detector. This design, which is almost entirely digital, has evolved from consideration of the following three important constraints:

- The input signal to the synchronizer is Manchester encoded data
- The bit synchronizer performance is to be maintained within 0.5 dB from theoretical for values of the signal-to-noise ratio, E_b/N_o, of -5 dB to +10 dB, with a bit rate uncertainty of 0.05%.
- The output is to be compatible with a Viterbi decoder interface to assure meeting overall detection performance requirements.

A key feature of our design is the digital transition tracking clock recovery loop (DTTL) based upon the DTTL principle originally identified by Dr. Lindsey in 1966. At -5 dB E_b/N_o, this is the most critical element in obtaining near ideal bit error rate performance and rapid acquisition. This unique Manchester-DTTL phase detector extracts timing information both from the between-symbol transitions in essentially the classical manner, and from the mid-symbol transitions which are

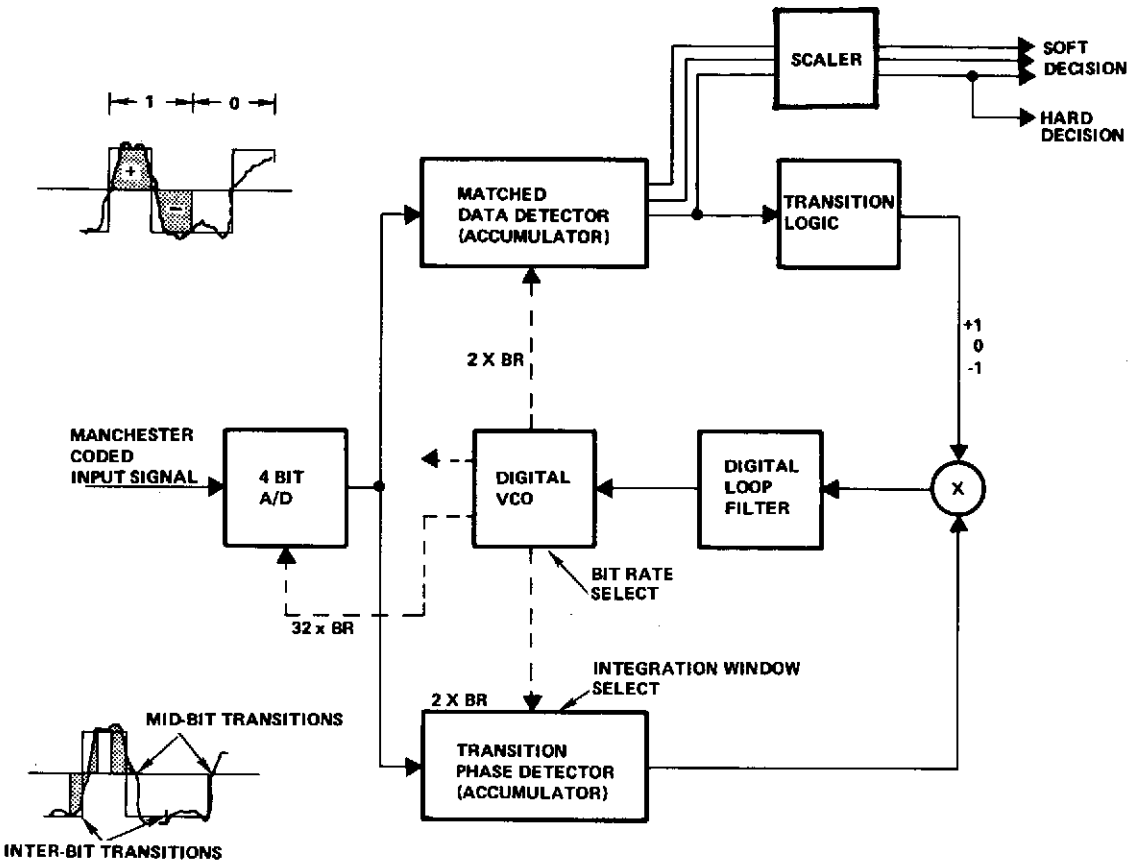


Figure 2-1. Simplified Bit Synchronizer Block Diagram

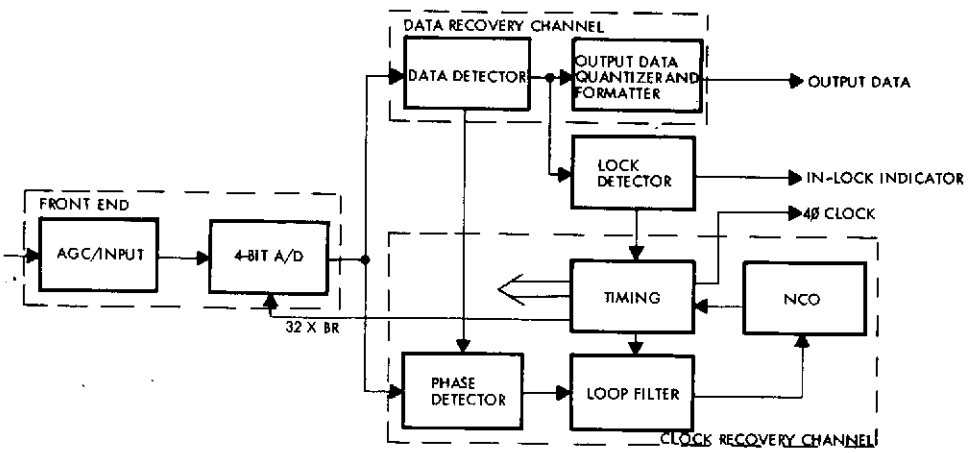


Figure 2-2. Brassboard Synchronizer Block Diagram

corrected for data polarity. The clock recovery loop is essentially a second order phase-locked loop with an all digital implementation.

The front end provides AGC and A/D conversion to normalize the soft decision output against input amplitude variations and to minimize quantization noise produced by the A/D conversion process.

The data recovery channel has two functions: (1) the data detector performs a matched filter operation on the incoming Manchester data and outputs a 9-bit soft decision on each data bit and (2) the output data quantizer provides variable threshold quantization of the soft decision output for NASA's test and optimization of the bit synchronizer - Viterbi decoder performance.

The loop detector has two functions: (1) it establishes that the clock recovery loop has regenerated a clock at the bit rate that is in synchronism with the incoming Manchester data, and (2) corrects the one-half bit period phase ambiguity which Manchester data permits.

The following subsections describe the detailed operation of each block shown in Figure 2-2 and show how the transition from the acquisition mode to the tracking mode is achieved.

2.1 INPUT DATA CONDITIONING AND AGC

The input signal into the bit synchronizer is characterized in the statement of work as follows:

- Bandwidth B of 10 times the bit rate (BT = 10), with a 6-pole rolloff
- Operating E_b/N_o range of -5 to +10 dB in the bit rate bandwidth
- Nominal input level of 2.8 volts p-p and overall dynamic range of 0.5 to 5.0 volts p-p
- $\pm$100% differential baseline variation
- 600 ohm, balanced ac coupled input
- Maximum fault input voltage of $\pm$32 volts dc.

Two important factors were considered in the processing of this input signal: performance is to be maintained within 0.5 dB of theoretical and the bit synchronizer must be compatible with the Viterbi decoder to assure meeting overall detection performance requirements. These requirements necessitate input data conditioning and AGC of the bit synchronizer input signal before it is A/D converted, as shown in Figure 2-3.

A protection circuit and ac coupling provide overvoltage fault isolation and remove dc baseline voltage variations which would otherwise disturb the operation of the AGC and cause clipping of the signal at the A/D input.

The AGC technique implemented is control of the mean value of the rectified signal-plus-noise in the input bandwidth (10 times the bit rate). The output voltage of the AGC amplifier is half-wave rectified (absolute value), compared to a reference voltage, and lowpass filtered in a 100 Hz bandwidth to produce a control signal for the amplifier. This mechanization produces an output voltage controlled to within $\pm$0.1 dB over a 30 dB input signal dynamic range (0.2 to 7 volts peak-to-peak).

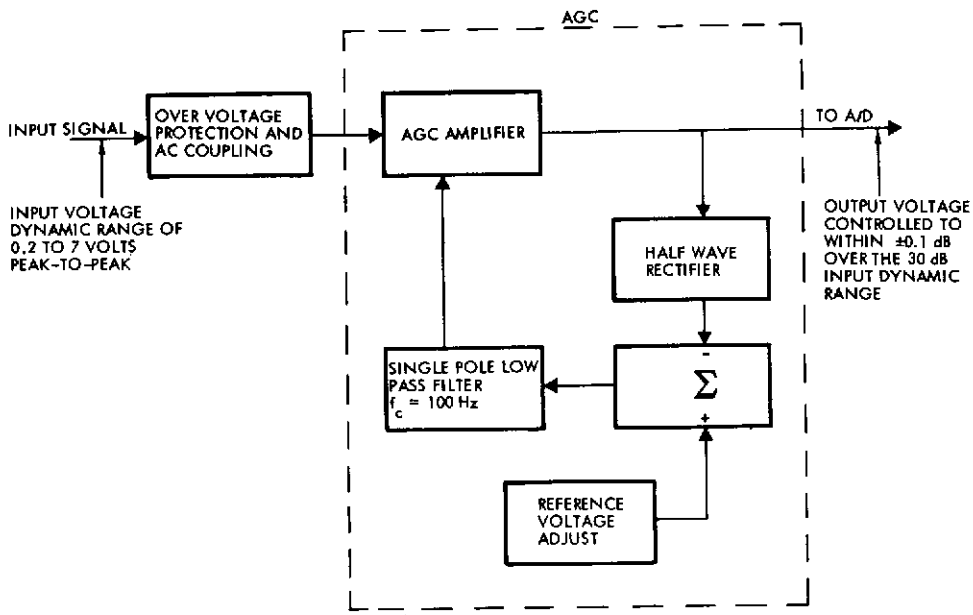


Figure 2-3. Input Data Conditioner and AGC

The reference voltage is adjusted to produce an AGC input signal-plus-noise level of 284 mV rms for an input SNR of -15 dB in the 10 BR bandwidth (or -5 dB in the bit rate bandwidth). This setting minimizes the quantization noise produced by the 4-bit A/D at the design threshold SNR of -5 dB.

Figure 2-4 shows the normalized variation in the input mean signal level into the A/D. Note that the increase of mean signal level over the assumed operating SNR range is approximately 4.1 to 1.

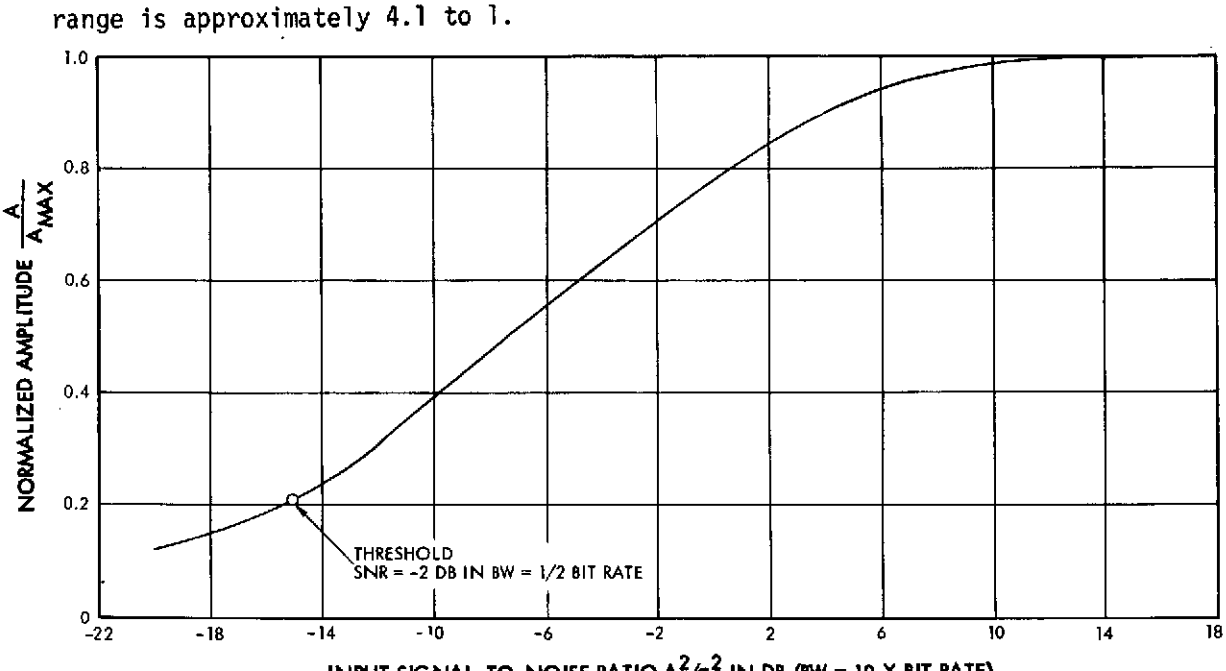


Figure 2-4. Normalized Output Signal Level Variations

2.2 ANALOG-TO-DIGITAL CONVERTER

The bit synchronizer A/D is a 4-bit converter with a transfer function as shown in Figure 2-5. The rationale for this choice is as follows. The first consideration in establishing the A/D coding and scaling is the influence of the choice of quantization symmetry. Figure 2-6 depicts two possible cases. Since the goal of the synchronizer is to detect the data polarity, a slicing level at zero is desired to extract signal polarity even for samples of amplitude below q (the quantization interval size). Next, a digital output code set must be assigned to represent each quantization level. A rounded 2's complement number system which generates a symmetrical output from the A/D was chosen as shown in Table 2-1. A drawback of this number scheme is that the A/D word size is increased by 1 bit; however, it should be noted that, in accumulating any even number of words from this set (as is always the case in the bit synchronizer), the least significant bit of the sum will be zero. Thus, this extra bit will not propagate through the entire unit.

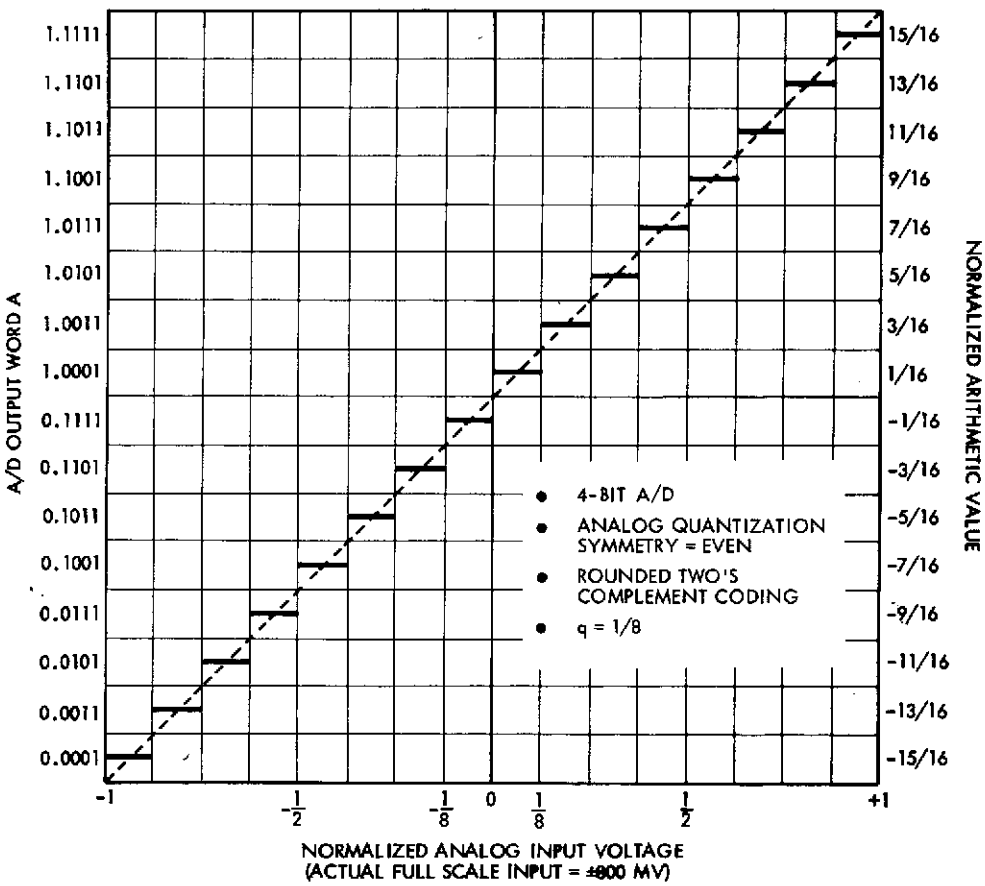


Figure 2-5. A/D Converter Transfer Function

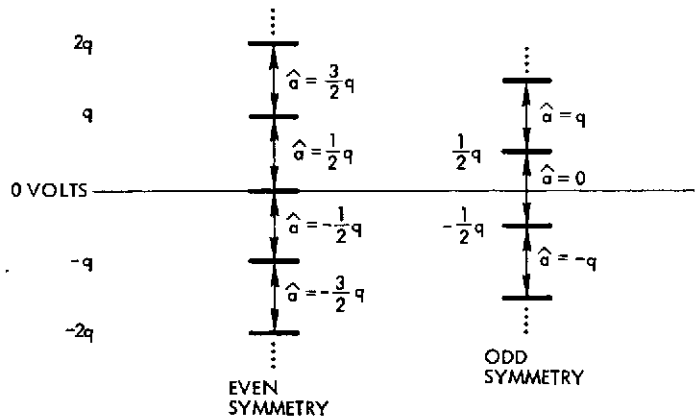


Figure 2-6. A/D Quantization Symmetry

Table 2-1. 4-Bit A/D Converter

Input		Output					
Actual (mV)	Normalized	2^0.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	Arithmetic Value
800	1						
		0.	1	1	1	1	15/16
700	7/8						
		0.	1	1	0	1	13/16
600	6/8						
		0.	1	0	1	1	11/16
500	5/8						
		0.	1	0	0	1	9/16
400	4/8						
		0.	0	1	1	1	7/16
300	3/8						
		0.	0	1	0	1	5/16
200	2/8						
		0.	0	0	1	1	3/16
100	1/8						
		0.	0	0	0	1	1/16
0	0						
		1.	1	1	1	1	-1/16
-100	-1/8						
		1.	1	1	0	1	-3/16
-200	-2/8						
		1.	1	0	1	1	-5/16
-300	-3/8						
		1.	1	0	0	1	-7/16
-400	-4/8						
		1.	0	1	1	1	-9/16
-500	-5/8						
		1.	0	1	0	1	-11/16
-600	-6/8						
		1.	0	0	1	1	-13/16
-700	-7/8						
		1.	0	0	0	1	-15/16
-800	-1						

A normalized full scale analog range of ± 1 is taken as the maximum A/D input for convenience. The output coding is chosen as representing the range -1 to +1, which is a direct unity gain mapping of the normalized analog inputs. This conversion gives the most significant bit, the sign bit, a weight 2^0. The remaining bits are weighted 2^{-1}, 2^{-2}, 2^{-3}, and 2^{-4}.

The sampling rates are as follows. At the 216 ($\pm 0.05\%$) Kbps input data rate, the A/D converter sampling rate is 6.912 MHz; at the 72 kbps input bit rate, the sampling rate is reduced by 1/3 to 2.304 MHz. In either case, these sampling rates produce 32 samples per bit at the nominal input data rates. Adequate data detection performance is available with only 16 samples/bit; however, 32 samples per bit was selected to minimize synchronization timing error produced by the clock recovery loop.

2.3 DATA DETECTION

The data detector is a digital implementation of an ideal matched filter matched to the unfiltered Manchester pulse shape. The analog Manchester bit detector is shown in Figure 2-7 for reference. The incoming data bits are correlated against a stored replica of a Manchester pulse and integrated over the bit period. The output of the integrator at time T is the soft decision bit statistic with mean $\pm A$, depending upon the polarity of the incoming Manchester bit, and a variation about the mean with Gaussian amplitude statistics.

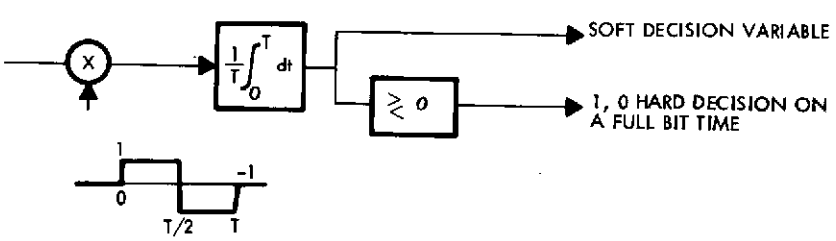


Figure 2-7. Analog Manchester Bit Detector

The digital implementation of the above matched filtering operation is shown conceptually in Figure 2-8. The input data samples (32 per Manchester data bit) from the A/D converter are scaled by 1/32, and a sum over 16 samples is formed and stored

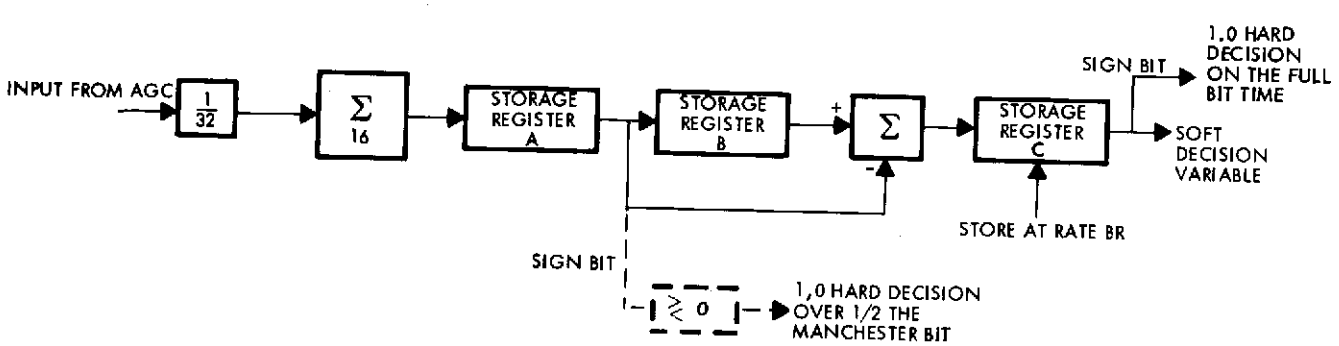


Figure 2-8. Digital Data Detector

in register A. The next group of 16 input samples is then summed and stored in register A just after the contents of register A are transferred to register B. Then the contents of register A are subtracted from register B and stored in register C. This sequence of operation is continually repeated at twice the bit rate (1/2 T).

There are a number of important aspects of this mechanization which require further discussion. First, the sum computed over 16 samples and saved in register A corresponds to performing the analog correlation over one-half a bit period. Second, by subtracting the sum of the second half of the bit period from the sum of the first half of the bit period, the values stored in register C correspond to the correlation of the incoming bits with a stored Manchester pulse shape. Third, the values appearing at the input to register C alternate between two assumed time origins (phases) offset by one-half the bit period T. The ambiguity resolver (discussed in Section 2.6) decides which of the two clock phases properly frames the incoming bits and stores them into register C at the bit rate. Fourth, the scaling of the A/D converter inputs provides unity gain for the data; i.e., the mean value of the detected Manchester data samples produced by the A/D converter. Fifth, hard decision detection of the Manchester bits is performed by retaining only the sign (most significant) bit of the 9-bit soft decision variable contained in register C. This corresponds to the greater-than/less-than decision in the analog implementation. Finally, a hard decision variable is produced over each half Manchester bit from the contents of register A. This is shown as a dotted block in Figure 2-8. This decision variable, although not required for Manchester data detection, is used in the data transition detector of the clock recovery loop. This corresponds to treating the synchronizer input data stream as twice the bit rate NRZ data and producing a hard decision output on each half bit of the input Manchester waveform.

2.4 CLOCK RECOVERY — THE DTTL

Clock recovery is achieved by means of a digital transition tracking loop as shown in Figure 2-9. The loop contains a phase detector, a data transition detector, a second-order-loop filter, a numerically controlled oscillator, and associated timing logic. The sum of the input signal-plus-noise is passed through the upper and lower branches which are triggered by the timing generator according to a digitally filtered version of the error signal formed from the product of the branch outputs. Furthermore, the timing between the two branches is held at a fixed phase relationship. Basically, the data transition detector (in-phase branch) monitors the polarity of the actual transitions of the input data, and the phase detector (quadrature branch) obtains a measure of the lack of time synchronization between the reconstructed bit rate clock produced by the numberially controlled oscillator and the actual incoming data rate. The operation of each of the major elements is now described.

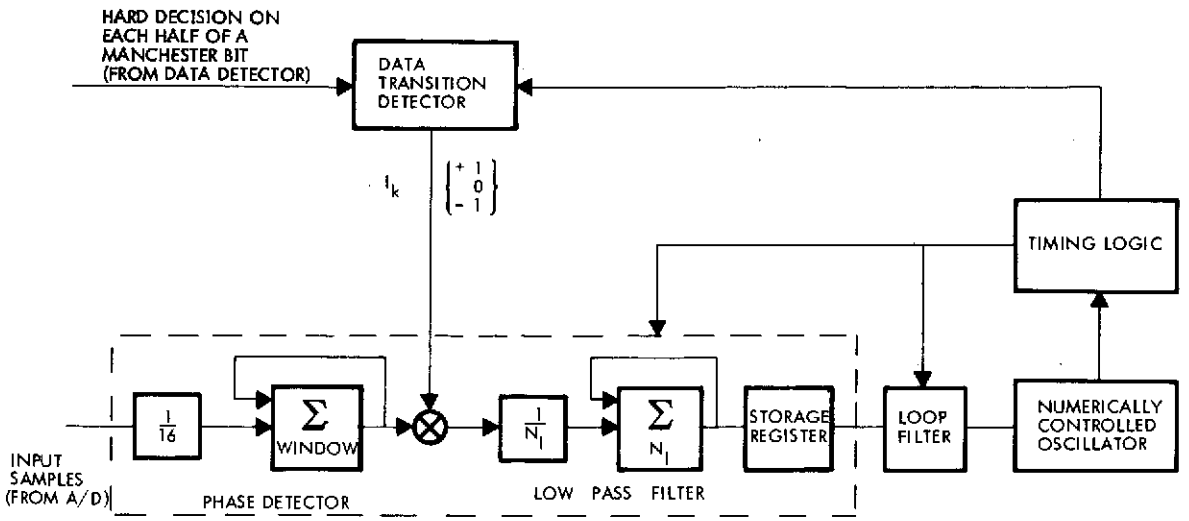


Figure 2-9. Clock Recovery — DTTL Loop

Figure 2-10, in conjunction with 2-9, shows how an estimate of bit sync timing error is produced from a noise-free input signal in an analog implementation (processing delays have been neglected in this diagram). The timing logic opens a window of width $\xi_0 T$ ($\xi_0 \leq 1/2$) (waveform 2) about the assumed data transition point and an integration is performed across this window to produce an error voltage as shown in waveform 3. Note that the mid-bit error voltage sign is the same as the direction of the actual data transition shown in waveform 1. The data transition logic detects

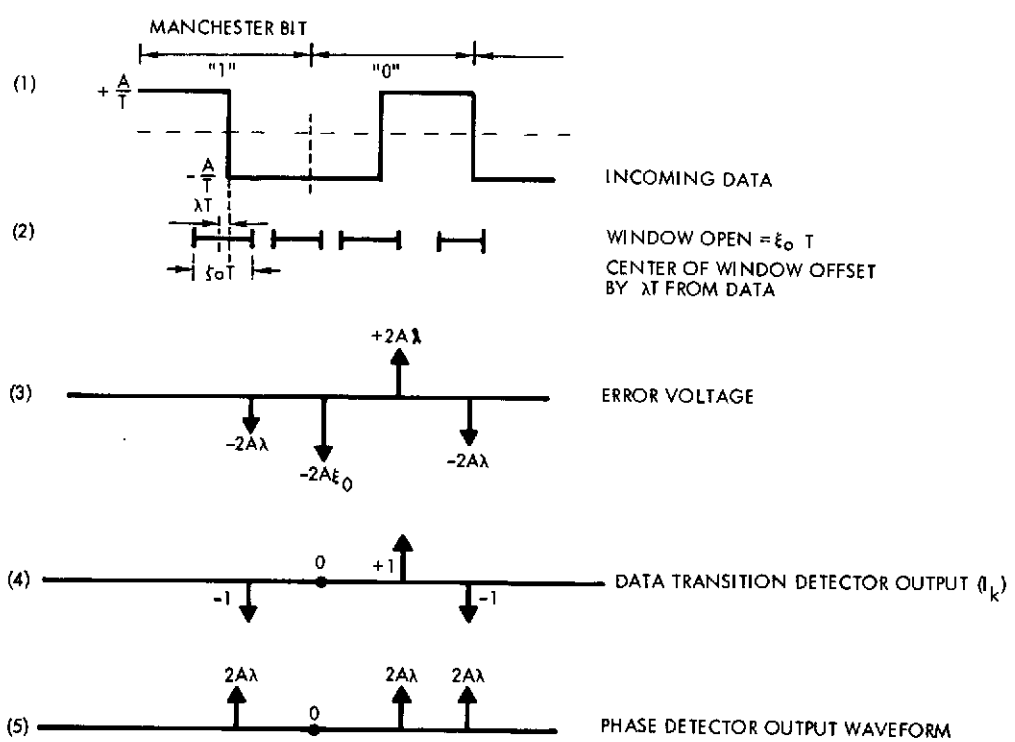


Figure 2-10. Bit Timing Error Estimation

the data transition direction or the absence of such a transition and assigns the value -1, +1, or 0, respectively. This output is shown in waveform 4. The phase detector output waveform 5 is obtained by multiplying the error voltage waveform 3 by the data transition detector waveform 4. In the digital bit synchronizer implementation, the integrations are realized by accumulating samples of the input waveform.

Three key observations can be made from waveform 5. First, the phase detector output error voltage is positive for a positive timing offset λT. Second, for no timing offset ($\lambda = 0$), the phase detector error voltage is zero. Finally, an error voltage is produced only where there is a transition in the incoming data. For Manchester data there is always a transition in the mid-bit position; for the between bit position, it only occurs with a probability $P_T = 1 - 2pq$ (p and q are the probability of a "1" and "0", respectively, in the NRZ data before it is encoded into the Manchester format; thus 2 pq is the NRZ data transition density). In the absence of noise, the normalized phase detector output characteristic $g(\lambda)$ is shown in Figure 2-11. Note that a stable lock point exists every half bit period, and the slope of the error voltage increases as the transition probability 2pq in the NRZ data decreases.

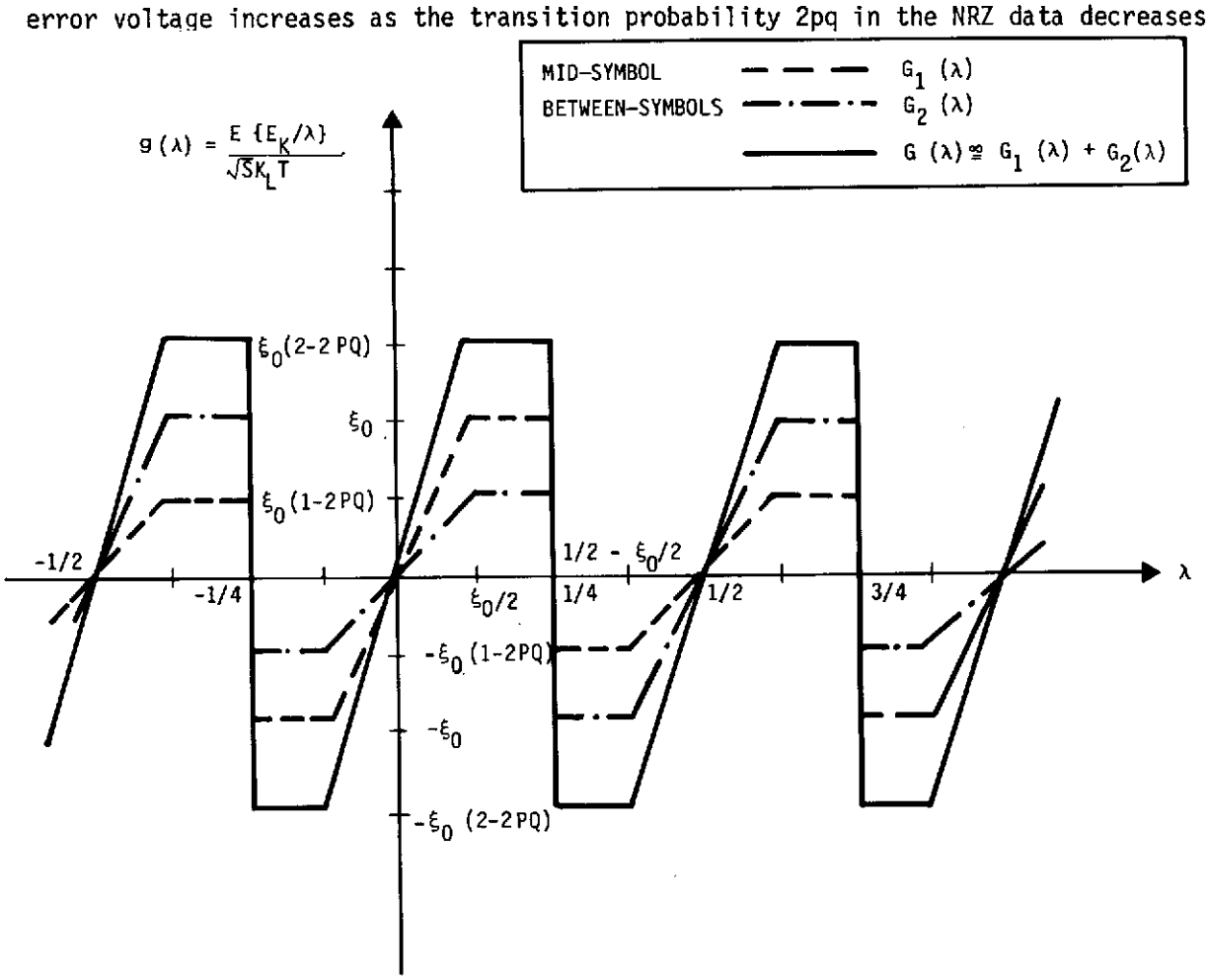


Figure 2-11. Twice Bit Rate NRZ Phase Detector Characteristics (Noise Free)

In the presence of noise, the particular implementation of the data transition detection algorithm influences the shape of the phase detector characteristic. In the brassboard synchronizer, two distinctly different data transition detector algorithms have been implemented (one for acquisition and one for tracking). The acquisition data transition detector treats the incoming Manchester data as though it were NRZ data at twice the bit rate. It makes a hard decision ("1" or "0") on each half bit as described in Section 2.3. The transition detector then examines two adjacent decisions a_{k-1}, a_k about the window and forms the transition detector output I_k as follows:

If $a_k = a_{k-1}$, then $I_k = 0$

If $a_k = 1$, $a_{k-1} = 0$, then $I_k = +1$

If $a_k = 0$, $a_{k-1} = 1$, then $I_k = -1$

Figure 2-12 shows the normalized error voltage for the 2BR NRZ phase detector versus timing offset λ as a function of SNR.

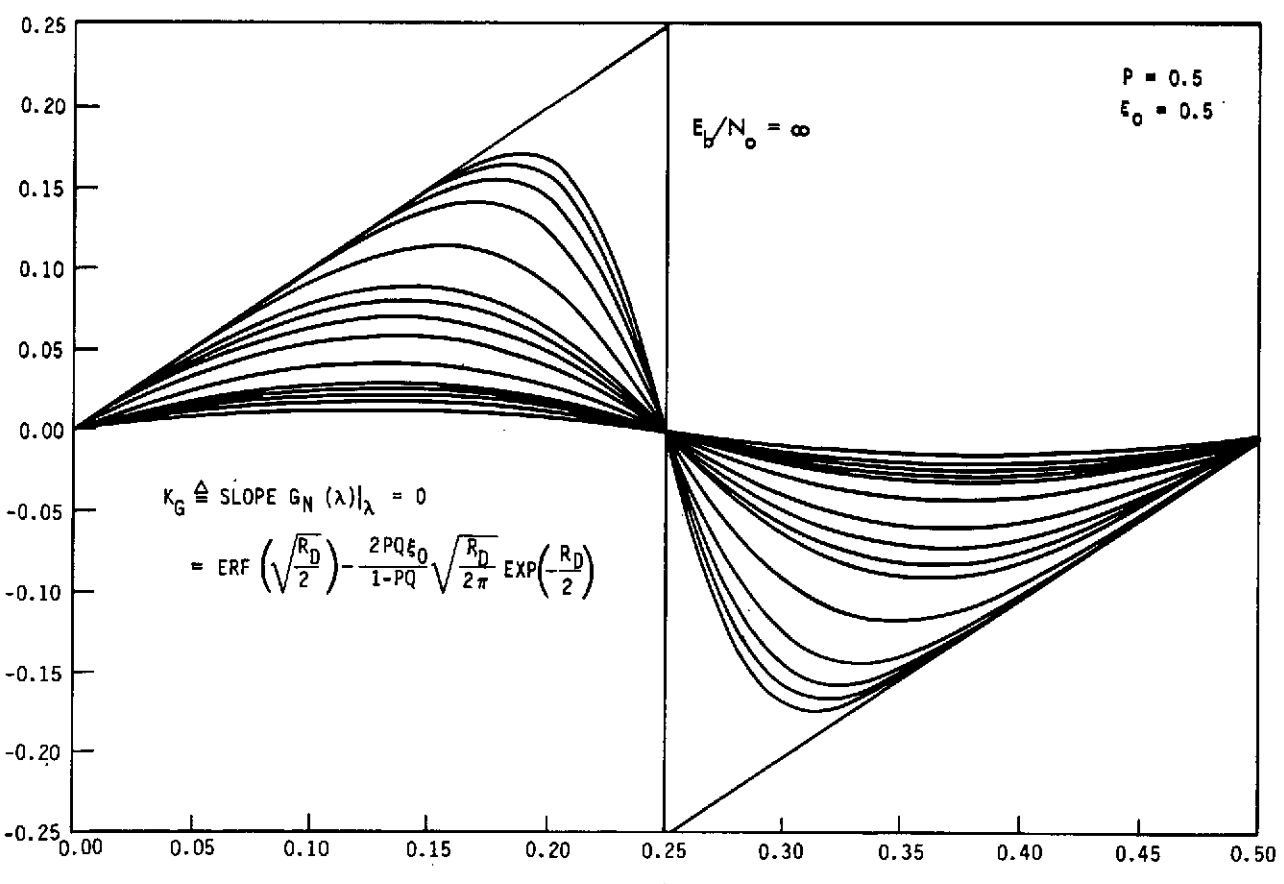


Figure 2-12. Twice Bit Rate NRZ Phase Detector Characteristics

In the tracking mode, the data transition detector is reconfigured to optimally detect the data transitions after the timing ambiguity is resolved. In this mode of operation, the mid-bit transition is determined from the decision on the complete Manchester bit since it always contains a transition. Defining b_k as the hard decision output of the bit detection described in Section 2.3, the mid-bit data transition detector output is obtained as follows:

If $b_k = 1$, then $I_k = -1$

If $b_k = 0$, then $I_k = +1$

The between-bit transition detector output (defined as I_k') is obtained by comparing adjacent mid-bit decisions as follows:

If $b_k \neq b_{k+1}$, then $I_k' = 0$

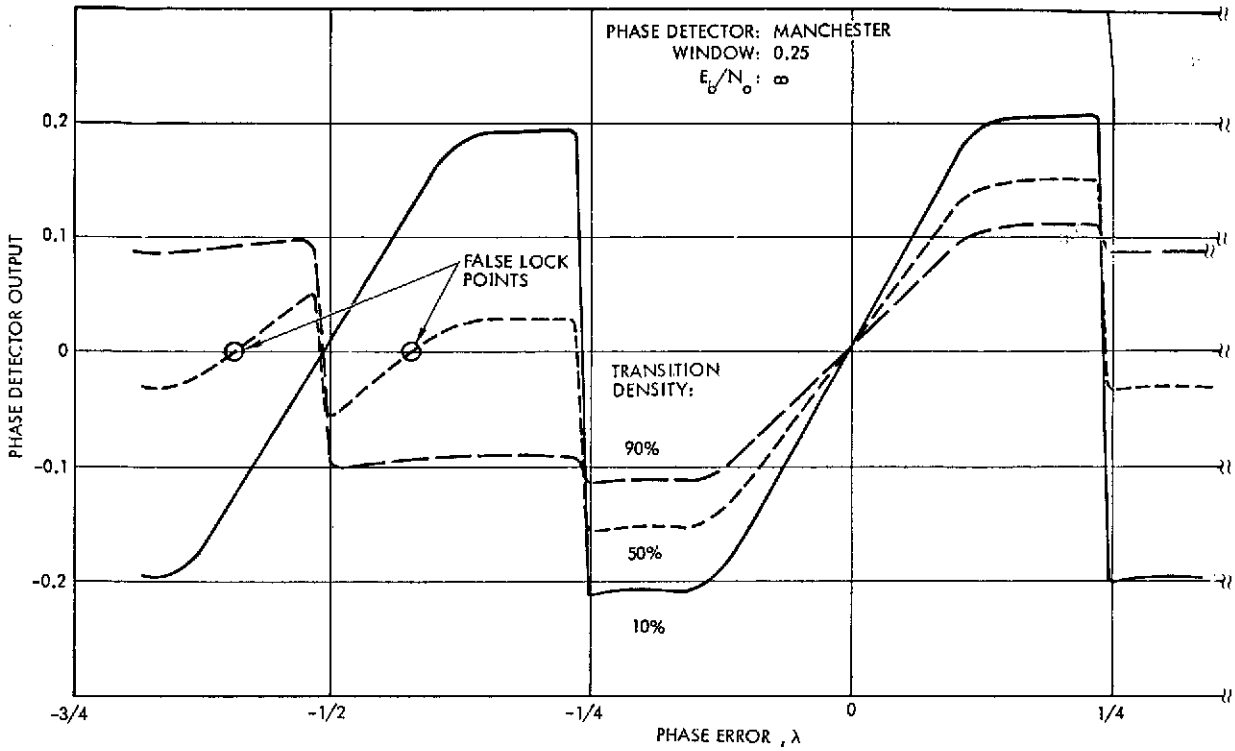
If $b_k = +1$, $b_{k+1} = +1$, then $I_k' = -1$

If $b_k = -1$, $b_{k+1} = -1$, then $I_k' = +1$.

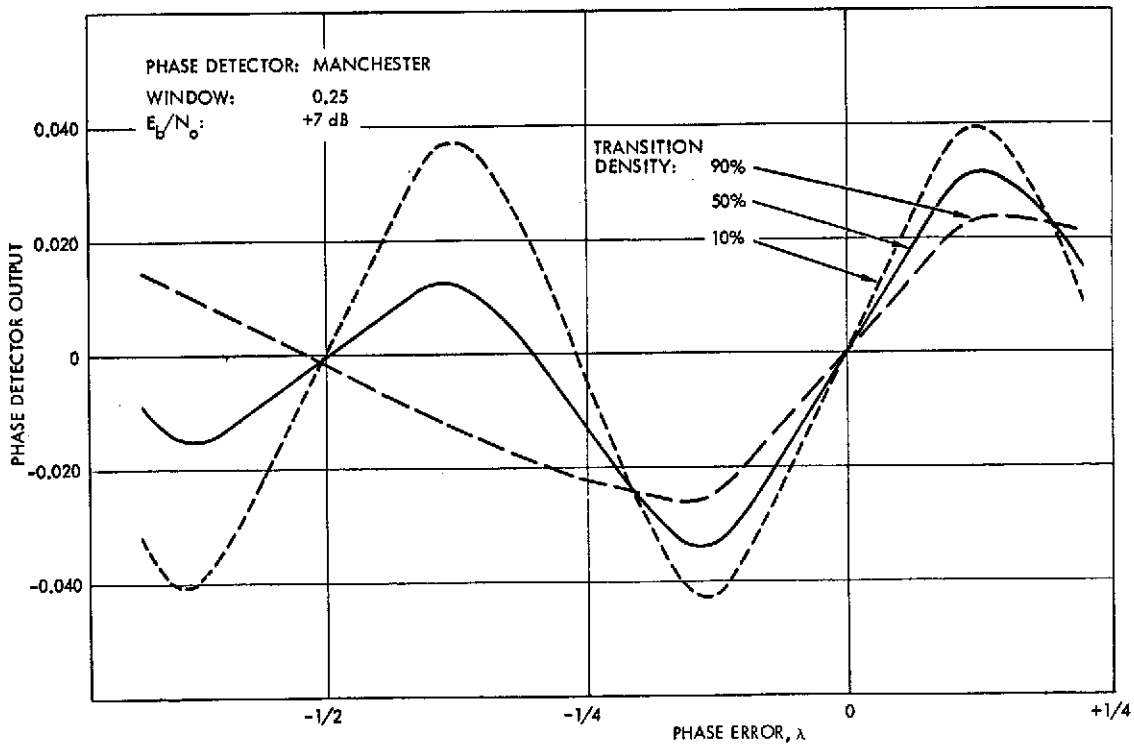
Figure 2-13 shows an experimental error voltage plot for the Manchester phase detector versus timing offset λ as a function of SNR. Note that this phase detector characteristic has false lock points at various phases between the stable lock points depending upon transition density and thus cannot be used in the acquisition mode.

In the digital implementation of the phase detector, a post detection integration (summer) has been included which averages the mid-bit and between bit outputs over N_I observations ($N_I = 16$ in the brassboard). The purpose of this integration is to reduce the noise variance associated with the phase detector output to minimize clipping which can occur in the loop filter.

The next component of the clock recovery loop is the second-order-loop filter, which requires the summing of two scaled terms, proportional plus integral, from the phase error signal. Figure 2-14 shows how the brassboard loop filter is implemented. The upper arm is the proportional term. Since the scaler L can be negative, saturation logic is included to ensure that the term $E \cdot 2^{-L}$ remains in the range -1 to +1. The lower arm is a digital integrator with saturation logic to keep it from overflowing. Since the control word F is an estimate of the static frequency offset of the incoming data (specification ± 108 Hz maximum), and since the NCO can deviate 1688 Hz for a full scale input, the pre-integrator scaling of 2^3 and post-integrator scaling of 2^{-3} ensure that F can never represent a frequency offset of more than 211 Hz. Finally, P and F are summed to produce the loop filter output. Here, again, saturation logic is employed to ensure that $-1 < C < +1$.



a) $E_b/N_o = \infty$



b) $E_b/N_o = 7$ dB

Figure 2-13. Manchester Phase Detector vs Normalized Phase Error

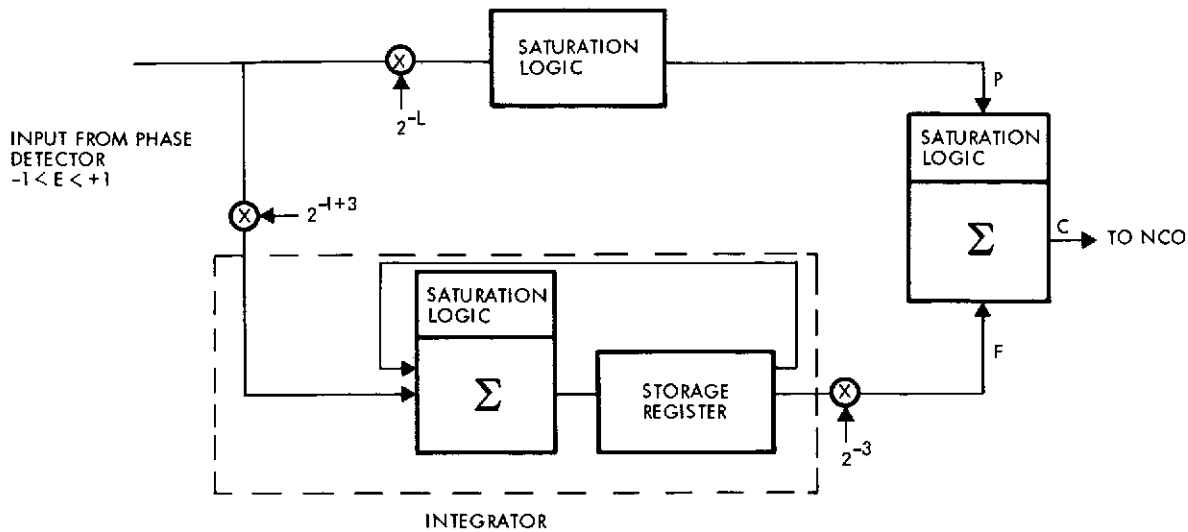


Figure 2-14. Second Order Loop Filter

The numerically controlled oscillator (NCO) (Figure 2-15) functions in a manner analogous to an analog VCO. It operates using a variable modulus division of a 256 F_s oscillator (≈ 55 MHz) where F_s is the bit rate. The average output data rate is matched to the input data rate by altering the division ratio of 256 by 0 or ±1 count at an appropriate rate determined by the accumulated error signal in the 12-stage accumulator. (The maximum rate is twice per bit.) Phase error is accumulated in the 12-stage accumulator. The function of this accumulator is analogous to the integrator

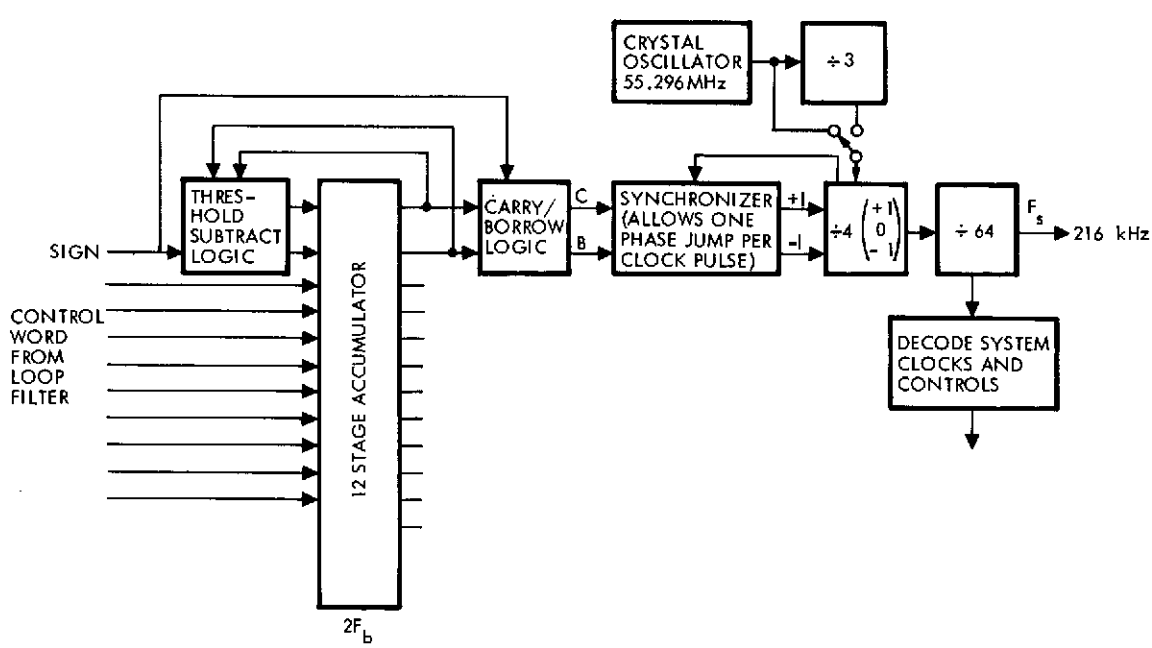


Figure 2-15. Numerically Controlled Oscillator

in a normal VCO. In the digital mechanization, the output frequency is only allowed to change after enough phase error has been accumulated and thus discretizes its operation. When a carry or borrow is generated to create a frequency change, the amount of phase error corresponding to the frequency change is added or subtracted from the accumulator. The frequency range of the NCO is thus $\pm(2/256) * F_S = \pm 1688$ Hz.

The clock recovery loop bandwidth and damping are established by the values of the selectable loop filter scalers (I, L).

2.5 SYNC DETECTOR

Sync detection is accomplished in the brassboard synchronizer by monitoring the average correlation function of the signal plus noise as a function of the synchronization error and using this voltage to drive a threshold/decision making circuit. The successful operation of the sync detector for bit synchronization relies on producing in each bit interval a signal which, when averaged over many bit intervals, is maximum when the synchronizer is perfectly in lock (i.e., zero sync error) and equally less than the maximum for positive and negative sync errors of the same magnitude. Accumulation of this error signal, as a function of the sync error, over many bit intervals and comparison with a predetermined threshold provides an indication of the bit sync loop's state. The threshold is chosen based upon system requirements and on the false alarm probability (the probability of deciding the loop is out of lock when, in fact, it is in lock) and the false dismissal probability (the probability of deciding that the loop is in lock when, in fact, it is out of lock).

The sync detector for Manchester coded data is illustrated functionally in Figure 2-16. In the absence of noise, the sync detector error characteristic (a plot of the average output vs normalized symbol sync error) has a maximum at zero symbol sync error and decreases linearly with an increasing symbol sync error magnitude. The normalized error curve is shown in Figure 2-17. The unnormalized amplitude is a function of SNR due to the fact that the correlation voltage is a function of the signal level produced by the AGC. Furthermore, the sync detector error characteristic is both symmetric and periodic with a period equal to one-half of the symbol interval T.

We note several key points regarding the interpretation of the functional diagram shown in Figure 2-16. First, k is an integer, taking on values 0, ± 1, ± 2, ..., which corresponds to particular bit intervals that are being processed by the sync detector matched filters. The timing which sets the integration for the integrate and discharge circuits is obtained from the timing generator used to operate the phase detector. Processing of the voltages to determine sync is accomplished with two matched filters, one that is matched to the mid-bit transitions, and one that is matched to the between-bit transitions. Since time can slip by 1/2 bit period, the role of the arm processing can reverse.

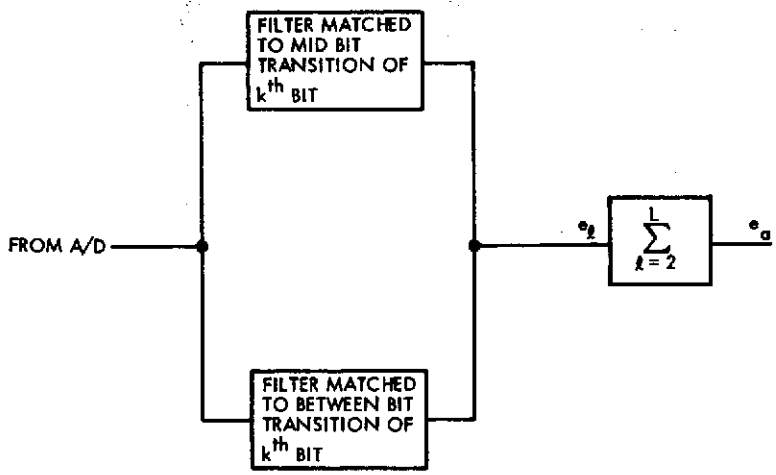


Figure 2-16. Sync Detector

Figure 2-16. Sync Detector

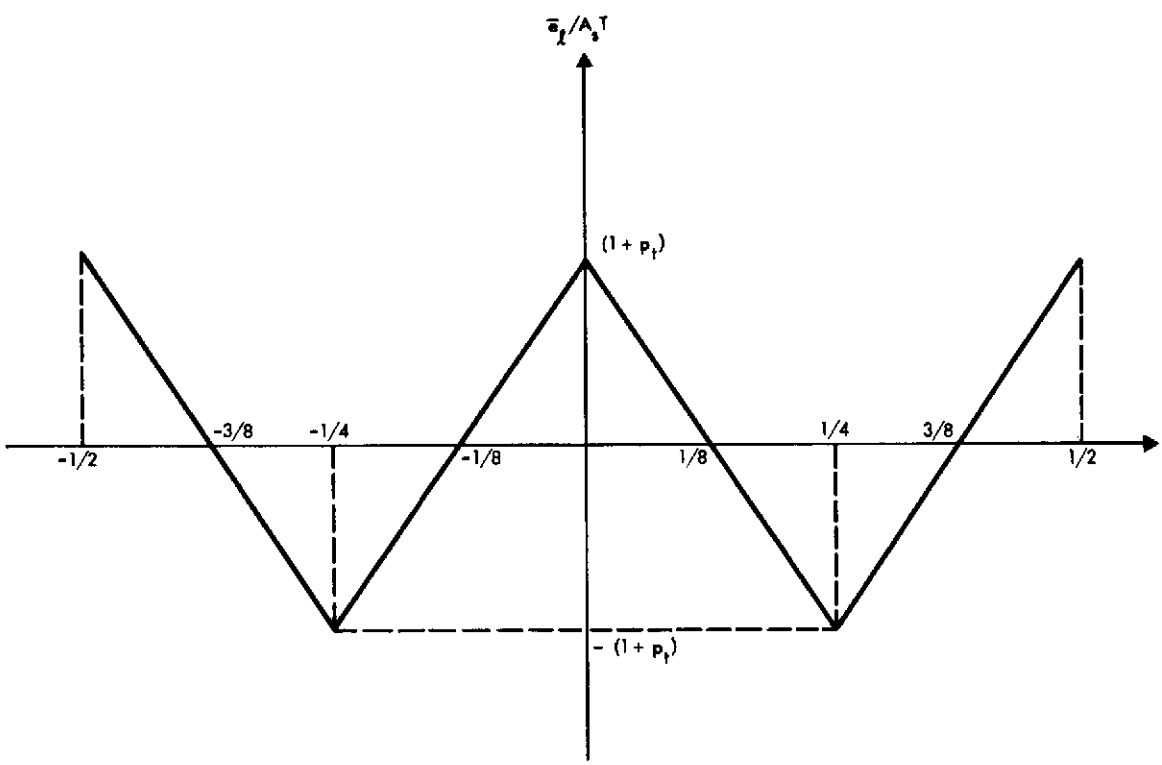


Figure 2-17. Detector Error Characteristic (Noise Free)

Performance of the sync detector, in terms of the probability of false acquisition P_{FA}; i.e., the probability of deciding the loop is in lock when, in fact, it is out of lock, and the false dismissal probability P_F; i.e., the probability of deciding that the loop is out of lock when, in fact, it is in lock, depends on the statistics of the random variable

$$e_a \triangleq \frac{1}{L} \sum_{\ell=1}^{L} e_\ell$$

and the comparison of this random variable with a threshold T_s such that

$$e_a > T_s \Rightarrow \text{in sync}$$

$$e_a < T_s \Rightarrow \text{not in sync}$$

Figure 2-18 illustrates the probability of false dismissal at E_b/N_o = -5 dB versus $n = \log_2 L$ for a transition probability of 2 pq = 0.5 when the threshold T_s is adjusted such that the probability of false dismissal of lock equals the probability of false acquisition. Here $L = 2^n$ represents the number of symbols of integration required to give a particular $P_F = P_{FA}$. Table 2-2 shows the normalized threshold setting T_s versus E_b/N_o for 2 pq = 0.5. These values of T_s can be adjusted for transition density by multiplying by the factor (1 + 0.5)/(1 + 2 pq).

Table 2-2. Normalized Threshold Settings for Various Values of E_b/N_o (2pq = 0.5)

ST/N_o	TS/2A
-5	0.143
-3	0.170
-1	0.198
+1	0.211
+3	0.238
+5	0.247
+7	0.249

The threshold is set for E_b/N_o = -5 dB. The pdf's of interest for this condition are shown in Figure 2-19. As E_b/N_o increases, the probability of false dismissal remains approximately the same since σ_a is approximately constant (-5 to +10 dB), but the probability of false acquisition P_{FA} decreases because the mean of the pdf increases due to the AGC action.

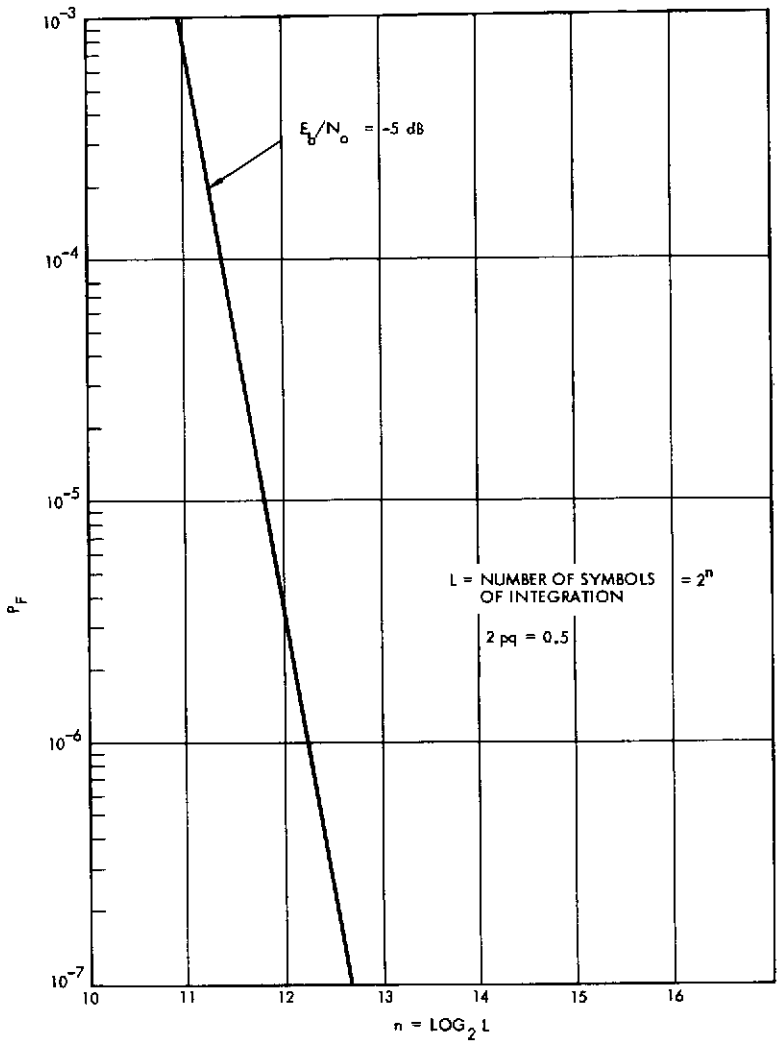


Figure 2-18. Probability of False Dismissal of Lock vs Integration Time

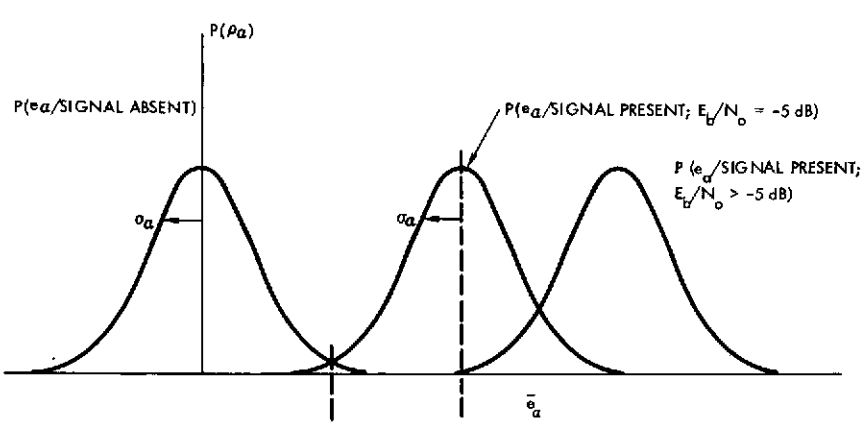


Figure 2-19. Probability Density Functions Illustrating Behavior of Sync Detector Performance as the Signal-to-Noise is Increased from E_b/N_o = -5 dB

Although a value of L equal to 2^{13} would be adequate in terms of P_F and P_{FA}, L has been conservatively selected to be 2^{14}, thus making P_F and $P_{FA} << 10^{-7}$. It should be noted that this error rate corresponds to an average of one false dismissal every 2.1×10^5 hours.

2.6 AMBIGUITY RESOLUTION FOR MANCHESTER DATA

As already observed, the phase detector characteristic used for acquisition has two stable lock points in the interval (+0, T). The points at 0 (and T) correspond to desirable lock points, while the point at $\lambda = T/2$ (see Figures 2-11 and 2-12) corresponds to the situation where the estimated clock produces data detector outputs at the mid-bits rather than at the desired between-bits. Stated another way, if bit synchronization is done at twice the bit rate and then divided by 2, a clock phase ambiguity is possible.

The loop ambiguity can be resolved by using the Manchester code property that a mid-bit transition occurs with probability one every bit time, whereas the presence of a between-bit transition depends upon the lack of a transition in the NRZ data. The between-bit and the mid-bit transitions can be obtained directly from the output of the data transition detector described in Section 2.4. The output of the data transition detector can be sorted into two conjectured groups, namely, those having to do with mid-bit transitions (say, I'_k) and between bit transitions (say, I_k). Now, I_k and I'_k are random variables taking on values

$$\text{Between-bit} \quad I_k = \begin{cases} 1 & \text{negative going transition} \\ 0 & \text{no transition} \\ -1 & \text{positive going transition} \end{cases}$$

$$\text{Mid-bit} \quad I'_k = \begin{cases} 1 & \text{negative going transition} \\ 0 & \text{no transition} \\ -1 & \text{positive going transition} \end{cases}$$

The absolute values I_k and I'_k of these random variables are used to drive an up/down counter in such a way that it counts up on transitions occurring at the conjectured mid-bit transitions and down on the conjectured between-bit transitions as shown in Figure 2-20. After L mid-bit and between-bit observations have been counted, the count is examined, and the ambiguity is resolved as shown in Figure 2-20.

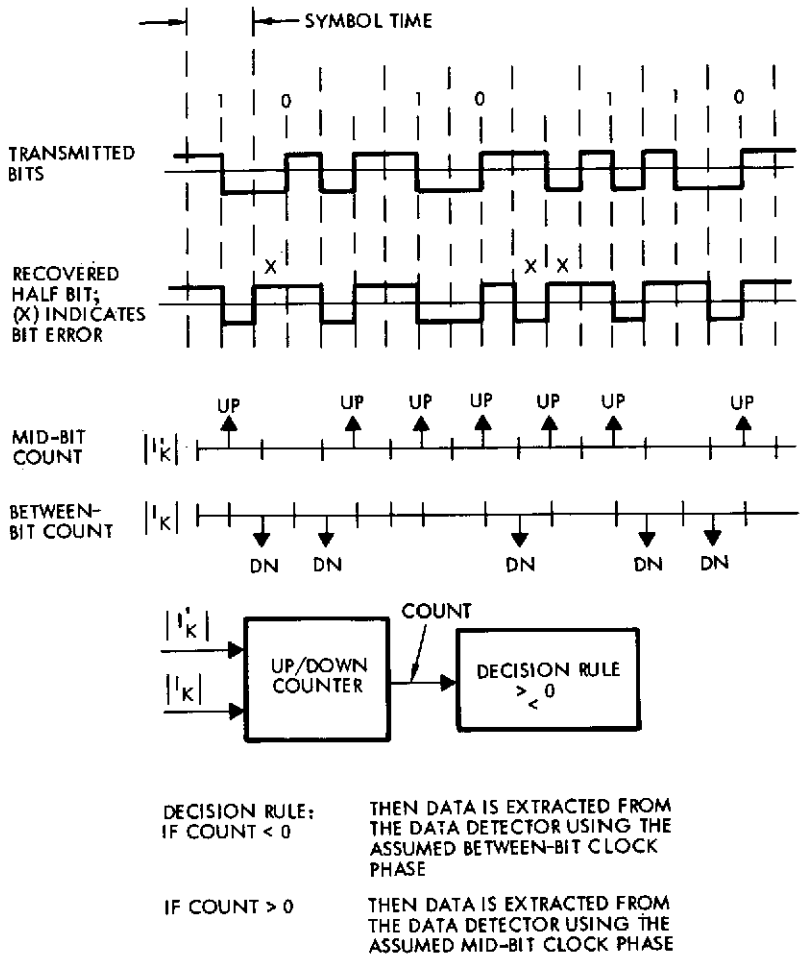


Figure 2-20. Manchester Bit Timing Ambiguity Resolution

For design purposes, it is desirable to know the probability of incorrect ambiguity resolution as a function of the number of bits of integration for E_b/N_o = -5 dB. Figure 2-21 illustrates the probability of incorrect ambiguity resolution P_I obtained from

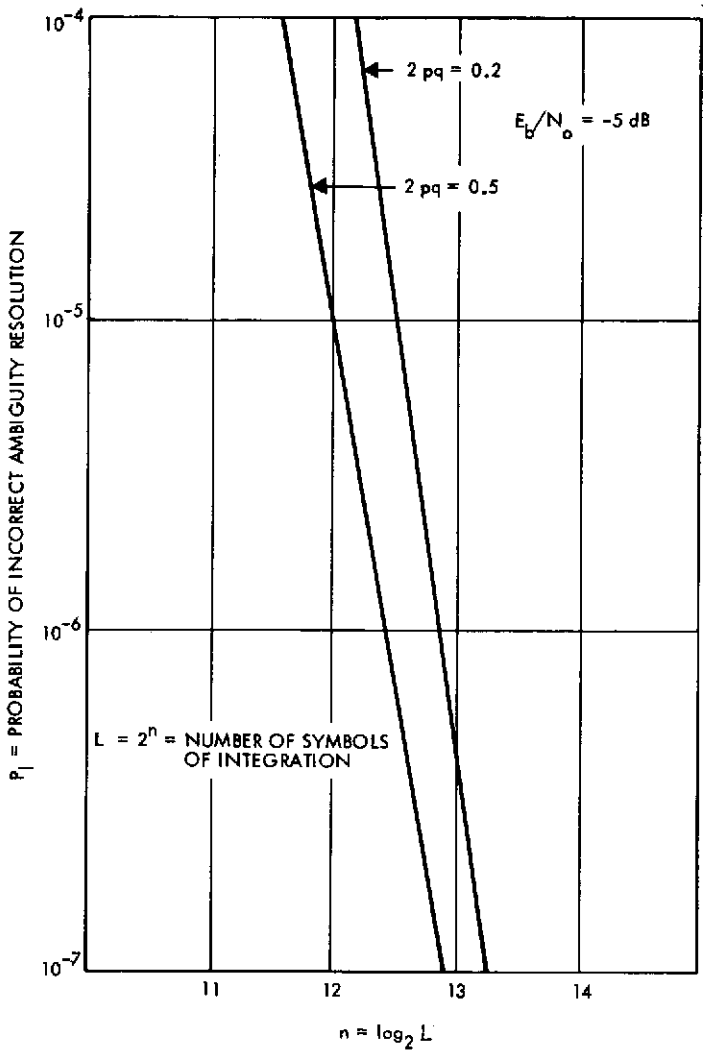


Figure 2-21. Probability of Incorrect Ambiguity Resolution

$$P_I = 1 - \text{Prob}\left[\sum_{k=1}^{N} |I'_k| > \sum_{k=1}^{N} |I_k|\right]$$

versus $n = \log_2 L$ for E_b/N_o = -5 dB and data transition densities of 2 pq = 0.2 and 0.5, respectively. From this curve it appears that $N = 2^{14}$ will give a probability of incorrect ambiguity resolution of the order of 10^{-10} for E_b/N_o = -5 dB. Higher values of E_b/N_o will give even lower values for P_I. For convenience, the value of L for the ambiguity detector is chosen to be the same, then, as that for the lock detector (2^{14}) since that integration time is also adequate in this case.

2.7 AGC BASIS AND SOFT DECISION THRESHOLDS

The bit synchronizer derives data timing and detects each channel symbol in the matched filter. In order to retain the most information for the convolutional decoder, a soft decision is made whereby the detected signal-plus-noise is quantized. For each particular number of quantization levels and SNR there exists an optimum value of the quantizer step size relative to the detected signal and noise (optimum in the sense of providing the most useful information to the decoder). Over the operating range of E_b/N_o for the bit synchronizer, the optimum thresholds are nearly constant relative to the noise. This it is desirable to AGC the input to the bit synchronizer on noise alone. However, because of the large prediction bandwidth, a noncoherent AGC on the signal-plus-noise gives comparable performance and is far easier to implement. Thus it is the selected means of AGC.

This section presents the optimum soft decision thresholds as a function of SNR and computes the system degradation associated with the use of either coherent or noncoherent AGC. The degradation for noncoherent AGC is negligible at low SNR where performance is critical. At high E_b/N_o (10 dB), the degradation in system performance reaches 0.25 dB for 8 level soft decisions but is still negligible for 32 levels.

2.7.1 Analysis of The Soft Decision Process

The AGC and soft decision process in the bit synchronizer is modeled in Figure 2-22. The input is a Manchester coded data signal in white Gaussian noise. The energy per bit is denoted by E_b. The noise has one sided power spectral density N_o and has been prefiltered at 10 times the data bandwidth. The AGC gain, G, holds the signal constant in the coherent mode and the signal plus total noise constant in the noncoherent mode.

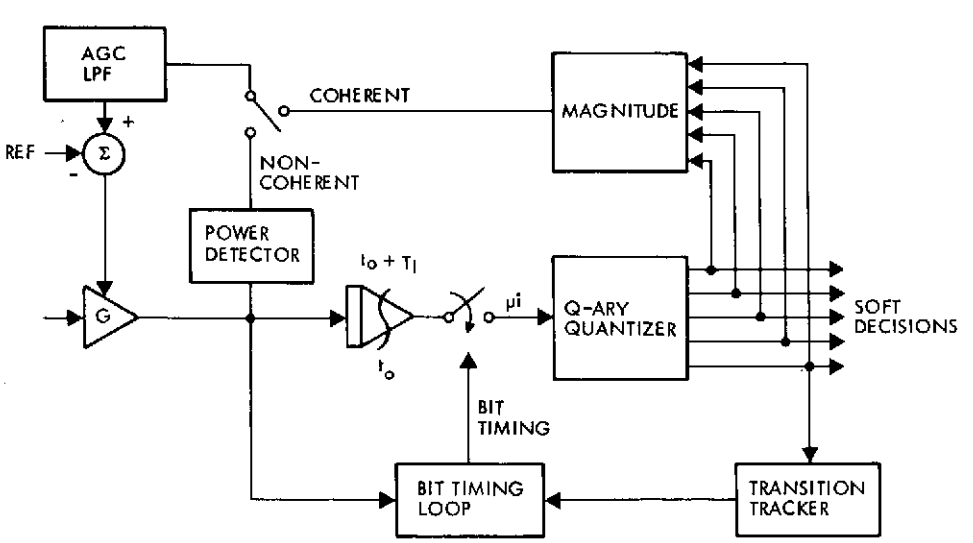


Figure 2-22. Bit Synchronizer Model for AGC/Soft Decision Analysis

The input to the soft decision quantizer, μ, is a Gaussian random variable with normalized variance $\sigma^2 = 1$ and mean $\pm \sqrt{2E_b/N_o}$, depending upon the sign of the transmitted data symbol. The probability density function, conditioned on the transmission of a negative symbol, is shown in Figure 2-23 for uniform Q = 8 level quantization. The normalized threshold spacing is defined as γ. The conditional probability of the ith level is given by the area under the curve, A_i.

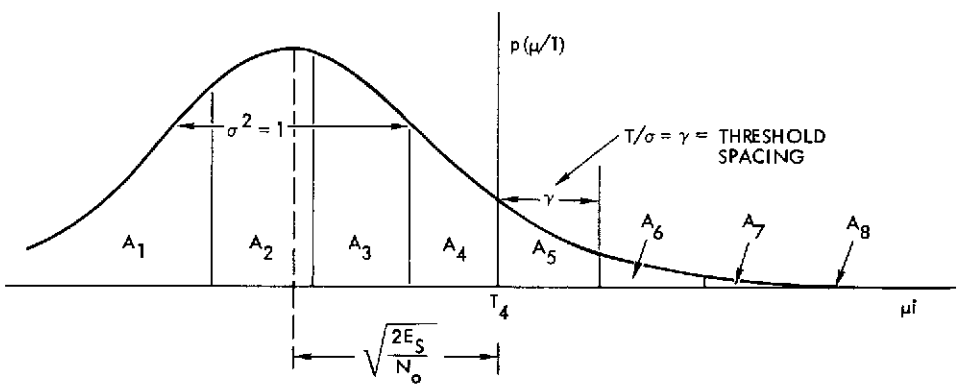


Figure 2-23. $P(\mu/1)$ With Q = 8 Level Quantization

There are several approaches to optimization of the threshold spacing. The best quality criterion is the ultimate error rate out of the convolutional decoder which can be conceptually determined by varying the threshold spacing to find an optimum at each E_b/N_o. In fact, limited results on threshold optimization are available from decoder simulations. The error rate was minimized for a K = 7, rate = 1/2 Viterbi decoder with Q = 8 level soft decisions operating at E_b/N_o = -1.5 dB by choice of a quantization threshold $\gamma = 0.54$.

Alternate approaches which are more amenable to parametric analysis include maximization of channel capacity or R_{comp}, the theoretical maximum rate for sequential decoding of convolutional codes. The quantization thresholds which maximize each of these quality criteria as a function of E_b/N_o and Q have been computed. The results of the R_{comp} and capacity calculations are typified in Figure 2-24 where R_{comp} is shown for Q = 8 as a function of the normalized threshold spacing γ. The optimum value of γ is also plotted and seen to be nearly constant with respect to the noise variance σ^2 ($\gamma_{opt} \approx 0.58\sigma$) which agrees exactly with previously published results. One other curve is included for comparison, namely the optimum curve for γ based on channel capacity (the result of maximizing over γ). This curve in general shows a smaller optimal threshold spacing, and a tendency to grow smaller as SNR increases.

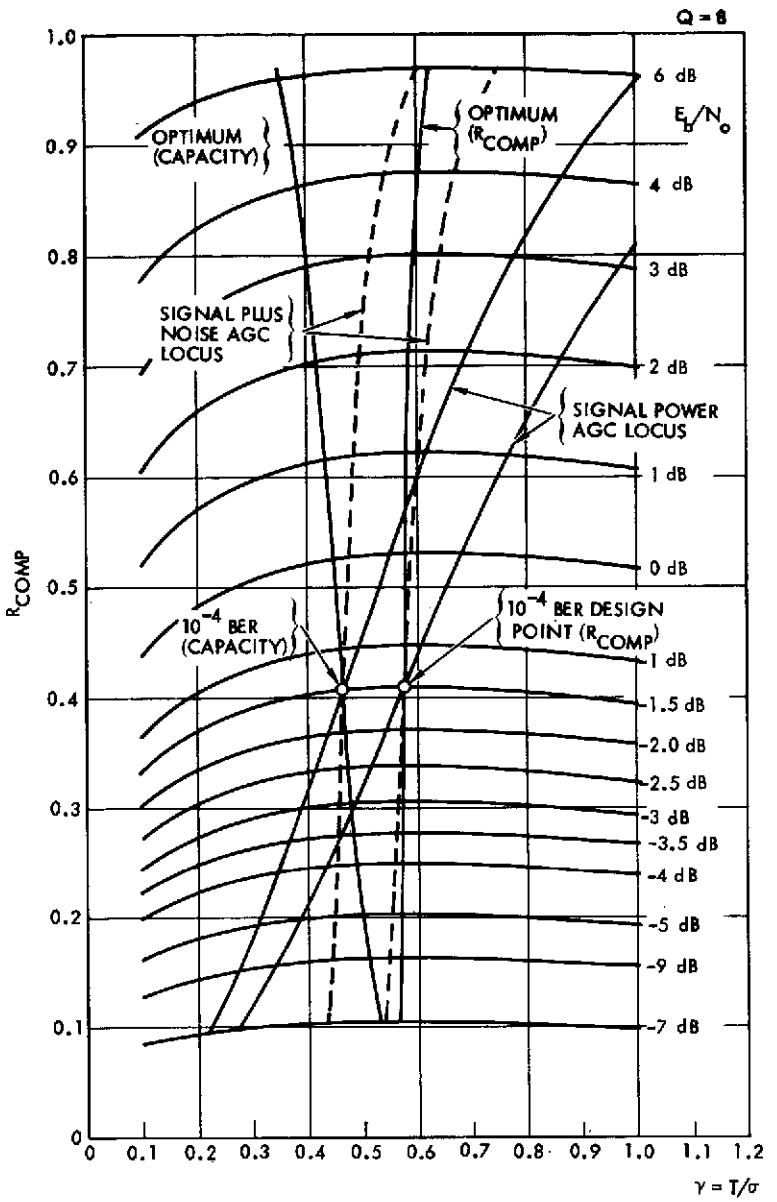


Figure 2-24. R_{comp} vs T/σ (Q = 8)

Threshold variation caused by either coherent or noncoherent AGC circuits is shown in Figure 2-25. The design point for fixing the AGC proportionally constant and optimizing the threshold for this example is E_b/N_o = -1.5 dB, which corresponds to a 10^{-4} bit error rate at the decoder output. This choice reflects anticipated link performance for high quality Shuttle voice links with K = 7, rate = 1/3, Q = 8 Viterbi decoding. Clearly the locus of suboptimum thresholds for noncoherent AGC provides a better fit to both the optimum capacity and optimum R_{comp} values of γ. Figure 2-25 shows the relative fit of γ, altered by the noncoherent AGC, relative to the optimum (R_{comp}) for Q = 4, 8, 16, and 32. The desired point $2E_s/N_o$ = 1.5 dB.

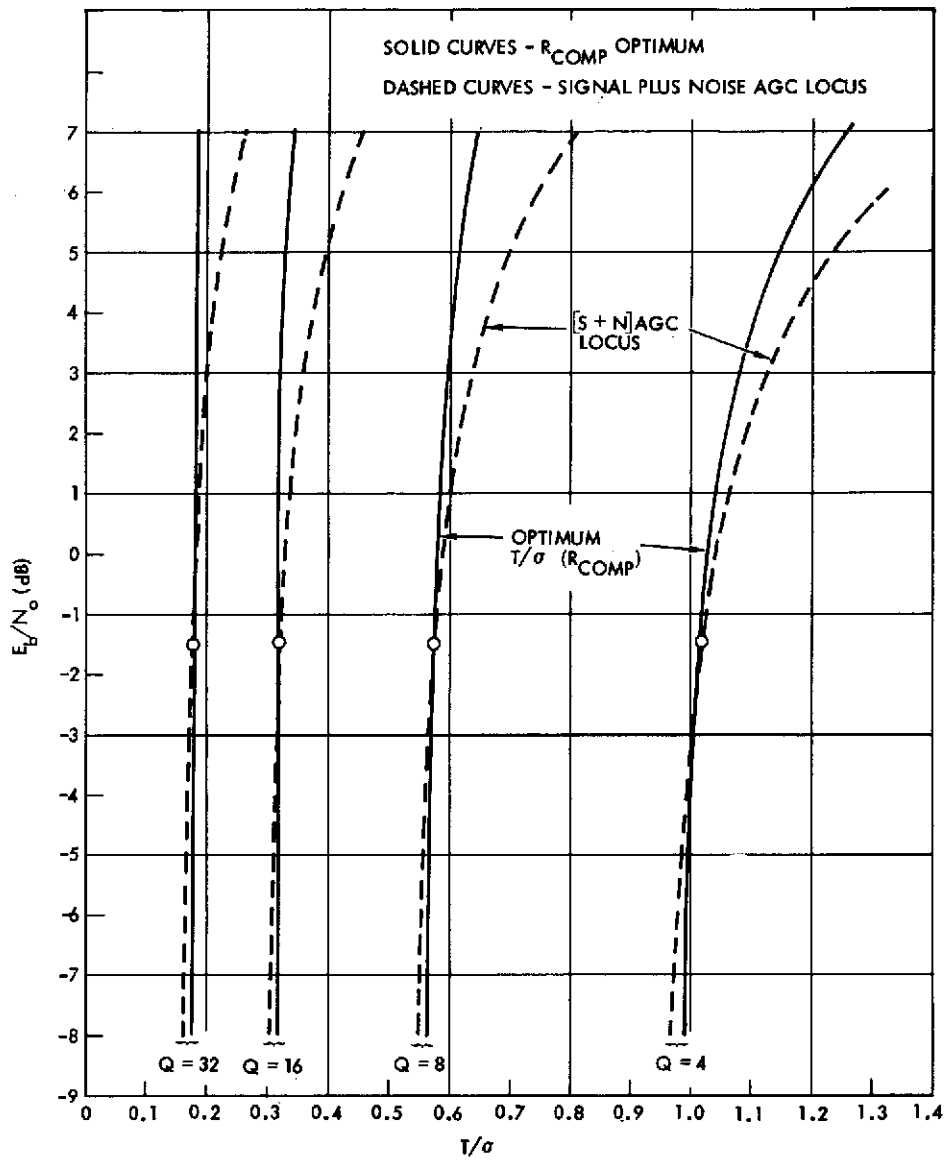


Figure 2-25. Optimum T/σ vs E_b/N_o

In order to quantitively evaluate the effect of the relative fit between the AGC locus and the optimum γ curves, calculations were run to determine the incremental E_b/N_o need to raise R_{comp} (or capacity) on the AGC locus to the value of optimum γ. For the Q = 8 case, Figure 2-26 shows the degradation as a function of E_b/N_o, relative to the infinite quantization case. The curves are plotted for both capacity and R_{comp}, and for both coherent and noncoherent AGC. The cpacity curves show that only 0.105 dB is lost in going from $Q = \infty$ to Q = 8, while R_{comp} predicts a loss of 0.157 dB. These values then degrade more as γ departs from the optimum due to coherent and noncoherent AGC variations. The question of which values are most indicative of true performance can be addressed by comparison with simulation results.

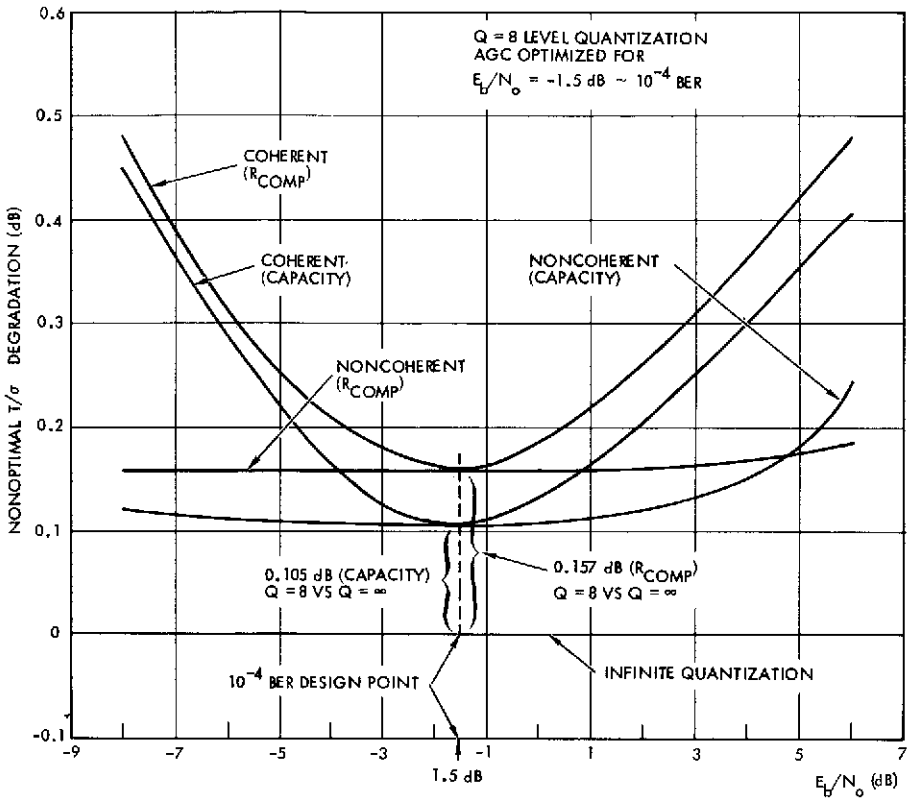


Figure 2-26. Degradation Due to AGC (Q = 8)

Table 2-3 shows the predicted degradation due to varying γ at a specific SNR, which is to be compared with simulation results obtained by Heller and Jacobs.[1] The fit of R_{comp} is better than that of capacity at this SNR. Further, Odenwalder's[2] simulation results show an increase of 0.2 dB in coding gain in going from Q = 8(γ = 0.58) to Q = 32 (γ = 0.18), which agree more closely with R_{comp} predictions (0.15 dB) than the capacity prediction (0.10 dB).

Table 2-3. Degradation due to Soft Decision Quantization*

$\gamma = T/\sigma$	0.3	0.4	0.5	0.6	0.7	0.8
Predicted (R_{comp})	0.27	0.09	0.01	0.0	0.02	0.06
Predicted (capacity)	0.05	0.0	0.0	0.02	0.08	0.13
Observed (R_{comp} simulation)	0.20	0.05	0.0	0.0	0.02	0.10

*Degradation (dB) at E_b/N_o = -1.5 dB for various values of T/σ

[1] Heller and Jacobs, "Viterbi Decoding for Satellite and Space Communication," IEEE Transactions on Communication Technology, October 1971.

[2] Odenwalder, "Optimal Decoding of Convolutional Codes," PhD Dissertation, UCLA, 1970.

Using the prediction based on R_{comp}, the overall tradeoff between quantization, threshold spacing, and AGC is presented in Figure 2-27. An additional 0.145 dB of coding gain is predicted at a decoder BER = 10^{-4} by going from Q = 8 to Q = 32. Noncoherent AGC, selected for the bit sync brassboard, is strongly preferred to coherent AGC, resulting in up to 0.32 dB improvement at low E_b/N_o for Q = 8. Finally the optimum quantization spacing γ_{opt}, for Q = 4, 8, 16, and 32 and E_b/N_o = -1.5 dB are 1.017, 0.575, 0.324, and 0.181, respectively.

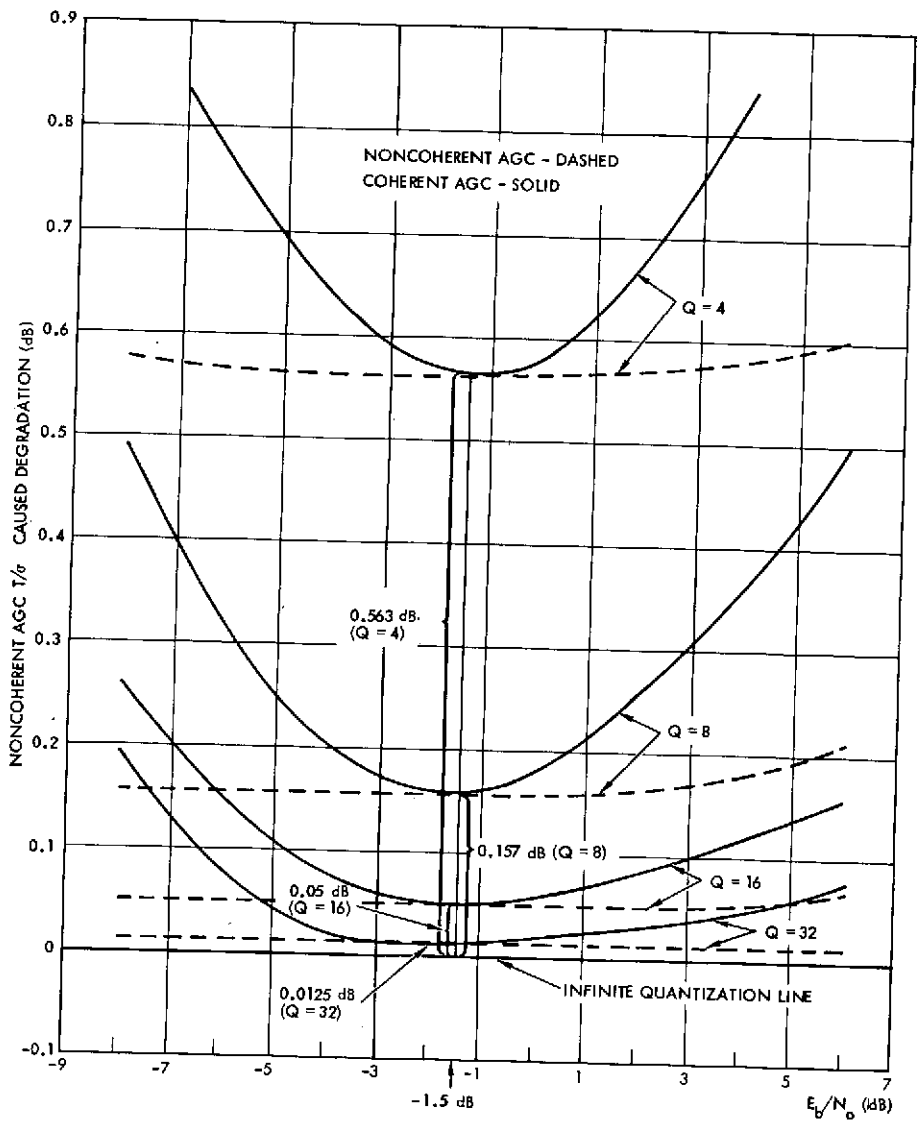


Figure 2-27. Degradation Due to AGC and Quantization

2.7.2 Soft Decision Output Formatting

Figure 2-28 depicts how the data recovery integrator (I accumulator) signal range is mapped into the output word. (Note that the most significant bit, and even the next MSB, of the accumulator is rarely occupied.) The AGC, in conjunction with the A/D converter output word format, determines the range of the data accumulator output $\hat{a}$. Since 32 samples are accumulated for each bit and the maximum bit value is $\pm 15/16$ before virtual scaling by 2^{-5}, the actual output range of the bit detector is limited to $\pm 240/256$ and can assume any number in that range in multiples of 1/256. The mean $\bar{a}$ and the standard deviation σ of $\hat{a}$ are scaled by the AGC and are a function of the synchronizer input E_b/N_0. Table 2-4 shows this variation versus the input E_b/N_0 measured in a bandwidth equal to the bit rate.

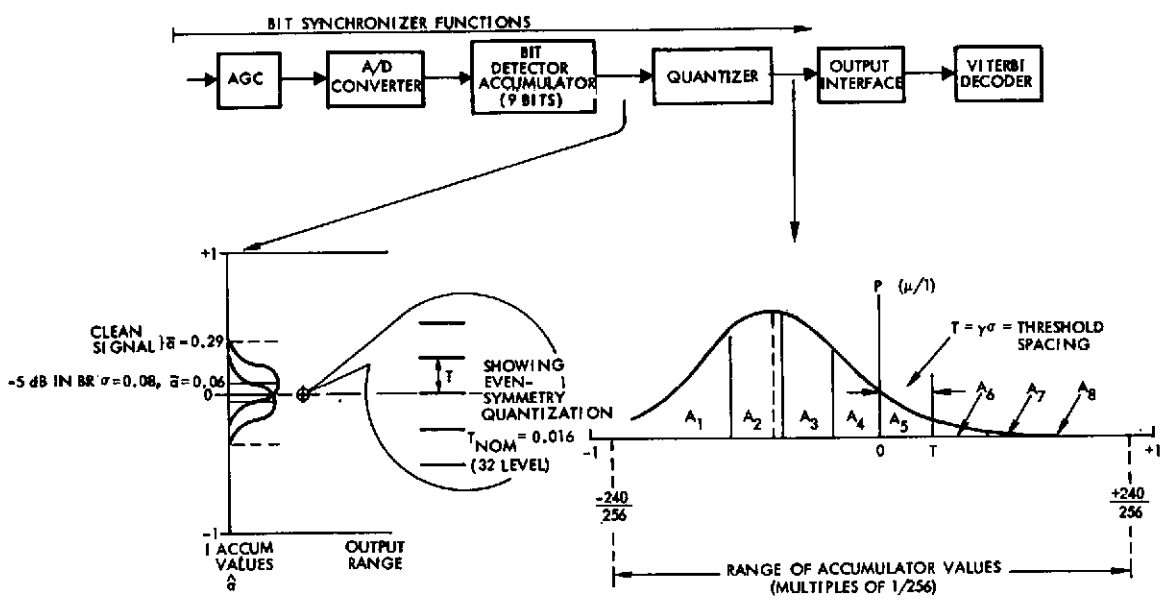


Figure 2-28. Mapping of Data Recovery Integrator into Soft Decision Output

Table 2-4. Data Accumulator Contents

SNR	Signal	Noise
IN BW = Bit Rate	$\bar{a}$	σ
-5	0.068	0.078
-2	0.086	0.077
0	0.107	0.076
2	0.131	0.074
4	0.0158	0.071
6	0.188	0.066
8	0.217	0.061

The threshold T can be set at any multiple K of 2^{-8} ($1 \leq K \leq 63$) in a front panel octal switch and thus establishes the bin width for the soft decision quantization. Table 2-5 shows an example of how the threshold T can be selected for a design point of E_b/N_o = -1.5 dB. Due to the digital implementation, the value of γ obtained, γ_K is close to, but not exactly equal to γ_{opt}. As can be seen from the figure, the percent error in selecting γ increases as the number of quantization levels increases. However, since the SNR degradation is not a particularly sensitive function for small changes in γ from the optimum, the performance loss is minimal (less than 0.1 dB for a 15% variation).

Table 2-5. Soft Decision Threshold Selection Example

E_b/N_o = -1.5 dB 5 dB

Q	T	K = 256T Base 10	Base 8	γ_K	γ opt	% from γ opt
8	0.04299	11	13	0.5580	0.575	3.0
(3 bits)	0.04675	12	14	0.6088		5.8
16	0.02344	6	06	0.3044	0.324	6.1
(4 bits)	0.02734	7	07	0.3551		9.5
32	0.01172	3	03	0.1522	0.181	16.0
(5 bits)	0.01562	4	04	0.203		12.0

The soft decision threshold values given in Table 2-5 should be optimum over the synchronizer operating SNR range (-5 to +10 dB). Referring to Figure 2-25, it can be noted that the threshold value required to maximize R_{comp} only increases a small fraction (approximately 10% for 8, 16, and 32 level quantization.

The final processing performed on the soft decision data estimate is associated with the actual output binary code used to represent that estimate. Thus, the nominal output code is offset binary, but 2's complement and three other mappings are available.

2.8 TRANSITION FROM THE ACQUISITION TO TRACKING MODE

The brassboard synchronizer is designed to operate with two bandwidths; one for the sync acquisition mode and one for the tracking mode. Transition from the acquisition mode to the tracking mode constitutes the handover problem. The supervising signal which can be used to "switch" the bandwidth is derived from the sync detector output. Unfortunately, switching of the loop bandwidth creates a stochastic transient which can force the loop out of lock. To minimize this probability,

it is desirable to enter the tracking mode by providing a slow reduction in bandwidth in order to limit the peak phase error during the duration of the transient. The transition from the acquisition to tracking mode is complicated by the fact that it involves:

- Detection of sync
- Changing bandwidth and/or damping
- Narrowing window
- Resolving ambiguity
- Switching the phase detector algorithm.

The total acquisition time budget includes:

- T_{acq} - Time to phase and frequency lock
- T_L - Time for sync indicator to indicate lock after the loop locks
- T_N - Time to narrow window
- T_{B_L} - Time to narrow bandwidth
- T_A - Time to resolve ambiguity
- T_{PD} - Time to reconfigure the phase detector.

Table 2-6 illustrates the acquisition time budget for E_b/N_o = -5 dB while Figure 2-29 demonstrates the acquisition to tracking handover algorithm as well as the monitoring of lock status. Notice that the handover sequence consists of four major steps. The configuration at each one of these steps is shown in Table 2-7.

Table 2-6. Acquisition Time Budget (at E_b/N_o = -5 dB)

Acquire lock with wide bandwidth, wide window, NRZ phase detector	4.5 sec (T_{acq})
Narrow window delay > 2 loop time constants	76 msec (T_N)
Measure V	76 msec
Narrow bandwidth to 20 Hz Delay ≈ 1 loop time constant	76 msec (T_{BL})
Measure V	76 msec
Resolve ambiguity and switch to Manchester phase detector	76 msec (T_A, T_{PD})
Check V	76 msec
Delay	76 msec
Total	5.1 sec

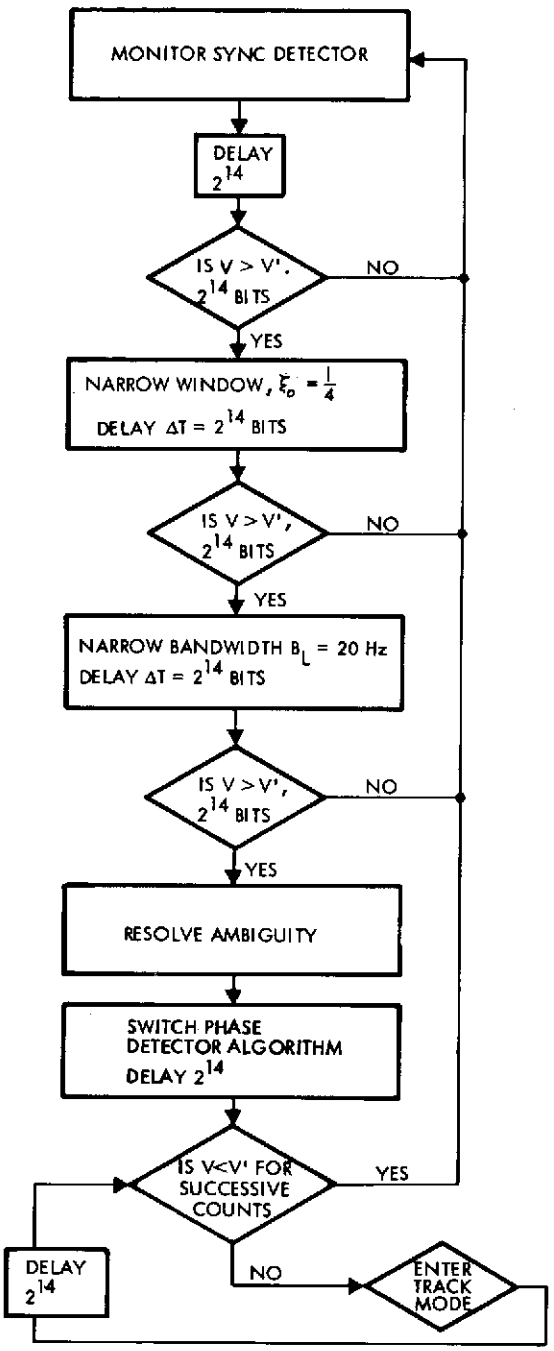


Figure 2-29. Acquisition to Tracking Algorithm

Table 2-7. Configuration of Each Step of the Handover Sequence

Sequence Steps	Bandwidth	Window Width	Phase Detector
Initial acquisition	Wide	Wide (1/2)	2R/NRZ/DTTL
Wideband acquisition	Wide	Narrow (1/4)	2R/NRZ/DTTL
Narrowband acquisition	Narrow	Narrow	2R/NRZ/DTTL
Tracking	Narrow	Narrow	Manchester/DTTL

There are two basic questions associated with this switching sequence. The first has to do with when to switch or proceed to the next step and the second, after the step is performed, what is the probability that it will remain in lock? As already mentioned, the sync detector output can be used to make the initial decision for switching to begin and the probability of false dismissal and false alarm can be made on the order of 10^{-14} at E_b/N_o = -5 dB by integrating 2^{14} samples of the sync detector output.

The question of whether the bit synchronizer remains in lock is formidable to answer from analysis because it represents a characteristically nonlinear problem; however, it is noted that the main causes of loss of lock will be due to the stochastic transient introduced by switching of the loop parameters. The effect has been minimized by the introduction of the integrator at the output of the phase detector.

3. MECHANICAL DESIGN DESCRIPTION

Details of the Shuttle bit synchronizer brassboard are presented in Figures 3-1, 3-2, and 3-3. The drawer consists of a frame containing 18 boards upon which are plugged in components mounted on component carriers and IC packages. The majority of interconnections between components are formed using wire wrap. The low power dissipation requires no special cooling. Dust covers, both top and bottom, are provided to protect the circuitry from any accidental damage and to protect users from electrical shock. High voltages are insulated against possible contact in normal maintenance. With the dust covers removed, easy access is provided to both the top and bottom of the circuit boards. The size of the unit is 19 inches wide, 5-1/2 inches high, and 19 inches deep.

The frame is partitioned into 10 modules (Figure 3-4). Each module consists of one or more 2-1/2 by 4 inch circuit boards. The majority of these boards use wire wrap interconnections. In areas where high frequencies exist or isolation is needed, the integrated circuits and components are soldered on a printed circuit board and interconnected with soldered wires. The total number of IC's used is 272.

The prime power, a 115 volt ac 60 Hz source, is switched by the back-illuminated POWER ON push button switch located on the front panel. This provides power to the two internal regulated power supplies which produce ± 5 volts dc and ± 10 volts dc. The total regulated power consumed by the unit operating under nominal signal and temperature conditions is 10.3 watts.

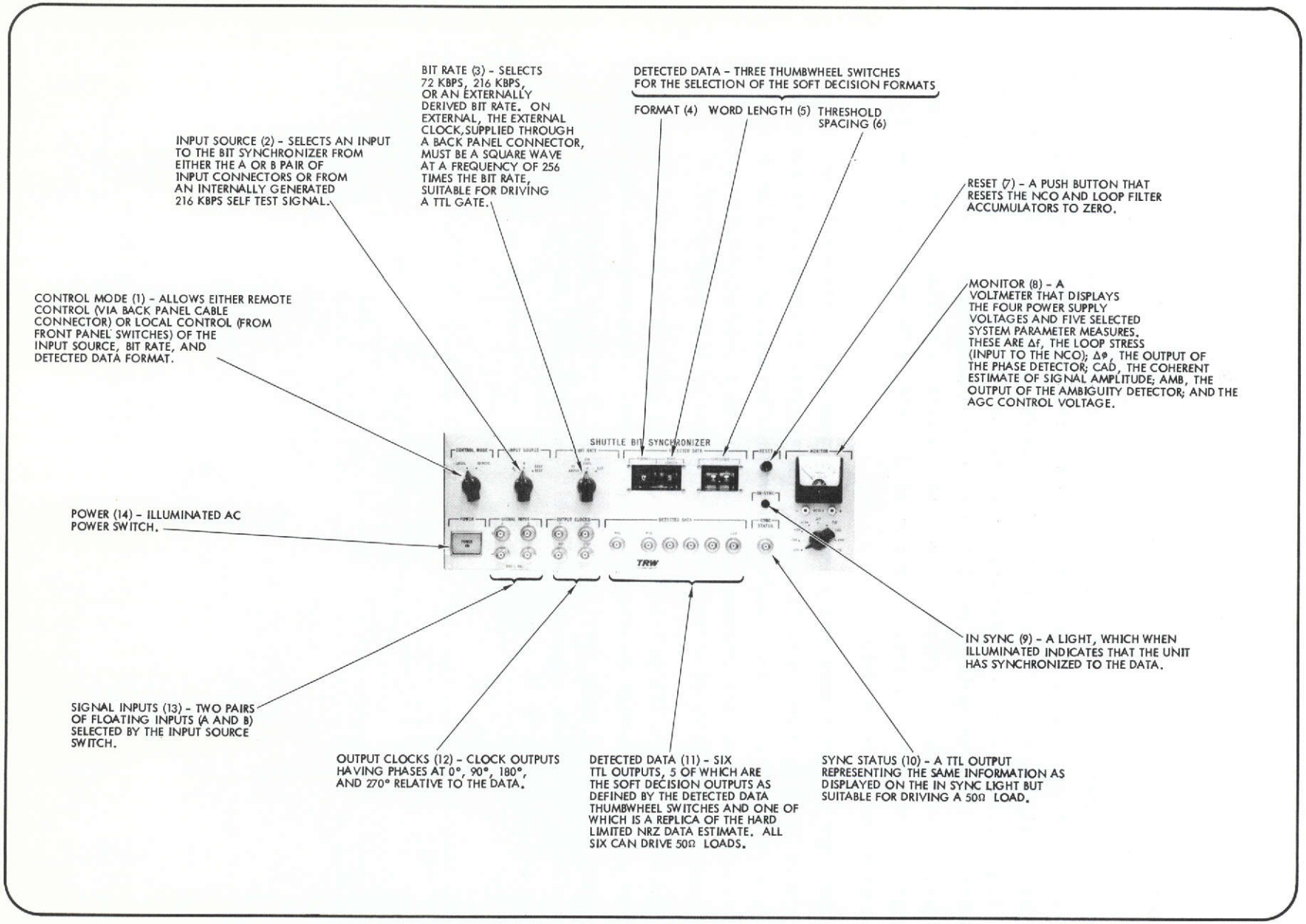


Figure 3-1. Front Panel Controls, Indicators, and Connectors

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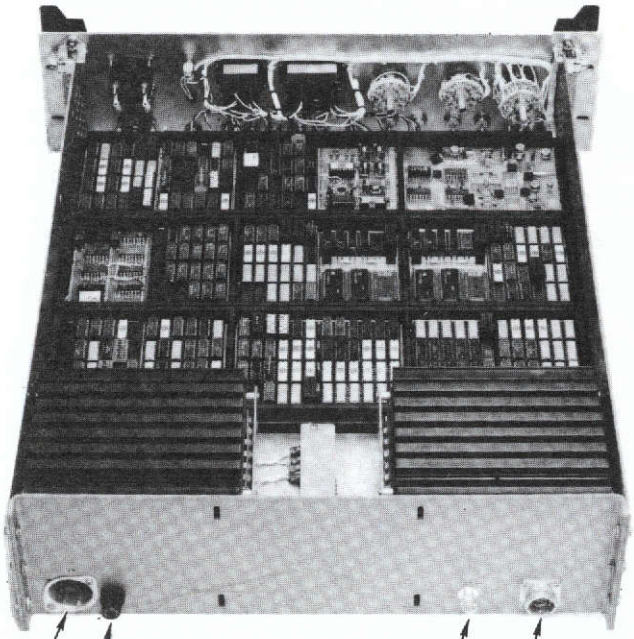


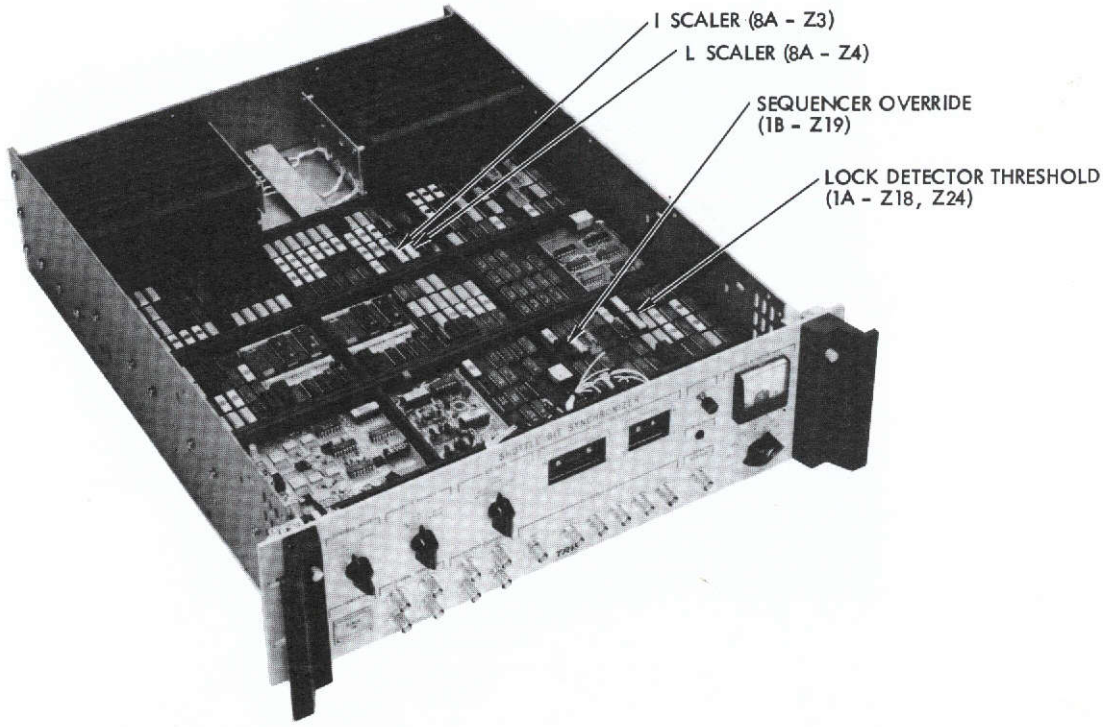
FUSE (16)
A 3 AMPERE FUSE (BUS F02A OR EQUIVALENT).

REMOTE MODE CONTROL CONNECTOR (18)
A CONNECTOR FOR INTERFACE TO TEST SET OR OTHER CONTROLLING EQUIPMENT. THE CONNECTOR IS A 7419E DEUTSCH 460-14-19PW-3005.

POWER CONNECTOR (15)
115 VAC THREE WIRE PLUG WHICH IS GROUNDED TO THE CHASSIS. ALL OF THE CIRCUITRY IS GROUNDED TO A SEPARATE AND ISOLATED EXTERNAL GROUND POINT.

EXTERNAL CLOCK (17)
A CLOCK INPUT AT 256 TIMES THE BIT RATE FOR USE WHEN "EXTERNAL REFERENCE" IS SELECTED ON THE FRONT PANEL.

Figure 3-2. Back Panel Connectors



INTERNAL SWITCHES

INTERNALLY THERE ARE THREE SETS OF SOCKET LOCATIONS WHICH HAVE PREWIRED COMPONENT CARRIERS INSERTED BUT WHICH CAN BE REPLACED WITH DUAL-INLINE-PACKAGE SWITCHES (AMP 7419 OR EQUIVALENT) IF DESIRED. THE FUNCTIONS CONTROLLED INCLUDE THE ACQUISITION AND TRACK MODE BANDWIDTH SELECT SWITCHES (I AND L SCALERS), LOCK DETECTOR THRESHOLD, AND THE ACQUISITION SEQUENCER OVERRIDE.

I AND L SCALER SWITCHES (18)

THERE ARE TWO ROCKER ACTIVATED DIP SWITCHES WHICH CONTAIN 8 INDEPENDENT SPST SWITCHES. SWITCHES 1 THROUGH 4 CONTROL THE SCALER DURING TRACK AND SWITCHES 5 THROUGH 8 CONTROL THE SCALERS DURING ACQUISITION. I AND L SCALERS ARE USED TO ADJUST THE GAINS 2^{-I} AND 2^{-L} OF THE INTEGRATED AND LINEAR TERMS OF THE LOOP FILTER.

SEQUENCER OVERRIDE (19)

THIS SET OF SWITCHES IS PROVIDED TO INTERUPT THE NORMAL FLOW OF THE ACQUISITION SEQUENCE.

LOCK DETECTOR THRESHOLD (20)

USED TO SET THE LOCK DETECTOR THRESHOLD FOR OPTIMUM DETECTION PROBABILITY. THE TWO SETS OF DIP SWITCHES ALLOW THE THRESHOLD SETTING RESOLUTION TO 16 BINARY DIGITS, IN A 2'S COMPLEMENT REPRESENTATION. THE SWITCH ON POSITION REPRESENTS AN "O" AND THE "OFF" POSITION REPRESENTS A "1".

Figure 3-3. Internal Switches

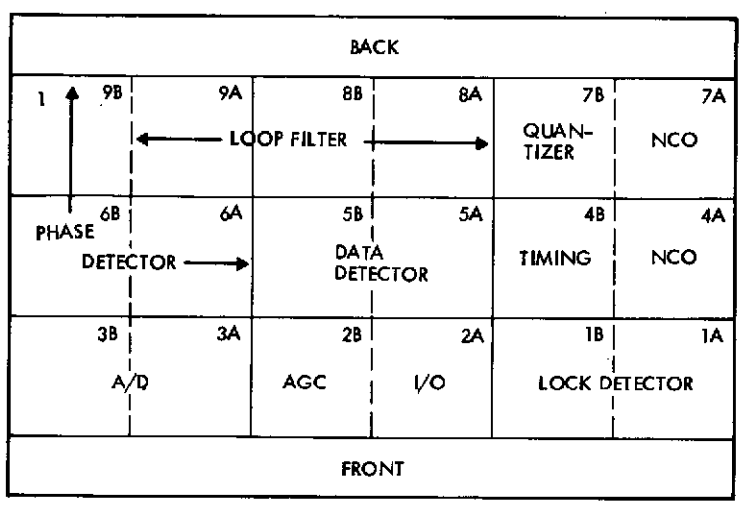


Figure 3-4. Top View of Module Partitioning

4. PERFORMANCE

4.1 PERFORMANCE SPECIFICATIONS

The performance of the bit synchronizer is evaluated in this section with respect to both the acquisition and tracking modes. In the acquisition mode, the specification of interest is the acquisition time which necessitates knowing the loop parameters B_L and ξ, and also the optimal sync detector threshold. To determine these quantities, the phase detector gain as well as the sync and ambiguity detector probabilities (of false lock and false dismissal) must be known. In the tracking mode the specifications of interest are phase jitter (of the recovered clock) and the bit error rate (BER). The BER is evaluated by comparing the actual value against the theoretical and determining the signal-to-noise ratio (E_b/N_o) of that value. BER degradation is then the difference, in dB, between the actual value of the input E_b/N_o and the equivalent detected value of E_b/N_o.

In all the measurements discussed above, several parameters affect the measured performance. These include NRZ data transition density (T.D.), offset frequency (doppler), input phase jitter, baseline variation, and, of course, the value of E_b/N_o. Thus measurements and theoretical data are obtained, when practical and meaningful, as functions of these parameters.

4.2 TEST SET

In order to obtain the variety of performance data indicated above, a test set has been designed and supplied with the brassboard as shown in Figure 4-1. It is discussed in detail in the test set document and so will not be discussed here. It is sufficient to say that it, along with its associated commercial test equipment, is capable of supplying a stable signal (signal plus noise) to the bit sync over the range of values of E_b/N_o of -5 to + ∞. The basic accuracy of the value of E_b/N_o has been determined to be $\pm$ 0.3 dB.

4.3 COMPARISON OF EXPERIMENTAL AND THEORETICAL RESULTS

Prior to evaluating the performance of the unit as a bit synchronizer, measurements on several portions of it need to be made. These include the AGC - A/D converter
ments on several portions of it need to be made. These include the AGC - A/D con-
verter, the phase detector, and the sync and ambiguity detector. From that information, meaningful results can be obtained for the performance of the entire bit synchronizer.

4.3.1 AGC - A/D Converter Tests

The analog front end of the bit synchronizer brassboard, consisting of the input conditioning, AGC, and A/D converter, is best characterized by two tests. The first is

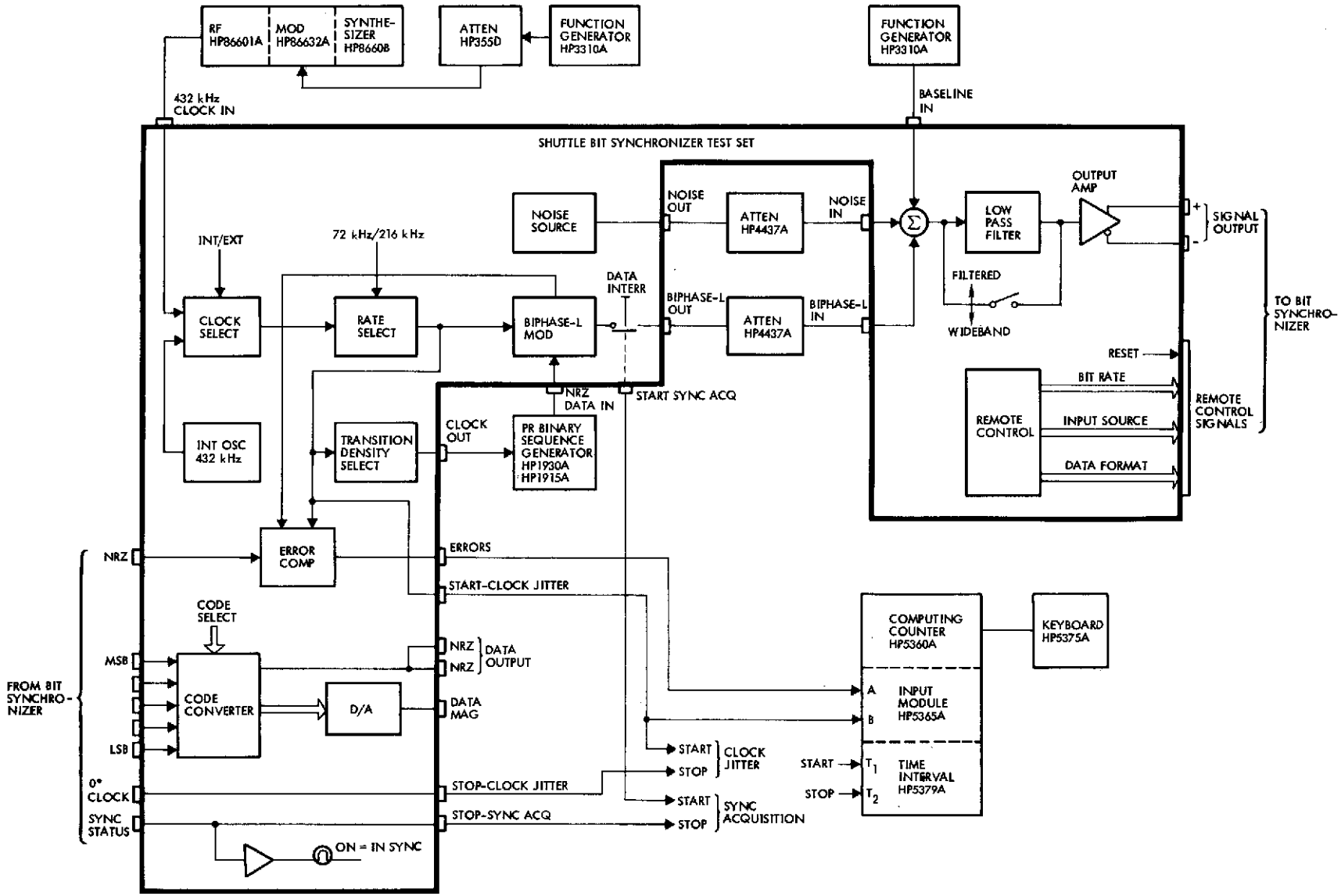


Figure 4-1. Test Set Block Diagram

second is a noise power ratio (NPR) test. The results of the loading tests are shown in Figure 4-2. Notice that the AGC control was not exercised over its specified input range of 0.5 to 5 V rms. This is due to the inability of the test set to generate such levels. However, the linearity display at E_b/N_o, such as + ∞ indicates that the AGC will, in fact, meet the required tolerance of ±0.1 dB. The difference in loading between high values of E_b/N_o, such as + ∞, and at those in the specified operating range (-5 to +7 dB) arises because of the use of an absolute value detector in the AGC rather than a true rms detector. However, such loading variations occur only at higher values of E_b/N_o where they do not affect either the bit synchronizer or the convolutional decoder performance.

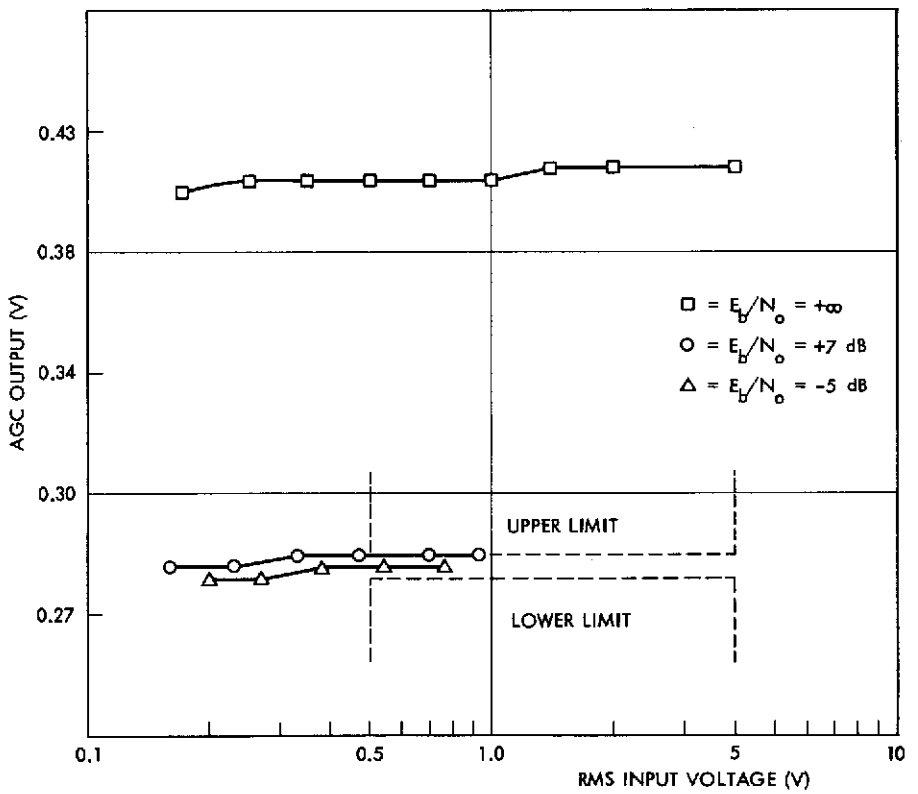


Figure 4-2. AGC Control

This second test uses a "notched" bandlimited noise (at a bandwidth of one-half the A/D sampling rate) as input to the AGC. Measurement of the D/A converted output of the A/D with a narrowband filter centered at the original notch yields a measure of the total distortion of the two units. For comparison, theoretical results have been obtained for the case of a 4-bit A/D and D/A converter. Table 4-1 presents the results of NPR tests upon the bit synchronizer's AGC and A/D.

Table 4-1. Noise Power Ratio Test Results

Input Level	Optimal Loading		NPR	
	Measured	Predicted*	Measured	Predicted*
0.5 V(rms)	0.287 V(rms)	0.283 V(rms)	19.5 dB	19.3 dB
4.0	0.300	0.283	20.5	19.3
5.0	0.290	0.283	20.0	19.3

* TRW Memo 7132.25-04, D. J. Secor "A/D Performance on Baseband and IF Gaussian Processes."

4.3.2 Phase Detector Characteristics

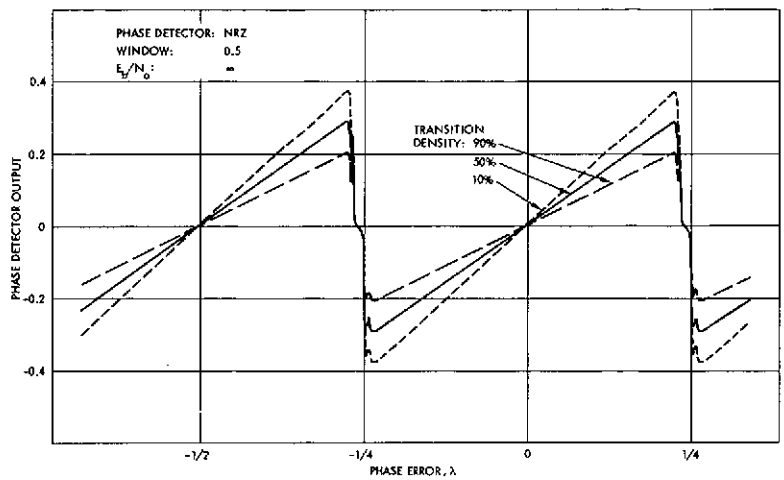
The phase detector is best characterized by observing its output as a function of normalized phase offset, λ. From such graphs, K_ϕ, the slope at the lock point, as well as other properties, can be obtained. Figures 4-3a, b, and c show a set of curves at three different values of E_b/N_o and three different transition densities, for the twice bit rate NRZ phase detector as used while the unit is acquiring the signal. The slope at $\lambda = 0$, i.e., the gain of the phase detector is tabulated in Table 4-2 for all cases. Shown in Figures 4-4a, b, and c and Table 4-3 are the phase detector curves for the Manchester phase detector as used in the tracking mode.

Table 4-2. Twice Rate NRZ Phase Detector Gain

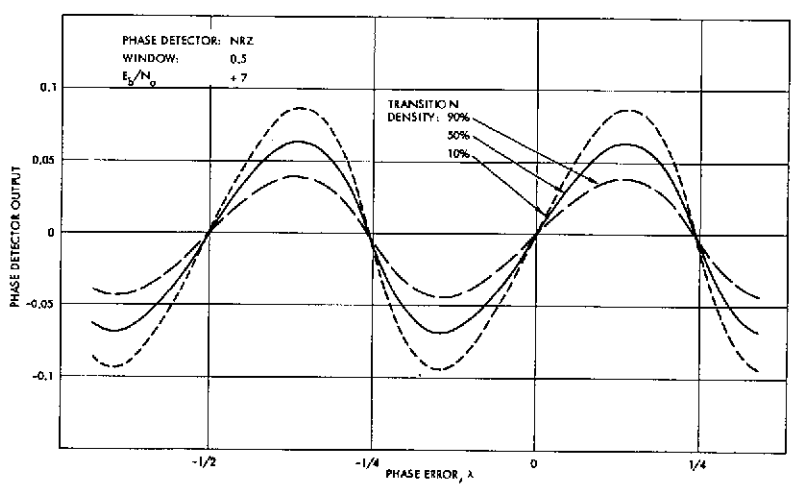
Signal-to-Noise Ratio / Transition Density	∞		+7 dB		-5 dB	
	Theo-retical	Experi-mental	Theo-retical	Experi-mental	Theo-retical	Experi-mental
10 percent	1.078	1.175	0.682	0.856	0.073	0.121
50 percent	0.850	0.910	0.539	0.607	0.0576	0.069
90 percent	0.624	0.642	0.394	0.414	0.042	0.037

Table 4-3. Manchester Phase Detector Gain

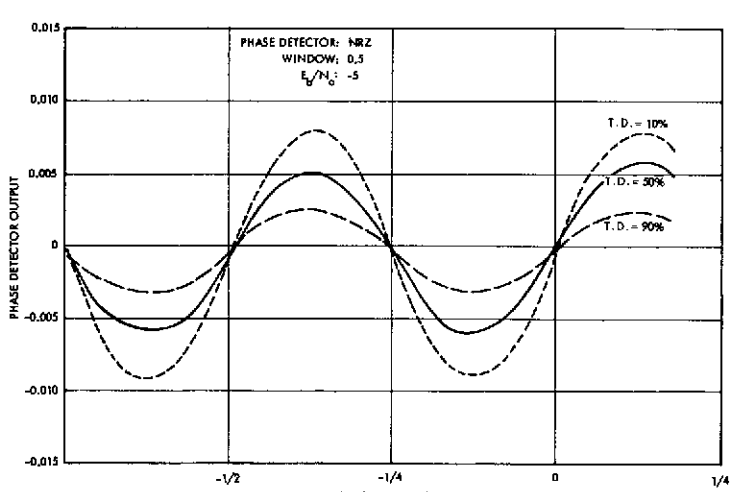
Signal-to-Noise Ratio / Transition Density	∞		+7 dB		-5 dB	
	Theo-retical	Experi-mental	Theo-retical	Experi-mental	Theo-retical	Experi-mental
10 percent	1.08	1.14	0.754	0.87	0.102	0.158
50 percent	0.850	0.848	0.588	0.67	0.0792	0.121
90 percent	0.622	0.63	0.43	0.46	0.058	0.074



a) $E_b/N_o = \infty$



b) E_b/N_o = 7 dB



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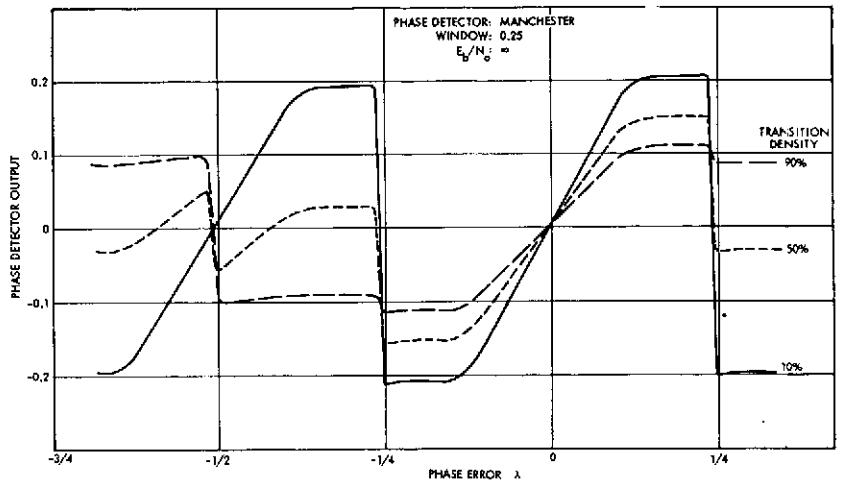
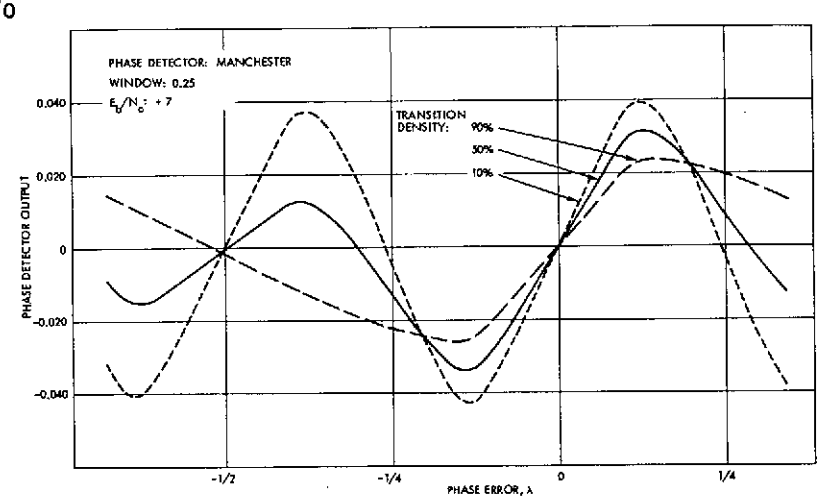
c) E_b/N_o = -5 dB

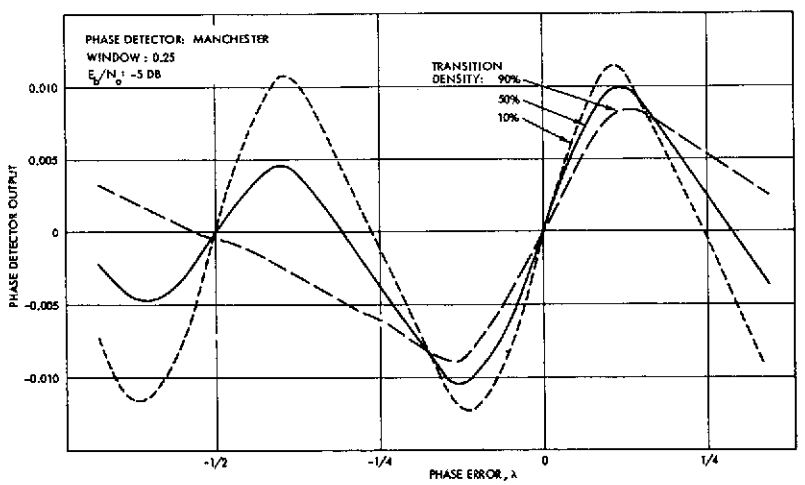
Figure 4-3. NRZ Phase Detector vs Normalized Phase Error



a) $E_b/N_o = \infty$



b) $E_b/N_o = 7$ dB



c) $E_b/N_o = -5$ dB

Figure 4-4. Manchester Detector vs Normalized Phase Error

Notice that the NRZ phase detector has two stable lock points (i.e., positive slope and zero value) at $\lambda = 0$ and $-1/2$. These correspond to the proper and ambiguous lock points common in any Manchester encoded system. The ambiguous point is detected in and corrected by the ambiguity detector discussed in Section 4.3.3 and thus this point presents no problem. On the other hand, the Manchester phase detector has the stable lock point at $\lambda = 0$ and two additional stable points in the range $-3/4\ \lambda$ to $-1/4\ \lambda$ whose existence and location are dependent upon transition density and signal-to-noise ratio. Thus the Manchester phase detector is not usable as an acquisition mode phase detector. However, comparison of the slopes of the two-phase detectors indicates that the Manchester phase detector has a higher value at the threshold condition, and its value does not vary as much over the range of parameters as does the slope of the NRZ phase detector. Thus, the resulting variations in B_L and ξ over that range are less. A set of curves is shown in Figures 4-5a and b showing the theoretical variation in phase detector gains as a function of the phase detector type, the transition density, and E_b/N_o. Notice that the range is approximately 33:1 and 25:1 for the NRZ and Manchester phase detectors, respectively.

An inherent property of both of the phase detectors is that there is an E_b/N_o dependent dc shift of their curves whose magnitude is on the order of a least significant bit. Uncorrected, this can prevent the unit from acquiring at -5 dB. The adder on the output of the phase detector is used to compensate this offset. Because of the increase in slope of the phase detector curves at higher values of E_b/N_o, the added offset does not reflect itself in a phase offset at those points.

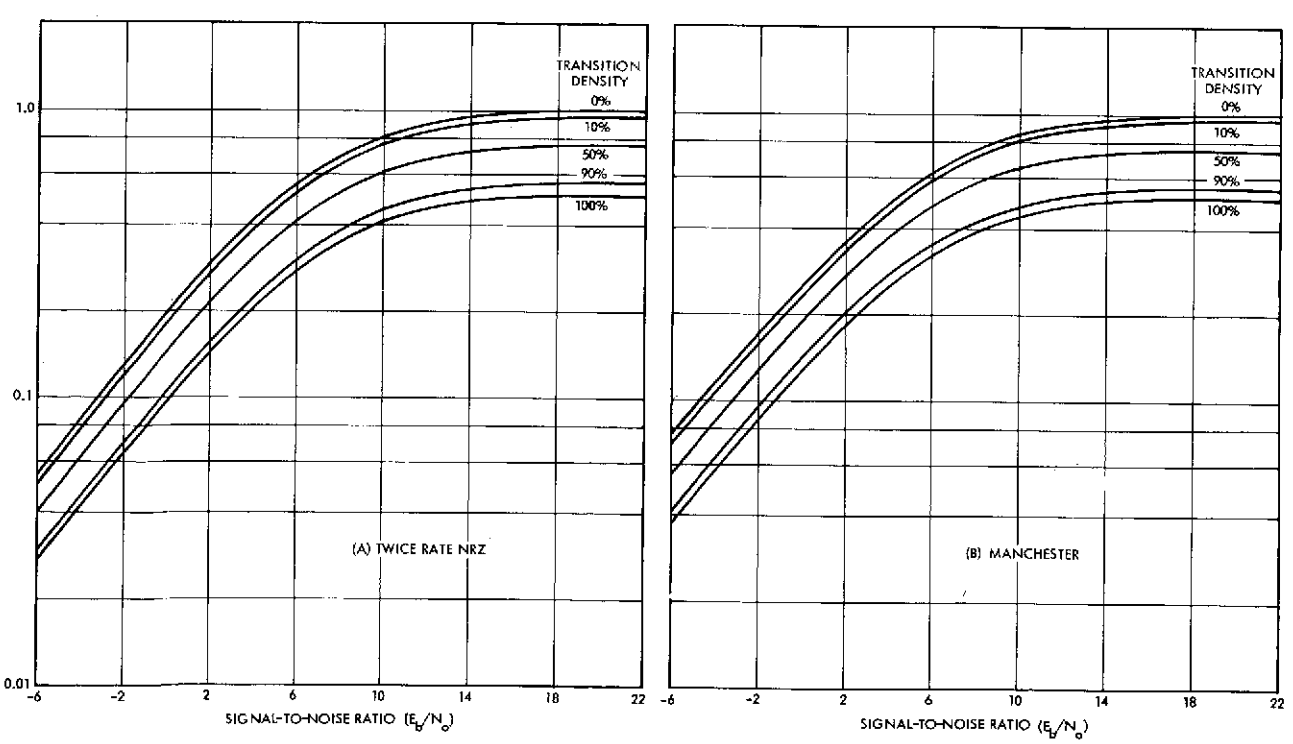


Figure 4-5. Normalized Phase Detector Gain

4.3.3 Sync and Ambiguity Detector Performance

An experimental sync detector normalized phase error curve is shown in Figure 4-6 for the case of 0 percent and 100 percent transition density and E_b/N_o = +7 dB. Notice that the peak values occur at $\lambda = 0$ and $\lambda = -1/2$, and that the ratio of the peak value at $\lambda = 0$ for the two transition densities is 2, exactly as predicted in the discussion of the lock detector in Section 2.5. In order to further evaluate the lock detector, the optimal threshold must be determined and then the probability of false acquisition (P_{FA}) and false dismissal (P_F) measured or predicted. The latter approach is taken since the probabilities involved are less than 10^{-8} and, as such, are unmeasurable. In order to determine the threshold, a set of random samples of the sync detector output was obtained for an integration time of 2^{14} bit times and their mean and variance computed. From this information, the optimal threshold was determined to be 120 for $P_{FA} = P_F = 10^{-13}$. The conditions under which the two sets of data were taken are as follows: (1) $E_b/N_o = -\infty$ dB and (2) E_b/N_o = -5 dB, transition density = 90 percent. The results are tabulated in Table 4-4.

The ambiguity detector whose transfer curve is shown in Figure 4-7 for 100 percent transition density and E_b/N_o of ∞, +7 dB, and -5 dB, is experimentally evaluated in the same way as the lock detector in that the mean and variance of the output of the ambiguity detector are computed for the case of E_b/N_o at -5 dB and a transition density of 50 percent as shown in Table 4-5. Since the optimal threshold is zero, it is necessary only to predict the probabilities of false dismissal of ambiguity, P_F, and of false acquisition of ambiguity, P_{FA}. These were found to be less than 10^{-42}.

Table 4-4. Sync Detector Threshold Statistical Measurements

Signal Conditions		Mean	Variance
E_b/N_o	T.D.		
$-\infty$	--	3.9	260
-5	90%	243	298

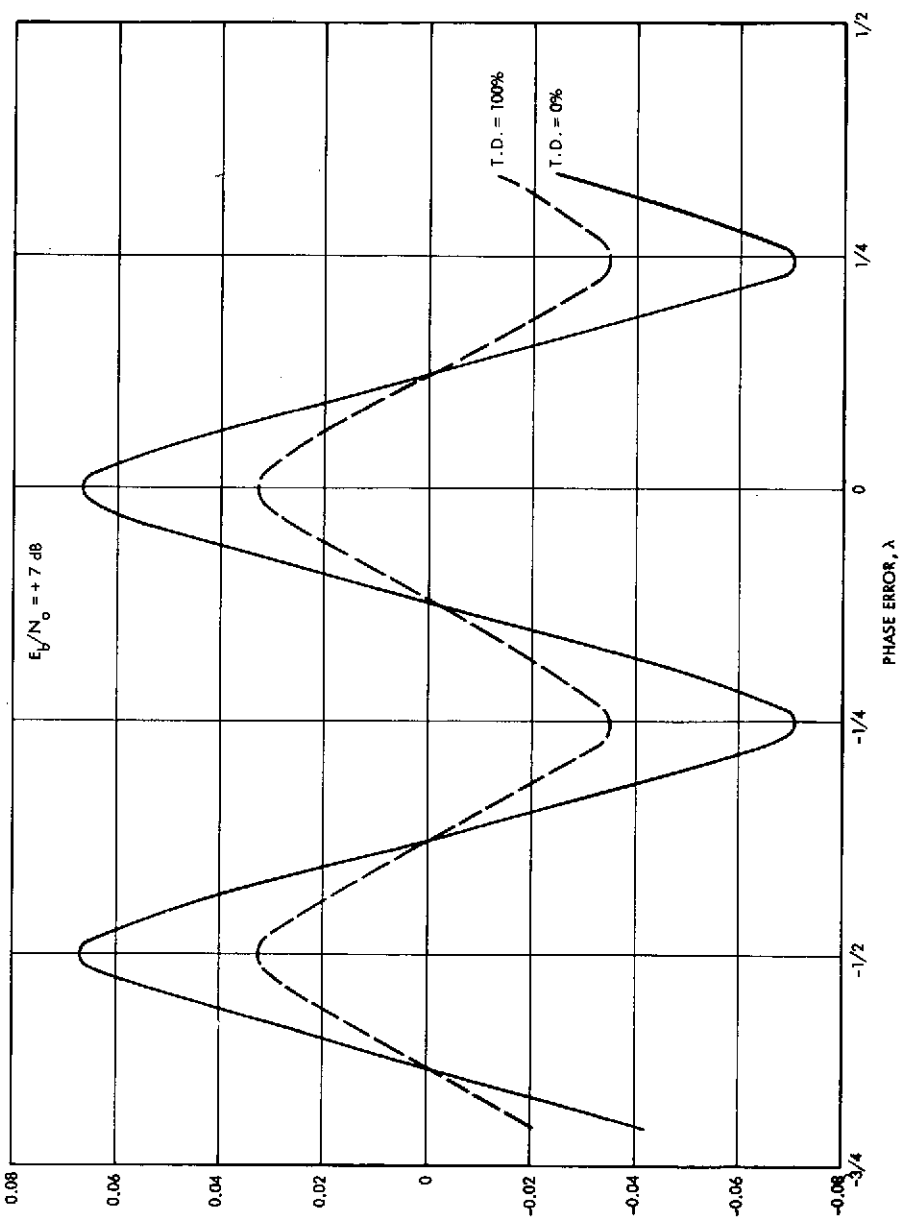


Figure 4-6. Sync Detector vs Normalized Phase Error

Table 4-5. Ambiguity Detector Statistical Measurements

Signal Conditions			Mean	Variance
E_b/N_o	T.D.	Lock Point		
-5	50%	0	312	518
-5	50%	-180	-311	462

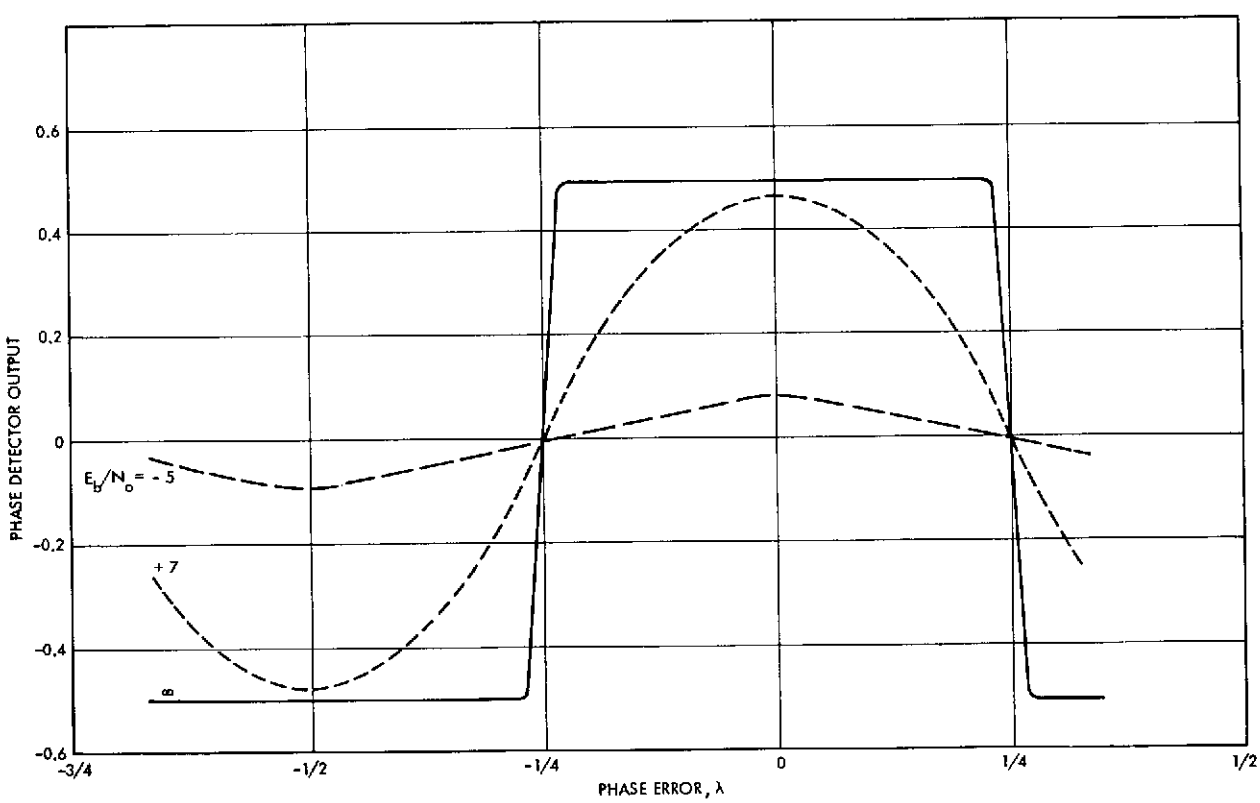


Figure 4-7. Ambiguity Detector vs Normalized Phase Error

4.3.4 Acquisition Time

A very important measure of a bit synchronizers performance is that of acquisition time, especially for the worst case condition of low E_b/N_o and high frequency offset. For the sake of discussion, the average acquisition time, $\overline{T}_A$, is defined as the mean time from the application of the Manchester encoded data to the time at which the sync indication indicates synchronization has occurred. Prior to the application of the data, a noise-only signal is applied to the bit sync, and all memory in the unit is preset to zero.

Figure 4-8 represents a plot of measured $\overline{T}_A$ versus E_b/N_o for various values of the NRZ transition density (TD). In addition, a straight line through the specification limit points of -5 dB and +7 dB are demonstrated. This figure illustrates the fact that synchronizer performance is well within the specification for various values of NRZ transition density and signal-to-noise ratios.

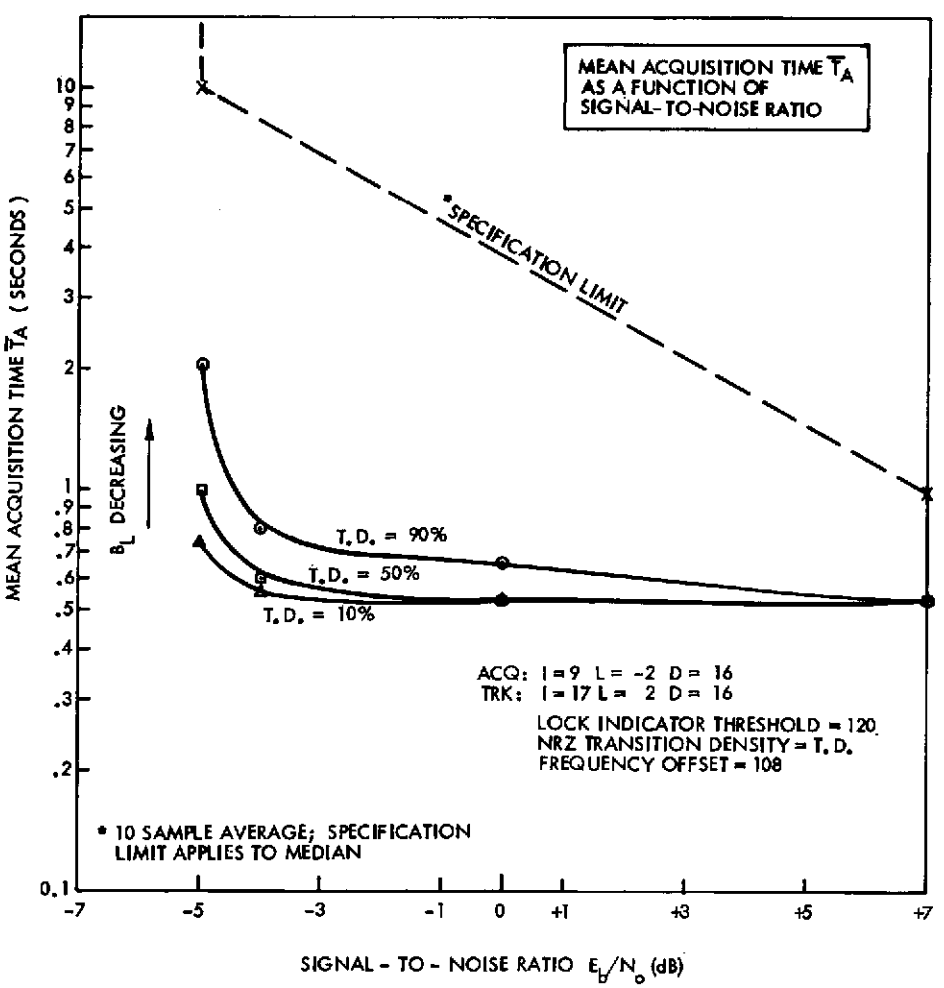


Figure 4-8. Mean Acquisition Time as a Function of E_b/N_o

In evaluating the figures, it should be kept in mind that a fixed interval of 0.4 to 0.6 seconds is required between the time the clock tracking loop has acquired the signal (in the wideband acquisition mode) and before the lock indicator detects this fact and sequences the loop configuration into the tracking mode. Thus the minimum acquisition time shown in the figures consists almost entirely of system overhead time. In any event, the mean acquisition time satisfies the specification by a factor of 2 to 5 over the range of interest of the various parameters. The results seem to indicate that the acquisition time grows rapidly in the vicinity of -5 dB. In fact, theory has predicted a mean acquisition time of 2 seconds for a E_b/N_o of -5 dB and transition density of 50 percent, while a few milliseconds are required at +7 dB for 50 percent transition density. At -5 dB, the acquisition bandwidth chosen for theoretical calculations was 540 Hz with a doppler frequency of 108 Hz assumed. However, the actual bandwidth used is 200 Hz.

Figure 4-9 demonstrates the mean acquisition time versus frequency offset for the design point E_b/N_o of -5 dB and various transition densities. Although theory would say that $\overline{T}_A$ versus Δf is symmetric about $\Delta f = 0$, there is slight asymmetry being demonstrated for TD = 90 percent. This is probably due to the fact that too few a number of samples were taken in obtaining the statistical estimate for $\overline{T}_A$; i.e., at low SNR the variance of $\overline{T}_A$ for 10 samples is appreciable and is transition density dependent. Also there may be residual dc offset in the loop due to the phase detector. In addition, the increase in $\overline{T}_A$ as a function of increasing transition density is in agreement with theoretical predictions. This is due to the fact that the bandwidth narrows as transition density increases; therefore a longer acquisition time is required for a given E_b/N_o and frequency offset.

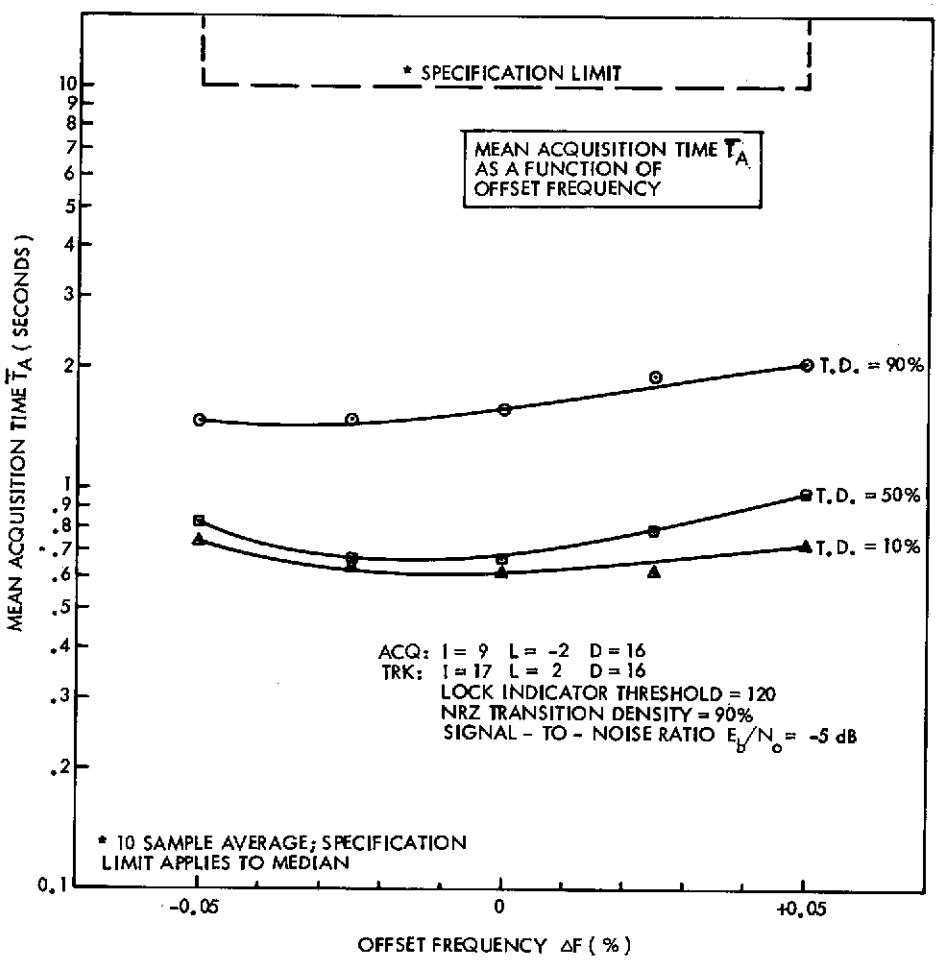


Figure 4-9. Mean Acquisition Time as a Function of Offset Frequency

4.3.5 Loop Parameters

The theoretical values of loop noise bandwidth (B_l) and loop damping (ξ) have been calculated and measured, and the results are shown in Figures 4-10 and 4-11. Notice that, for the acquisition mode, the two estimates track but differ by a fixed ratio.

A problem arose in measuring the loop parameters at low values of E_b/N_o in the acquisition mode due to random phase jitter present in the loop. Any additional excitation which is necessary to measure B_L and ξ invariably causes the loop to break lock. More work needs to be performed to define measurement techniques under these conditions.

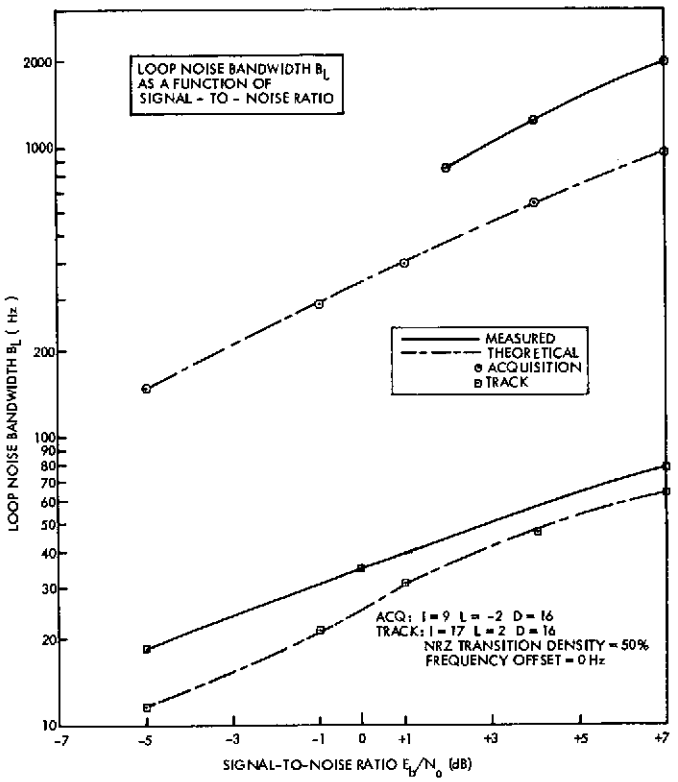


Figure 4-10. Loop Noise Bandwidth

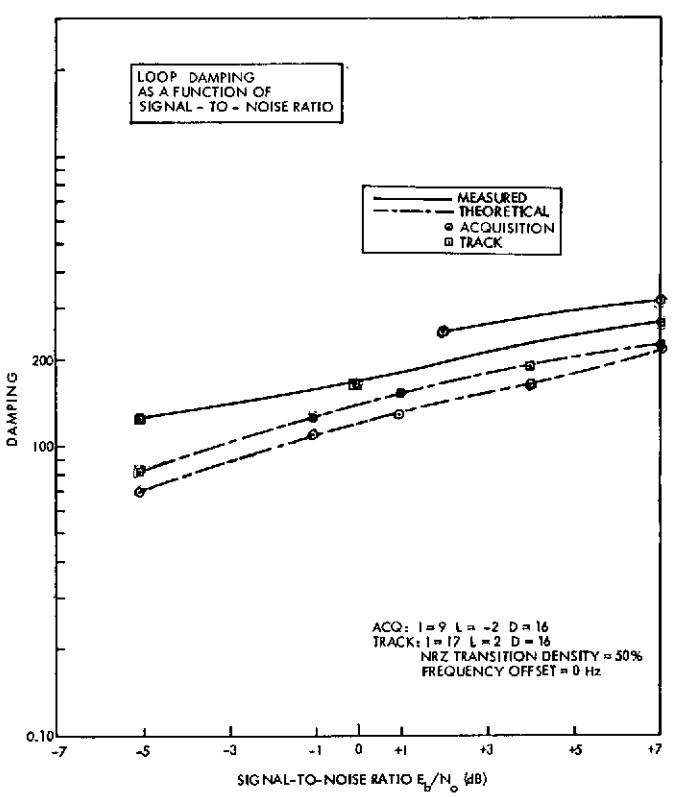


Figure 4-11. Loop Damping

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4.3.6 Phase Jitter

The experimental and theoretical rms phase jitter as a function of E_b/N_o and acquisition or track mode is shown in Figure 4-12. It can be seen that the unit meets the specified value of 1 percent rms phase jitter at -5 dB. Because of the chosen implementation of the numerically controlled oscillator, a minimum value of phase jitter of 0.1 percent will be present even at very high values of E_b/N_o and this effect accounts for the deviation from theoretical that is present.

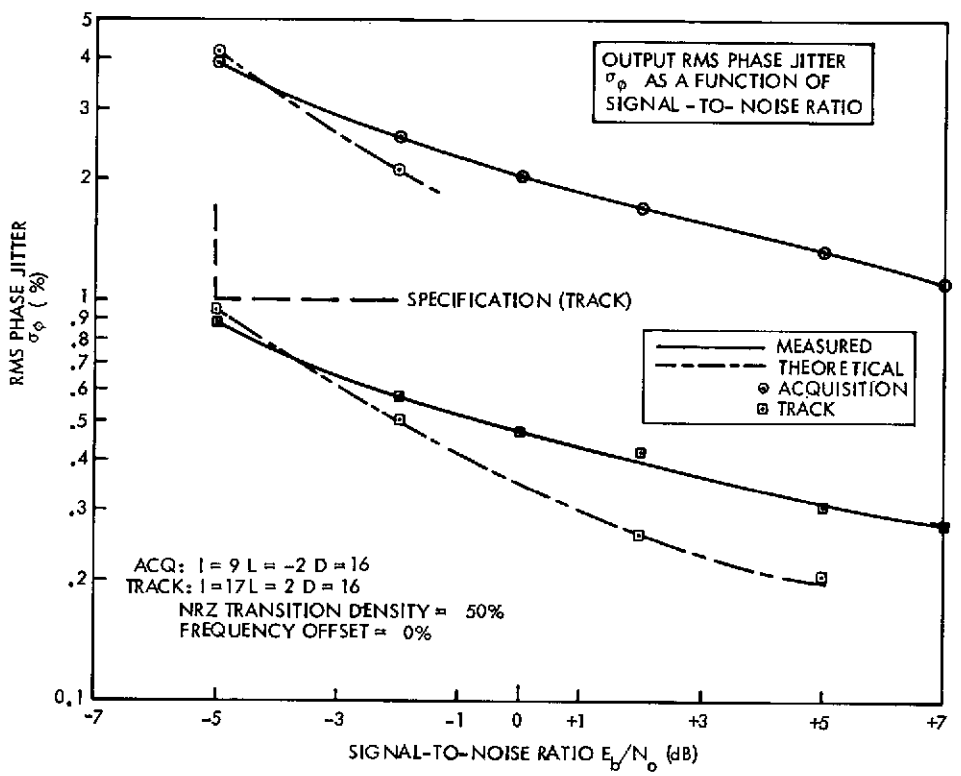


Figure 4-12. Phase Jitter

4.3.7 Bit Error Rate

Bit error rate (BER) is the means by which the bit synchronizer is evaluated while in the tracking mode. The optimum theoretical performance of the unit is a well known tabulated function and is plotted versus E_b/N_o in Figure 4-13. The difference between the E_b/N_o that is present at the input and the equivalent value of E_b/N_o for the measured error rate is defined as the BER degradation. Parameters that can contribute to this degradation include band limiting of the input signal,

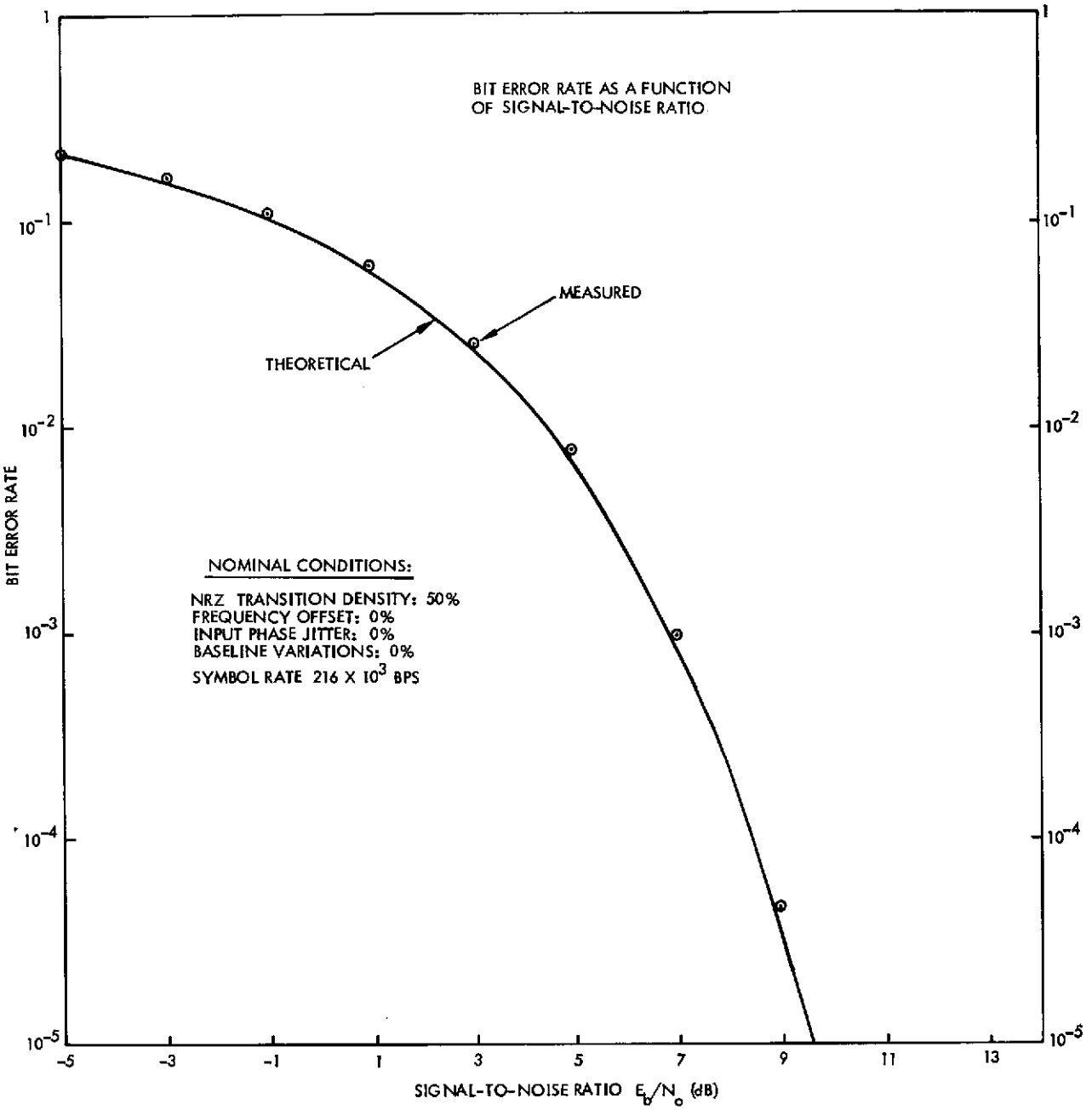


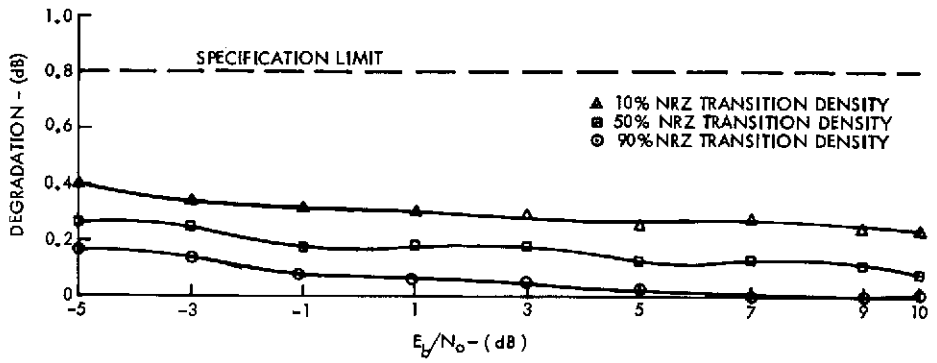
Figure 4-13. Bit Error Rate

finite sampling rate, finite quantization phase jitter (and hence transition density), and baseline variation and frequency offset. Four curves are shown in Figure 4-14 showing degradation versus E_b/N_o for the parameters transition density, frequency offset, baseline variation, and input phase jitter. In the case of curves b and c, these parameters result in no measureable change in degradation as they are varied. Figure 4-15 shows the computed theoretical degradation for a bit synchronizer corresponding to Figure 4-14a. At +10 db E_b/N_o and a transition density of 90 percent, the experiment data indicates no degradation, while the theoretical prediction is 0.14 dB. It appears that there is about 0.1 dB bias in the setting of the E_b/N_o in the test set. In general, there is good agreement between the degradation predicted from theory and the experimental data.

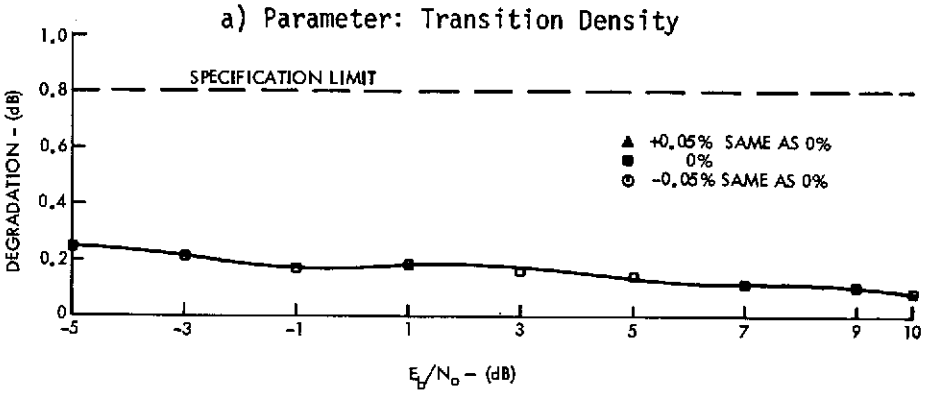
The specification of the bit synchronizer brassboard is that the maximum degradation shall be less than 0.8 dB. An error budget showing predicted degradations is shown in Table 4-6.

Table 4-6. Bit Synchronizer Data Degradation Budget

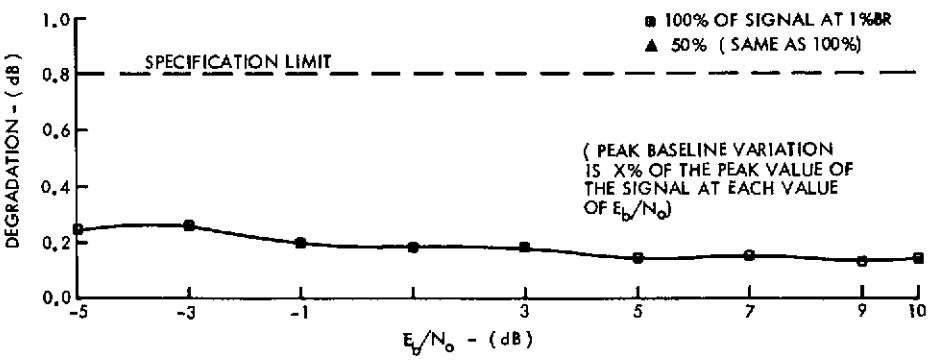
Parameter	TD	E_b/N_o = -5 dB Degradation (dB)	E_b/N_o = +10 dB Degradation (dB)
Filtering (BT = 10) and 32 Samples Per Bit	100%	0.20	0.20
	50%	0.15	0.15
	0%	0.10	0.10
Quantization (amplitude) 4-bits		0.033	0.06
100 percent baseline variation		0.001	0.012
Jitter at -5 dB 1 % input 3.6° Loop 3.6° } RSS 5.3° NCO 1.5° 5.3° = 0.1 2.7° = 0.05 Jitter at + 10 dB 1 % input 3.6° Loop 1.6° } RSS 4.2° NCO 1.5°		0.15	0.08
Total degradation	100%	0.38	0.40
	50%	0.32	0.35
	0%	0.28	0.30



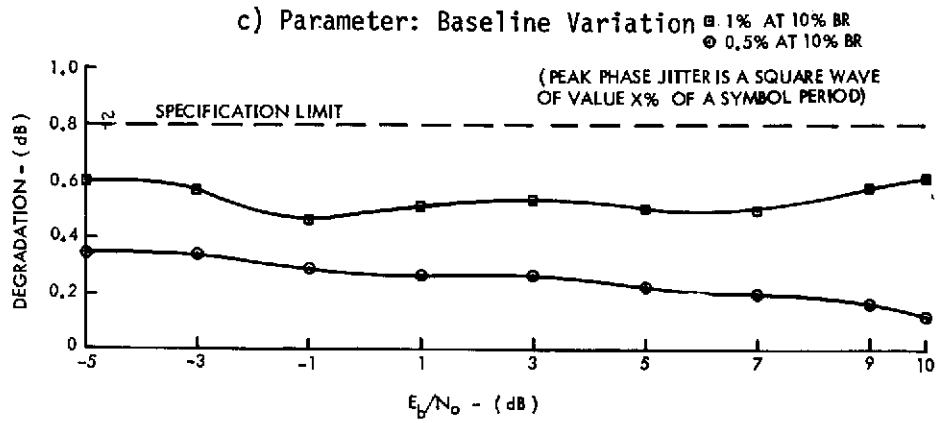
a) Parameter: Transition Density



b) Parameter: Frequency Offset



c) Parameter: Baseline Variation



d) Parameter: Input Phase Jitter

Figure 4-14. Bit Error Rate Degradation vs Signal-to-Noise Ratio (E_b/N_o)

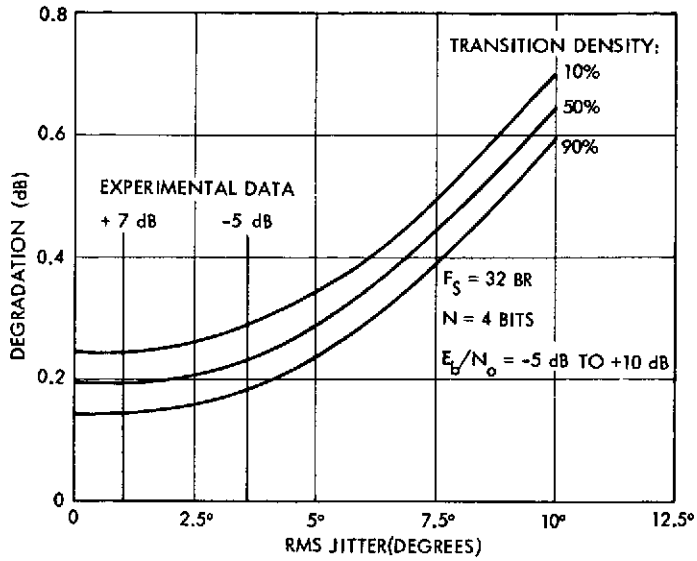


Figure 4-15. Bit Error Rate Degradation vs Phase Jitter

4.3.8 Combined Operation of Bit Synchronizer — Convolutional Decoder

Although not part of the contract requirements, the bit synchronizer brassboard has been operated with an eight-level convolutional decoder (rate 1/3, constraint length = 7). The acquisition time performance is comparable to the bit synchronizer alone, as the decoder acquires well within the sync detection sequencing time. The BER performance of the combined units is shown in Figure 4-16 where the theoretical performance of the decoder is that obtained in a simulation for a rate 1/3 code. The energy per information bit (E_{ib}) is three (4.8 dB) times greater than the energy per bit. Thus the two scales shown on the figure differ by the 4.8 dB factor. The data points that are on the ideal curve were taken with the input 3-bit words having true Gaussian statistics, whereas the experimental data points obtained with the bit synchronizer brassboard have a degradation of 0.6 dB. The additional degradation over that of the bit sync, which is about 0.3 dB, is thought to be due to the bit sync soft decision output having non-Gaussian statistics.

Table 4-7 shows the actual degradation over the measurable range. Note that no simulation results are available for the low SNR region, and comparison is impossible.

Table 4-7. BER Degradation of Combined Bit Synchronizer — Convolutional Decoder

SNR		BER Degradation
E_b/N_o	E_{ib}/N_o	
0	4.8	0.8
-0.5	4.3	0.8
-1	3.8	0.7
-1.5	3.3	0.7
-2.0	2.8	0.67
-2.5	2.3	0.65

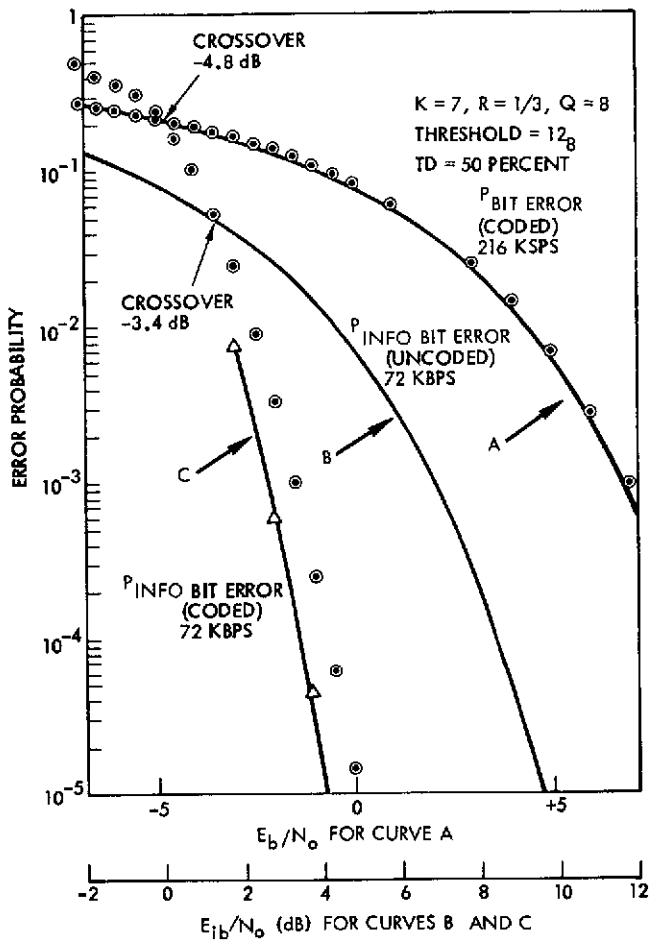


Figure 4-16. Bit Error Rate Performance of Combined Bit Synchronizer-Convolutional Decoder