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# APOLLO

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## GUIDANCE COMPUTER AND ASSOCIATED GROUND SUPPORT EQUIPMENT

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**QUARTERLY  
TECHNICAL REPORT  
NO. 2  
FR-2-29**

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 Quarterly Technical Report, 1 Oct. - 31 Dec.  
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QUARTERLY  
TECHNICAL PROGRESS  
REPORT NO. 2

FR-2-29

Reporting Period  
1 October 1962 - 31 December 1962

Prepared by  
RAYTHEON COMPANY  
MISSILE AND SPACE DIVISION  
Sudbury, Massachusetts

for  
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1. INTRODUCTION

This is Quarterly Technical Progress Report No. 2 issued in place of Monthly Technical Progress Report No. 6 in accordance with Work Statement for Industrial Support E-1097. A monthly report is not required when a quarterly is issued. The next Progress Report issued will be Monthly Technical Progress Report No. 7. Information normally contained in No. 6 is contained in this report.

This Quarterly Technical Progress Report covers the period 1 October through 31 December 1962. Forty-eight Technical Directives have been received to date; seven have been completed.

Raytheon Milestone Charts for the AGC and GSE are shown in figures 1 and 2 respectively. These charts were drawn to NASA format with arrows depicting Design and Development or Delivery milestones. Filled-in arrows depict a completed milestone; blank arrows depict incomplete ones. Up-dating of these charts will be performed on a monthly basis and will be included within this report. Discussions will be included when applicable.

A revised GSE fragnet was submitted on 7 December 1962. This fragnet more accurately describes present development plans. The revised AGC fragnet is currently being prepared and will be submitted to MIT/IL when finalized.

2. INDUSTRIAL SUPPORT

2.1 APOLLO GUIDANCE COMPUTER

Micrologic circuit investigations have been expanded. Efforts are being directed toward verifying the capabilities of micrologic elements under all possible conditions. The elements will be separated into groups for testing; each

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group having a particular goal. Each element of a group will be subjected to similar test conditions to provide a basis for comparison. Extrapolation may be necessary to obtain absolute worst case performance. In addition to performance characteristics, the subtleties of micrologic will also be studied.

Operation of micrologic elements at reduced supply voltages to conserve power are being examined. A mathematical analysis of the sense amplifier is nearly complete. Ground planes and capacitors have been recommended for the AGC as a precaution against ground noise. Several ground planes will be evaluated, while mated with an actual stick.

Fabrication of the arithmetic sticks for the AGC breadboard has begun. One stick has been completely constructed and tested. A test procedure has been established to facilitate testing the remaining sticks. Preliminary programs are being written to check-out the breadboard computer.

Efforts are being made to provide a single stick tester capable of testing all micrologic sticks. Special attention has been given to the problems in providing such a machine having automatic error detection capabilities. Preliminary design of the erasable memory tester has been completed.

Power supplies for the AGC have been breadboarded and are currently being tested. Efforts are being made to provide an output voltage which will vary by a predetermined amount with temperature. Efforts are also being conducted on a duty cycle controlled voltage regulator. This approach offers the prospect of greater efficiency.

Configuration of the micrologic stick has been changed. The latest design incorporates an "I" section as a separator for the micrologic elements. Interconnections of the two logic sections are made by utilizing a wire-wrapped block connector. A prototype stick is being fabricated for evaluation, using dummy micrologic elements.

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Process sheets have been prepared for master welding tape preparation and for punching, winding, and welding of matrices. These process sheets are incomplete due to lack of information on final matrix configurations. Raytheon is investigating the requirements for a miniature wire-wrap capability.

All phases of the resistance welding study have been completed except for life testing, final test (after welding), and data analysis. Preliminary design of a rope threader has been completed and will be submitted to MIT/IL for evaluation. A locating fixture is being designed to be used in conjunction with the threader and can be manually operated or programmed using a tape reader and logic combination.

Four welding heads have been added to the matrix fabricator to provide the full capacity of seven welders. A channel selector and pushbutton have been added to the control circuitry to permit the operation of individual welders. Power supply cables were lengthened to allow relocation of the welder power supplies. Comprehensive evaluation of matrix weld strengths is in progress. This evaluation includes visual inspection, pull testing, and photomicrographs.

#### 2.1.1 Core Rope Tester

In AGC-4 12,228 words of fixed memory are divided into three separate physical groups called "ropes". Each rope stores 4096 words in 1024 cores. Words are 16 bits long and there are 4 words per core so 64 sense lines are required in each rope. Because it is desirable to maintain advantageous signal to noise ratios it is not desirable to have sense lines long enough to thread 1024 cores. Each rope actually contains 128 sense lines each long enough to thread 512 cores. Sixteen sense lines make up a 16 bit word. A rope with its 128 sense lines has eight groups of 16 sense lines called "strands"; each strand is 512 cores long so there are 512 words per strand. There are eight separate sets (128) of sense lines or strands in each rope and therefore 24 strands (384) among which to select.

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Information in the fixed memory is stored geometrically and is not electrically alterable. As a matter of fact functional requirements for the fixed memory are that it be permanent, insensitive to accidents of input-output, and to failures in other parts of the computer. These functional requirements and sheer equipment complexity reflect the importance of core rope fabrication and testing.

Fabrication of a core rope tester breadboard is complete and electrical check-out has begun. The tester compares core rope output with a predetermined program tape. Two capabilities are provided: a test capability and an instruction capability. The test philosophy established is to test one sense line at a time. This approach offers two important advantages; it minimizes the degree of test set complexity and allows core rope testing before the rope is completely constructed. The detection of errors can therefore be made early in the manufacturing process. Instructions are stored on the program tape. The tester recognizes these instructions and tests sense line and word selection or memory output level.

Two modes of operation are provided under the test capability: manual and automatic. The automatic mode is the normal operating mode of the tester. Each address in a core rope is progressively selected and every output is compared with the predetermined program. A switch is provided (in automatic mode only) to control the number of cores to be scanned. The entire operation is controlled by the tape program. If the word read-out of the core ropes does not match the programmed word, error detection circuits halt further read-out and display the actual address of the incorrect word. A bypass switch is provided which will override halt circuits and allow testing to continue. However, closer observation of an error can be made by switching to the manual mode of operation. In the manual mode the tape reader is halted and the error detection circuits are disconnected.

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During the manual mode of operation only one core is selected repeatedly. An option is provided so the circuits can be made to "step" along the output of each sense line or to continuously monitor one sense line. In either case the output is available for a scope display. A sync pulse is provided to facilitate scope inspection. Time of sync pulse generation during the cycle can be controlled by a selector.

Every sense line is associated with each core. Therefore, before any one sense line is completely tested each core must be addressed while the output of the sense line is monitored. The program tape is subdivided into separate sections separated by tape feed characters. Each subdivision contains information required to test one sense line completely. Each section of the tape contains 513 characters; one to select a particular sense line and to excite the rope word selection circuits, and 512 subsequent characters - each character addressing one of the 512 cores in two quarter ropes (one quarter rope consists of 4 substrands, 256 cores, and 1024 words. Four pluggable quarter rope modules make up a rope).

There are three types of information stored on the program tape: (1) sense line and word selection, (2) memory output level (1 or 0), and (3) manufacturing directions. A character consists of one group of eight parallel bits. The information category applicable to any one character is described by bits 7 and 8 which is the only function of these two bits. Information categories are designated by bits 7 and 8 as shown in table 1.

The core rope tester circuits recognize the information category code of bits 7 and 8, and select and furnish only that data corresponding to the code. During a test, for instance, only those characters which pertain to test conditions a and c in table 1 would activate circuits to provide test information.

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TABLE 1  
INFORMATION CATEGORY CODE

Condition	Bit 7	Bit 8	Information Category
a	0	1	Test; sense line and word selection
b	1	1	Manufacturing instructions
c	0	0	Test; memory output level (1 or 0)
d	1	0	Appears only during a tape-feed character

## 2.2 RELIABILITY AND QUALITY ASSURANCE

The study to determine the distribution of parameters for micrologic units is continuing. Statistical parameters have been determined for the micrologic units tested thus far.

A program to determine the mechanical reliability of Corning Glass resistors has been completed. Results will be documented at a later date.

During this reporting period, the Design Review committee met and conducted mechanical reviews of the GSE Calibration Equipment, Logic Drawer, resistor module, and diode module. Electrical reviews will be conducted at a later date.

## 2.3 FUNCTIONAL SUPPORT

The Preface and Index and Issue 1 of the Apollo Guidance Computer Information Series (AGCIS) are being revised to be compatible with the latest design concept. Issue 1 which concerns the erasable memory is currently being written and will be issued shortly. The revised edition of the Documentation Plan is shown in figure 3. Up-dating and expansion of this plan will be performed on a monthly basis.

DOCUMENTATION PLAN REVISION NO. I  
I DEC 1962

ITEM	TASK	DESCRIPTION	TYPE GROUP	TD NO.	QTY	STATUS
1.0	DEVELOPMENT PLAN MANUFACTURING SUPPORT FACILITIES	RAYTHEON FORMAT	II	TDR-2	1	COMPLETED SEPT 1962
2.0	SPECIFICATIONS AGC INTERFACE GSE INTERFACE SPECIAL PROCESS AND MATERIALS SCD'S	ND SIMILAR TO OD'S	I I I I	TDR-39 TDR-36/37	1 1 20 200	4 COMPLETE 27 COMPLETE
3.0	FACTORY TEST PLANS AGC GSE	RAYTHEON FORMAT	III	TDR-11	1 1	IN PREPARATION
4.0	PROCEDURES IN PROCESS TESTS IN PROCESS INSPECTION IN PROCESS ASSY FINAL ACCEPTANCE TESTS	RAYTHEON FORMAT  ND SIMILAR TO OD'S	III III III I			
5.0	REPORTS	RAYTHEON FORMAT			MONTHLY	
5.1	PROGRAM PROGRESS TD REPORT PROGRAM PLANNING MANAGEMENT		II II II	TDR-43		
5.2	TECHNICAL DATA & ANALYSIS		II	TDR-29	AR	
5.3	FAILURE DATA REPORT		II	TDR-43	AR	
5.4	EMERGENCY ACTION REPORT		II	TDR-43	AR	
5.5	MONTHLY TECHNICAL PROGRESS REPORT		II	TDR-21	MONTHLY	
5.6	QUARTERLY TECHNICAL PROGRESS REPORT		II	TDR-21	QUARTERLY	
5.7	RELIABILITY AND QUALITY CONTROL REPORTS		II			
5.8	QUALIFICATION TEST REPORTS		I			
5.9	MOTION PICTURE REPORT (TOTAL 20 MIN.)	20 MIN. TOTAL	II	TDR-43		
5.10	STILL PHOTOS	300 SHOTS (2 NEGATIVES & 3 PRINTS OF EACH)	II	TDR-43		
6.0	INFORMATION SERIES			TDR-30		
7.0	MANUALS					NOT STARTED
7.1	AGC FAMILIARIZATION		I			
7.2	AGC OPERATION & MAINTENANCE		I			
7.3	GSE OPERATION & MAINTENANCE 1. COMPUTER TEST SET 2. COMPUTER SIMULATOR 3. CALIBRATION EQUIPMENT		I			
8.0	DOCUMENTATION ADMINISTRATION			TDR-26		

AR = AS REQUIRED

Figure 3. Documentation Plan

3. COMPUTER CIRCUITS

The generation of noise on ground wires by micrologic elements was discussed in Quarterly Technical Progress Report No. 1. A study was made to determine the amount and character of such noise relative to various circuit configurations. A test set-up was established in which a pulse generator feeds a breadboard circuit.

The pulse generator feeds the breadboard circuit with a +3VDC pulse (PW = 4  $\mu$ sec, f = 50 KC) that switches eight micrologic G elements simultaneously. These eight elements are emitter connected to a heavy ground buss on the breadboard (figure 4). A ninth element is emitter connected to the same buss. The base of this ninth element is connected back to B+(+3VDC) through 620 ohms causing the ninth element to be in constant saturation.

The ground buss on the breadboard is connected to a quiet ground plane through three 10 inch nickel wires in parallel, plus one number 18 copper wire 12 inches long. The total wire length is 20 inches.

The output of the saturated ninth element is connected to the input of a tenth element. This tenth element, together with its follower elements, is emitter connected to the quiet ground plane. The switching of the eight elements produces a +0.8VDC (figure 5, A) pulse on the breadboard ground buss at point A, figure 4. This pulse is coupled through the saturated ninth element and appears as a +0.26VDC level at the collector of the saturated ninth element, and therefore at the base of the tenth element (figure 5, B). The input noise was sufficient to cause the tenth and eleventh element to switch. The pulse appearing at the collector of the eleventh element was negative-going from a +3.0VDC level to a +1.15VDC level (figure 5, C). Figure 5, D shows the pulse appearing at point D.

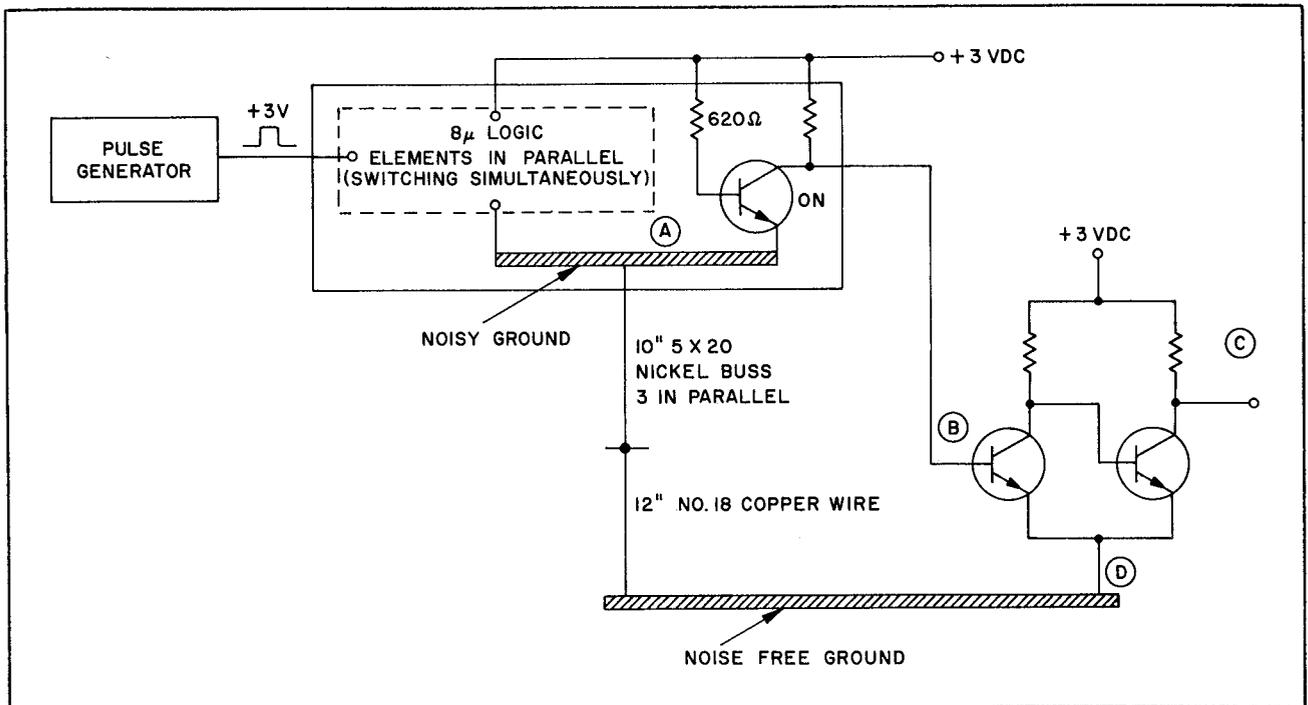
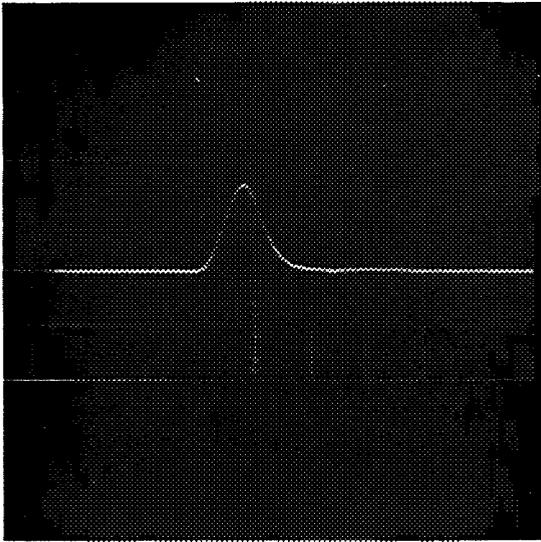
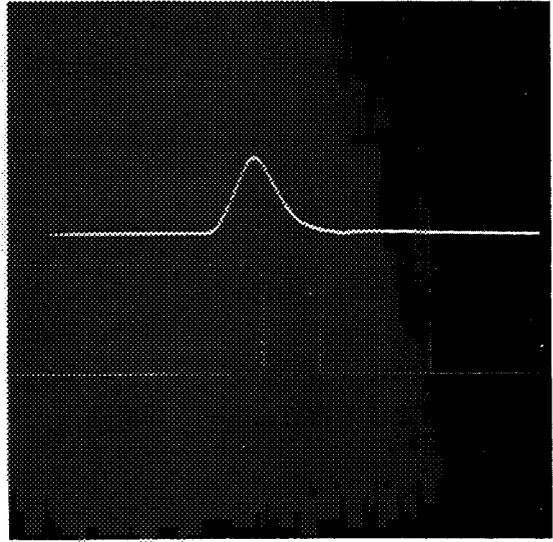


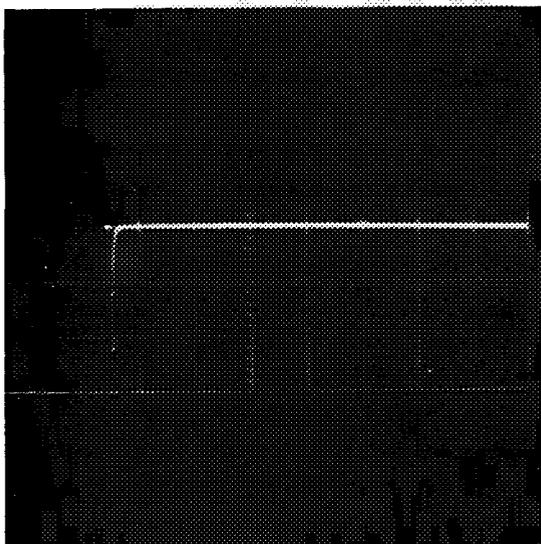
Figure 4. Micrologic Noise Test Circuit



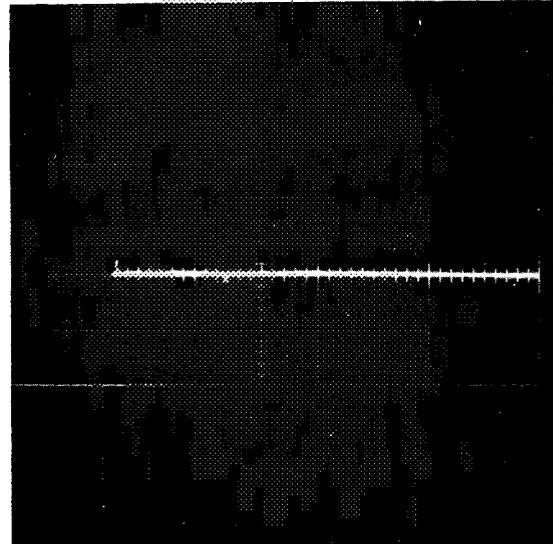
(A) 0.5V/CM, 50 NANoseconds/CM



(B) 0.5V/CM, 50 NANoseconds/CM



(C) 1.0V/CM, 2 MICROSECONDS/CM



(D) 0.05V/CM, 2 MICROSECONDS/CM

Figure 5. Micrologic Noise Test Circuit Waveforms

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These tests have substantiated earlier concern of ground noise problems. They have shown that an unusually severe condition exists. Results of these tests are particularly meaningful because micrologic circuits have been switched by noise which was generated solely by other micrologic elements. On the basis of these preliminary tests, the use of ground planes and a decoupling capacitor in each stick have been recommended for the AGC. Further tests are being performed to determine the effectiveness of these measures.

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4. GROUND SUPPORT EQUIPMENT

Investigations are continuing for a more weldable connector pin material. Gold plated steel pins were subjected to humidity tests and were found to rust. Samples of steel alloys are being subjected to the same tests.

Samples of keying inserts have been evaluated. The key tab on several units failed at the bend radius when subjected to moderate forces along the axis of the insert. Indications are that this situation can be corrected by bending the tab through a smaller angle.

The transformer driver and NOR modules have been reviewed by MIT/IL and released. The diode and resistor modules are expected to be reviewed during the next reporting period.

An acceptable light indicator to be used in the Computer Test set is being investigated. Mechanical and electrical design for the AGC Calibration Unit has been completed and submitted to MIT/IL for evaluation. Block diagrams for the Computer Test Set are being prepared.

Construction of the Computer Simulator breadboard is complete. Logical check-out is complete with the exception of the crystal oscillator being integrated into the simulator during testing. Fabrication of the mechanical mock-up of the Computer Simulator package led to a basic GSE packaging concept - the "logic drawer". The mechanical mock-up is complete. Certain design improvements evident during fabrication are being incorporated into the mechanical layout.

#### 4.1 LOGIC DRAWER

The Logic Drawer was designed to package logic circuit modules of the AGC Ground Support Equipment. Because many computer elements are available as commercial items and are most commonly sized to fit 19 inch panel width enclosures, it seemed logical at the outset to design a package that would be compatible with such standard enclosures and equipment as well as satisfy this particular GSE application.

##### 4.1.1 Logic Drawer Package

The Logic Drawer package (figure 6) is designed to be slide-mounted in cabinets with 28 inches depth, 19 inches panel width, and a minimum height of 8-3/4 inches. The packaging capacity of the drawer is divided into smaller subassemblies consistent with handling requirements and contributing a flexibility factor. Cabinet adaptability from the point of view of display is versatile. Front panels can vary in height to accommodate situations where display area requirements exceed the packaged logic area. Components within the drawer are cooled by the natural vertical air flow within a given cabinet. Cut-outs at the bottom of the drawer allow cooling air to pass over the encapsulated module shells.

Two rows of 32 circuit modules and one 60 pin connector per row make up one logic plate subassembly. Interconnections on the plate are wire-wrapped. The wire-wrapped plate is mounted in a slide-out frame that has a protective cover for the wire-wrapped terminals. The cover includes test point receptacles, spaced 0.20 inch apart on X and Y coordinates, that align with the pins of the wire-wrapped plate. Five of these slide-out logic plate subassemblies are packaged in one Logic Drawer providing for a maximum packaging capacity of 320 modules per drawer. Each logic plate subassembly weighs approximately 30 pounds fully loaded, in compliance with practical

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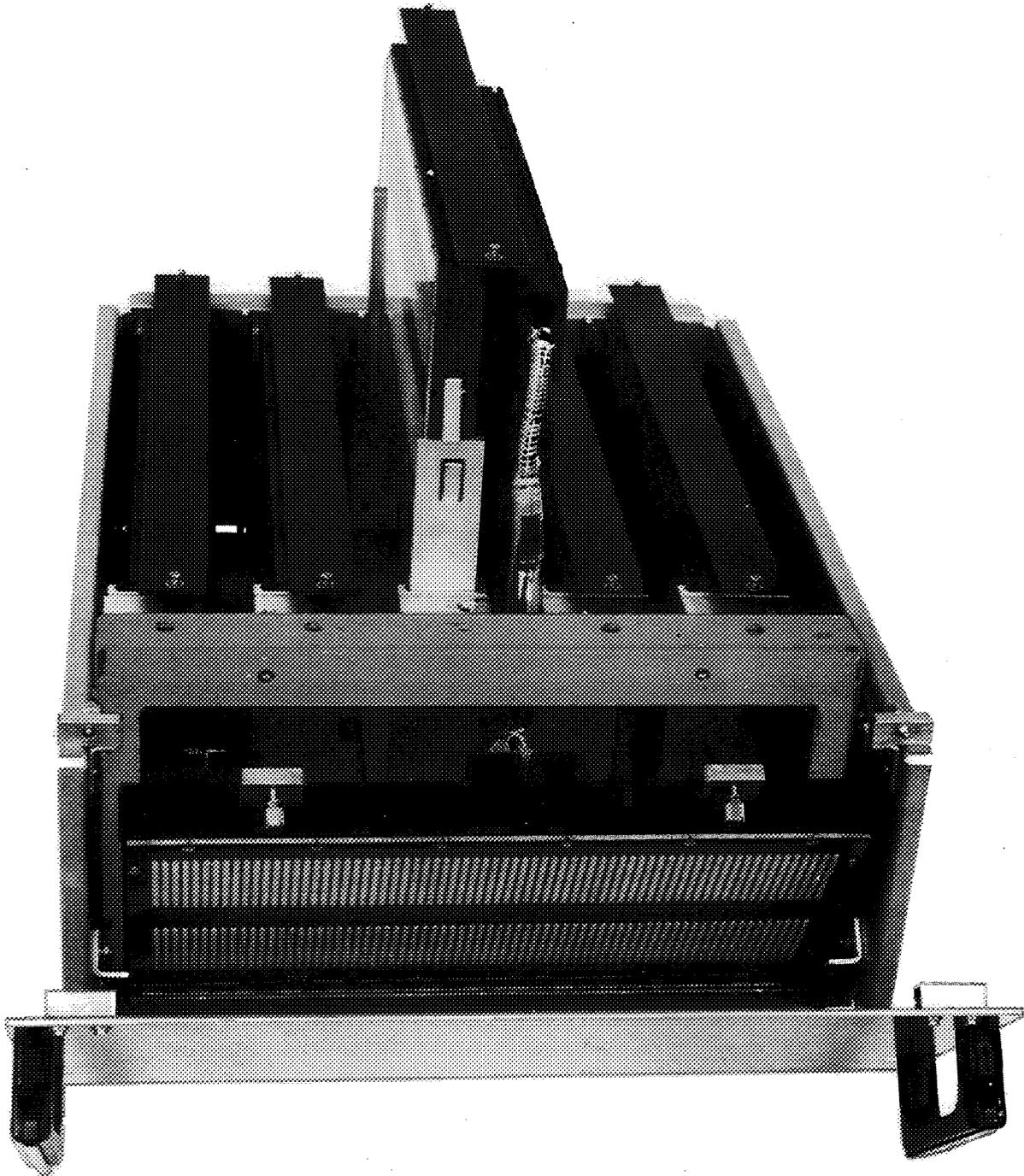


Figure 6. Logic Drawer

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handling requirements for one man. The five logic plate subassemblies are interconnected by a sixth wire-wrapped plate mounted across the front of the drawer. This plate, hinged at the bottom, becomes a structural part of the overall package with the capacity for as many terminals as required, and has the same test point cover as the logic plate subassemblies. The interconnections plate is hinged for access to cables that attach to each of the five logic plates. The cables are designed so the logic plates slide up and down and the hinged interconnection panel moves freely without undue kinking of or pressure on the cable harnesses.

#### 4.1.2 Logic Modules

Logic circuits are packaged in modules compatible with the logic plate subassembly. All of the circuits are internally interconnected by resistance spot welding. Approximately 80 percent of the modules contain micrologic and all are encapsulated in their final form. The module structure consists of three parts:

- a. a connector, molded of Diallyl Phthalate and containing 20 feed-through pins that rise the height of the module on the circuit side of the connector: this feature reduces the number of welds in a circuit and contributes to the structural integrity of the circuit matrix prior to encapsulation
- b. indexing receptacles that integrate module keying and a means of fasten the module structure together
- c. an extruded module frame incorporating a receptacle for an extraction tool, a protective wrap-around for logic circuits, a module frame that can be used as a

heat sink when necessary, and an extrusion that has a flexible third dimension.

If the need for logic modules should require less than five logic plate subassemblies, the remaining drawer space is suitable for special packaging considerations.

#### 4.2 CALIBRATION EQUIPMENT

Utilization of VLF rather than VHF techniques is rapidly becoming the accepted method of establishing the error in frequency standards, because the propagation of VLF is such that phase shifts, except during diurnal periods, are negligible (diurnal phase shift occurs during night transmission due to a change in the ionosphere). Thus the received signal may be used as a frequency reference and is as accurate as the transmitted signal (on the order of one part in  $10^{10}$ ). On the other hand, phase shifts associated with VHF propagation may be quite large and it is usually not possible to make frequency determinations to an accuracy better than one part in  $10^6$ . Therefore, the NBA standard (18KC) has been selected for calibrating frequency standards in preference to others because it usually carries no traffic and is the only one radiating enough power to be easily received in the United States. The Apollo oscillator frequency and aging characteristics will be measured by counter techniques utilizing the calibrated frequency standard as the counter time base.

##### 4.2.1 Calibration Theory

An 18KC signal received from NBA is transmitted through a receiver (figure 7). This signal is multiplied and divided in a frequency synthesizer unit to produce a 100KC signal that is fed to a phase comparator.

The frequency standard (1-MC) is divided down to 100KC, fed through a

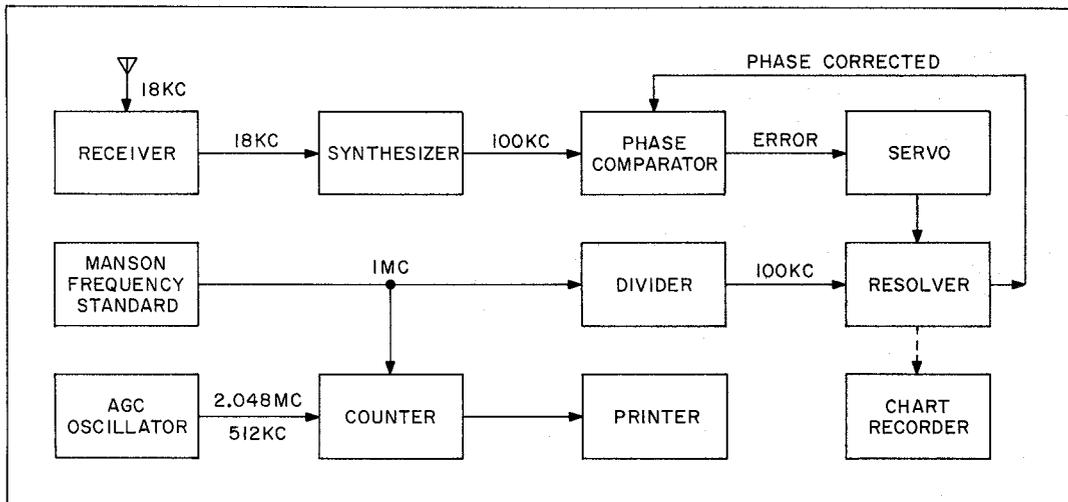


Figure 7. Technique Used to Measure AGC Oscillator Characteristics

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resolver and then to the phase comparator. The signals from NBA and the frequency standard are compared for phase relationship. If there is a phase error, a signal is produced that activates a servomotor to drive the resolver. This resolver drives a chart recorder that indicates how much error there is in the phase of the standard. If an error exists, it must be corrected by manipulating a manual control located on the frequency standard. Thus, a permanent record of the frequency characteristics of the standard is provided. It is assumed that the incoming signal from NBA is much more accurate than the signal from the frequency standard. Therefore, any error signal produced is due to the standard unit changing frequency.

The 1-MC output of the calibrated standard is used as the time base of an eight stage counter. The AGC oscillator output (2.048 MC) is fed into this counter. The output of the counter is fed through a printer that records the frequency of the oscillator. Thus, by calibrating the frequency standard with the NBA standard, the frequency and aging characteristics of the AGC oscillator can be determined.

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