(NASA-CR-173008) SPACECRAFT IF SWITCH MATRIX FOR WIDEBAND SERVICE APPLICATIONS IN 30/20 GHz COMMUNICATION SATELLITE SYSTEMS (Ford Aerospace and Communications Corp.) 170 p

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SPACECRAFT IF SWITCH MATRIX FOR WIDEBAND SERVICE APPLICATIONS IN 30/20 GHz COMMUNICATION SATELLITE SYSTEMS

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MAJOR REVIEW #1

CONTRACT NO. NAS3-22501

PRESENT TO: NASA/LEWIS RESEARCH CENTER
CLEVELAND, OHIO

February, 1981

Western Development
Laboratories Division
3939 Fabian Way
Palo Alto, California 94303

Ford Aerospace &
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SPACECRAFT IF SWITCH MATRIX FOR WIDEBAND SERVICE APPLICATIONS IN 30/20 GHz COMMUNICATION SATELLITE SYSTEMS

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PRESENTATION OUTLINE

Executive Summary

Introduction

Task I

IF Switch Matrix Design Using 1982 Technology

- Technology Assessment
- IF Switch Matrix Design

Task II

Alternate Switch Matrix Design Study Using 1987 Technology

- Large IF Switch Matrix Design Concept
- Large Baseband Analog Switch Matrix Design Concept

Task III

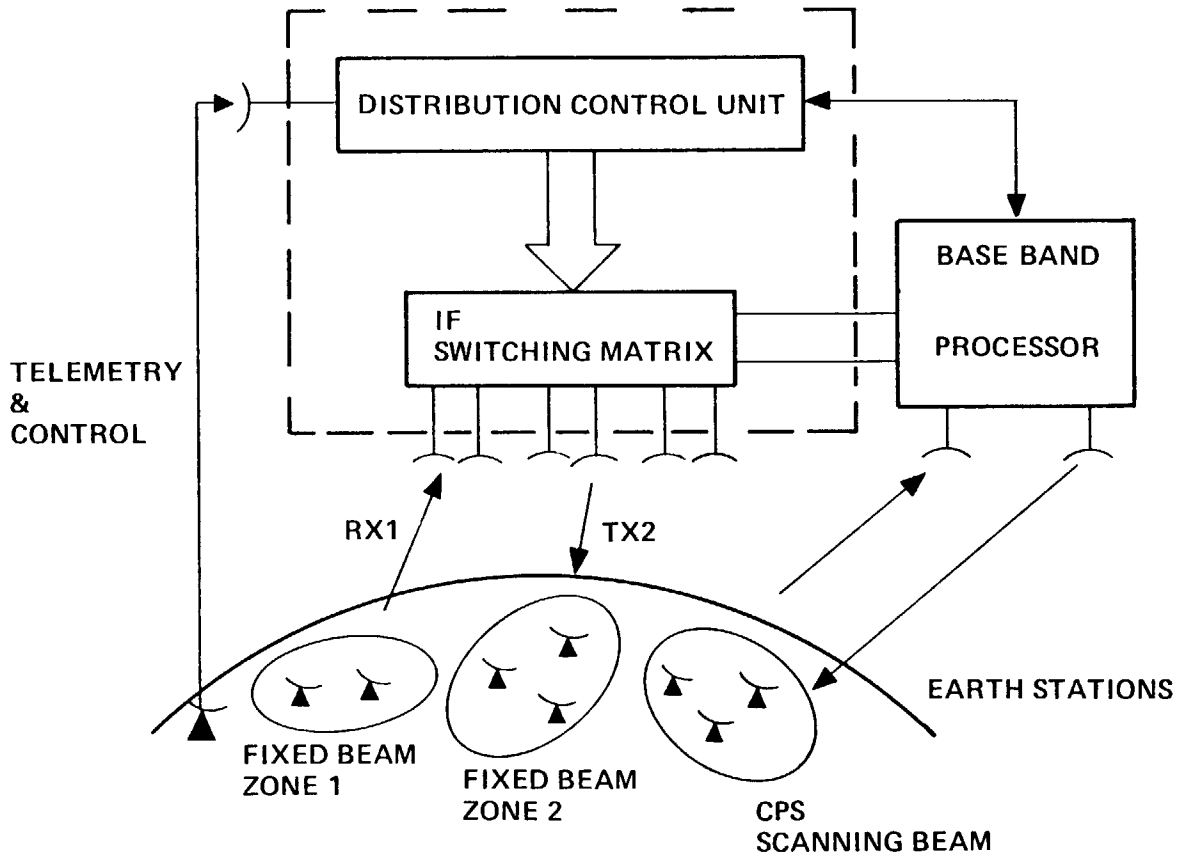
Breadboard Development of Critical Switch Technology

- Coupler Development
- Switch Amplifier Development
- Switch Driver Development
- Distribution Control Unit Development
- Mechanical Packaging Concept

OBJECTIVE

Develop an IF switch matrix to demonstrate the feasibility of providing high capacity channel interconnectivity on board a 30/20 GHz multiple beam communication satellite.

IF SWITCH MATRIX ON BOARD
A 30/20 GHz COMMUNICATION SATELLITE



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CRITICAL DESIGN PARAMETERS:

- Connectivity:
  - Communication mode
  - Broadcast mode
- Random switching
- Switching speed
- D.C. power consumption
- Mechanical structure
- Manufacturability
- Reliability
- Size, weight

EXPECTED PERFORMANCE OF THE POC MODEL IF SWITCH MATRIX

PARAMETERS	REQUIREMENTS	EXPECTED PERFORMANCE
MATRIX SIZE	20 x 20	20 x 20
RECONFIGURATION RATE	2 μ SEC (MAX)	2 μ SEC
SWITCHING TIME	10 N SEC (MAX)	10 N SEC
IF FREQUENCY	3 TO 8 GHZ	5 GHz
BAND WIDTH	1000 MHZ (MIN)	2500 MHZ
GAIN RIPPLE	1 DB/1000 MHZ	1 DB/1000 MHZ
PHASE LINEARITY VARIATION	$\pm$ 5 DEGREES (MAX)	$\pm$ 5 DEGREES
INSERTION LOSS	15 DB (MAX)	12.83 DB
ISOLATION	40 DB (MIN)	45.78 DB
INPUT/OUTPUT VSWR	1.2 (MAX)	1.25:1
INPUT SIGNAL LEVEL	-30 DBM TO 10 DBM	-30 DBM TO 10 DBM
DC INPUT POWER		30.0 WATTS
RELIABILITY		0.9630 FOR 10 YEARS
DIMENSION		10.9" x 18.85" x 1.56"
WEIGHT		14.0 LBS

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TASK 1. IF SWITCH MATRIX DESIGN USING 1982 TECHNOLOGY

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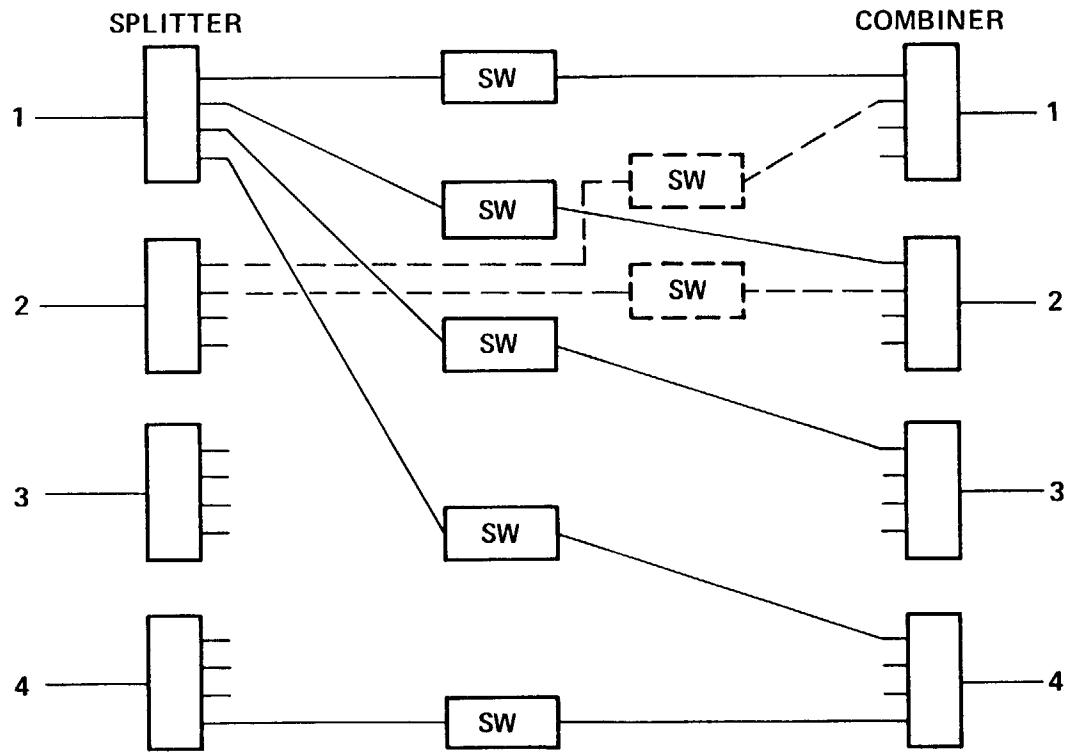
FAN-OUT/FAN-IN MATRIX



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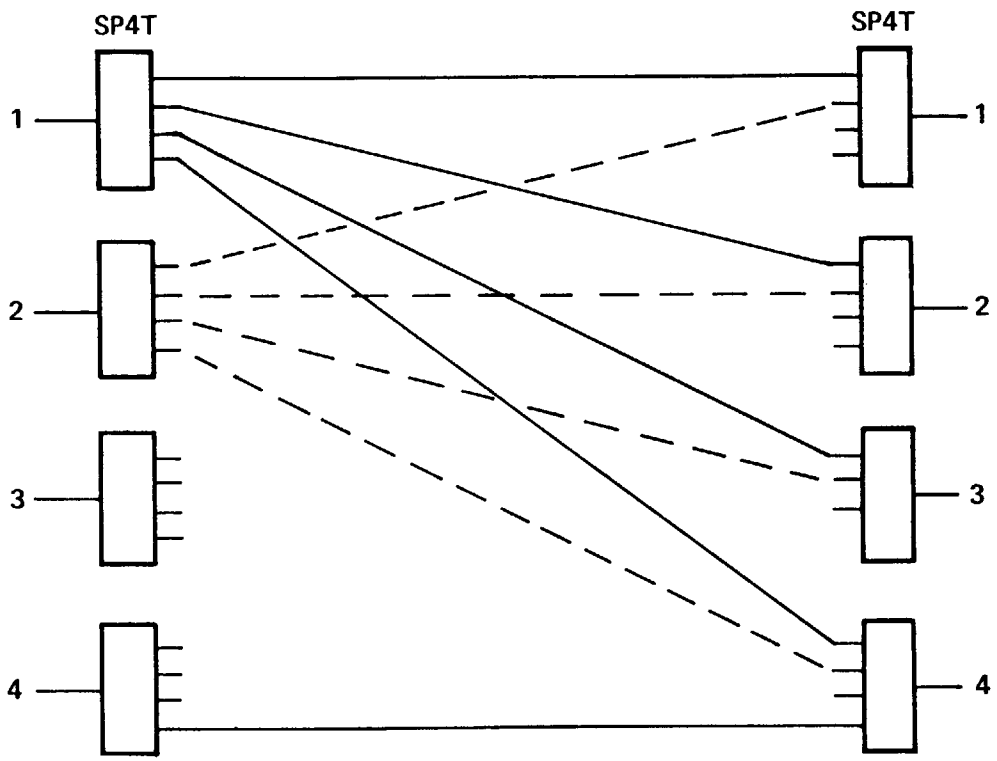
SPMT MATRIX



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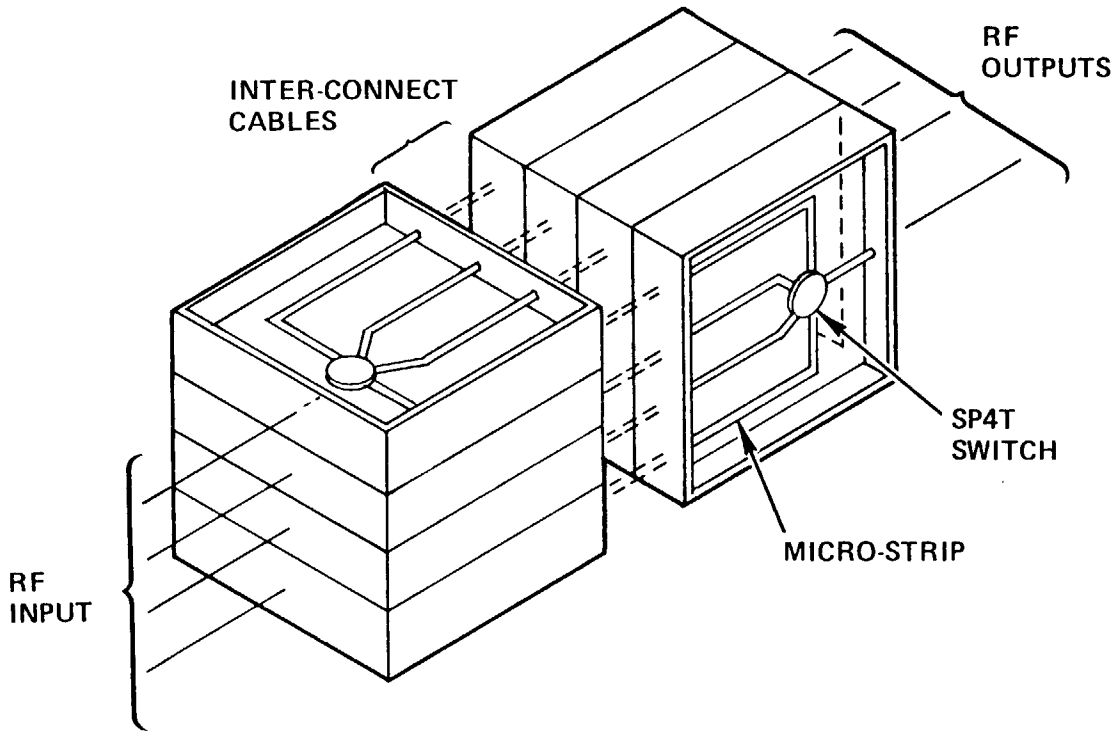
MECHANICAL CONSTRUCTION OF THE SPMT MATRIX



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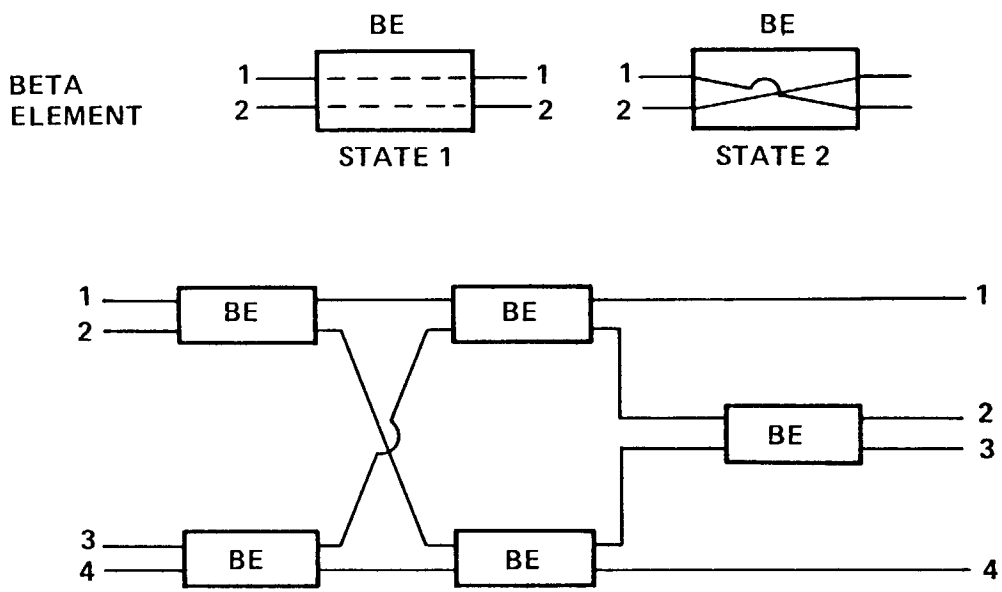
REARRANGEABLE SWITCH MATRIX



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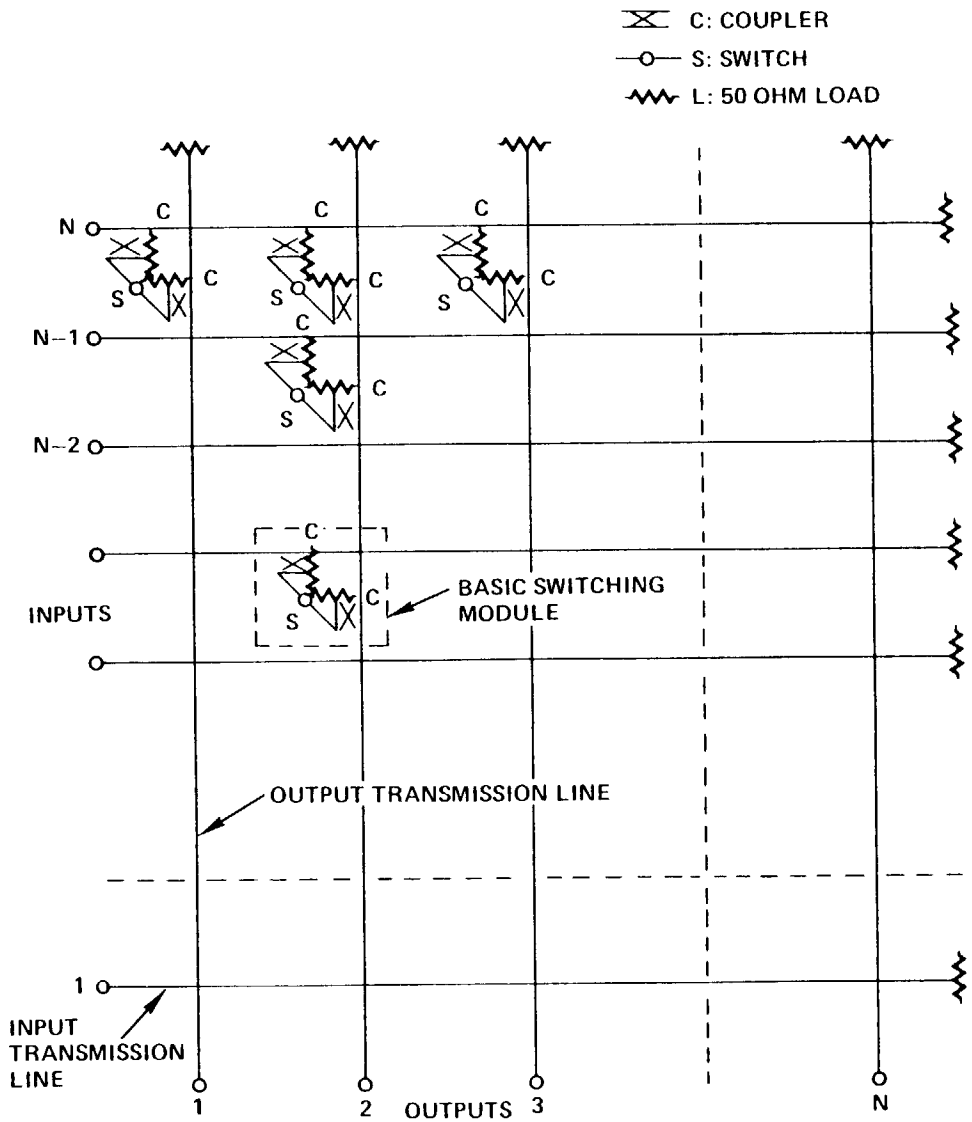
COMPARISON OF EXISTING SWITCH MATRIX

DESCRIPTION	ADVANTAGES	DISADVANTAGES
FAN-OUT/ FAN-IN	BROADCAST MODE CAPABILITY	HIGH INPUT VSWR HIGH INSERTION LOSS. REDUNDANCY DIFFI-CULT TO IMPLEMENT
SINGLE POLE MULTIPLE THROW	LOW INSERTION LOSS	POOR RELIABILITY
REARRANGEABLE SWITCH	LOW INSERTION LOSS	POOR RELIABILITY RANDOM INTERRUPTIONS CONTROL ALGORITHM TOO COMPLICATED

MICROWAVE SWITCH MATRIX USING COUPLER CROSS BAR CONFIGURATION



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ADVANTAGE OF COUPLER CROSSBAR SWITCH MATRIX ARCHITECTURE

- Planar structure. Monolithic MIC possible in the future.
- Modular approach. Simple manufacturing
- Enhanced reliability
  - Minimum switching devices per cross point are used
  - Failure of a device means at the most the loss of one cross point
  - Redundancy is simpler to implement
- Easier to match than other approaches
- Input and output signal levels are independent of the switching path
- Broadcast mode of operation with no input matching problems

FUNCTIONAL CAPABILITIES OF IF SWITCH MATRIX ARCHITECTURES

ARCHITECTURE / FUNCTIONAL REQUIREMENT	FAN-OUT/ FAN-IN	SINGLE-POLE-MULTIPLE-THROW	REARRANGEABLE SWITCH	COUPLER CROSSBAR
BROADCAST MODE	YES	NO	NO	YES
VARIABLE TIME ASSIGNMENT	YES	YES	NO	YES
MECHANICAL CONSTRUCTION	CUBIC	CUBIC	PLANAR	PLANAR

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SWITCHING DEVICES CHARACTERISTICS

TYPE OF DEVICE	DISADVANTAGES	ADVANTAGES
PIN DIODE (SERIES, SHUNT, SERIES-SHUNT)	NOT TOO FAST. LOW ISOLATION. HIGH CONTROL CURRENT/ POWER. NOT EFFICIENT FOR A LARGE SWITCH.	ESTABLISHED RELIABILITY HISTORY
FERRITE SWITCH	SLOW, HEAVY	HIGH POWER HANDLING CAPABILITY LOW INSERTION LOSS
DUAL-GATE GAAS FET	DEVICE RELIABILITY NEED TO BE ESTABLISHED	INSERTION GAIN. HIGH ISOLATION. LOW DRIVING POWER. HIGH SWITCHING SPEED. SUITABILITY FOR MONOLITHIC I.C.

MICROWAVE SWITCHING DEVICES: COMPARATIVE PERFORMANCES

DEVICE	SPEED (NS)	HOLDING "ON" POWER (MW)	LOSS/GAIN (DB)	ISOLATION (DB)
PIN DIODE	1	300	−1.5	30
	50	20	−1.5	30
FET	0.05	100	−3.0	20
	10	0.01	−3.0	20
FERRITE	100	0	−0.5	20
MECHANICAL	100,000	0	−0.25	60
DUAL-GATE FET	0.05	0.001	+15	30

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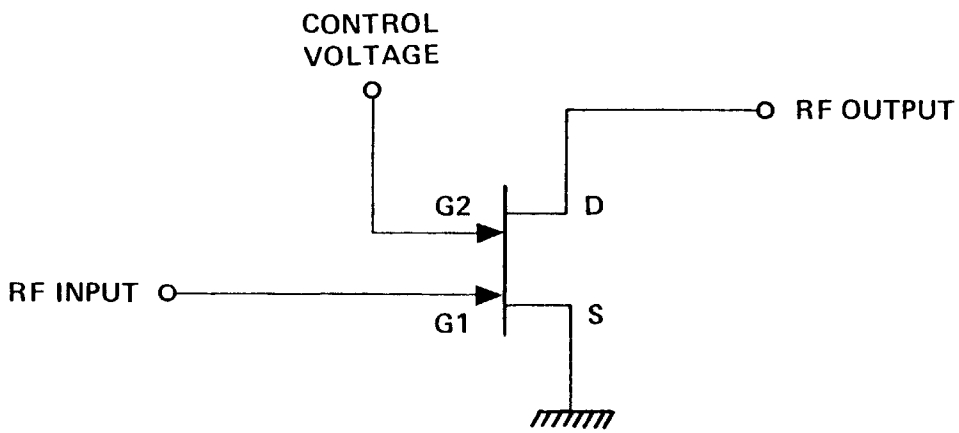
SCHEMATIC OF DUAL GATE FET



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DUAL-GATE MICROWAVE GaAs FET TRANSISTOR SPECIFICATIONS

PERFORMANCE \ PART NUMBER (SUPPLIER)	LND 832 (RAYTHEON)	NE 46300 (NEC)	DUGAT 10/100 (PLESSEY)	DXL-2703A (DEXCEL)
MAXIMUM AVAILABLE GAIN	12 DB @ 10 GHZ	20 DB @ 4 GHZ 15 DB @ 8 GHZ	22 DB @ 4 GHZ 17 DB @ 8 GHZ	18 DB @ 4 GHZ 13 DB @ 8 GHZ
POWER OUTPUT	+10 DBM	———	+10 DBM	+10 DBM
NOISE FIGURE	4 DB @ 10 GHZ	1.5 DB @ 4 GHZ 2.7 DB @ 8 GHZ	1.5 DB @ 4 GHZ 2.8 DB @ 8 GHZ	2.5 DB @ 4 GHZ
AVAILABLE GAIN CONTROL	30 DB TYP V_{G2S} =0 V TO −2.5V	20 DB @ 4 GHZ V_{G2S} = 0 V TO −2 V	30 DB @ 10 GHZ (V_{G2S} = 0 TO −4 V	30 DB @ 4 GHZ V_{G2S} = 0 TO −4V

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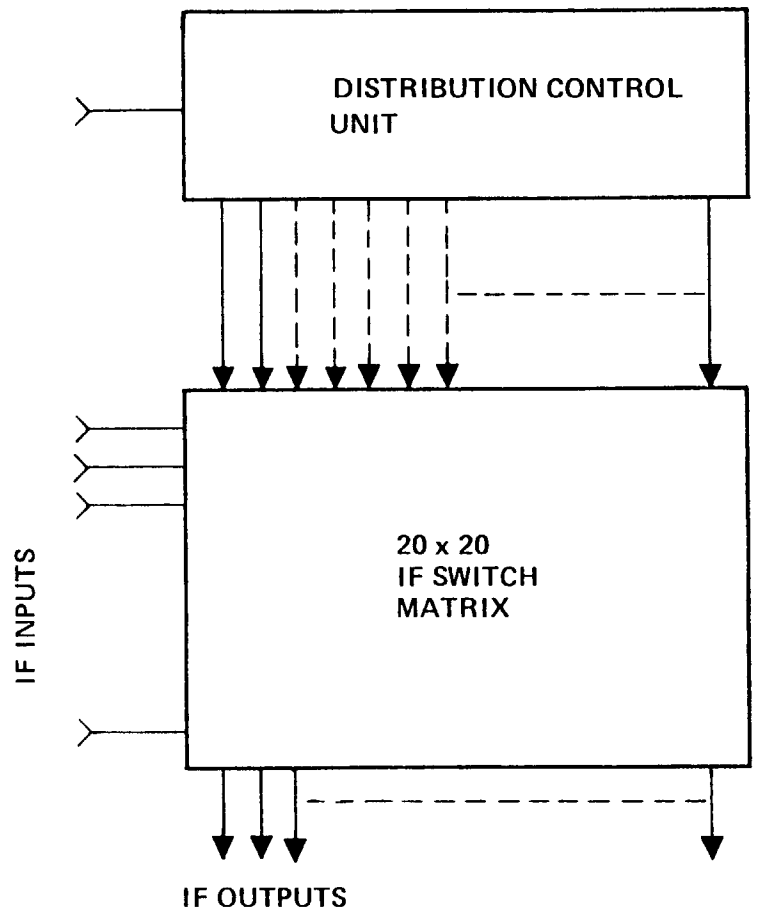
IF SWITCH MATRIX SYSTEM



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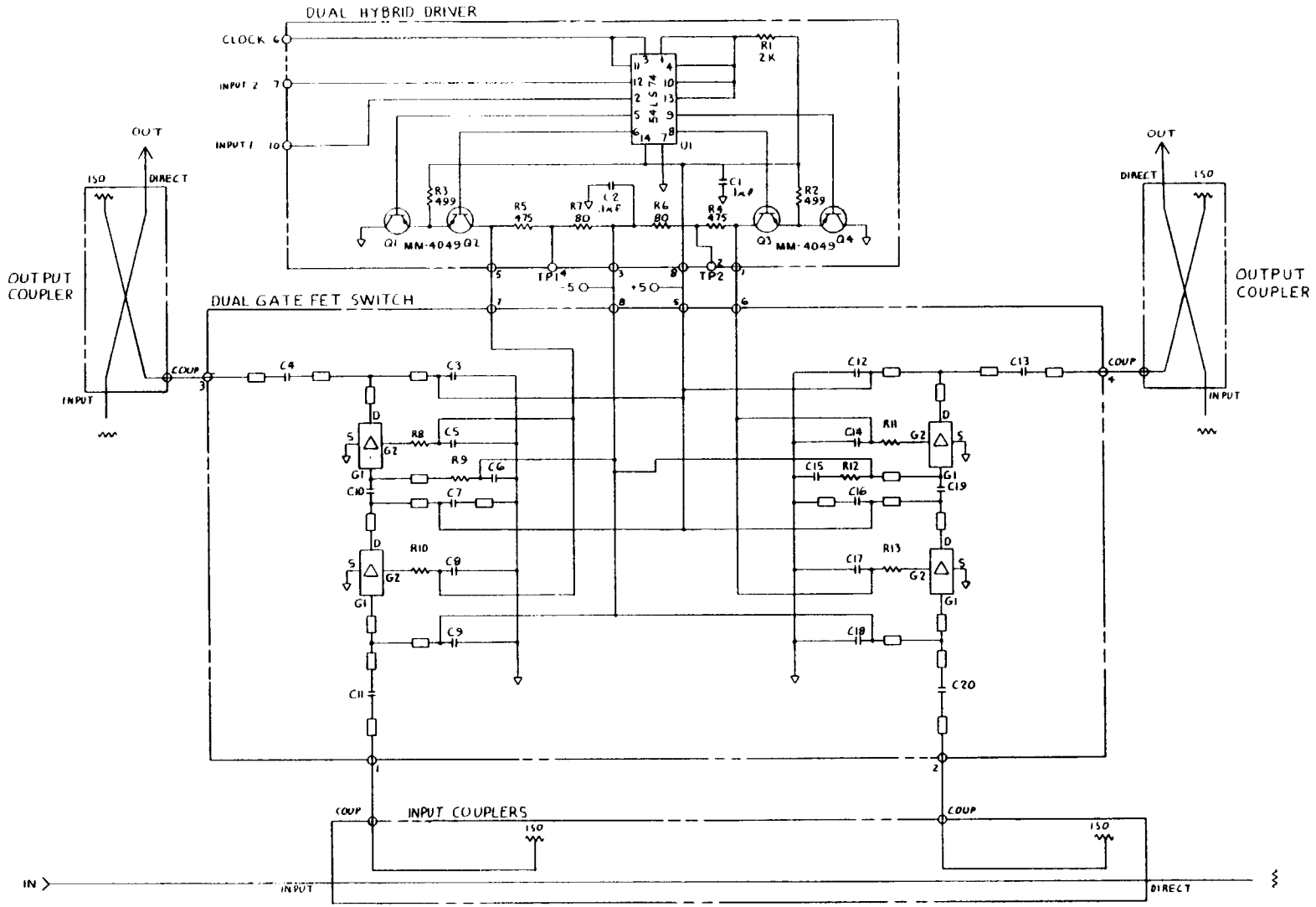
SCHEMATIC NASA SWITCH MATRIX



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IF FREQUENCY SELECTION

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SPURIOUS VS IF FREQUENCY
(FOR 2.5 GHz BANDWIDTH)

IF CENTER FREQUENCY MHz	IF RANGE		RECEIVE		TRANSMIT		COMMENT
	FROM	TO	WORST SPURIOUS	CODE*	WORST SPURIOUS	CODE*	
3250	2000	4500	DOUBLE 2,2	1 1-1/2	2,1	2	NOT GOOD
3750	2500	5000	DOUBLE 2,2	1-1/2 1-1/2	2,1	2	NOT GOOD
4250	3000	5000	4,5	3	2,2	2	
4500	3250	5750	4,5	3	2,2	2	
4750	3500	6000	3,4	3	2,2	2	
5000	3750	6250	3,4 4,5	3 3	2,2 3,0	2 2-1/2	
5250	4000	6500	3,4 4,5	3	2,2 3,0	2 2-1/2	
5500	4250	6750	3,4 4,5	3	1,2 2,2 3,0	1 2 2-1/2	NOT GOOD
6000	4750	7250	3,4 4,5	3	1,2 3,0	1 2-1/2	NOT GOOD

* CODE 1 = NOT GOOD. CODE 2 = POTENTIAL PROBLEM. CODE 3 = PROBABLY NOT A PROBLEM.

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SPURIOUS VS IF FREQUENCY
(FOR 2.5 GHz BANDWIDTH)

IF CENTER FREQUENCY MHz	IF RANGE		RECEIVE		TRANSMIT		COMMENT
	FROM	TO	WORST SPURIOUS	CODE*	WORST SPURIOUS	CODE*	
6500	5250	7750	2,3 3,4 4,5	2 3 3	1,2 3,0	1 2-1/2	NOT GOOD
6750	5500	8000	2,3 3,4 4,5	2 3 3	1,2 3,0	1 2-1/2	NOT GOOD
7750	6500	9000	2,3 3,4 4,5	2 3 3	2,0 2,3	1-1/2 2-1/2	
8750	7500	10000	1,2 2,3 3,4 4,5	1 2 3 3	2,0	1-1/2	NOT GOOD
9750	8500	11000	1,2 3,4 4,5	1 3 3	0,2 1,3 2,0	1 1-1/2 1-1/2	NOT GOOD
10750	9500	12000	2,4	3	2,0	1-1/2	
11750	10500	13000	2,4	3	1,4 2,1	1-1/2	
12750	11500	14000	2,3	2	0,3	1	NOT GOOD

* CODE 1 = NOT GOOD. CODE 2 = POTENTIAL PROBLEM. CODE 3 = PROBABLY NOT A PROBLEM.

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SPURIOUS VS IF FREQUENCY
(FOR 1 GHz BANDWIDTH)

IF CENTER FREQUENCY MHz	RECEIVE WORST SPURIOUS	CODE*	TRANSMIT WORST SPURIOUS	CODE*	COMMENT
2500	NONE	–	5,2	3	ABOVE PAR
3000	NONE	–	4,2	3	ABOVE PAR
3500	NONE	–	4,2	3	ABOVE PAR
3950	5,6	3	3,2	3	ABOVE PAR
4000	5,6	3	3,2	3	ABOVE PAR
4500	4,5	3	4,0	3	ABOVE PAR
5000	4,5	3	2,2	2	BELOW PAR
5500	3,4	3	4,0	3	PAR
6000	3,4	3	3,0	2 1/2	PAR
6500	NONE		1,2	1	NOT GOOD
7000	2,3	2	3,0	2 1/2	BELOW PAR
7500	2,3	2	4,1	3	BELOW PAR
8000	4,6	3	2,3	2 1/2	PAR
19950	3,12	3	2,4	2	SINGLE TRANSLATION

*Code 1 = Not Good Code 2 = Potential Problem Code 3 = Probably Not a Problem

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RELIABILITY ANALYSIS

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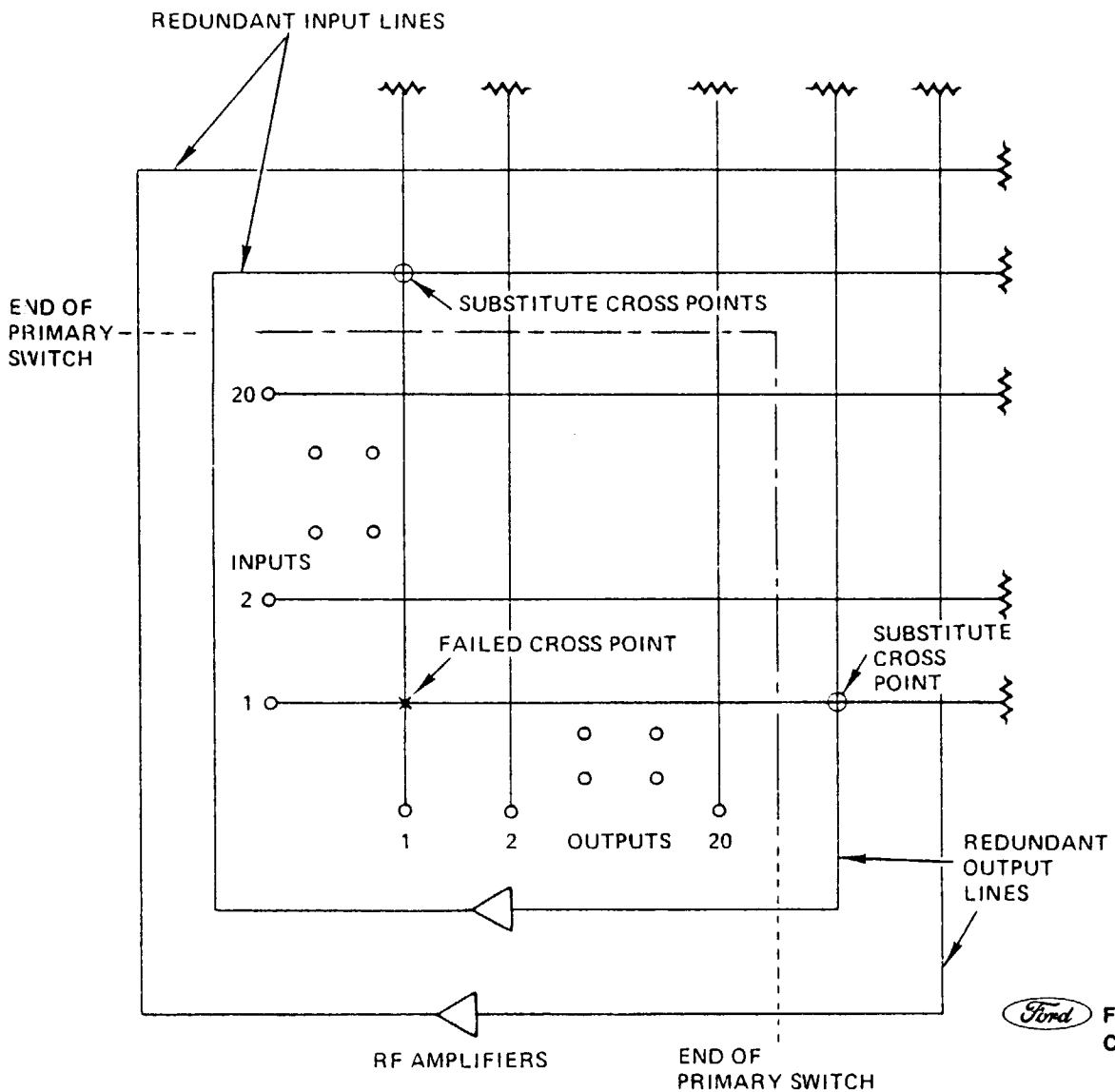
20 X 20 MICROWAVE SWITCHING MATRIX WITH 2 LEVEL OF REDUNDANCY



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RELIABILITY PROJECTION OF COUPLER CROSSBAR MICROWAVE SWITCH MATRIX (WITH 2 LEVEL OF REDUNDANCY)

	Failure Rate	Probability of Surviving for 10 Years
Dual gate FET	9.05×10^{-9}	
RF switch	33.6×10^{-9}	
Driver circuit	36.4×10^{-9}	0.997735
Cross-point	70×10^{-9}	
Probability of no open switch		0.991792
Probability of no closed switch		0.998936
RF matrix reliability		0.9907

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RELIABILITY PROJECTION OF IF SWITCH MATRIX SYSTEM

		Probability of Surviving for 10 Years
• IF switch matrix (with driver)	2 level redundancy	0.9907
• Distribution control unit (with decoder)	2 for 1 redundancy	0.9721
• IF switch matrix system		0.9630

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CRITICAL HARDWARES TO BE DEVELOPED

- Dual-Gate FET Switch-Amplifier
- Broadband Directional Couplers
- High Speed Switch Driver Circuit
- Distribution Control Circuit
- Integrated Packaging Technique

TASK II. ALTERNATE SWITCH MATRIX DESIGN STUDY USING 1987 TECHNOLOGY

CANDIDATE MATRIX SWITCH OBJECTIVES USING 1987 TECHNOLOGY

- Monolithic gallium arsenide technology
- High density
- 100 x 100 port switch using 10 x 10 port blocks
- Low voltage
- Low power consumption
- High microwave isolation
- Wide IF passband
- High reliability
- Capability of mass production at low price

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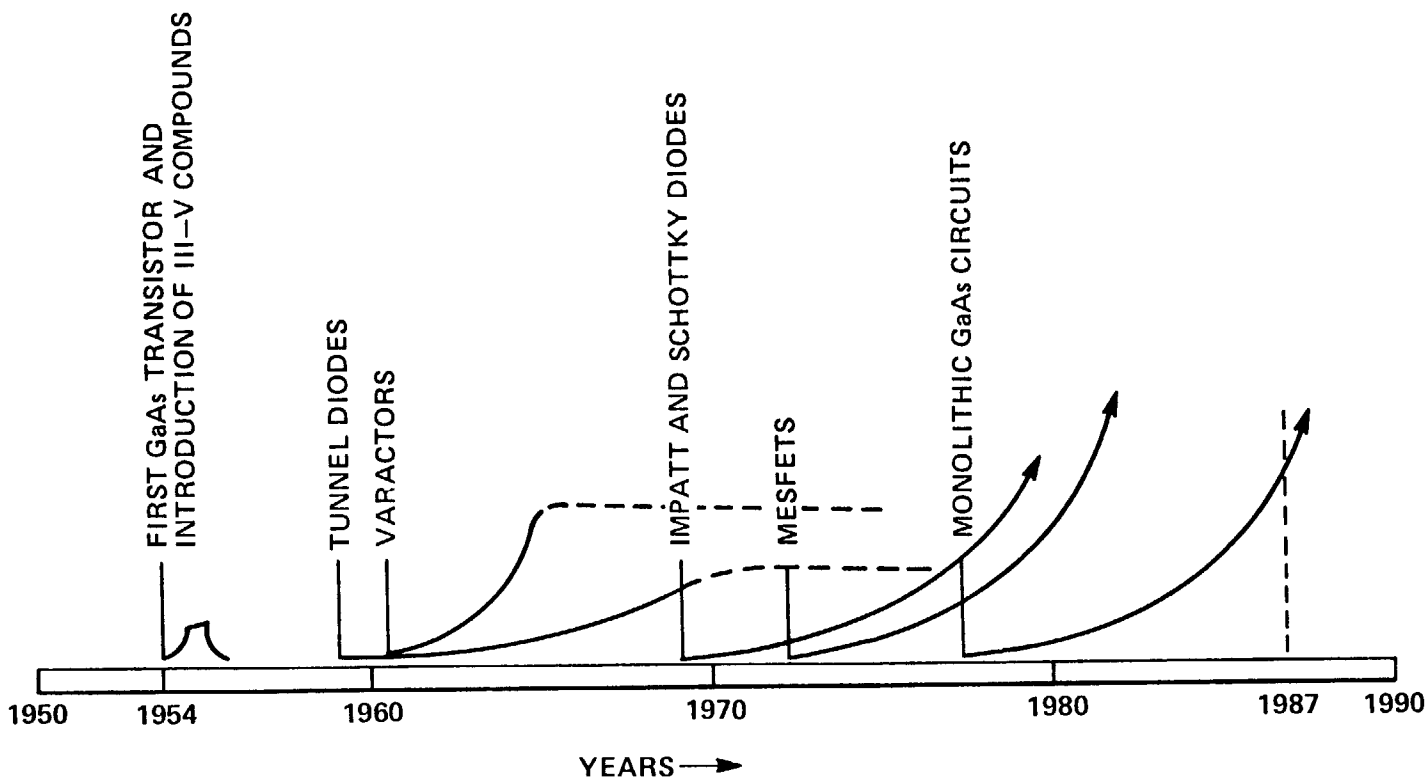
DEVELOPMENT AN UTILIZATION OF GALLIUM ARSENIDE



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THE GALLIUM ARSENIDE INTEGRATED CIRCUIT COMPETITION

Advantages

- Higher frequency than Si
- Faster computation than Si
- More functions at microwave frequency
- Lower power

Japanese Effort

- Very intensive - more than U.S.
- Fujitsu developing GaAs computer chips to compete against IBM
- Major Japanese TV-manufacturers to use GaAs tuner ICs
- Major Japanese researching GaAs circuits - Hitachi, Matsushita, Mitsubishi, Oki, NEC, Sony, NTT, Fujitsu, etc.

MESFET TECHNOLOGY

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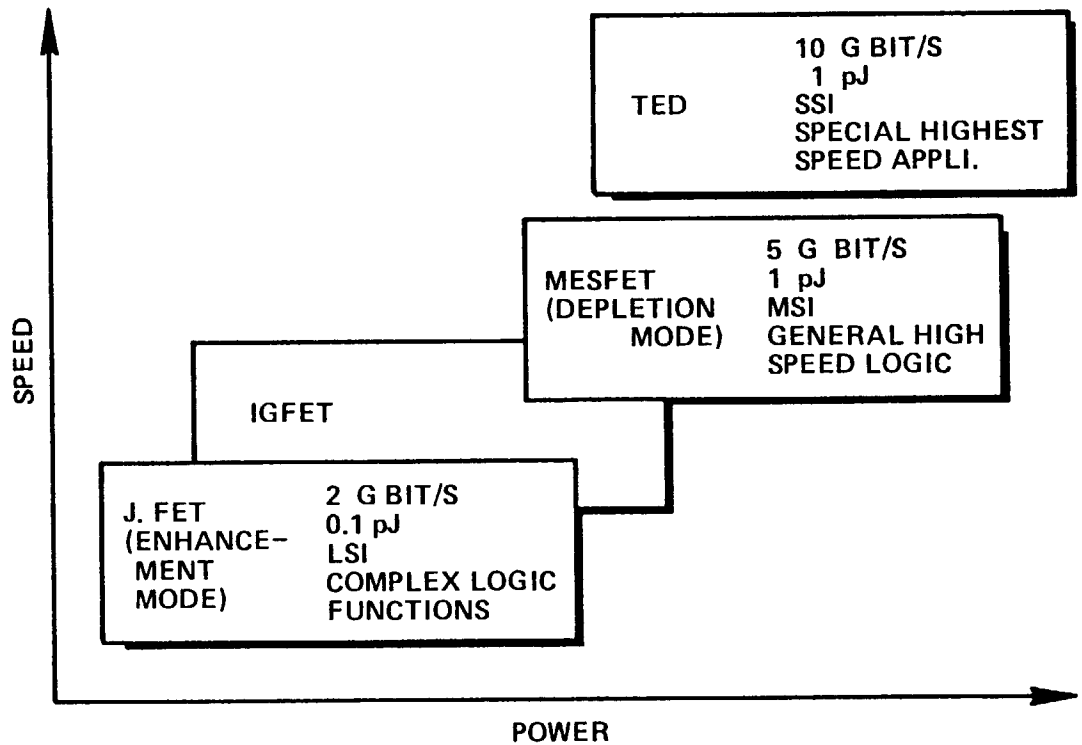
ESTIMATED FUTURE PERFORMANCE, LEVEL OF INTEGRATION AND APPLICATION AREAS FOR THE GaAs LOGIC FAMILIES



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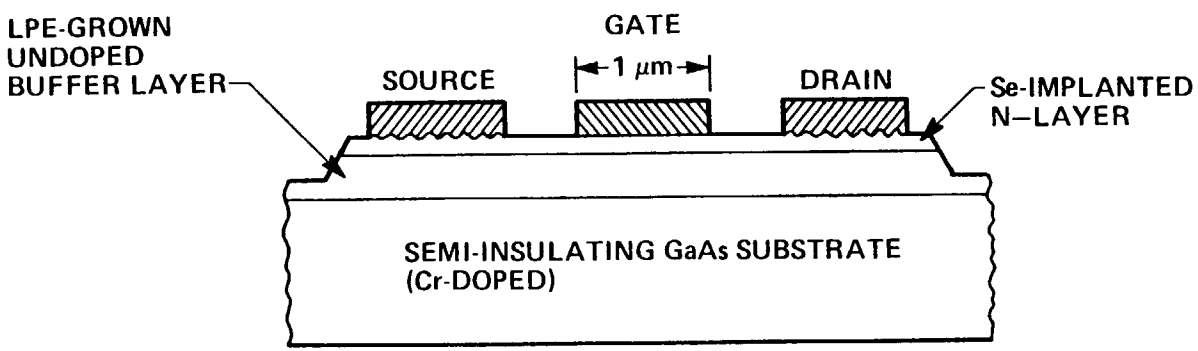
a.



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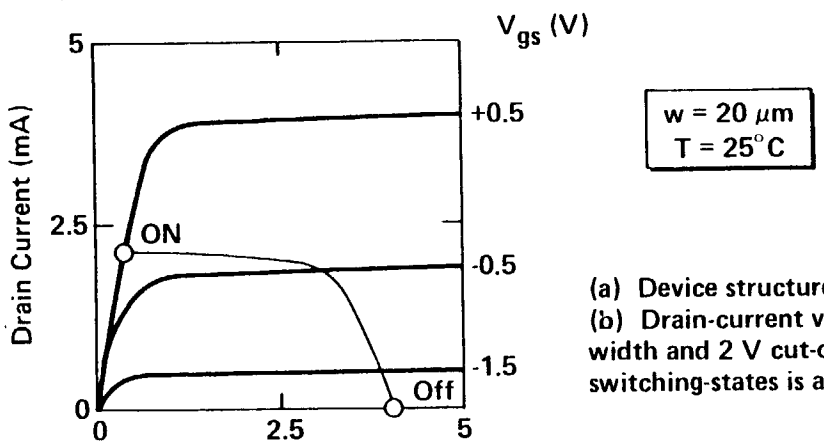

(a) Device structure of depletion-mode GaAs MESFET with implanted channel.
(b) Drain-current versus drain-voltage of a MESFET with 1 μm gate length, 20 μm width and 2 V cut-off gate voltage. A typical active load line with on- and off-switching-states is also plotted.

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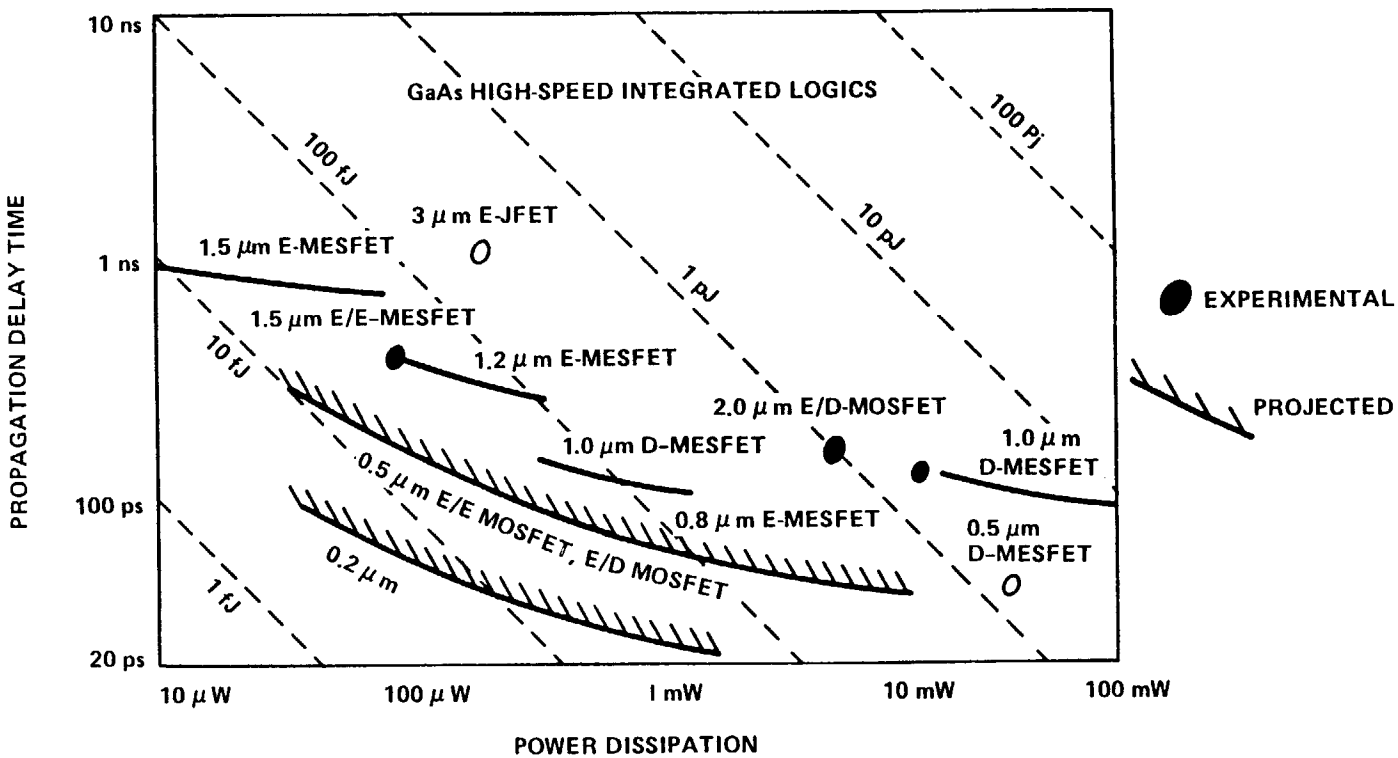
SPEED POWER PERFORMANCE OF GaAs ICS



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GaAs ICs, LSI, VLSI

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RECENT ACTIVITY IN MONOLITHIC GaAs CIRCUITS

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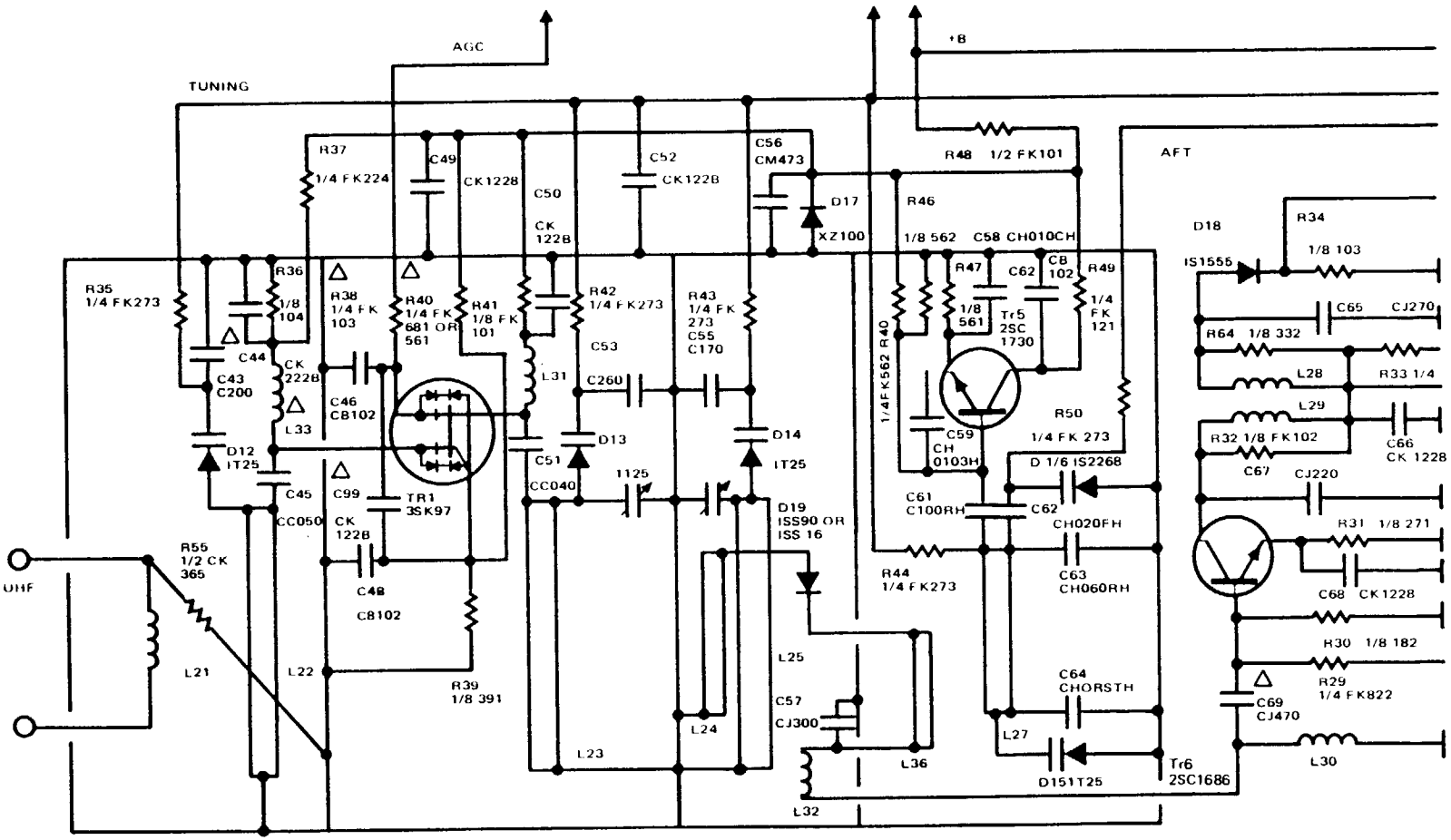
COMMERCIAL TV'S TUNER USES
GaAs MESFET



- IMPROVED NOISE FIGURE WILL DRIVE USE OF MILLIONS OF CHEAP FETs.
- USED BY SANYO ELECTRIC CO. LTD. IN JAPAN USING MATSUSHITA 3SK97 WITH 1.3 db NF. EXPECTED PRODUCTION 50000 TUNERS/MONTH.

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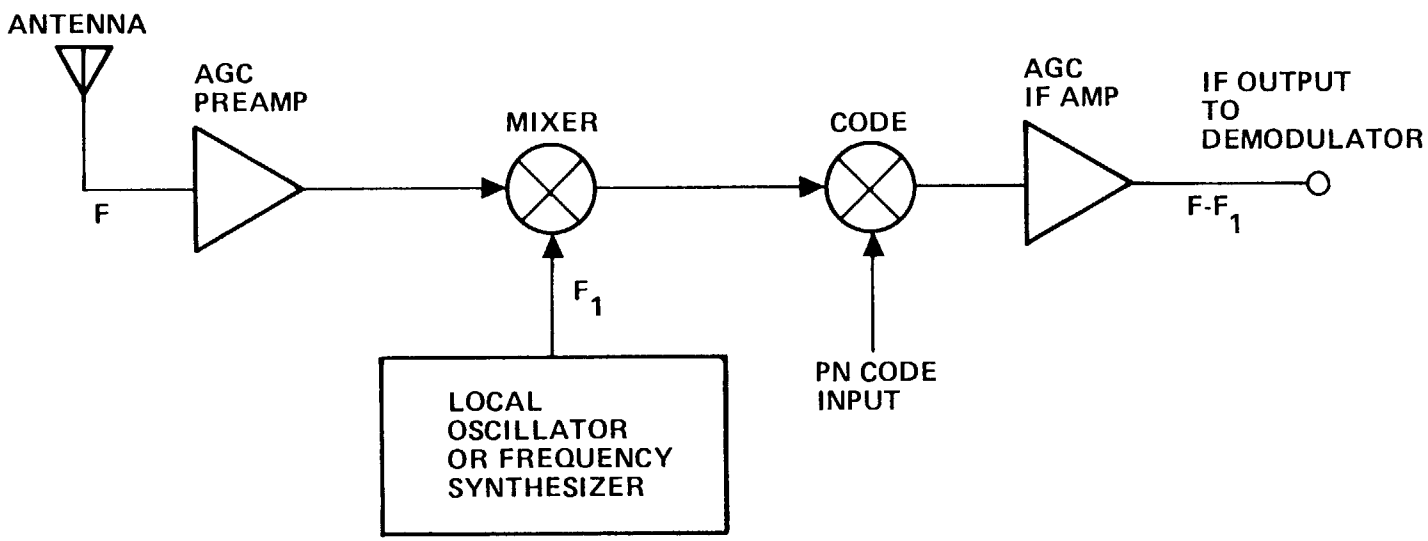
TYPICAL ACTIVITY IN MONOLITHIC GaAs CIRCUITS IN 1980

Objectives: Multiple functions on a single chip

- Plessey: Single chip receiver front-end to work over 2.7-3.4 GHz band and chips up to 36 GHz
- H.P.: RF signal generation amplifier, and instrumentation chips under development
- Westinghouse: Two stage microstrip amplifier for 5-10 GHz
- Hughes: Advocate hybrid integration; have developed 10 GHz monolithic amplifiers
- Bell Labs: Monolithic circuits of all types
- T.I.: Phase array radar amplifier replacement
- Raytheon: Low cost X-band amplifier evaluation
- GE: Use silicon-on-saphire MESFETS
- Rockwell: Digital logic GaAs 8 x 8 parallel multiplexer with 1000 gates, and 4-12 GHz amplifiers

ANALOG APPLICATION
MICROWAVE RECEIVER FRONT END TUNER



APPLICATIONS

- SPREAD SPECTRUM COMMUNICATION RECEIVER, F = 1 TO 20 GHz
- EW SEARCH RECEIVER, F = 0.1 TO 20 GHz
- PULSED RADAR RECEIVER, F = 1 TO 20 GHz
- GLOBAL NAVIGATION RECEIVER, F = 1.5 TO 2 GHz

MONOLITHIC FEATURES

- SINGLE CHIP/LOW COST
- NO TUNING ADJUSTMENTS
- HALF OCTAVE BANDWIDTHS

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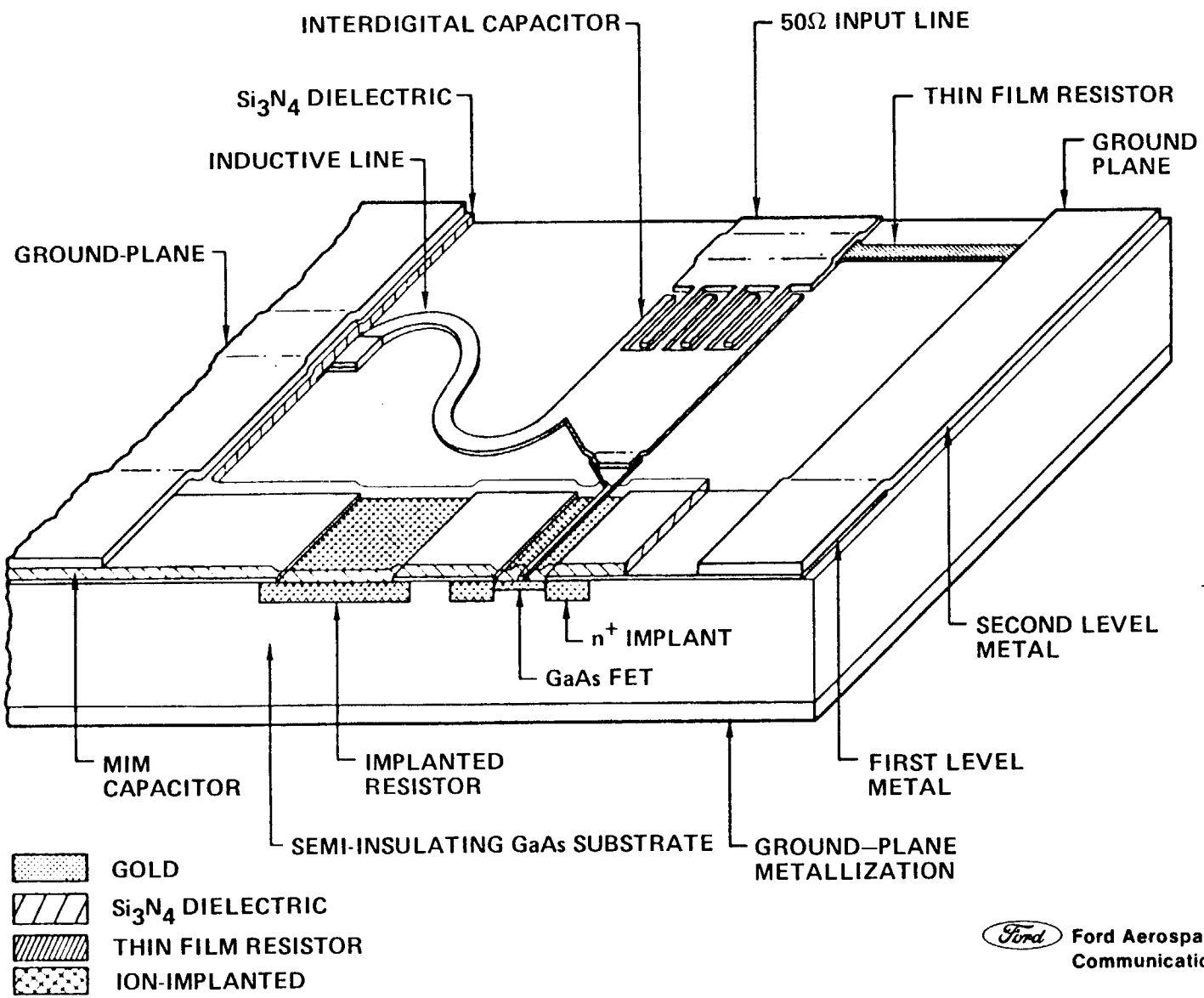
MONOLITHIC MICROWAVE INTEGRATED CIRCUIT



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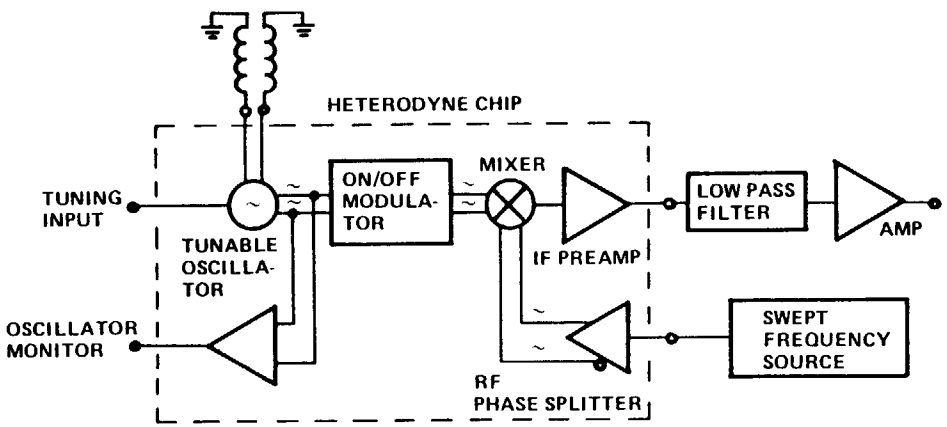
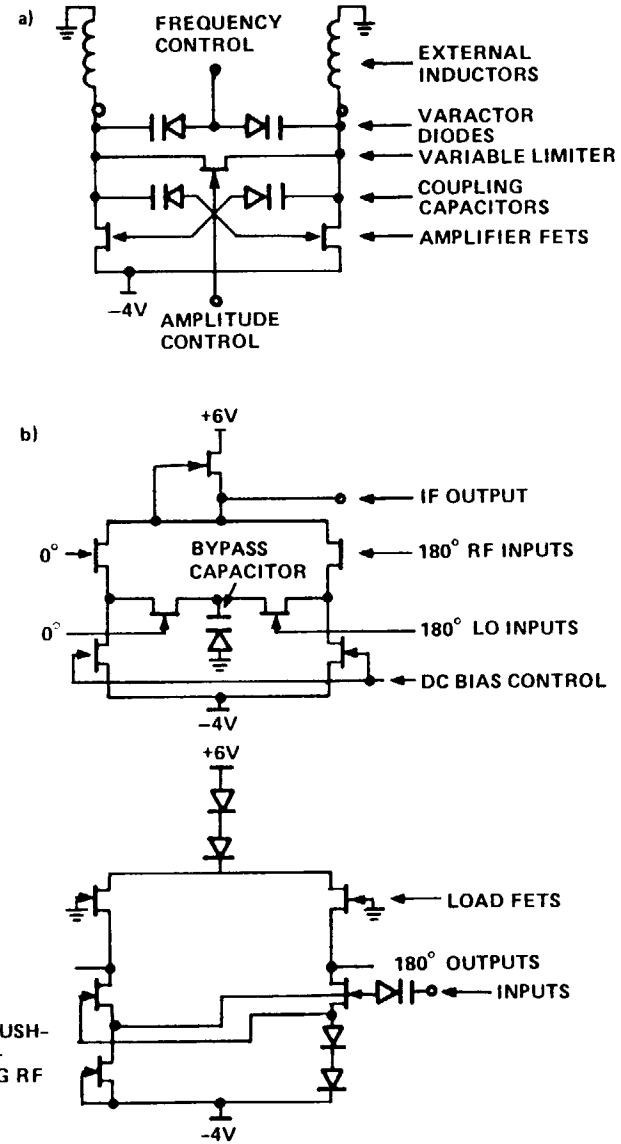
MONOLITHIC GaAs RF SIGNAL GENERATION CHIP DUE TO R. VAN TUYL



SIZE: 400 μm x 350 μm

CIRCUIT DISSIPATION: 300 mw

BLOCK DIAGRAM OF THE HETERODYNE SIGNAL GENERATION CHIP AND ASSOCIATED OFF-CHIP COMPONENTS.



PRINCIPAL CIRCUITS OF THE CHIP: (a) PUSH-PULL LOCAL OSCILLATOR, (b) DOUBLY-BALANCED MIXER, (c) PHASE-SPLITTING RF INPUT BUFFER.

ADVANCES IN MONOLITHIC GaAs LSI/VLSI TECHNOLOGY

- The first major non-silicon integrated circuit technology
- Active devices are easier to fabricate than passive devices
- Realization of gigabit digital circuits
- Very high switching speed - as low as 100 picoseconds
- Development of planar GaAs fabrication technology
- Uses multiple ion implantation directly into semi-insulting GaAs substrates which is compatible with schottky diode FET logic (SDFL)
- Current MSI involves 60-100 gates
- Ion implantation is substituted for epitaxial layers
- No chemical processing used - use projection photo-lithography and electron beam lithography to produce GaAs devices with MESFET gate widths down to the 0.5 μ m level
- Localized ion implantation can be used to optimize individual device
- Fabrication techniques for high density and fine line SI VLSI and GaAs VLSI are quite similar

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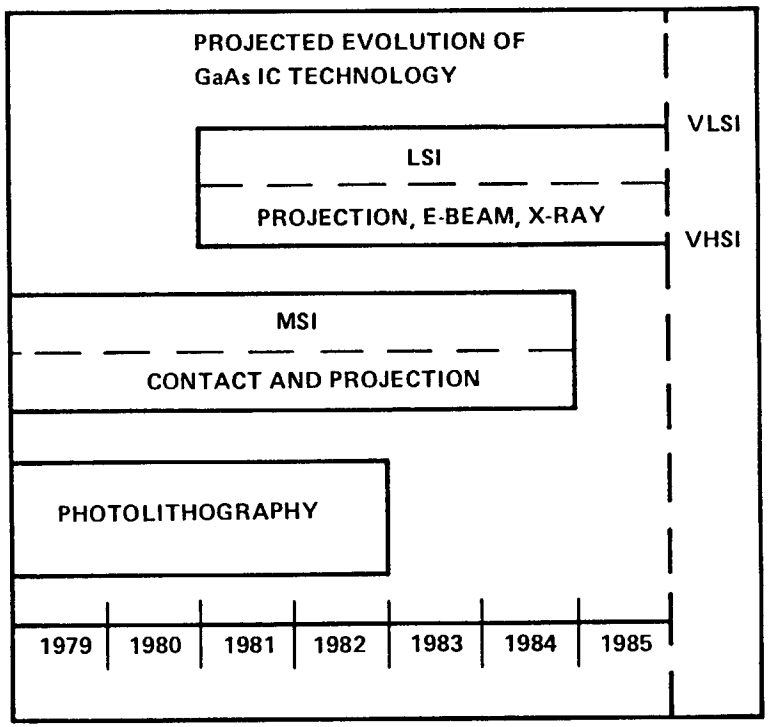
MICROWAVE AND DIGITAL TECHNOLOGIES COMPARED

MICROWAVE AND DIGITAL TECHNOLOGIES COMPARED

TODAY	
MICROWAVE	DIGITAL
0.5 MICRON FEATURES	2-3 MICRON FEATURES
GaAs ACCEPTED	SILICON ONLY
10^2 UNITS	10^6 UNITS
HYBRID	MONOLITHIC
COST-INSENSITIVE	COST-SENSITIVE
SPECIFIC PRODUCTS	BUILDING BLOCKS; GENERALIZED PRODUCTS
FOR SPECIFIC FUNCTIONS	FOR USER-DEFINED FUNCTIONS
IN THE 1980-85 PERIOD	
MICROWAVE	DIGITAL
0.2-0.5 MICRON FEATURES	0.5-1.25 MICRON FEATURES
GaAs AND Si	Si AND GaAs
10^6 UNITS	10^6 UNITS
MONOLITHIC BUILDING BLOCKS	MONOLITHIC BUILDING BLOCKS

THREE APPROACHES TO GaAs INTEGRATION

DEVICE	CIRCUIT COMPLEXITY	IC FABRICATION	POTENTIAL YIELD	SPEED	POWER DISSIPATION
D-MESFET	HIGH (2 POWER SUPPLIES)	SIMPLE	HIGH	HIGH	HIGH-MEDIUM
E-MESFET	LOW	DOPING CRITICAL	LOW	MEDIUM	LOW
E-JFET	LOW	REQUIRES P-N JUNCTION	MEDIUM	LOW	LOW



(25)

SOURCE: LOCKHEED MICROELECTRONICS CENTER

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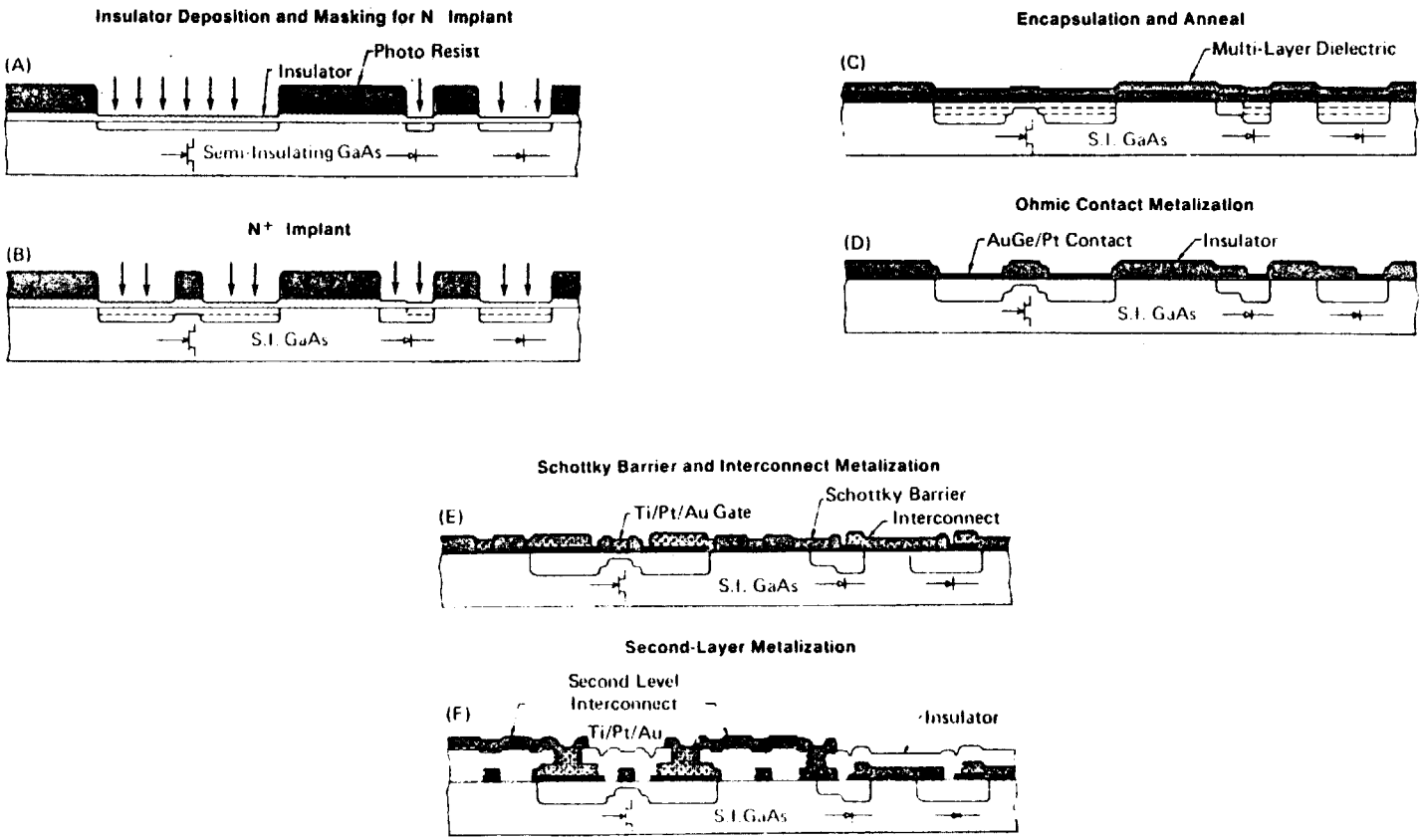
PLANAR GaAs IC FABRICATION STEPS



PLANAR ION-IMPLANTATION PROCESS IS BEING USED TO FABRICATE LOW-POWER GaAs MESFET INTEGRATED CIRCUITS.

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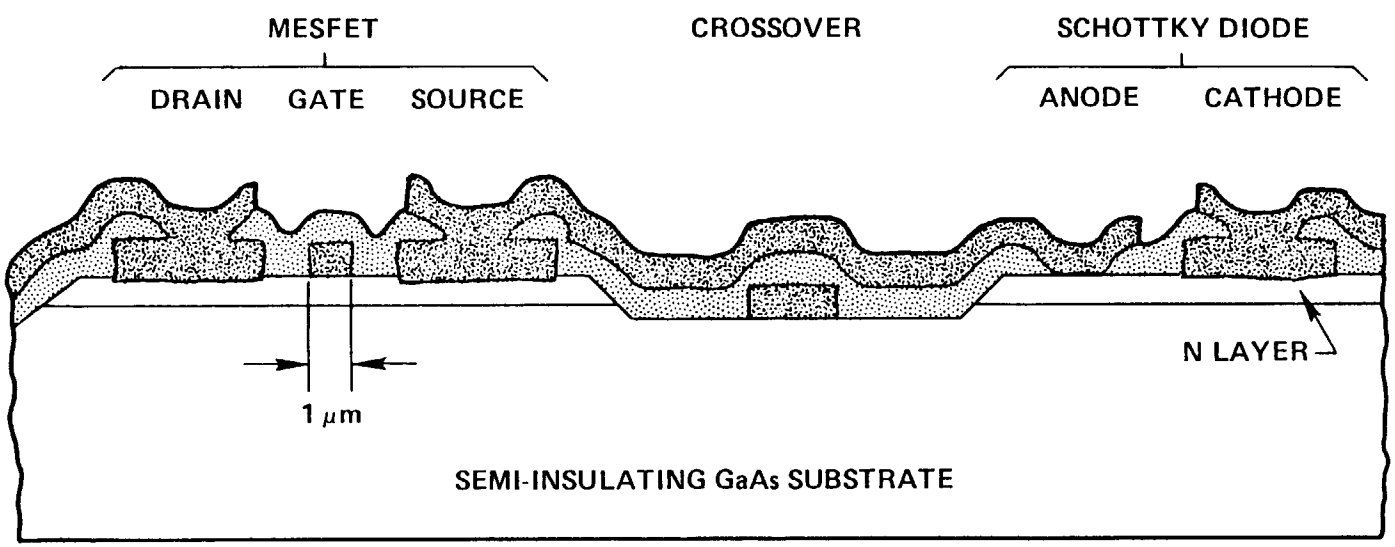
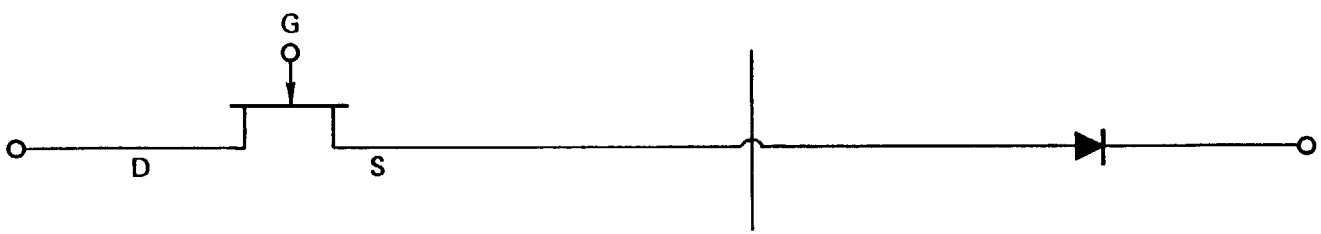
CROSS-SECTION OF IC SHOWING A MESFET, SCHOTTKY DIODE, AND CROSSOVER CONNECTION





MESFET SCHOTTKY DIODE AND INTERCONNECTION WITH SECOND LAYER METALLIZATION

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MICROWAVE ANALOG IC APPLICATION EXAMPLES-PERFORMANCE SUMMARY

ANALOG APPLICATION EXAMPLES	ESTIMATED PERFORMANCE CAPABILITY/PROJECTIONS			
	1980		1987	
	SILICON IC	GaAs IC	SILICON IC	GaAs IC
RECEIVER TUNER FRONT END				
• FREQUENCY F	1 TO 1.5 GHz	18 GHz	1 TO 2.5 GHz	30 GHz
• NF	4 DB	4 DB	2 TO 4 DB	4 DB
• NO. CHIPS	1	5	1	1
PHASE COHERENT DEMODULATOR				
• FREQUENCY F	1 GHz	5 GHz	2 GHz	20 GHz
• BIT RATE	10 MBPS	1 GBPS	100 MBPS	4 GBPS
• NO. CHIPS	1	1	1	1
• INPUT SIGNAL LEVEL	-30 DBM	0 DBM	-30 DBM	-30 DBM
RADAR PULSE ANALYZER				
• FREQUENCY	250 MHz	250 MHz	500 MHz	2 GHz
• NO. CHIPS	2	20	1	2

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GIGABIT DIGITAL IC APPLICATION EXAMPLES - PERFORMANCE SUMMARY

DIGITAL APPLICATION EXAMPLES	ESTIMATED PERFORMANCE CAPABILITY/PROJECTIONS			
	1980		1987	
	SILICON IC	GaAs IC	SILICON IC	GaAs IC
PRN CODE GENERATOR (1 CHIP)				
• FREQUENCY F	0.6 GHz	2 GHz	1 GHz	5 GHz
• NO. STAGES N	16	4	100	16
DIGITAL FREQUENCY SYNTHESIZER				
• FREQUENCY F	1.5 GHz	5 GHz	2 GHz	10 GHz
• NO. CHIPS	2	10	1	1
DIGITAL RF PULSE MEMORY				
• FREQUENCY F	0.5 GHz	–	1 GHz	5 GHz
• NO. CHIPS	12	–	2	2
A/D CONVERTER (SINGLE CHIP)				
• SERIAL				
• SAMPLING RATE	15 MSPS	50	50 MSPS	100 MSPS
• ACCURACY	10 BITS	5	10 BITS	10 BITS
• SERIAL-PARALLEL				
• SAMPLING RATE	50 MSPS	–	100 MSPS	500 MSPS
• ACCURACY	10 BITS	–	10 BITS	9 BITS
• PIPELINED FEED FORWARD				
• SAMPLING RATE	–	5 GSPS	–	10 GSPS
• ACCURACY	–	4 BITS	–	8 BITS

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SWITCHING DEVICES

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MICROWAVE SWITCHING DEVICES: COMPARATIVE PERFORMANCES

DEVICE	SPEED (ns)	HOLDING "ON" POWER (MW)	LOSS/GAIN (dB)	ISOLATION (dB)
PIN diode	1	300	−1.5	30
	50	20	−1.5	30
FET	0.05	100	−3.0	20
	10	0.01	−3.0	20
Ferrite	100	0	−0.5	20
Mechanical	100,000	0	−0.25	60
Dual-Gate FET	0.05	0.001	+15	30

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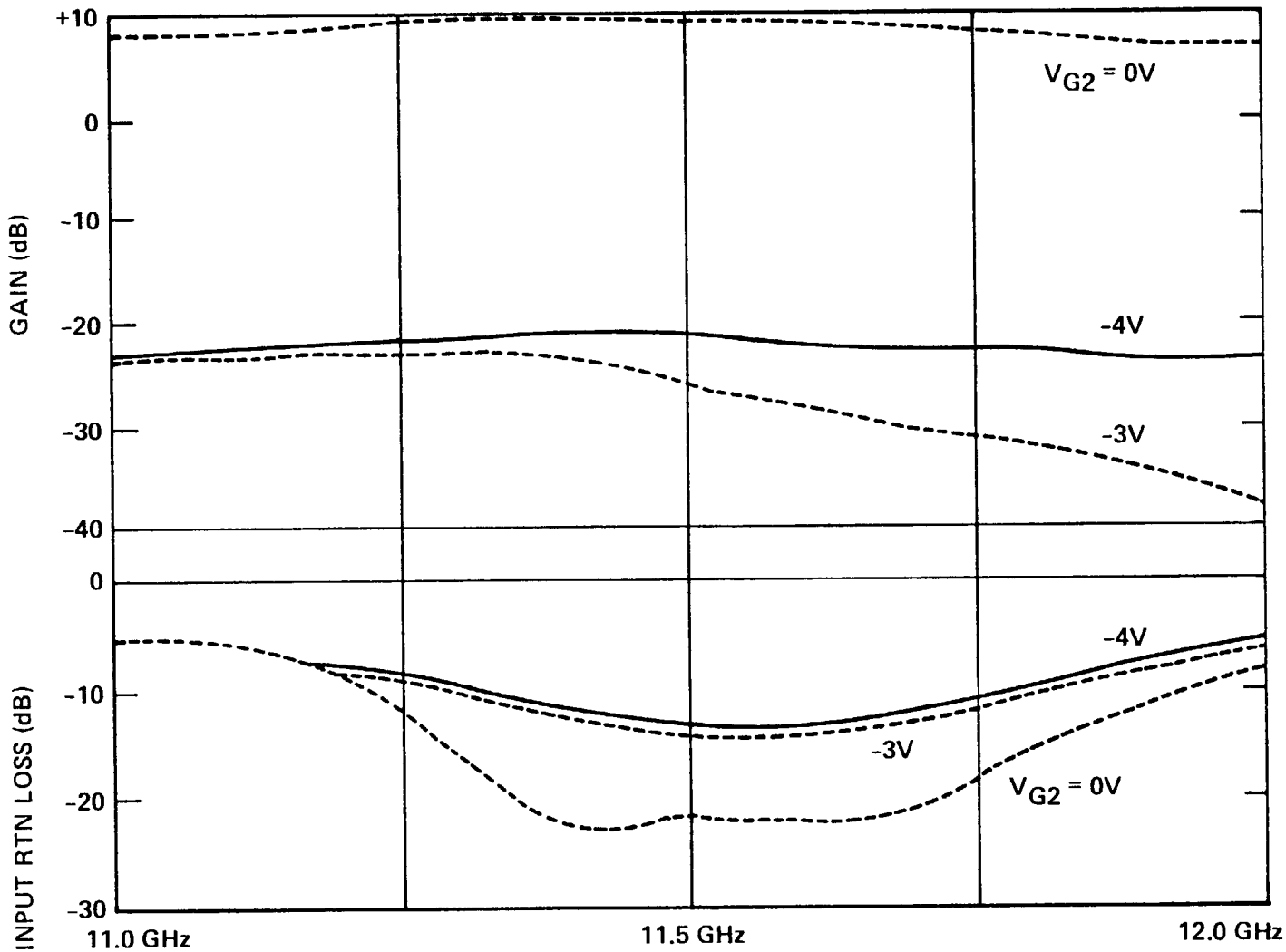
GaAs MESFET SWITCH IMPEDANCE AT 11-12 GHz



FET SWITCH IMPEDANCE REMAINS RELATIVELY CONSTANT UNDER THE LOAD, WITH A NOMINAL GAIN OF 10 dB in X-band. IT CAN BE BIASED TO PROVIDE OVER 30 dB ISOLATION FOR A TOTAL ON-OFF RATIO OF 40 dB.

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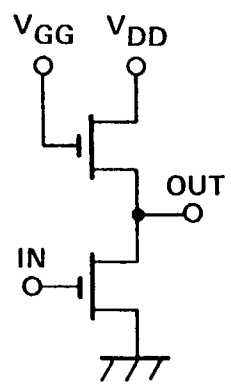
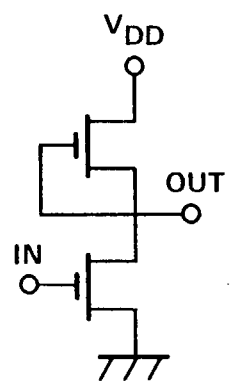
FUJITSU MOSFET DEVICES USING GaAs

- ADAPTABLE TO LSI AND HIGH SPEED
- ALLOWS A HIGHER VOLTAGE SWING ON A SCHOTTKY GATE THAN GaAs MESFETS TO MATCH THE TRANSISTOR (FET) VOLTAGES INCLUDED IN THE LSI CHIP

GaAs MOSFET LOGIC

TYPE	E/E	E/D
GATE LENGTH	1.5 μm	2.0 μm
GATE WIDTH DRIVER LOAD	100 μm 10 μm	200 μm 80 μm
EQUIVALENT CIRCUIT FOR UNIT INVERTER		

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BASIC 2X2 MATRIX SWITCH ELEMENTS

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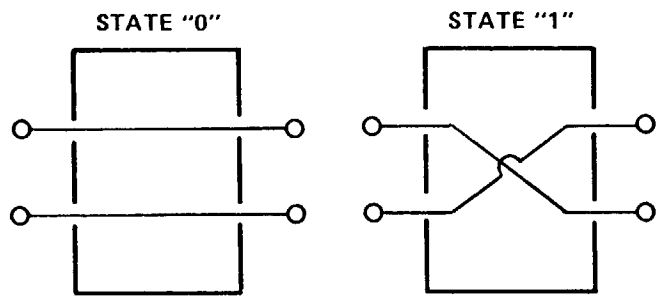

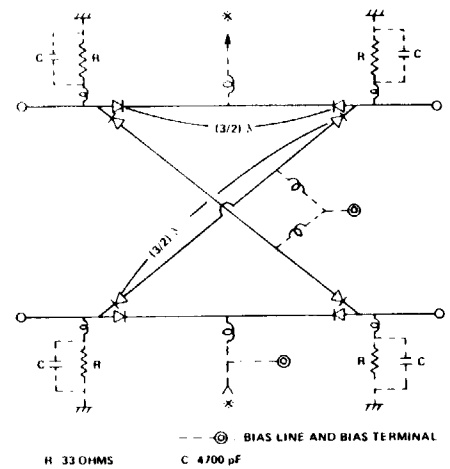

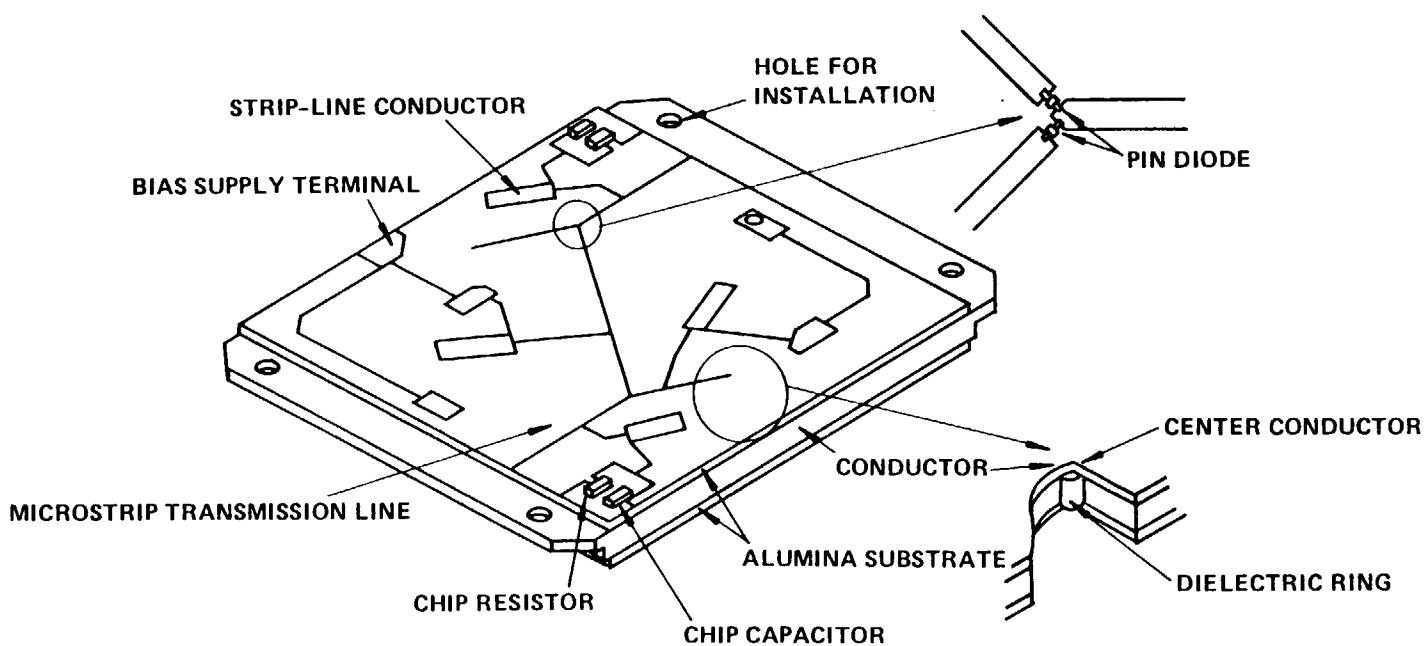

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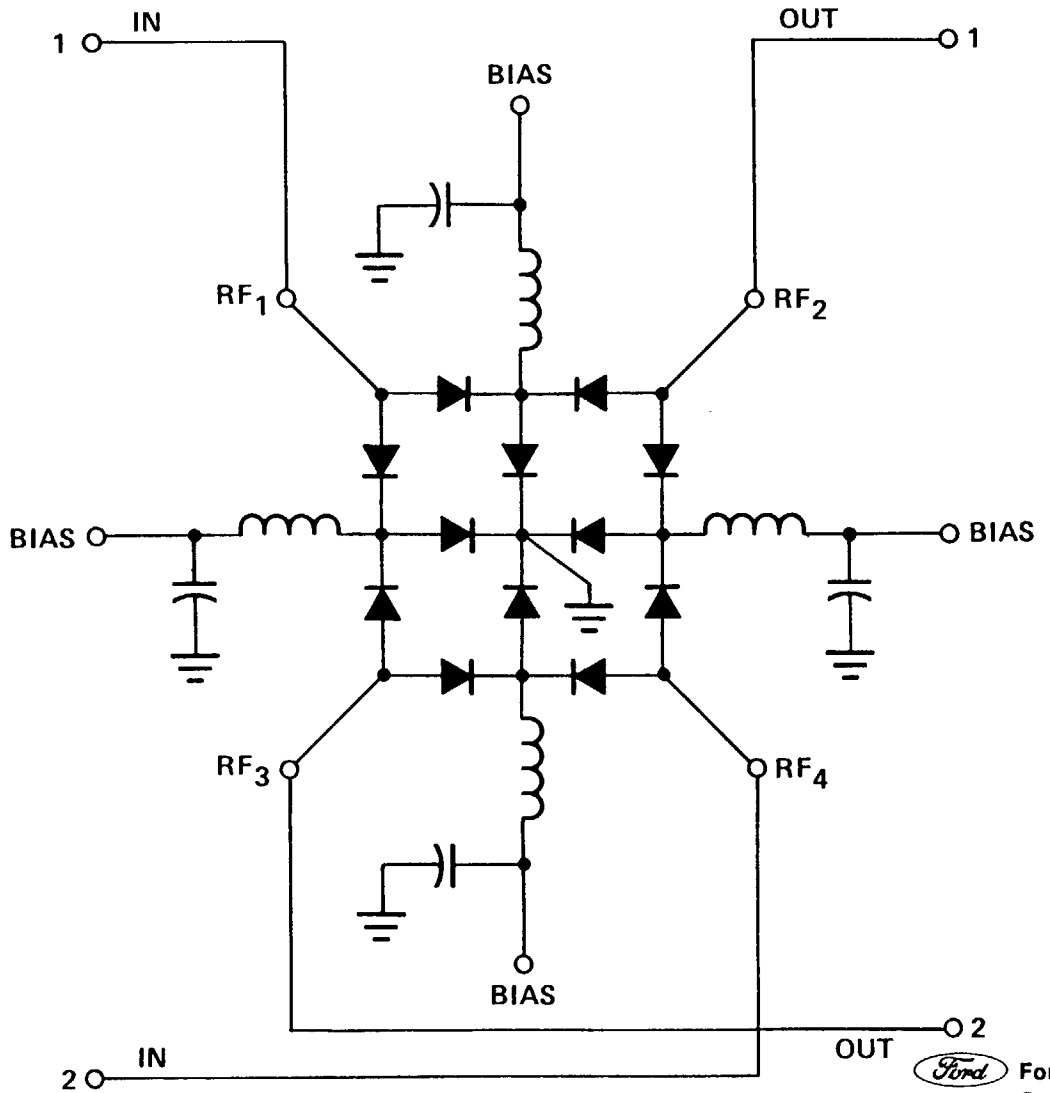
2 X 2 BETA ELEMENT USING SCHOTTKY DIODES



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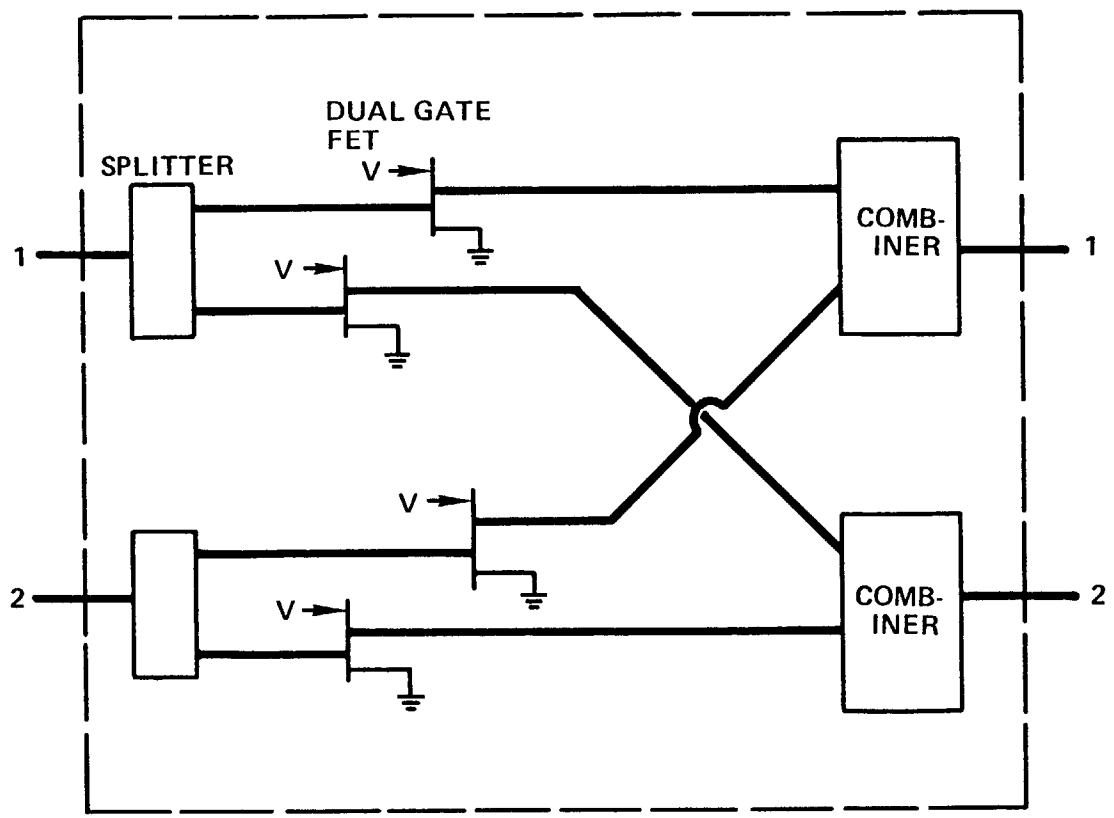
REARRANGEABLE BETA SWITCH USING DUAL GATE FETs



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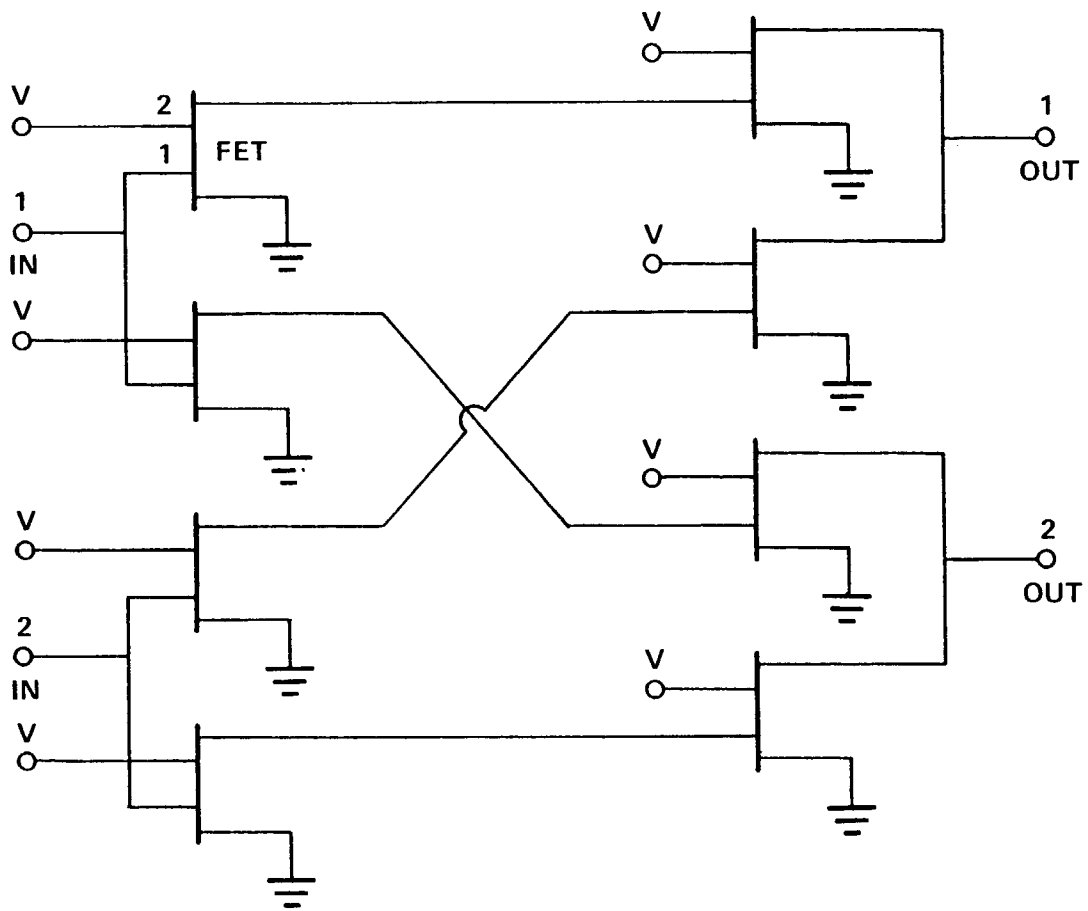
GaAs FET 2 X 2 SWITCH DESIGNED BY DEXCEL FOR FORD AEROSPACE USING DUAL GATE FETS



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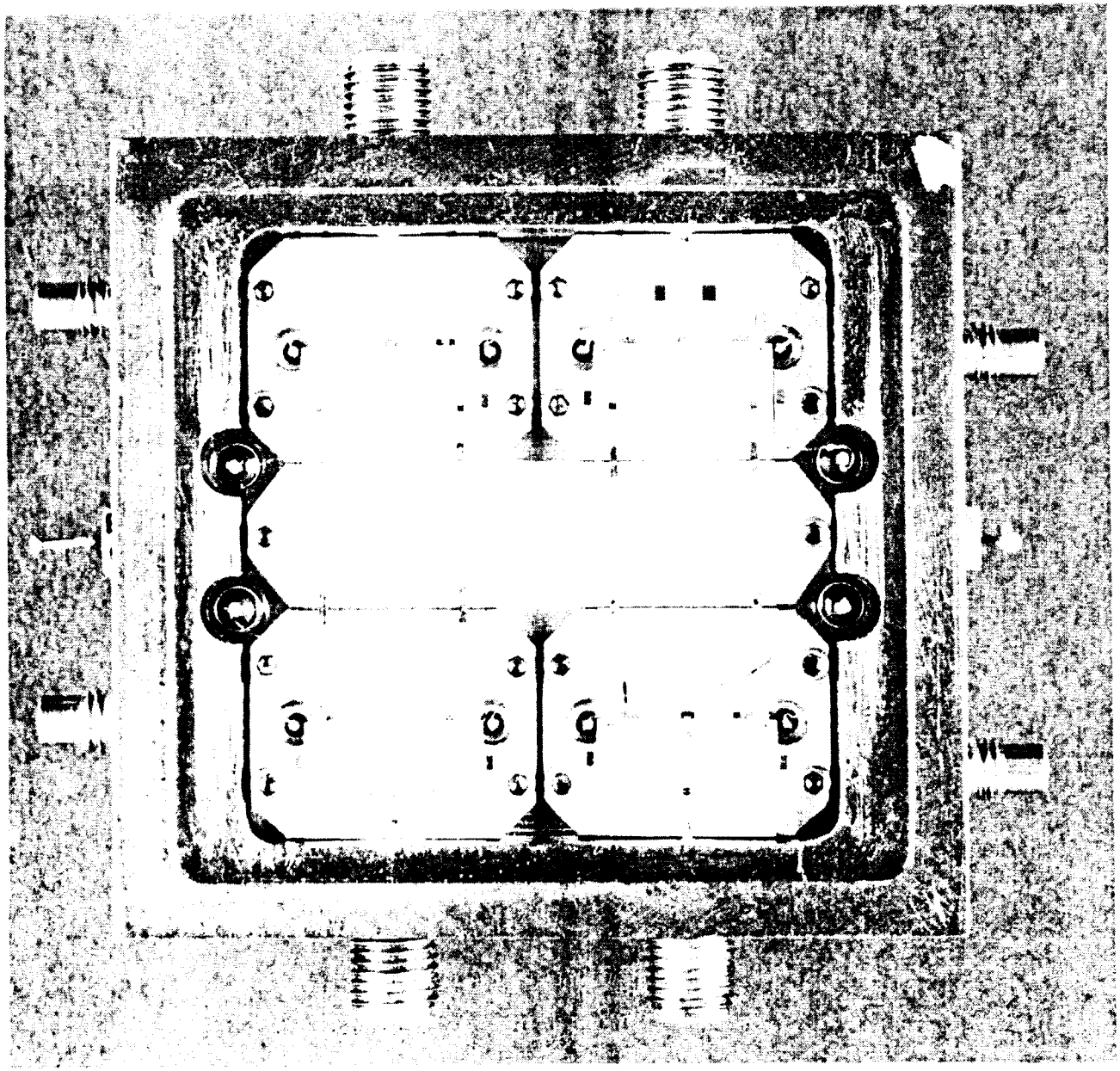
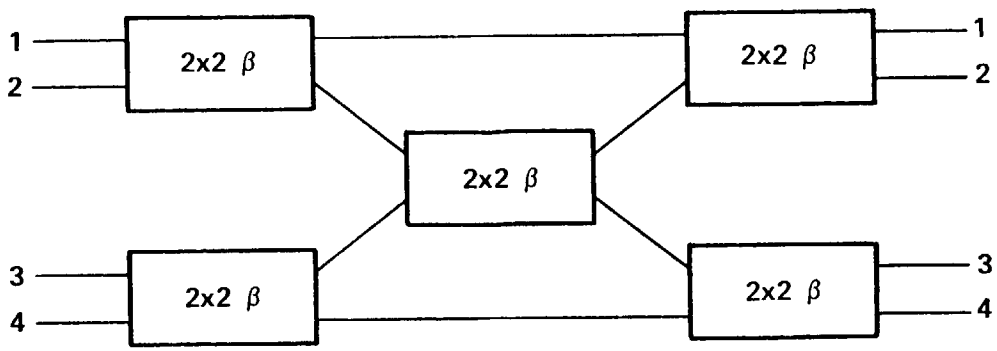
2 X 2 DUAL-GATE FET SWITCH

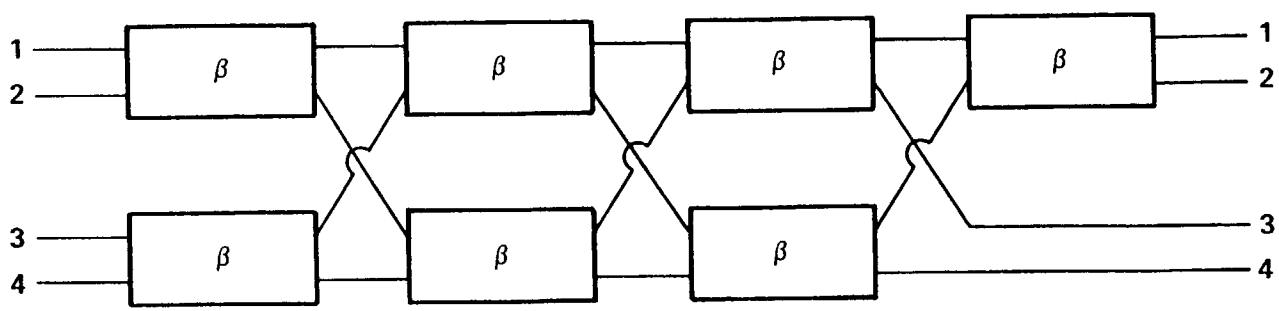


4 X 4 PLANAR SWITCH MATRIX USING BETA ELEMENTS (2X2)

ADVANCED WESTAR



JAPAN KDD



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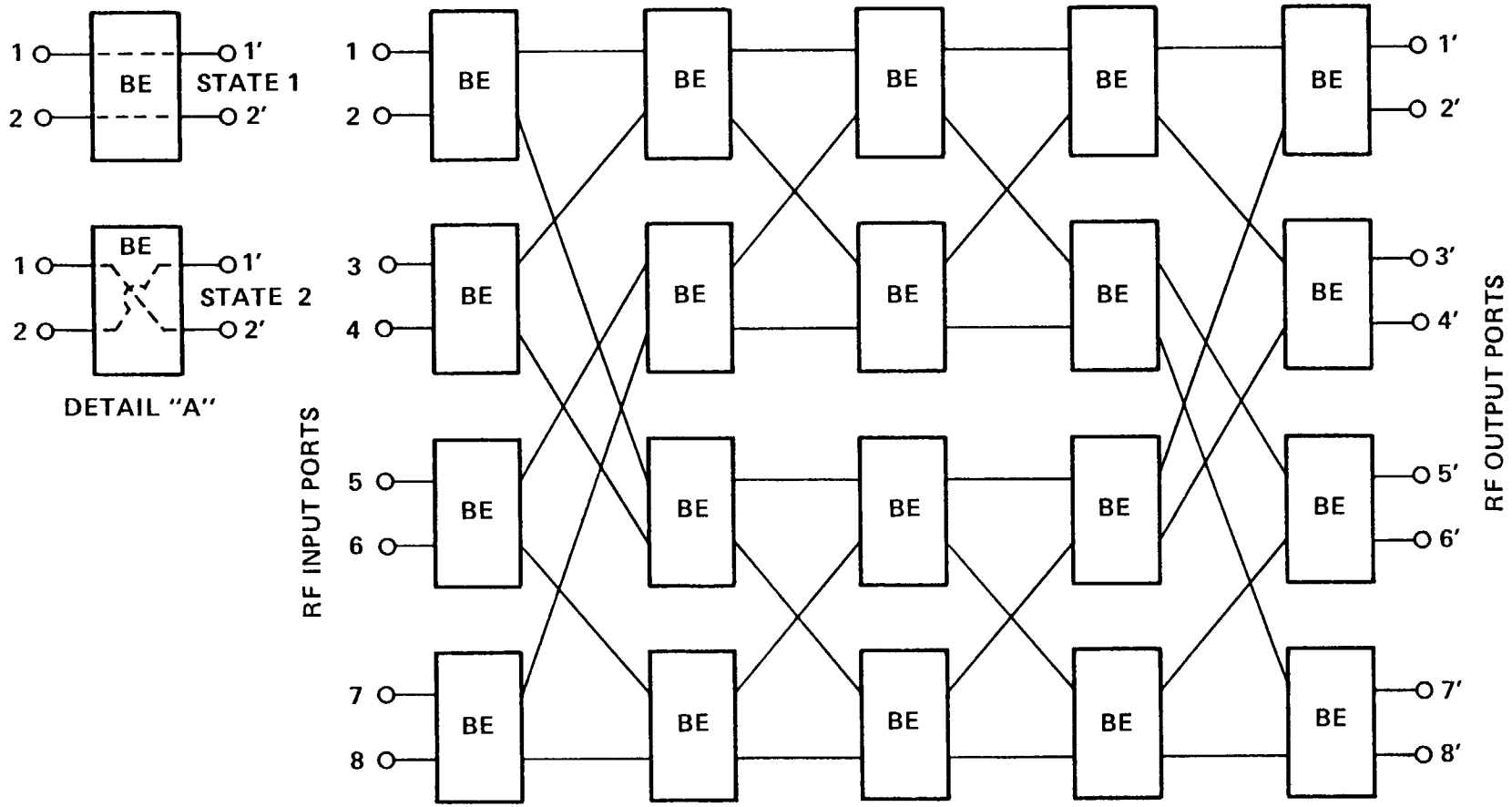
CANDIDATE - PLANAR REARRANGEABLE SWITCH



REARRANGEABLE SWITCH ARCHITECTURE CONCEPT

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BASIC MONOLITHIC GALLIUM ARSENIDE BUILDING BLOCKS AND CANDIDATES FOR A 1987 100 x 100 MATRIX SWITCH

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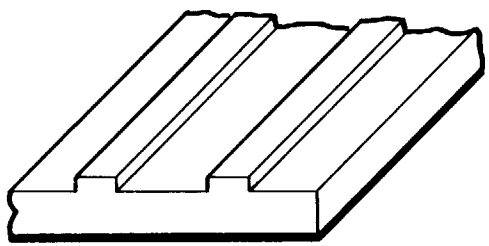
NEW TECHNOLOGIES

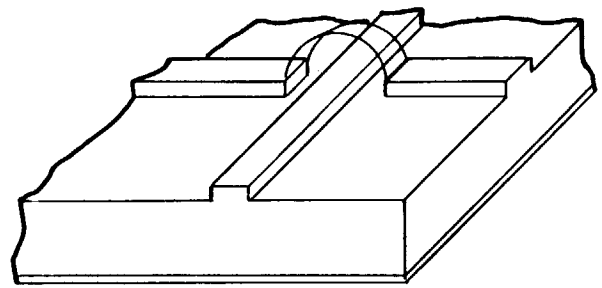
- Multiple layer buried-line
- Miniature FET distribution/combiner lines
- High isolation beta elements
- Studies of alternate path reliability techniques
- Maximum packing density chip fabrication
- Lowest loss FET/schottky diodes switch techniques

FIRST LOOK -- CROSS-OVER TECHNIQUES FOR MICROWAVE LINES IN GaAs CIRCUITS

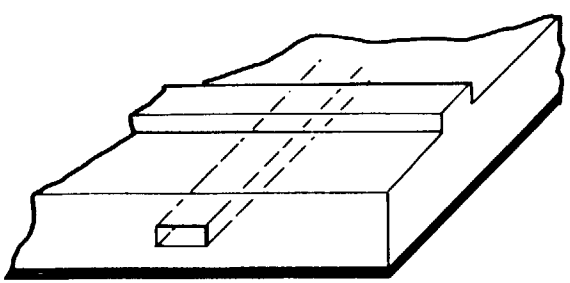
PARALLEL LINE



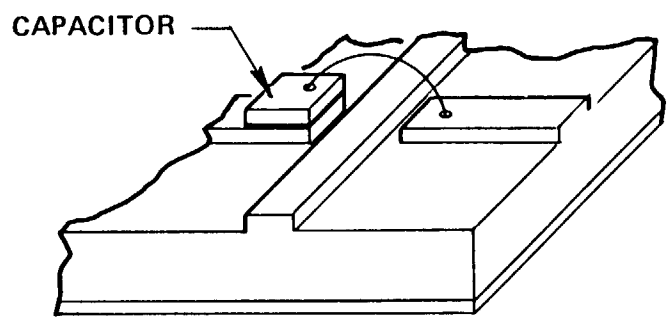
CROSSOVER USING AIR BRIDGE



ORTHOGONAL BURIED LINE



CROSSOVER USING SERIES RESONANT CHART CKT



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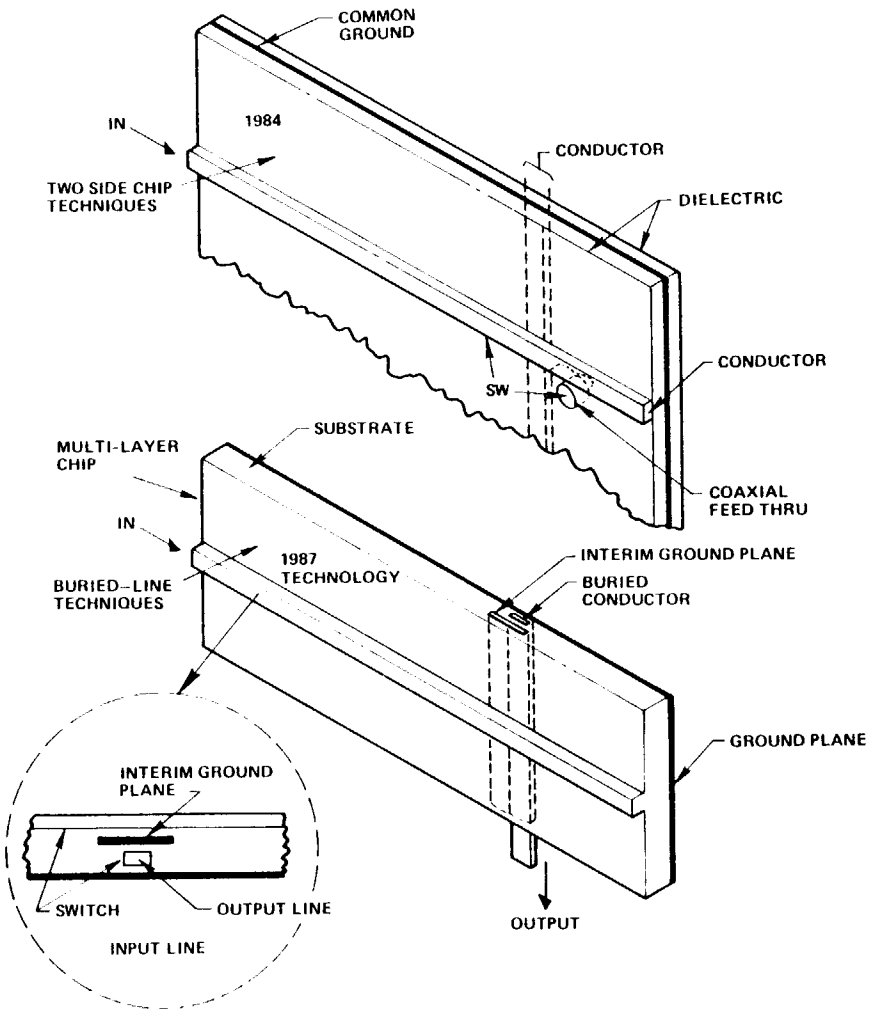
CANDIDATE - BURIED LINE CROSSPOINT SWITCH



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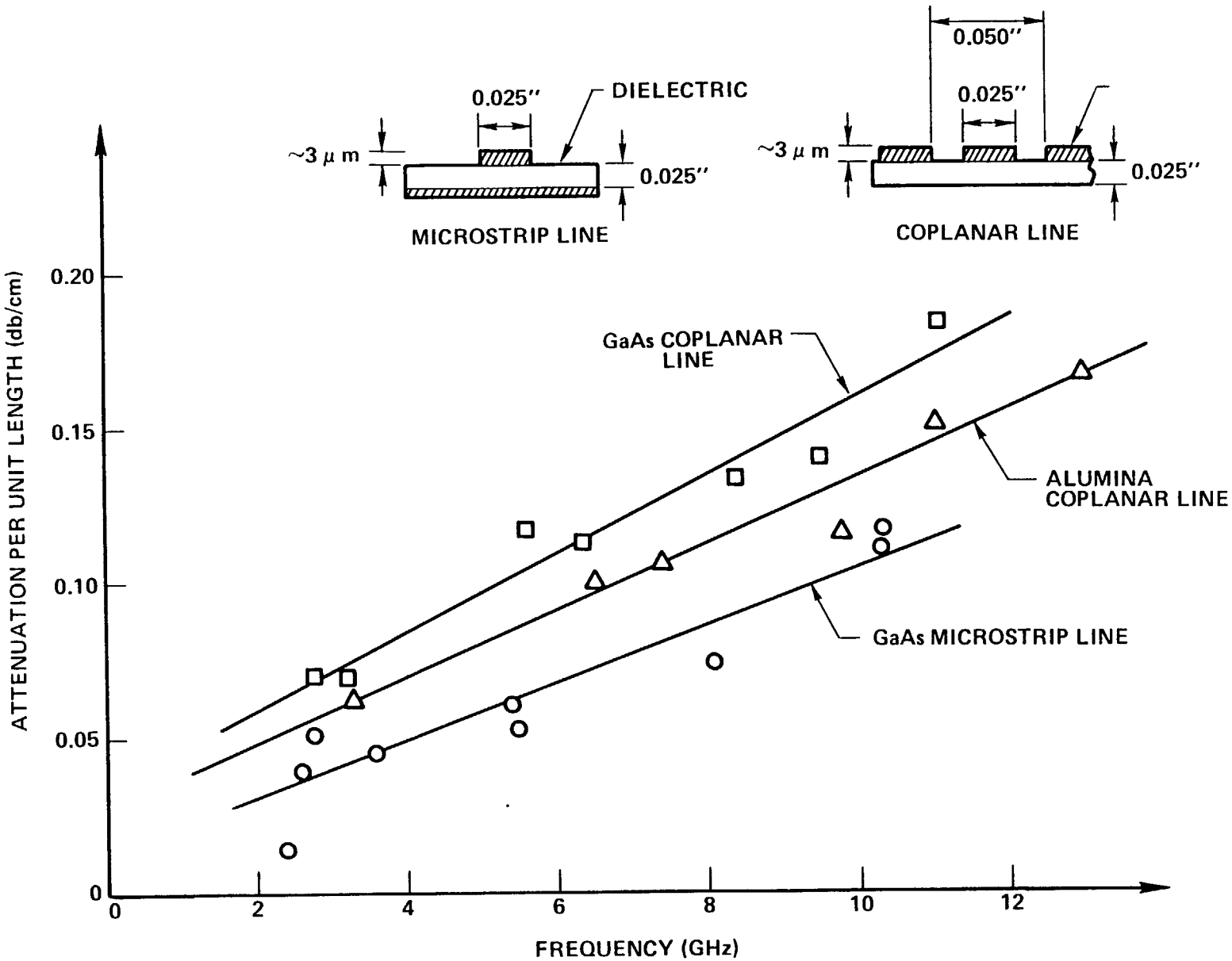
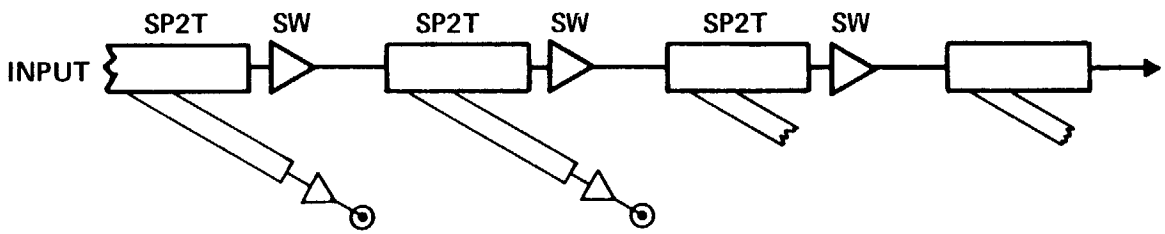
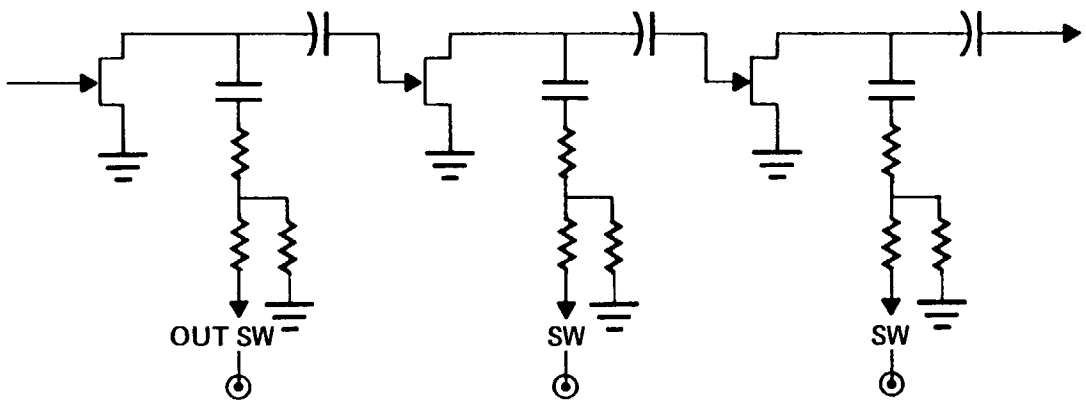

0.025"
DIELECTRIC
~3 μ m
0.025"
MICROSTRIP LINE
0.050"
0.025"
~3 μ m
0.025"
COPLANAR LINE
ATTENUATION PER UNIT LENGTH (db/cm)
0.20
0.15
0.10
0.05
0
GaAs COPLANAR LINE
ALUMINA COPLANAR LINE
GaAs MICROSTRIP LINE
0
2
4
6
8
10
12
FREQUENCY (GHz)

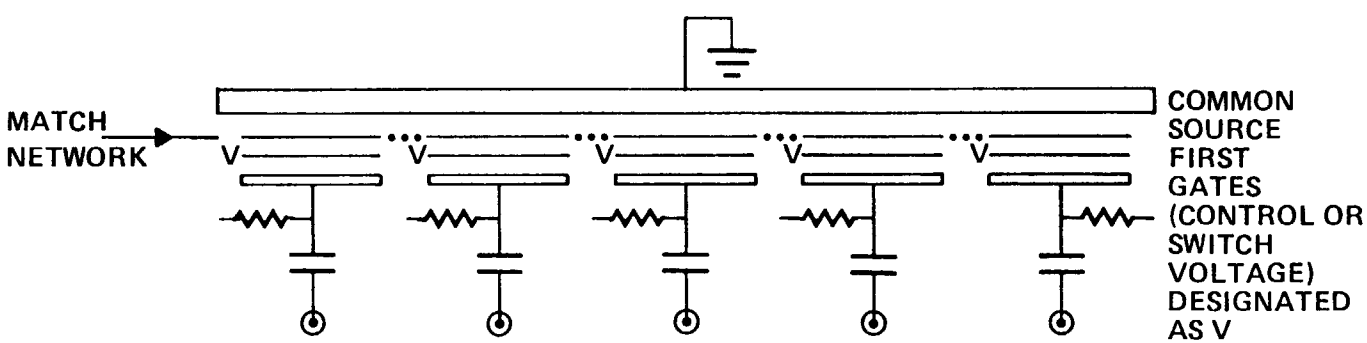
CANDIDATE INPUT NETWORK CONCEPTS



MITRE SWITCHED DIODE SIGNAL DISTRIBUTOR



CASCADED FET AMPLIFIERS WITH 1:1 GAIN PER STAGE



COMMON SOURCE MULTIPLE GATE/DRAIN ACTIVE FET SIGNAL DISTRIBUTOR AND SWITCH

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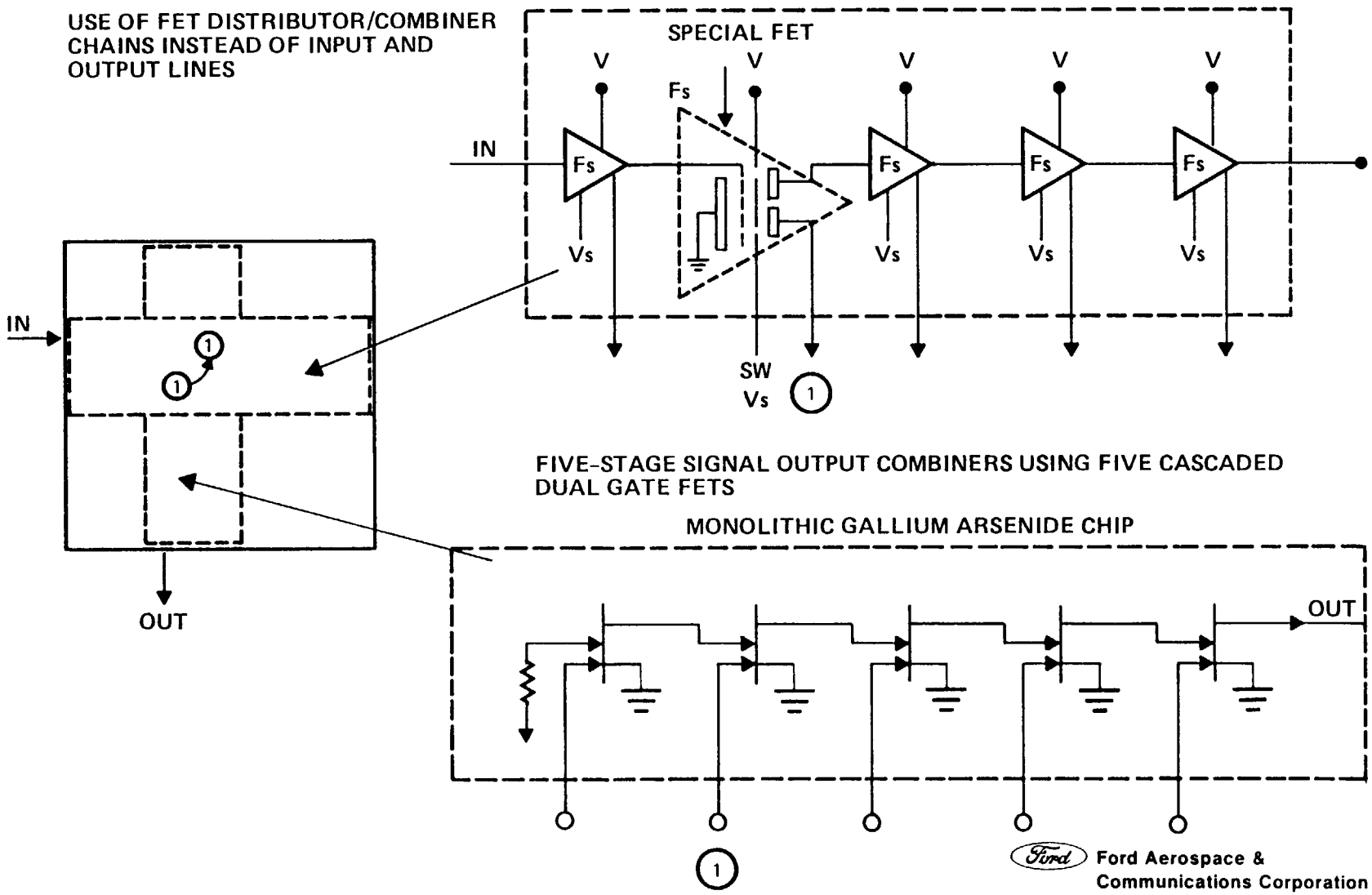
OTHER CONCEPTS

ADVANCED MESFET TECHNOLOGY APPLIED TO
5-STAGE INPUT DISTRIBUTOR SWITCH

MONOLITHIC CHIP

USE OF FET DISTRIBUTOR/COMBINER
CHAINS INSTEAD OF INPUT AND
OUTPUT LINES



FIVE-STAGE SIGNAL OUTPUT COMBINERS USING FIVE CASCADED
DUAL GATE FETS

MONOLITHIC GALLIUM ARSENIDE CHIP

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LARGE IF SWITCH MATRIX DESIGN CONCEPT

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BASIC ELECTRICAL SPECIFICATION

- 100 x 100 - made up of 100 10 x 10 chips
- Bandwidth - 1 GHz min in C-band/Ku-band
- Isolation - 60 dB
- Switch time - 10 ns
- Insertion loss - 0 dB
- VSWR - 1.4:1
- DC power - TBD
- Bandpass insertion - ±0.5 dB loss variation
- Bandwidth insertion - ±0.5 ns delay variation

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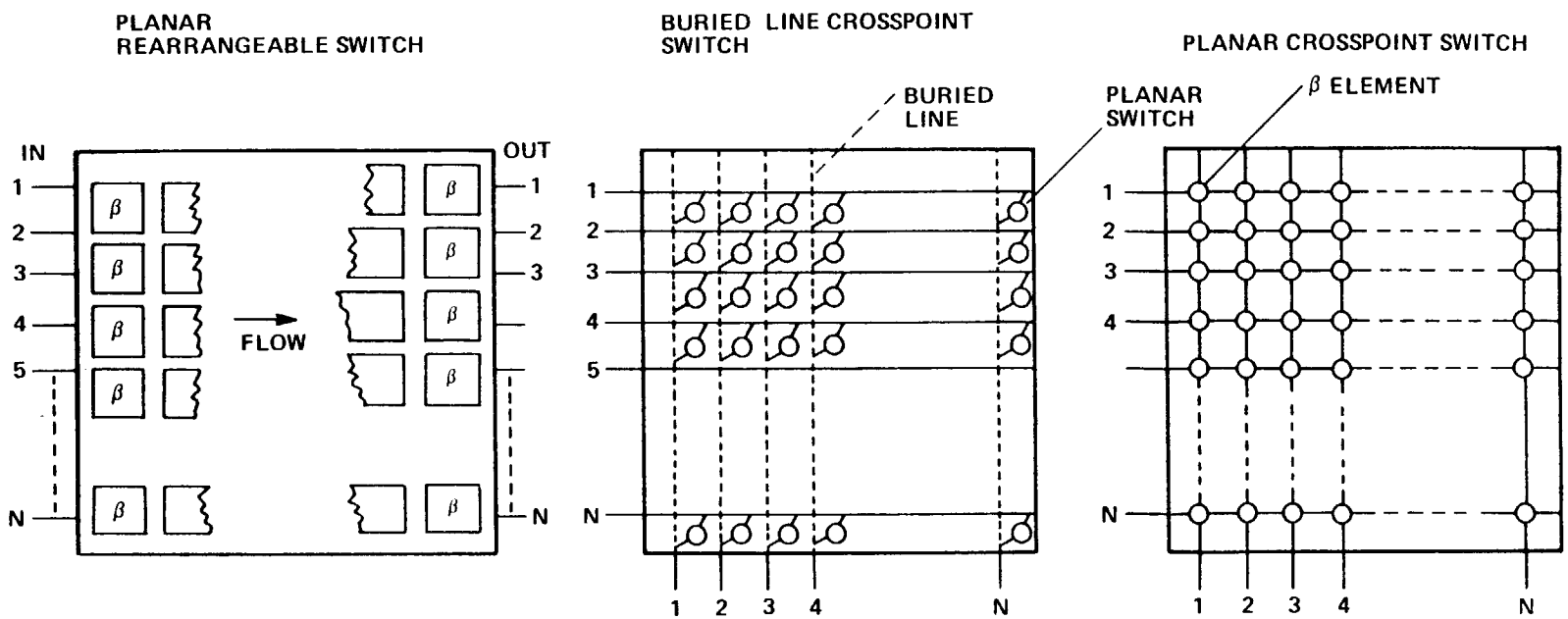
THREE CANDIDATE MONOLITHIC SWITCH MATRIX APPROACHES



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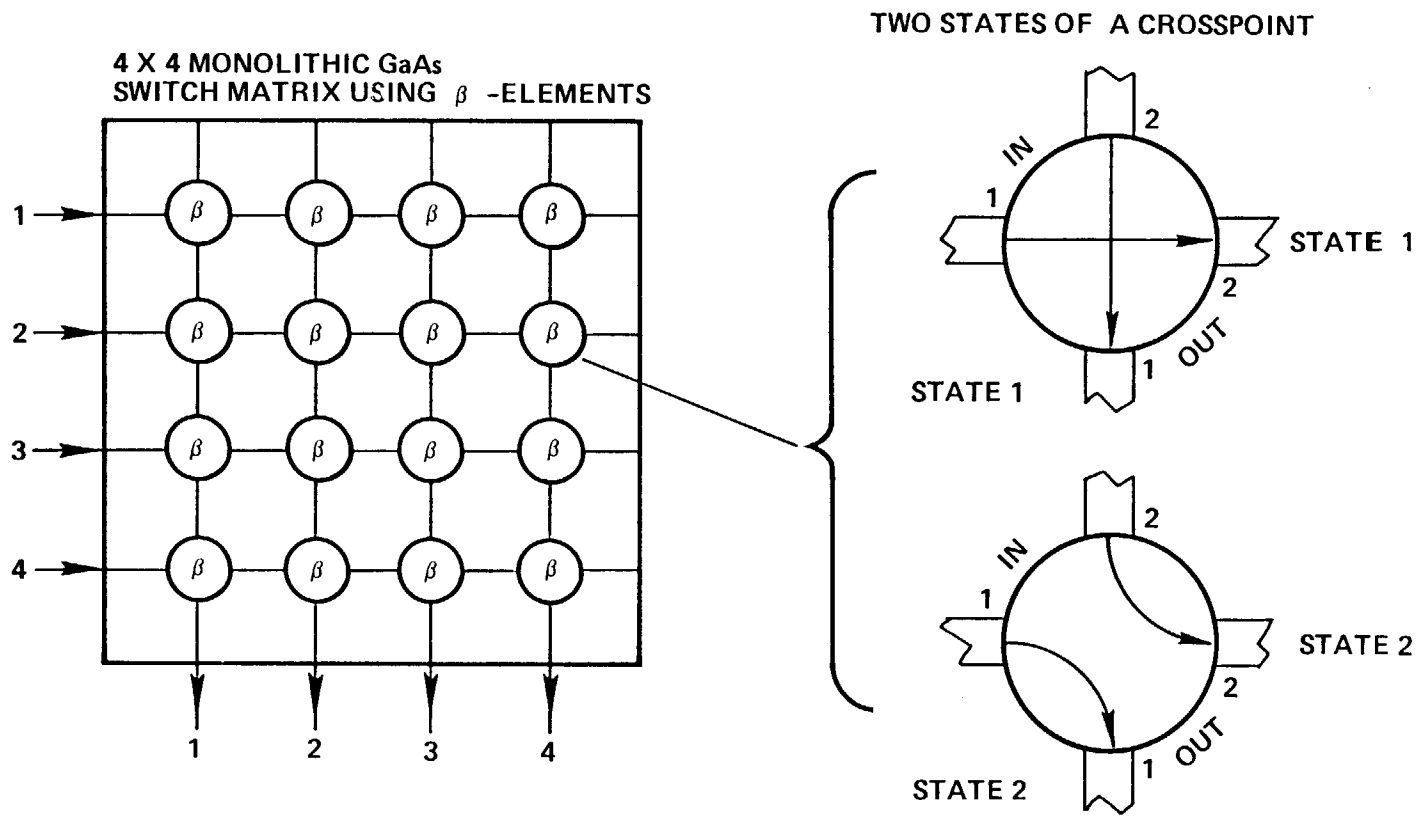
THREE CANDIDATE MONOLITHIC SWITCH MATRIX APPROACHES



CANDIDATE SWITCHES DIODE TRANSFER 2 X 2 or DUAL GATE FET SWITCH

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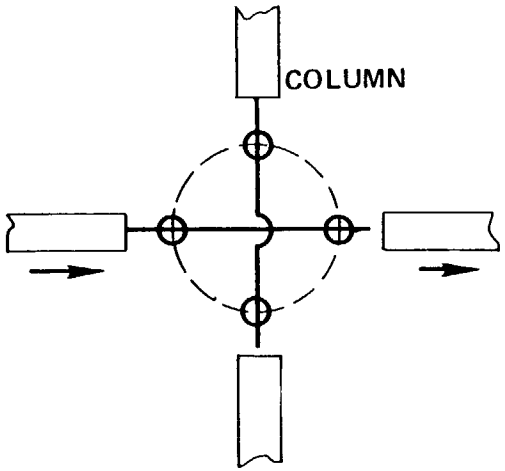
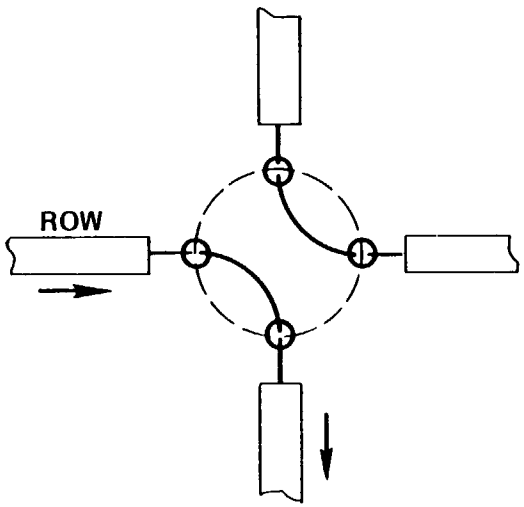
BETA ELEMENT MODE OR BROADCAST MODE AT EACH CROSSPOINT

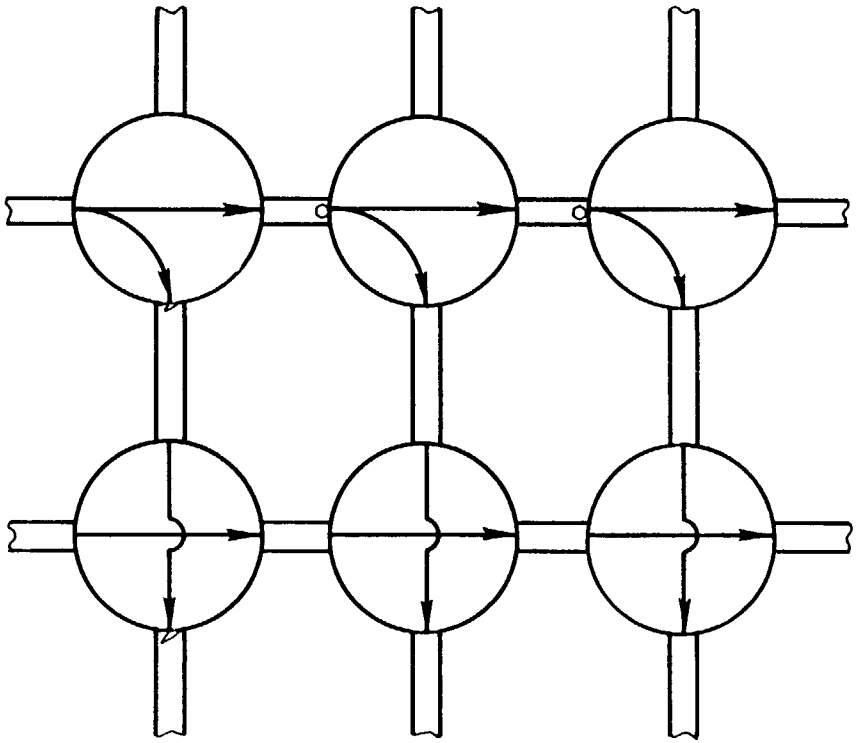
β-ELEMENT
CROSSPOINT-NON CONTACT



CROSSPOINT-CONTACT



BROADCAST MODE



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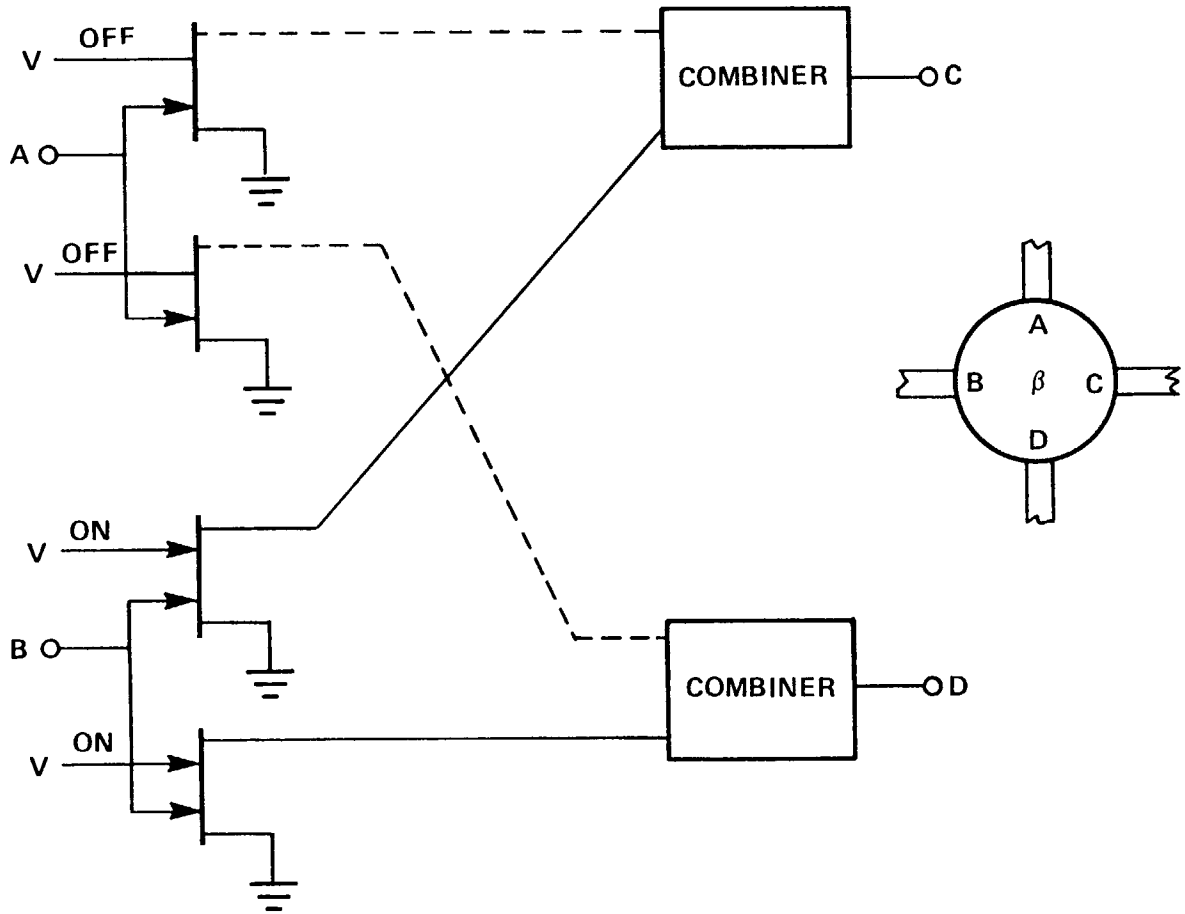
FET BETA ELEMENT IN BROADCAST MODE



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LARGE BASEBAND ANALOG SWITCH MATRIX DESIGN CONCEPT

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BASE BAND SWITCH MATRIX DESIGN REQUIREMENTS

- The matrix size shall be 100 x 100, and shall on command connect the set of 100 inputs to any combinations of 100 outputs on a one to one basis. It shall be capable of reconfiguring by command from any existing connectivity pattern to any other pattern.

- Only space qualifiable components and materials shall be utilized in this design. All parts or semiconductor devices to be available by 1985.

- All fabrication and packaging techniques used shall be such as to provide a space qualifiable design.

GENERAL REQUIREMENTS FOR BASE BAND SWITCH

• Switch size NXN	N = 100
• Reconfiguration rate	2 ms max
• Switch time	10 ns max
• Frequency response	25 MHz - 500 MHz
• Insertion loss	15 dB max
• Isolation between any output port	40 dB below signal level
• Input signal structure	
- Digital	25 Mb/s - 500 Mb/s
- Analog	25 MHz - 500 MHz
- Level	-10 dBm thru - 50 dBm
- Dynamic range	±10 dB about input level
- Input-output impedance	50Ω nominal
- V.S.W.R.	1.2:1 Z_0 =(50 ohms)

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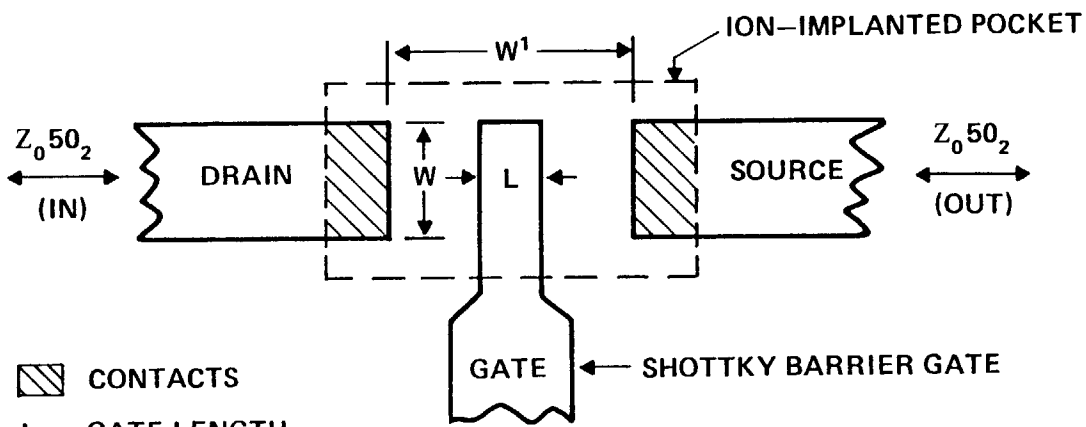
SEMICONDUCTOR TECHNOLOGY

- GaAs MESFETS
  - Switching
  - Logic
  - Amplification
- C-MOS-SOS
  - Switching
  - Logic
  - Amplification

GaAs MESFET SWITCH



CONTACTS

L = GATE LENGTH

W = GATE WIDTH

W¹ = LENGTH OF CHANNEL

INPUT OUTPUT METAL LOOKS LIKE 50_2 TRANSMISSION LINE

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TYPICAL CHARACTERISTICS OF MESFET

DESIGNED FOR SWITCHING BASEBAND
SIGNALS TO 1 GHz

PARAMETERS	A-SWITCH W = 300 μm	B-SWITCH W = 120 μm
INSERTION LOSS	.67 dB	.67 dB
ISOLATION	28 dB	28 dB
FREQUENCY RESPONSE	1 GHz	1 GHz
TYPICAL ON RESISTANCE	8Ω	12Ω
TYPICAL OFF RESISTANCE	16 kΩ	16 kΩ
SWITCH TIME	~2 NS	~2 NS

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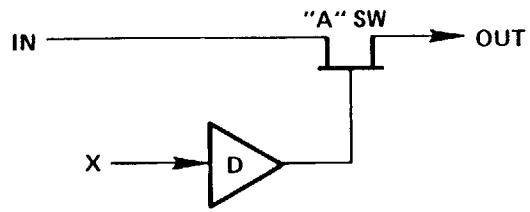
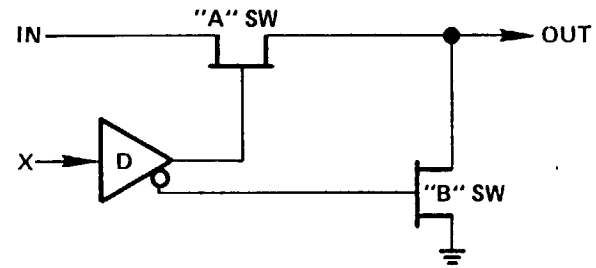
CANDIDATE GaAs MESFET SWITCH CONFIGURATIONS

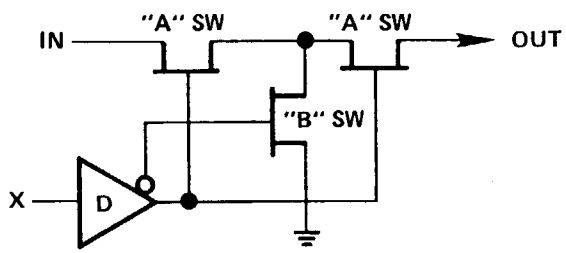
A) SIMPLE FET SWITCH ("S")



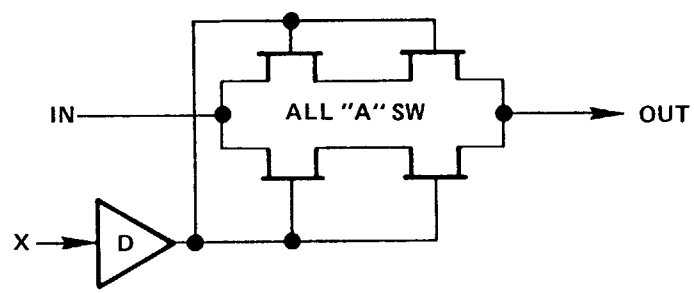
B) "L" SERIES–SHUNT



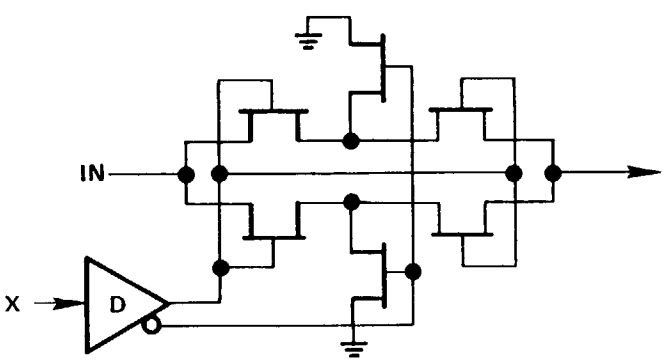
C) "T" SWITCH SERIES–SHUNT–SERIES



D) REDUNDANT SERIES PARALLEL "SP"



E) "PT" PARALLEL T SWITCH



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SWITCH CHARACTERISTICS

TYPE	INSERTION	ISOLATION	REDUNDANCY	BW	CROSS BAR SWITCH APPLICATION
SERIES (S)	~.67 dB	~28 dB	NONE	>1 GHz	POOR
SERIES-SHUNT (L)	~.67 dB	~28 dB	NONE	~1 GHz	POOR
SERIES-SHUNT-SERIES (T)	~1.34 dB	~53 dB	NONE	~1 GHz	GOOD
SERIES-PARALLEL (SP)	~.67 dB	~28 dB	SINGLE AND SOME, TWO SWITCH FAILURES	<1 GHz >500 MHz	FAIR
PARALLEL-T (PT)	.67 dB	~50 dB	SINGLE AND SOME TWO SWITCH FAILURES	<1 GHz >500 MHz	GOOD

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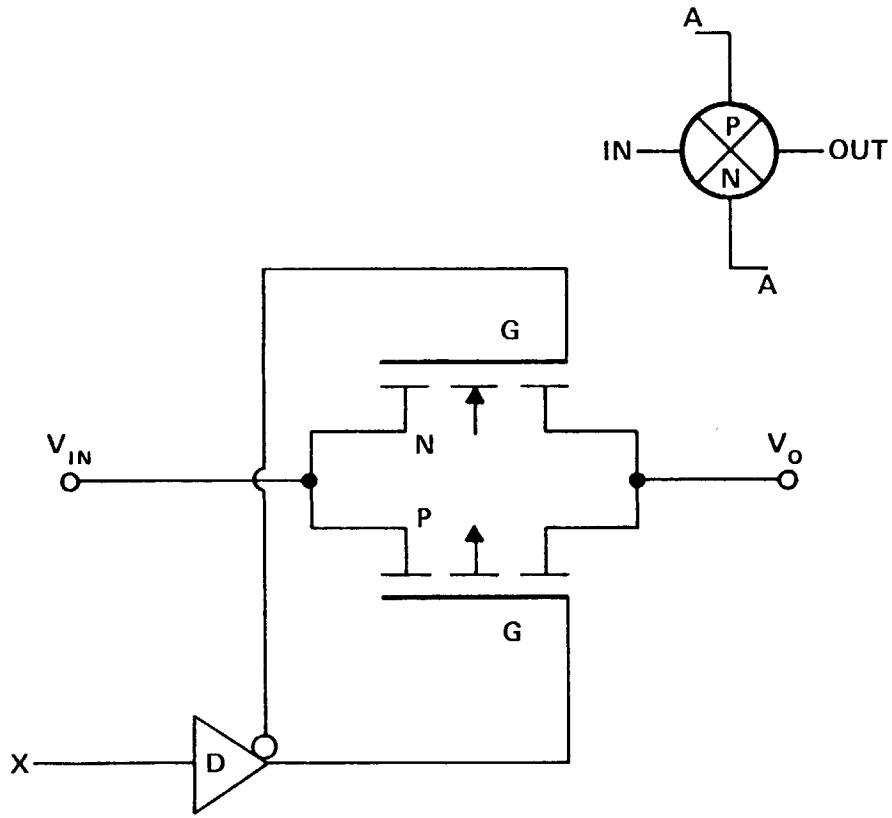
BASIC ANALOG C-MOS FET TRANSMISSION GATE



BI DIRECTIONAL ANALOG FET SWITCH CONDUCTS WHEN V_{GS} OF N–MOS TRANSISTOR IS POSITIVE WITH RESPECT TO V_S, AND THE P–MOS TRANSISTOR CONDUCTS WHEN V_{GS} GOES NEGATIVE WITH RESPECT TO V_S

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CHARACTERISTICS OF TRANSMISSION GATE FET

Frequency response	$<$ 500 MHz
Isolation	$\sim$ 30 dB
Insertion loss(Z=50)	$\sim$ 3 dB
Switching speed	$<$ 210 ns
FETswitch resistance (800μm width)	
ON	50 Ω
OFF	$>$ 50 kΩ

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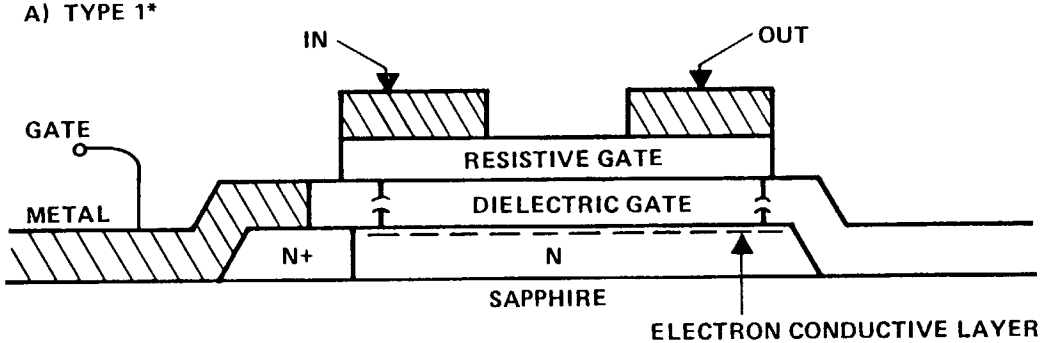
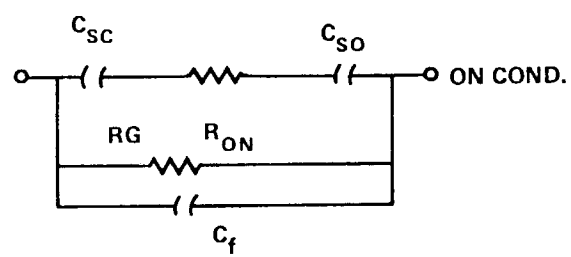
RESISTANCE GATE FET SWITCHES

A) TYPE 1*



EQUIVALENT CKT AT R_f



* BY PING KWOK (HUGHES)

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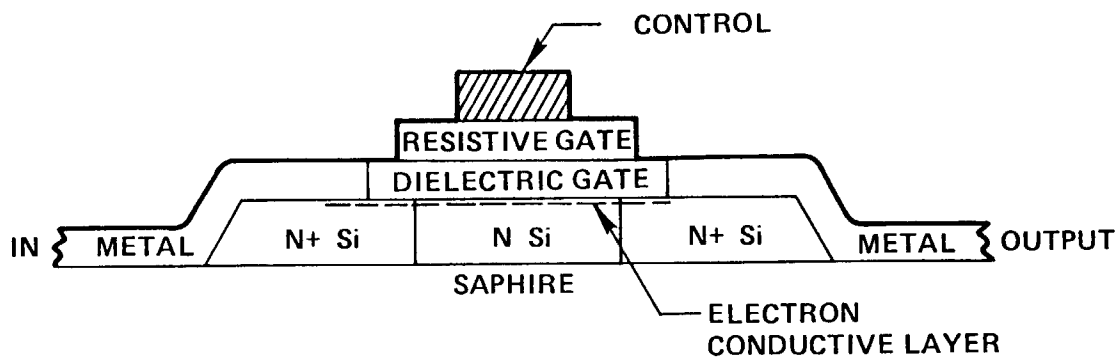
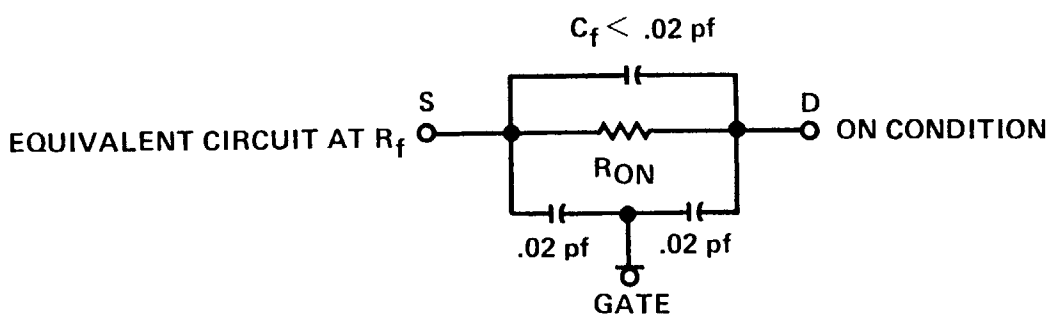
TYPE II**
D.C. COUPLED RESISTANCE GATE FET





** BY HAGON (ROCKWELL)

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RESISTANCE GAT SWITCH CHARACTERISTICS

	X-BAND SWITCH TYPE I	BASEBAND DEVICE TYPE II	IMPROVED BASE-BAND DEVICE TYPE II
BANDWIDTH	8 GHz	200–1.2 GHz	500 MHz
COUPLING	AC	DC	DC
ISOLATION-SWITCH	20 dB	20–30 dB	30 dB
INSERTION LOSS SWITCH	1–1.5 dB	~.3 dB	<1.0 dB
SWITCHING TIME	~500 NS	1 μS	<10 NS
"T" SWITCH ISOLATION	<40 dB	>40 dB	>60 dB
INSERTION LOSS	1.5–2.5 dB	<.6 dB	<1 dB
SWITCHING CONTROL POWER	<10 μW	<10 μW	<10 μW

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CONTROL LOGIC SEMICONDUCTOR REQUIREMENTS

- All switch decode logics on same chip as signal switch
- Switch drivers to be part of decode logic where applicable
- Control logic memory buffers also part of switch chip
- GaAs logic shall use:
  - Shottky diode FET logic (SDFL)
  - D-MESFET devices using selective implantation
- C-MOS-SOS logic
  - 2 μm enhancement mode silicon on sapphire (SOS)

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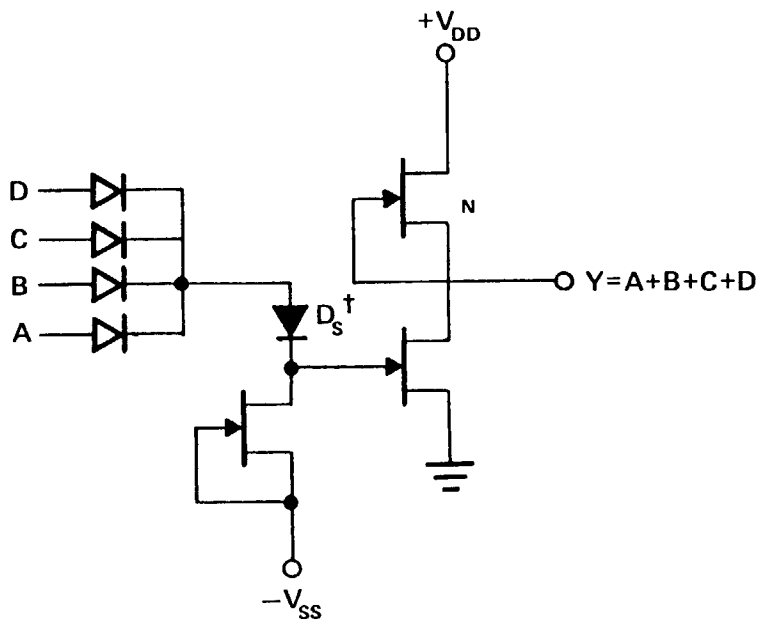
SDFL D-MESFET NOR GATE



† OPTIONAL: D_S, A HIGH CONDUCTANCE SHOTTKY BARRIER VOLTAGE SHIFT DIODE, IS NOT REQUIRED FOR VERY LOW VOLTAGE CIRCUITS USING LOW V_{PE} GaAs FET's.

ALL GaAs FET's AND ACTIVE LOADS ARE DEPLETION MODE (NORMALLY –ON) SHOTTKY GATE TYPES

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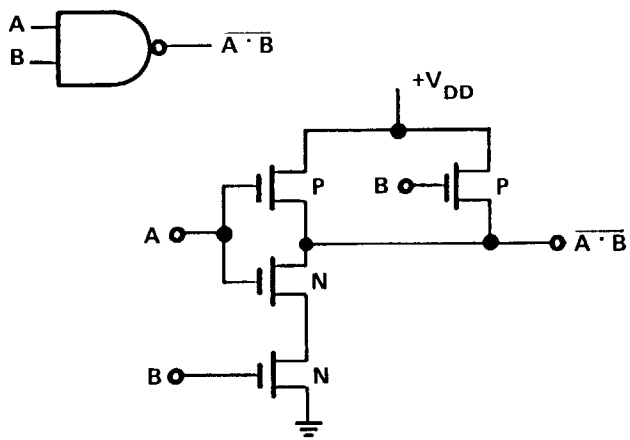
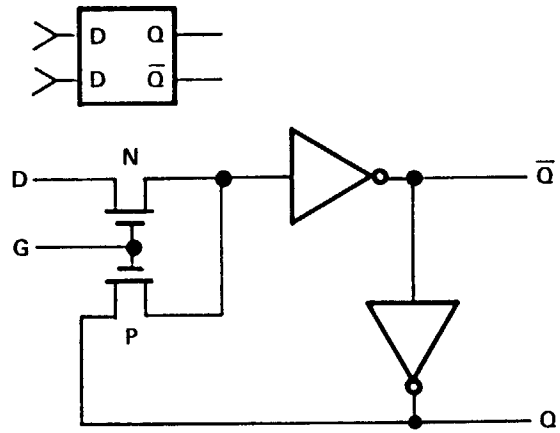
C-MOS-SOS LOGIC

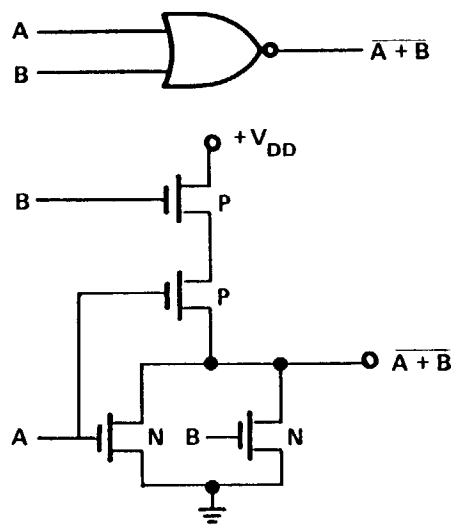
A) TWO INPUT NAND GATE



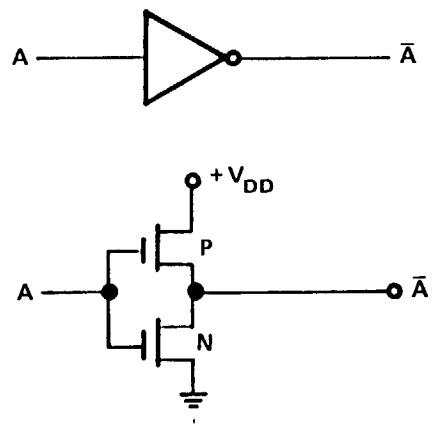
B) GATED LATCH



C) TWO INPUT NOR GATE



D) INVERTER GATE



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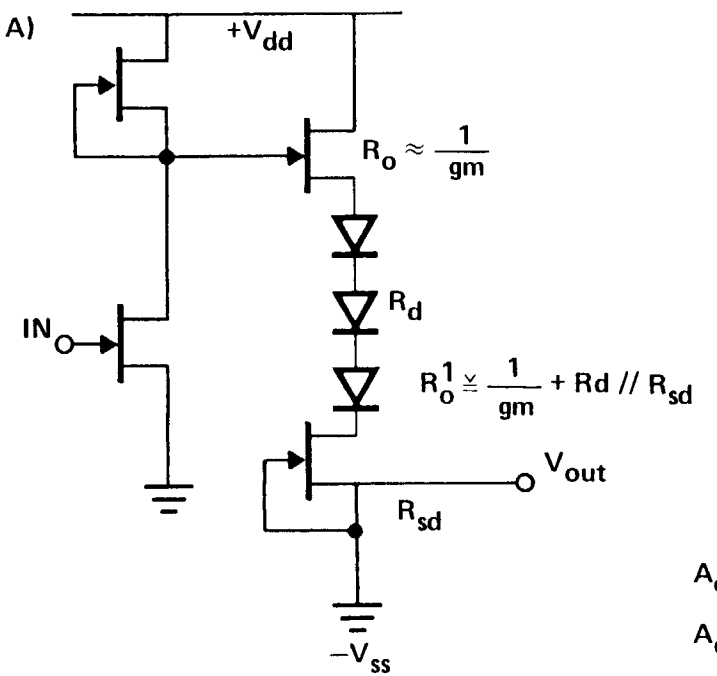
NXN CROSS-BAR SIGNAL AMPLIFIER REQUIREMENTS

- Fixed gain amplifier (+6dB) designed as part of output signal buss
- Unity gain buffer chip. Designed as separate buffer chip for input cross-bar signals
- GaAs designs uses N-channel J-FET on GaAs (1μm gates)
- CMOS-SOS using single poly-single match depletion load devices with $<\mu$m gate

FET AMPLIFIER ON GaAs

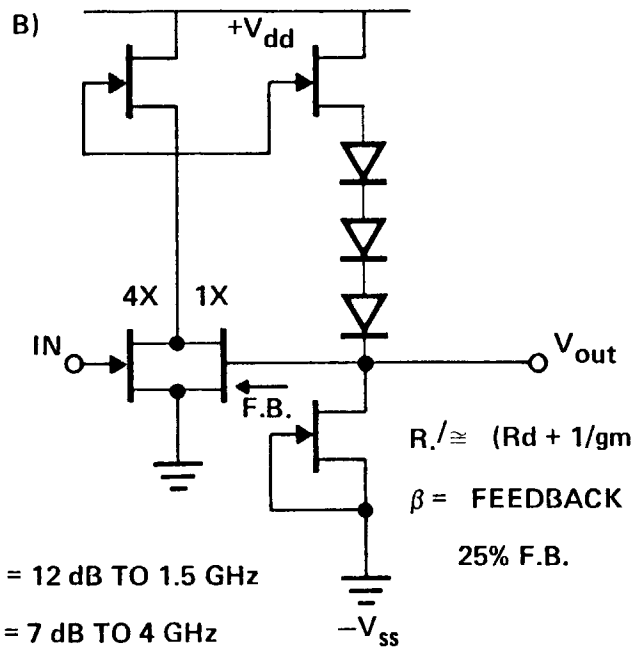
COMMON SOURCE WITH
LEVEL SHIFT, BUFFER

A)



COMMON SOURCE WITH
FEEDBACK

B)



$R_o' \cong (Rd + 1/gm \;//R_{sd}/\beta$

$\beta =$ FEEDBACK GAIN

25% F.B.

A_{ol} = 12 dB TO 1.5 GHz

A_{cl} = 7 dB TO 4 GHz

$\beta = \log^{-1}\left(\frac{A_{ol}-A_{cl}}{10}\right)$

$\beta = 3.16$

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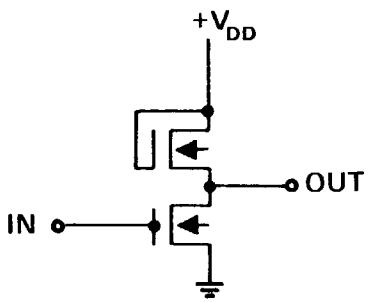
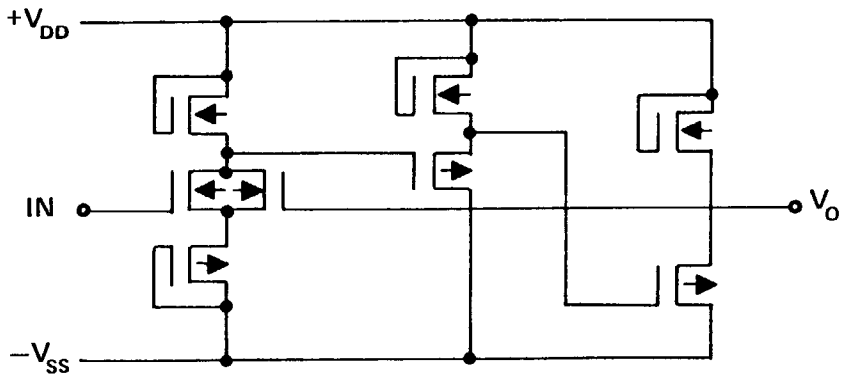
POSSIBLE MOS AMPLIFIER CONFIGURATION

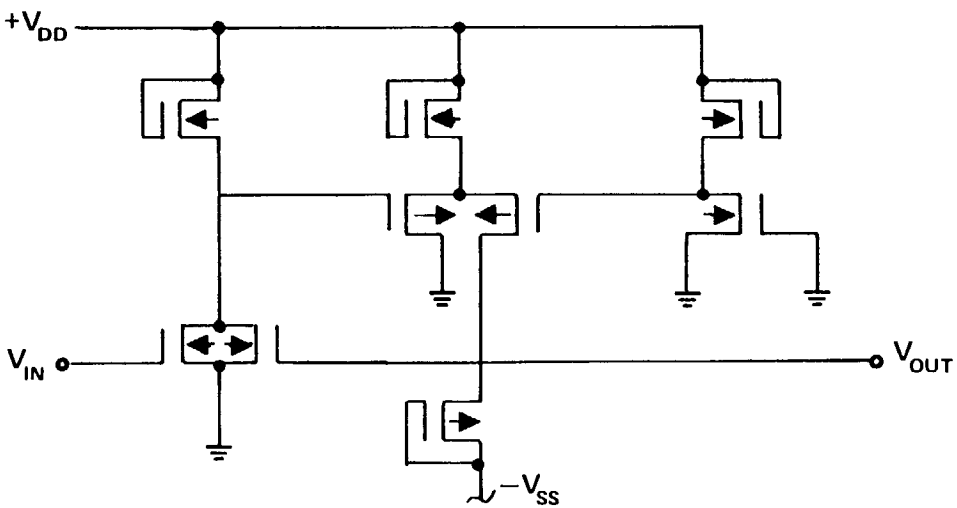
A) COMMON SOURCE



B) COMMON DRAIN–COMMON SOURCE WITH FEEDBACK



C) COMMON SOURCE–DIFFERENTIAL P CHANNEL LEVEL SHIFTER AND FEEDBACK



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TECHNOLOGY SUMMARY CHART SEMICONDUCTORS

TECHNOLOGY	BANDWIDTH	INSERTION LOSS 50Ω/100Ω	SWITCHING TIME	POWER DISSIPATION	AVAILABILITY
• GaAs					
• FET SWITCH	1 GHz	1.34 dB/–	<10 NS	<50 mW	1982
• LOGIC	2 GHz	–	<1 NS	<1 mW	1981
• AMPLIFIER	>1 GHz	–	–	10 mW	1981
• SWITCH DRIVER	>1 GHz	–	<10 NS	10 mW	1981
• C-M05-505					
• TRANSMISSION GATE SWITCH	<500 MHz	3 dB/1.8 dB	10 NS	–	1981
• RESISTANCE GATE SWITCH	600 MHz	1 dB/.7 dB	10 NS	–	1982
• C-MOS LOGIC	<200 MBS	–	1 NS	1 mW	1980
• AMPLIFIER	400 MHz	–	–	10 mW	1982
• SWITCH DRIVER	100 MHz	–	<3 NS	< 1 mW	1980

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PARAMETERS CHARACTERISTICS OF OTHER SEMICONDUCTOR DEVICES

DEVICE	DEVICE PASS BANDWIDTH	LOGIC SW. TIME	DEVICE POWER DISP.	SYSTEM PWR. 6 K SW.	MEETS SYSTEM CAPABILITY GOALS
• BI POLAR					
T^2L	–	10–20 NS	15–20 mW	~160 WT	VERY LOW
ECL	–	1.0–2 NS	5–15 mW	>10 KW	VERY LOW
DIODE SWITCH	>1 GHz	~1 NS	–	~500 W	LOW
SWITCH AMP.	~300 MHz	~10–15 NS	50–100 mW	~600 W	LOW
• BULK MOS					
C-MOS	<100 MHz	~20 NS	20 μW SWITCHES	<50 WT	VERY LOW
N-CHANNEL	<300 MHz	~6 NS	~2 mW/CONT.	>160 WTS	LOW

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NXN NONBLOCKING CROSS BAR

One Level Design

- Block diagram
- Subswitch design
- Mechanical layout

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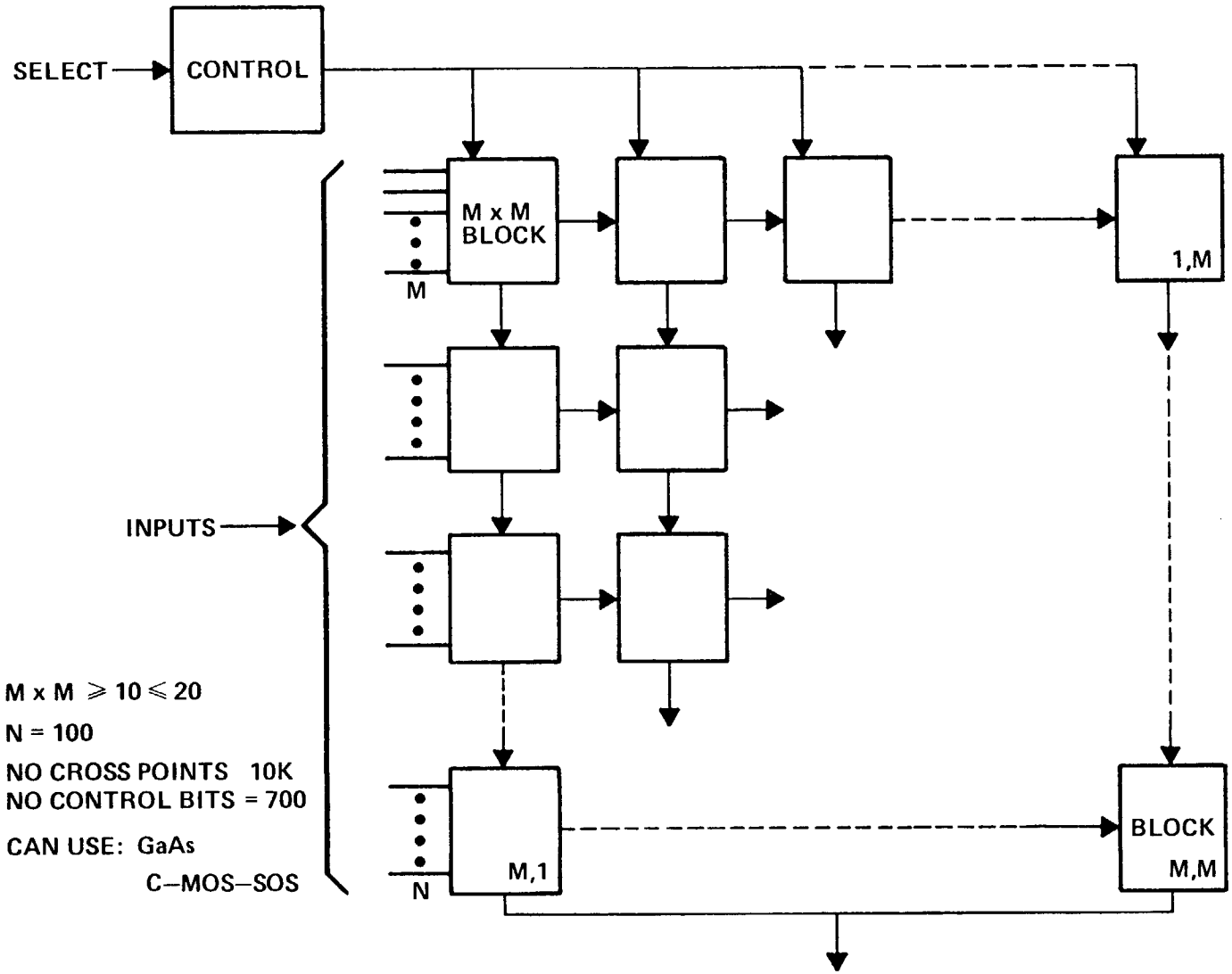
NXN SWITCH MATRIX 1 LEVEL



M x M ⩾ 10 ⩽ 20

N = 100

NO CROSS POINTS 10K
NO CONTROL BITS = 700

CAN USE: GaAs
C–MOS–SOS

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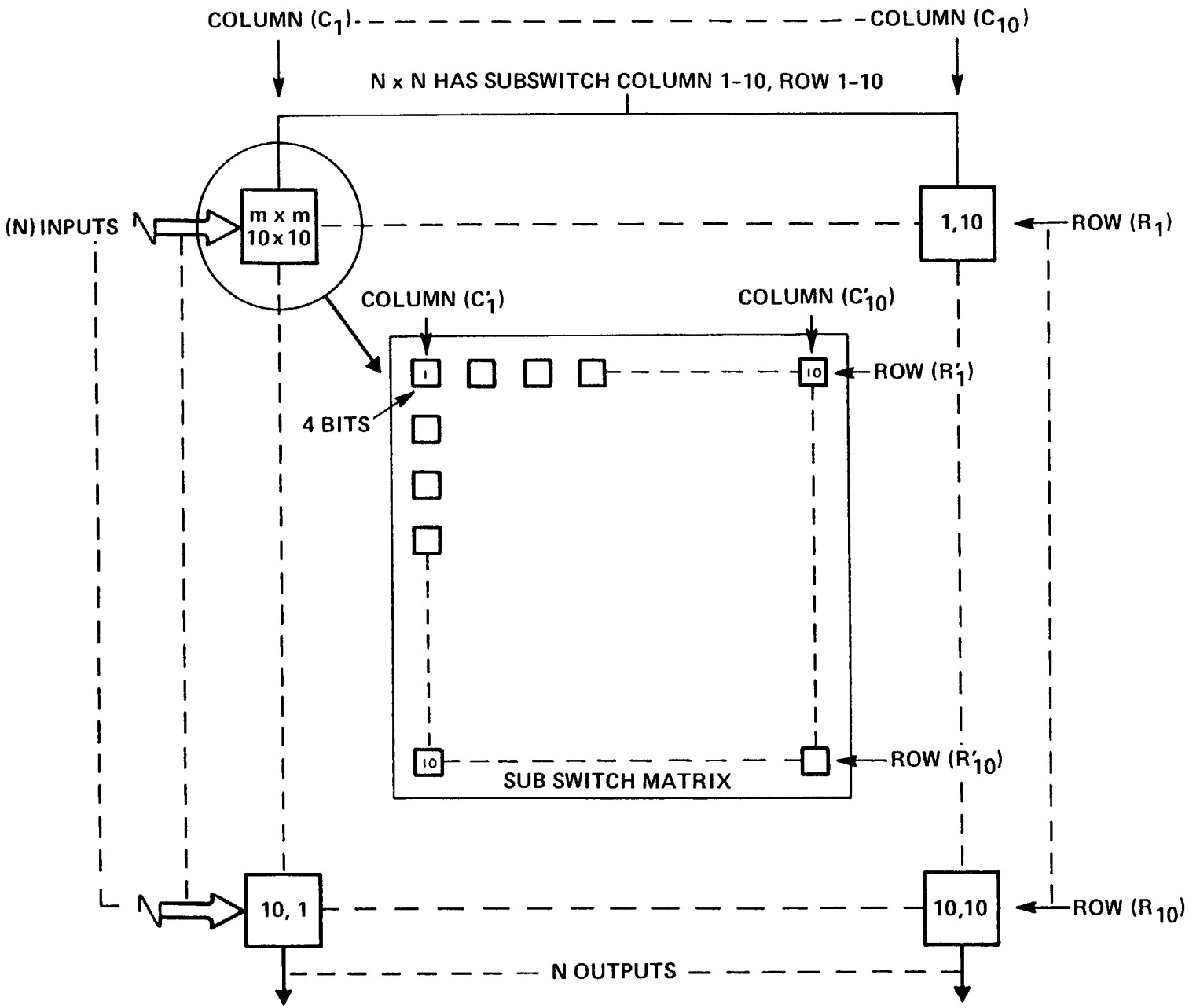
CONTROL BIT REQUIREMENTS FOR NXN CROSS BAR



BASIC MXM SUB-SWITCH

- Semiconductor technology

  - C-MOS-SOS
  - GaAs

- Subswitch size

  (m x m) where m = 10 for one level design

  (p x q) where p = 10, q = 20
  (q x p) where q = 10, p = 20
  (l x l) where l = 10

  } for three level design

- On-chip transmission line characteristics

  C-MOS-SOS - Z_o = 150 ohms
  GaAs - Z_o = 100 ohms

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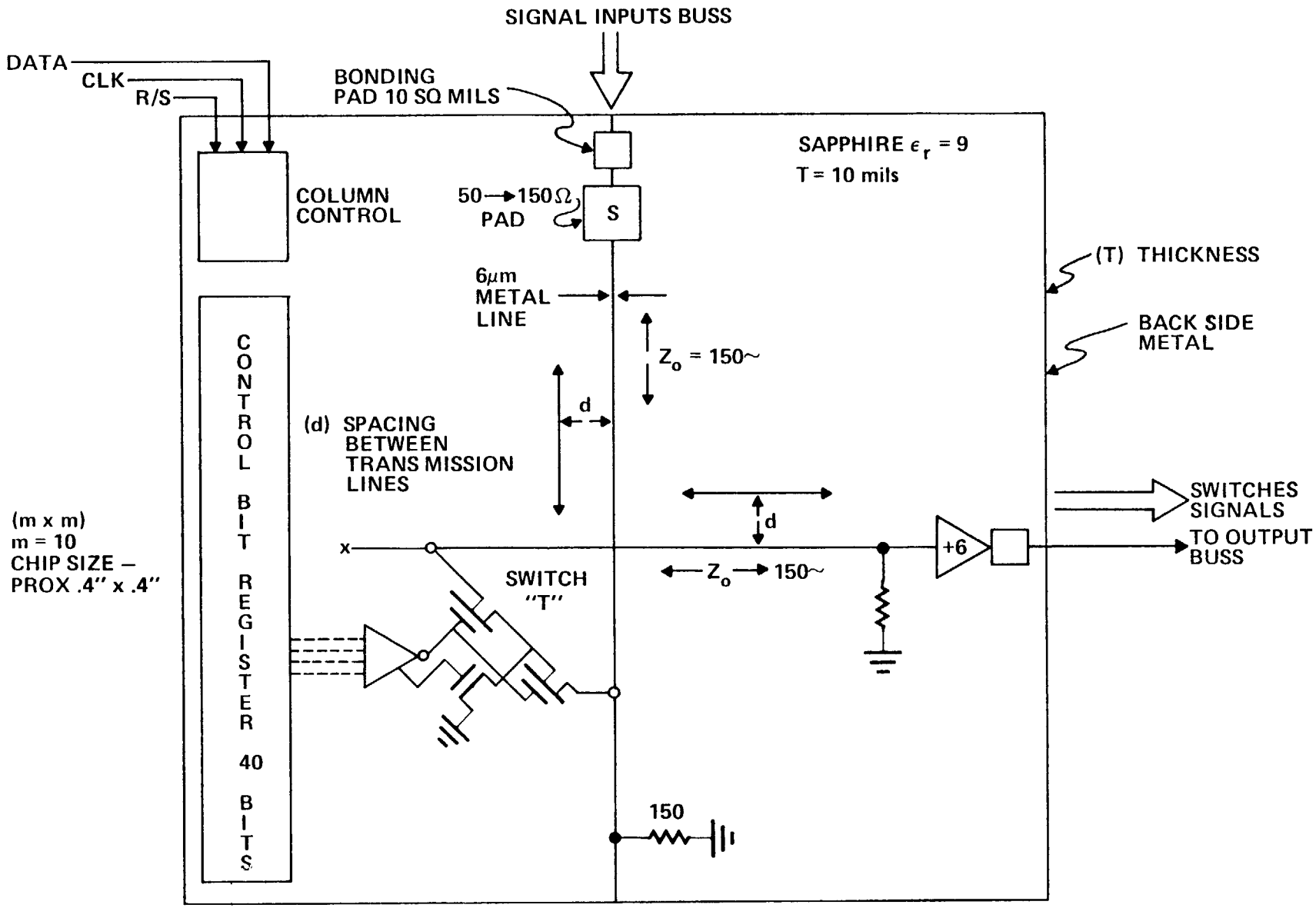
C-MOS-SOS SUBSWITCH MATRIX



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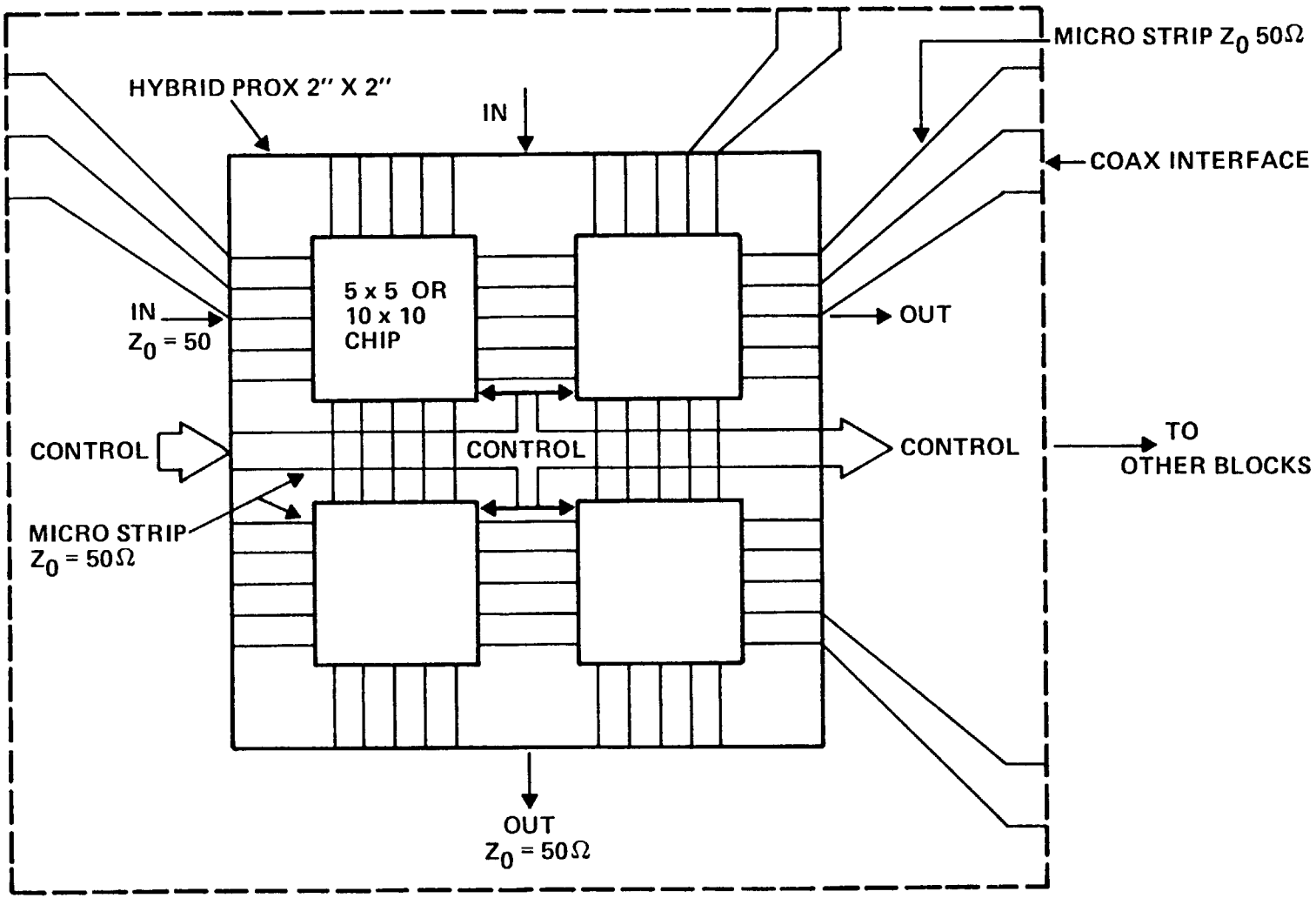
TYPICAL SWITCH PACKAGING FOR SUBSWITCH BLOCKS PXG, MXM



NOTE: SUB SWITCH BUILDING BLOCK

- MICRO STRIP, INTERCONNECT
- VARIABLE MATRIX SIZE
- ANY OF THE SEMICONDUCTOR TECHNOLOGIES

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CHARACTERISTICS OF C-MOS-SOS CHIP

- LINE WIDTH 6 μM
- SUBSTRATE THICKNESS 10 MIL

$Z_0 = 150\Omega$

- LINES SEPARATION >50:1

CO CHANNEL ISOLATION >55 dB/CM

- CROSSOVER SEPARATION 1 μM
  FC = .5 X 10^9 Hz

$X_{CX} \sim 220\ K\Omega$,
ISOLATION >28 dB RMS
>32 dB X-OVER

- RESISTANCE GATE SWITCH ISOLATION > 40 dB
  "T" SWITCH CONFIGURATION > 60 dB
- SWITCH INSERTION LOSS < 2 dB
- AMPLIFIER GAIN +6 dB
- AMPLIFIER CONFIGURATION

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CHARACTERISTICS OF GaAs CHIP

- LINE WIDTH 25 μM
- SUBSTRATE THICKNESS 250 μM } $Z_0 = 100\Omega$
- $\epsilon_r = 12.7$
- CROSSOVER SEPARATION 250 μM } X_c = 12 megohms
  F_o = 500 MHz
- CROSSOVER ISOLATION > 40 dB
  RMS 10 CROSSOVERS > 35 dB
- MESFET SWITCH ISOLATION > 60 dB
  "T" CONFIGURATION
- SWITCH INSERTION LOSS < 1.2 dB
- AMPLIFIER GAIN +3 dB
- AMPLIFIER CONFIGURATION

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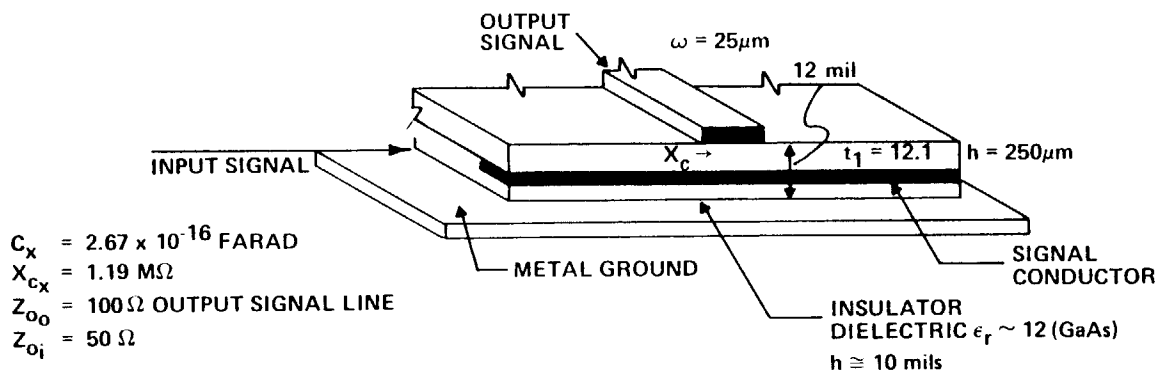
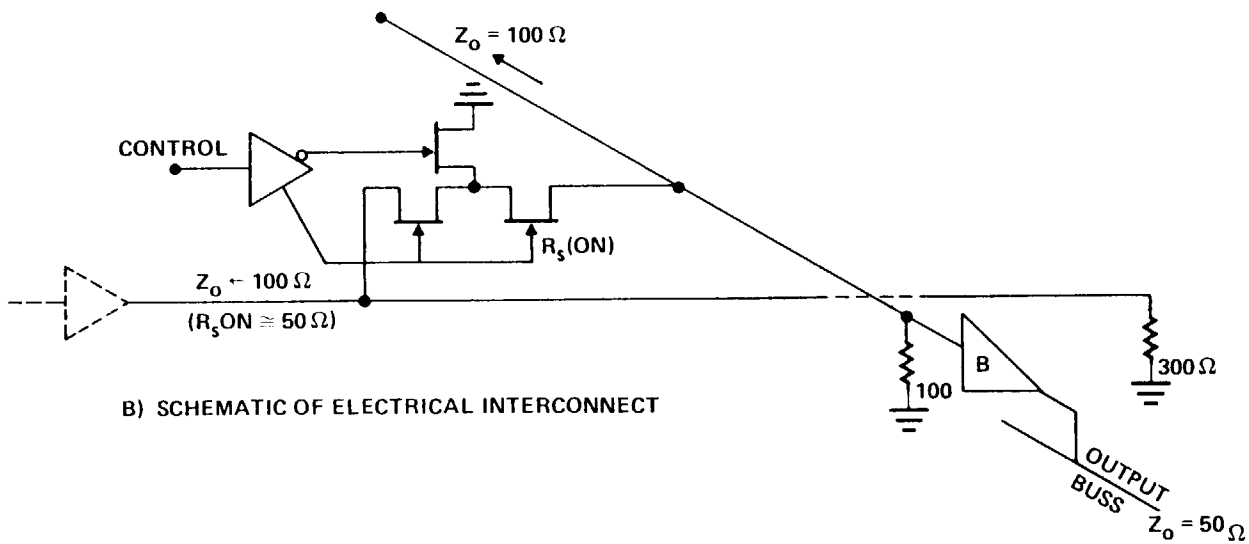
GaAs MXM SUBSWITCH DESIGN FOR MINIMUM CROSS TALK

A) CROSS SECTION OF CHIP



C_x = 2.67 x 10^{-16} FARAD
X_{C_x} = 1.19 MΩ
Z_{oo} = 100 Ω OUTPUT SIGNAL LINE
Z_{oi} = 50 Ω



B) SCHEMATIC OF ELECTRICAL INTERCONNECT

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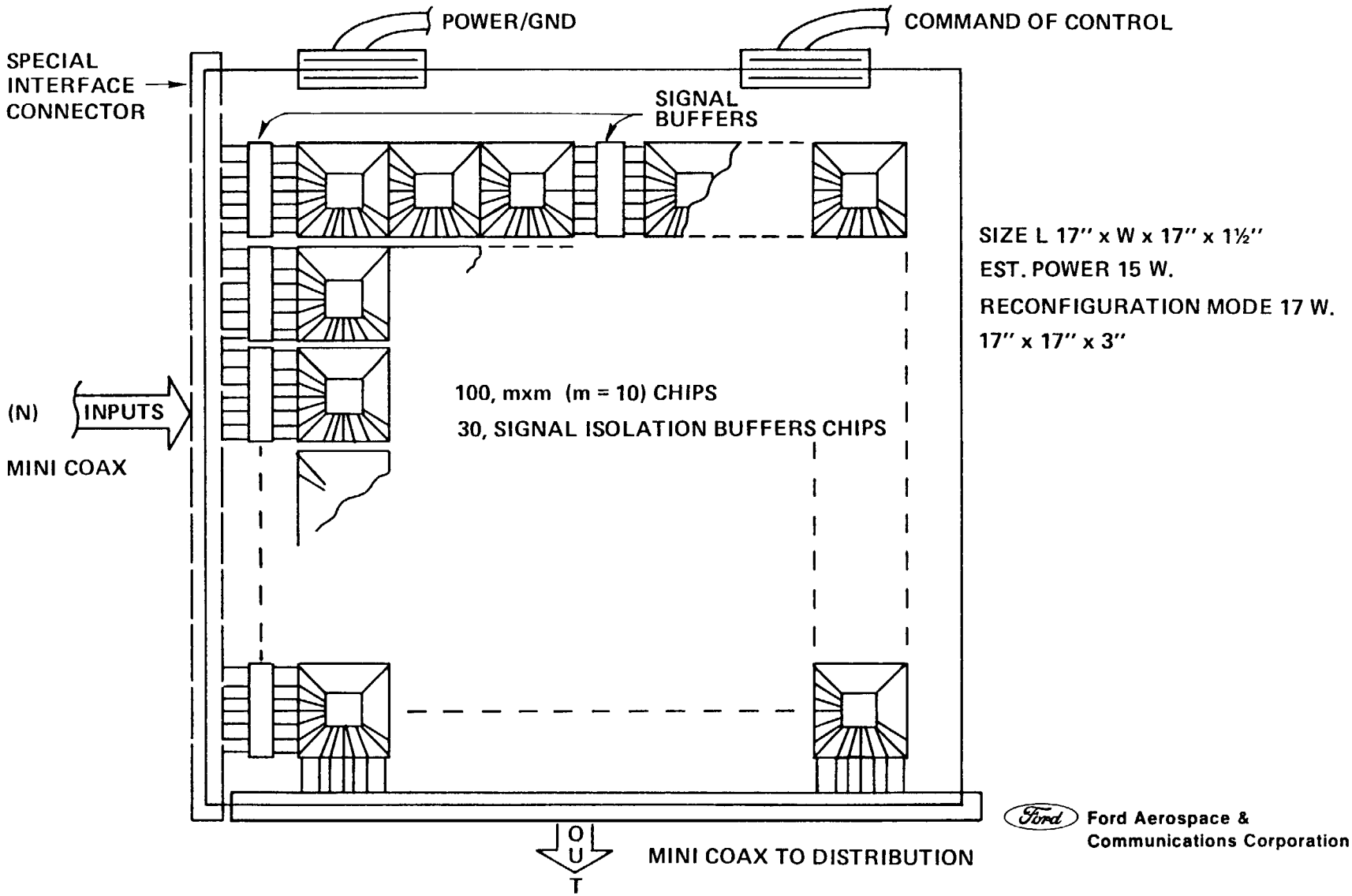
NXN MATRIX LAYOUT USING C-MOS-SOS CHIPS AND CARRIERS



NXN NONBLOCKING CROSS BAR

Three Level Design

- Block diagram
- Subswitch design
- Mechanical layout

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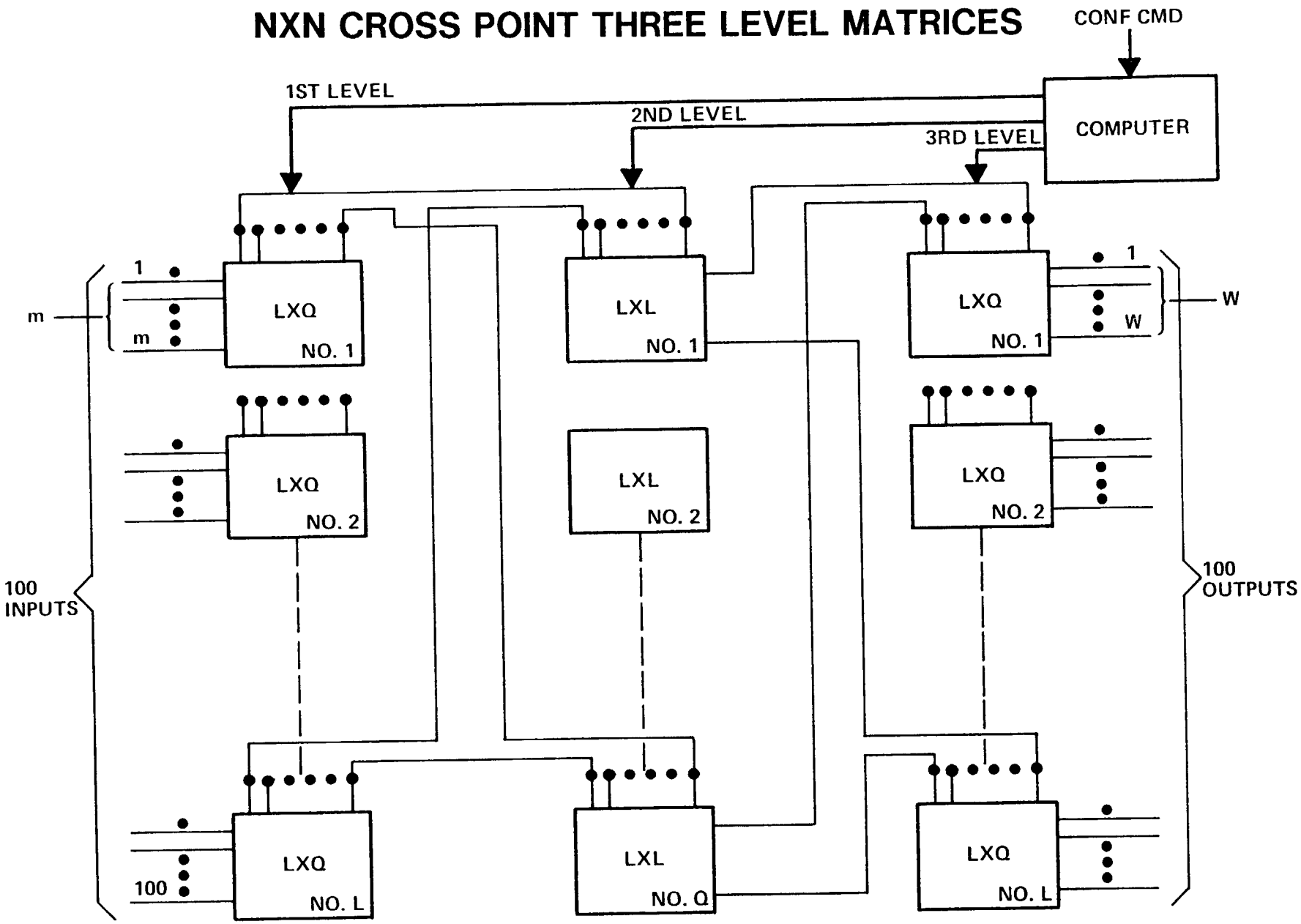
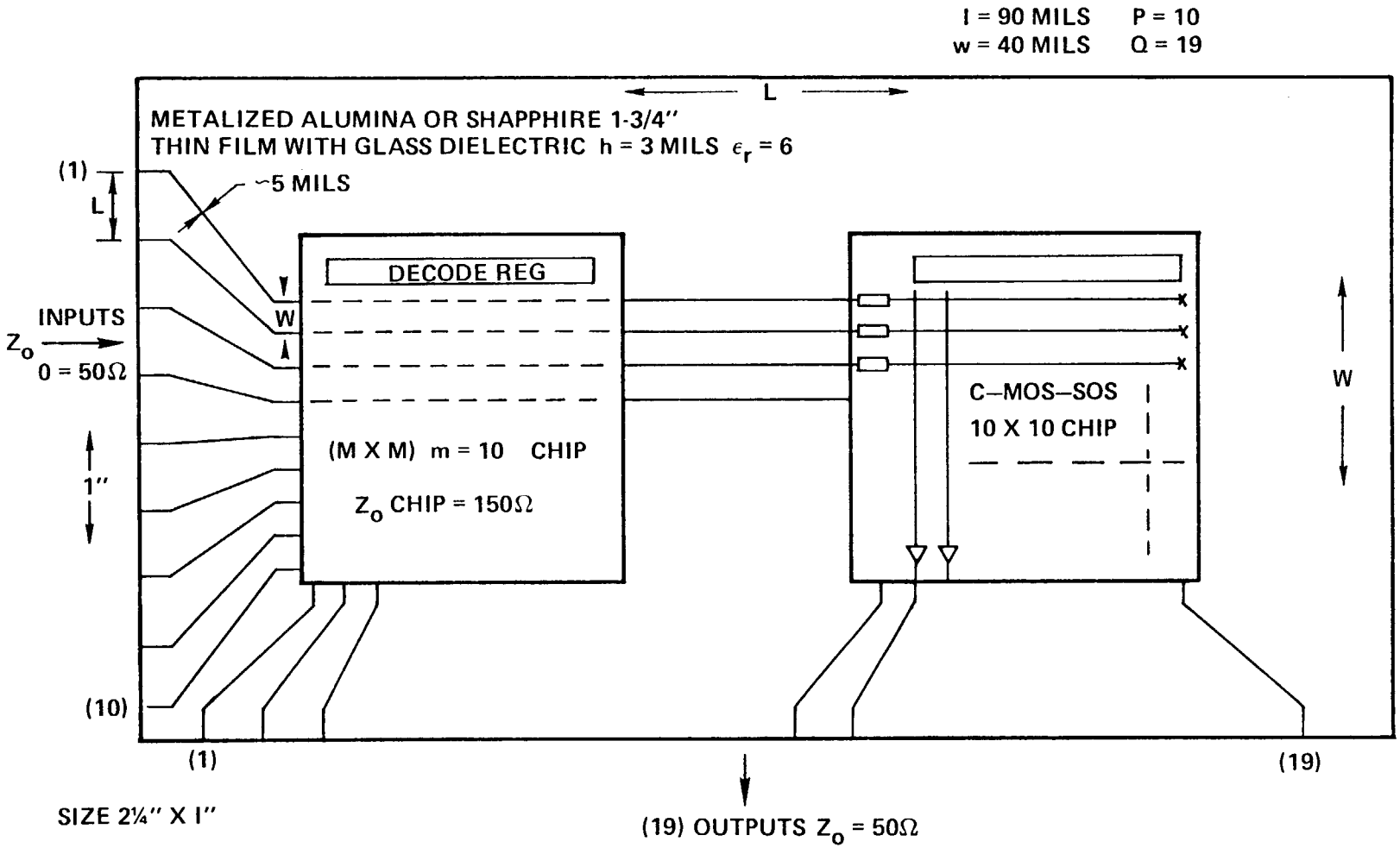
NXN CROSS POINT THREE LEVEL MATRICES



- NO. CROSS POINTS = 5,700
- L = 10, Q = 19
- 20 (LXQ) BLOCKS
- 19, LXL BLOCKS
- 1800 CONTROL BIT REQUIRED

(PxQ) SWITCH FOR THREE LEVEL CROSS BAR



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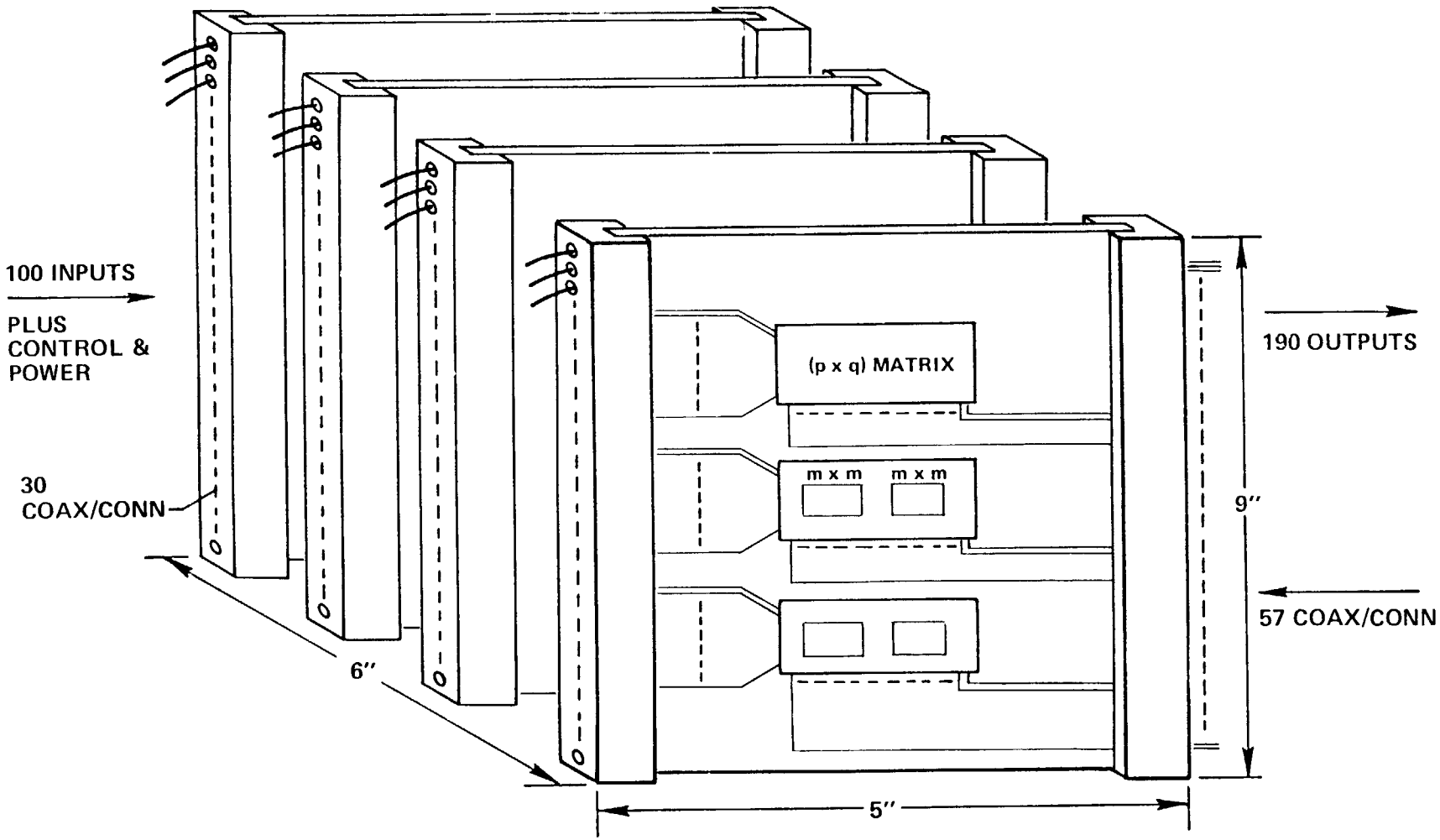
INPUT (P X Q) FIRST LEVEL SWITCH



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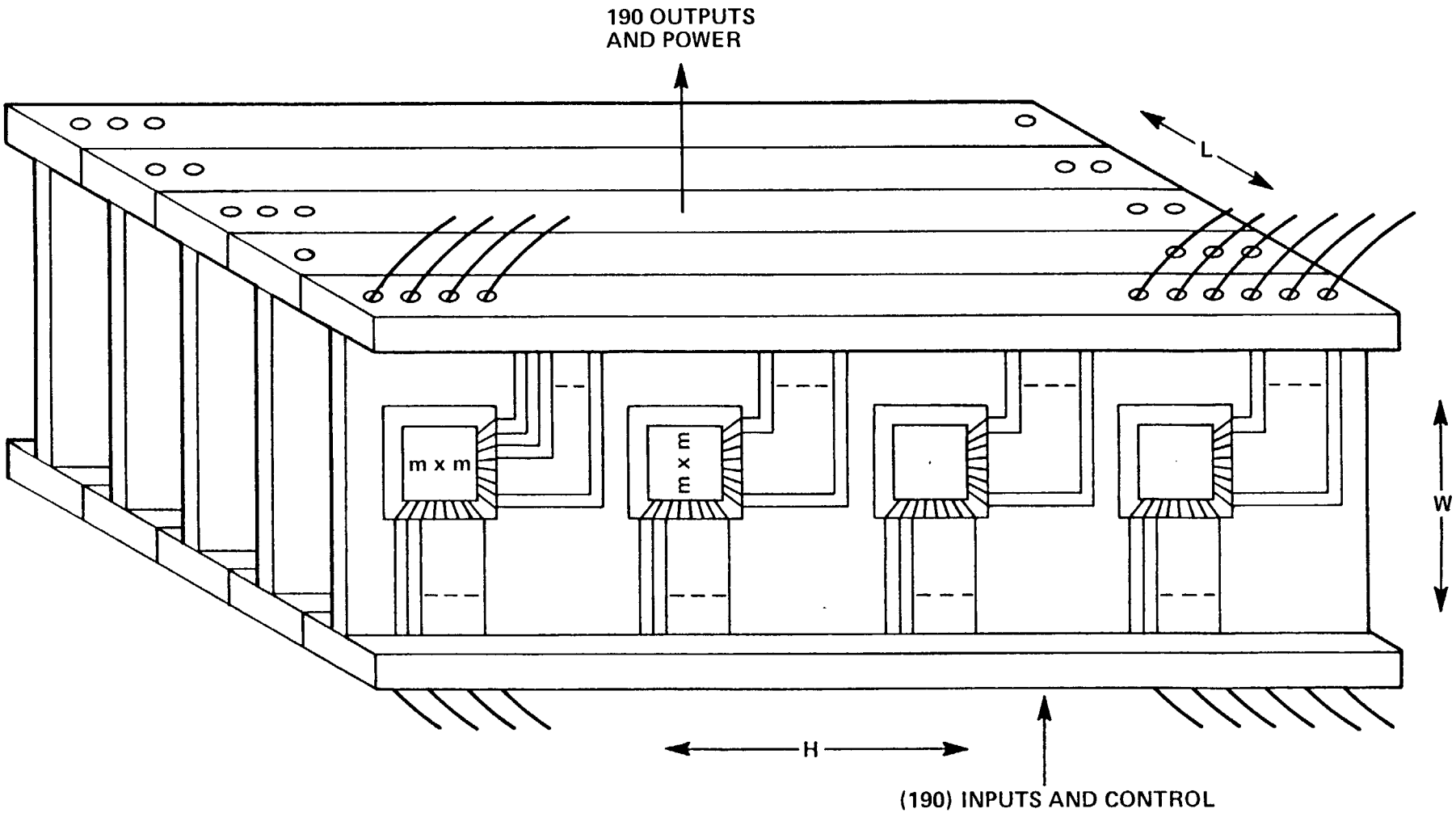
L X L SUBMATRIX (SECOND LEVEL SWITCH)



9"H X 3"W X 5"L

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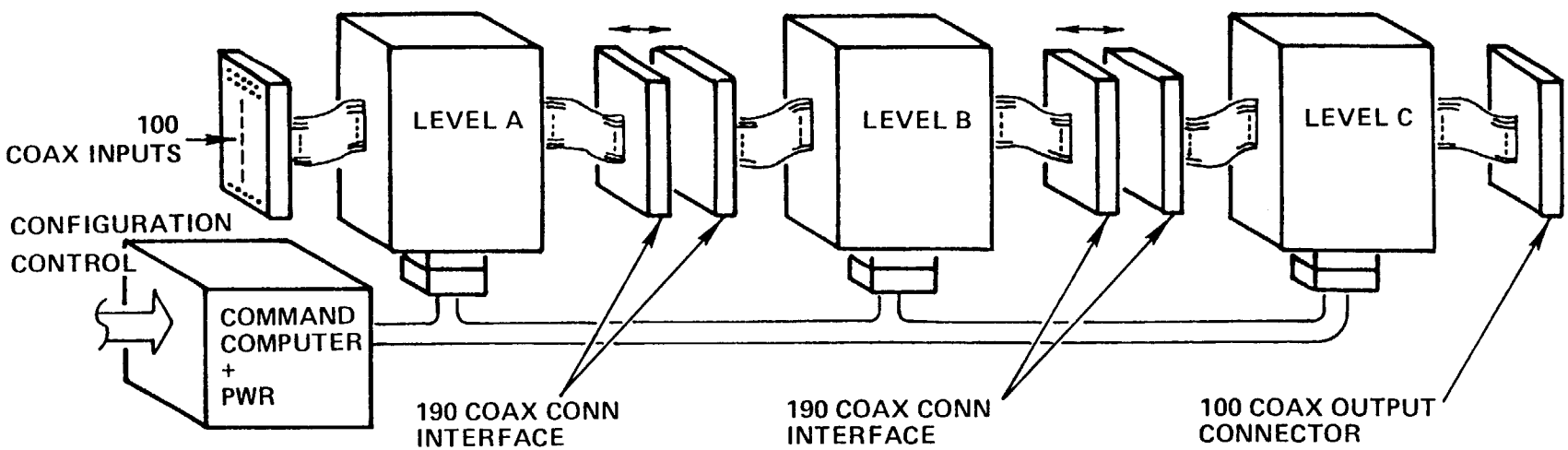
THREE-LEVEL SWITCH AS SEPARATE SWITCH MODULES



PROX SIZE PER MODULE 12" X 8" X 8"
SPECIAL MINT COAX WIDE BAND INTERFACE
REQUIRE 700 WIDE BAND COAX INTERFACES

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N X N CROSS BAR CHARACTERISTICS N=100

FEATURE	ONE LEVEL DESIGN		THREE LEVEL DESIGN	
	C-MOS-SOS	GaAs	C-MOS-SOS	GaAs
SIZE	17" X 17" X 3"	17" X 17" X 4"	12" X 15" X 9"	12" X 15" X 12"
WEIGHT	PROX 20 LBS	PROX 20 LBS	PROX 80 LBS	PROX 90 LBS
POWER	17 WATTS	PROX 100–120 W	PROX 17 WATTS	60–70 WATTS
INSERTION LOSS	<6 dB	<6 dB	<6 dB	<6 dB
ISOLATION	PROX 28 dB RMS	PROX 36 dB RMS	PROX 28 dB RMS	PROX 36 dB RMS
COMPLEXITY				
M X M CHIP	LOW	HIGH	LOW	HIGH
INTERCONNECT	LOW	LOW	HIGH	HIGH
CONTROL	LOW	LOW	MEDIUM	MEDIUM
REPAIRABILITY (1-10)	5	4	7	6
RELIABILITY (1-10)	5	3	6	5
COST TO DEVELOP (1-10)	4	6	5	7

(1) LOW

(10) HIGH

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SUMMARY MAJOR CONSIDERATION FOR N X N SWITCH MATRIX

CONSIDERATION	SUB SWITCH CHIP		CROSS BAR	
	GaAs	C-MOS	ONE LEVEL	THREE LEVEL
SIGNAL INTERFACES	~20	~20	200	200
INTERCONNECTS	–	–	3600	570
INTERCONNECT TYPE	MICRO-STRIP	MICRO-STRIP	MICRO-STRIP	COAX-OPTICAL
ISOLATION INTERCONNECTS	–	–	GOOD	GOOD
SUB SWITCH SIZE	.5 IN. SQ.	.5 IN. SQ.	1.0 X 1.0 IN.	2-1/4 IN X 1 IN.
POWER DISSIPATION	~1 WATT	~100 MW	–	–
POWER ROUTING	–	–	GOOD	GOOD
ISOLATION	FAIR	POOR	POOR	POOR
MULTI INTERCONNECT	–	–	GOOD	POOR
CONTROL BITS	–	–	700	1760
CONTROL INTERFACES	–	–	10	39
SIGNAL INTERCONNECT ALGORITHM	–	–	SIMPLE	COMPLEX

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BASEBAND SWITCH CONCLUSIONS

REQUIREMENT	GOAL	CONCLUSIONS	YEAR TECHNOLOGY MATURE
SWITCH SIZE N X N	100 X 100	ACHIEVABLE	1984
RECONFIGURATION RATE	<2 MS	<2 MS	1982
SWITCH TIME	<10 NS	<10 NS	1982
INSERTION LOSS	<15 dB	<10 dB	1982
ISOLATION	<40 dB	PROXIMATELY 40 dB	1982
ANALOG IF BANDWIDTH	25–500 MHz	25–500 MHz	1982
DIGITAL BIT RATE	25–500 MBS	25–500 MHz	1982
SIGNAL LEVEL	–10 THRU –50 dBm	–10 THRU –50 dBm	1982
VSWR	<1.2:1 50 Ω	NOT POSSIBLE TO MEET ~1.5:1	1984

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TASK III BREADBOARD DEVELOPMENT OF CRITICAL SWITCH TECHNOLOGY

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COUPLER DEVELOPMENT

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COUPLER DESIGN REQUIREMENT

- Broad bandwidth
- Low insertion loss
- Low VSWR
- Good isolation

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LARGE INTERDIGITATED COUPLER

- Calculate even and odd mode impedances using in-house computer program
- Find microstrip linewidth (w) and line spacing (s) using Paolino's table (Microwaves, May 1976)
- Perform coupler analysis using "COMPACT" Computer Analysis Program

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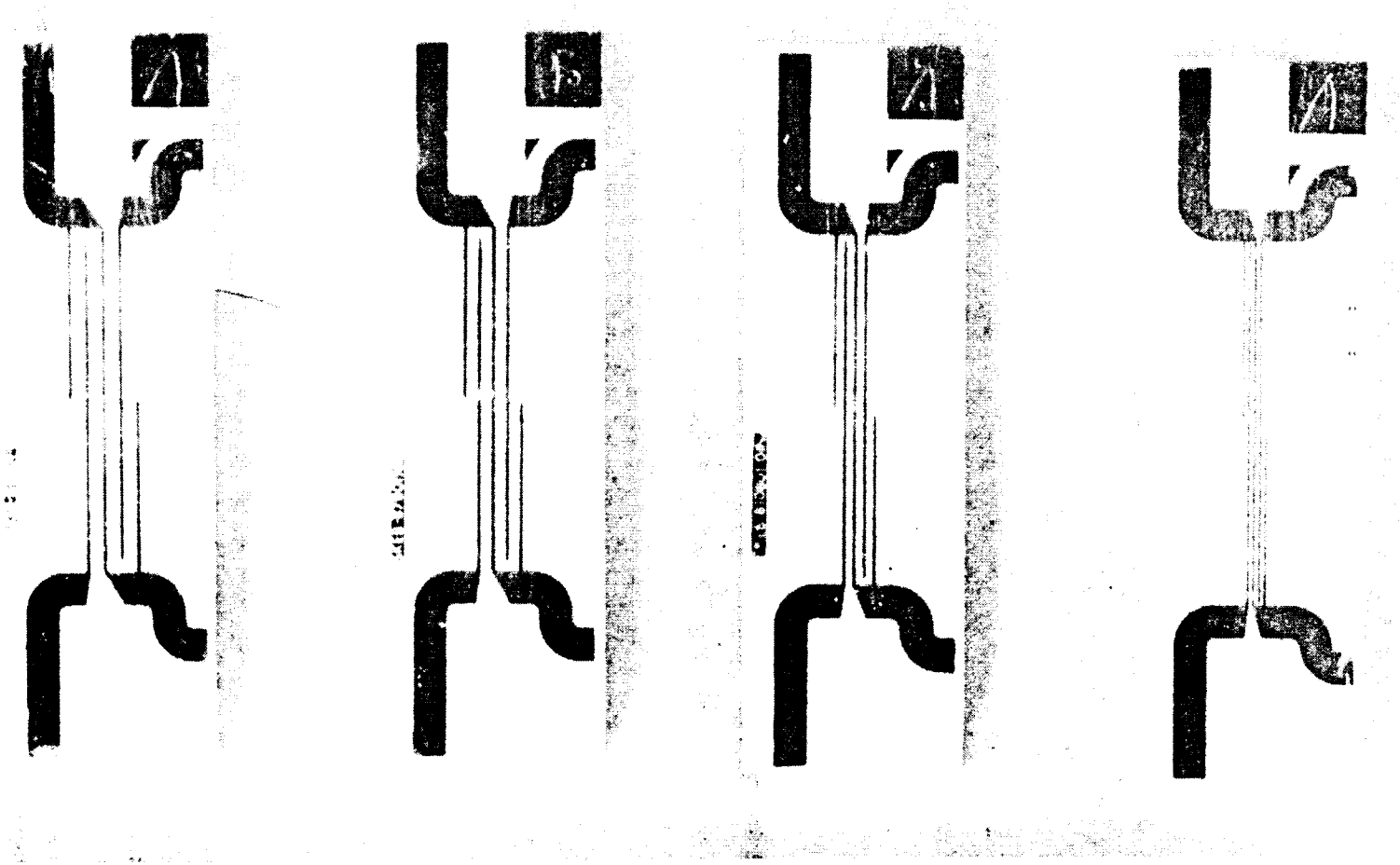
BREADBOARD COUPLER DESIGN

COUPLER (dB)	WIDTH (MILS)	SPACING (MILS)	LENGTH (MILS)
3	2.45	1.5	250
4.7	2.8	4.15	240
6	3.5	6.2	235
7	3.3	8.2	235

*USING 25 MIL THICK ALUMINA SUBSTRATE WITH Cr-Cu-Au METALIZATION.

INTERDIGITATED COUPLERS FOR THE MICROWAVE SWITCH MATRIX



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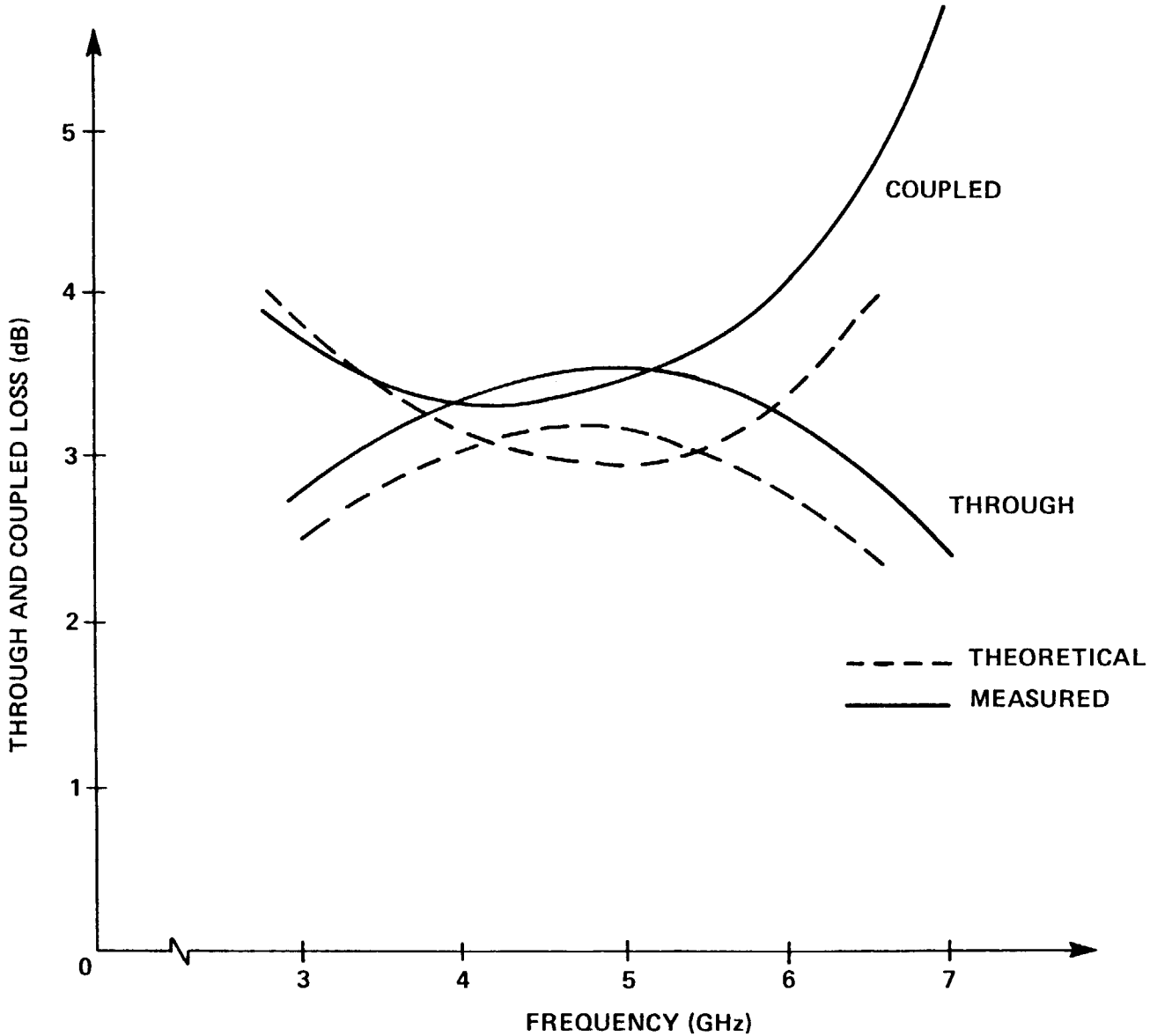
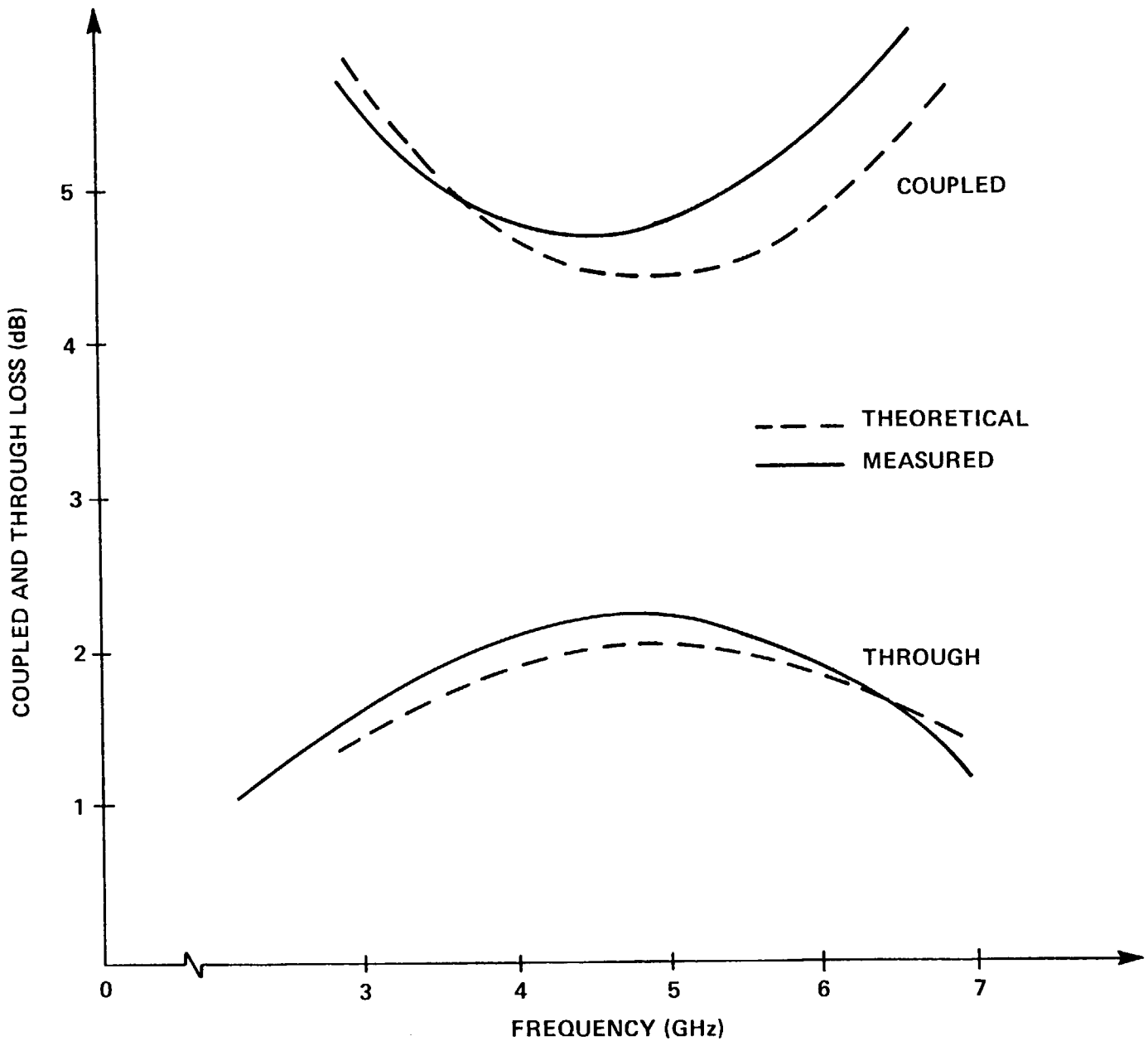
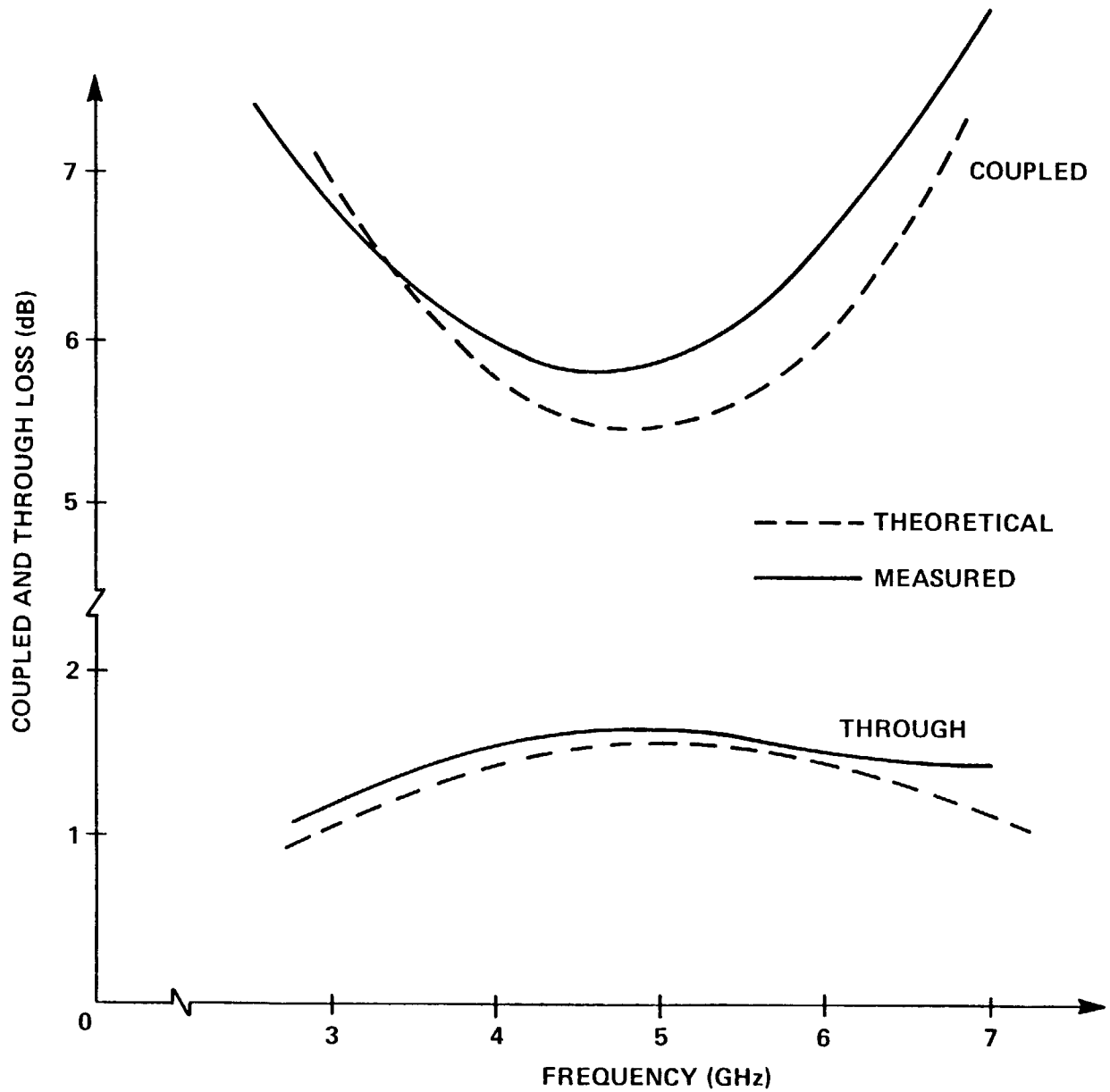
PERFORMANCE OF 3 dB INTERDIGITATED COUPLER



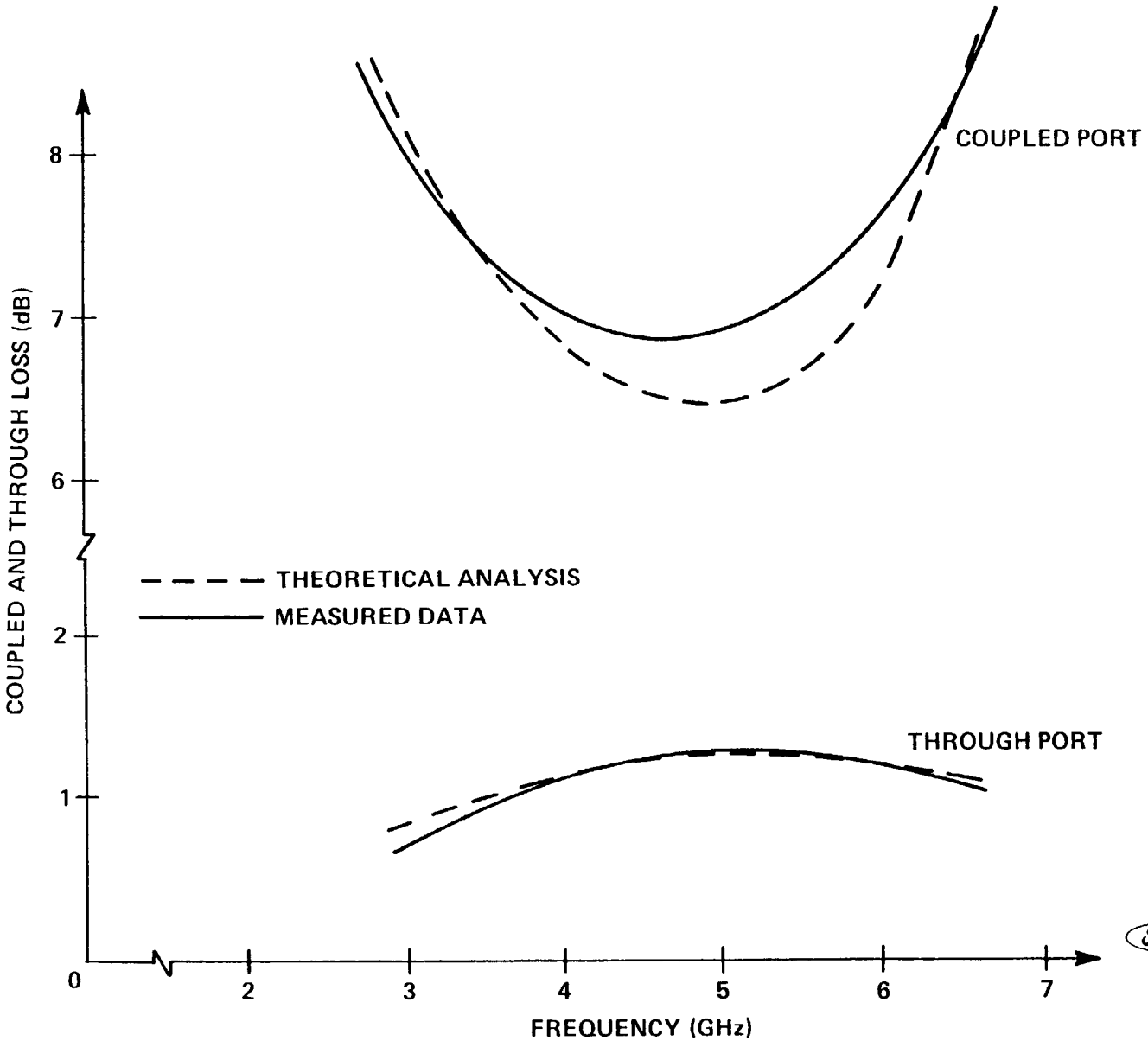
PERFORMANCE OF 4.77 dB INTERDIGITATED COUPLER



PERFORMANCE OF 6 dB INTERDIGITATED COUPLER



PERFORMANCE OF THE 7dB INTERDIGITATED COUPLER



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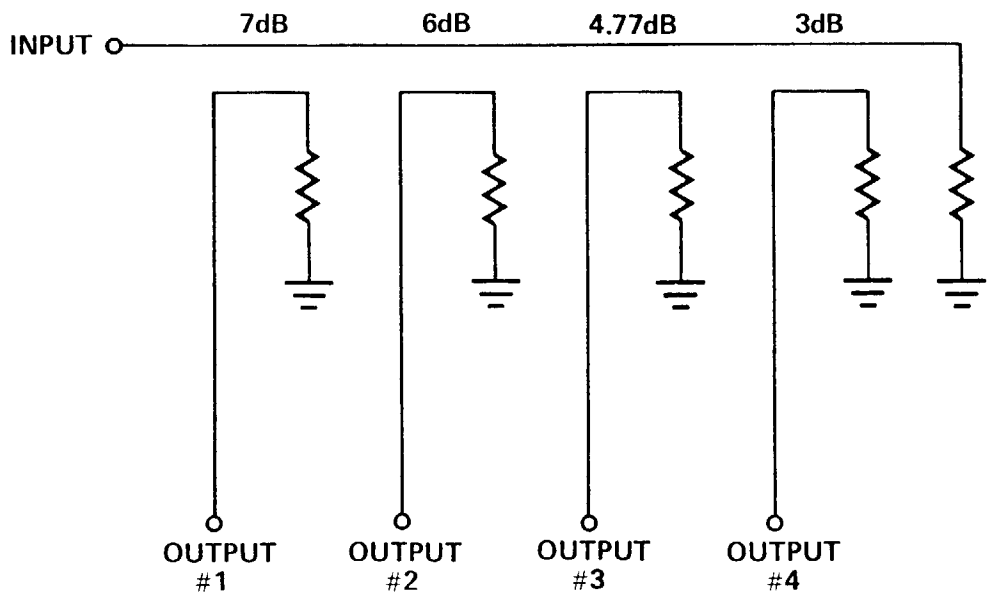
CASCADED COUPLER PERFORMANCE



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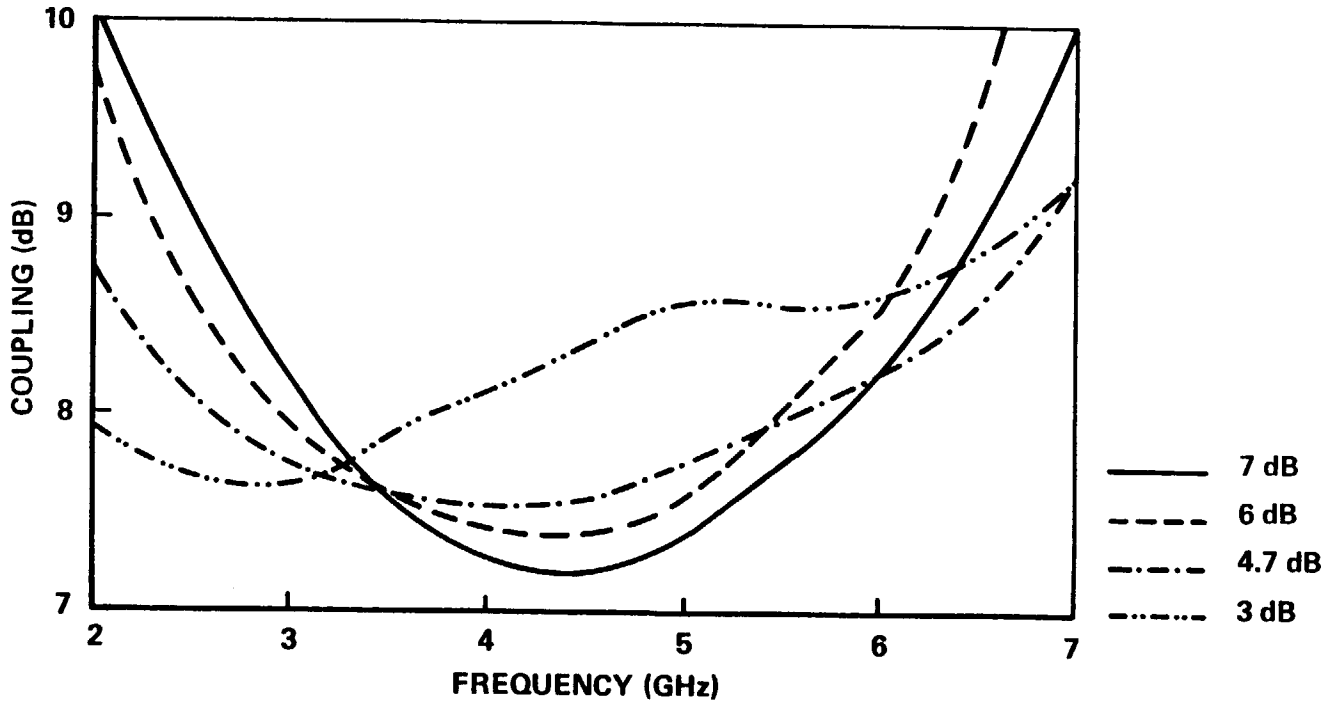
CASCADED COUPLER



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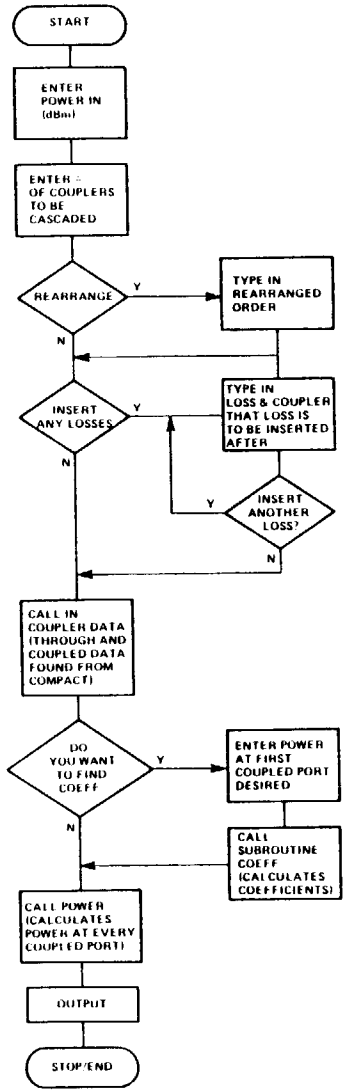
COMPUTER PROGRAM FOR CIRCUIT ANALYSIS OF CASCADE COUPLERS



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SWITCH AMPLIFIER DEVELOPMENT

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Communications Corporation

DEVICE SELECTION

- Characterization of different Dual Gate Fet Transistors
- Comparison of device electrical performance
- Device reliability and assembly tradeoffs

AMPLIFIER DESIGN GOALS

• Bandwidth	3.5-6.0 GHz
• Gain	20 dB nominal
• Isolation	50 dB minimum
• Gain Ripple	less than 1 dB
• Switching Time	less than 10 nsec

- Stable operation
- Insensitivity to component parameter changes

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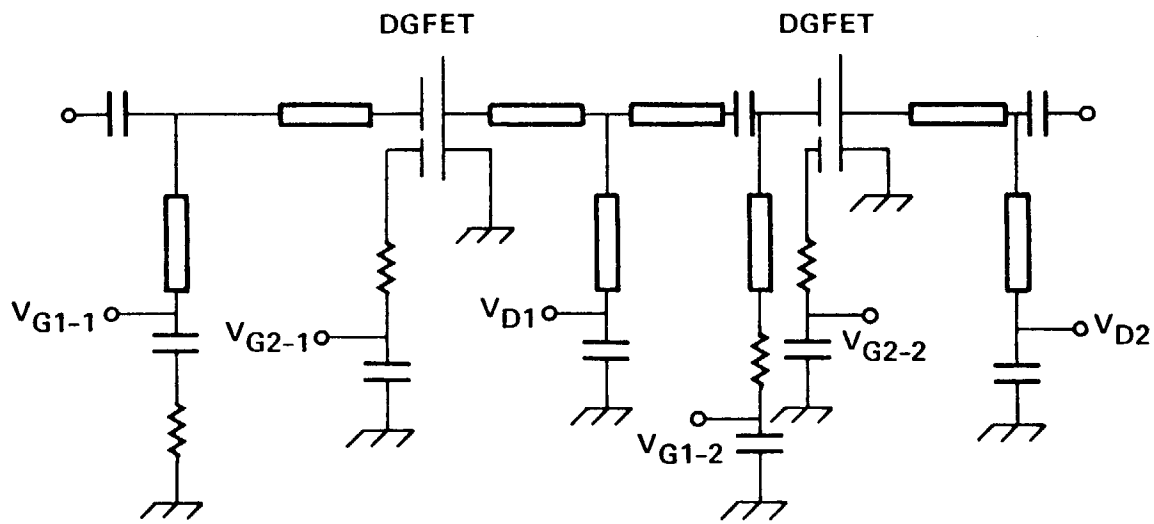
FIRST SWITCH/AMPLIFIER DESIGN



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ACHEIVED FIRST SWITCH AMPLIFIER PERFORMANCE (TWO STAGE CASCADE AMPLIFIER)

• Bandwidth	4.0-5.5 GHz
• Gain	20 dB
• Isolation	> 50 dB
• Gain Ripple	< 1 dB

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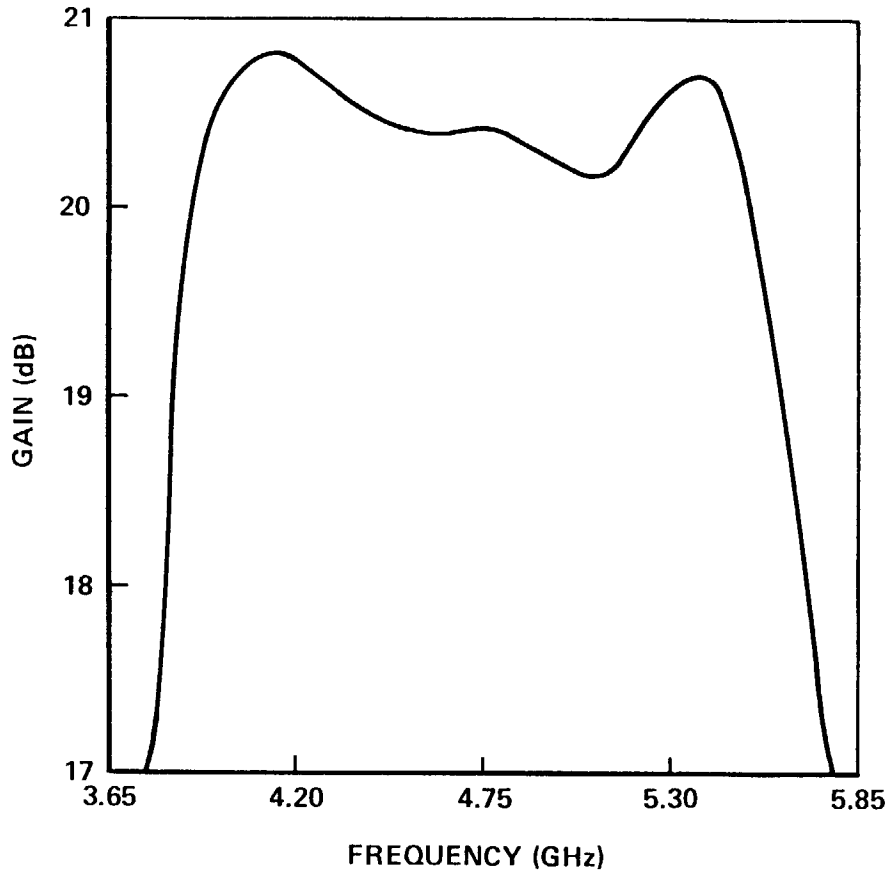
SWITCH AMPLIFIER PERFORMANCE OF THE FIRST DESIGN

VD = 4.0 V VG1–1 = –1.24 V VG1–2 = –1.26 V VG2 = 1.0 V
ID = 40 mA



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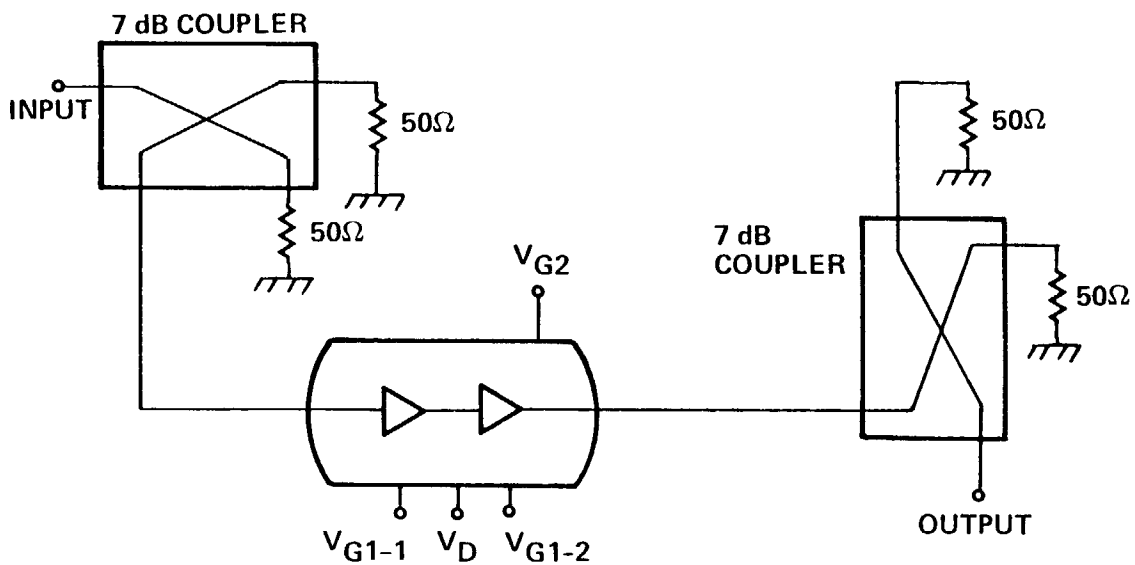
SINGLE SWITCH MATRIX CROSSPOINT

INTEGRATION OF TWO 7 dB COUPLERS WITH
FIRST SWITCH AMPLIFIER



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PERFORMANCE OF THE SINGLE SWITCH MATRIX CROSS POINT (FOR 4 x 4 SWITCH MATRIX)

• Bandwidth	4.05-5.50 GHz
• Gain	7.1 dB nominal
• Gain Ripple	1 dB
• Isolation	> 50 dB
• VSWR	1.7 : 1 maximum
• Switching Speed	< 2 nsec

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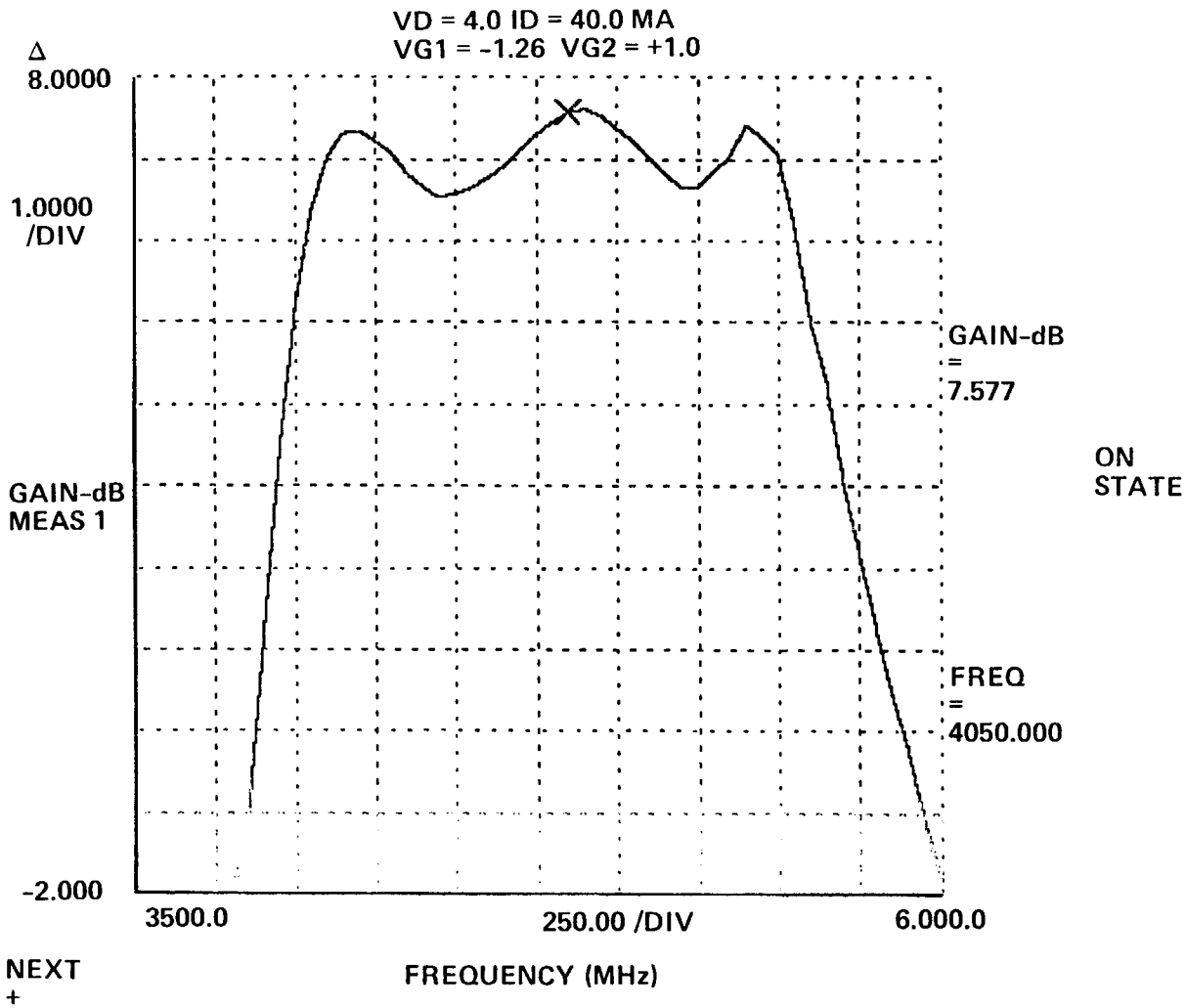
NASA 30/20 GHz SWITCH MATRIX AMPLIFIER
SINGLE CROSSPOINT TEST



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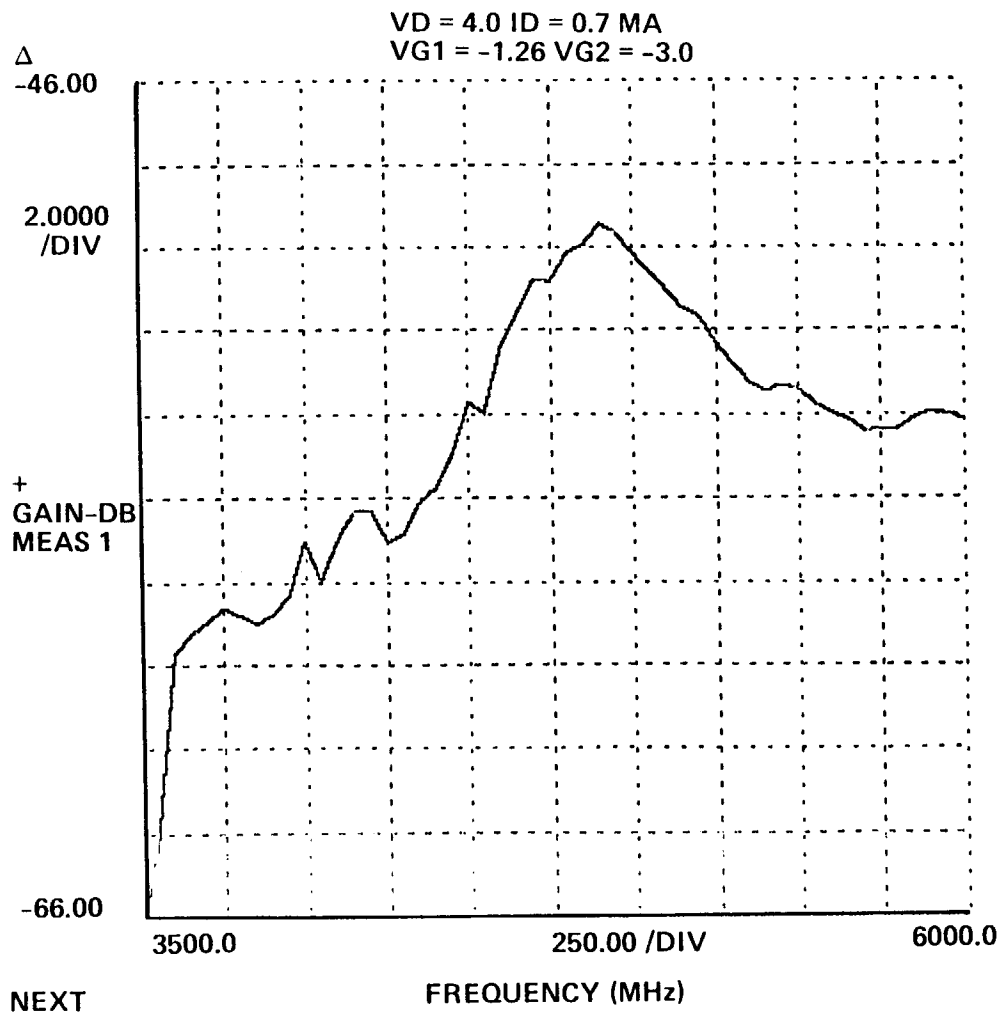
NASA 30/20 GHz SWITCH MATRIX AMPLIFIER
SINGLE CROSSPOINT TEST



OFF
STATE

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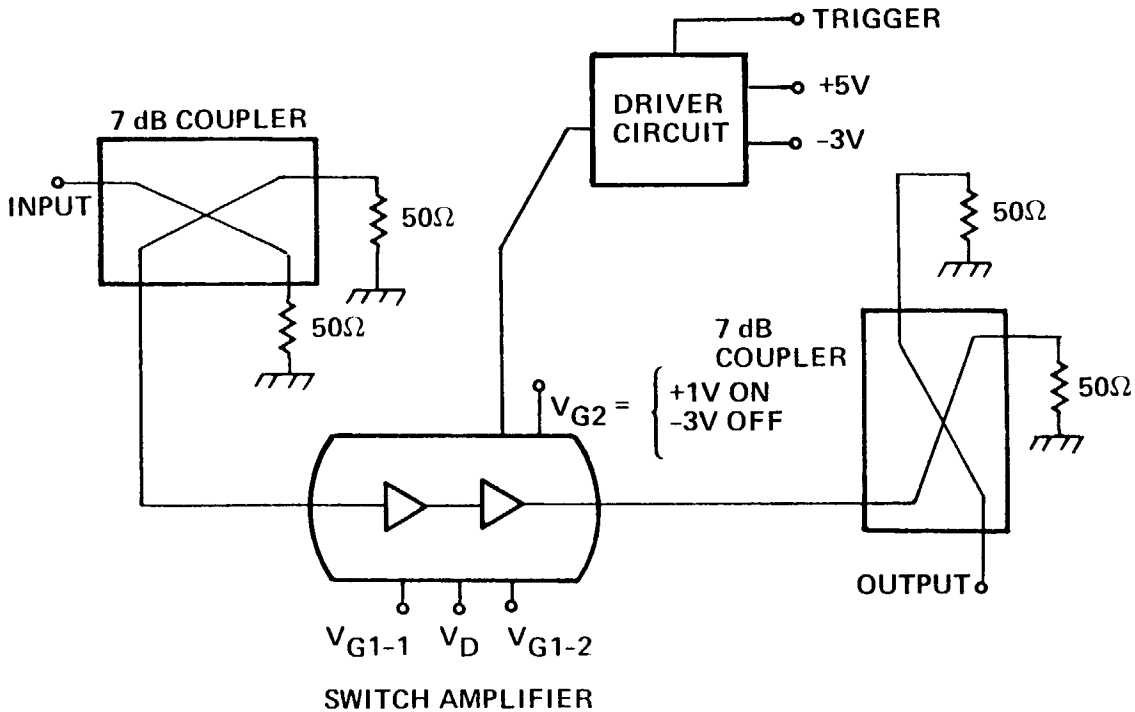
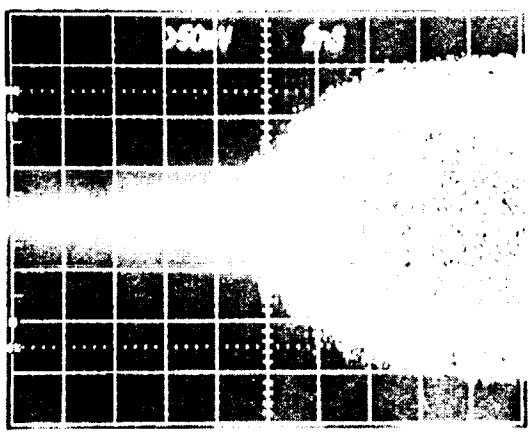
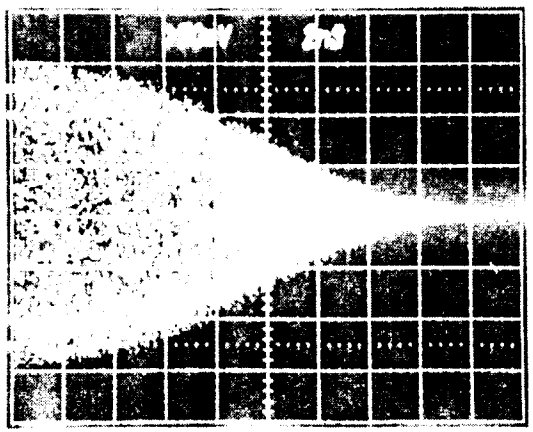
INTEGRATION TEST OF SWITCH AMPLIFIER AND COUPLER ASSEMBLY WITH THE BREADBOARD DRIVER CIRCUIT



SWITCHING ON



SWITCHING OFF



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SECOND SWITCH AMPLIFIER DESIGN

- Self biasing circuit was incorporated to simplify device biasing
- Eleminate gate-2 capacitance in order to achieve better stability and faster switching speeds
- Replacement of chip resistors with thin film resistors to improve circuit performance and reduce assembly time
- Use module package design that house two individual switch amplifiers to reduce package weight and help ease amplifier testing

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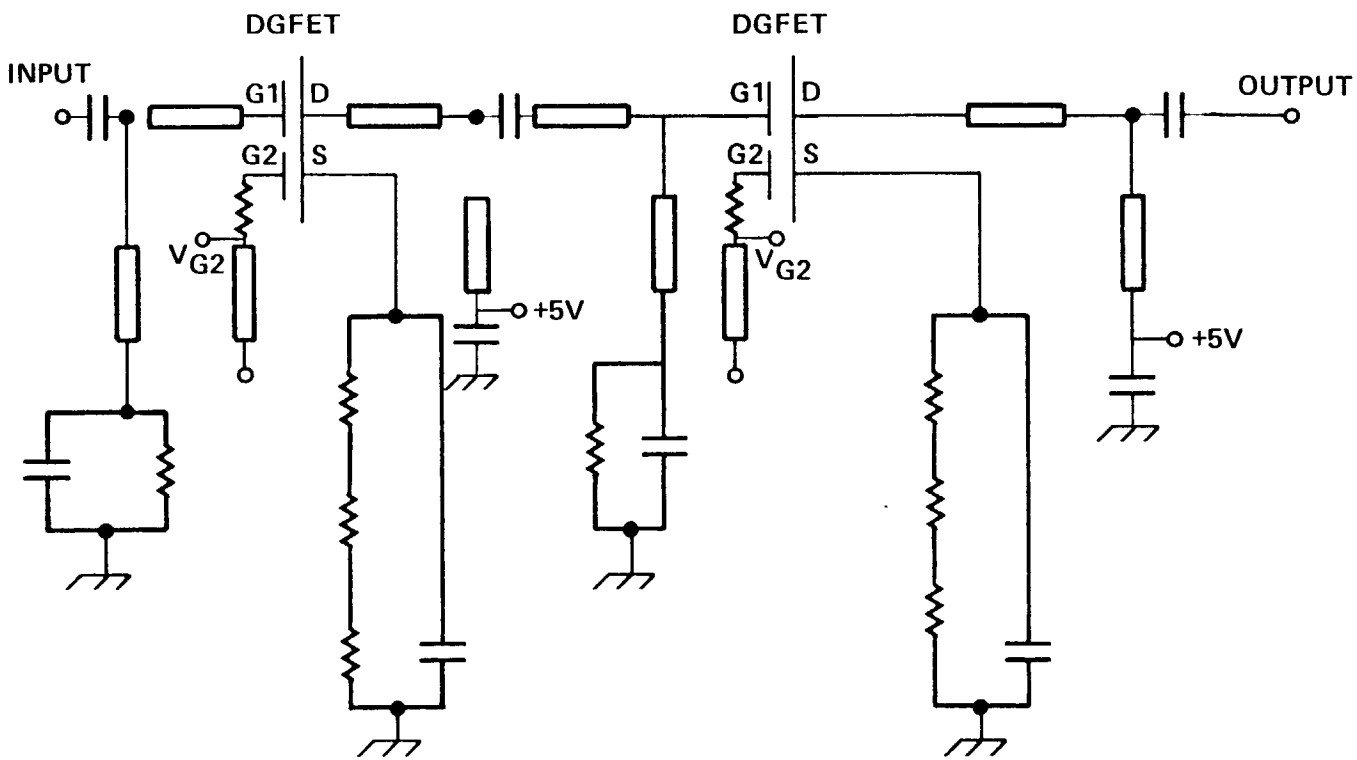
SECOND SWITCH AMPLIFIER DESIGN



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COMPUTER ANALYSIS USING COMPACT PROGRAM

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN<ANGL)	S21 (MAGN<ANGL)	S12 (MAGN<ANGL)	S22 (MAGN<ANGL)	S21 DB	K FACT.
2000.00	0.65< 176	0.07< 32.1	*****DB-125.4	0.99< 150	-22.66	999.99
2500.00	0.65< 150	0.23< 90.3	-95.1DB -51.0	0.98< 140	-12.71	999.99
3000.00	0.54< 99	2.66< 83.1	-73.6DB -45.4	0.96< 126	8.48	54.21
3250.00	0.23< 15	10.04< 11.0	-62.3DB-113.4	0.91< 117	20.04	10.21
3500.00	0.04< -125	10.11< -70.9	-61.8DB 170.0	0.88< 107	20.09	14.02
3750.00	0.21< -93	9.61<-113.9	-62.6DB 131.0	0.81< 91	19.66	22.59
4000.00	0.44< -120	10.15<-150.8	-61.8DB 99.4	0.72< 69	20.13	23.58
4250.00	0.57< -140	10.00< 174.4	-62.5DB 68.3	0.54< 42	20.00	31.40
4500.00	0.67< -156	10.16< 140.0	-62.8DB 38.0	0.39< -10	20.14	31.63
4750.00	0.73< -169	9.98< 106.6	-62.7DB 9.4	0.39< -76	19.99	26.80
5000.00	0.78< -179	9.93< 75.8	-63.3DB -17.2	0.58< -119	19.94	19.07
5250.00	0.80< 171	9.80< 48.9	-62.3DB -39.2	0.72< -143	19.83	11.05
5500.00	0.82< 163	9.97< 19.7	-60.3DB -61.9	0.84< -163	19.98	4.62
5750.00	0.82< 155	10.23< -12.9	-59.1DB -88.9	0.89< 180	20.20	2.73
6000.00	0.82< 147	10.01< -49.9	-57.8DB-118.3	0.88< 167	20.01	3.38
6250.00	0.80< 141	8.17< -82.7	-57.8DB-149.7	0.81< 160	18.24	6.60
6500.00	0.79< 135	6.18<-110.2	-58.3DB-175.3	0.77< 157	15.82	11.52
7000.00	0.79< 124	3.82<-151.8	-60.3DB 149.9	0.79< 152	11.65	19.10
8000.00	0.79< 98	2.24< 153.8	-60.0DB 111.8	0.85< 138	6.99	23.09
9000.00	0.78< 69	2.16< 104.2	-56.2DB 82.9	0.89< 123	6.67	11.94
10000.00	0.78< 33	3.14< 34.8	-49.5DB 37.2	0.94< 105	9.93	1.99
11000.00	0.67< -3	2.40< -79.7	-49.0DB -55.9	0.80< 86	7.59	11.76
12000.00	0.70< -33	0.98<-149.2	-53.8DB-104.0	0.80< 74	-0.22	46.35

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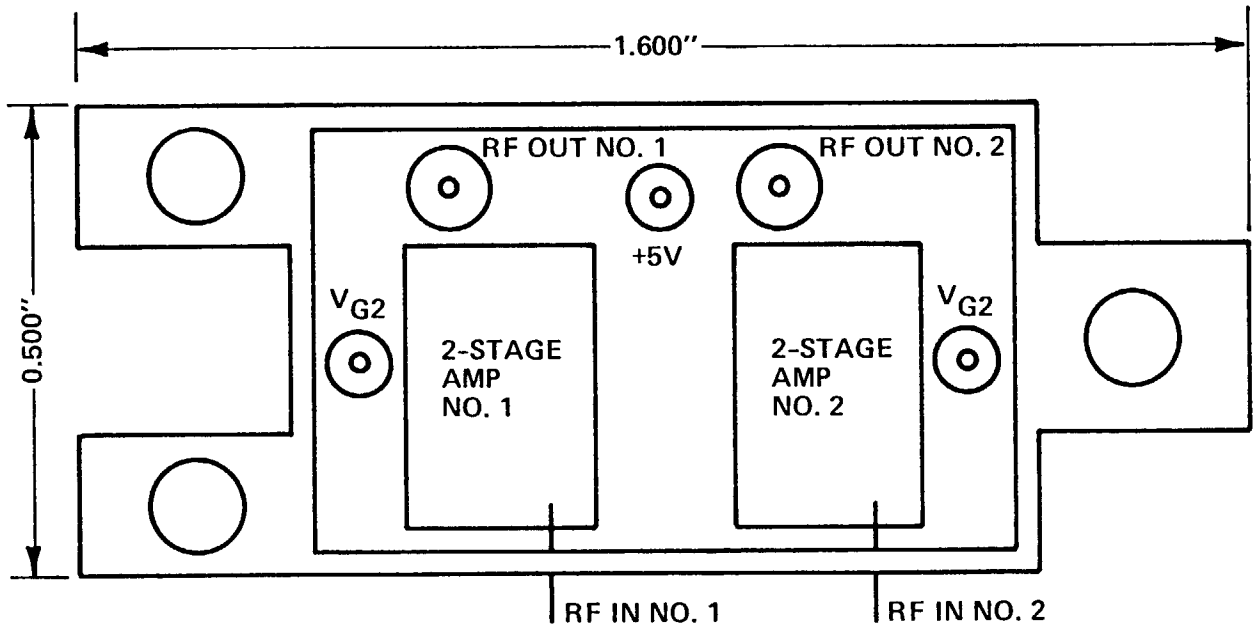
SWITCH AMPLIFIER MODULE DESIGN



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SWITCH DRIVER DEVELOPMENT

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Communications Corporation

DESIRED PARAMETERS

- Maximize switching speed
- Minimize power consumption

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PERFORMANCE OF SWITCH DRIVER

- DESIGN APPROACHES
- SWITCH DRIVER VERSIONS

VERSION NO.	POWER FOR (20 X 20) MATRIX (W)	RISE TIME (NSEC)	FALL TIME (NSEC)	REMARKS
1	15	5.0	7.0	2 TRANSISTORS
2	22	4.5	5.0	2 TRANSISTORS
3	26.5	5.0	5.0	2 TRANSISTORS (POSITIVE OUTPUT)
4	1.54	7.0	13	1 TRANSISTOR
4A	4.24	4.5	6	1 TRANSISTOR (+1, −3 V OUTPUT LEVELS)
5	.7	7	25.0	(HUGHES)
6	5.0	7.0	13.0	(TOO COMPLEX)
7	3.08	7.0	13.0	(DUAL VERS. 4)

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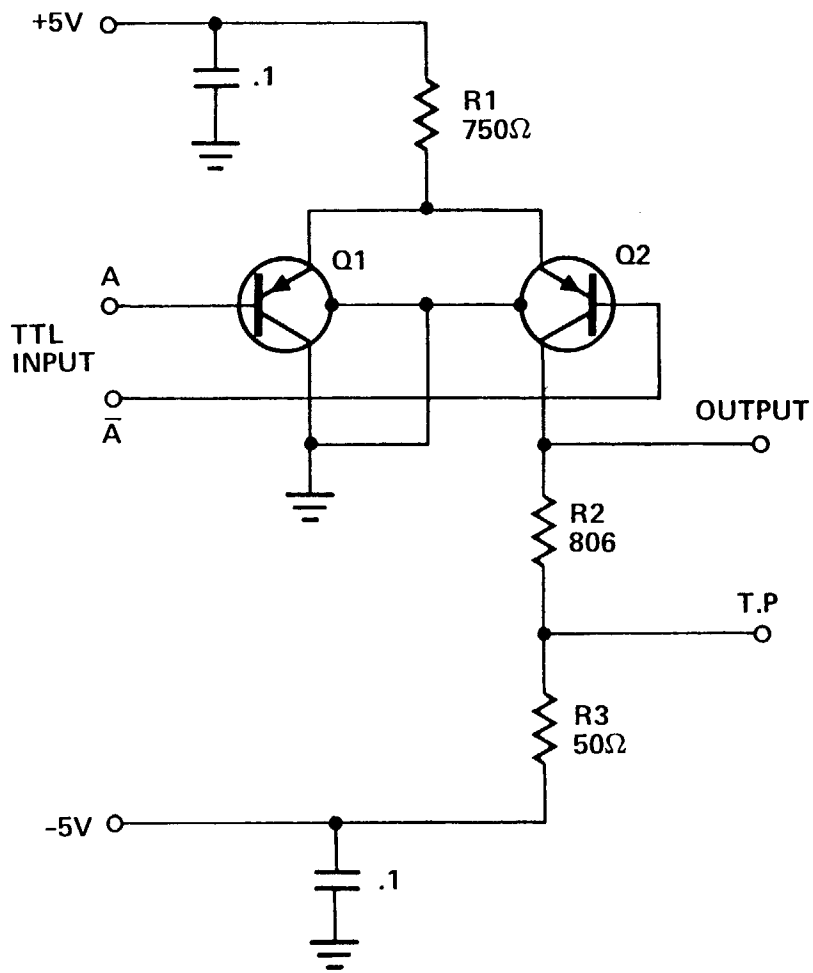
SWITCH DRIVER (VERSION 1)



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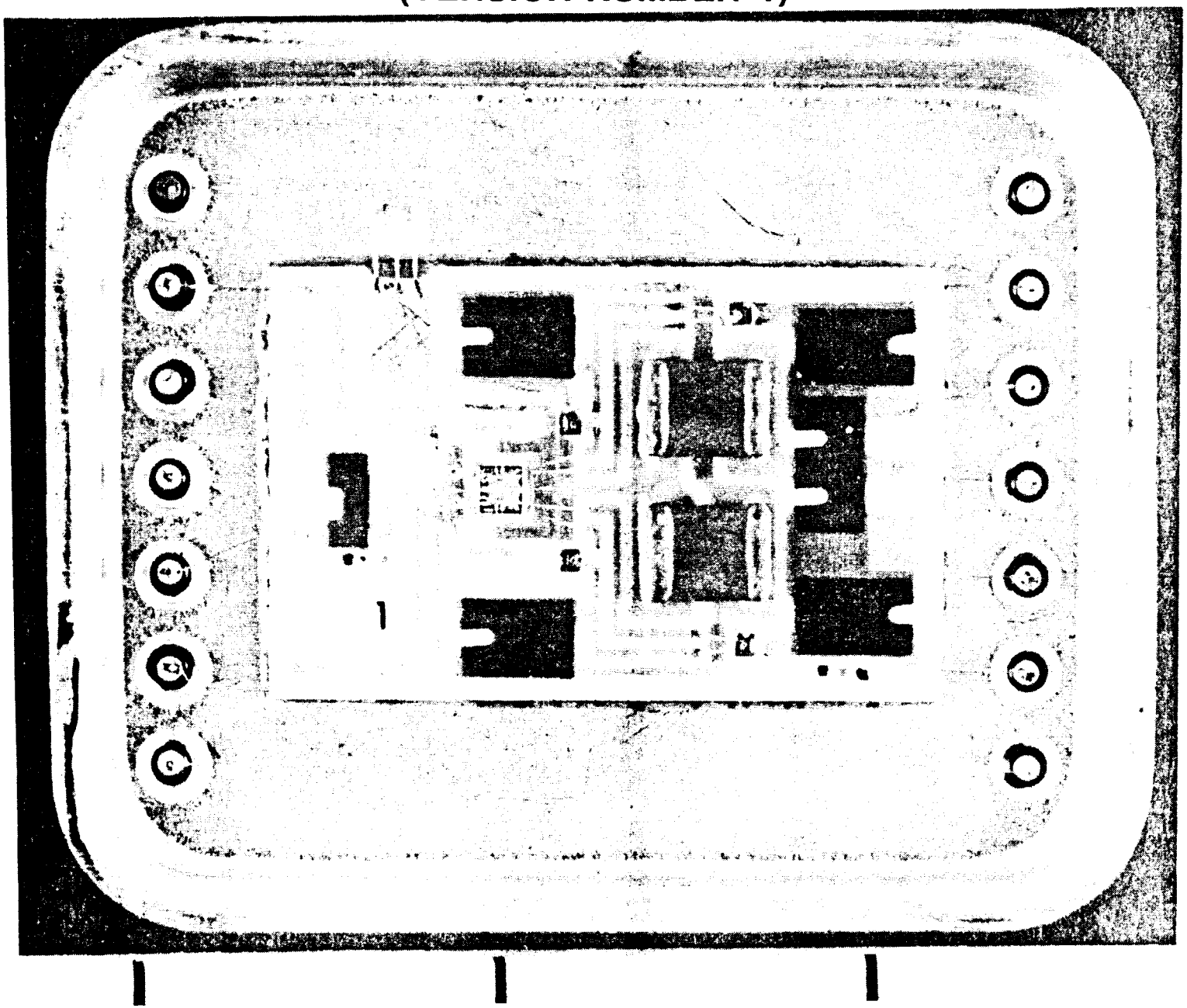
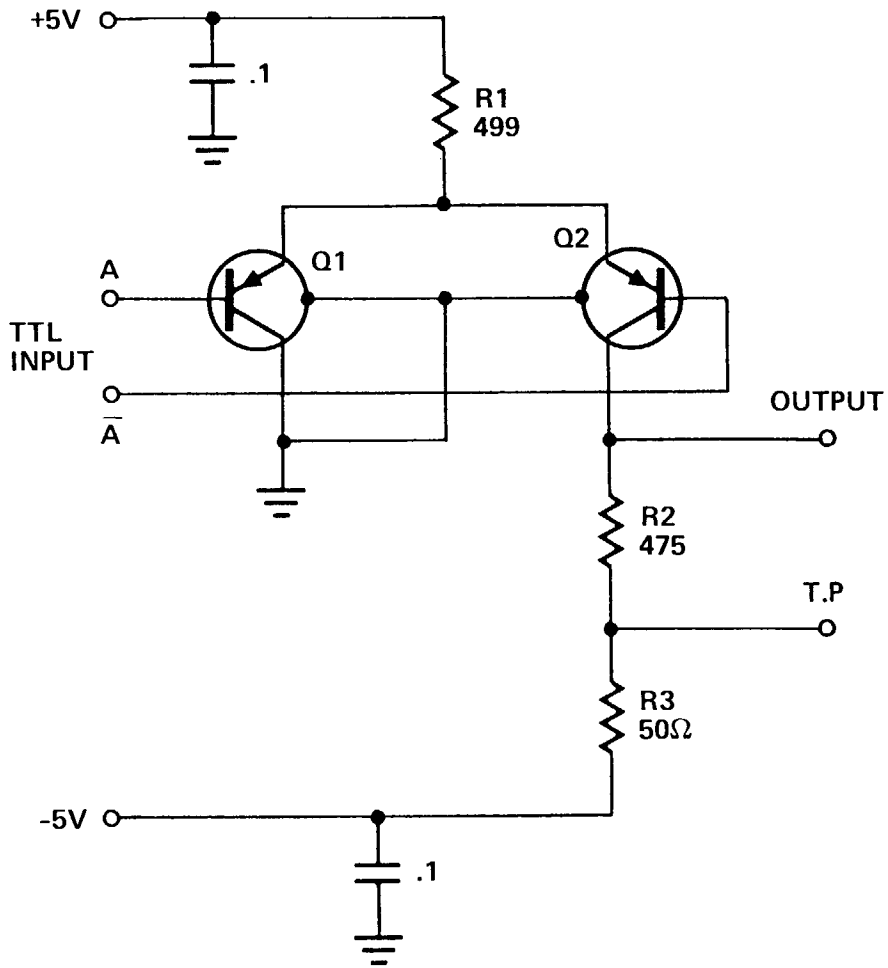
DUAL DRIVER CIRCUIT
(VERSION NUMBER 1)



SWITCH DRIVER (VERSION 2)



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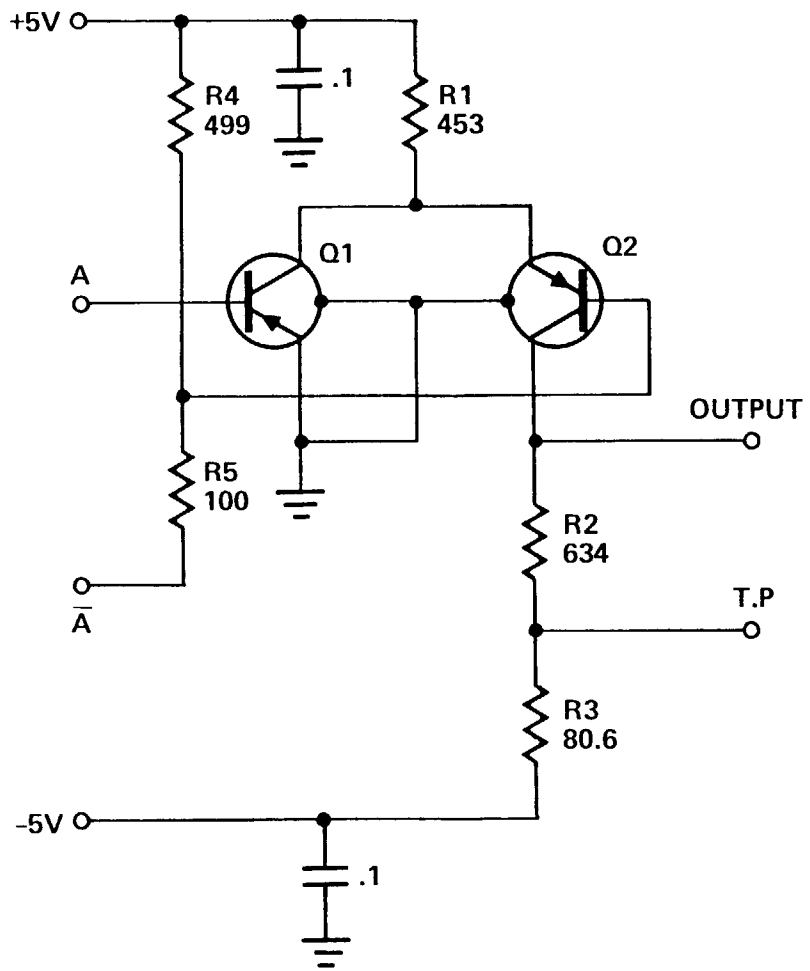
SWITCH DRIVER (VERSION 3)



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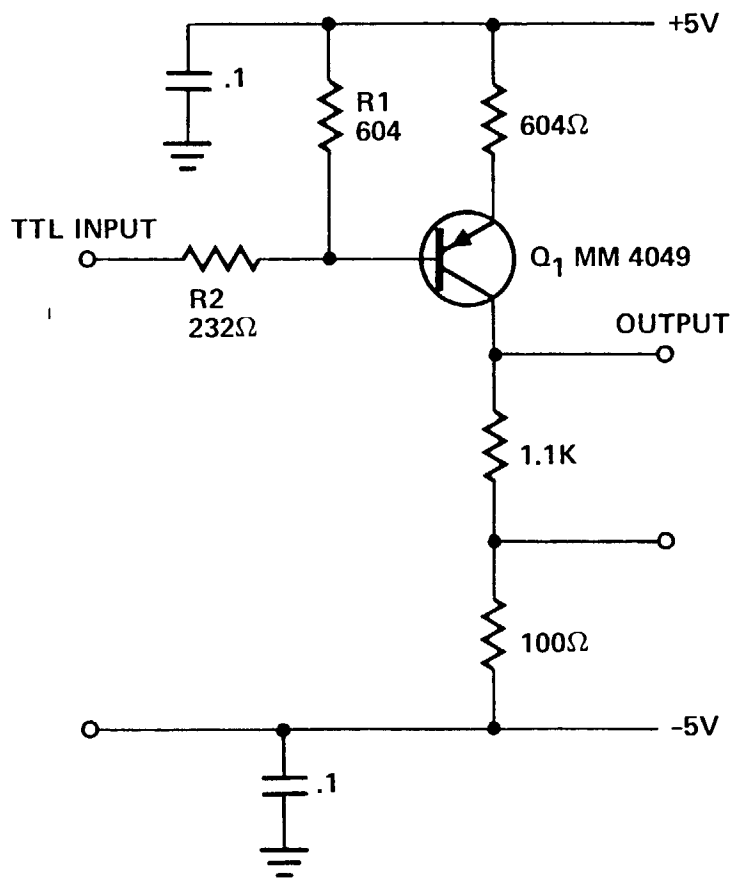
SINGLE TRANSISTOR SWITCH (VERSION 4)



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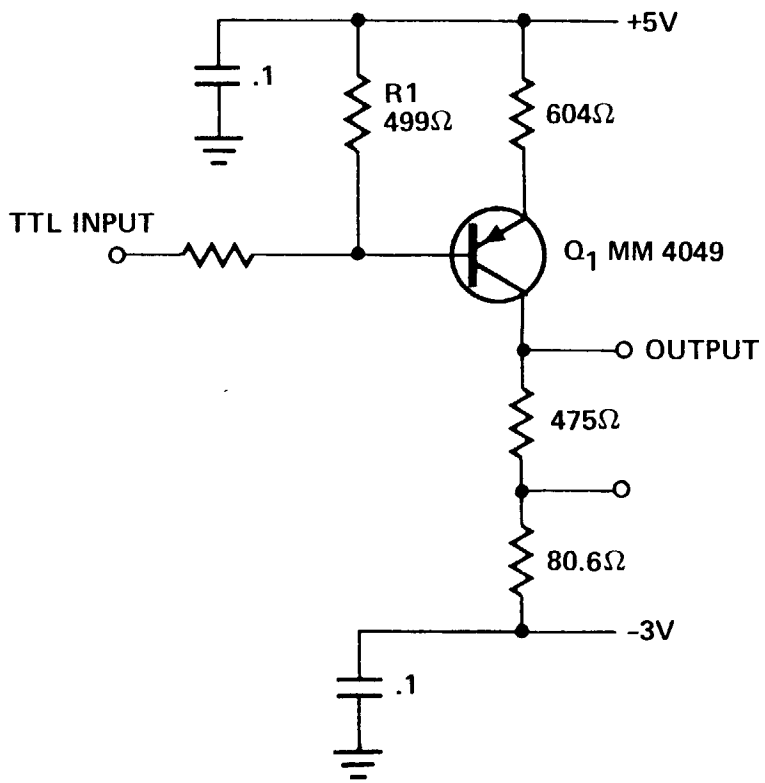
SINGLE TRANSISTOR SWITCH (VERSION 4A)



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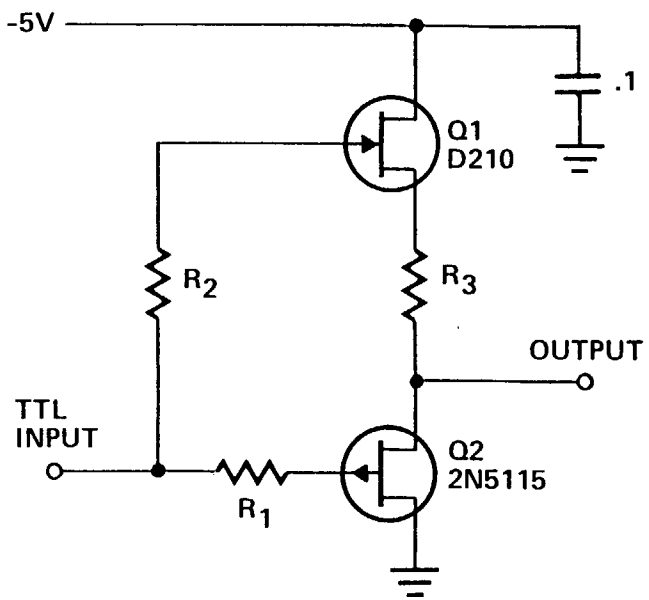
HUGHES SWITCH DRIVER (VERSION 5)



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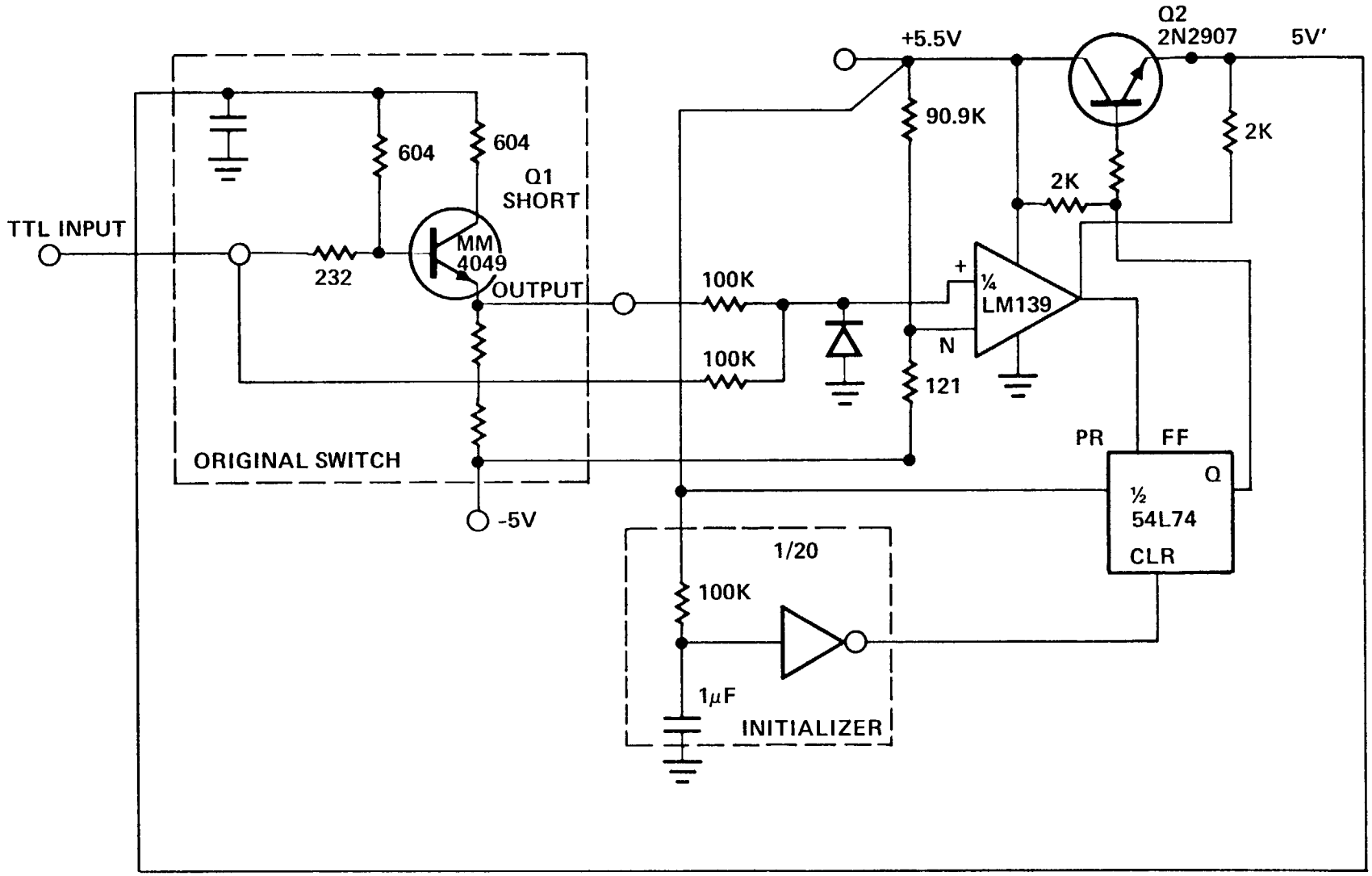
SWITCH DRIVER (VERSION 6)



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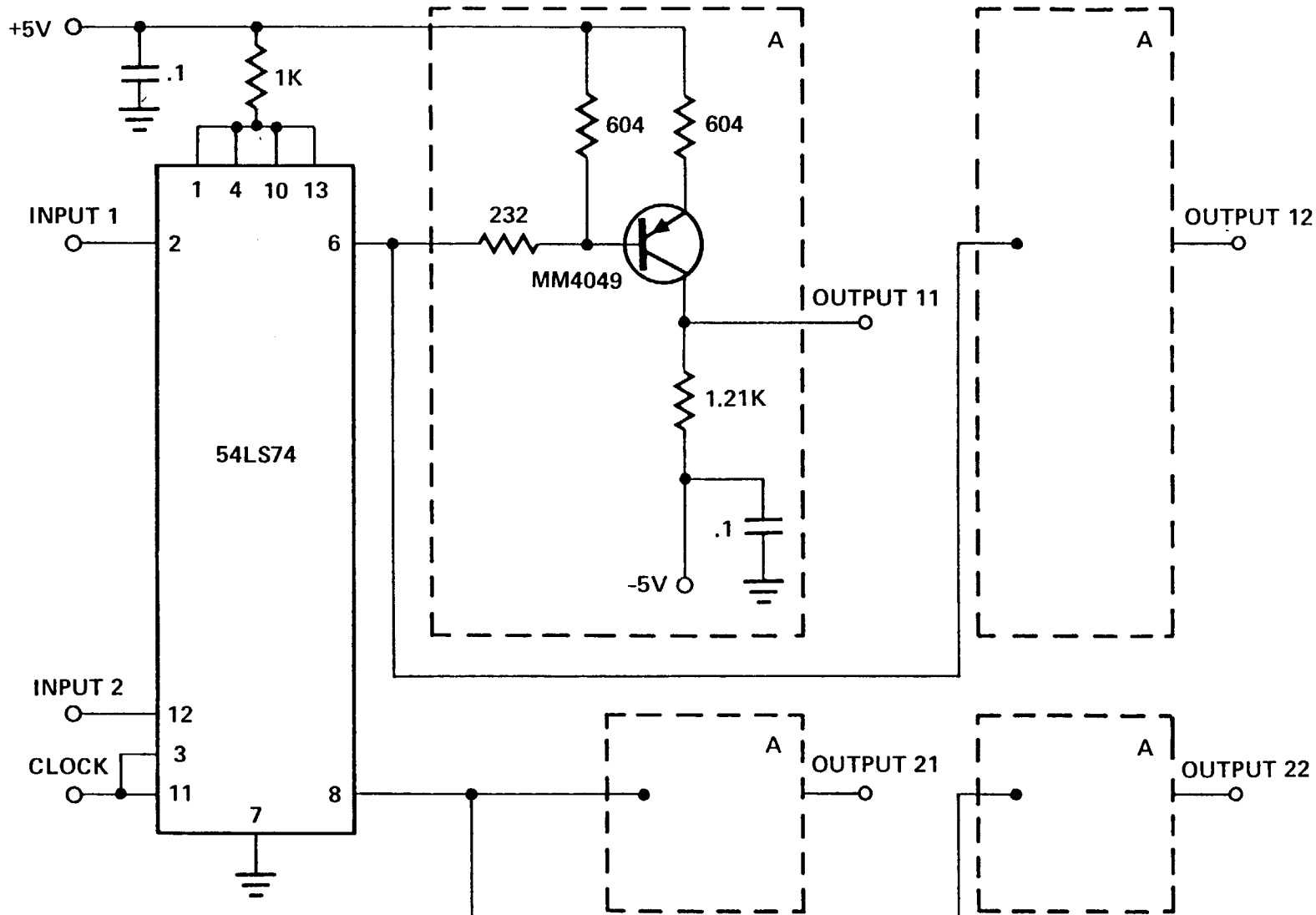
SWITCH DRIVER (VERSION 7)



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DISTRIBUTION CONTROL UNIT DEVELOPMENT

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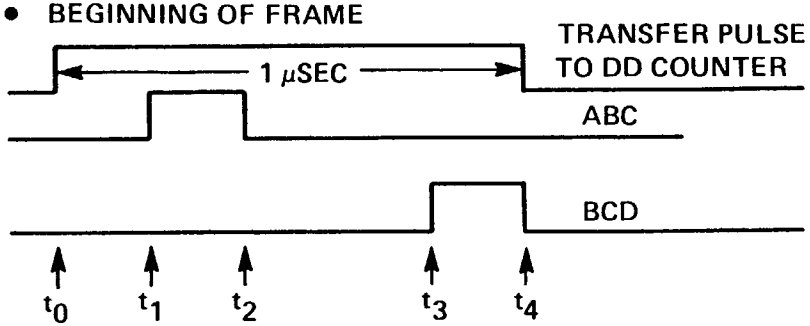
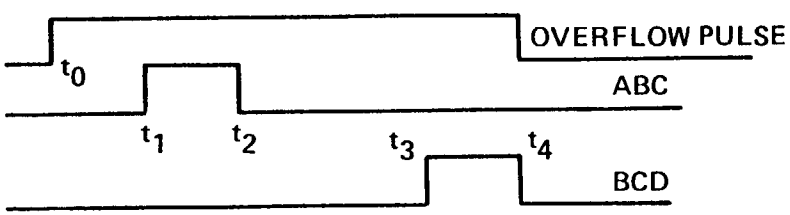
4 x 4 SWITCH MATRIX DISTRIBUTION CONTROL UNIT

- FRAME LENGTH 100 μSEC
- NUMBER OF STATES 8
- SCHEMATICS
- TIMING

- BEGINNING OF FRAME



- COUNTER OVERFLOW – STATE TRANSITION



A)	t_0	MEMORY ADDRESS START CHANGING
B)	t_1–t_2	CONTENTS OF SELECTED MEMORY ADDRESS REACHES OUTPUT
C)	t_3	MEMORY ADDRESS CHANGES (INPUT ONLY)
D)	t_4	MEMORY OUTPUT LOADED TO DDC
E.	t_0	t_0
F.	t_1–t_2	SAME AS A
G.	t_3	SAME AS C
H.	t_4	SAME AS D

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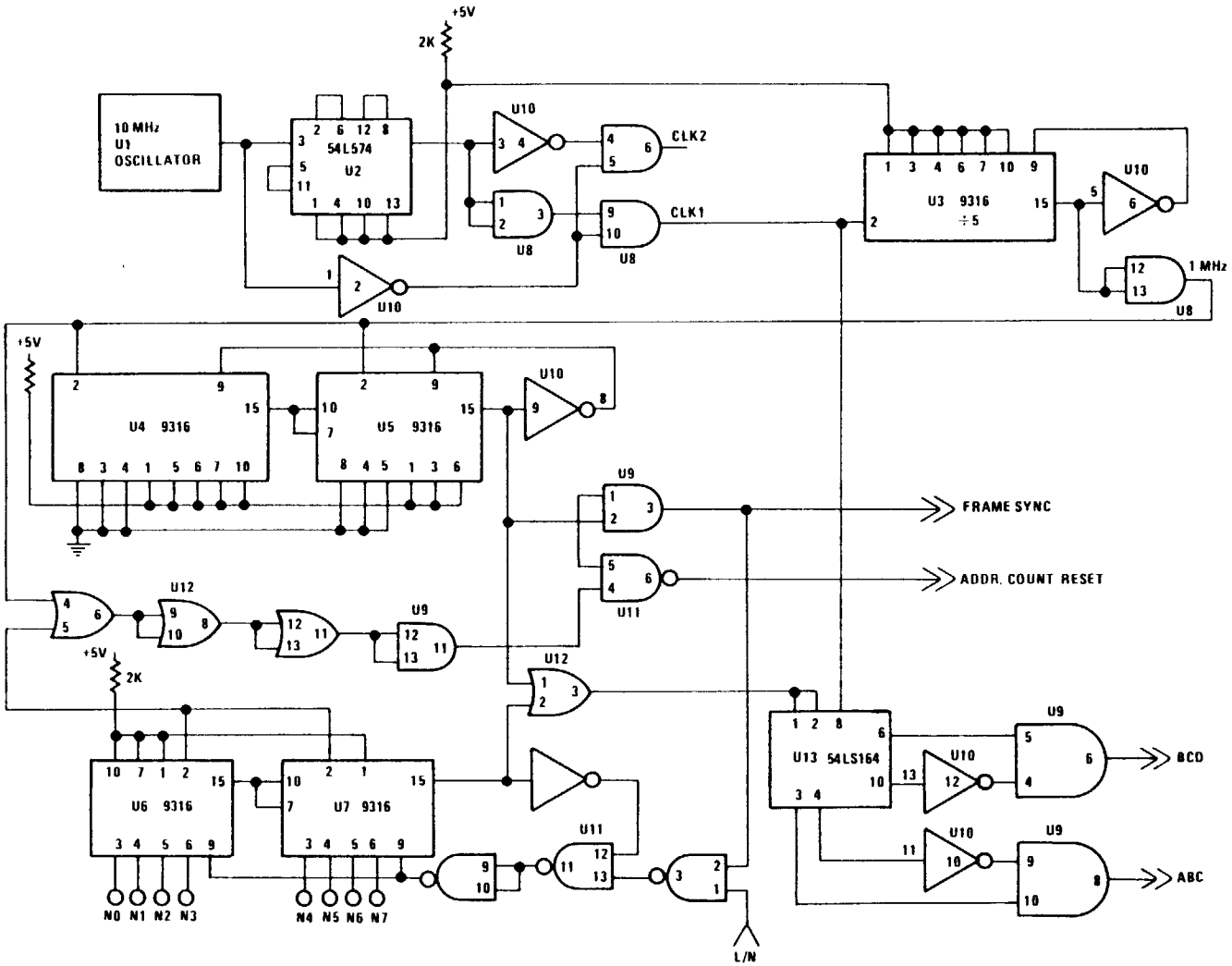
M.S.M. CONTROLLER 1



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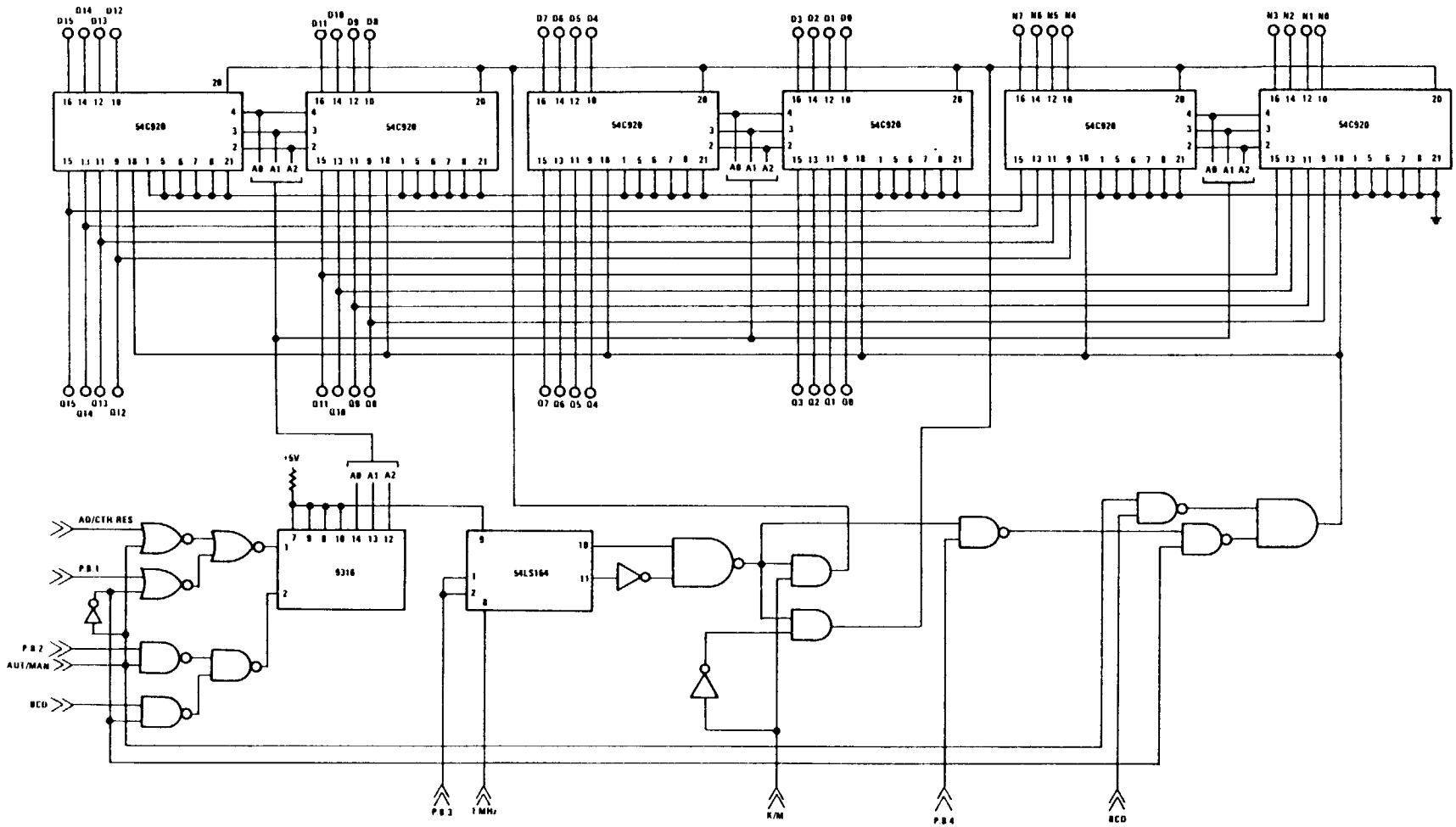
M.S.M. CONTROLLER 2



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20 X 20 SWITCH MATRIX DISTRIBUTION CONTROL UNIT DESIGN CONCEPT

- Similarities with the 4 x 4 matrix DCU
- Differences
- Functional Blocks

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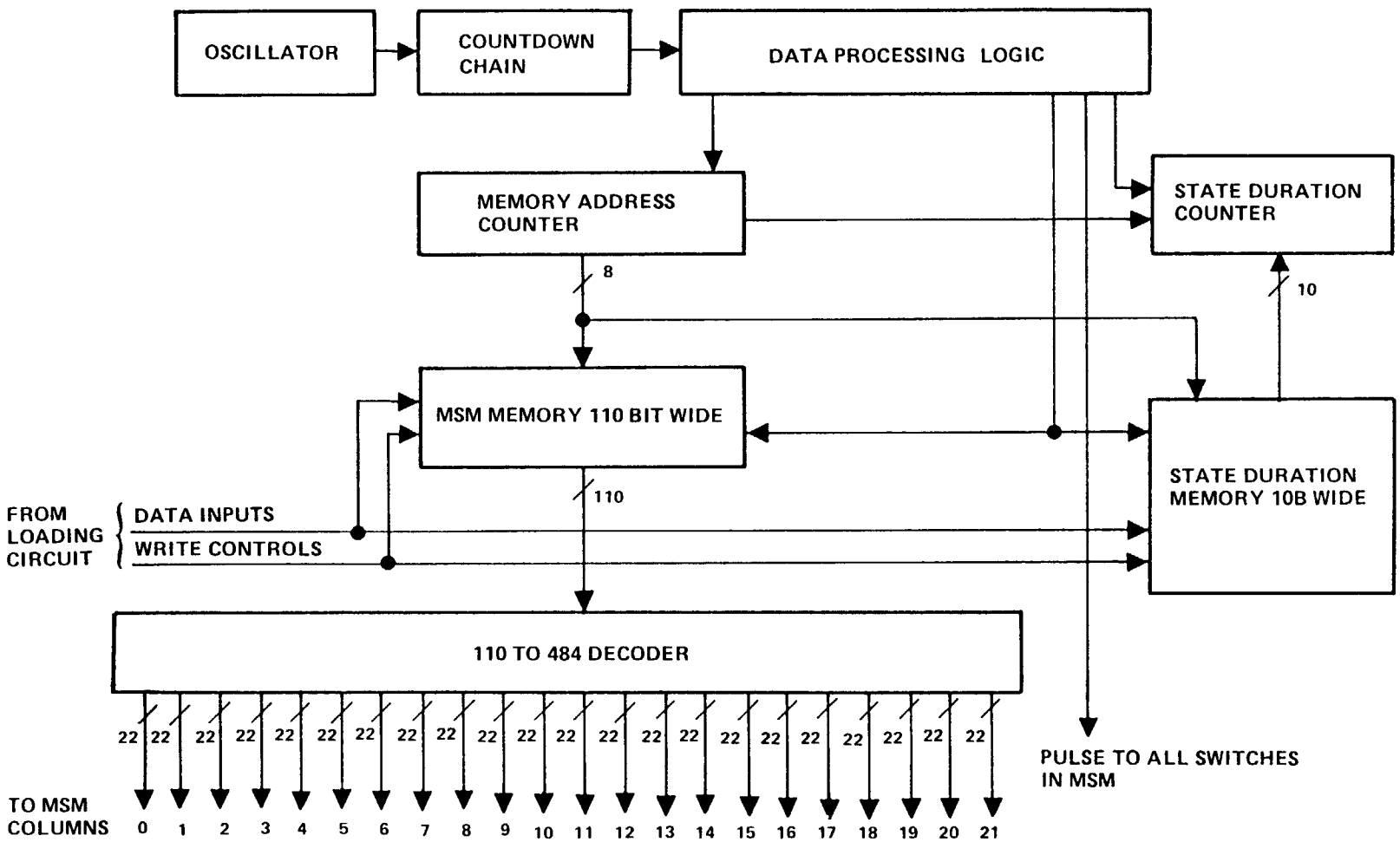
20 x 20 MSM DISTRIBUTION CONTROL UNIT BLOCK DIAGRAM



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M.S.M. DECODER

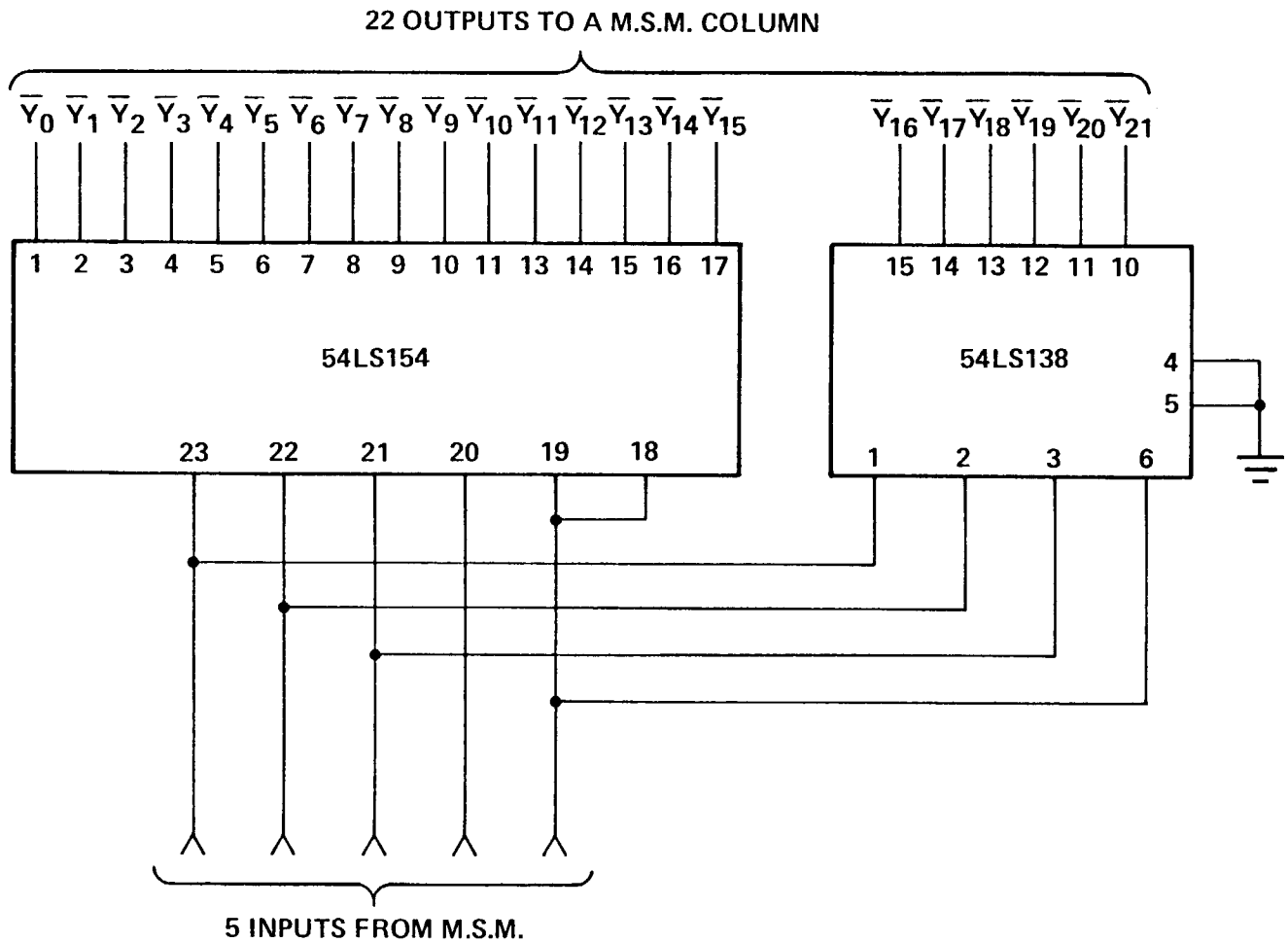

FIGURE 2.7.1. M.S.M. DECODER

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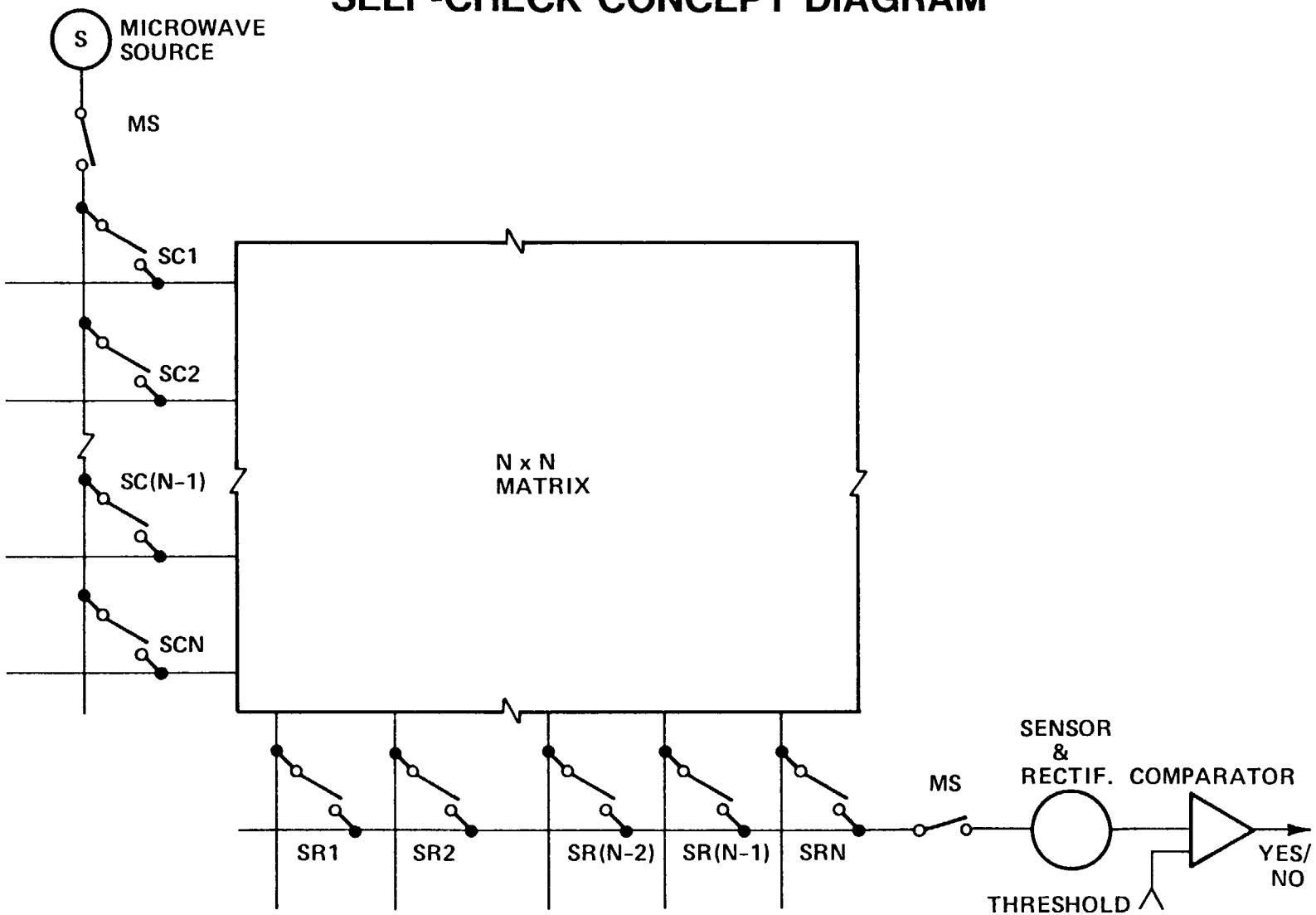
SELF-CHECK CONCEPT DIAGRAM



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MECHANICAL PACKAGING CONCEPT

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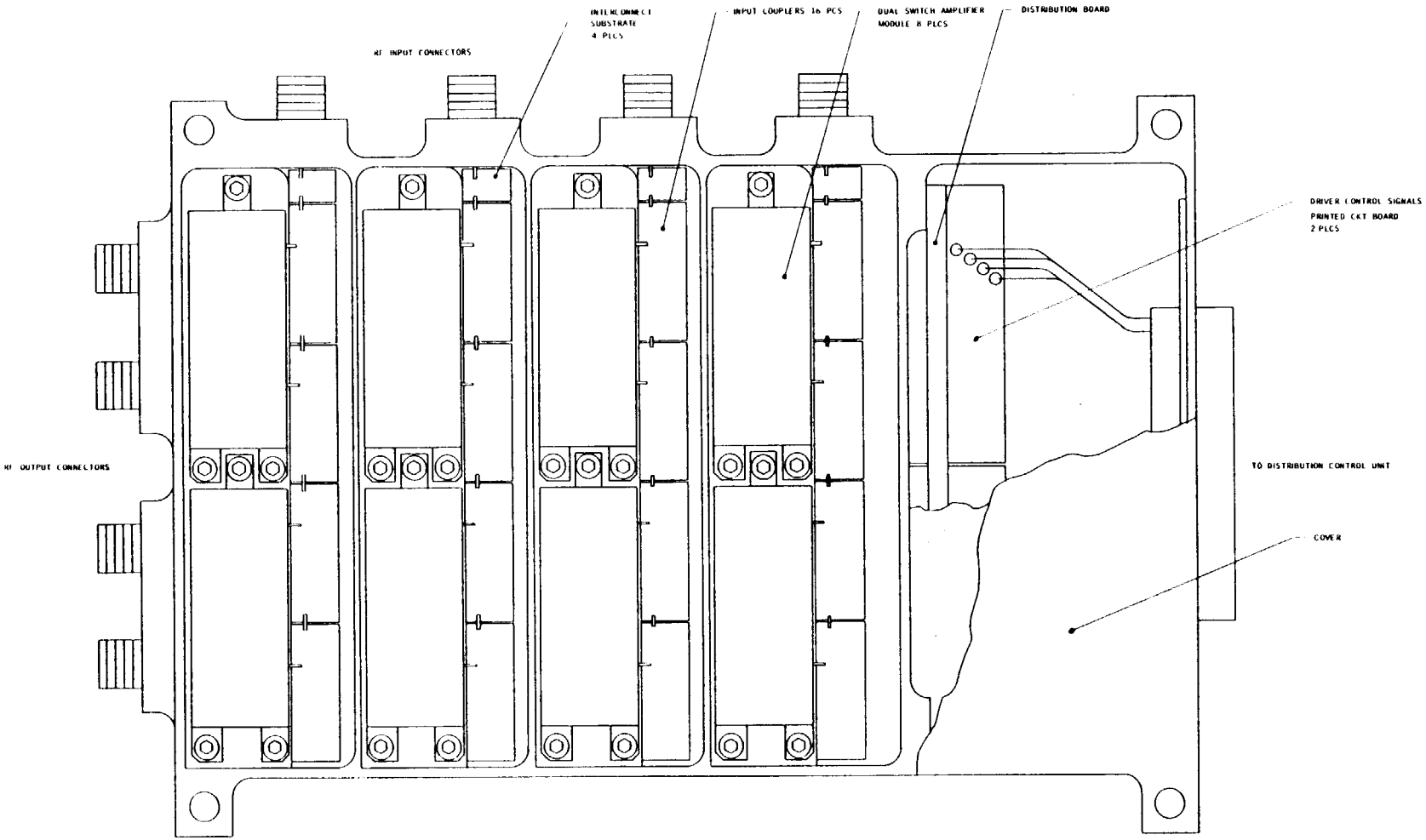
TOP VIEW OF THE 4 X 4 MICROWAVE SWITCH MATRIX



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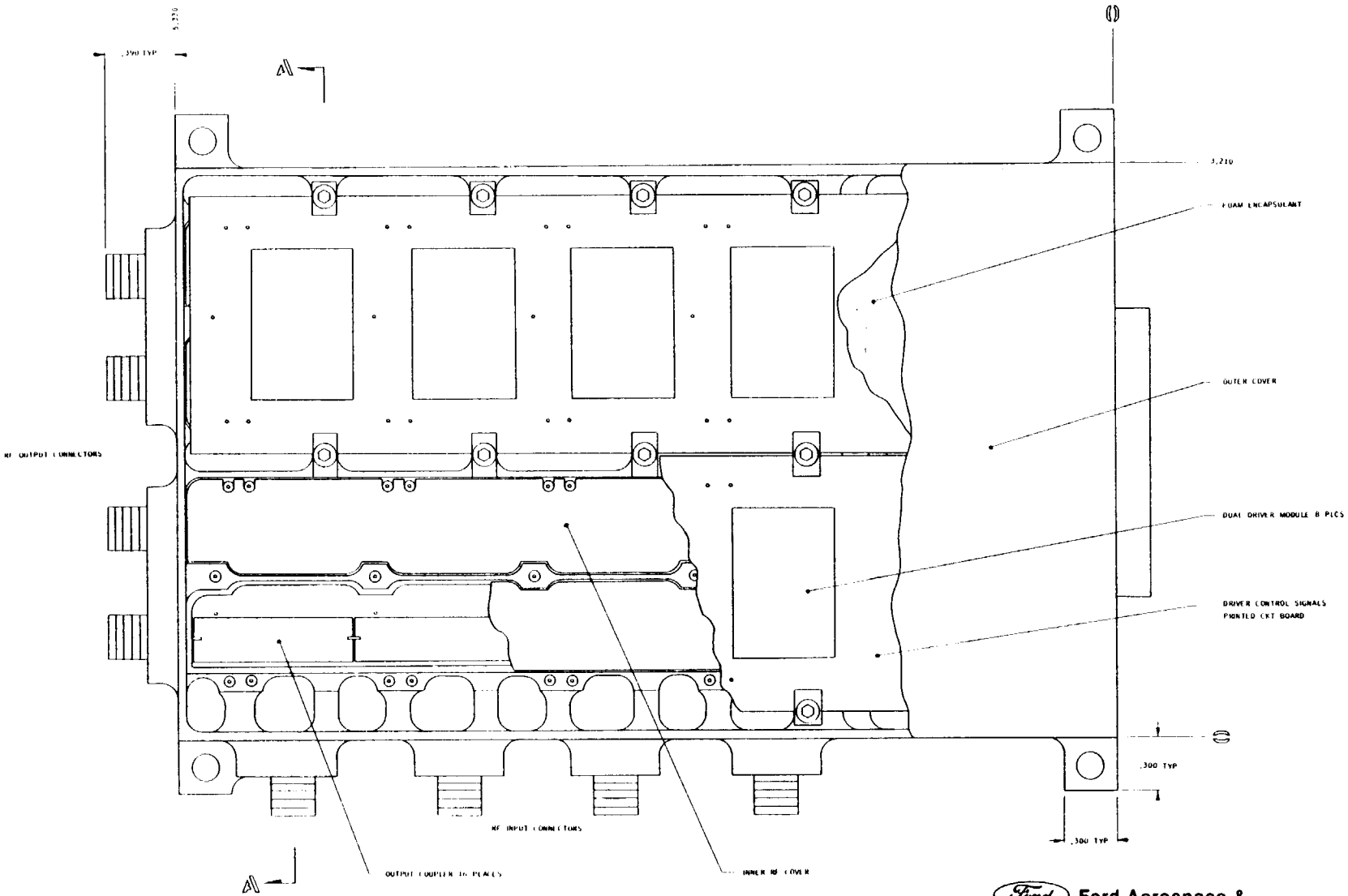
BOTTOM VIEW OF THE 4 X 4 MICROWAVE SWITCH MATRIX



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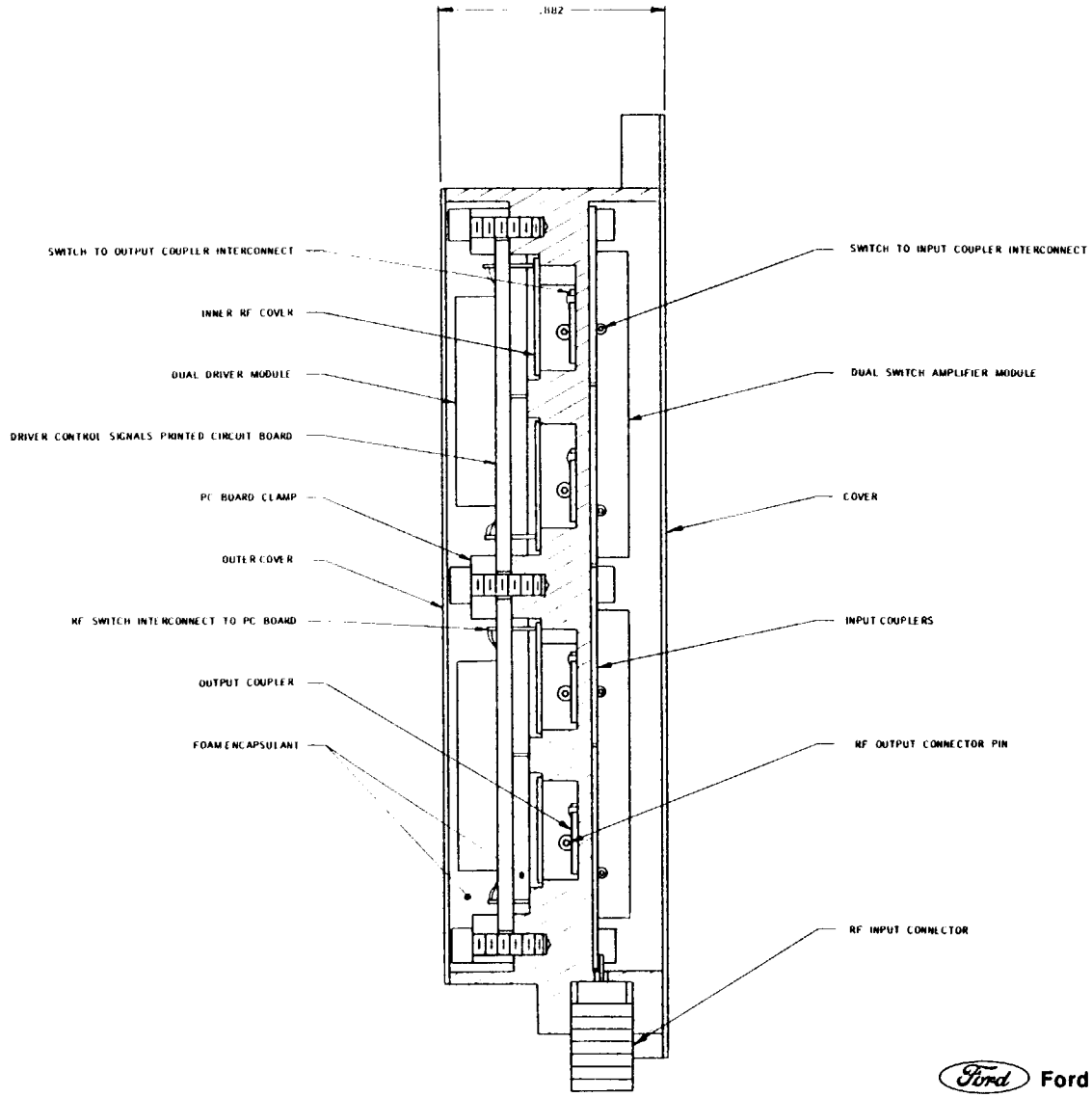
CROSS-SECTION VIEW OF THE 4 X 4 MICROWAVE SWITCH MATRIX



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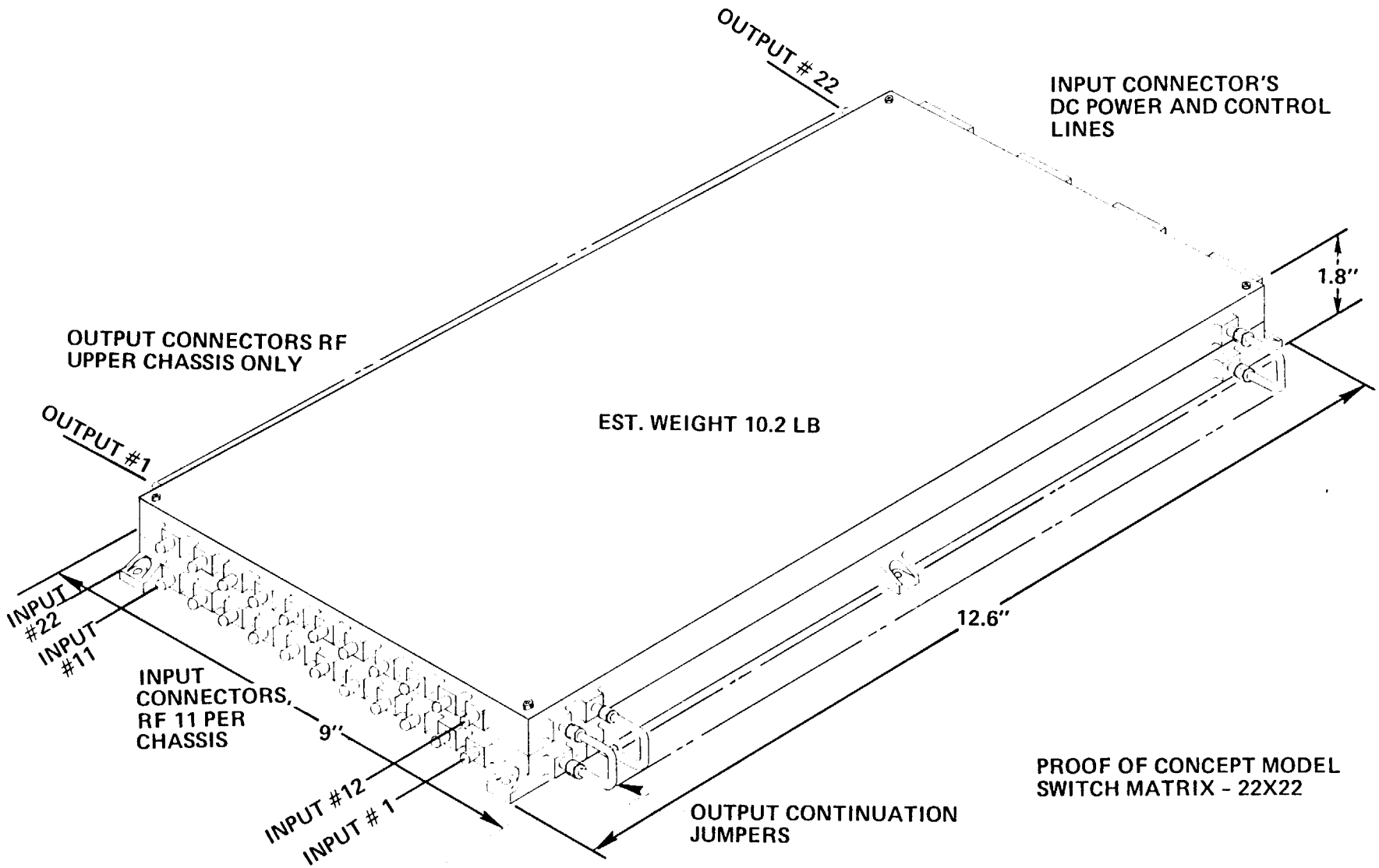
SECTION A-A

MECHANICAL CONFIGURATION OF THE POC MODEL (20 X 20 MICROWAVE SWITCH MATRIX)



PROOF OF CONCEPT MODEL
SWITCH MATRIX - 22X22

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