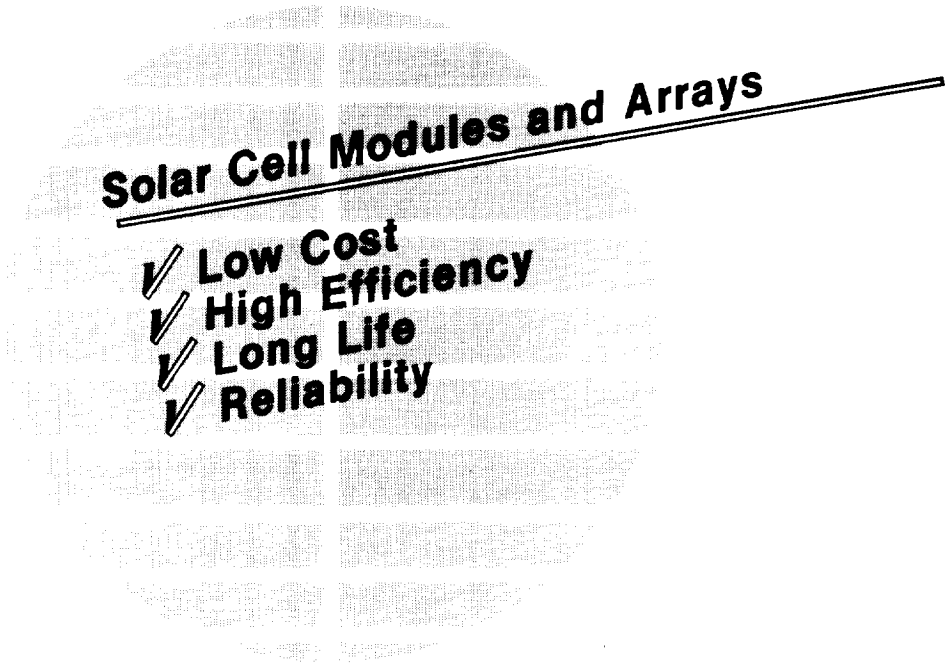
JPL Publication 86-31

Electricity from Photovoltaic Solar Cells

Flat-Plate Solar Array Project Final Report

Volume III: Silicon Sheet: Wafers and Ribbons

11 Years of Progress



October 1986

Project Managed by the Jet Propulsion Laboratory for the U.S. Department of Energy

(NASA-CR-180661) FLAT-PLATE SOLAR ARRAY PROJECT. VOLUME 3: SILICON SHEET: WAFERS AND RIBBONS Final Report (Jet Propulsion Lab.) 132 p CSCL 10A

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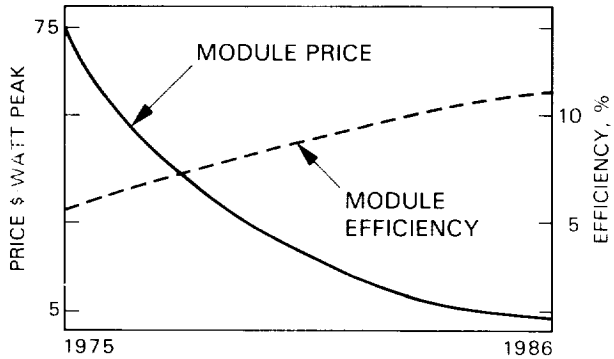
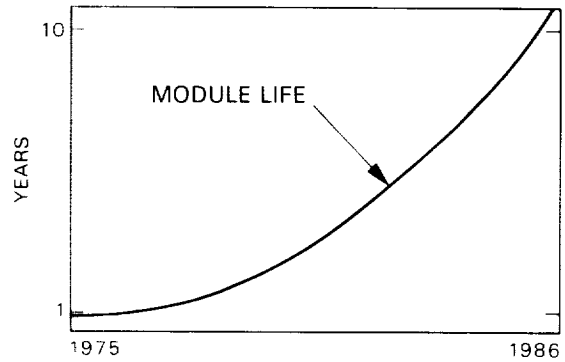
Photovoltaic Module Progress



Flat or non-concentrating module prices have dropped as module efficiencies have increased. Prices are in 1985 dollars for large quantities of commercial products.



Typical module lifetimes were less than 1 year but are now estimated to be greater than 10 years. (Ten-year warranties are now available.)

Technology advancement in crystalline silicon solar cells and modules (non-concentrating).

Union Carbide Corporation (UCC) funded the now operational silicon refinement production plant with 1200 MT/year capacity. DOE/FSA-sponsored efforts were prominent in the UCC process research and development.

The automated machine interconnects solar cells and places them for module assembly. The second-generation machine made by Kulicke and Soffa was cost shared by Westinghouse Corporation and DOE/FSA.

A Block I module (fabricated in 1975), held in front of four Block V modules, represents the progress of an 11-year effort. The modules, designed and manufactured by industry to FSA specifications and evaluated by FSA, rapidly evolved during the series of module purchases by DOE/FSA.

More technology advancements of the cooperative industry/university/ DOE/FSA efforts are shown on the inside back cover. Use of modules in photovoltaic power systems are shown on the outside back cover.

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Electricity from Photovoltaic Solar Cells

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Volume III: Silicon Sheet: Wafers and Ribbons

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11 Years of Progress

October 1986

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Final Report Organization

This FSA Final Report (JPL Publication 86-31, 5101-289, DOE/JPL 1012-125, October 1986) is composed of eight volumes, consisting of an Executive Summary and seven technology reports:

Volume I: Executive Summary.

Volume II: Silicon Material.

Volume III: Silicon Sheet: Wafers and Ribbons

Volume IV: High-Efficiency Solar Cells.

Volume V: Process Development.

Volume VI: Engineering Sciences and Reliability.

Volume VII: Module Encapsulation.

Volume VIII: Project Analysis and Integration.

Two supplemental reports included in the final report package are:

FSA Project: 10 Years of Progress, JPL Document 400-279, 5101-279, October 1985.

Summary of FSA Project Documentation: Abstracts of Published Documents, 1975 to 1986, JPL Publication 82-79 (Revision 1), 5101-221, DOE/JPL-1012-76, September 1986.

Upon request, this FSA Final Report (JPL Publication 86-31) and the two supplemental reports (JPL Document 400-279 and JPL Publication 82-79) are individually available in print from:

National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

Abstract

The Flat-Plate Solar Array (FSA) Project, funded by the U.S. Government and managed by the Jet Propulsion Laboratory, was formed in 1975 to develop the module/array technology needed to attain widespread terrestrial use of photovoltaics by 1985. To accomplish this, the FSA Project established and managed an Industry, University, and Federal Government Team to perform the needed research and development.

The primary objective of the Silicon Sheet Task of the FSA Project was the development of one or more low-cost technologies for producing silicon sheet suitable for processing into cost-competitive solar cells. Silicon sheet refers to high-purity crystalline silicon of size and thickness for fabrication into solar cells.

The Task effort began with state-of-the-art sheet technologies and then solicited and supported any new silicon sheet alternatives that had the potential to achieve the Project goals.

A total of 48 contracts were awarded that covered work in the areas of ingot growth and casting, wafering, ribbon growth, other sheet technologies, and programs of supportive research. Periodic reviews of each sheet technology were held, assessing the technical progress and the long-range potential. Technologies that failed to achieve their promise, or seemed to have lower probabilities for success in comparison with others, were dropped. A series of workshops was initiated to assess the state of the art, to provide insights into problems remaining to be addressed, and to support technology transfer.

The Task made and fostered significant improvements in silicon sheet including processing of both ingot and ribbon technologies. An additional important outcome was the vastly improved understanding of the characteristics associated with high-quality sheet, and the control of the parameters required for higher efficiency solar cells. Although significant sheet cost reductions were made, the technology advancements required to meet the Task cost goals were not achieved.

Foreword

Throughout U.S. history, the Nation's main source of energy has changed from wood to coal to petroleum. It is inevitable that changes will continue as fossil fuels are depleted. Within a lifetime, it is expected that most U.S. energy will come from a variety of sources, including renewable energy sources, instead of from a single type of fuel. More than 30% of the energy consumed in the United States is used for the generation of electricity. The consumption of electricity is increasing at a faster rate than the use of other energy forms and this trend is expected to continue.

Photovoltaics, a promising way to generate electricity, is expected to provide significant amounts of power in years to come. It uses solar cells to generate electricity directly from sunlight, cleanly and reliably, without moving parts. Photovoltaic (PV) power systems are simple, flexible, modular, and adaptable to many different applications in an almost infinite number of sizes and in diverse environments. Although photovoltaics is a proven technology that is cost-effective for hundreds of small applications, it is not yet cost-effective for large-scale utility use in the United States. For widespread economical use, the cost of generating power with photovoltaics must continue to be decreased by reducing the initial PV system cost, by increasing efficiency (reduction of land requirements), and by increasing the operational lifetime of the PV systems.

In the early 1970s, the pressures of the increasing demand for electrical power, combined with the uncertainty of fuel sources and ever-increasing prices for petroleum, led the U.S. Government to initiate a terrestrial PV research and development (R&D) project. The objective was to reduce the cost of manufacturing solar cells and modules. This effort, assigned to the Jet Propulsion Laboratory, evolved from more than a decade-and-a-half of spacecraft PV power-system experience and from recommendations of a conference on Solar Photovoltaic Energy held in 1973 at Cherry Hill, New Jersey.

This Project, originally called the Low-Cost Solar Array Project, but later known as the Flat-Plate Solar Array (FSA) Project, was based upon crystalline-silicon technology as developed for the space program. During the 1960s and 1970s, it had been demonstrated that photovoltaics was a dependable electrical power source for spacecraft. In this time interval, solar-cell quality and performance improved while the costs decreased. However, in 1975 the costs were still much too high for widespread use on Earth. It was necessary to reduce the manufacturing costs of solar cells by a factor of approximately 100 if they were to be a practical, widely used terrestrial power source.

The FSA Project was initiated to meet specific cost, efficiency, production capacity, and lifetime goals by R&D in all phases of flat-plate module (non-concentrating) technology, from solar-cell silicon material purification through verification of module reliability and performance.

The FSA Project was phased out at the end of September 1986.

Acknowledgments

The Task gratefully acknowledges the contributions of the many non-Jet Propulsion Laboratory (JPL) technical experts who took part in this program as subcontractors, consultants, workshop participants, and interested friends. Their competence and their enthusiastic support was responsible for much of the accomplishments of the Task.

The Task also recognizes the JPL staff members responsible for the Task and its various elements since its inception 11 years ago. They include: C. Chen, L-J Cheng, J. Collier, G. Cumming, T. Digges, M. Hagan, S. Hyland, K. Koliwad, J. Liu, A. Mokashi, T. O'Donnell, C. Radics, R. Shima, K. Stika, and J. Zoutendyk.

FSA Project Summary

The Flat-Plate Solar Array (FSA) Project, a Government-sponsored photovoltaic (PV) project, was initiated in January 1975 with the intent to stimulate the development of PV systems for economically competitive, large-scale terrestrial use. The Project's goal was to develop, by 1985, the technology needed to produce PV modules with 10% energy conversion efficiency, a 20-year lifetime, and a selling price of $\$0.50/W_p$ (in 1975 dollars). The key achievement needed was cost reduction in the manufacture of solar cells and modules.

As manager, the Jet Propulsion Laboratory organized the Project to meet the stated goals through research and development (R&D) in all phases of flat-plate module technology, ranging from silicon-material refinement through verification of module reliability and performance. The Project sponsored parallel technology efforts with periodic progress reviews. Module manufacturing cost analyses were developed that permitted cost-goal allocations to be made for each technology. Economic analyses, performed periodically, permitted assessment of each technical option's potential for meeting the Project goal and of the Project's progress toward the National goal. Only the most promising options were continued. Most funds were used to sponsor R&D in private organizations and universities, and led to an effective Federal Government-University-Industry Team that cooperated to achieve rapid advancement in PV technology.

Excellent technical progress led to a growing participation by the private sector. By 1981, effective energy conservation, a leveling of energy prices, and decreased Government emphasis had altered the economic perspective for photovoltaics. The U.S. Department of Energy's (DOE's) National Photovoltaics Program was redirected to longer-range research efforts that the private sector avoided because of higher risk and longer payoff time. Thus, FSA concentrated its efforts on overcoming specific critical technological barriers to high efficiency, long life, reliability, and low-cost manufacturing.

To be competitive for use in utility central-station generation plants in the 1990s, it is estimated that the price of PV-generated power will need to be $0.17/kWh (1985 dollars). This price is the basis for a DOE Five-Year Photovoltaics Research Plan involving both increased cell efficiency and module lifetime. Area-related costs for PV utility plants are significant enough that flat-plate module efficiencies must be raised to between 13 and 17%, and module life extended to 30 years. Crystalline silicon, research solar cells (non-concentrating) have been fabricated with more than 20% efficiency. A full-size experimental 15% efficient module also has been fabricated. It is calculated that a multimegawatt PV power plant using large-volume production modules that incorporate the latest crystalline silicon technology could produce power for about $0.27/kWh (1985 dollars). It is believed that $0.17/kWh (1985 dollars) is achievable, but only with a renewed and dedicated effort.

Government-sponsored efforts, plus private investments, have resulted in a small, but growing terrestrial PV industry with economically competitive products for stand-alone PV power systems. A few megawatt-sized, utility-connected, PV installations, made possible by Government sponsorship and tax incentives, have demonstrated the technical feasibility and excellent reliability of large, multimegawatt PV power-generation plants using crystalline silicon solar cells.

Major FSA Project Accomplishments

- Established basic technologies for all aspects of the manufacture of nonconcentrating, crystalline-silicon PV modules and arrays for terrestrial use. Module durability also has been evaluated. These resulted in:
  - Reducing PV module prices by a factor of 15 from $\$75/W_p$ (1985 dollars) to $\$5/W_p$ (1985 dollars).
  - Increasing module efficiencies from 5 to 6% in 1975 to more than 15% in 1985.
  - Stimulating industry to establish 10-year warranties on production modules. There were no warranties in 1975.
  - Establishing a new, low-cost high-purity silicon feedstock-material refinement process.
  - Establishing knowledge and capabilities for PV module/array engineering/design and evaluation.
  - Establishing long-life PV module encapsulation systems.
  - Devising manufacturing and life-cycle cost economic analyses.
- Transferred technologies to the private sector by interactive activities in research, development, and field demonstrations. These included 256 R&D contracts, comprehensive module development and evaluation efforts, 26 Project Integration Meetings, 10 research forums, presentations at hundreds of technical meetings, and advisory efforts to industry on specific technical problems.
- Stimulated the establishment of a viable commercial PV industry in the United States.

Silicon Sheet Summary

Silicon sheet is the primary component of a crystalline silicon photovoltaic (PV) module. The quality and shape of the sheet, as well as the process by which it is produced, influence the fabrication, costs, and efficiencies of solar cells and modules. Because the cost of silicon sheet dominates the overall cost of a PV module, the production of high-quality silicon sheet must be based on low-cost growth processes. The primary objective of the Silicon Sheet Task in the Flat-Plate Solar Array Project was to develop these processes.

The direction of the development has been toward both the reduced use of silicon and other consumable materials and the achievement of high throughput (meter^2/h) and high sheet quality (higher device efficiency). These goals were to be attained within the bounds of an initial add-on price goal of \$18/m^2. This price goal, which did not include the cost of silicon, depends upon the specific process used and its effect on the overall price of the module. Taken into account were the potential trade-offs between solar cell efficiency, sheet production throughput, material use, and other indirect costs associated with the sheet growth process.

As with many other technology development activities, the Task faced a major trade-off between high-risk, high-return opportunities, and those that were more secure and potentially less rewarding. In order of increasing risk, as perceived in the early years of the Project, most of the silicon sheet technology processes supported by the Task can be grouped into the following three options:

Option 1: Ingot and wafering technology.

- Advanced Czochralski (Cz) ingot growth (Kayex, Siltec, Varian, Texas Instruments).
- Ingot casting (Crystal Systems, Solarex).
- Internal diameter (ID) saw wafering (Siltec, Silicon Technology).
- Multiple-blade wafering (Varian, P.R. Hoffman).
- Multiple-wire wafering (Crystal Systems, Solarex).

Option 2: Shaped ribbon growth.

- Edge-defined film-fed growth (EFG) (Mobil Solar).
- Dendritic-web growth (Westinghouse).
- Inverted Stepanov process (RCA).
- Ribbon-to-ribbon growth (Motorola).
- Low-angle silicon sheet growth (Energy Materials Corp.).

Option 3: Silicon coating on low-cost substrates.

- Silicon-on-ceramic dip coating (Honeywell).
- Chemical vapor deposition (GE, Rockwell, RCA).
- Liquid-phase epitaxy (Astrosystems).

Vacuum casting of silicon wafers was supported at ARCO Solar and at SRI International. Advanced development of a commercial and proprietary polycrystalline silicon casting technique was supported separately at Solarex by the U.S. Department of Energy (DOE), and technical direction was provided by the Task.

To develop these technology options, the Jet Propulsion Laboratory (JPL) awarded contracts to industries and universities. Specific research was aimed at understanding the behavior of low-cost silicon sheet based on the characterization of its structural, chemical, and electronic properties. Although this research was performed by JPL and others, the primary role of JPL was to plan, manage, and coordinate Task activities.

The Task was planned to proceed in the following phases: feasibility research and development, advanced development, prototyping, and production development. Because of the great complexity, variety, and novelty of some sheet technology options, the rates of progress varied among the options. Consequently, only those options that evolved most rapidly and offered the greatest promise for high-quality and low-cost sheet received continuing Project support. New process options were considered and supported as they became available.

In addition to studies of sheet technology development, supporting research also was conducted in the areas of:

- Interaction of various materials with molten silicon.
- Development of improved refractory materials to be used in contact with molten silicon.
- Determination of the sources and implementation of the control of stresses and strains encountered during the growth of silicon ribbons. This was a major focus of the Task at the conclusion of the Project.

The redirection of the DOE National Photovoltaics Program in late 1981 shifted emphasis to longer-term, high-risk research. This essentially led to the termination of the prototype and production phases of the original concept, and to the end of the support for nearly all the process option developments except the dendritic-web effort. The latter was judged most promising because of its quality and low cost. None of the technical efforts involving the highest risk (Option 3) were brought to the point of commercial feasibility. This was especially true in view of the need for increased module efficiency that emerged after 1980. Because of the large funding reduction in 1981 and the Project termination in 1986, many promising technical activities are incomplete. Some technical activities have continued with private sponsorship, but at reduced levels of effort. The diverse technical aspects of the Task work are reviewed and summarized in this report.

In spite of the limitations mentioned above, there were many major accomplishment, including:

- Growth of a 150 kg single crystal, Cz ingot (15-cm diameter) from a single crucible at a throughput rate of 2.2 kg/h.
- Casting of a 34 x 34 x 17 cm shaped ingot (35 kg) by the heat exchange method.
- Demonstration of ID sawing of a 15 cm Cz ingot at 17 wafers per centimeter of length of the ingot (0.69 m^2/kg).
- Demonstration of wire sawing of a 10 x 10 cm cast ingot at 25 wafers per centimeter of length of ingot (1 m^2/kg).
- High throughput growth of EFG ribbons (40 cm^2/min; 10 cm wide at 4 cm/min).
- Simultaneous growth of multiple EFG ribbons (five ribbons, each 5 cm wide; three ribbons, each 10 cm wide).
- High throughput growth of high-quality dendritic-web ribbons (13 cm^2/min for short ribbon lengths).
- Demonstration of 8 h dendritic-web ribbon growth at constant melt level.
- Identification of mechanical stress and deformation as a primary limitation to the rapid growth of high-quality silicon ribbons.
- Significant progress in understanding and control of thermal stress/strain effects in high-speed ribbon growth.
- Understanding and modeling of the origin of defects in low-cost silicon sheet and the effects of these defects on electronic transport behavior.
- Development of a ceramic composition (Mullite) whose thermal expansion precisely matches silicon over the temperature range from room temperature to the melting point of silicon.
- The first detailed and comprehensive study of the interactions of various refractory materials with semiconductor-grade silicon.
- The generation of fracture data for silicon and its application to growth and processing of silicon sheet.
- Economic advancements were implemented by the various industrial contractors to reduce their product cost. Detailed information on the specifics of these implementations and their effects of actual cost are proprietary.

The Task efforts led to commercialization of one ribbon option and extensive progress toward the commercialization of another. It also contributed to the commercialization of ingot casting and to the advancement of the Cz growth technique. Work with the Cz growth technique now continues under numerous private development activities. The Task also aided understanding and development of wafering technology, the crystallization process, and the effects of the crystallization process on electronic properties and solar cell quality. Material interactions with molten silicon are now better understood, as are some of the limitations on growth rates and the trade-offs between production rates and quality.

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SECTION I

Introduction

A. BACKGROUND

Despite its simple appearance and uncomplicated structure (Figure 1), a crystalline-silicon solar cell is a sophisticated semiconductor device. Solar cells that convert sunlight into electricity with high efficiency require high-quality silicon substrates with the following precisely tailored physical and electronic properties: low density of structural defects, high purity, long minority-carrier diffusion lengths, and high uniformity. Unlike most semiconductor devices, the cost of a solar cell is highly dependent on the cost of the silicon sheet substrate on which it is fabricated. The solar cell is an area-dependent device, i.e., large solar cell areas are required to produce large amounts of power. To achieve low manufacturing costs, the silicon sheet growth process[1] must be inexpensive and yet not compromise the material quality or its properties with regard to subsequent processability. Processability requires high mechanical strength, low residual stress, and uniform, standard-shaped, flat wafers. The major cost drivers for silicon sheet growth include costs of consumables, throughput rate, labor, and the cost of capital equipment (Appendix A).

In January 1975, the Flat-Plate Solar Array (FSA) Project (then called the Low-Cost Silicon Solar Array Project) was established at the Jet Propulsion Laboratory (JPL) as part of a National Photovoltaics Energy Conversion Program. The objective of this Project was to achieve a major cost reduction in silicon solar array prices by 1986. The FSA Project approach consisted of technology development, industry involvement, commercialization, and market stimulation.

When the FSA Project started, only two silicon sheet types were available in the marketplace: the wafers were sliced from either float-zone (FZ) or Czochralski (Cz) single-crystal cylindrical ingots. These high-cost materials (typically $4 to $5 per wafer) were of a quality (purity and crystallinity) adequate for use by the growing semiconductor industry and for photovoltaics (PV).

The standard semiconductor industry process for silicon wafer manufacture in 1975 included Cz ingot growth, centerless grinding, trimming, wafering by internal diameter (ID) saws, etching, polishing, and cleaning. These steps were expensive, low-yield, labor-intensive, and resulted in an expensive substrate material. This material cost was acceptable when spread out among the many individual semiconductor devices obtained from a single wafer, but was prohibitive for low-cost terrestrial PV applications.

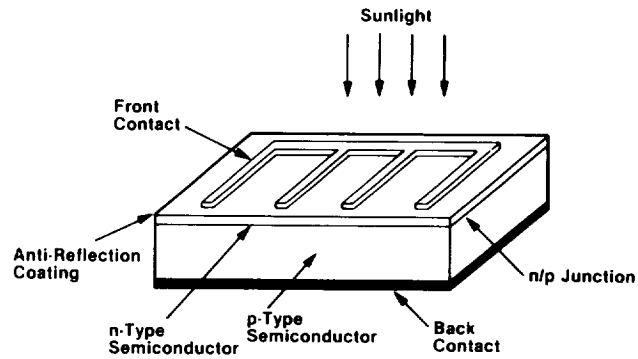

Figure 1. Crystalline Silicon Solar Cell

Cz wafers also were used for space-qualified solar cells in which reliability and performance were the issue, not cost.

Neither of these materials, however, seemed to have a high probability for meeting the low-cost criterion of the new Project. For that reason, alternative silicon sheet processes were sought that had potential for meeting the Task's add-on cost goals. At that time, in the materials community, several innovative sheet growth processes were in the conceptual or early developmental stages. These included ingot growth processes employing directional solidification techniques, and methods to grow silicon in sheet form directly from the melt. The direct sheet-growth processes avoided the costly wafering step altogether. Although the ingot processes yielded a product that required subsequent wafering, they seemed to have the advantage of low process costs.

This report summarizes the 11-year-long activities of the Silicon Sheet Task. The general goal of the Task consistently has been better silicon sheet at lower cost. Specific Task objectives and approaches evolved substantially because of changes in funding level, redirection from the U.S. Department of Energy (DOE), and response to the results of continuing analyses concerning cost and technology trade-offs (Reference 1).

B. INITIAL GOALS AND OBJECTIVES

FSA Project price goals for solar arrays were established on the basis of rated power ($\$/W_p$) and of area of arrays ($\$/m^2$). These price goals were translated into various technology goals in terms of throughput, efficiency, material consumption, and yields appropriate for each process step (see Appendix A).

[1] In this report, the term "sheet" is used to mean silicon in a form suitable for processing into solar cells regardless of whether it was grown in ingot form and subsequently sliced or grown directly from the melt to the desired thickness, i.e., ribbons.

By the time of the first Task Integration Meeting in January 1976, the 1985 FSA silicon sheet goals for price, quality, and throughput had been established. The goals were:

(1) A value-added cost of $<\$18/m^2$ for large-area silicon sheet.

(2) Silicon sheet capable of array fabrication with $>10\%$ energy-conversion efficiency.

(3) Automated sheet production capability of $>5 \times 10^6$ m^2/year.

These engineering and production goals were designed to meet the Project's $\$0.50/W_p$ (1975 dollars) goal. The goals were contingent upon scaling up for commercialization (more machines per operator, better process automation, lower consumables costs, etc.). At this stage, the focus of the National Program and the Project was on developing process technologies that showed technical and economic feasibility, more than on the fundamental technical issues such as developing an understanding of the influence of growth-process-related defects on device performance.

C. EARLY APPROACH/IMPLEMENTATION PLAN

The Task approach and schedule established in 1975 was to pursue evolving technologies in four phases:

(1) Proof of concept and feasibility demonstration (FY 76 to FY 77).

(2) Advanced development (FY 78 to FY 80).

(3) Prototype process development (FY 79 to FY 82).

(4) Scaling up of processes as a transition to automated process development (FY 81 to FY 86).

Phase 1 was to include both theoretical and experimental evaluation of the feasibility of candidate processes to achieve the technical and cost goals of the Task (development of goals commensurate with Project cost goals).

In Phase 2, each technology that had demonstrated technical feasibility was to be analyzed, critical barriers to successful process development were to be identified for directed R&D effort, and technical goals were to be assigned to each process commensurate with Project-derived cost add-on goals.

Phase 3, the Technology Readiness (TR) demonstration phase, was planned to encompass the design, construction, development, and quasi-production demonstration of prototype machines. TR demonstrations were intended to provide operation and cost data to be compared against 1985 goals, and would be used for the selection of processes for the final phase.

Phase 4 was intended to be the operation of a pilot production facility consisting of several machines. This was to develop and demonstrate production capability commensurate with Project goals.

At its inception, the Task elected to support a parallel-path technology development program. It would support, at least through Phase 1, all those technologies perceived as having a potential for achieving the technical and economic goals of the Project. The approach included support, through subcontracts, of R&D of silicon crystal growth methods. It also included in-house silicon sheet characterization and assessment, as well as complementary material and crystal growth studies. In January 1975, an industry briefing and planned solicitation were announced. By August, source selections for the Silicon Sheet Growth Development Subtask were presented. A list of contractors to the Project in January 1976 is given in Table 1. At the outset of the Project, a few of the sheet growth methods had already been in development or operation for some time, while others were only concepts. The status of each of the technologies in 1976 is given in Reference 2.

Table 1. FSA Project R&D and Silicon Sheet Growth Methods 1975 to 1977

Organization	Method
Ribbon growth	
University of South Carolina	Dendritic web
IBM	Shaping capillary die
Mobil-Tyco	EFG
RCA	Inverted Stepanov
Motorola	Ribbon-to-ribbon laser zone melting
Vapor deposition	
Rockwell	CVD
Novel sheet growth	
GE	Floating substrate
Honeywell	Dip coating
Crystal Systems	Heat exchange ingot casting
Ingot cutting	
Varian	Breadknife sawing
Crystal Systems	Wire sawing

Three milestones were defined by the Task to measure the progress of technology development of these sheet technologies against the Project goal of demonstrating Technology Readiness by FY 82 (TR 82). The milestones were:

(1) Simultaneous demonstration of performance and productivity goals assigned to each process. Each process was assigned individual goals based on estimated performance and productivity potentials and the trade-off effect of the variables on performance against Project goals.

(2) Completion of design and fabrication of a prototype Experimental Sheet Growth Unit.

(3) Successful completion of operation of the Growth Unit in a pilot production mode.

The task was not constrained to support only the original subcontractors or technologies. Even as some technologies failed to achieve their promise, others were added, at least to the point of feasibility demonstration. The Cz process, for example, was added to the program in 1977. Four Cz approaches ultimately were supported. The original two wafering options were expanded to four before wafering technology development (TD) was dropped altogether in 1985. Ultimately, the parallel-path TD program included three ingot growth processes, four wafering processes, and nine direct sheet formation processes (Table 2). All technologies supported by the Task are reviewed in the following sections.

In 1979, six FSA-supported technologies were identified as candidates for TR 82. The six represented the three major silicon sheet technology options pursued by the Task: (1) ingot technology represented by the advanced Cz process and the heat exchange method (HEM), (2) supported-film technology represented by the silicon-on-ceramic (SOC) process, and (3) shaped-ribbon technology represented by the edge-defined film-fed growth (EFG) process and the dendritic web process.

In addition to these primary studies of crystal growth and wafering, the Task supported and conducted parallel technological studies to support the primary investigations. These technological studies involved:

(1) In-house determination of the interactions of molten silicon with the various materials that were anticipated to be used in contact with molten silicon.

(2) In-house investigation of the effects of structural defects and their distribution on electronic properties and cell performance.

(3) Subcontracted development efforts to optimize the performance determined by the in-house investigations of mechanical behavior of silicon in crystallization and the finished sheet.

*Table 2. Total Parallel-Path Technology Development Program for Silicon Sheet**

Ingot Growth
Czochralski (Cz)
Heat exchange method (HEM)
Semicrystalline casting (SEMIX)
Wafering
Fixed abrasive internal diameter (ID)
Fixed abrasive multiple wire (FAST)
Free abrasive multiple wire
Free abrasive multiple blade
Direct Sheet Formation
Vacuum die casting
Ribbon-to-ribbon (RTR)
Dendritic web
Edge-supported pulling (ESP, ESR)
Shaped ribbon growth (EFG, CAST)
Low-angle silicon sheet (LASS)
Floating substrate
Silicon on ceramic (SOC)
Inverted Stepanov
Support Technologies
Die and container materials studies
Theoretical studies on heat flow, interface stability, mechanical properties, stress and strain in ribbon growth
Abrasion analysis in various chemical environments
Development of analytical tools (moire pattern Interferometric analysis of residual stress in ribbons, etc.)
Miscellaneous
Deformation processing

*This work included both subcontracted and in-house R&D efforts.

(4) Additional appropriate subcontracted and in-house studies.

In 1981, the Task initiated a series of Project workshops and research forums beginning with the Low-Cost Solar Array Wafering Workshop. The objectives of the Wafering Workshop were to clarify and define the state of the art of ingot wafering, to define the requirements for future work, to solicit and explore innovative ideas, and to stimulate a productive exchange of technology within the technical community. The Workshop accomplished these objectives. But major developments clearly were needed to achieve the Project economic goals.

This approach to problem solving and technology transfer was followed by other major technical workshops dealing with growth and characterization of crystals for solar cells as well as a continuing series of mini-workshops on the problem of stress and strain in high-speed ribbon growth processes (Table 3).

Table 3. Silicon Sheet Task Technical Workshops and Research Forum *

Low-Cost Solar Array Wafering Workshop, June 8-10, 1981, Phoenix, Arizona
Flat-Plate Solar Array Project Research Forum on the High Speed Growth and Characterization of Crystals for Solar Cells, July 25-27, 1983, Port St. Lucie, Florida
Flat-Plate Solar Array Project Workshop on Crystal Growth for High-Efficiency Silicon Solar Cells, December 3-4, 1984, San Diego, California

*In addition to the above, four mini-workshops were held on stress/strain in silicon ribbons.

D. PROJECT REDIRECTION

The first redirection came from DOE late in 1981. It specifically supported a research thrust to address the fundamental barriers to achieve the Task goals, in contrast to emphasis on TD for commercialization. The second redirection came in 1985 and redefined the sheet performance goals to meet the new energy-conversion efficiency requirement for utility-projected modules of 15 to 17% at air mass (AM) 1.5. The new specifications for sheet suitable for fabrication into high-efficiency solar cells were established by the Task to be 0.1 to 1 Ω-cm, zero-D (e.g., $<10^3$ to 10^4 dislocations per square cm) 250- to 500-μm minority carrier diffusion length, controlled impurities (oxygen, nitrogen, carbon), processable shape, and low residual stress. Ribbon stress problems became apparent only when ribbons were grown wider and faster. These remained the goals of the Task until its phaseout at the end of FY 86.

The impact of the budget reductions and changes in program emphasis included the phaseout of technologies perceived to be ready for commercialization (the wafering and ingot TD programs),[2] and the focusing of research efforts and funding for the ribbon and support technologies onto generic topics and critical elements of specific sheet growth processes.

As part of its in-house research and test and verification work, the Task at JPL had built up research facilities during the first 6 years of the TD program. Materials and device characterization, device processing, and crystal growth laboratories already were in place and operational in 1982 when the Project focus was redirected. Thus, intensive research could be performed at JPL addressing generic problems and topics of critical importance to the successful development of the sheet technologies.

A discontinuity occurred in 1982 when funding for all technology options was substantially reduced. Not only were the ingot and wafering processes dropped, but the ribbon options also were narrowed. This reduced funding and also reduced the probability of technical success for the remaining processes.

In 1983, DOE issued its Five-Year Research Plan for the National Photovoltaics Program (Reference 3). The plan cited the success of the U.S. Government/industry partnership in the development of the ingot-based single-crystal silicon technology on which the then emerging PV industry was based. It reiterated the Federal role "to undertake research activities with the potential for achieving long-term benefits in areas that industry is unlikely to pursue because of the costs and risks involved." It further stated that "The Program, in response to industry's need, is working to resolve the critical problems which currently limit the improvement of crystalline silicon technology." The goal, established for the Task, was to "resolve generic impediments to improve ribbon growth speed and quality in different environments." The goal was scheduled for completion by the end of CY 85. The resources that were made available to achieve this goal, however, were considerably less than those estimated to be required (Figures 2 and 3).

In February 1984, at the request of DOE, the FSA Project issued a Crystalline Silicon Implementation Plan to respond to the DOE's Five-Year Plan (see Reference 3). In the Implementation Plan, the Task goal is unchanged from the goal stated in the Five-Year Plan. The generic problems that must be understood better to achieve successful ribbon growth TD are identified as the problem of stress and strain in high-speed growth of ribbons and the relationship between growth parameters and solar cell performance.

[2]Wafering and ingot technologies were not yet ready to stand on their own to meet commercially the low-cost needs of the PV community. Although several paths for possible R&D development in ingot wafering were identified at the Workshop, no continued R&D then was supported by industry. The Defense Advanced Research Projects Agency (DARPA) today is supporting an effort in fixed-abrasive slicing technique (FAST) development. The state of the art in wafering and ingot technologies is virtually unchanged since 1982. The inability of the wafering technologies to reach their goals by 1982 effectively prevented further consideration of the ingot technologies. The Cz ingot growth process has advanced only incrementally since 1982. The FZ process, which yields the highly perfect wafers on which all devices with the highest reported efficiencies have been fabricated, still remains unexplored for low-cost terrestrial PV application.

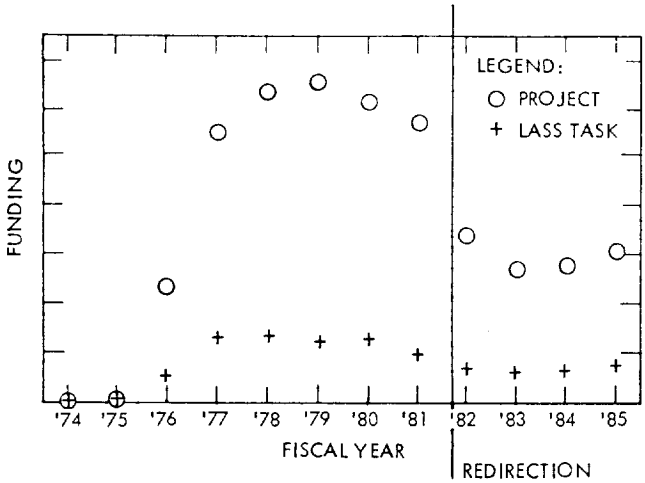

Figure 2. Funding History for Flat-Plate Solar Array Project and Large-Area Silicon Sheet Task

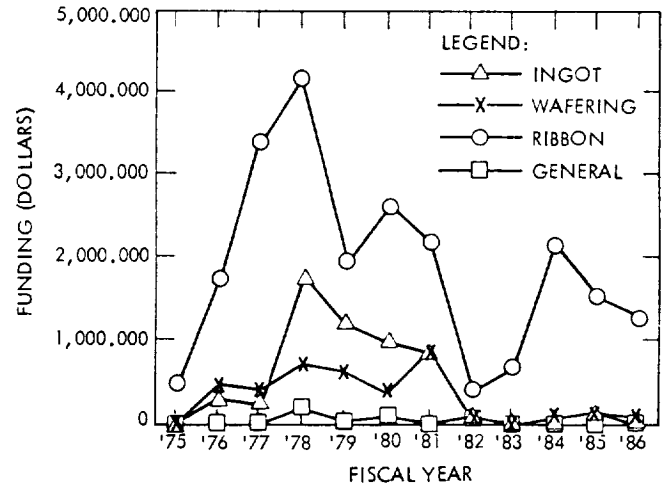

Figure 3. Funding History for Silicon Sheet Technology (Flat-Plate Solar Array Project Contracted Effort)

Because analyses by utilities were placing higher performance requirements on the modules to enhance the feasibility of central station photovoltaics (Reference 4), the potential device efficiencies of the candidate sheet technologies became important selection criteria. In 1985, the Task objective in terms of silicon perfection and properties was redefined because of the high module-efficiency requirements (15 to 17% AM1), projected by the Electric Power Research Institute (EPRI) and JPL. Dendritic web ribbon became the prime sheet candidate because of its crystalline perfection and, therefore, potential for fabrication into high-efficiency devices. The Implementation Plan proposed that dendritic web research continue to be funded at Westinghouse. The goal was to demonstrate a 15 cm^2/min throughput rate of ribbon yielding 14.5% efficiency average cells by mid-FY 85. It also was proposed that a second dendritic web contractor be supported to accelerate the rate of development and increase the probability of technical success; interest was solicited in the industry without success. JPL was chosen as the second contractor because of its demonstrated capability in the field of remote sensing and its familiarity with dendritic web technology and the Project. The purpose of the "Web Team," established at JPL, was to support the Westinghouse effort and increase its probability of success. The "Web Team" was independently to develop sensing and control tools to be transferred to Westinghouse when developed. The plan anticipated that growth-process verification would be completed by the end of FY 86, and that an Advanced Silicon Sheet Summary Document would be issued by early FY 87. The achievements of the Westinghouse and JPL teams are summarized in Section IV.B.2.

Because these new requirements placed severe constraints on most of the silicon sheet materials under development, interest has been renewed in the potential for high-quality Cz or FZ silicon wafers.

When Project wind-down activities were begun, limited time and funding prevented substantive changes in the approach or plan of the Task.

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SECTION II

Ingot Technology

A. INTRODUCTION

At the inception of the Project and the Silicon Sheet Task, the operational sheet technology was ingot growth and wafering. Although mature and effective for the semiconductor industry and then-existing solar cell production, this combination of growth and slicing was perceived to be too costly and wasteful of purified silicon material. Initial FSA Project efforts emphasized sheet preparation by direct growth of thin silicon sheets, as indicated by Table 1. However, continuing in-house analysis of costs of Cz crystal growth suggested that ingot technology could meet Project goals with the aid of numerous technical advances, and that wafering technology (Section III) could also reach the cost goals with technical improvement.

Specifically, it was seen that the small-batch processing limit on crystal growth could be challenged. The production of multiple Cz ingots from a single crucible and crystal-grower run and the growth of large crystals at faster rates was considered. Beginning in 1977, four contractors (Kayex, Siltec, Texas Instruments, and Varian) addressed these Cz-improvement options, with varying approaches and degrees of success, as described in Section II.B.1.

Alternative ingot technologies to the Cz growth method were also explored: the Heat Exchange Method (HEM) of Crystal Systems Inc., and the Ubiquitous Crystallization Process (UCP) of the Solarex Corp. (supported under a cooperative agreement with DOE, with FSA technical cognizance). The UCP effort also included wafering activities, some described in Section II.B.3 and others as a part of the Wafering Section (see Section III).

Another alternative ingot technology in service at the outset of the Project, FZ crystal growth, was deliberately not selected for development support because of a general perception of the limitations of this process step and its products. Although of high purity, and capable of being processed into high-quality wafers and high-efficiency solar cells, FZ silicon wafers are soft (because of low oxygen content) and limited to small diameter. Thus, both processability and manufacturing cost are adversely affected.

In addition to wafering, several other FSA studies supporting bulk crystal growth were performed. A study of heat flow in Cz crystals was carried out by investigators at Washington University at St. Louis. Work relevant to molten silicon/container chemistry is discussed in Section VI.B.1. Studies of the role of gas environments on silicon crystal growth were a consideration in a variety of programs, specifically including those of EFG growth, Cz (Kayex), and materials (University of Missouri).

At JPL, a small in-house program was supported to produce specialized Cz crystals for research applications. Emphasis was placed on unusual crystal orientations (such as <110>), controlled bi-crystals, unusual dopants, and dopant levels.

The Cz growth TD effort was terminated in 1982 as part of the Project redirection. Since 1982, outside of FSA, commercial Cz processes have been continuously upgraded. Interest in continuous silicon ingot growth presently is enjoying a resurgence. Numerous totally automated pullers now are available in the marketplace, 20-cm-diameter ingots are routinely grown by silicon producers, and the introduction of magnetic fields to inhibit melt convection has resulted in more uniform, controlled-oxygen-content crystals.

B. IMPLEMENTATION

1. Czochralski Crystal Growth

The Cz method produces a cylindrical ingot of single-crystal silicon by slowly withdrawing (pulling) a silicon "seed" of the appropriate crystallographic orientation from a pool of molten silicon in a quartz crucible. In 1977, four research teams (Texas Instruments, Varian, Siltec, and Kayex) were selected to perform TD programs aimed at reducing the cost of Cz-grown silicon ingot. Two major drivers of the cost of Cz ingots were the cost of the quartz crucible and the low throughput rate of the process (Reference 5). Thus, the goals of the subcontracted programs included the development of continuous growth processes (more silicon crystals from a single crucible) and increased process throughput rates.

a. *Kayex Corp.: Continuous Czochralski Growth.* The approach taken by Kayex Corp. in 1977 was to modify existing commercial Kayex ingot-growth equipment to pull multiple, batch-recharged, larger-diameter crystals from a single crucible. The original goals of the program included:

(1) Continuous growth of 100-kg ingots of single-crystal silicon from one common container. State of the art at that time was 25 kg from one container.

(2) A growth rate of 20 cm/h instead of the then available capacity of 5 cm/h.

(3) An ingot diameter of 10 cm (4 in.) as compared to the 7.5-cm-diameter ingots then available.

From October 1977 through April 1982, Kayex performed a TD effort involving the continuous

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process scale-up (References 6, 7, and 8). The goals evolved as the process developed and as Project goals and DOE guidelines changed (Table 4). Late in the effort, the work at Kayex included research on more fundamental problems of Cz growth such as the role of gas composition in the growth chamber. This Cz TD effort, the most successful of the Cz work supported by the Project, resulted in the design and commercial production of a new generation of automated, batch-rechargeable, 15.0-cm-diameter, silicon ingot-growth systems.

From October 1, 1977 through March 31, 1980, "Continuous Czochralski Growth" was a two-phase TD contract. The specific objective of Phase 1 was the growth from a single crucible of a 100-kg single-crystal ingot with a diameter of 10 cm or greater. The goal of Phase 2 was the growth of a 150-kg, 15-cm-diameter, single-crystal ingot from a single crucible. To achieve these objectives, Kayex initiated a program of equipment design and development, process R&D, characterization, data analysis, and economic analysis.

The redesigned Kayex CG-1000 commercial puller featured a 20-torr operating pressure with continuous argon purging, a flapper isolation valve between the growth and upper chambers of the system to allow ingot removal, a reseeding capability, a recharging capability without cooldown of the crucible and growth chamber, and recharge mechanisms for both solid polycrystalline rod or lump material. Redesign included scale-up (for both) from a 30-cm to a 35-cm (14-in) crucible, and incorporation of a bead-chain pull mechanism. Two growth runs, each greater than 150 kg, successfully were demonstrated. During the performance period, six 25-kg ingots were pulled from a single 35-cm crucible in the modified system redesignated as CG-6000.

The process development effort included development of multiple ingot growth from a single container, recharging of crucibles while at operating temperature, and the growth of larger diameter ingots (10 and 15 cm) from the larger crucibles. A significant effort also focused on understanding the influence of the atmosphere of the growth system on crystal quality. The multiple ingot growth technique required successful development of both the above hardware and the recharging technique. For the recharge process, the lump recharge methods prevailed because of problems experienced with the solid rod recharge approach and the successful design of a novel hopper for lump feed. A successful dopant recharge system also was developed to maintain the consistency of the electronic character of succeeding ingots.

The scale-up to 10.0-, 12.5-, and 15.0-cm crystals was economically motivated. Throughput, and therefore cost, is extremely sensitive to ingot diameter, and increase in ingot diameter is not limited by the more fundamental barriers to high-speed linear growth. Although the contract goal of a 20-cm/h linear growth rate successfully was demonstrated for selected crystals during the contract period, the maximum overall growth rate observed during a 100-kg run was 8.7 cm/h.

The furnace-atmosphere study emphasized the identification and elimination of sources of impurities that could end up in the melt and result in deterioration of ingot quality. The silicon material etching process, the bake-out procedures for the graphite furnace components, and other sources of volatile impurities were reviewed and remedied. A residual gas analyzer (RGA) was used to monitor the CO concentration (correlated directly with SiO concentration) in the system atmosphere during the growth runs. SiO and CO are believed to be elements of an impurity transport couple ultimately responsible for degradation of crystal quality. In a typical growth run, the CO level rose dramatically during meltdown, dropped during the melt-stabilization period, and gradually increased during the growth period. The RGA also detected air and water leaks in the system.

Table 4. Goals of the Kayex Corp. Czochralski Ingot-Growth Program

Parameter	Contract 954888 Oct 1977	Contract 954888 Mar 1980	Contract 955270	Contract 955733 Apr 1982
Continuous growth total (kg)	≥100	≥150*		50.0
Growth rate of length (cm/h)	≥ 10	≥ 10	≥10	15.0
Diameter (cm)	≥ 10	15	15	15.0
Ingot yield after growth and before trimming (%)	90			>90.0
Throughput (kg/h)				> 2.5
Cell performance (% AM1)				>14.0

*Six ingots, each 25 kg, from a single crucible.

Kayex also performed an extensive study of the influence of crucible devitrification and erosion on crystal quality. The vitreous quartz containers were suspected as the source of impurities or of SiO_2 particles responsible for loss of ingot structure. Although state-of-the-art crucibles were shown to be impure and clear evidence of crucible degradation was developed, the direct influence of the crucible on crystal quality was not determined. Based upon the devitrification rate, crucible lifetime was extrapolated to be >100 h.

Solar cell performance was used as the final measure of crystal quality. Data from 2 x 2 cm baseline cells, fabricated and tested by Applied Solar Energy Corp. (ASEC), were used to evaluate the baseline growth process, to evaluate the influence of extended growth runs involving larger single crystals and multiple crystals from a single crucible, and to test the usefulness for devices of wafers with degraded structure. Typical results are given in Figure 4. Triangles represent single-crystal material and show no appreciable degradation after >80 kg of growth. The squares represent polycrystalline cells and, although no degradation is observed relative to total material grown, the performance of the polycrystalline material clearly is inferior to that of the single-crystal cells.

In 1979, a series of unique short-term, high-risk, accelerated TD contracts was awarded in parallel with the work continuing according to the Project plan. These contracts were funded by a special Congressional appropriation and are known as the "Tsongas" contracts. One of them was the JPL contract, "Low-Cost Czochralski Crystal Growing Technology," awarded to Kayex. Its purpose was the short-term cost reduction of the Cz process by:

(1) Adaptation of "cold-crucible" technology to recharge the continuous Cz growth process.

(2) Development of microprocessor control to increase yield and throughput.

(3) Use of radio frequency (RF) heating and a water-cooled heat sink in the growth chamber to accelerate both melt-in and crystal-pulling rates.

During the 18-month course of the contract, the process of melt recharging by the cold-crucible technique was developed only through the bench test stage. This system featured an RF premelter/levitator that delivered high-purity liquid silicon to the growth crucible, without the silicon contacting the delivery system. Successful bench testing was demonstrated, but the process was never adapted to, and demonstrated in, the crystal-growth system. The programmable microprocessor controller was used successfully to control the diameter of a crystal for a limited period of time. The developments of hardware and software to control meltdown, dipping, growth of the shoulder, and tailing, all of which were to be part of the program, were not achieved during the performance period. The use of RF heating and water cooling to accelerate the process was unsuccessful. The buildup of SiO on the coils interfered with the process, and the effort was terminated.

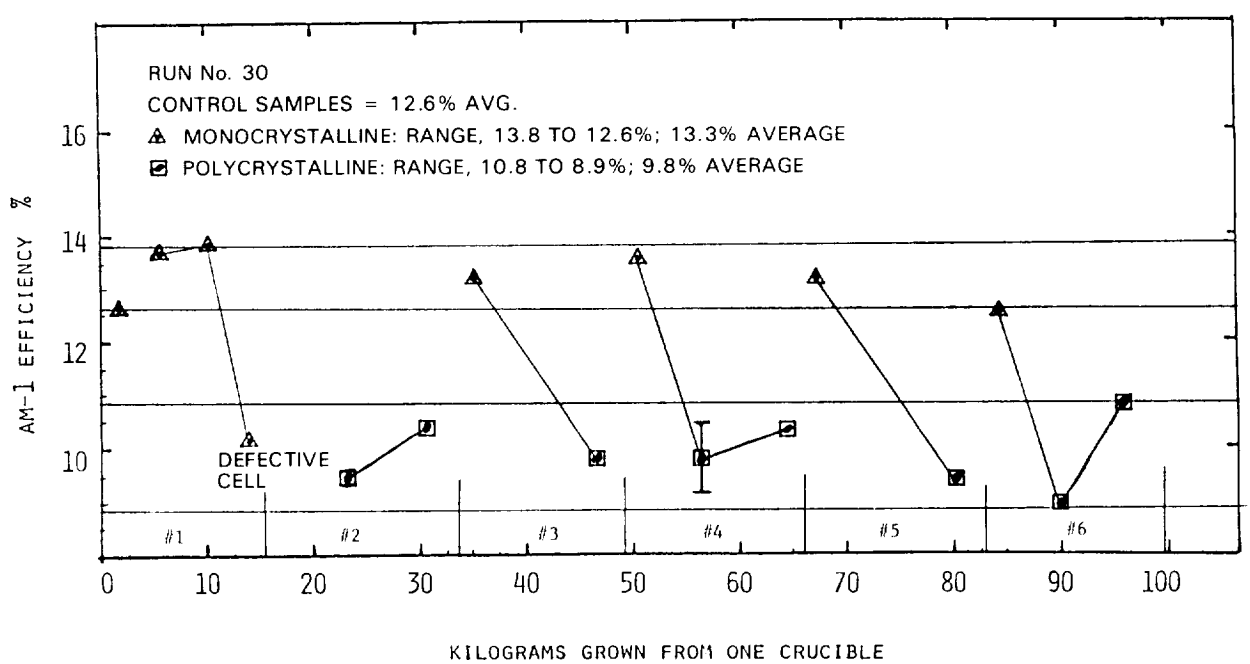

Figure 4. Solar Cell Efficiency Versus Kilograms of Silicon Grown

Two accomplishments of the program are noteworthy:

(1) The microprocessor work became the foundation upon which a very successful automated growth process control system ultimately was developed partly under a JPL contract, and partly with Kayex internal funding.

(2) A conical molybdenum heat shield was developed that is placed above the melt in the crucible. It results in accelerated melt-in and crystal growth rates by effectively reducing heat loss from the melt surface and establishing a steep thermal gradient above the melt.

The Project undertook to support the further development of the commercial Cz process to achieve lower costs and higher throughputs. To achieve the cost goal of the FSA Project, the following program goals were established:

(1) Continuous growth from one common crucible, with melt replenishment, of 150 kg or more of multiple ingots, each approximately 30 kg in weight.

(2) All crystals should have a resistivity of 1 to 3 Ω-cm, p-type.

(3) Dislocation density of $\leq 10^4/cm^{-2}$.

(4) Diameter of 15 cm for each ingot.

(5) Growth throughput ≥2.5 kg/h of machine operation.

(6) Crystal orientation <100>.

(7) After-growth yield of ≥90% of the as-grown crystal.

(8) Development of prototype equipment suitable for high-volume silicon production that is transferable directly to industry.

Modifications (to a Kayex CG-2000 puller) included microprocessor process automation, >25 kg/h accelerated chunk silicon recharge/melt-in capability, and a radiation shield to help accelerate the product throughput to >2.5 kg/h. A study of the influence of process parameter variation on crystal quality was included in the program as well as a demonstration of equipment and process capability. The latter included the requirement that five consecutive runs produce a minimum of 150 kg of good-quality silicon material by pulling a maximum of five ingots, each of 15 cm diameter and of 30 kg weight, at a growth throughput rate of 2.5 kg/h from a single crucible, with the melt-replenishment procedure developed previously.

Six months into the program, the FY 81 funding was reduced and the contract was extended 6 months through March 1982.

The new prototype crystal grower (Figure 5), designated Mod CG-2000 during the program, was offered with slight modification commercially as the CG-6000 at the completion of the program. The new baseline machine featured improved hot-zone design with up to 40-cm- (16-in.-) diameter crucible capability, improved crucible and seed rotation mechanisms and seals, improved chamber design to reduce the chance of water leaks, a larger power supply (150 kW versus 125 kW), a molybdenum heat shield/purge cone, modular construction, and a modified control console to interface with the Kayex Automatic Grower Logic (AGILE) computer control system. Construction and trial testing of the Mod CG-2000 was completed in April 1981. During subsequent process development testing, a growth run was made in which five 30-kg crystals were pulled, totaling 145.5 kg. The first two crystals were 90 and 65% dislocation-free, respectively, but the subsequent crystals were dislocated.

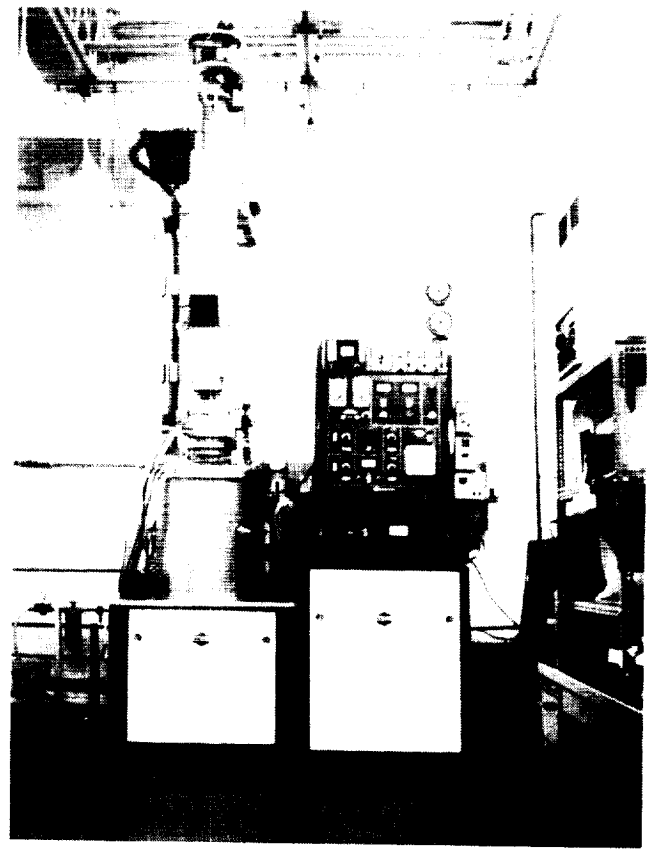

Figure 5. Kayex Prototype Crystal Grower (Model CG-2000)

The program then was revised by direction from JPL. The number of 150-kg demonstration runs was reduced in favor of:

(1) Increasing throughput, especially through use of a radiation shield.

(2) Development of the microprocessor control system.

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(3) Study of the interaction between the furnace atmosphere and the crucible/melt.

(4) Evaluation of the possible use of synthetic-quartz crucibles. (The cost of such crucibles, either bulk or synthetic-quartz-lined, was prohibitive.)

A molybdenum cone radiation shield, supported by a graphite ring and legs, was designed to stand on the top heat shield ring. The cone extended up to the furnace tank cover and down into the crucible. Using this conical shield, accelerated growth rates up to 20 cm/h were achieved. Additional advantages obtained from using the shield included the growth of crystals free from oxide coating and simplified melt-in due to the shield's funneling of silicon chunks toward the center of the crucible.

The most significant single achievement of the Kayex program was development of the hardware and software to automate the growth process. Sensors were developed to measure melt temperature, ingot dimensions, and melt level to support automation of seed dipping, termination of crown growth and shouldering, ingot diameter control, and melt level control. The proprietary Kayex AGILE control system was joined to the Mod CG-2000 to complete the control loop.

The AGILE computer-based control system, a Kayex Corp. proprietary development, not only contains a control loop for setting and stabilizing the melt temperature prior to seed dip, but also the logic to control the growth of the neck, shoulder, body, and tail of the ingot. The system reduces the responsibility for continuous monitoring by the operator as well as the operator's freedom to vary arbitrarily growth process conditions during the run. The result is the reproducible growth of more-perfect crystals. Operation of the integrated system successfully was demonstrated by growth of four 10-kg crystals from 12-kg melts using identical process parameters. Two of the crystals are shown in Figure 6.

The purpose of the gas analysis program was to determine the effects of process parameters on the furnace atmosphere. This would relate process parameters and furnace atmosphere to characteristics of the crystal. A new gas analysis system was designed consisting of a modified ethylene gas analyzer sensitive to low levels of CO and hydrogen, a continuous oxygen monitor, and a hygrometer that could be used to provide continuous data to monitor water vapor levels. Completion of the entire gas analysis system was extended because of a reduction in funding. During testing, the oxygen monitor was found unsatisfactory and was removed from the system. The final system was capable of monitoring hydrogen, carbon monoxide, and water vapor.

A characteristic plot of hydrogen and CO concentrations as functions of time during a crystal growth run is shown in Figure 7. The overall pattern was similar for all growth runs with details changing as run details changed. In one case, continuous monitoring provided real-time evidence of a major air leak that was remedied during the growth run. Minor air leaks were lost in the signal noise. Use of the analyzer provided valuable insight into the requirements for the graphite, hot-zone hardware, bake-out process. Monitoring of the water vapor and CO concentrations in the furnace during the bake-out of new

Figure 6. Ingots Grown with AGILE Control, 100-mm-Diameter, 10-kg

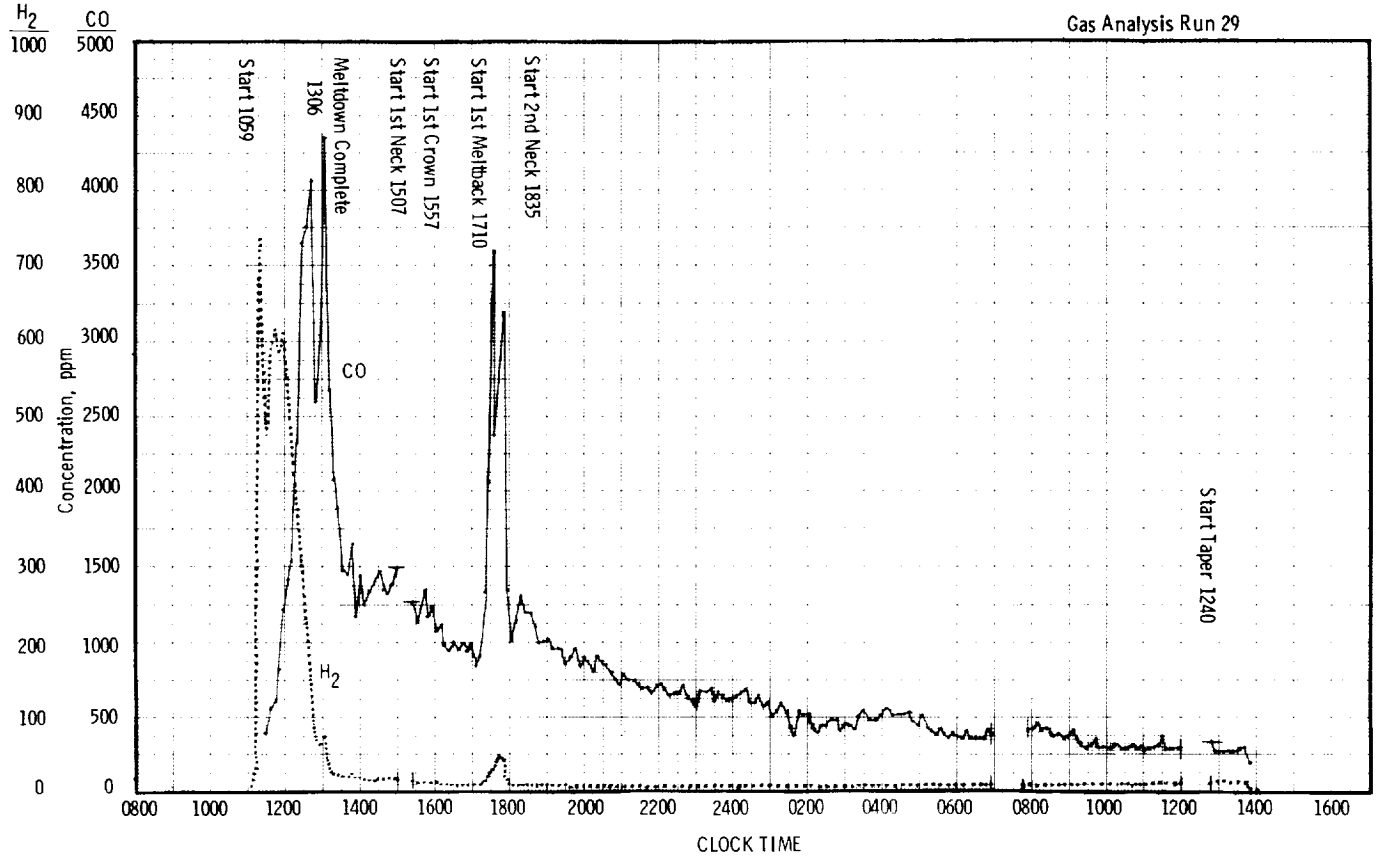

Figure 7. H_2 and CO Concentrations During Crystal Growth Run 29

parts indicated a 3-day bake-out (5 to 7 h/day) was necessary to reduce the production of CO and hydrogen during the heat-up. Lower water vapor and CO concentrations typically are seen in the bake-out of used graphite setup parts.

In 1982, as part of the Project redirection by DOE, the Cz crystal growth TD effort was terminated. At Kayex, all of the contract goals were achieved individually (e.g., growth rate, throughput, yield, etc.), but not simultaneously.

The Mod CG-2000 prototype puller was shipped to Arizona State University where it has been set up to continue scaled-up silicon crystal growth TD with alternative sources of funding. The Kayex CG-6000, a modified Mod CG-2000, is commercially available and is being used for the production of silicon ingots for solar cells.

Key Accomplishments. The key accomplishments of the Kayex Corp. R&D are:

(1) Development of the hardware and software for automating the growth process.

(2) Demonstration of the growth of 150 kg of 15-cm-diameter ingots from one quartz crucible.

(3) Development of a conical molybdenum heat shield located above the melt. It resulted in accelerated melt-in and crystal growth rates.

(4) Development of a multiple growth process for large ingots from one container. This included development of a method to recharge crucibles with chunks of silicon while at operating temperature. Large-diameter ingots (up to 15-cm diameter) were grown. Five 30-kg ingots were grown in a single growth run.

(5) Demonstration of no appreciable degradation in the performance of solar cells made from silicon obtained from extended growth runs of multiple ingots from a single crucible after 80 kg of growth.

Present Status. The Kayex CG-6000 Cz ingot puller with automatic controls is a modification of the puller developed under FSA Project support. It is available commercially and is being used in industry for production of silicon ingots for solar cells.

b. *Siltec Corp.: Continuous Liquid Feed Czochralski Method.* Beginning in December 1977, the Siltec Corp. was funded by the Task to develop the continuous liquid feed (CLF) Cz ingot growth process. Progress on this continuous ingot growth method is summarized in this section and reported in detail in contractor quarterly reports (Reference 9).

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The new CLF concept proposed by Siltec involved a dual-chamber Cz growth system. Silicon feed material, in the form of chunks of polycrystalline ingot, continuously is fed into the hot zone of one furnace chamber and melted in a quartz crucible. The molten silicon then is transferred by a pressure differential through a heated transfer tube into a second furnace chamber from which it is concurrently withdrawn as a single-crystal silicon ingot using the Cz process. The dual-chamber system includes melt-level control in the second chamber by a closed-loop system that senses the melt level and controls the rate of melting in the first chamber (Figure 8).

The original contract called for the design, development, and fabrication of a CLF growth furnace, theoretical analysis of the process, and evaluation of the completed system. Evaluation was to include demonstration of nonreplenished Cz growth, meltdown in the first chamber, and melt transfer. Ultimately, the evaluation was to include three 100-kg runs each made up of five continuously replenished 20-kg ingots.[3] The growth process parameters also were to be evaluated by characterizing the quality of the CLF silicon sheet product through the fabrication and testing of solar cells.

By 1979, the furnace (Figure 9) had been designed and fabricated, and initial liquid silicon

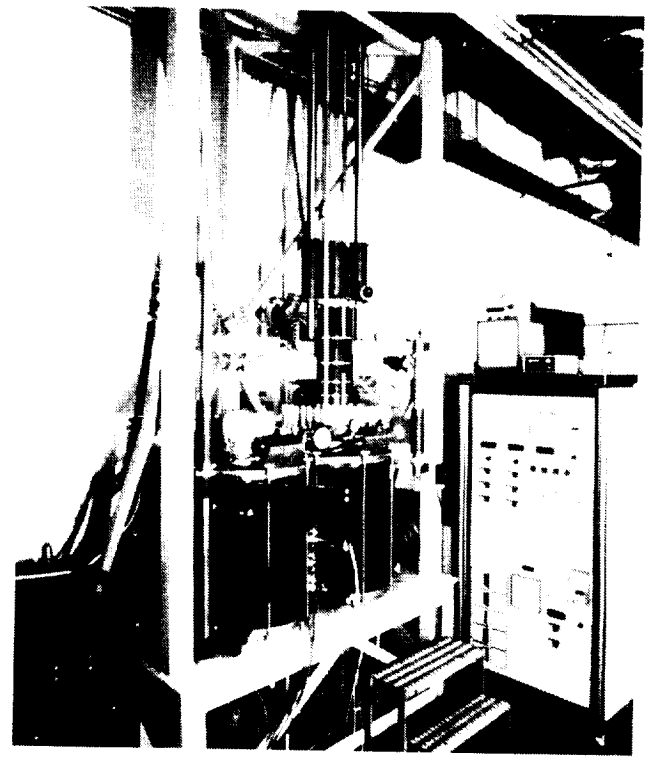

Figure 9. Siltec Furnace for Continuous-Liquid-Feed Growth

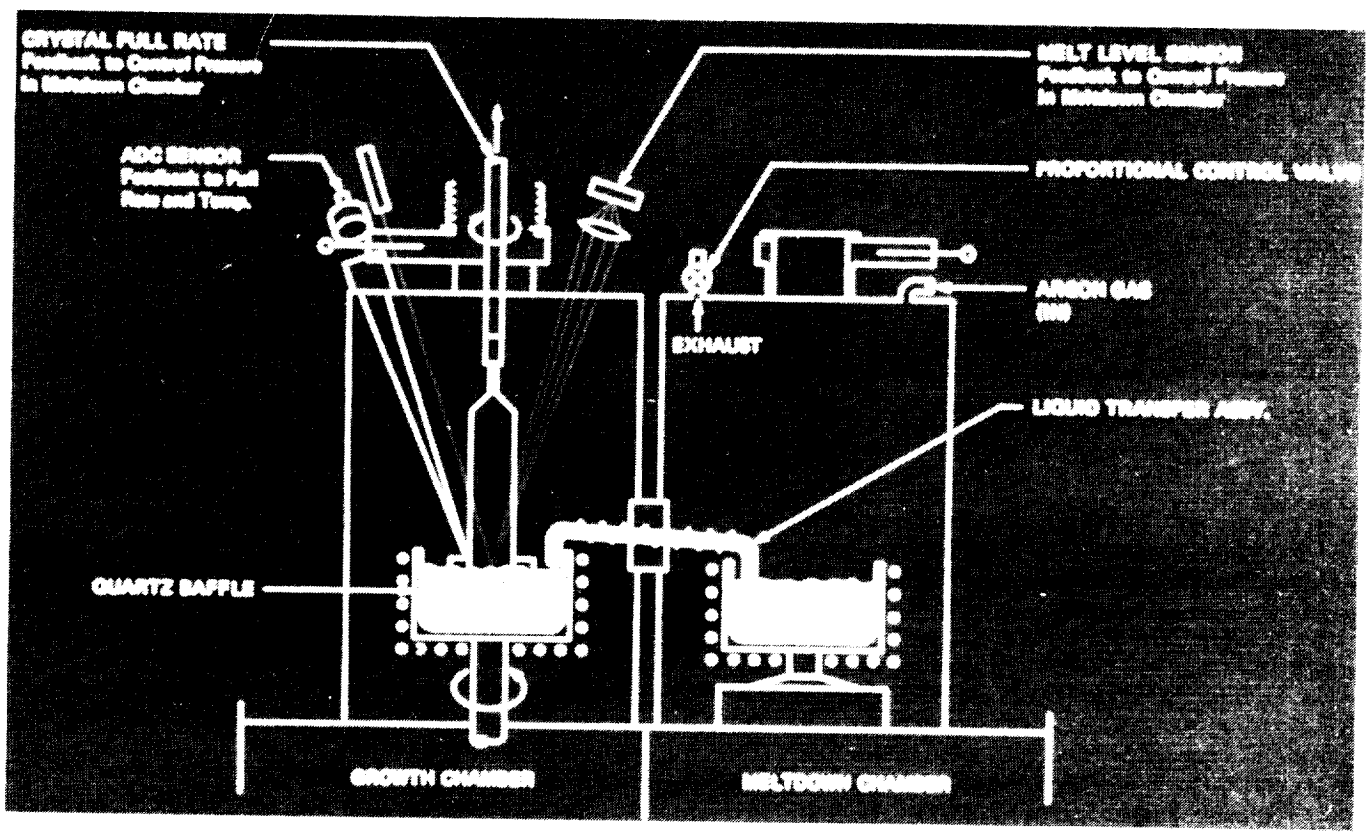

Figure 8. Schematic of Siltec Continuous-Liquid-Feed Czochralski Ingot Growth Process

[3]The goal of 100 kg for each continuous CLF run was based on a Task analysis that indicated this was the minimum yield required to achieve the 1982 cost goal (see Reference 5).

transfer had been demonstrated. Some operational shortcomings had been encountered, however, and further cost analysis had indicated that continuous runs yielding more than the 100-kg goal of the initial contract would be required to achieve the 1986 cost goals of the FSA Project.

A June 1979 contract extension and modification called for redesign and improvement of the transfer tube, design and fabrication of an automated silicon-particle feed-hopper system, and modification of the furnace to operate under reduced pressure. Most importantly, the contract called for two demonstrations each of 150 kg of 15-cm-diameter single-crystal silicon (six ingots each of 25 kg from a single crucible) grown by the continuous CLF Cz growth method. By October 1979, Siltec had demonstrated successful furnace operation and liquid transfer at 30 to 35 torr and had grown, on their third effort, a 10-kg, 12.5-cm-diameter by 32.5-cm-(13-in.-) long, zero-defect silicon ingot (Figure 10). (The silicon transfer tube is seen to the left of the ingot.) By February 1980, however, numerous technical difficulties were encountered with the growth system. These included melt vibration caused by the vacuum pump, SiO_x falling onto the melt surface and interrupting the growth process, and, most critically, repeated transfer tube failure.

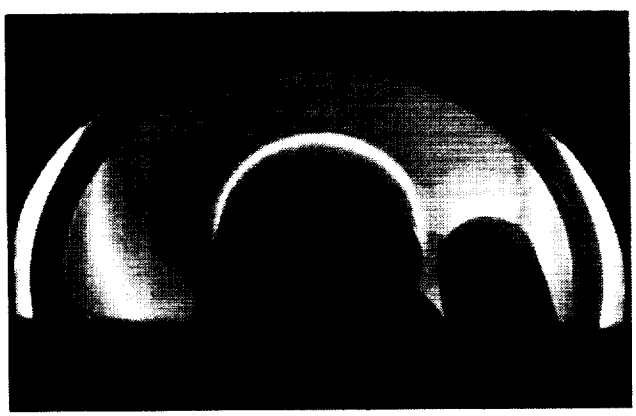

Figure 10. Growth of Silicon Ingot by Continuous Liquid Feed

In March 1980, a new transfer tube design was successfully demonstrated and the Siltec contract was extended. The goals of the extension (Phase 3) called for two 150-kg scale-up feasibility demonstration runs by July 1980. All original goals of the program remained unchanged, including a growth throughput rate of 2.5 kg/h, ≥90% yield of high-efficiency cells (≥15% AM1) to be fabricated from the sheet, uniform resistivity from ingot to ingot, etc. An additional 15 months were added for the design, construction, and demonstration of a prototype production puller (Phase 3) and 10 demonstration growth runs. Initiation of Phase 3 depended on successful completion of Phase 2.

By April 1980, Siltec had successfully demonstrated the following individual accomplishments: 70 kg of ingot up to 15 cm in diameter from one crucible, 2.5 kg/h growth rate, 85% yield, 14% solar cell efficiency, and 1 kg/h growth rate average for 70 h. Because of Siltec's inability to achieve the required contract deliverables and Project budget restraints, however, the CLF TD effort was reduced. A final maximum throughput demonstration of the process at Siltec was the growth of a boule 65 kg in weight, 15 cm in diameter, and about 1.5 m in length (Figure 11). The first 30 cm of growth was single crystal, the remainder being polycrystalline.

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Figure 11. Comparison of Czochralski Ingots Grown by Early Technology and by Continuous-Liquid-Feed Process

In 1982, the CLF growth system was shipped to JPL where it was installed and made operational. It was dismantled for storage after it was run intermittently in a non-CLF mode until the end of the FSA Program in 1986.

In this effort, Siltec successfully grew 100 kg of ingot from a continuously recharged crucible at an average rate of 2.1 kg/h; continuous liquid-silicon feed from melt chamber to growth chamber was demonstrated. Automatic control of ingot diameter (±380 μm in 12.5 cm or more) was developed and demonstrated.

c. *Texas Instruments: Czochralski Process and Multiblade Slurry Sawing Technology Development.* From 1975 to 1977, Texas Instruments pursued a large-area Cz silicon ingot growth TD effort and a parallel multiblade slicing TD effort. In both cases, the work involved development of innovative approaches to achieve cost reduction. In a separately funded effort, Texas Instruments endeavored to develop an innovative "continuous" Cz process that included the premelting of silicon in a separate crucible within the growth chamber (Reference 10) and delivery of molten silicon to the main melt as required to maintain the melt level (Reference 11).

The "continuous" crystal growth method, developed in the period 1975 to 1977, employed the use of water-cooled coils and direct gas flows around the growing crystal. This cooling technique was to remove the latent heat of fusion and increase the growth rate and the use of an auger and vibrating drive to feed granular silicon to the melt and allow semicontinuous

crystal pulling from a Varian Associates production puller. Vertical and horizontal crucible premelters were evaluated experimentally and the results compared to theoretically derived maximum pull rates for the Cz crystal growth process. A complete cost analysis was included as part of this program.

Numerous problems were encountered in the effort to charge or recharge the crucibles continuously. Because of oxide formation and the introduction of carbon and the subsequent formation of silicon carbide in the melt, no large single crystals were grown by either process. No appreciable increases in growth rate were obtained by either of the ingot cooling schemes. In the slicing program, cutting rate goals were approached using boron carbide as the abrasive. The high cost of boron carbide, however, made its use unacceptable in a scaled-up operation. Cutting rate goals for use of silicon carbide as an abrasive were not achieved. This effort was terminated because of blade failure caused by bowing of the diamond impregnated blades.

The wafering efforts tested both free and fixed-abrasive multiblade sawing of fixed and rotating silicon ingots. As part of the wafering cost-reduction program, Texas Instruments evaluated the use of laser scribing as opposed to ingot grinding for wafer shaping. An economic analysis of the cost reduction potential of these processes also was included in the program.

None of the innovations evaluated during the two Texas Instruments TD efforts is in commercial use today. The Texas Instruments effort was the first Cz contract to be dropped from the program. The conclusions and recommendations of the team at Texas Instruments are:

(1) Crystal growth modeling and experiments:

(a) Pull rate enhancement techniques, such as employing cold coils around the growing crystals or funneling ambient gas over the crystal, have minor effects on the maximum possible pull rate.

(b) The maximum pull rate varies inversely as the square root of crystal diameter.

(c) Melt agitation from incoming molten silicon droplets does not, of itself, destroy crystallinity.

(d) From economic and operational standpoints, furnace runs consisting of four or five crystals per run with a total weight of silicon of 100 kg are optimal. A negligible cost improvement is obtained for larger runs.

(e) Oxide buildup on the premelter was the major problem inhibiting more extensive continuous runs.

(f) Auger-feed mechanisms for silicon result in contamination from abrasion by the silicon particles.

(2) Multiblade slurry sawing:

(a) Slice thickness of 0.25 mm (plus 0.31-mm kerf) can be achieved with high yield for large-diameter crystals.

(b) Sawing rates are directly proportional to blade load and speed.

(c) A cutting rate of 5 mm/h is obtainable with SiC abrasive. B_4C abrasive is about 2.5 times faster, but its cost is prohibitive.

(d) As-sawed slices have a lapped appearance and can be readily processed into solar cells after a texture etch. Saw damage depth increases with blade load with 33 μm being maximum at 2.5-N loads.

d. *Varian Associates, Inc.: Continuous Czochralski Growth.* In December 1977, the Lexington Vacuum Division of Varian Associates initiated a continuous Cz silicon crystal growth process TD program (Reference 12). Continuous growth was defined in the contract as the growth of 100 kg or more of single-crystal material from a single quartz crucible. The overall objective of the work was to "lower the add-on cost for the Cz growth of silicon to $\$11/m^2$ or less (at 0.795 m^2/kg wafering capability)."

The program was divided into two phases. The first phase was to demonstrate true continuous growth using a modified Varian 2850 Cz furnace. Demonstration milestones were to be:

(1) Simulated recharging prior to furnace modification, e.g., repeatedly remelting and regrowing one ingot without opening the furnace.

(2) Batch recharging with solid silicon.

(3) Continuous recharging with solid silicon.

(4) Continuous recharging with molten silicon.

Modifications to the 2850 furnace to make this possible were to include incorporation of an isolation valve between the main chamber and the seed mounting/ingot removal chambers, and addition of a silicon feeder with its own charge-isolation lock. Although the modifications were made, and an automated control system was installed on this furnace, none of the replenishment or throughput goals were demonstrated with it.

Phase 2 was to be the design, fabrication, and demonstration of a commercially scalable production prototype furnace, designated the 2860, capable of achieving the performance and cost goals of the Project. The prototype furnace was planned to include all the features of the modified 2850, plus improved sensing and automation expected to result in higher throughput of uniform-diameter ingot. The latter could be subsequently ground to specification with nearly one-third greater after

grind yield. The furnace was to be designed to be capable of growing individual ingots up to 1.8 m long and also to use up to 40-cm (16-in.) crucibles. Although the contract called for only a 100 kg demonstration, 150 kg of ingot growth continuously per crucible were projected by Varian to be required to meet the $11/m^2 goal.

Key Accomplishments of the Varian R&D. The single most significant accomplishment of the program was the design and construction of the model 2860 Cz crystal growing system (Figure 12). This machine, although never finally assembled or operated, incorporated both state-of-the-art and innovative features for its time. The Cz growth system technology developed under this contract served as the foundation for the design of the present commercial production machine produced by the Ferroelectrics Corp.

e. *Washington University at St. Louis: Czochralski Crystal Growth Modeling.* From April 1985 through June 1986, Washington University at St. Louis performed an extensive modeling study of Cz crystal growth heat flow (Reference 13). The goal of the study was to develop a comprehensive predictive model that can be used to guide the direction of process TD for the growth of larger, more perfect crystals. The work

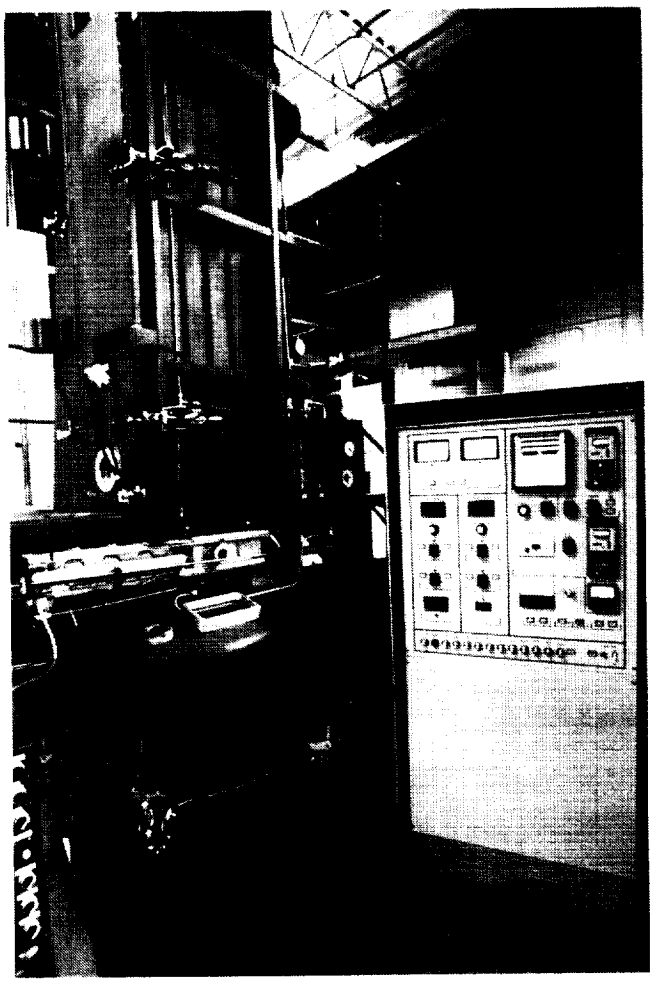

Figure 12. Varian Model 2860 Czochralski Crystal Growing System

plan consisted of the following five tasks: (1) a critical literature survey, (2) development of an algorithm/model suitable for predicting the temperature distribution in the crystal and for calculating the melt-crystal interface shape, (3) performance of parametric studies using the new model, (4) modeling of the melt hydrodynamics, and (5) assessment of the model using available experimental data.

A mathematical model, developed for the simulation of the Cz process, predicted the temperature field in the crystal and the melt along with the crystal-melt interface shape and the pull rate. The modeling approach analyzes the complete system: crystal, melt, and enclosure. This model assumed either conduction-dominated heat transfer in the melt or known heat transfer coefficients. The shape of the crystal-melt interface affects the quality of the crystal by influencing the radial dopant concentration profile. The pull rate is important in keeping the diameter of the crystal constant and in achieving the acceptable level of productivity. The temperature field in the crystal is needed to calculate thermal stresses. These, in turn, are used to estimate the extent of dislocations in the wafers along the crystal. Accounting for both direct and reflected radiation, the effects of the melt-gas meniscus shape and detailed radiation calculations were incorporated into the model.

The detailed model of the Cz process was used for extensive parametric studies. The effects of important variables on growth rate and interface shape were examined and explained. The results of the detailed model were used to develop a simple model that describes the relationships among the important variables such as crystal radius, pull speed, crucible temperature, melt volume, and interface shape.

The simple model can be used to simulate the entire growth cycle of the Cz process and can also be used to develop and implement various operating strategies to monitor the growth process.

Based on the above simulations, a novel technique that uses a gas jet to control the growth process was analyzed. Adjustments of the gas flow rate through the jet can be used to control the crystal diameter which is more stable when the crystal is grown in a convection-dominated environment. Control of diameter by gas-jet cooling is more effective than control through adjustments of crucible temperature or pulling rate. In the presence of jet cooling, it may be possible to control simultaneously both the diameter and the interface shape.

A steady-state model of the hydrodynamics in the melt also was developed to study the relative effects of conduction and convection heat transfer. The Navier-Stokes equations with the Boussinesq approximation are solved with a checking finite-element solution technique. The model and the computer code are useful in studying and characterizing the relative importance of the various phenomena (natural convection, crystal rotation, thermocapillary flow, etc.) that dictate the melt flow field. Model convergence is not

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achieved, however, at the Reynolds and Grashoff numbers characteristic of the commercial operating region of interest. This implies that the flow field may be of an oscillatory nature and that a transient model may be needed. This would indicate that the highest quality crystals cannot be grown without some stabilizing effect such as a magnetic field.

Thermally induced stresses are one of the major causes of dislocations (by slip and twinning) in the crystal. Preliminary stress calculations were performed to study the dislocation density distribution on the wafer surface. It was concluded that the best-quality wafer is obtained away from the center and the outer periphery. This distribution has also been observed in past experimental investigations. The key to reducing the stress levels in the crystal is to have growth at low Biot numbers.

Key Accomplishment of the Washington University at St. Louis Research. Development of a comprehensive predictive model for the Cz growth process that can be used to guide the direction of process technology development for improved growth.

f. *JPL In-House Research and Development.* JPL's crystal growth effort grew specialized Cz ingots for research applications. The Siltec CLF furnace, described in Section II.B.1.b, and a modified Norton system were used.

A variety of specialized crystals were grown to evaluate and support in-house and contractor studies. Single-crystal ingots of p- or n-type with orientations of <100>, <111>, and <110> were grown up to 15-cm diameter. Accelerated ingot growth experiments were performed using helium gas and copper dopants. Small amounts of copper aided the growth speed, but larger quantities of copper resulted in polysilicon material (Reference 14). Bicrystals of <110>/<111>, <100>/<110>, and <110>/<111> configurations, and <100>/<111>/<100> tricrystals were deliberately grown with angles between the orientations ranging from 1 to 20 deg. The smaller angles were stable and formed straight-grain boundaries readily, but larger angle structures were unstable. Straight-grain boundaries were more difficult to maintain, frequently resulting in twins, polysilicon interfaces, and zigzag grain boundaries.

Cz crystal growth runs also were made in support of the Silicon Materials Task to provide material to evaluate the silicon purification processes.

2. Heat Exchange Method

a. *Crystal Systems, Inc.: Process Development.* From November 1975 to June 1981, the FSA Project supported the development of the HEM to grow silicon ingots at Crystal Systems, Inc. (CSI) of Salem, Massachusetts (References 15, 16, and 17). As part of the same contract (954373), CSI also worked on the development of a multiwire ingot slicing technique called Fixed Abrasive Slicing Technique (FAST), described in Section III.B.3.b.

The HEM process employs a directional solidification technique in which a silicon melt contained in a crucible is solidified by controlled removal of heat without moving the crucible, heat zone, or crystal. Removal of heat from the bottom of the crucible is accomplished by a heat exchanger employing helium gas. After its growth, the ingot (Figure 13) can be annealed and cooled at a controlled rate to relieve stresses and thereby prevent cracking. A configuration of the HEM furnace is shown in Figure 14, and the crystal growth scheme is displayed in Figure 15.

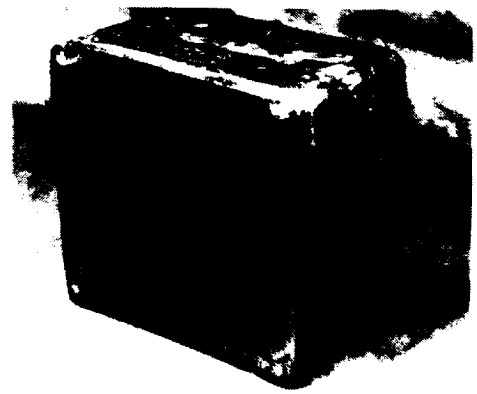

Figure 13. Ingot Cast by Heat Exchange Method at Crystal Systems, Inc.

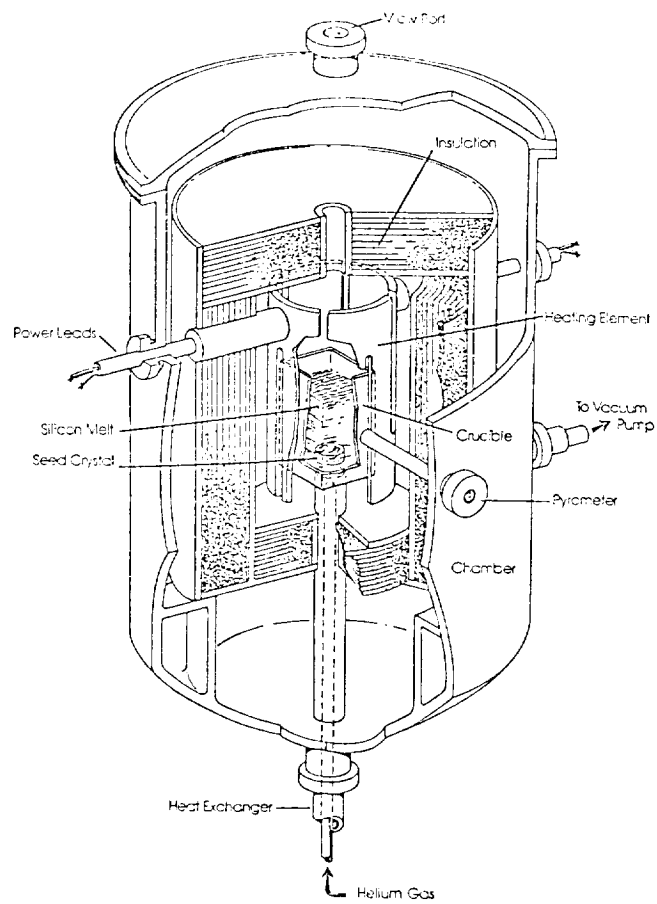

Figure 14. Schematic of Heat Exchange Method Furnace

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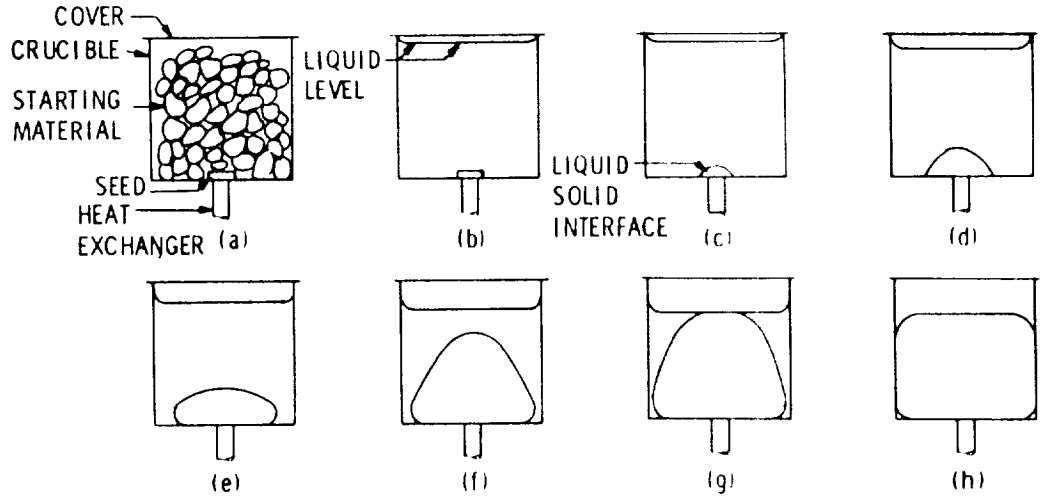

Growth of a crystal by the heat exchanger method:
(a) Crucible, cover, starting material, and seed prior to melting.
(b) Starting material melted.
(c) Seed partially melted to insure good nucleation.
(d) Growth of crystal commences.
(e) Growth of crystal covers crucible bottom.
(f) Liquid-solid interface expands in nearly ellipsoidal fashion.
(g) Liquid-solid interface breaks liquid surface.
(h) Crystal growth completed.

Figure 15. Crystal Growth Using the Heat Exchange Method

The HEM program consisted of the following four phases:

(1) Phase 1: Establishment of the proof-of-concept.

(2) Phase 2: Square cross-section ingots were grown with a high degree (up to 90%) of single crystallinity; 10 x 10 cm cross-section ingots weighing 3.3 kg were grown.

(3) Phase 3: Scaled-up process to grow 22 x 22 cm ingots weighing 16.5 kg. No degradation in material quality resulted from the five-fold scale-up as the 90% single crystallinity was maintained.

(4) Phase 4: Design, fabrication, and testing of a prototype furnace capable of directional solidification of cubic ingots 30 cm on a side. The concept of using grower parts made of unpurified graphite and removing impurities by initial bakeout at high temperatures was established. Use of this procedure did not degrade quality of the silicon product. Ingot size was scaled up to 34 x 34 x 17 cm with a mass of 45 kg.

One advantage of the HEM process is solidification of the melt from the bottom center toward the walls and the top surface. Thus, impurities are driven to the outside surfaces. Subsequent trimming of the resulting ingot removes this outer, less-pure material. Analyses of an ingot grown from solar-grade silicon produced by the Dow Corning Corporation's Direct Arc Reactor process showed that significant purification and effective segregation has been achieved. Another advantage of the HEM process involves ingot slicing. It yields square wafers that provide high solar cell packing densities.

Numerous problems were identified and, in some cases, solutions were found. One problem was to achieve sharp corners for the ingot. Rounded corners decreased silicon yields considerably. Some improvement was attained by supporting the crucible walls to prevent deformation (rounding) during exposure to elevated temperatures. Use of crucibles fabricated from flat sheets of silica gave sharp ingot corners but no low-cost technique for producing crucibles by this method was available. Control of heat flow to obtain rapid solidification rates and yet prevent formation of polycrystalline silicon was not achieved (Figure 16), nor was a sufficient reduction in cooldown time achieved to improve the economics of the process. At the close of the program, it required about 24 to 36 h after solidification of the melt before the ingot could be removed from the furnace. Silicon carbide particles were found to be dispersed throughout HEM material. They have been associated primarily with backstreaming of oil vapors from the mechanical pump. A molecular sieve trap on the vacuum line reduced the contamination, but did not eliminate it entirely.

Solar cell efficiencies for these unoptimized HEM materials throughout the ingot averaged significantly

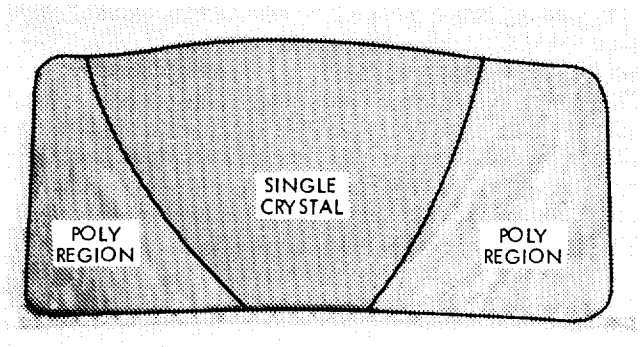

Figure 16. Cross-Section of Ingot Cast by Heat Exchange Method Showing Single-Crystal and Polycrystalline Regions

below that of coprocessed Cz material. This is a serious disadvantage if high efficiency is an important factor. The large-grain polycrystalline regions produced solar cells having efficiencies comparable to those made from the single-crystal regions. This suggested that grain boundaries are not limiting material quality, and therefore that silicon carbide precipitates are probably responsible. In regard to cell performance, it should be pointed out that the device processing was not optimized for HEM.

Key Accomplishments. Key accomplishments of the CSI HEM development are:

(1) The HEM process was scaled up to produce ingots about 34 x 34 x 17 cm in size that weighed 45 kg.

(2) A square cross-section crucible was developed that gives >90% yield of silicon ingot.

(3) Solar cell efficiencies greater than 12% were obtained from solar-grade silicon using HEM material after a double-solidification process.

Present Status. Development of the HEM process under JPL/DOE sponsorship ended in June 1981. Crystal Systems, Inc. provides commercially available HEM multicrystalline silicon that has a columnar structure. Ingots about 33 x 33 x 15 cm are sectioned into nine 100 x 100 mm bars.

b. *JPL In-House: Characterization of HEM Silicon.* Research was conducted to characterize the chemical, mechanical, and electrical properties of HEM material as functions of spatial position within the ingots (References 18 and 19).

The study led to the following conclusions:

(1) Resistivity is very uniform throughout the ingot.

(2) Oxygen content has no effect on the efficiency of the material.

(3) Overall efficiency of the usable material averaged throughout the ingot is about 85% of that observed for coprocessed Cz cells.

(4) Large-grain polycrystalline HEM material is comparable in efficiency to that of single-crystal HEM material.

(5) Large SiC precipitates (50 to 100 μm) may limit solar cell efficiency.

(6) A high dislocation density of about $10^6/cm^2$ results in an overall low diffusion length of 34 μm.

3. Ubiquitous Crystallization Process: Solarex Corp.

A portion of the ubiquitous crystallization process (UCP) development program was supported as part of a cooperative agreement between DOE and the Solarex Corp., and was instituted in June 1980 (Reference 20). FSA Project personnel had technical cognizance of the work with administrative control directly from DOE. For two reasons, the information reported here is abridged considerably. First, the scope of the program was quite large, initially planned to cost-share $9 million, although budgetary restrictions eventually reduced that to less than $5 million. Second, the development was conducted under a proprietary arrangement in which many of the details of the technical processes involved were held proprietary to Solarex. Significant technical progress was made, however, and can be reported in a summary fashion.

At the outset of this development program, UCP was a commercial operation. It produced blocks of silicon approximately 10 x 10 x 12 cm high weighing about 4 kg. These subsequently were wafered into square slices for solar cell processing (Figure 17). As initially planned, the specific elements of the development program were to demonstrate:

(1) Suitablility of the polycrystalline cast material for terrestrial applications.

(2) Development of equipment at the throughput levels consistent with DOE price goals.

(3) Operation of production equipment consistent with the DOE price goals. Key elements of the effort involved development of scaled-up equipment for casting, with the ultimate goal being single blocks of silicon in the 50 to 100 kg range, followed by cost-effective wafering of this material into useful slices. The manufacture of these slices into solar cells was a part of this program only to the extent that it had to be demonstrated that the material produced was consistent with the necessary efficiency. Emphasis was on the control and understanding of defects in the cast material. Device design and other cell and module processing elements were not included.

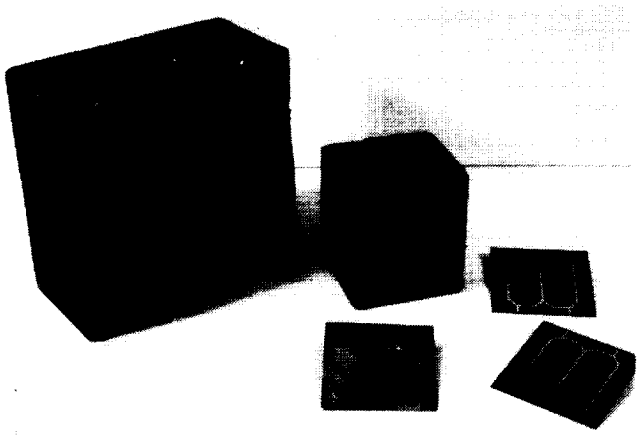

Figure 17. UCP-Cast Polycrystalline Blocks and Solar Cells Fabricated from UCP Material (Solarex Corp.)

Cost analysis of the critical elements of the process indicated major cost reduction could be achieved by increasing the size of the cast block from the initial 4 to 50 kg or better. To achieve this, several prototype furnaces were built. The first had a capacity of about 17 kg, producing an ingot 20 x 20 x 12 cm high. Larger units designed for 50 kg operation were constructed and initial operating conditions successfully determined. At that point in the development, emphasis in the DOE cooperative agreement changed to a more fundamental nature in which further development of this furnace was not included as part of the agreement.

The furnace scale-up activities resulted in several important conclusions concerning casting of polycrystalline silicon blocks. First, larger furnaces showed significant advantages with respect to increases in kilowatt-hours per kilogram for casting and with respect to increases in the average grain size of the cast product.

The successful scale-up of this operation to an economic level consistent with DOE goals requires a wafering process capable of producing sufficiently thin slices at an appropriate rate. Within this program, several alternative wafering methods were evaluated as well as additional development of new advanced methods.

Early studies evaluated the performance of conventional commercial multiblade slurry saws with respect to the requirements of this program. Results of these studies indicated these saws were incapable of simultaneously meeting both the throughput requirements and the slice thickness plus kerf-loss requirements. Individual tests targeted for either parameter approached the necessary values, but always at the sacrifice of the other parameter. For this reason, these studies were discontinued with the conclusion that such wafering could not meet the economical goals of the Project and that no concepts for technical improvements were apparent.

Subsequently, a high-speed multiblade slurry saw was evaluated that was capable of operating at speeds up to five times that of a conventional saw. This study was done under a proprietary agreement with the saw manufacturer. This saw showed considerable improvement over the conventional multiblade slurry saw and simultaneously demonstrated output rates of 0.52 m^2/h at 0.57 m^2/kg (slightly greater than 50% of required values). In spite of these reasonable successes, numerous technical problems, involving failure of mechanical components in the saw and repeated adjustments during the course of a run, indicated that substantial additional development would be required. Consequently, evaluation was discontinued at that time.

Studies were then conducted of conventional ID wafering machines. After significant development in conjunction with saw manufacturers and, more critically, blade manufacturers, the ID wafering process was developed to where the slice and kerf goals were achieved essentially at 0.86 m^2/kg with a throughput rate of 0.25 m^2/h (about 25% of the required values). A more serious limitation was the lifetime of the thin diamond-coated blades. It was concluded that further metallurgical development of appropriate high-strength steel core material would be necessary. Such efforts were not attempted.

Studies were also made of the sources of defects within the material. Significant improvement was made with respect to cell efficiency. At the earliest stages of the research, conversion efficiency was about 10% for 10 x 10 cm devices from the production line. At the end of the program, the efficiency was above 13%. This value compared to a single-crystal control efficiency of 15%. Although some of this efficiency improvement was the result of improved processing, not directly supported by this program, better understanding and control of the casting process itself also resulted in significant improvements. Specifically, the velocity of the crystallization front must be maintained at a level to avoid constitutional supercooling (References 21 and 22). Specific crystallization velocities are dependent upon the ingot size and the detailed shape of the crystallization front. The effect of stress and associated deformation during the casting process could also be observed when thermal geometry was not properly controlled.

To assist in a design of wafering experiments, other research investigations included a study of the fracture strength of the UCP material compared to more conventional silicons. The results indicated no detrimental effects from grain boundaries in the material when compared to single-crystal silicon. This is consistent with accepted theories of brittle fracture that relate the fracture to microcracks in the material rather than crystal structure.

Automated and semi-automated diffusion length measurement techniques were developed to assist in the characterization and analysis of the large quantities of material that were produced as part of this program.

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These were applied both to silicon wafers and to ingots in the as-cast condition. An excellent technique was developed for measuring the diffusion length in wafers. It involved the reflectance of microwaves as a function of resistivity of the reflector. The reflectance of a silicon wafer, when pulsed by an external light, could be measured to yield the resistivity and bulk lifetime of carriers.

A similar technique to evaluate the lifetime of an ingot prior to wafering was developed. It consisted of measuring the quantity of free carriers in a volume of material using a 1.32 μm infrared laser, while carriers in that volume were activated by an external, energetic, penetrating source. Two external sources were considered: pulsed x-rays and a laser near the band edge of silicon (1.1 μm). The x-ray source was not considered further because the short lifetime associated with high-energy pulsed x-ray sources would be excessively expensive. Consequently, a tunable pulsed dye laser was used. This combined laser technique was able to measure lifetime in the silicon at distances up to 2 cm from the surface in a 10-cm-diameter ingot. Because this process measures the change in concentration of carriers upon excitation, extremely low resistivity material is not practical because of the higher intrinsic concentration of free carriers. As developed, a lower limit of the resistivity for this technique was about 0.3 Ω-cm.

From the results described above, the cooperative agreement with Solarex resulted in both numerous technological advances to be used in a production environment as well as other research advances of a more general nature. Because many of the technical advances were incomplete, and because of the proprietary nature of the agreement, the extent to which these processes have contributed to the manufacturing capability of Solarex cannot be quantified. A more general technology development, such as ingot lifetime measurement and better understanding of the requirements of a bulk crystallization process, however, is available for application to other technologies.

a. *Key Accomplishments.* The key accomplishments of the Solarex Corp. UCP development under the DOE agreement are:

(1) The UCP was successfully scaled up from 4 kg/ingot to 50 kg/ingot, with improvements in power use and crystal quality.

(2) A rapid technique was developed to measure bulk lifetime in wafers.

(3) A rapid technique was developed to determine bulk lifetime in cast bulk silicon ingots to a depth of about 2 cm.

b. *Future Work.* It would seem that the casting process, per se, does not constitute a fundamental limitation to the UCP technique. Scale-up seems to be largely a matter of economics and market. Wafering is the most critical element remaining, and substantial improvements are still required. Device performance suffers to a limited extent because of the polycrystalline nature of the material. The use of hydrogen passivation, however, could alleviate this problem somewhat and should be pursued. Precise control of the casting process seems to be an engineering development and is required to ensure reproducibility in the material.

4. Oscillating Crucible Technique: JPL In-House

The efficiency of devices from cast material is limited by structural factors such as dislocations and grain boundaries. The oscillating crucible technique (OCT) was evaluated in the hope of improving crystal quality (References 23 and 24). In this method, the crucible containing the melt periodically is rotationally accelerated and decelerated to cause an effective melt stirring which promotes single-crystal growth. The silicon ingots used in this program were grown by IBM, and the characterization was performed both by IBM and JPL.

Several ingots were prepared. Two different types of oscillations were tried: unidirectional and bidirectional. The latter method, in which the crucible was rotated first in one direction and then in the other, was expected to improve the stirring action and keep the liquid-solid interface cleaner.

The ingot oxygen content was measured both by infrared spectrophotometry and secondary ion mass spectroscopy (SIMS). The results indicated the oxygen concentration was uniform throughout the ingots. SIMS also was used to measure the total carbon in the ingots and it showed no carbon gradient within each ingot.

Structural analysis was carried out for OCT ingots and for a single ingot grown without rotation for comparison. For both ingot types, the single-crystal growth front broke down early in the runs and turned to small-grained polycrystalline material. In the case of the non-rotated ingot, the remainder of the ingot consisted of this polycrystalline material with the grains randomly oriented. In the case of the OCT ingots, columnar grains typically nucleated from the single-crystal regions and grew all the way to the top of the ingot. The optimal oscillation rate was not determined nor whether bidirectional rotation is better than unidirectional rotation.

In one case, furnace modifications were made to improve control of the thermal environment, and an ingot was grown at a relatively high growth rate with bidirectional rotation. The structural change was dramatic: about 70% of the ingot was single-crystal with the remainder being columnar large-grain polycrystalline material.

Silicon carbide particles, seen throughout the ingots, may be responsible for the breakdown of the single-crystal growth front. Vitreous carbon crucibles were used to prevent their cracking upon solidification.

The highest efficiency of solar cells made using OCT material was 12.9% AM1. This was comparable to that

of Cz control cells. Minority carrier diffusion lengths in the single-crystal regions reached 200 μm, and values in the polycrystalline regions exceeded 100 μm, indicating excellent quality for both types of material.

The uniformity of the oxygen and carbon data indicates that the primary objective of the program was achieved: oscillation of the crucible leads to an adequate stirring of the melt.

C. SUMMARY

Development of the ingot growth processes was supported by the FSA Project. Work also was conducted on three efforts in support of bulk growth.

Substantially increased throughput and reduced cost of the Cz process were achieved, and measurable technological developments of other ingot processes also were achieved. Specifically:

Kayex Corp. completed a contract in 1980 in which the capability was developed and demonstrated of growing 150 kg of 15-cm-diameter silicon ingot material from one quartz crucible. Technology was developed to allow the crucible to be recharged with silicon while still under vacuum and at temperatures above the silicon melting point. Significant improvements were obtained compared to conventional Cz technology including controls with improved sensors, prototype equipment that was transferable to industry, and increase in yields (90% of melt pulled). High solar cell efficiencies were obtained for the material from the 150 kg demonstration growth-run product.

Siltec was successful in growing 100 kg of ingot material from a crucible at an average rate of 2.1 kg/h, using continuous liquid silicon feed from the meltdown chamber to the growth crucible. Equipment for automatically controlling ingot diameter to ± 0.38 mm was developed.

Washington University at St. Louis completed a Cz crystal growth modeling study to predict the important process parameters such as pulling rate and interface shape, to provide strategies for growth of large-diameter crystals, and to lead to improved process control algorithms.

JPL completed a crystal growth effort both to produce specialized Cz ingots and to characterize OCT and HEM ingots.

CSI, which successfully pursued the HEM TD program, now provides HEM silicon to the commercial market.

Solarex Corp. carried out a TD program on their UCP under a cooperative program funded directly by DOE, with technical management provided by JPL. Solarex commercially used the resulting scaled-up ingot technology. The latter part of the program was changed to a more fundamental nature wherein studies were made of the sources of defects within the material (as related to the casting process), of fracture strength (to assist in design of wafering experiments), and of characterization of the material.

SECTION III
Wafering

A. INTRODUCTION

The ability to wafer or slice silicon ingots, grown by any one of numerous techniques, has a major impact on the final cost of the wafers produced. Kerf losses (material removed during slicing of the ingot) result in the waste of considerable amounts of expensive silicon, and wafering uses expensive, precision machines whose productivity is relatively low. The added cost of the wafering step, therefore, is large. Analyses of the cost elements of PV manufacturing led to the conclusion that slicing needed to result in about 1 m^2 of wafers per kilogram of silicon, and at a rate of between 0.2 and 1 m^2/h, depending upon other factors of the specific technology.

At the outset of the program, ID sawing and multiblade sawing were the standard techniques employed for slicing silicon ingots. Evaluation and developmental programs for these technologies were conducted by ASEC, Varian Associates, Hoffman Division of Norlin Industries, Inc., Siltec Corp., and Silicon Technology Corp. Several other novel and new wafering technologies also were evaluated and developed. These included a free-abrasive wire saw produced by Yasunaga in Japan and evaluated by JPL and by the Solarex Corp. A proprietary high-speed multiblade saw (800 to 1000 cycles/min) was evaluated in the Solarex cooperative agreement and is described as part of the ingot-casting subsection. A completely new technique, called fixed-abrasive slicing technique (FAST), using diamond-coated wires, was developed by Crystal Systems, Inc. None of these technologies achieved the Project goals because of reasons described in detail within this Section. The limit encountered was a trade-off between cutting speed and cutting yield.

A more recent study at the University of Illinois at Chicago contributed to understanding the basic process of material removal. Scratch tests, indentation tests, and other surface studies were conducted as functions of the test environment. The results suggest that better understanding of the process of wafering could, in fact, improve its performance. Application of such findings, however, was not attempted as part of this effort.

The inability to achieve wafering goals in the middle years of the Project was a significant factor in the decision to terminate the process of ingot growth and subsequent wafering as a viable option to produce silicon sheet.

At present, ID sawing remains the most important commercial process for fabricating silicon wafers. A free-abrasive wire saw designed and built by Monsanto now is used in the regular production of wafers at Monsanto, and a new multiwire saw is finding a favorable market reception. The FAST R&D is being funded by DARPA as a possible method for slicing ingots of various electronic materials. None of these processes has come within a factor of two of meeting the add-on costs required to support a viable ingot alternative.

B. IMPLEMENTATION

1. Assessment: Optical Coating Laboratory, Inc.

From September 1977 through February 1978, the Photoelectronics Division of Optical Coating Laboratory, Inc. (OCLI) (now Applied Solar Energy Corp. or ASEC) performed an "Assessment of Present State-of-the-Art Sawing Technology of Large Diameter Ingots for Solar Sheet Material" (Reference 25).

The OCLI approach was:

(1) To perform a series of slicing experiments using multiple-blade slurry (MBS) saw slicing, multiple-wire slurry (MWS) saw slicing, and ID saw slicing to characterize the results in terms of process variables, product yield and quality, and process cost.

(2) To perform a cost analysis in terms of add-on slicing cost, wafer cost, and cost per square meter of usable sheet area.

(3) To assess the cost reduction potential for each of the processes and to draw up conclusions and recommendations. These are given, unabridged, below.

The OCLI assessment did not as thoroughly explore all the process variables for the wafering methods (MBS, MWS, and ID) as did subsequent specialist subcontractors to the Project (Norlin, Varian, Solarex, Siltec, and Silicon Technology Corp.), nor did it include the fixed-abrasive multiple wire technique (Crystal Systems, Inc.).

The final conclusions and recommendations of OCLI were:

(1) At present, Solar Array Manufacturing Industry Costing Standards (SAMICS) cost assessment indicated that the ID saw slicing is more favorable than the MBS saw and MWS saw techniques. Its capability of automation, essential for large-volume production, adds advantage over the other two methods. Preliminary results indicated the ID saw slicing technique would meet the slicing goal in 1982 without significant innovation of the slicing techniques. Significant improvements in blade package, slurry, wire, and machine capacity, however, were needed to meet the goal for the MBS saw and MWS saw techniques.

(2) The advantage of lower kerf loss by the MWS saw slicing was obtained at the expense of an add-on slicing cost higher than the ID and MBS saw techniques.

(3) Mechanical wafer parameters, such as thickness variation, taper, bow and roughness, were considerably better for wafers sliced with both the ID and MWS saw than for those with the MBS saw. Wafers sawed with the ID saw (sliced at 2 in./min of cut rate) showed slightly better parameters than those sliced with the MWS saw.

(4) The add-on slicing cost should be assessed taking into account the specifications of thickness, kerf loss, and diameter of the wafers to be sliced. These are the major parameters that strongly influence the overall slicing cost. The surface damage generated by the slicing methods should be investigated, and the electrical power output that can be obtained from the sliced wafer should be incorporated in the overall assessment. In other words, a systems approach is necessary to obtain optimum slicing conditions.

(5) Preliminary results using thin ID blades were not successful, mainly because of short lifetime of the blades. Development of ID blades that will give low kerf loss with long life is needed.

(6) To achieve further reduction of the cost of wafering, the following areas of development of ID saw machine design are suggested: improvement in machine productivity, use of a rotating crystal system, and development of techniques to detect mechanical instability (or vibration) of ID blades during the slicing process. These instabilities result from the blade head, inadequate blade tension, etc.

2. Multiple-Blade Slicing

In the advanced MBS process, flat steel blades are drawn back and forth across the ingot, in a fashion analogous to a knife slicing bread. Instead of using a blade with fixed teeth, however, as does a bread knife, the MBS process uses a suspension of abrasive particles in a carrier fluid that is poured over the flat steel blades and ingot at the point of cutting.

a. *Norlin Industries, Inc.: Free-Abrasive Multiple-Blade Slurry Sawing Process.* Two contracts for MBS technology assessment and development were awarded to the P.R. Hoffman Company, Division of Norlin Industries.

The first contract, "Slicing of Single Crystal and Polycrystalline Silicon Ingots Using Multi-Blade Saws," was a 6-month effort (January through July 1980). Its goals were to qualify P.R. Hoffman as a Project technology development contractor and to evaluate the feasibility of the MBS process to achieve Project wafering goals. The contract required that wafering runs be performed on the Varian 686 saw, the Meyer and Berger GS-1 saw, and the Hoffman PL-4 saw (Figure 18). Hoffman investigators were to perform a technical and economic evaluation of the MBS process to determine what, if any, further technology development effort was warranted.

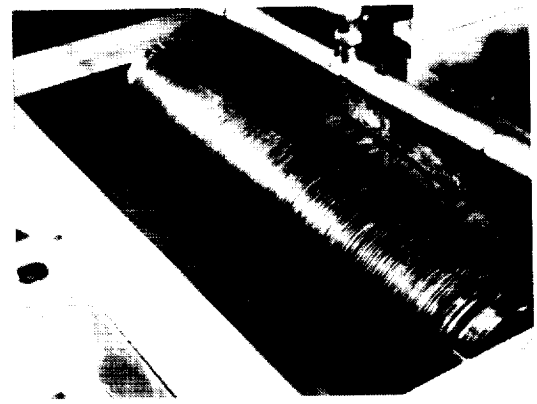

Figure 18 Hoffman PL-4 Saw in Operation

The second contract, "Multiple-Blade Sawing of Silicon Ingot Into Sheet: Testing and Development," was planned to be a 15-month effort, beginning in March 1981. It was terminated, however, after 10 months as part of an overall Task redirection. The original work plan, resulting from analysis of the first 6-month contract, consisted of two phases:

(1) Phase 1, a 12-month effort, included design and fabrication of a microprocessor-controlled workpiece feed mechanism; design and fabrication of a wafer lift-off mechanism; test and evaluation of slurry and abrasive recycling; test and evaluation of new abrasive, vehicle, and blade materials; a parametric process optimization study; and definition of the process and design parameters for the Phase 2 engineering design task.

(2) The objective of Phase 2 was to design a high-throughput (1000-blade) MBS saw that would be capable of achieving the Project throughput and cost goals of 1/2 wafer/min (up to 15-cm-diameter), with a conversion ratio of 1 m^2/kg at an add-on cost of $\leq$\$14/m^2 (1980 dollars).

Details of the program plans, the work performed, and the results were documented by Norlin Industries, Inc. (References 26 and 27).

Key Accomplishments. The key accomplishments of the Norlin/Hoffman MBS R&D efforts are:

(1) MBS became better understood as a candidate wafering technology. Run process variables and their impact on performance

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were evaluated, and areas were determined that required attention to increase yield and throughput and reduce cost. The latter included reduction of consumable costs (perhaps through recycling), optimization of process control and process parameters, improved wafer handling methods, and increased productivity per saw (a 1000-blade machine).

(2) Performances demonstrated individually, but not simultaneously, included 400 wafers/run, 100% yield of 5-cm-diameter wafers, 20 wafers/cm of 5-cm-diameter wafers, and a 38 μm/min cut rate in a 10-cm-diameter workpiece. The add-on cost for state-of-the-art MBS wafering was projected to be \$104/m^2 (1980 dollars). These achievements and this cost are to be compared with the SAMICS goals of simultaneously achieving 455 10-cm-diameter slices, 25 slices/cm, 95% yield, and \$13.70/m^2 add-on cost (1980 dollars).

(3) Because the contract was terminated before its scheduled completion date, few of the deliverables were completed. The microprocessor-controlled workpiece feed mechanism was neither designed nor built. A wafer lift-off mechanism, including a heated stage for wafer mounting and demounting and floating brushes to support and protect the wafers, was designed and partially fabricated.

(4) Considerable effort was spent to identify a vehicle or abrasive recycling process using an off-saw cyclone separation reclamation process. By the termination of the effort, the system had been designed, all the components had been ordered, and some had been received. However, the process was not developed.

(5) Numerous slurry saw wafering tests were performed to establish a baseline technology, and to evaluate process variables such as blade head speed, workpiece/blade force, deliberate bounce, abrasive/vehicle ratios and slurry volumes, etc. The purpose of these runs was to indicate optimum process parameters to incorporate into the Phase 2 saw design. The trend of the results was not surprising (increased blade head speed resulted in higher cutting rates).

With the termination of these contracts, technology development of MBS came to a halt. None of the new technologies under development is known to have been carried forward by the industry and implemented. Cost of MBS remains about the same as it was in 1980. The process has had limited application for silicon ingot wafering.

b. *Varian Associates: Free-Abrasive Multiple-Blade Slurry Sawing.* In 1976, Varian Associates became a subcontractor for a TD program with the goal to develop a multiple-blade sawing technology that by 1986 could meet the FSA Project add-on cost goal of \$13/W$_p$. The program consisted of an experimental wafering process parameter optimization phase; an equipment design, fabrication, test and evaluation phase; and a continuing economic assessment of the technology. The work included parallel analysis of the process of free-abrasive slicing and blade dynamics. Details of the program can be found in the Final Report from Varian Associates (Reference 28). A summary of this comprehensive report is available in a JPL publication (Reference 29).

The process parameter optimization program was performed on a modified Varian 686 free-abrasive multiple-blade saw. The saw included an improved drive system and instrumentation for monitoring the process. The experimental effort included a study of various abrasive materials and abrasive vehicles, parameter variations including ingot orientation, blade-head speed, upside-down cutting, "loading," high blade-head speed, ingot diameter, kerf width, and abrasive size and slurry makeup. Analysis of the results of these efforts included scanning electron microscopic study of the abrasive particles before and after cutting, the use of a dynamometer to measure the vertical and horizontal components of force occurring as a result of parameter variation during the slicing experiments, a study of blade wear characteristics (blade corrosion using a water-base slurry), and etching and scanning electron microscope studies of the damage in the silicon wafers incurred as a result of cutting process parameter variations (Figure 19).

The design, construction, and testing of a 1000-blade MBS saw (Figure 20) was planned as a result of an economic analysis that indicated that the higher throughput of a 1000-blade machine would be

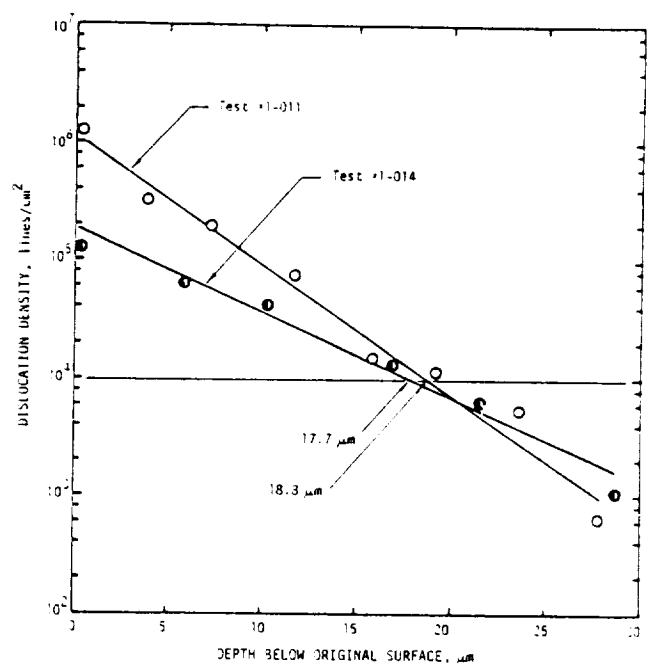

Figure 19. Dislocation Density as a Function of Depth

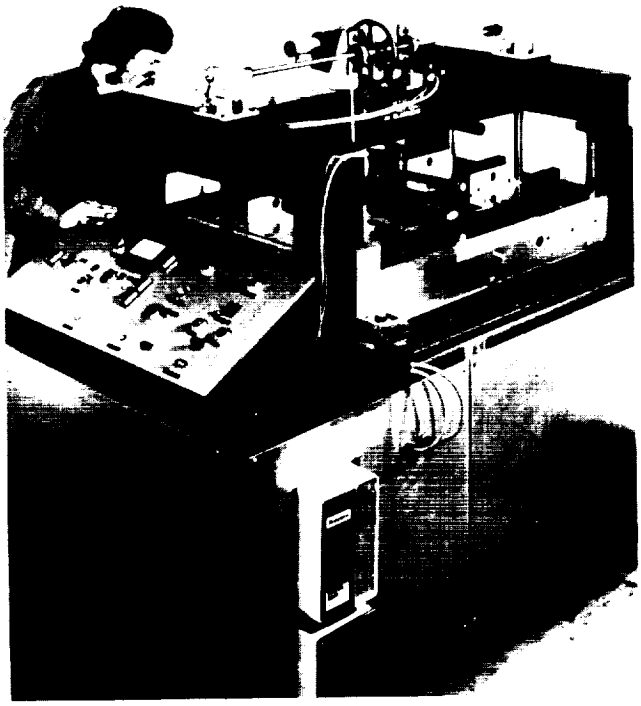

Figure 20. Varian Experimental 1000-Blade Saw

necessary to achieve the economic goals of the program. The mass of a blade head strong enough to hold 1000 blades in tension was so great that, to achieve the blade-to-workpiece relative velocities required for efficient cutting, Varian designed and built a novel saw in which the workpiece itself reciprocated instead of the blade head. The final design embodied many improvements over state-of-the-art MBS technology. Unfortunately, in operation, the machine was plagued with short lifetimes for its bearings and poor and uneven slurry distribution problems. By the termination of the program in 1979, the saw had not achieved its promise.

Varian analyses of multiple-blade sawing included an economic analysis as well as a process analysis and a blade analysis. Using the Improved Price Estimation Guidelines (IPEG) method, the results of the 1979 cost analysis, involving a state-of-the-art sawing technique, indicated that the 1979 technology scaled up to yield 51,500 m^2/year of wafers could do so at the wafering value added cost of $128/$m^2$. A 1986 cost reduction scenario, based on reasonable expectations of technology development, projected a value added of $19.20/$m^2$ for a factory scaled up to 518,000 m^2/year. This projected figure still is larger than the Project goal.

Process analysis included a study of the efficiency of the cutting process and a study of geometric and kinematic fundamentals of the slurry sawing process. Analysis of the efficiency of the cutting process relates both to the process of planar wear, which is affected by abrasive geometry, load, hardness, and sliding distance, and to the nonplanar "wedging" process that occurs in the wear trough. Workpiece "bounce" is a critical process parameter in MBS wafering. Blade analysis included a study of blade stability and deflection, the influence of pre-tipped blades, and the process of blade buckling during the wafering process. Because blade strength typically varies inversely with the kerf, the reduction of both kerf loss and blade buckling is a formidable problem. The statistics of a blade package and probability of cumulative error in blade and spacer stacking also were analyzed. The probability of blade runout as a function of blade and spacer tolerances and number of blades per package has been calculated as well as the expected effects of blade runout in wafer damage and breakage.

Observations and conclusions drawn from the program are summarized in the Varian and JPL reports, and the most significant are included below:

(1) General.

(a) MBS sawing easily may be used to produce 16.4 wafers/cm of 100-mm-diameter ingot (0.2-mm blades and 0.4-mm spacers) or 17.9 wafers/cm of 100-mm-diameter ingot (reducing blade thickness by 0.05 mm) at commercially acceptable yields using commercial technology.

(b) Careful use of commercial technology allows cutting of 19.7 wafers/cm of 100-mm diameter ingot (0.15-mm-thick blades and 0.35-mm spacers) at or near commercially acceptable yields.

(c) On an experimental basis, 21.9 wafers/cm of 100-mm-diameter ingot have been cut successfully.

(d) Crystal orientation and polycrystallinity have no effect on the slurry-sawing process.

(2) Slurry Vehicle.

(a) The most important factor in oil-based slurry vehicle selection is "lubricity," a parameter that characterizes the drag force encountered with small clearances.

(b) Suspension power is not important as long as mechanical stirring allows delivery of the abrasive to the cutting interface.

(c) Extensive (>80%) recycling of non-suspension vehicles is easy and practical.

(3) Abrasive.

(a) Boron carbide and zirconia-aluminum oxide abrasive are not suitable for economic and technical reasons, respectively.

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(b) For an abrasive, #600 silicon carbide (as sized by Micro Abrasives Corp.: 10 to 30 μm diameter, average) is the best cost-efficiency trade-off.

(c) Abrasive is most easily recycled using a centrifuge.

(4) Wafers.

Removal of 10 to 15 μm/side from a wafer by etching is sufficient to remove saw-induced damage.

c. *JPL In-House Blade Evaluation.* For the MBS wafering technology, potential cost savings were considerable for the use of a water-base slurry instead of the standard polishing-cutting oil vehicle. Significant failures of high-carbon-steel blades were observed, however, using a water-based slurry during silicon wafering. Mechanical testing blades in appropriate environments showed that failures were due to stress corrosion.

To determine the feasibility of using corrosion inhibitors in water-base MBS wafering, a specifically designed fatigue test was carried out involving 1095 steel blades operating in distilled water in which various corrosion inhibitors had been dissolved. Results indicated several corrosion inhibitors had significant potential for use in a water-based MBS operation. Blade samples tested in these specific corrosion inhibitor solutions were found to exhibit considerably greater fatigue life than blades tested in cutting oil (Reference 30).

Amorphous metal ribbons manufactured by Allied Chemical Company were evaluated to determine the feasibility of their use for MBS ingot wafering. Their mechanical properties and corrosion resistance were reported to be reasonable. A series of material characterization and fatigue tests, carried out at JPL, indicated that these materials have greater hardness and wear resistance than high-carbon-steel blades. Because these materials lacked plasticity, however, they seemed to be more susceptible to notching, resulting in fracture.

3. Multiple-Wire Slicing

MWS is achieved by reciprocally moving one continuous wire over the workpiece at many parallel locations, or by moving several parallel wires simultaneously over the workpiece. Cutting may be accomplished by abrasive particles fixed to the wires or by a slurry of abrasive particles in a carrier fluid. MWS resembles MBS except that wires rather than blades are used. This results in less damage to the wafer surface, but cutting rates are slower.

a. *Solarex Corp.* Solarex Corp. performed a 1-year (July 1978 to July 1979) "Evaluation of the Technical Feasibility and Effective Cost of Various Wafer Thicknesses for the Manufacture of Solar Cells." The work is reported in detail in the final report (Reference 31). This study was essentially a test in a production environment of the Yasunaga Model YQ-100 free-abrasive multiple-wire saw.

The Yasunaga YQ-100 saw uses a single continuous wire, fed from one spool around a three-roller loom to a take-up spool. The spacing of the wires on the loom (pitch) is determined by the spacing of grooves cut into the rollers. The wire feeds back and forth between the spools, incrementally advancing toward the take-up spool on each cycle. The wire advances at a rate high enough to prevent its wearing too thin and breaking under the tension. Constant tension is maintained on the wires. As the loom drops down onto the workpiece, cutting is effected by an abrasive slurry pumped onto the wires and workpiece. Wafer thickness and kerf loss are determined by roller pitch, wire diameter, and abrasive size. Cutting rates and wafer quality are determined to a great extent by the load applied between the workpiece and the wires. Process cost drivers include the usage rate of wire and abrasive, cutting rates, and labor. The evaluation effort included a series of experiments varying such parameters as pitch, wire diameter, and abrasive particle size wafering, characterization of the product wafers including depth of damage, and evaluation of the practicality of module fabrication using thin wafers.

A parametric wafering study was performed using this saw. Low kerf losses, low wafer surface damage, and high wafer/inch yields were achieved. Kerf loss as low as 0.165 mm was shown to be possible, less than half observed for present state-of-the-art techniques. No appreciable damage was observed in wafers cut with 5 to 10 μm abrasives, although the cutting rate was unacceptably slow. Damage as little as 15 to 10 μm was observed using 30-μm abrasive particles. Using the YQ-100, a cutting yield of 25 wafers per centimeter was demonstrated. Thirty-three 0.13-mm-thick wafers per centimeter seemed feasible. Productivity was reduced, however, as numerous problems were encountered that originated with the state of the art of the machine. Problems included ruptured slurry lines, catastrophic failure of the wire spools, unwieldy loading mechanisms, bearing failures, and limited workpiece size. Work including spool winding and wafer clean-up was surprisingly labor-intensive. Wire breakage was common, and wire usage was unacceptably high. Some re-use processing, perhaps plating-up the used wire, would be required to make the process economically acceptable.

Cells were fabricated from wafers sliced with the MWS saw, and two modules were assembled from these cells. The performance of the cells, as expected, varied with the amount of wafering damage removed. The advantages of flexible modules containing thin cells was analyzed and the results are given in the Final Report along with current-voltage (I-V) curves of the modules.

The conclusions and recommendations of the Solarex team are summarized below:

(1) Numerous problems were experienced with wire saw equipment, causing the program to fall behind schedule. The saw operation was substantially more labor-intensive than anticipated.

(2) Wafer characterization of saw runs has established extremes of technical possibility with the saw. It was concluded that thin wire (0.08-0.1 mm) cannot be used presently to cut large quantities of wafers. At the other end of the spectrum, thick wires do not increase reliability over those of medium gauge and are not cost effective.

(3) The thinnest wafers that seem practical to saw are 0.1-0.2 mm thick. To get a thickness of 2 mils, the sliced wafers require more chemical etching than would be needed just to remove the surface damage from the saw. The sawed wafers, however, are within 12 μm of being absolutely flat (convex lens shape). This is necessary for etching to 2 mils thickness. Large-diameter (7.5-cm) ultrathin wafers were etched down to 50 $\pm$12 μm.

(4) The maximum number of wafers (roller pitch) is not established. Estimated optimums are achieved with 0.15-mm wire and 0.4 mm pitch and various grits. This yields a weight percent yield of from 50.3 to 58, and an area yield of 1.08 m^2/kg. The 0.3-mm tool may work with sufficiently high reliability to give an area yield of 1.43 m^2/kg.

(5) Results of the cell processing of wafers produced in sawing runs indicate that much less etching is required to remove saw damage than was anticipated. The wafer surface is good. It is flat, not pitted, with very infrequent wire marks.

(6) Recommended wafering system modifications include a much improved constant torque motor and controller on the respooling system, steel rather than cast aluminum wire spools, and the design and fabrication of a 0.3 mm roller grooving bit that will permit high wafer area per kilogram sawing. A significant modification is the building of a constant loading device for the saw itself.

(7) Labor loading for a single sawing run by a competent, experienced technician presently breaks down to nearly $0.80 per wafer for labor alone. Even at 200 wafers/run, it is still >$0.30. Additional engineering development on the saw and its efficient operation is necessary to make the operation less labor-intensive.

b. *Crystal Systems, Inc.: Multiple-Wire Slicing/Fixed-Abrasive Slicing Technique.* A technology development program on a multiple-wire FAST was supported by the FSA Project at CSI, the innovators of the technique. The work and results are reported in detail in the Final Reports of Phases 1 through 4 of the contract (see References 15, 16, and 17). The features of the latest embodiment of the process include a low-mass, high-speed reciprocating blade head, a multiple-wire blade pack containing small-diameter, high-tensile-strength wires with fixed diamond abrasive only on the cutting surface, and a rocking ingot mount (Figure 21). The potential advantages of such a system include low equipment, labor

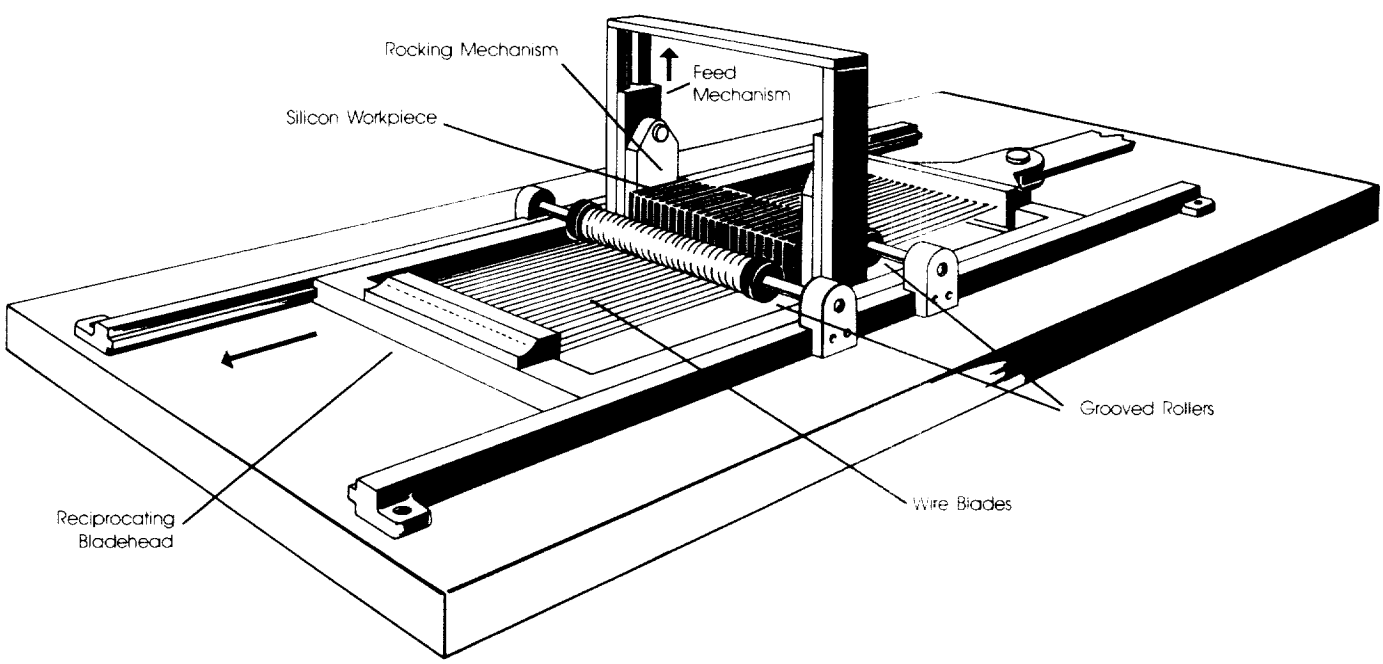

Figure 21. Crystal Systems, Inc. FAST Multiwire Saw

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and expendable costs, high throughput and material utilization, and low wafer-surface damage.

The program included machine and wire development efforts and testing. In the course of the program, two generations of FAST slicers were built. The final configuration employed a smooth granite block on which the reciprocating frame, the workpiece carriage, and the vertical feed mechanism were all mounted and precisely aligned. The wire-pack frame was designed to accommodate workpieces up to 30 cm in length and 15 cm in diameter. The experimental systems employed a counterweight to balance the motion of the blade head. In a production machine, this would be accomplished by a second blade head. A two-blade head configuration was used in the cost analysis of the process. Linear blade-head speeds up to 2.2 m/s were successfully achieved in the cutting tests (versus 0.33 to 0.43 m/s typical speeds in the MBS systems).

The wire development effort included evaluation of abrasive-impregnated and plated-wire fabrication methods and testing of the wires. The impregnation study variables were wire material (steel and tungsten), wire diameter (3, 4, and 5 mils), copper-plated wire sheath thickness (7.5 to 15.5 μm), diamond abrasive size (15, 30, 45, and 60 μm) and electroless nickel plating. The electroplating of diamonds onto wires was studied using as variables: wire material (steel and tungsten), wire preparation (nickel flashing on tungsten and postplating bake of steel), abrasive size and sized distribution (22 to 60 μm diamonds and combinations), nickel plating thickness, and distribution of diamonds on the wire (entire circumference, 60 deg V-groove, and bottom surface only). A wire plating facility was set up by CSI for this work. Natural and synthetic diamonds were compared; natural diamonds were observed to cut more effectively than the synthetics, perhaps because of their "blocky" morphology.

A test plan was used to evaluate the various wires and to identify wire failure mechanisms. Once the initial wire technology development problems for electroplated and impregnated wires were overcome, the wires could be directly compared in slicing runs. Results of the comparison showed the electroplated wires to yield higher cutting rates and yields and longer service lifetimes than the impregnated wires. The latter were dropped to concentrate on developing the electroplating process. Diamond pull-out was the major failure mechanism of both types of wire, but it occurred at a much higher rate in the impregnated wires.

An economic analysis of the potential add-on cost for the FAST process was performed by CSI using the IPEG equation. The respective projected results, optimistic and conservative, were \$5.90 and \$13.13/m^2, versus the Project goal of about \$18/m^2. Each of the process goals required to meet the projected costs (0.14 mm/min cutting rate, 25 slices/cm, and 90 to 95% yield) was achieved individually. A key requirement, 5 to 10 slices per wire, however, was not achieved, nor were the above achieved simultaneously.

Key Accomplishments. The key accomplishments of the CSI multiple-wire fixed-abrasive R&D are:

(1) Achieved the slicing of 25 wafers/cm on a 10-cm-diameter silicon ingot with greater than 99% yield (222 out of a possible 224 wafers) for 0.249-mm-thick wafers and 0.151 mm kerf (Figure 22).

(2) Achieved the slicing of 19 wafers/cm on a 15-cm-diameter workpiece.

(3) Attained an average slicing rate of 0.14 mm/min on a 10-cm-diameter ingot.

(4) Three 10-cm-diameter ingots were sliced using a single wire pack.

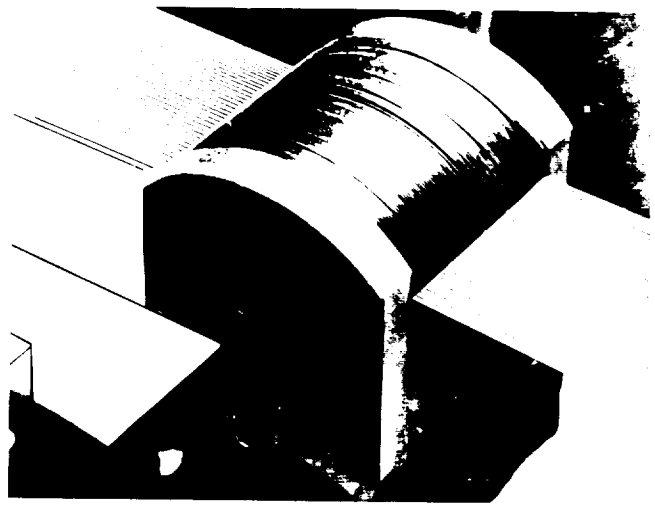

Figure 22. Slicing of Silicon Ingot by FAST

Present Status. Since the termination of FSA funding, process development has continued at CSI supported by internal and DARPA funds.

c. *JPL In-House Evaluation of Multiple-Wire Slurry Sawing.* JPL also evaluated a new multiple-wire slurry-type sawing machine, Model YQ-100, manufactured by Yasunaga Engineering Company of Japan. (Results of a similar study by Solarex are reported in Section III.B.3.a.). The new saw was claimed to be capable of slicing workpieces as large as 10 x 10 x 10 cm into 250 wafers simultaneously with low kerf loss.

A series of slicing demonstrations was made with the MWS saw to evaluate its silicon ingot wafering capabilities (Reference 32). Results revealed that sawing can provide 1.05 m^2/kg of usable wafer area from an ingot (e.g., kerf width 0.135 mm and wafer thickness 0.265 mm). Satisfactory surface qualities and excellent yield of silicon wafers were found. The add-on cost of producing wafers from this saw is high, primarily because the Yasunaga saw uses a large quantity of wire. The add-on cost must be significantly reduced, perhaps by extending the wire life and/or by reuse of properly plated wire to restore the diameter.

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4. Internal-Diameter Slicing

a. *Siltec Corp.: Enhanced ID Slicing Technology for Silicon Ingots.* The objective of this program, started in 1979, was to develop processes capable of significantly increasing the number of usable ingot slices per unit length as compared to industry practice. This was to be achieved through reduction of both kerf and slice thickness. To attain this objective, a combination of three key technologies was investigated: ingot rotation with minimum exposed blade area, dynamic cutting-edge control (Figure 23), and the use of prefabricated blade inserts (Figure 24). The program called for demonstrating the feasibility of low-cost slicing with a kerf loss of between 127 and 178 μm, with a combined kerf and slice thickness of less than 406 μm (25 slices/cm). Results of the program are presented in the contract final report (Reference 33).

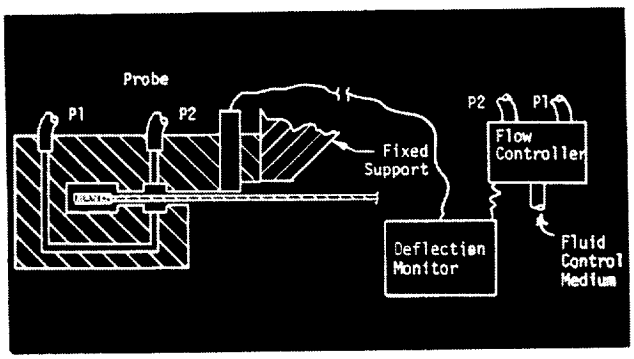

Figure 23. Schematic of Closed-Loop Blade Position Control System

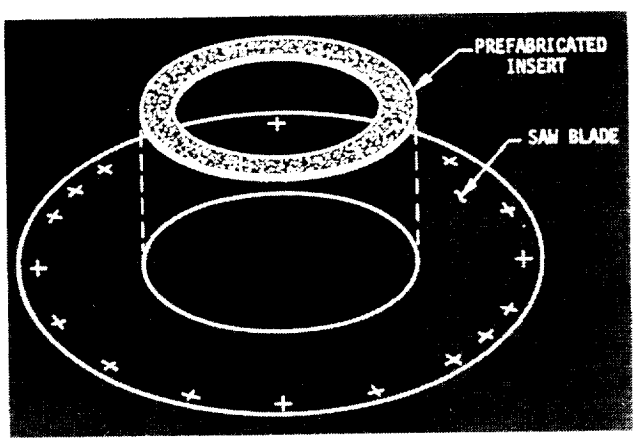

Figure 24. Perspective View of Prefabricated Insert Blade

A commercially available Siltec saw (Figure 25) was equipped with a programmable ingot advance/rotation unit and a closed-loop cutting edge position control system. Ingot rotation had previously been projected to be useful during a JPL in-house program. An obvious advantage with this approach is the much-reduced head size because the ingot travel distance is

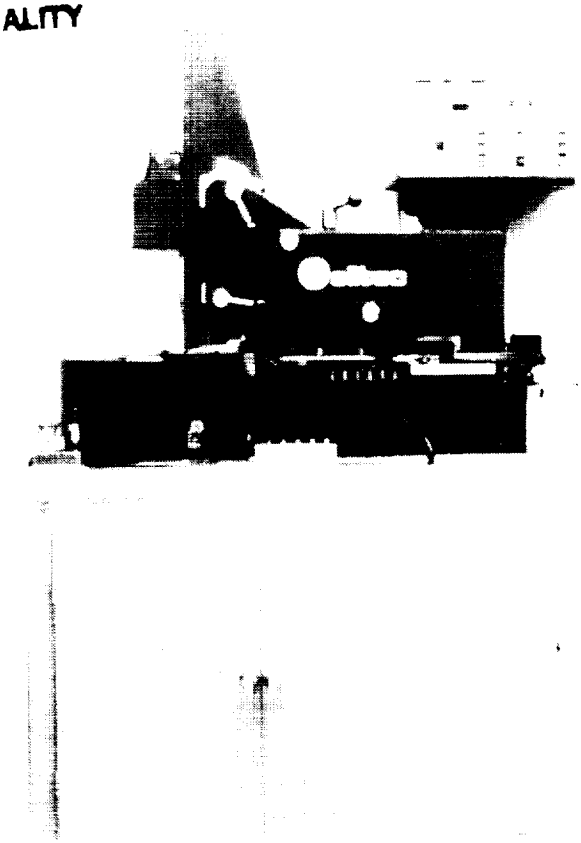

Figure 25. Commercial Siltec ID Saw

reduced to half that for the case of no rotation. Experimentation with ingot rotation revealed that severe limitations on productivity were imposed because of the combination of the anisotropic material character of the monocrystalline silicon and ingot rotation during cutting. Cutting edge position control, with low kerf blades, proved to be very effective through reduction of the deflection by one order of magnitude. This contributed significantly to kerf reduction.

Closed-loop control of blade deflection proved to be essential for reduced kerf and slice breakage. It also gave valuable information as to the state of the cutting edge profile and the tension of the blade core material.

In the area of blade development, the use of prefabricated blade inserts, consisting of nickel rings impregnated with diamonds, was investigated. This investigation was terminated prior to its completion, and no results were obtained.

An alternative method of blade construction was investigated. Through a precision etch process, material was symmetrically removed on both sides of the blade near the cutting edge. The nickel/diamond cutting material then was applied to this region. This configuration permitted low-kerf slicing (achieving a cutting edge width of 127 μm), but further refinement of the process is necessary to achieve greater blade lifetime.

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Two beryllium copper blades were designed, constructed, and tested. This material was selected for its increased ductility. Performance of the blades seemed consistent, exhibiting very low natural deflection, differential expansion, and loaded deflection. Slice bow, however, was about twice that of stainless steel because, with beryllium copper (a softer material), resistance to blade deflection was less. This disadvantage, together with the fact that slicing speeds with the beryllium copper blades had to be reduced, led to discontinuance of this approach.

Key Accomplishments. The key accomplishments of Siltec Corp. R&D are:

(1) Low blade life and low productivity prevented ingot rotation from being an economical solution to low-kerf slicing of silicon ingots.

(2) Dynamic cutting-edge control is an important element to reduce kerf.

b. *Silicon Technology Corp.: ID Wafering of Silicon for Solar Cells.* Silicon Technology Corp. (STC) performed an empirical parametric study of ID wafering on 15-cm-diameter and 10-cm-square ingots (References 34 and 35). Specifically, the goals of the work were to achieve 17 to 18 wafers per centimeter length from 15-cm-diameter ingots, and 25 wafers per centimeter from 10-cm circular or square ingots. Improved throughput rate was a secondary goal of the contract.

Both plunge cutting (straight through the ingot) and rotational cutting were used in the study. The standard 22-in.- (56-cm-) diameter ID saw (Figure 26) was used for all slicing operations except plunge-cutting the 15-cm round ingots, for which a prototype 32-in (81.3-cm) saw, capable of slicing 20-cm ingots, was employed. Both 15- and 10-cm round ingots were rotated, while slicing, but the 10-cm square ingots were plunge-cut only.

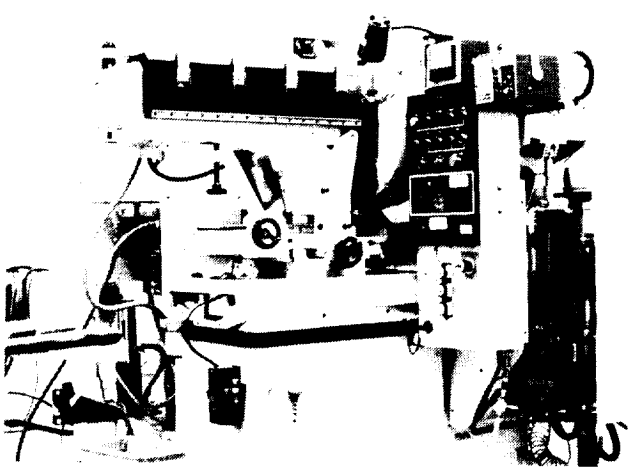


Figure 26. Microprocessor-Controlled ID Saw Made by Silicon Technology Corp.

Results and accomplishments of the study are as follows:

(1) Plunge slicing of 10-cm-square, fine-grained polycrystalline material achieved >90% yield with 23 to 26 thin wafers/cm (0.13 to 0.15 mm thick with 0.28-mm kerf) at 2.5 cm/min plunge rate, or thick wafers (0.25 to 0.3 mm) at 6.3 cm/min.

(2) Plunge slicing of 15-cm-diameter ingots achieved <85% yield with 16 slices/cm at 3.8 cm/min plunge rate.

(3) Rotating the ingots produced <21 wafers/cm at acceptable yields (0.23-mm wafers, 0.24-mm kerf) from 10-cm-diameter ingots, but unacceptable breakage of the 15-cm-diameter material even with very thick (0.5-mm) slices.

(4) IPEG analysis indicated \$25 to \$42/m^2 add-on costs for the plunge-cutting options studied, compared to the cost goal allocation of \$13.70/m^2 (1980 dollars).

Present Status. Although substantial automation of the ID wafering process had been implemented since the termination of wafering technology development in the FSA Project, process cost and productivity have not improved appreciably since 1981. Blade technology, the key to kerf reduction, is unchanged.

c. *JPL Modeling of ID Sawing.* The efficient use of silicon was critical for the FSA Project. A variety of slicing techniques were investigated to minimize wafer thickness and kerf. It would be more cost effective to produce larger-diameter silicon Cz solar cells. It was anticipated, however, that greater thickness would be necessary for larger-diameter wafers to withstand wafering, cell processing, and handling. No means of quantifying this anticipated thickness increase was available to provide standards or guidelines for cell manufacturers.

Analytical models were derived by using fracture mechanics analysis. These models were used as a guideline to estimate minimum silicon wafer thickness versus diameter requirement for ID sawing (References 36 and 37) and rotated ingot ID sawing (References 38 and 39) in terms of wafer surface damage and sawing parameters (cutting rate and blade vibration). Important controlling factors for each sawing technique were suggested to produce minimum thickness wafers. The model also indicated the minimum wafer side support required for ID sawing for various wafer thicknesses at any diameter. The fracture mechanics analysis of rotated-ingot ID sawing predicted that a minimum wafer thickness was about 0.15 to 0.2 mm for conventional sizes of rotated-ingot wafering. Fractures through the thickness of the wafer rather than through the center core were found to limit the minimum wafer thickness.

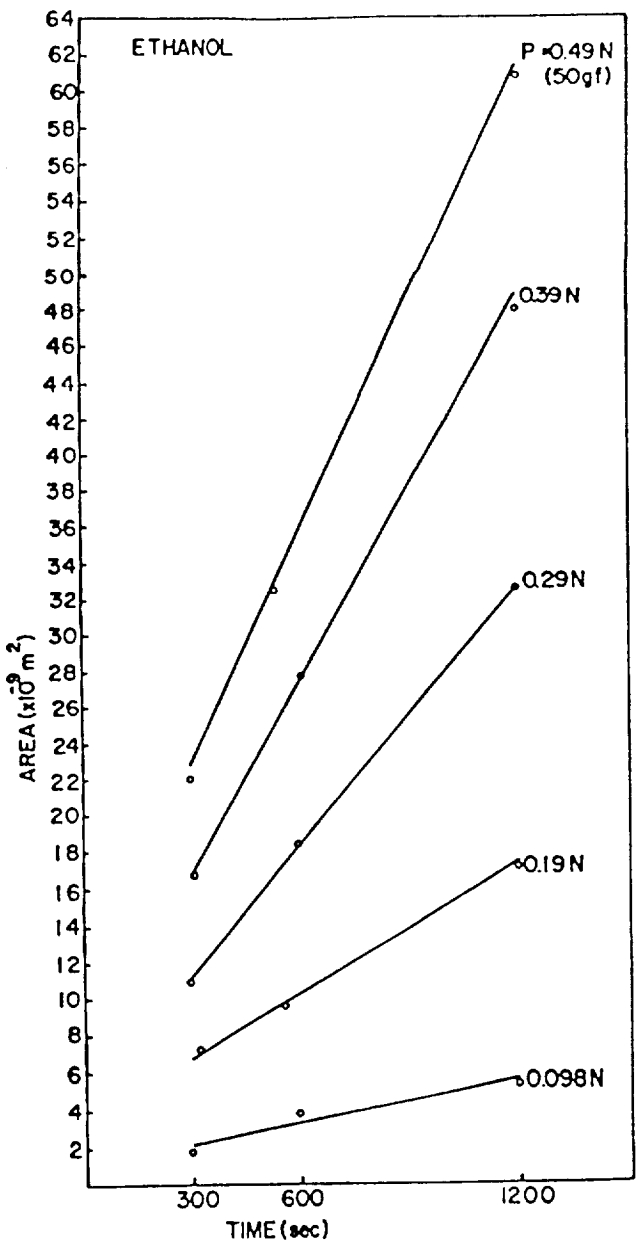
The model suggested that for <111> silicon ingots, the use of a vacuum chuck on the wafer surface to enhance cleavage fracture of the center support core has potential for reducing minimum wafer thickness.

5. Surface Property Modification of Silicon by Fluid Absorption: University of Illinois at Chicago.

Wafering of silicon generally involves abrasive wear by the rubbing of diamond-impregnated wheels or wires. A fluid environment normally is used to cool the contact region and carry away the debris. The University of Illinois at Chicago (UIC) simulated the wafering process by using their own slow-speed and high-speed scratching apparatuses. They also performed indentation tests. The results of these experiments were compared with a space charge model.

a. *Slow-Speed Scratching Test.* Two slow-speed scratching test apparatuses were constructed. A circular, multiple-scratch test facility was used to generate grooves in Cz silicon, and the cross-sectional area of the grooves was examined and measured in the scanning electron microscope (References 40 and 41). Grooves were produced when the silicon surface was immersed in ethanol, methanol, acetone, and deionized water. Radical differences in the groove surface morphology were observed as a function of fluid environment. The groove cross-sectional area formed in ethanol was significantly larger than that formed in the other fluids. Figure 27 demonstrates that, for a given dead-weight load on the scratching diamond, the groove area formed in ethanol is twice as large as the groove formed in deionized water. These results have also been disclosed in a patent application and a NASA Tech Brief. The dielectric properties of the fluid were found to be correlated with the wear rate, which was able to be predicted assuming that the hardness of the silicon is known. These results have shown that the load, dielectric constant, and hardness are critical parameters that influence the wear rate and surface damage (Reference 42).

An apparatus used to form linear scratches also was constructed. A dead-weighted diamond, instrumented with strain gauges, scratches a fixed Cz silicon wafer surface. The groove depth and width, and the damage beneath the groove, depend on the load and fluid used in the experiment. Figure 28 shows scanning electron



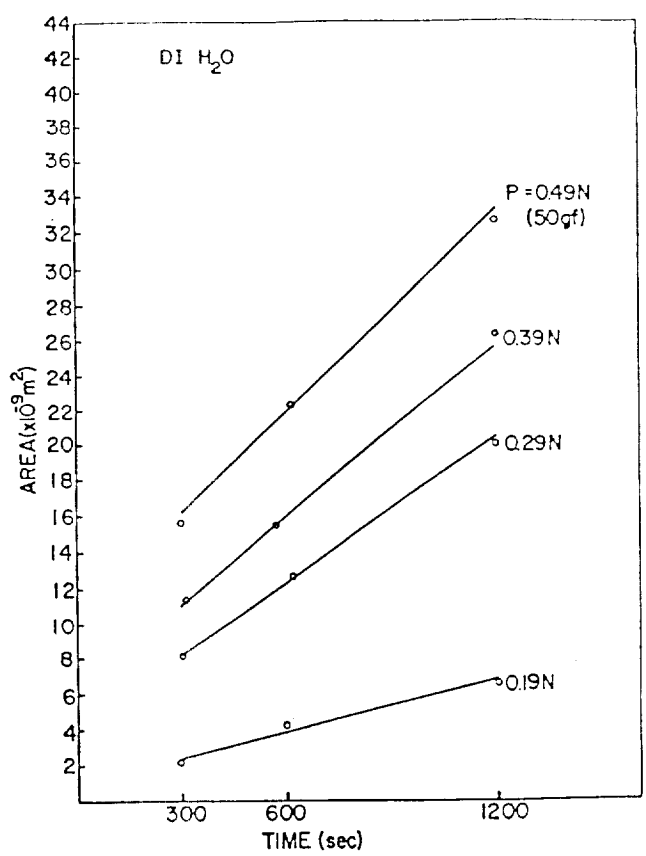
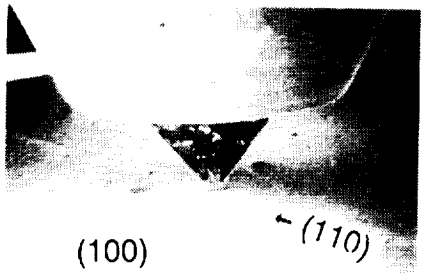


Figure 27. Cross-Sectional Area Versus Abrasion Time for Grooves Formed in Ethanol and Water when the Dead-Weight Load on the Diamond is Varied



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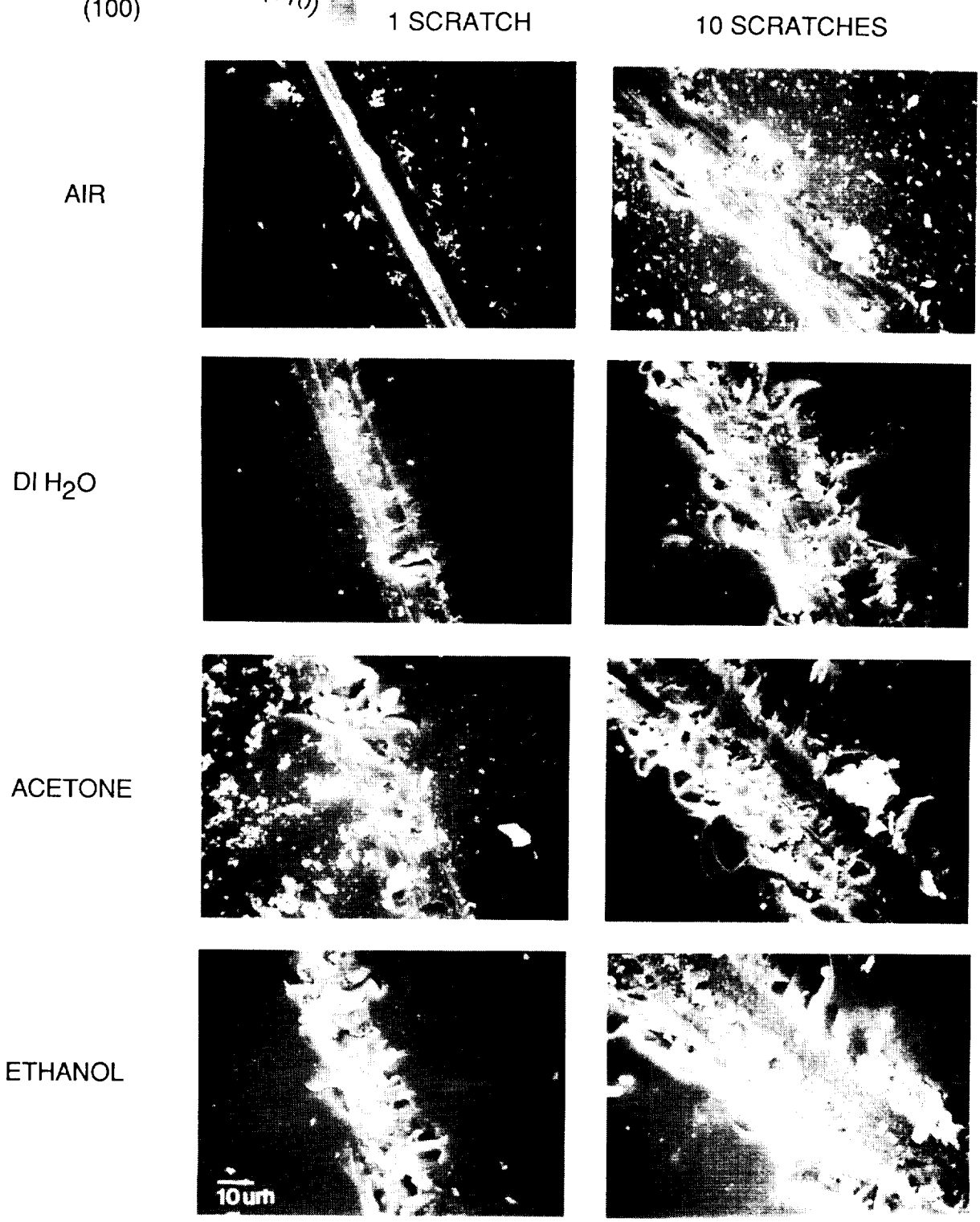

Figure 28. Scanning Election Micrographs of a Single Scratch and Multiple Scratches Formed in Various Media by a Vickers Pyramidal Diamond at a Load of 0.49N

microscope (SEM) micrographs of the surface morphology of a single scratch and 10 scratches formed in ethanol, methanol, deionized water, and air. The scratched surface morphology, debris distribution and size, and the scratch width depend on the fluid in contact with the silicon surface during the test.

Four-point, bend-fracture, stress measurements were conducted on these linear grooves, and the tensile residual stresses corresponding to the subsurface damage were obtained (Reference 43). The residual stresses are 15.6 and 99 MN/m^2 associated with the damage generated in deionized water and ethanol, respectively.

b. *Indentation Tests.* Vickers diamond indentation tests were carried out both at room temperature in fluids and at high temperatures in a laboratory air environment. The indent diagonals were used to obtain hardness as a function of the dielectric constant of the fluids (Reference 44). These data showed that fluids and loads influence the hardness measurement. If the indents are etched in a dilute Sirtl solution, then (in addition to the indent diagonals) a damage zone is visible along with median and radial cracks. Figure 29 shows the variation of the damage zone morphology and size with surface orientation and bulk doping for tests in sodium iodide at room temperature.

The indentation results showed that plastic deformation is generated at loads below 0.98N and that cracks predominate at loads greater than 0.98N.

c. *High-Speed Cutting.* A high-speed, high-temperature cutting facility was constructed to accomplish cutting at a precise feed rate, depth of cut, and fluid environment. The major results of this study were that the surface morphology and debris size analysis indicated the deformation mode. The average debris

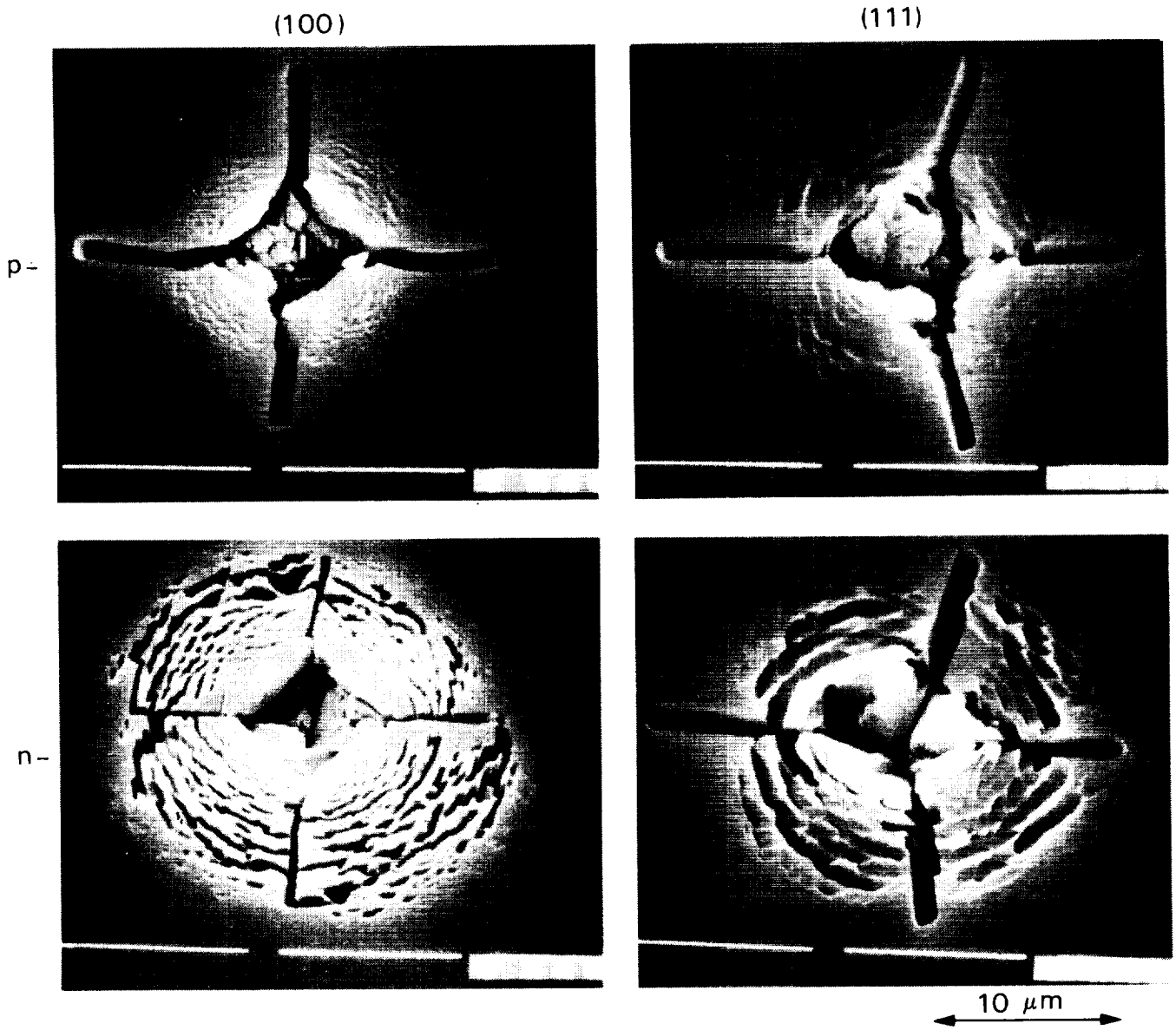

Figure 29. SEM Micrographs of Indentations (P = 0.49N, Sirtl Etch for 25 s)

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size decreased from 1.7 to 1.0 μm when the temperature is raised to 100 °C for cuts made in air. At room temperature, the average debris size increased from 1.7 to 5.6 μm for cuts made in air and ethanol, respectively.

The surface morphology of the groove also varied with fluid and temperature. As temperature increased, the ploughed regions broadened by a factor of two.

d. *Deformation Model.* The damage formed during scratching and/or indentation was modeled by dislocations propagating in the space charge field of the silicon. The surface of the silicon was described by a limited number of surface sites that may interact with fluids or adsorbates. Because the surface sites are limited, they may not sustain the surface charge necessary for equilibrium, and the extent of the space charge region may vary with the surface site density and energy as well as the electrochemical potential. The Debye length, which may be calculated by this model, is related to the damage zone (generated by indentation) because dislocations must propagate in the space charge field.

C. SUMMARY

Nine groups engaged in R&D programs to advance the technology of silicon ingot wafering. Their work included evaluation and development programs for standard techniques (ID saws and multiblade saws), evaluation and development of novel and new wafering technologies (including a free-abrasive wire saw), and studies aimed at achieving a basic understanding of the mechanisms of cutting silicon.

OCLI assessed the state of the art of the technology available for sawing large-diameter ingots by performing a series of slicing experiments using various wafering methods.

Under two separate contracts, Norlin Industries (Hoffman Division) conducted technology assessment and development of the free-abrasive, MBS sawing process. As a result, MBS became better understood as a candidate wafering technology. The design and development of a 1000-blade saw was terminated early because of redirection of the FSA Project.

Varian conducted an effort dealing with multiple-blade saw technology, including construction of a 1000-blade saw and economic analysis of MBS technology. Operation of the saw was plagued by problems, and the saw did not achieve its expected performance.

Solarex performed a parametric wafering study that essentially was a test of a Yasunaga free-abrasive, multiple-wire saw in a production environment. Wafering tests were made over ranges of operating parameters, the product wafers were characterized (including determination of the depth of damage), and the practicality of module fabrication using thin wafers was evaluated.

CSI developed the FAST wafering process that employed a saw having diamond-impregnated wires. The ability to slice 25 wafers/cm from a 10-cm-diameter ingot with greater than 99% yield was demonstrated. The FAST saw also was able to slice 19 wafers/cm from 15-cm-diameter ingots, although the yield was low.

JPL conducted studies that included a MWS saw development, evaluation of blades in support of multiple-blade sawing, and analytical modeling of ID sawing and rotated-ingot ID sawing techniques.

Siltec pursued a program to enhance ID sawing technology by achieving a significant increase in the number of usable slices per unit length of ingot as compared to industry practice. Extensive experimentation was performed with ingot rotation, but limitations to the technique remained. The effectiveness of a cutting-edge position control was demonstrated.

STC performed an empirical parametric study of ID wafering on 15-cm-diameter and 10-cm-square cross-section ingots. Goals of the program were to achieve certain numbers of wafers of specified thickness per unit length for cylindrical and square ingots, and to obtain improved throughput.

UIC conducted a program to develop an understanding of the basic mechanisms of the deformation of silicon when silicon is cut in the presence of lubricants. UIC also developed a nondestructive measurement technique for residual stresses in thin, flat-sheet silicon.

SECTION IV
Ribbon Growth

A. INTRODUCTION

Silicon sheet conventionally is produced by sawing Cz-grown ingots into individual wafers. This process, developed for the semiconductor industry, yields silicon wafers of excellent quality, but of high cost. An obvious way to circumvent the problems inherent in the ingot-to-wafer technology is to grow silicon in sheet form of the desired thickness directly from the melt. From the start of the FSA Project, development of such silicon ribbon growth processes received considerable emphasis. Most approaches required feasibility demonstration, because the specific technique involved had not been used for silicon if at all.

At the beginning of the FSA Project, many sheet-growth concept studies were supported, especially those involving ribbon. Periodic reviews reduced the number of options to the most promising few, but from time to time newly proposed concepts were considered and supported. The ribbon technologies that received the the greatest support over the life of the Project were:

(1) Edge-supported film-fed growth (EFG), at Mobil Tyco.

(2) Capillary action shaping technique, at International Business Machines (IBM).

(3) Dendritic web, at University of South Carolina, Westinghouse, and JPL.

(4) Inverted Stepanov, at RCA Laboratories.

(5) Ribbon-to-ribbon (RTR) laser zone crystallization, at Motorola/Solavolt.

(6) Low-angle silicon sheet (LASS) process, at Energy Materials Corp.

The EFG, CAST, dendritic web, RTR, and inverted Stepanov processes all involve vertical or near-vertical growth where heat removal is symmetrical or nearly so. The LASS process, however, involves asymmetrical heat removal.

In early 1982, almost all work on ingot technologies was terminated in accordance with DOE guidelines, and the development of sheet growth processes was concentrated into two ribbon efforts deemed to offer the highest probabilities of success: the dendritic web process at Westinghouse Electric Corp., and the EFG process at Mobil Tyco Solar Energy Corp., now known as Mobil Solar Energy Corp. (MSEC). At the same time, emphasis and support was placed upon understanding and controlling the fundamental limitations to ribbon technology.

In the use of these ribbon processes, two factors have been, and continue to be the limitations to meeting the DOE module price goal of $0.50/W_p$.

(1) Generation of stresses and consequent strain as ribbon growth rate is increased to achieve the required throughput.

(2) Formation of defect arrays and structures that act to limit solar cell conversion efficiencies.

Two Supporting Studies contracts were also awarded: solid/liquid interface studies at Solar Energy Research Institute (SERI), and analysis of high-speed growth of silicon ribbon in inclined-meniscus configurations at Massachusetts Institute of Technology (MIT). The SERI program is covered in Section VI, and the MIT effort is described in Section VII.

Two other ribbon growth techniques that were supported by DOE (edge-supported pulling at A.D. Little and edge-supported ribbon at SERI) are not covered in this report because they were not part of the FSA program.

B. IMPLEMENTATION

1. Shaped Ribbon Growth

a. *Mobil Solar Energy Corp.: Edge-Defined Film-Fed Growth, Process Development.* In the EFG process, silicon ribbon is pulled from the top of a die through which molten silicon is fed by capillary action (Figure 30). The molten silicon wets the top of the die and extends out to the outer edge of the die top. Thus, the cross-sectional shape of the ribbon pulled from the molten silicon is defined by the shape of the top of the die.

In 1975, in response to the general sheet growth Request for Proposal (RFP), Tyco Laboratories, Inc. proposed an effort to develop the EFG process to produce low-cost silicon sheet. The EFG process originally had been developed for growing sapphire ribbons, and some preliminary work involving silicon had been done under National Science Foundation (NSF) and NASA support prior to the RFP. This EFG technology development continued to the end of the FSA Project, and still continues under corporate support. The EFG technology development supported by the FSA Project focused entirely on ribbon quality and cost (References 45 and 46). Parallel elements of development involving cell processing and module preparation were entirely supported by MSEC. For this reason, information concerning specific cell processing procedures is not available.

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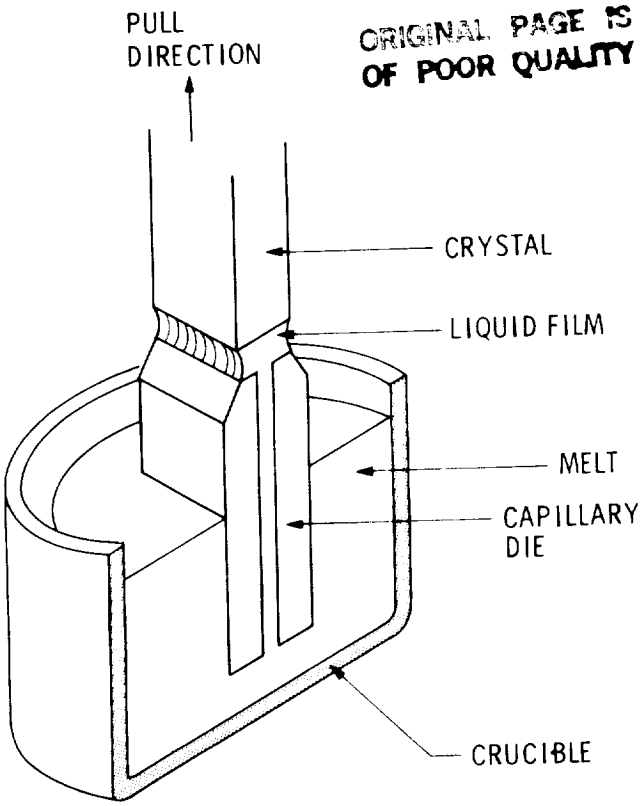

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Figure 30. Schematic of Edge-Defined Film-Fed Growth Process for Silicon Ribbons

Early economic analysis established the throughput requirements for cost-effective ribbon to be about 200 cm^2/min total of ribbon per machine. Evaluation of the technology suggested multiple ribbons and individual ribbon growth speeds of 40 to 50 cm^2/min. During the 11-year course of the program, the technical approach to the achievement of this throughput was modified, but the technology goal remained.

Work during the early years (1975 to 1977) focused largely on the establishment of growth conditions, materials of construction, melt replenishment methods, and other technology requirements necessary to achieve reproducible ribbon growth. Technology developments included the introduction of both cooled thermal elements near the growth interface to extract the heat of fusion, and a controlled gradient exit furnace needed to reduce stresses introduced by the rapid cooling from the cold elements. Many early ribbons, produced through the use of only the cold element, literally exploded from stress.

During the middle years of the technology development (1978 to 1981), major emphasis was placed on the design, development, and operation of several multiple-ribbon growth machines. Early designs were directed at ribbon widths of 7.5 cm and growth speeds approaching 7.5 cm/min, but it ultimately was concluded that these speeds were unreasonable because of the inability to control stress of the ribbons. Detailed technical goals were established for four ribbons 10 cm wide at 4.5 cm/min.

A photograph of a multiple-ribbon growth machine ultimately developed is shown in Figure 31. By 1981, preliminary operating characteristics of the machine had been determined for growing three 10-cm-wide ribbons. Growth speeds as high as 3-1/2 cm/min were achieved as compared to the required 4-1/2 cm/min, with duty cycles of about half that required. This corresponds to about 30% of the area growth rate required. Even at these speeds, the primary problem was the development of stress during ribbon growth. In contrast, lower speed growth could be demonstrated at high duty cycle (but not continuously) for periods approaching 1 week. Late in 1981, the FSA Project was redirected from demonstration of technology development to research involving the understanding of the more fundamental problems in ribbon growth. This resulted in termination of FSA support for multiple ribbon development.

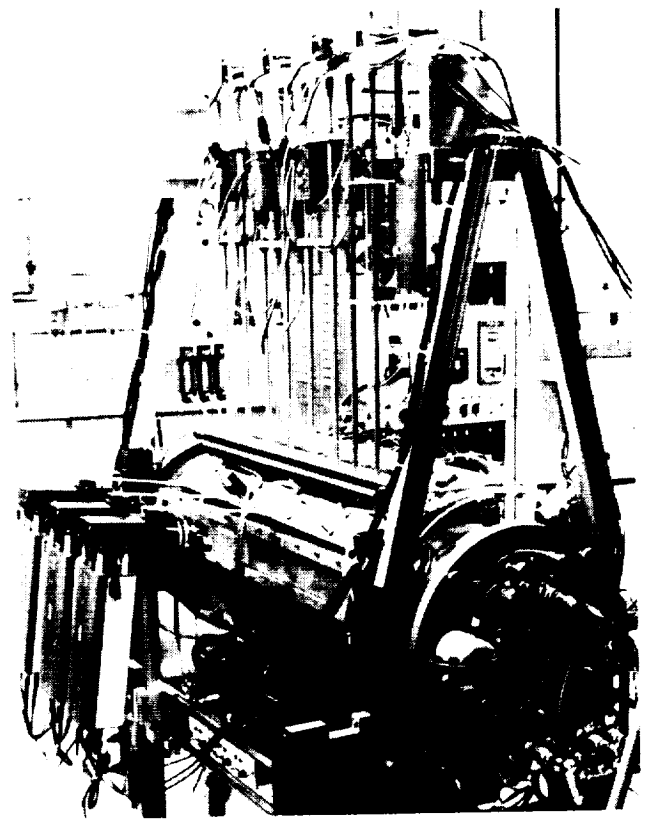

Figure 31. Multiple-Ribbon Furnace for Edge-Defined Film-Fed Growth

However, under support of MSEC, both the latter stages of multiple ribbon development and a parallel effort of a new form were carried out to produce silicon ribbons. This consisted of growth of a closed form of ribbon having nine sides (nonagon) with each side being slightly greater than 5 cm across. The nonagon was cut into nine 5-cm-wide strips. This technique is capable of producing nearly 150 cm^2/min, at pull speeds of about 3 cm/min. This production rate amounts to 0.90 m^2/h, nearly equaling the FSA Technology Readiness goal of 0.96 m^2/h.

Also, during this program's middle years, many associated technologies were developed that are important to the present and future development of ribbon growth. An automated ribbon growth control system was designed and developed. It uses optical monitoring of the ribbon during growth to control thermal elements in the growth system to maintain dynamic stability. A unique anamorphic television camera was developed that provided a height-to-width magnification ratio of 40 to 1. The system demonstrated the ability to control ribbon growth for periods of tens of hours without operator intervention.

A special carbon-silicon thermocouple was developed to map the temperature distribution in silicon ribbons. Carbon threads were attached to the silicon ribbon by means of graphite cement and the outputs were read with a sensitive voltmeter.

Considerable effort was expended in evaluation of the effect of oxygen and carbon on solar cell performance. Table 5 is a summary of early cell results in these studies. Although the detailed mechanism for the role of carbon and oxygen in silicon photovoltaics remains unclear at this time, its importance cannot be challenged.

The ability to slant the liquid-solid interface by the position of the EFG die tops was demonstrated to be useful in moving silicon carbide precipitates to the last material to crystallize. The side containing these precipitates then could be placed at the back of the solar cell to prevent junction penetration.

A major discovery concerning the growth of EFG ribbon was the existence of an "equilibrium defect" structure that developed after a period of growth. The structure exhibited a <110> growth surface with a <112> growth direction and had a large quantity of twins nearly parallel to the growth direction and perpendicular to the ribbon surfaces. Neither the mechanism for the formation of these twins nor their role in growth or stress is fully understood. It has been observed that large quantities of closely spaced twins (<10 μm) are frequently free of dislocation and not harmful to solar cell performance. In contrast, regions without twins often exhibit higher dislocation density and reduced cell efficiency. Seeding of this "equilibrium defect" structure has been considered and is sometimes effective (Reference 47). The generation of silicon carbide particles and other structure-perturbing elements during growth, however, produces continuous variations in the structure, and the equilibrium structure is essentially independent of the seed structure. This equilibrium structure is fundamental to semiconductors and has been observed in other ribbon growth approaches described in this report (RTR and SOC) and in other semiconductors (laser-recrystallized GaAs).

In 1981, with reorientation of the FSA Project toward research concerning the limitations of ribbon growth, support for the MSEC TD was terminated, and contract effort focused largely on problems of mechanical strain and its understanding and control. Studies included heat flow modeling, growth cartridge design and construction, and evaluation of macroscopic structural and electrical characteristics of grown ribbon. These studies have contributed greatly to the understanding of stress limitations during ribbon growth. As part of this study, preliminary mechanical properties of silicon, including FZ, Cz, and EFG silicon, were measured to temperatures of about 10°C below the melting point of silicon. Supporting studies also were conducted at Harvard University by J. Hutchinson and by R. Brown at MIT. These studies partly were supported by MSEC and partly by the FSA Project.

Table 5. Performance Data for Solar Cells Made From EFG Ribbon (100 mW/cm^2; ELH Lamp, 28°C; AR Coated; 14 cm^2)

Process	Ambients Condition	J_{sc}, mA/cm	V_{oc}, V	Fill Factor	η, %
PH_3 900°C	CO_2 off	22.2	0.523	0.738	8.7
		18.7	0.499	0.723	6.8
		22.7	0.530	0.732	8.9
		18.9	0.501	0.731	7.0
		23.1	0.534	0.760	9.4
	CO_2 on	28.0	0.570	0.721	11.6
		28.8	0.580	0.698	11.8
		28.1	0.574	0.717	11.7
		26.4	0.562	0.695	10.4
		26.9	0.565	0.730	11.2
		27.5	0.573	0.727	11.6
		26.3	0.560	0.730	10.4
		27.3	0.573	0.714	11.3
		26.1	0.562	0.739	11.0
		26.1	0.560	0.741	10.9
		25.2	0.555	0.738	10.4
		26.2	0.563	0.765	11.4

Key Accomplishments. The key accomplishments of the MSEC R&D are:

(1) The EFG process for the preparation of low-cost silicon sheet was demonstrated to be practical. Although the technology had not demonstrated all the requirements for the achievement of DOE goals, it showed sufficient performance to receive major industrial support, and has been industrialized and commercialized by MSEC in a somewhat modified form.

(2) The importance of control of stress during ribbon growth was clearly identified, and many contributions to its control were developed.

(3) An optical control system was developed to automate the process for the industrial production of silicon material.

(4) The importance of carbon and oxygen in the growth and performance of silicon ribbons was identified.

b. *International Business Machines Corp.: Capillary Action Shaping Technique.* A study of ribbon growth by means of a capillary action shaping technique (CAST) was conducted at IBM (Reference 48). The basic mechanism of CAST growth is identical to that of the EFG process. In addition to the crystal growth and related characterization and performance evaluation studies, analyses were made of the economics of the process and related means of producing sheet.

This CAST program was a continuation of efforts initially supported by NASA to evaluate the potential for shaped crystal growth as a means of shaping silicon for PV applications. The continuation program placed greater emphasis on the understanding and the potential for the control of the growth process rather than on the empirical development of the growth process. In spite of this emphasis on understanding, demonstration results were very good.

The scale-up of growth width from about 1 to 10 cm by the time the program ended involved many technical developments. These included early awareness of the importance of stress and strain in the stability of ribbon growth, and the development of thermal modifiers above the crystallization point to contour properly the temperature gradient. Analysis of the growth rate provided one of the early definitions of the limits to growth rate as controlled by the rejection of the heat-of-fusion (Reference 49). Also, the use of controlled gas flows was found to be an important factor in modifying the behavior of the crystallization front.

The use of alternative die materials also was investigated (Table 6). In general, it was concluded that these alternative die materials offered little potential for improvement of the ribbon purity and structure. Other die materials exhibited gross reactions with the silicon and could be totally rejected.

Other studies involved control of the fluid behavior in the capillary die to distribute impurities (intentional and unintentional) within the growing ribbon. It was found that the use of a higher-than-ordinary meniscus was capable of reducing the silicon carbide particle density on the surface of the ribbon from $5/cm^2$ to less than $4 \times 10^{-3}/cm^2$. These silicon carbide particles interfered with processing and often resulted in short circuits in the junction of a fabricated solar cell. It was further determined that ribbon resistivity could be tailored by means of fluid flows across the width of the capillary die. By controlling the transverse fluid flow, ribbons could be produced with controlled variations in resistivity across their width.

An effective technique was developed for quickly determining the generation lifetime in a piece of ribbon over a large area. A series of metal-oxide-semiconductor (MOS) capacitors (0.5 or 0.15 mm in diameter) were produced for generation lifetime measurements. They then were evaluated by a computerized system. Results were compared with detailed structure within the ribbons and on a coarser scale with solar cell performance. An outgrowth of these studies was the correlation of ribbon structure with defects. A summary of this ribbon quality evaluation is shown in Table 7.

In addition to these general conclusions, many detailed structural evaluations yielded an improved understanding of the source and role of defects in silicon. One study, using transmission electron microscopy (TEM), defined the epitaxial growth of silicon carbide films on silicon surfaces. Numerous other studies of similar detail are presented in the Final Report (see Reference 48).

Solar cells routinely were produced in this program primarily as analytical tools in the understanding of defect generation and its control. Baseline cell processing was used on 1 to 2 Ω-cm material, and efficiencies of nearly 12% were produced.

The second major element of this program at IBM involved an economic analysis of the ribbon growth process as a source of sheet for low-cost terrestrial photovoltaics. The study used a decision analysis approach called Photovoltaic Energy Conversion Analysis (PECAN). The technique employed an economic evaluation of the cost of the various direct and indirect elements involved in the production of ribbon and included labor, capital recovery of equipment, materials, services, and supplies. Scenarios were developed based on reasonableness of technical accomplishment, and final sheet costs were developed.

The results provided support for the selection of this and similar ribbon technology as a means of satisfying grid-connected power applications. At the time of analysis, sheet costs of \$25 to $\$50/m^2$ (1975 dollars) were projected for 1986 with the upper limit based on existing technology at the time of analysis. Ultimately, target prices of about $\$20/m^2$ were developed for the Project. These early results emphasized the need for technical developments to achieve the required Project goals.

Table 6. Die Material Evaluation

Material	Capillary Rise	Durable In Molten Silicon	Ribbon Growth
Aluminum boride[a]	--	--	--
Titanium boride	Yes	No (dissolves)	Short ribbons
Zirconium boride	Yes	No (dissolves)	Short ribbons
Aluminum carbide[b]	--	--	--
Boron carbide	Yes	Yes	Long ribbons
Silicon carbide	Yes	Yes	Long ribbons
SiN bonded SiC	No[c]	Somewhat	None
Vitreous carbon	Yes	Yes	Long ribbons
Graphite (dense)	Yes	Yes	Long ribbons
Boron nitride	No	Yes	None
Silicon nitride	No[c]	Yes	None

[a]Vapor pressure too high at 1412°C.
[b]Decomposed and crumbled during storage.
[c]Evidence of surface wetting, but no rise in capillary slot.

Table 7. Evaluation of Quality of Ribbons Grown by the Capillary Action-Shaping Technique

Class	Lifetime Range, μs	Solar Cell Efficiency,* %	Dominant Defects
I	1 to 10	5 to 8	Coherent twins, stacking faults, dislocations below $10^4/cm^2$
II	0.01 to 1	3 to 5	Non-coherent twins, multiple stacking faults, low-angle grain boundaries, dislocations above $10^4/cm^2$
III	< 0.01	1 to 3	Grain boundaries, dislocations above $10^6/cm^2$
IV	Not measurable	--	Silicon carbide, dendrites on surface
Standard Cz	10 to 500	8 to 12	None

*Measured at AM1, no AR coating.

2. Dendritic-Web Ribbon

The dendritic-web process, originally developed at Westinghouse before the FSA Project and then dropped, produces long, thin, single-crystal ribbon directly from liquid silicon. The ribbon forms by solidification of a liquid film that forms between two silicon filaments, called dendrites, that grow downward into the silicon meniscus and form the borders of the ribbon (Figure 32). The silicon surfaces produced are of a high quality that permits solar cell fabrication without any lapping or polishing, and there is no kerf loss because of slicing. Ribbon thickness is nominally 150 μm, although thinner material suitable for making solar cells can be produced.

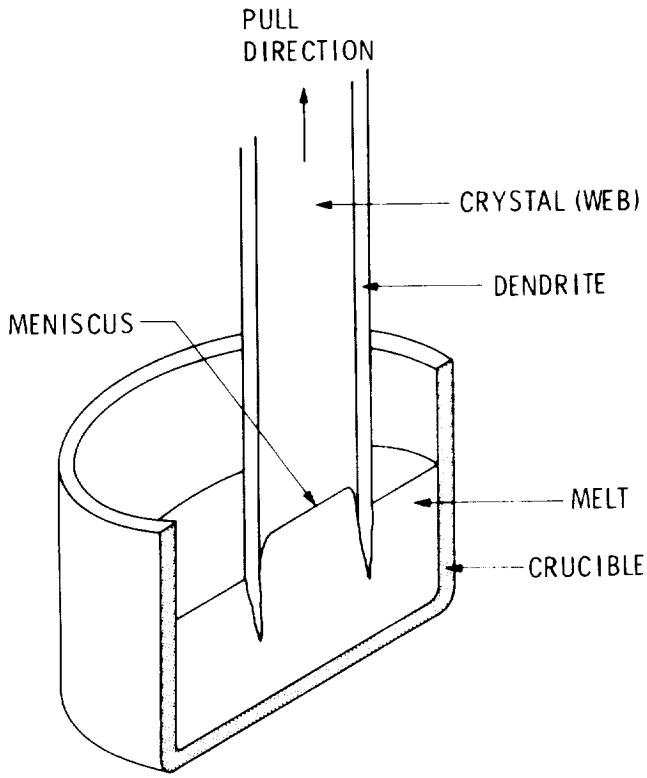

Figure 32. Silicon Dendritic-Web Ribbon (top) and Solar Cell (bottom) (Westinghouse Electric Corp.)

a. *University of South Carolina: Process Development.* The primary objectives of this program (Reference 50), were to:

(1) Activate, operate, and modify an existing silicon dendritic web growth machine as necessary to investigate the role of the various machine design parameters on the growth of ribbon, to support thermal modeling studies, and to obtain a better understanding of the growth process and its limitations.

(2) Characterize the grown ribbon.

(3) Investigate mechanical stability of the silicon ribbon.

(4) Investigate and define thermal stability, and conduct thermal modeling studies.

Parts of a prototype dendritic web growth machine, on hand at the start of the contract, were assembled and put into operation. A program to investigate the role of the various machine design parameters on the growth of ribbon was carried out during the duration of the contract. Development of the machine proceeded to the point where ribbons could be grown reproducibly up to lengths of 1 m, with widths increasing linearly from the width of the seed button initially, up to 1 cm at termination of growth.

Detailed comparisons of the analytical results of ribbon growth with experimental results were not performed because the experimental data were of insufficient detail to make realistic comparisons. General agreement was found, however, with respect to satisfactory pull speeds for ribbon growth. Both theoretically and experimentally, they were determined to be in the range of 3 to 5 cm/min.

To be cost competitive with the Cz process, it was concluded that a ribbon process must have the following capabilities:

(1) Pull speed in excess of 5 cm/min.

(2) A ribbon width at least 5 cm.

(3) Continuous growth (i.e., incorporation of melt replenishment).

It was shown that the 5-cm/min pull speed is attainable, although no value could be set as to the maximum speed. From information obtained on thermal gradients and the length of the opening in the top thermal shield through which the ribbon is drawn, it seemed that 5 cm width would be possible. There was concern, however, about the feasibility of simultaneously attaining the goals of both width and pull speed.

In the thermal modeling studies, mathematical models of dendritic-web ribbon growth were developed to predict both furnace-design parameters that affect this growth, and the temperature distributions in the melt, crucible, susceptor, and thermal shield. It was found that the ribbon pull speed was strongly dependent on the temperature of the top thermal shield, the spacing between this shield and the melt, and the thickness of the growing ribbon.

Key Accomplishments. The key accomplishments of the University of South Carolina's dendritic-web R&D are:

(1) Developed a ribbon-growth machine process to the point where ribbons could be grown reproducibly up to lengths of 1 m with widths up to 1 cm at the point of growth termination.

(2) Determined that to achieve suitable growth, the mechanical system must be very rigid and stable.

(3) Determined that certain twin spacing in the seed favors high ribbon-pull speeds whereas other spacings are unfavorable.

(4) Determined that the ribbon pull speed strongly is dependent on the temperature of the top thermal shield, the spacing between this shield and the melt, and the ribbon thickness.

b. *Westinghouse Electric Corp.: Process Development.* Since April 1977, the FSA Project has continuously supported development of the silicon

dendritic-web ribbon growth process at Westinghouse (References 51 to 54). The objective of the effort has been to demonstrate the feasibility of the process and advance its technology to the point of readiness for commercial application. A section of dendritic-web ribbon and a solar cell made from this material is shown in Figure 33.

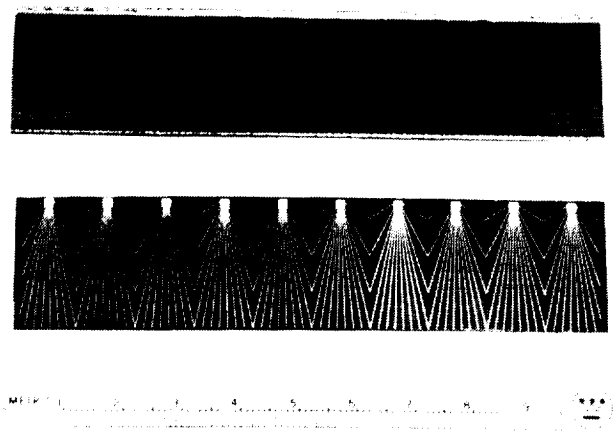

Figure 33. Schematic Diagram of Silicon Dendritic-Web Ribbon Growth Process

A larger program directed by DOE, initiated early in 1984, involved development by Westinghouse of dendritic-web ribbon and high-efficiency solar cells made from this material. It is a 3-year effort jointly funded by the DOE (through both JPL's FSA Project and SERI), Westinghouse, the EPRI, the Southern California Edison Company, and the Pacific Gas and Electric Company. The program is aimed at developing the technology required for use by electrical utilities.

A cross-sectional view of the growth configuration, including the shield/stack located above the susceptor lids and used to determine the thermal profile of the cooling ribbon, is shown in Figure 34. Shield/stack configurations that lead to improved growth are arrived at by an iterative process involving modeling and computer simulation of the web growth process, including the thermal environments produced by web growth systems, and by testing (thermal probing as well as ribbon growth). Two dendritic-web ribbon growth systems are shown in Figure 35.

Experiments are conducted to verify the model predictions and computer simulations and to provide data by which the furnace configurations and process parameters could be modified to achieve improved ribbon growth. The lateral (horizontal) temperature profiles in the melt and ribbon, as well as the temperature profile along the cooling ribbon, are important factors affecting the stress and, therefore, the quality of the ribbon. Westinghouse has determined that concave-downward ("frowning") lateral thermal profiles along the cooling ribbon are desirable for producing low-stress ribbon. Figures 36 and 37 show the maximum width of ribbon and the maximum length of ribbon,

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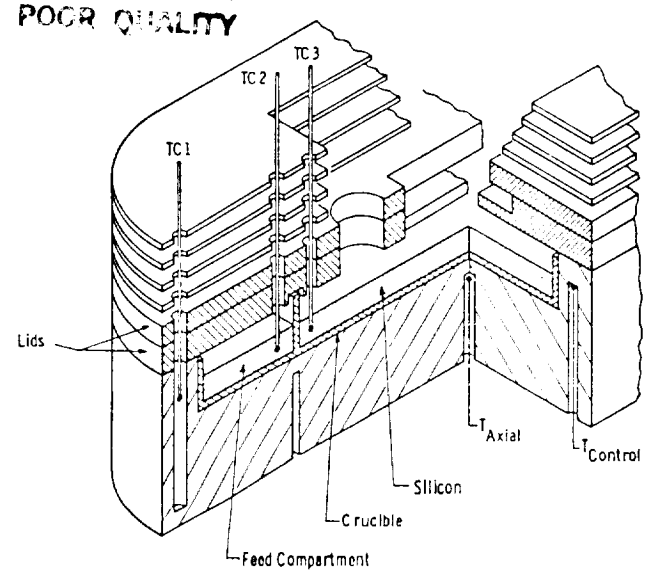

Figure 34. Sectional View of Dendritic-Web Ribbon Growth Configuration (Westinghouse)

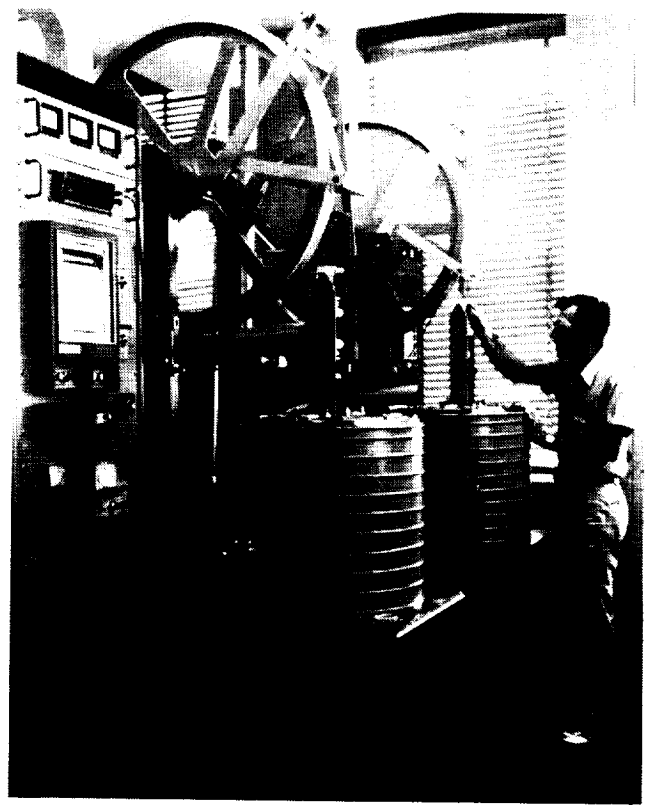

Figure 35. Two Westinghouse Dendritic-Web Ribbon Growth Systems

respectively, as functions of time. Use of an improved model was introduced in 1982, and (as can be seen from Figures 36 and 37) progress toward increasing ribbon width and length improved dramatically.

An important feature for reducing ribbon cost is the use of automated (unattended) ribbon growth.

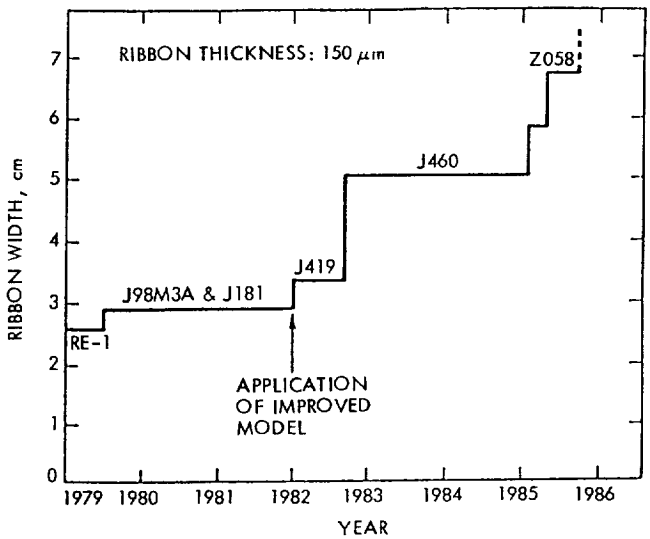

Figure 36. Maximum Width of Undeformed Dendritic-Web Ribbon for Period 1979 to 1986

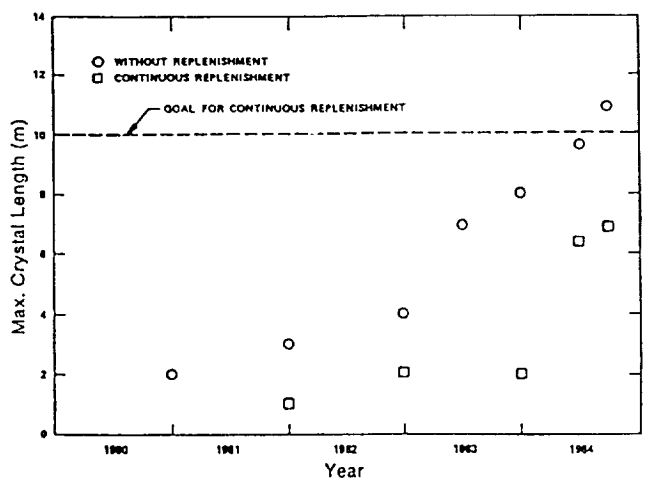

Figure 37. Maximum Length of Dendritic-Web Ribbon for Period 1960 through 1964

Such operation provides closer (and more objective) control of the process than can be provided by an operator, and it allows more growth systems to be supervised by each operator, reducing labor cost. From 1984 to 1986, Westinghouse, with the encouragement of both a Technical Advisory Committee and a Management Committee, has been placing heavy emphasis on developing and demonstrating automated closed-loop control of ribbon growth. The control system consists of two elements. One is a melt-level control system in which a laser is employed to sense the level of the silicon melt from which the ribbon is drawn. This information is fed to a melt replenishment system that adds silicon pellets to the melt at a controllable rate to maintain the desired level. The other element of the closed-loop control system employs a dendrite thickness monitor (DTM) to measure the thickness of each of the two dendrites by a non-contact method. This information is used to provide side-to-side temperature control of the melt in the growth region through control of the position of the induction coil that surrounds and heats the susceptor. The average thickness of the two dendrites is used for fine control of the temperature level of the melt, while coarse control is provided by a light-pipe system.

Because growth configurations suitable for starting ribbon growth typically are different from those required for rapid steady-state growth, Westinghouse has investigated the use of dynamic control, wherein selected elements of a growth configuration move during ribbon growth. In the approach employed by Westinghouse, the vertical distance from the bottom of the furnace lid to the ribbon growth interface (the boundary between the liquid and solid portions of the ribbon) was selected to be controlled. Large increases in pull speed, up to 58%, were attained compared to those achieved with corresponding static configurations, but the quality of the ribbon produced at these high speeds was degraded. Investigations of dynamic control were incomplete at the conclusion of the Project.

Although considerable progress has been made in the advancement of the capabilities of the dendritic web growth process, some formidable obstacles remain that hinder the attainment of program goals. The major problem to be overcome is the limitation on high rates of area growth. Economic analyses (1981) indicate that growth rates of the order of 18 cm^2/min are required on a continuous basis.

Westinghouse has achieved area growth rates as high as 13 cm^2/min for ribbon lengths of under 1 m, but the maximum rate for long ribbons (ranging from 8 to 17 m) of high-quality material was about 6 cm^2/min. When higher growth-speed is attempted, the ribbon often deforms because of excessive stresses in the material. These deformations take the form of buckling, rippling, and twisting and can produce defects that adversely affect solar cell processing yields and device performance. For example, when thermal stresses exceed the material's yield point during growth, plastic deformation occurs. This, in turn, causes a strained crystal lattice when the ribbon is cooled to ambient temperature. These dislocations can deteriorate cell performance. High-stress material also can be unsuitable for cell fabrication because of increased fragility (e.g., it can fracture during cutting). Deformed material also can be unsuitable because lack of flatness interferes with further processing. Several studies related to these problems were carried out at JPL and other laboratories with Project support; these are reported in Section VII.

Other problems relate to premature termination of ribbon growth or interference with proper growth. These problems include the following:

(1) Particulate matter floating in the growth region of the melt. These particles can either be silicon oxide that drops into the melt, or silicon crystals that form on cool regions in the crucible.

(2) Excessive silicon oxide deposits in the growth slot (the slot in the lid through which the ribbon is withdrawn from the melt) that interfere with growth.

(3) The ribbon pulling out from an excessively hot melt.

(4) Formation of extra dendrites in the ribbon.

(5) Degeneration of the ribbon crystal structure into polycrystalline material from high stress or improper growth-interface temperatures.

This variety of problems related to growth speed has caused Westinghouse to fail to meet a goal for throughput, defined as the ribbon area produced in a single furnace in a week's time. However, as shown in Figure 38 and also as described below, Westinghouse has achieved significant increases in this parameter since March 1985.

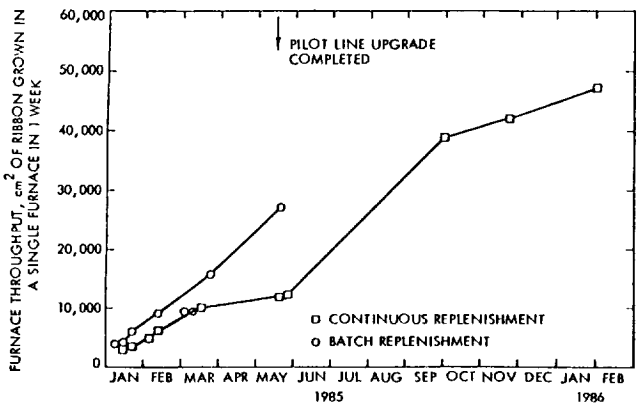

Figure 38. Maximum Throughput for Dendritic-Web Ribbon Furnaces in 1985 and 1986

Key Accomplishments. The key accomplishments of the Westinghouse Electric Corp. R&D are:

(1) Throughput: In June 1986, a single furnace grew 4.7 m^2/week under conditions of nearly constant melt level (melt replenished growth). In February 1985, the record throughput was only 0.93 m^2/furnace-week. Under other support, throughput is expected to continue improving.

(2) Demonstrated closed-loop temperature control of ribbon growth, wherein both the lateral (across the growth region) temperature variation as well as the temperature level were controlled by remote (non-contact) monitoring of the dendrite thicknesses.

(3) Development of melt replenishment process and its use to grow a single ribbon to 17 m length.

(4) Area growth rates of about 6 cm^2/min were achieved for long ribbons (8 to 17 m).

(5) Area growth rate of 13 cm^2/min was achieved for short ribbon lengths (a few tens of centimeters).

(6) Long-term growth with melt replenishment (constant melt level) demonstrated for up to 11-1/2 h, and for no replenishment for up to 18 h.

(7) Maximum ribbon width of 6.9 cm was demonstrated.

(8) Ribbon restart was demonstrated for maximum ribbon width of 6 cm.

(9) High-efficiency solar cells, in the range of 16.0 to 16.9% as measured by Westinghouse, have been made from dendritic web ribbon.

Present Status. As described earlier, Westinghouse is engaged in the third year of a 3-year expanded effort. It started in early 1984 and is aimed at achieving technology readiness of the dendritic web ribbon and associated solar cell technologies. Support from JPL ended in September 1986; however, the program is continuing under support of the other sponsors.

The areas of work are as follows:

(1) Increasing ribbon area growth rate.

(2) Computer modeling to define the thermal conditions required to produce high-quality ribbon at high growth rates.

(3) Further development of the closed-loop growth control system to improve the long-term stability of growth under conditions of high area-growth rates.

(4) Improvement of the melt replenishment process.

(5) Study of the growth interface region to define conditions to increase heat loss (increasing area growth rate) and to improve long-term growth stability.

Technical Needs to Complete. Advancements in two critical technical areas are needed to move the technology of silicon dendritic web ribbon to the point where the process is ready for commercialization:

(1) The foremost requirement is to increase the area growth rate to levels required to attain JPL/DOE PV cost goals. Cost analyses (1981) indicated that for a polysilicon cost of $14/kg, for a cell efficiency of 15% AM1, a growth cycle of 3 days, and semi-automated growth, the ribbon growth plus silicon cost goal of $22.4/$W_p$ (1980 dollars) could be met with a ribbon area growth rate of at least 18 cm^2/min. An updated economic analysis of the ribbon growth process should be prepared.

(2) The other key requirement is to improve (or at least maintain) the ribbon quality so that solar cells with higher efficiencies can be made from ribbon. The cell efficiency goal currently is 17.5% (AM1).

c. *JPL In-House: Web Team.* An in-house effort was established in 1984 to complement and support the web-dendrite R&D program at Westinghouse. The JPL goal was to develop and transfer technology to Westinghouse that would enhance the probability to meet the program goals for web dendritic growth.

The first effort was to obtain a Westinghouse dendritic-web crystal grower. The ribbon grower was received at JPL in February 1985 and, after training at Westinghouse, and assembly, checkout, and initial debugging of the equipment, the JPL team successfully pulled dendritic-web ribbon in April 1985. The initial operating experience indicated it would be highly desirable to instrument the growth system more fully and to monitor simultaneously and continuously more process parameters than previously observed. Most of the basic instrumentation was completed by July 1985. Modifications to the chamber were made to reduce the incidence of water and air leaks and to improve the serviceability of the system.

In August 1985, several batch-replenished runs were made from wide starts. Ribbons achieved greater than 3 m length, and attained the maximum width possible for the growth slot design (4.2 cm). The growth rate was about 5 cm^2/min. The causes of termination of growth were varied, including oxide falling into the melt, extra dendrites, and excessive vibration.

A commercially available two-color pyrometer revealed rapid temperature fluctuations on the surface of the silicon melt, at times as much as $\pm 2\,°C$. The pyrometer proved to be an excellent means of profiling the temperature distribution of the melt surface along the length of the growth slot prior to seeding for growth. The previous method of mapping with a seed, which could take hours and frequently provided unreliable data, was replaced with a 1-min pyrometer scan.

The as-received spatial resolution of the commercial pyrometer viewing the melt surface was 4 mm. Better resolution was desired, but no commercial pyrometers could be found that met the requirements. JPL pyrometer design proved to be highly successful, achieving temperature resolution equivalent to the commercial unit ($\pm 0.5\,°C$) while improving the spatial resolution to the desired 0.5 mm. This instrument was sent to Westinghouse for their use.

A thermal analysis effort at JPL led to several important insights and innovations. Thermal submodels were generated for critical parts of the ribbon growth system. The susceptor, crucible, silicon melt (with and without ribbon), and the ribbon itself were modeled. An immediate result was the finding that controlling the susceptor-crucible gap would eliminate one source of variability in the heat transfer from the susceptor to the melt. Another important finding was that the growing ribbon itself acts as a heat shield that results in a substantially different thermal distribution than had been derived by previous analyses.

The thermal analytical effort was hampered by imprecise or unknown values for properties of materials at high temperatures. The spectral transmissivity of silicon was determined to assess the feasibility of an in-situ web thickness monitor. A secondary result of the transmissivity measurement virtually was to eliminate light-piping as a mechanism for carrying heat away from the growth interface.

Conclusions of the JPL In-House R&D are:

(1) The dendritic-web, crystal-growth process has a wider operating window than previously thought. Compensating trade-offs exist between the critical growth parameters of temperature, pull speed, and web thickness.

(2) Thermal instabilities and imbalances that lead to termination of growth result from unpredictability of the RF coupling to the susceptor and shields and the variability with time of radiating surfaces. Predictable resistance heating should be considered, or another layer of control should be installed between the RF heating and the growth interface.

(3) Additional instrumentation development will be required, both for exploratory purposes and for operational control. This instrumentation includes the JPL high-resolution, two-color pyrometer and the Westinghouse dendrite thickness monitoring system.

(4) Pure heat transfer analysis alone cannot predict the conditions that will lead to successful crystal growth. Experimental observations of such phenomena as button growth lead to the conclusion that solidification along the various crystallographic directions also imposes restrictions. Reconciling the crystallographic and heat flow restrictions is not obvious and requires further consideration.

(5) The control of ribbon buckling requires a forced thermal environment above the melt; these conditions are different from those required for button growth and for the start-up of ribbon growth. A dynamic configuration with better control of the thermal environment seem to be called for.

3. Inverted Stepanov: RCA Laboratories

From March 1976 to May 1977, RCA Laboratories performed work (Reference 55) on inverted Stepanov growth of silicon ribbon. This work was originally begun to provide shaped crystal growth by use of nonwetting dies, as an alternative method to conventional Stepanov, EFG, or CAST processes. The use of nonwetting dies was an attempt to avoid silicon contamination from typical graphite dies used in EFG or CAST processes. Growth in the downward direction was needed to compensate for the lack of capillary rise in the nonwetted dies.

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Fused silica and boron nitride were employed initially as nonwetting dies. Boron nitride was used initially, but because known doping occurred, fused silica dies were designed in a V-shaped geometry for subsequent use. Ribbon growth was not stable from silica dies and these growth instabilities were associated with the formation and evolution of SiO gas. The ribbon meniscus during growth was not "pinned" to the die, but was in constant motion.

Because of ribbon growth problems associated with the die material, alternative die materials were considered. A program that RCA Laboratories conducted on development and evaluation of other die materials for use in the inverted Stepanov process is described in Section VI.

Preliminary evaluation of reactivity of liquid silicon with both CVD Si_3N_4 and $Si_3O_xN_y$ indicated a high resistance to reaction. Eventually, silicon ribbon growth was carried out using CVD Si_3N_4-coated composite dies in the V-shaped crucible curved die configuration. Short duration growth was achieved of a 2-cm-wide, about 0.5-mm thick ribbon.

4. Ribbon-to-Ribbon Growth Process: Motorola, Inc.

The RTR process, supported at Motorola, Inc. (now Solavolt) from February 1976 to July 1979 (Reference 56), is a FZ crystal growth method. A segment of polycrystalline silicon ribbon is fed into a preheated region, heated additionally by a focused laser beam, melted, and then crystallized, still in ribbon form (Figure 39). The liquid silicon is held in place by its surface tension. During this process, the shape of the resulting single crystal is defined by the shape of the feedstock and the influence of surface tension. It was originally expected that the orientation would be determined by that of a seed single-crystal ribbon, brought into contact with the melted upper end

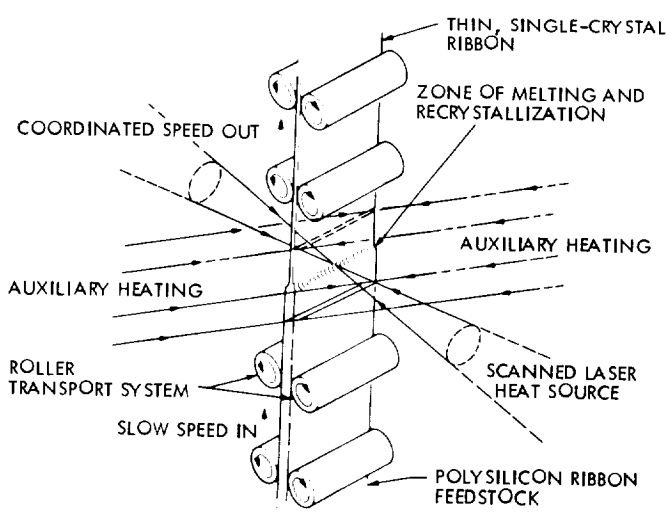

Figure 39. Schematic Diagram of Silicon Ribbon-to-Ribbon Growth Process (Motorola)

of the polycrystalline substrate. In fact, the structure of the product (Figure 40) was the "equilibrium defect structure" described in Section IV.B.1.a. of this report.

Figure 40. Segment of Ribbon-to-Ribbon Showing Defect Structure

The contract goals for the initial phase (feasibility demonstration) of the RTR process were as follows:

(1) Ribbon width, 2.5 cm.

(2) Steady-state linear growth rate, 18 cm/min.

(3) Thickness, 0.1 mm $\pm$0.05 mm.

(4) Dislocation density, $<10^4/cm^2$.

(5) Crystal structure, single-crystal.

(6) Length, 10 cm.

At the end of the first year's effort, 2.5-cm-wide ribbons had been grown, but linear growth rates had been limited to 0.25 cm/min. The ribbons grown at this rate were shown to have low thermal stresses. Solar cells made from the RTR material gave efficiencies 20 to 30% lower than coprocessed single-crystal cells. Various material evaluations were made. Dislocation etch measurements showed variations in defect structure across the surface with some local high defect densities, but also large areas of low defect densities. Spreading resistance measurements showed good uniformity and evidence that surface doping of undoped (high-resistivity) precursor ribbons was sufficient to result in homogeneously doped ribbons after growth. Surface photovoltage measurements indicated relatively short diffusion lengths.

A new RTR apparatus (RTR #2) was designed and constructed with increased capabilities and improvements over the first apparatus, and having the capability to grow silicon ribbon continuously. Addition of a high-temperature post-heater to the old RTR apparatus (RTR #1) allowed a very linear temperature distribution from 1260 to 800 °C over a 3.6-cm length. Operation with the post-heater allowed growth of ribbons at velocities of

about 7.5 cm/min. Growth of 0.1-mm-thick, 1.25-cm-wide polycrystalline ribbons at 5 cm/min with negligible residual stresses became routine.

Modifications to RTR #1 were made to increase laser power to 1.2 kW from 375 W. As a consequence, ribbon could be grown at 10 cm/min for 2-cm-wide ribbon stock. Accompanying this increase in growth velocity, however, was a new phenomenon of dendritic growth. Non-dendritic growth was achieved at velocities up to 7.5 cm/min. This limit subsequently was raised to between 8 and 9 cm/min by using inert gas jet cooling to steepen the post-heater temperature gradient.

RTR growth was achieved from a doped polysilicon ribbon feedstock obtained from a chemical vapor deposition (CVD) process. Diffusion length measurements of the resulting ribbon indicated equivalent performance to material regrown from single-crystal feedstock.

Using RTR #1 with the higher laser power, considerable increases were made in area growth rate. An area growth of 55 cm^2/min was achieved for a single ribbon by growing a 7.3-cm-wide ribbon at 7.6 cm/min. The feedstock was 7.6-cm-wide polycrystalline ribbon produced by CVD on a molybdenum substrate, and removed by thermal-expansion shear separation during cooling. Very uniform CVD layers of polysilicon could be grown on molybdenum substrates that were 1 mm thick, 15 cm wide, and 60 cm long. A series of polycrystalline ribbons measuring 5 x 61 cm were grown and successfully separated from molybdenum substrates.

Ultimately, one run attained a throughput of 77 cm^2/min for single-ribbon growth. A 90-cm^2/min throughput also was demonstrated by simultaneously growing two RTR ribbons, each about 5 cm wide at a pull speed of 8.9 cm/min.

Multiple ribbon growth was demonstrated by simultaneous growth of four ribbons. In this scheme, area growth rate is limited by furnace zone width. A furnace was designed and fabricated that would allow 15-cm-wide growth (e.g., two 7.5-cm-wide or three 5-cm-wide ribbons) that would attain an area growth rate of 100 cm^2/min. The contract for this work ended, however, before this furnace could be tested.

A technique was demonstrated that allows use of short (60-cm-long) substrates for material-efficient RTR growth, thereby eliminating the need for near-continuous sheets of polysilicon feedstock. The technique is based on rigid-edge growth wherein a thin unmelted strip about 1 mm wide on each side of the ribbon provides support to the ribbon, eliminating the need to hold the ribbon at the ends and thereby allowing all of the ribbon (except for the two narrow strips) to be recrystallized. In this approach, CVD ribbons having a limited length (1 m) would be grown, automatically loaded into a cassette, recrystallized, and reloaded into a cassette.

Early in the program, RTR material yielded solar cells of low performance (efficiencies averaged 7.7% against a goal of 12%). A degradation in open-circuit voltage (V_{OC}) of 50 mV was found to occur during the metallization step. By using a low-temperature metallization step, this V_{OC} degradation could be reduced to 10 to 15 mV.

Subsequently, some problems were encountered with contamination of RTR materials during growth. The presence of contaminants was indicated by a sharp drop in diffusion length as measured by surface photovoltage, and solar cell performances were in the 6% range. The elimination of several possible contaminating mechanisms resulted in increased diffusion lengths for RTR ribbon grown from CVD feedstock. By etching about 25 μm from the polyribbon surface that had been in contact with the molybdenum substrate, the molybdenum impurity level was reduced to below the detection limit of neutron activation analysis. A simple gettering sequence also was developed that used PH_3 and increased the diffusion length. The first solar cells made from gettered, pre-etched CVD feedstock were evaluated. The average efficiency for one lot of these cells was 9.1% AM1. The best cell had an efficiency of 11.3% AM1, with V_{OC} = 0.533 V, J_{SC} = 29.4 mA/cm^2, and a fill factor of 72%. A solar cell fabricated later on RTR material grown from CVD feedstock gave an efficiency of 11.8% AM1.

An initial economic analysis of the RTR process was conducted, based on using a polycrystalline feedstock produced either by a conventional CVD process or by a plasma deposition process. That analysis indicated that silicon ribbon produced by the RTR process in a 500-MW/year facility could be sold either at \$0.25/W_p using CVD polysilicon feedstock, or \$0.18/W_p using silicon ribbon feedstock formed by plasma deposition from silane.

Key Accomplishments. The key accomplishments of the RTR program are:

(1) Demonstrated feasibility of RTR process.

(2) Demonstrated throughput as high as 77 cm^2/min for single ribbon, and as high as 90 cm^2/min for multiple ribbon growth (two ribbons).

(3) Demonstrated solar cell efficiencies as high as 11.8% AM1.

(4) Demonstrated multiple ribbon growth by growth of four ribbons simultaneously.

(5) Economic analysis indicated that RTR silicon ribbon could be sold at \$0.25/W_p using CVD polysilicon feedstock or at \$0.18/W_p using silicon ribbon feedstock produced by plasma deposition from silane.

Present Status. Support of RTR process development by the FSA Project ended in July 1979, but the effort has continued under private support.

5. Low-Angle Silicon Sheet: Energy Materials Corp.

The LASS growth process consists of controlled freezing of a thin layer on the surface of the melt and pulling of the solidified material more or less parallel to the surface to some point of detachment of the solid from the melt (Figure 41). Early analyses by Energy Materials Corp. (EMC) had indicated that very high area rates of ribbon growth should be attainable by this process. The development effort supported by the FSA Project verified this. Key features of the process, accounting for the high pull speeds that can be achieved, are:

(1) The direction of ribbon pull is nearly perpendicular to the direction of crystal growth.

(2) The heat of fusion is lost by radiation from the upper surface of the solid ribbon to an environment above the ribbon that can be made cold.

(3) The solid-liquid interface area from which this heat is radiated is large.

(4) The thickness of the ribbon through which the heat of fusion must be conducted to be radiated is small (because of the wedge-shaped cross section along the growth front).

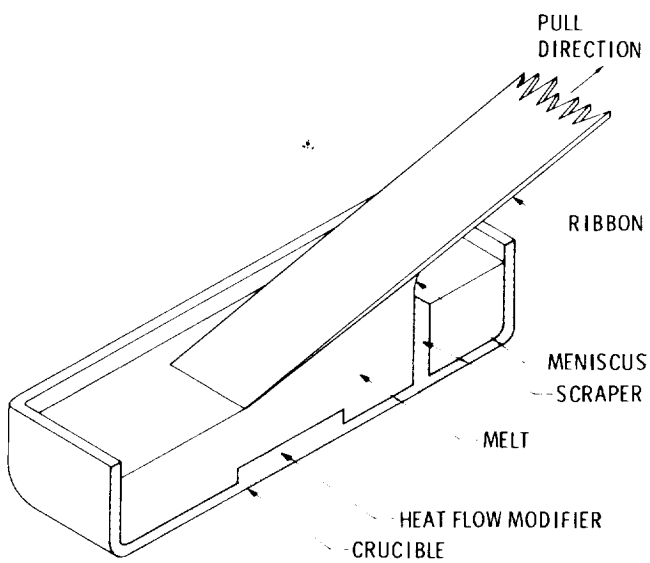

Figure 41. Schematic Diagram of Low-Angle Silicon Sheet Growth Process (Energy Materials Corp.)

Development of the LASS process at EMC for the JPL/DOE program was carried out in two phases. The first phase (Reference 57), from May 1979 to January 1981, had the objective of demonstrating the feasibility of the process. EMC's approach was to employ a shallow melt, thereby inhibiting the formation of substantial convective flows that would destabilize growth. Thermal gradients controlling the growth rate were established in the melt by thermal impedances within the growth region. The meniscus was detached from the bottom surface of the ribbon by a "scraper," that provided a lip that could be maintained at a temperature above the silicon melting point. After preliminary growth experiments were conducted, a gas cooling block, or "cold shoe," was designed and built to provide additional heat transfer from the seed and ribbon interface. The cold shoe produced a stream of helium directed essentially perpendicular onto the surface of the seed crystal. It was recognized that maintenance of constant melt level was important to the LASS process, but implementation of this feature was beyond the resources of the effort.

Experiments were conducted initially without the cold shoe. Various difficulties were encountered, including inability to control the direction of growth from the seed. Incorporation of the cold shoe led to successful ribbon growth. This demonstration of process feasibility accomplished the objective of the effort. Ribbon lengths up to 74 cm were grown with widths varying from 5 to 25 mm. Pull speeds ranged from 5 to 68 cm/min, and thicknesses varied from 0.6 to 2.5 mm, with typical values of about 1 mm. At the end of the effort, the primary problems were stated to be melt-level control and growth initiation. The top and bottom surfaces of a LASS ribbon are shown in Figure 42.

A second phase of the LASS program was supported by DOE outside the FSA Project (1981 to March 1984). FSA resumed participation in 1984 with an objective to overcome the barriers to the low-angle growth of high-quality material at high growth velocities. Parameters governing the growth of high-quality material at high growth rates were to be identified and optimized. The technical effort ended in June 1985.

During this last period of effort, a positive-pressure, clean-room facility was constructed for the growth experiments. A new furnace designed for high-quality ribbon growth and provided with a heater at the solid-liquid interface also was built. Although many problems were encountered in implementing the heater, a successful configuration evolved. In a growth run that produced about 30 m of ribbon, EMC pulled more than 5 m of material that had a full width of dendrites aligned with the growth direction. X-ray analysis at JPL indicated these dendrites are <111> single crystals. EMC believes that the aligned dendrite material should produce better solar cells than polycrystalline LASS ribbon. However, the use of any regular dendritic structure precludes very thin sheet and, thereby, limits silicon use because the dendrites must be thick enough to interconnect side to side.

Minority carrier diffusion lengths (L_D) were measured on LASS material at different depths. The results indicated that L_D decreases in value from the top surface to the bottom of the ribbon. The cause of this undesirable gradient was investigated, but was not determined. Diffusion length measurements on ribbon grown from semiconductor-grade silicon gave values as high as 40 μm.

Although solar cells were not made from LASS material as part of this program, it has been demon-

strated in other work that solar cells having efficiencies as high as about 13% AM1 can be made using LASS ribbon with unaligned dendritic structure.

Redesign of the cold shoe allowed the use of a video camera to observe the growth interface in real time. This capability is considered by EMC to be critical to understanding the solidification process and, as noted under Key Accomplishments, was employed to obtain information on the condition required for growing the aligned dendrite structure.

Key Accomplishments. The key accomplishments of the EMC low-angle sheet program are:

(1) Achieved highest throughputs of any of the FSA ribbon processes. Maximum throughput of 450 cm^2/min achieved. Demonstrated maximum width of 15 cm and maximum pull speed of 85 cm/min (but not simultaneously), and significantly reduced ribbon thickness from a range of 0.89 to 1.14 mm to a range of 0.64 to 0.76 mm.

(2) Developed the LASS process to the point where significant length of material consisting of aligned dendrites across the full width was produced. Determined through use of real-time video recordings that the aligned dendritic structure occurs when the shape of the solid/liquid interface is linear.

(3) Economic analysis indicated sheet add-on cost of \$6.90/m^2 (1980 dollars). For 0.4-mm sheet and silicon cost of \$10/kg, total sheet cost can be \$18.70/m^2.

(4) Solar cell efficiencies as high as 12.9% AM1 were demonstrated by another program for solar cells made of LASS material.

Present Status. Development of the LASS process under support of the FSA Project ended in June 1985.

Technical Needs to Complete. Probably the major technical need is to determine whether the material produced by the LASS process can be used to make high-performance solar cells. The material needs to be better characterized and investigations made of its solar cell performance. It should be determined whether or not the aligned dendrite structure produces better solar cells than polycrystalline LASS material. If the aligned dendrite structure is the preferred configuration, the process has to be better controlled so that this material can be produced consistently.

C. SUMMARY

Five different ribbon technologies were investigated as part of the FSA program. Two of these, the EFG and dendritic web processes, received the most support and were taken to mature levels of development. The EFG process has been commercialized by

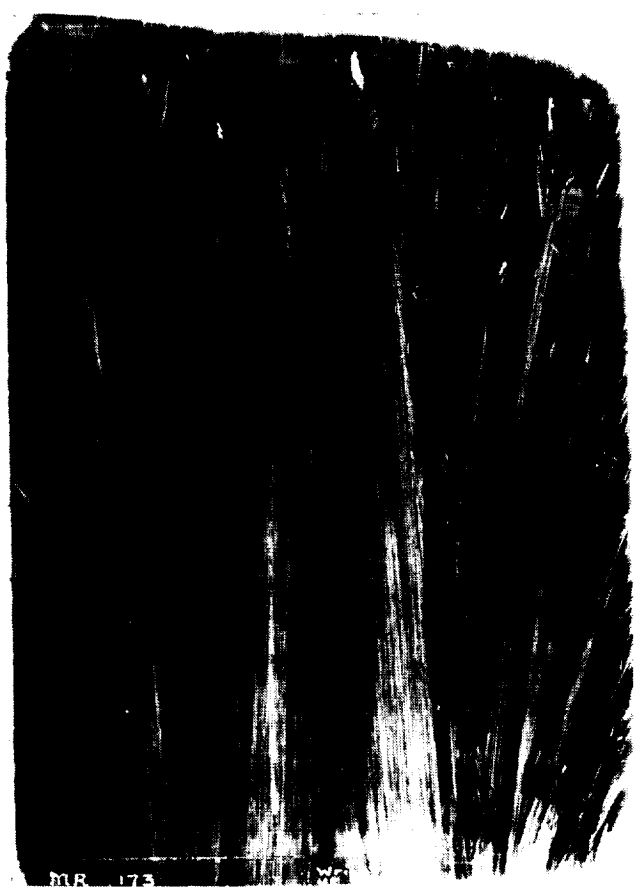

Figure 42. Low-Angle Silicon Sheet Ribbon Surfaces

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MSEC, and Westinghouse is in process of commercializing the dendritic web process. Higher rates of area growth are required of both processes to meet the DOE cost goals, but the growth rates of both are presently limited because of the development of stress at high growth speed. In the case of the dendritic web process, the quality of material produced is the highest of the ribbon processes that were investigated.

Other ribbon process development efforts supported by the FSA Project were taken to different levels of maturity, but were ultimately dropped so that the increasingly limited resources available to FSA could be concentrated on the Westinghouse program. In 1981, the FSA Project was redirected by DOE from a path that demonstrated the technology to research involving understanding of ribbon growth problems. At that time, the original goals for the EFG process and the dendritic web process had not been met. After the redirection, the MSEC program on the EFG ribbon process focused mainly on the generic problems of understanding and controlling stress/strain and on investigating the role of carbon and oxygen in the growth environment as affecting the performance of all ribbon materials.

The DOE redirection also resulted in a slowdown in the Westinghouse program on dendritic-web ribbon. In 1984, however, a 3-year program with multiple sponsorship, including the FSA Project, was undertaken with the goal to develop the technology for utility applications. This program was scheduled to be completed at the end of calendar year 1986 (DOE funding ended in September 1986). Although many accomplishments have been made in the course of this program, ribbon area growth rates have not been increased from the levels achieved by the end of 1982.

Major accomplishments achieved by the ribbon growth program include the following:

(1) Two of the five ribbon technologies supported by the FSA Project (MSEC EFG process and Westinghouse dendritic-web process) were selected as offering the most promise and were carried to mature states of development.

(2) MSEC demonstrated the practicality of the EFG process, showing sufficient performance to warrant major industrial support. The process has been commercialized.

(3) Westinghouse Electric Corp. demonstrated the practicality of the dendritic web process. Westinghouse is committing major funding and is engaged in efforts to commercialize the process. Dendritic-web ribbon has been shown to be of high quality suitable for making high-efficiency solar cells (as high as 16.9% AM1 efficiency as measured by Westinghouse).

(4) In conducting a research program on the dendritic web growth process, JPL found that thermal instabilities and imbalances that lead to termination of ribbon growth result from both variability with time of radiating surfaces and the susceptor and thermal shields.

(5) Motorola/Solavolt demonstrated the feasibility of the RTR process with its high throughput. Efficiencies of solar cells made from the material were as high as 11.8% AM1. R&D has continued under Solavolt sponsorship.

(6) In its development of the LASS process, the EMC achieved the highest throughputs of any of the ribbon processes, a maximum of 450 cm^2/min. In another program, it was demonstrated that solar cells made from LASS material can give efficiencies as high as about 13% AM1.

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SECTION V

Other Sheet Growth Processes

A. INTRODUCTION

At the inception of the Project, the Large-Area Silicon Sheet Task elected to support the technology development of all existing or proposed sheet growth processes that might have the potential to achieve the cost and performance goals of the Task. In addition to the ingot growth and continuous, direct sheet growth methods, other sheet growth processes supported by the Task included:

(1) A method to grow unsupported sheet segments directly from the melt using vacuum casting (ARCO Solar, Inc. and SRI International).

(2) The growth of supported sheet directly from the melt on ceramic substrates (Honeywell).

(3) The growth of supported thin-film sheet on non-silicon substrates from solution (Astrosystems).

(4) The growth of sheet by chemical vapor deposition (GE, Rockwell, and RCA).

(5) The fabrication of sheet by deformation processing (University of Pennsylvania).

All were high-risk techniques with no prior demonstration of feasibility. The initial contract goals in each case were to test feasibility with the promise of continued funding in the case of successful demonstrations. The contracted efforts were supported at different times during the 11 years of the program. The efforts met with varied success.

B. IMPLEMENTATION

1. Silicon-on-Ceramic Process: Honeywell Corporate Research Center

The silicon-on-ceramic (SOC) process was proposed by the Honeywell Corporate Research Center as one of the responses to the initial RFPs in 1975.

A program was carried out to assess the technical feasibility of the process (Reference 58). Fundamentally, the process consists of placing a piece of appropriate ceramic in contact with molten silicon and subsequently withdrawing the ceramic at a controlled rate to yield a coating of the desired thickness. An aluminosilicate mullite ($2\ SiO_2 \cdot 3\ Al_2O_3$) was selected as the ceramic, although other materials were evaluated. Because of marginal wetting of this mullite by silicon (contact angle 90 deg), a film of carbon on the ceramic was required to enhance the wetting. Initial cost projections were developed based on proposed technical performance goals. Initially, a velocity of 1 cm/s was proposed for the withdrawal rate of the ceramic from the molten silicon.

The specific technique chosen for initial development consisted of immersing an approximately 5 x 7-cm rectangular piece of ceramic into a crucible of molten silicon, allowing achievement of thermal equilibrium, and slowly withdrawing the ceramic piece (Figure 43). This experimental scale system was used to:

(1) Establish basic operating conditions.

(2) Evaluate several alternative ceramic materials.

(3) Evaluate a variety of carbon-coating techniques.

(4) Establish preliminary pull speed and film thickness parameters.

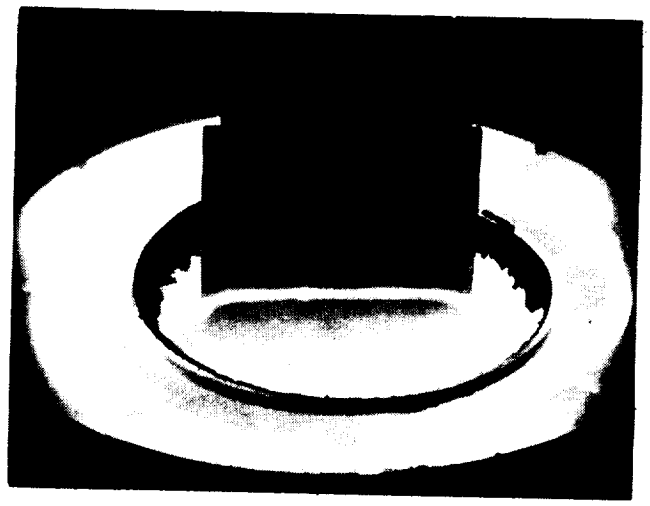

Figure 43. Dip Coating of Silicon-on-Ceramic Process (Honeywell)

Subsequently, using the same basic dipping principle, a second system was developed in which much greater attention was paid to the cleanliness of the operating conditions to improve the purity of the silicon coatings.

A variety of ceramics were evaluated to test requirements. These included: mullite, silicon oxide, aluminum oxide, zirconia, calcium aluminate, and cordierite.

Primary considerations were: high-temperature stability, thermal expansion match to silicon, and wettability. In most cases, the wetting problem was circumvented by means of carbon coatings.

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These investigations led to the conclusion that only mullite held potential as a substrate material because of reasonable match of its thermal expansion to that of silicon. In later stages of the program, however, it was found that, even with the minimal difference in expansions between mullite and silicon, spalling of the silicon coating occurred. For this reason, a program was instituted with Coors Porcelain to try to modify the thermal expansion of the mullite substrate by means of compositional adjustments. This program (described in Section VI.B.1.c.) was completely successful. A mullite composition was developed that precisely matched the thermal expansion of silicon and it was used extensively throughout this program.

Using the early immersion process, various processes of carbon coating the ceramic also were evaluated. These included mechanical scrubbing of the surface with carbon and the use of paints, suspensions, and impervious vitreous carbon films. The mechanically scrubbed surfaces and the vitreous carbon films produced by Tylan Industries were the most successful (see Section VI.B.1.d.). The vitreous carbon films also offered an advantage in lowering the sheet resistance of devices.

The initial studies of withdrawal of the ceramic from immersion in a crucible indicated that the process obeyed a functional relationship in which the silicon thickness varied inversely as the square of the removal velocity. It also was determined that to obtain reasonable film thicknesses (50 to 150 μm), pull speeds of less than 0.1 cm/s were required. Because this speed was too low to amortize equipment and labor, consideration was given to more rapid heat removal. Extensive thermal analyses were conducted based on accelerated heat removal by means of cold shoes and gas flows, as well as the potential for asymmetric growth. These analyses led to improved thicknesses, and useful layers ultimately could be obtained at velocities of the order of 0.25 cm/s. This level was adopted as an intermediate goal based on other revisions of the operating conditions.

Electrical and structural evaluation of the material produced led to several other important findings. The structure of the silicon films was the equilibrium defect structure identical to that described in Section IV.B.1.a. Regions in which the twin density was high and well ordered generally showed better diffusion lengths. It also was determined that the silicon in the crucible, when in contact with mullite, showed a reduction in bulk resistivity from about 50 Ω-cm to less than 1 Ω-cm in an hour. This was traced to the small but finite solubility of the mullite in the silicon, resulting in contamination of the melt by aluminum.

Early solar cell performance for photodiodes fabricated from this material was less than 5% for small photodiodes without antireflective (AR) coating. Because of the insulating nature of the ceramic substrate, however, larger area cells could not be produced initially because of the high sheet resistance of the base.

As a result of the problems stated here with the use of immersion coating, an alternative technique called Silicon Coating by Inverted Meniscus (SCIM) was proposed and developed in 1978. In this process, a long (1 m) sheet of mullite was passed above, but in contact with, a trough of molten silicon. Surface tension caused the silicon to be pulled along the substrate, depositing a film of silicon as the ceramic passed by. The SCIM approach is shown in Figure 44. Two operating systems were developed. In the first, the path of the mullite substrate was horizontal. In the second system, the mullite substrate could be tilted at some angle to obtain better control of the behavior of the meniscus. This offered the technical advantages of:

(1) Reduced time of contact of the melt with the substrate.

(2) Elimination of the need for thermal equilibrium.

(3) Greater control of the velocity-thickness relationship.

(4) Closer approximation to a continuous production process.

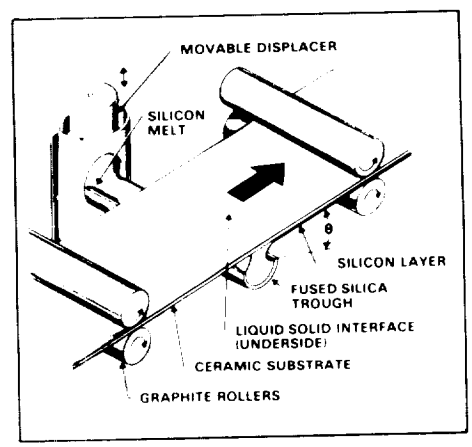

Figure 44. Schematic Diagram of Silicon Coating by Inverted Meniscus Process (Honeywell)

These two techniques were developed extensively, and the final system (Figure 45) was operated using two substrates, each 12.5 x 100 cm, moving through the coater at speeds ranging up to 0.1 cm/min. Again, it was found that the films produced obeyed a velocity squared-versus-thickness relationship and that application of only radiative cooling for the crystallization of silicon limits the growth velocities for practical thicknesses to <0.2 cm/min.

As the coating process began to show technical feasibility, a means was required to achieve contact to the back of the base material in the devices produced by this process. This was to reduce base series resistance. The approach ultimately selected used perforated ceramic having slots or holes to allow contact to the back of the base material. This approach was successful, and series resistance within the cells was

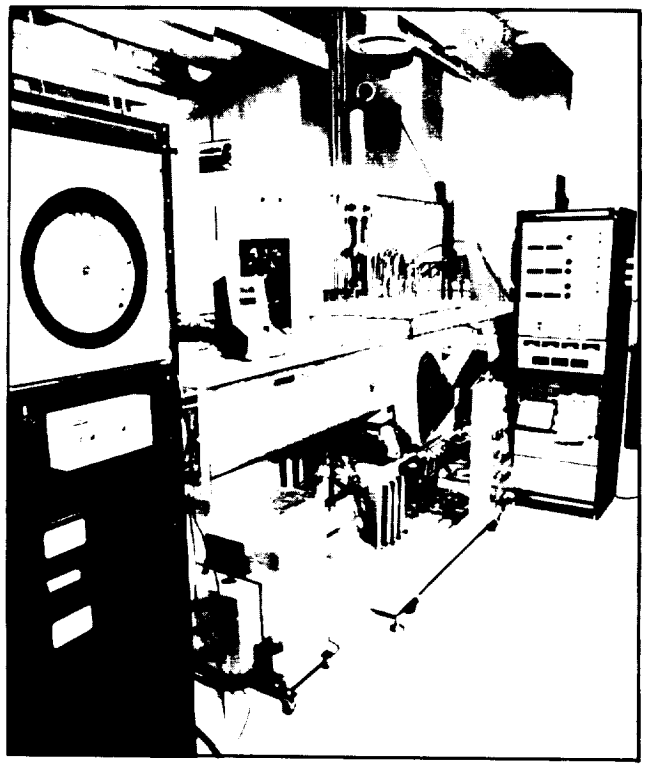

Figure 45. Honeywell Silicon Coating by Inverted Meniscus Coater for Silicon-on-Ceramic Process

reduced to acceptable limits. Solar cell efficiencies greater than 10% ultimately were achieved using this approach. The perforations within the ceramic substrate reduced its strength somewhat, but appropriate thermal gradients in the SCIM coaters, using entrance and exit furnaces, were able to control this problem.

An alternative scheme, considered for the base contact, used a striped configuration in which alternative base and emitter contacts were made. Molded, striped concentrators were to be used to eliminate the front surface area not irradiated. Analysis of this approach and limited experimentation indicated that stripe widths of the order of <2 mm would be required to reduce base series resistance, and that these widths would likely be impractical for the process envisioned.

Because of budgetary constraints, the SCIM process development was discontinued by the FSA Project in late 1980. Several process problems remained, all of which needed successful development to achieve a cost-effective process. The technical limitations that seemed most critical were:

(1) Appropriately high crystallization velocities (>0.5 cm/s) did not seem achievable.

(2) Solar-cell efficiencies continued to remain below that of competing technologies, and further improvements in efficiencies were needed.

(3) Production cost of the mullite substrates in large-scale operations remained in question.

2. Chemical Vapor Deposition

a. *General Electric Company: Floating Substrate Process.* The objective of this effort, which began in January 1976 and was supported by FSA (Reference 59), was to demonstrate the feasibility of the floating-substrate sheet-growth process for silicon. In this process, a thin, single-crystal sheet of silicon is to be grown by CVD on a pool of molten tin saturated with silicon. Most of the growth was to take place near the hot end of the tin pool. The silicon, arriving at the surface of the molten tin, was to dissolve in the liquid metal until the latter became saturated and then was to crystallize on the surface. Under steady-state conditions, the silicon sheet was to be drawn toward the cooler end of the furnace and then lifted off the supporting liquid after the silicon temperature had dropped below the range of plastic deformation. A schematic diagram of the process is shown in Figure 46.

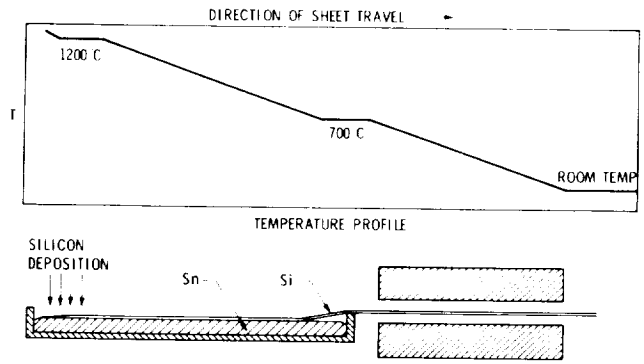

Figure 46. Floating Silicon Substrate Sheet Growth Process (General Electric Co.)

The following investigations were carried out to study the following processes involved in growing silicon sheet by this method: supercooling, crystal growth from supercooled tin-silicon alloy, silicon uptake into tin from silanes, and surface growth.

Results of the supercooling experiments were quite encouraging, indicating that reasonable sheet growth rates could be achieved in the temperature range from about 1100°C, even with melts whose surfaces were not completely clean (scums tended to form). Clean melt surfaces were expected to give increased growth rates through greater supercooling.

It was determined that silicon can be incorporated into a tin melt by direct interaction of the melt with a flowing silane gas stream. More than 30% of the silane was converted to silicon in a single pass. It was found that silicon is incorporated into liquid tin at the same rate that it is deposited upon silicon substrates and that this rate of incorporation was independent of the degree of melt saturation.

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The growth of crystals nucleated spontaneously at the tin-silicon alloy melt surface was characterized. The crystal growth was consistent with dendritic and web ribbon growth from (111) singly twinned, triangular nuclei. Examples of planar surface growth of small (<0.1 mm), thin crystals from these twinned surface seeds were observed, demonstrating, in principle, the feasibility of the process. Surface growth at velocities as high as 5 mm/min was obtained. This growth generally took the form of interlocking crystals and was thin enough to follow the liquid surface.

Small, single-crystal regions often appeared along the surface of the tin-silicon melt, but did not propagate. They persisted for only a few millimeters and then reverted to branched dendritic growth. The reasons for the polycrystalline growth are not clear. The contractor suggested that the most probable cause was poisoning of the growth interface by impurities, either in solution or at the melt surface.

b. *Rockwell International.* This program was instituted in response to the initial sheet growth RFP. The study (Reference 60), was directed at the evaluation of the CVD of silane (SiH_4) on low-cost substrates as a potential means of producing low-cost silicon sheet. Silane was chosen because of its relatively low decomposition temperature and availability in pure form. The program included selection and development of suitable substrates, preparation and evaluation of silicon films, and preparation and evaluation of solar cell structures. Although deposition was conducted in research-scale reactors, deposition rates and conditions were maintained to be consistent generally with cost-effective sheet production.

An extensive portion of the evaluation involved selection and development of low-cost substrates for the process. A wide variety of glasses were evaluated, including special and proprietary compositions as well as polycrystalline ceramics, such as Al_2O_3 and mullites. Emphasis was placed on a reasonable thermal expansion match between the substrate and silicon as well as careful evaluation of the details of the substrates. Specifically, ceramics of the same nominal composition were evaluated relative to their grain size, surface preparation, and other physical characteristics. Substrates of single-crystal sapphire and single-crystal silicon were used as controls in evaluation of deposition conditions. Extensive studies were conducted of the effect of diluent gases (hydrogen and helium), flow rates, temperatures, and pre-deposition thermal treatments.

Substrate surfaces and deposited layers were evaluated by a variety of techniques including SEM, x-ray diffraction, and conventional metallography. Electrical characteristics, including resistivity and diffusion length, were measured on the deposited films. In selected cases, small photodiodes and solar cells were produced by Optical Coating Laboratories, Inc. (now ASEC).

After consideration and evaluation of hundreds of substrates under a variety of deposition conditions, several meaningful conclusions were derived. Deposition compatibility for several special glasses was obtained, but the grain size of film so deposited was too small for adequate solar cell performance. High-purity alumina ceramics, especially those with large grains and carefully prepared surfaces, produced local epitaxy of large-grain silicon (>300 μm). Device performance was still unsatisfactory for PV power applications. Lower-purity alumina, because of multiphase structure, resulted in non-homogeneous silicon film growth.

c. *RCA Laboratories: Epitaxial Silicon Growth for Solar Cells.* The purpose of this program with RCA Laboratories was to evaluate the potential for the use of epitaxial silicon growth on low-cost silicon substrates to achieve higher conversion efficiency devices (Reference 61). A high-capacity rotary-disk reactor, developed by RCA for a separate program, was used as the basis for scaled-up cost projections. Most of the research was conducted in conventional epi-deposition reactors.

Several specific low-cost substrate products used in this program are described in Table 8. Cells were produced by epitaxial deposition or diffusion into these substrates, and results were compared to single-crystal control cells produced by either diffusion or epi-deposition. Selected results are shown in Table 9. In all cases, cells produced by epi-deposition of the emitter layer were inferior to those with a diffused junction. The n-type epi junction layers, however, were about 1 μm thick and certainly not optimum. No effort was made to optimize this aspect of the study.

Although variations from sample to sample among the low-cost substrates were significant, general trends were apparent. Multigrained substrates performed the poorest when epi-based layers were used. Conversely, the low-cost single-crystal substrates (titanium-doped Cz and upgraded metallurgical-grade silicons) came closest to reproducing the performance of the controls. Thus, the epitaxial growth process demonstrated the ability to enhance the performance of chemically contaminated material more readily than structurally defective material.

Cost analyses of the epi process were conducted to evaluate the potential value of the process. Analyses were conducted using the advanced rotary design reactor that had been demonstrated to perform well. An added value was obtained of \$0.46/W_p at a projected 12.5% cell performance level. Although such costs might find a role in intermediate module prices of several dollars per watt, they are inconsistent with ultimate module cost goals of \$0.50/W_p (1975 dollars). A conceptual design for an advanced reactor was developed and add-on costs for the process in this reactor were projected to be less than \$0.10/W_p (1975 dollars).

Table 8. Characteristics of Low-Cost Silicon Substrates

Substrate/Vendor	Type	Resistivity, Ω-cm	Level, ppm	Impurity	Crystallinity	Grain Size, mm
SILSO/Wacker[a]	p	4-8	1-5	C	Polycrystalline	1-10
RMS/Union Carbide[b]	p	~0.06	100-200	C,B,P,Fe	Polycrystalline	3-10
UMG/Dow Corning[c]	p	~0.02	10-100	Al,B,P	Single crystal	No grains
Cz-Ti/Dow Corning	p	0.3	2×10^{14}	Ti	Single crystal	No grains
Cast Silicon/Crystal Systems[d]	p	~1			Polycrystalline	

[a]Wacker Chemical Corp., Richardson, Texas; SILSO is a brand name.

[b]Union Carbide Research Laboratory, Tarrytown, New York; RMS is "refined metallurgical grade."

[c]Dow Corning Corp., Hemlock, Michigan; UMG is "upgraded metallurgical grade."

[d]Crystal Systems, Inc., Salem, Massachusetts.

Table 9. AM1 Characteristics of Solar Cells with Epitaxial Base Layer

Base Thickness Substrate	Jct, μm	Formation	Js, mA/cm^2	V_{OC}, V	Fill Factor	η, %
Control	10	Diff	27.0	572	0.782	123.0
Control	10	EPI	23.5	573	0.723	10.0
Wacker	10	Diff	26.9	450	0.531	6.6
Wacker	10	EPI	22.8	540	0.570	7.3
RMS	14	Diff	25.4	535	0.66	9.3
RMS	10	EPI	20.4	526	0.60	7.3
UMG	15	Diff	25.3	602	0.80	12.4
UMG	10	EPI	22.2	577	0.74	9.5
CAST	10	Diff	26.2	571	0.75	11.1
CAST	10	EPI	22.9	535	0.66	8.1
Cz/Ti	10	Diff	24.9	576	0.78	11.5
Cz/Ti	10	EPI	20.2	548	0.70	7.9
Cz/Ti	None	Diff	18.0	545	0.77	7.8

3. Vacuum Die Casting: ARCO Solar, Inc. and SRI International.

This short-term, high-risk effort was started in 1979 to investigate the possibility of die-casting silicon ribbon and fabricating low-cost solar cells from the resulting sheet material. It was one of the "Tsongas" contracts similar to that awarded to Kayex (see Section II.B.1.a.). The goals of this program were twofold:

(1) To develop a low-cost, polycrystalline sheet production technology through scale-up to a commercial level.

(2) To develop processing technology to produce polycrystalline solar cells with high energy-conversion efficiency.

The program was structured in three phases.

Phase 1, involving development of a silicon ribbon vacuum casting process, was to be performed by SRI International. The concept was to lower several ribbon molds simultaneously into molten silicon in a vacuum system and then to fill the molds by applying an over-pressure to the melt. No final report was issued on this effort.

Phase 2 depended on the success of Phase 1. In Phase 2, SRI was to scale up the vacuum casting technique to a low-cost commercial process. Phase 3, to be conducted entirely by ARCO Solar, would develop device processing methods and device designs that would allow the low-cost fabrication of 12% efficient cells on polycrystalline wafers. Phase 3 work was to begin using procured polycrystalline sheet, Wacker Silso for example, and the work then would be applied to the vacuum cast product as it became available.

The vacuum casting experiments of Phase 1 were unsuccessful. One data point, however, was obtained: molten $NaF \cdot .NaSiO_x$ successfully encapsulated silicon and acted as a mold release in carbon molds. Thus, SRI began a program to pressure-cast silicon discs in sodium fluosilicate-coated molds, and this effort yielded several polycrystalline discs. Because analysis indicated that the economic goals of the FSA Project would not be met using the pressure-casting process, the entire program was terminated when the initial funds for Phase 1 were exhausted.

4. Deformation Processing: University of Pennsylvania

This program was instituted to assess the potential of using a metal deformation process such as hot rolling as a means of forming sheet silicon (Reference 62). The program used a forging technique employing right circular cylinders of silicon as a means of assessing feasibility. This forging process is far simpler than hot rolling to implement, and was judged to be suitable for feasibility evaluation.

The experimental program included the construction of a modified hot forging system using a tungsten-rhenium platen to apply pressure both to right circular cylinders of single-crystal silicon of various orientations and also to polycrystalline silicon. Samples were deformed by 5 to 40% at temperatures ranging from 1000 to 1370°C, and then were analyzed by optical and x-ray diffraction techniques for structure and by diffusion length measurements for electrical character.

The feasibility study was successful in that the basic mechanical properties of silicon were determined, and were found to be incompatible with deformation processing as a method of producing useful sheet. The primary limitation derived from the large amount of energy required to allow the deformed silicon grains to recrystallize into a coarse-grained structure-free product. This limitation was restrictive in two ways: it precluded continuous or repetitive deformation in the silicon, and the deformed product contained excessive internal structure to be useful for electronic applications. It did, however, define preliminary deformation processing conditions for applications in which limited deformation and internal structure were acceptable.

5. Liquid-Phase Epitaxy: Astrosystems, Inc.

From February 6, 1984 through July 8, 1984, Astrosystems, Inc. worked to develop and demonstrate a process to deposit thin films of polycrystalline silicon onto foreign substrates (Reference 63). These silicon-substrate combinations were to be fabricated into high-efficiency solar cells. A secondary effort was aimed at development of a solar cell fabrication process for this material. This effort and subsequent work are described in Reference 64.

Specifically, the goal of this work was to grow polycrystalline films of silicon by liquid-phase epitaxy (LPE) from tin solution onto 0.13- and 0.25-mm-thick steel (coated with a proprietary metallurgical barrier) and onto 1-mm-thick quartz glass. The process was intended to produce 20-μm-thick p-type absorber layers with 120-μm diffusion lengths and epitaxial n-type regions. The growth process employed a "slider" boat and operated in the temperature range from 800 to 1000°C at cooling rates of 0.1 to 3.0°C/min. Growth rates of 0.4 to 4.0 μm/min were obtained.

During the course of this work, 32 separate layers were grown on quartz substrates. Of these, about one-third achieved 100% coverage. Initial silicon films on coated steel and molybdenum also were grown. The silicon grains grown on quartz ranged from 15 to 50 μm thick and 30 to 240 μm wide. The aspect ratio ranged between 1.71 and 8.00, and the measured film resistivity (including noncontinuous films) ranged between 0.05 and 186 Ω-cm. The films grown on coated steel were characterized using electron-dispersive analysis of x-rays and revealed only a trace of tin.

R&D continues on the thin-film crystalline silicon solar cell process at Astrosystems, Inc. Device efficiency of 9.7% AM1 (corrected for AR coating) for a 0.1 mm^2 solar cell, was reported by Astrosystems at the 6th European Conference, London.

C. SUMMARY

None of the seven efforts reported here has achieved commercial status. Only the work at Astrosystems is still ongoing, and it continues with internal funding. There were, however, many useful technical observations and achievements that resulted from the work of the various contracts.

A key conclusion common to all the contracts is that silicon compatibility with foreign substrates or container materials is a critical problem unlikely to yield to an easy or inexpensive solution. This was as true of the vacuum casting and supported-film work as it was of the epitaxial growth work. Each of the programs reported some highlights:

(1) Development of a custom-formulated mullite ceramic material with a thermal expansion closely matched to that of silicon (Honeywell and Coors).

(2) A novel release material that allowed casting of silicon sheet in molds without the usual catastrophic failure of the sheet or the mold as a result of wetting and subsequent stressing because of differential thermal expansion (SRI).

(3) The SOC process demonstrated that a controlled silicon coating can be applied to non-silicon substrates and coatings of relatively brittle materials.

(4) Linear growth rates of ≥ 0.5 cm/min of silicon sheet from the surface of a silicon-saturated tin solution were demonstrated by GE.

(5) Demonstration of growth by CVD of large-grain silicon films on non-silicon and low-grade silicon substrates (Rockwell and RCA).

(6) Definition of conditions for hot-forming single and polycrystalline silicon.

None of the high risk sheet growth processes described in this section achieved the cost, throughput, or performance requirements of the Project. The increased performance requirement perceived in the 1980s (i.e., 15 to 17% module efficiency) was beyond the perceived best potential performance for these materials.

SECTION VI

Supporting Research: Materials

A. INTRODUCTION

Many silicon sheet-growth problems associated with the physical and chemical limitations of materials were identifed early in the FSA Project. For example, corrosion arising from the containment of molten silicon results both in limited life of the containers and contamination of the silicon. Research also had to be done to improve the compatibility of ceramic materials with molten silicon to support the development of the SOC sheet growth process.

This section of the report deals with those research efforts that involved characterization of materials behavior as well as materials development. The research was conducted by 10 different organizations. For the purpose of this report, the various studies have been divided into materials development programs and materials evaluation studies, even though each contains some component of the other.

B. IMPLEMENTATION

1. Refractory Materials Compatibility/Die and Container Materials Studies

a. *University of Missouri-Rolla.* The University of Missouri-Rolla (UMR), initially a subcontractor to Eagle-Picher Industries (EPI), supported the EPI development of refractory dies and containers to be used in the handling of molten silicon. The UMR studies dealt with the effects of a controlled atmosphere on the silicon product in those cases where molten silicon was in contact with refractory materials. UMR, awarded a follow-on study contract in May 1979 (Reference 65), investigated the effects of partial pressures of reactant gases near the equilibrium partial pressure. The study was to look for the formation of reactant gaseous compounds.

Under the EPI subcontract, UMR demonstrated the importance of a partial pressure of very low amounts of oxygen on the refractory/molten silicon interaction. Using a thoria-yttria solid-solution electrolyte oxygen cell, routine measurements were made of the oxygen partial pressure well below the equilibrium partial pressure for the formation of SiO_2 (about 2×10^{-19} atmospheres at 1700 K).

A cell was constructed that could be used in the UMR laboratory for measuring oxygen partial pressures in sessile drop experiments. The cell also could be transported to other contractor facilities, so that oxygen concentrations could be measured in their silicon sheet and ribbon furnaces. Such measurements were carried out in the silicon ribbon furnace at Mobil-Tyco and at the JPL silicon sessile drop furnace.

The atmosphere in the Mobil-Tyco EFG ribbon-pulling furnace consisted of argon gas that flowed into the system at a rate varying from 2 to 10 liters/min. (Typically, commercially available argon contains about 1 to 100 parts per million of oxygen as an impurity. This corresponds to a 10^{-6} to 10^{-4} atmosphere partial pressure at 1 atmosphere total pressure.) The Mobil-Tyco furnace contained large amounts of graphite as crucibles, heaters, dies, and the like, all of which serve to reduce the amount of free oxygen in the system. The oxygen partial pressure of the purge gas after passing through the furnace was $10^{-12.1}$ atmosphere, as measured at 1273 K by the oxygen cell.

The gas used in the JPL sessile drop furnace was helium from standard cylinders. (Typically, cylinder helium has oxygen impurity levels of about 10^{-5} atmosphere at 1 atmosphere total pressure.) Graphite in the furnace reduced the oxygen content of the atmosphere through formation of CO and CO_2. The oxygen partial pressure of the purge gas exiting the furnace was $10^{-13.4}$ atmospheres, as measured at 1273 K by the oxygen cell.

Sessile drop experiments were carried out at UMR on a variety of candidate die and container materials including hot-pressed silicon nitride, CVD-coated silicon nitride, sialon, and CVD-coated silicon carbide on graphite. These experiments consisted of in-situ measurements of the contact angle between the liquid silicon and the substrate (Figures 47 and 48) and subsequent examination of the silicon/substrate interface to determine the degree of interaction. All sessile drop experiments were conducted at 1 atmosphere total pressure and oxygen partial pressures less than 1×10^{-19} atmosphere.

The materials investigated fell into two categories: those upon which silicon sessile drops did or did not form an equilibrium contact angle.

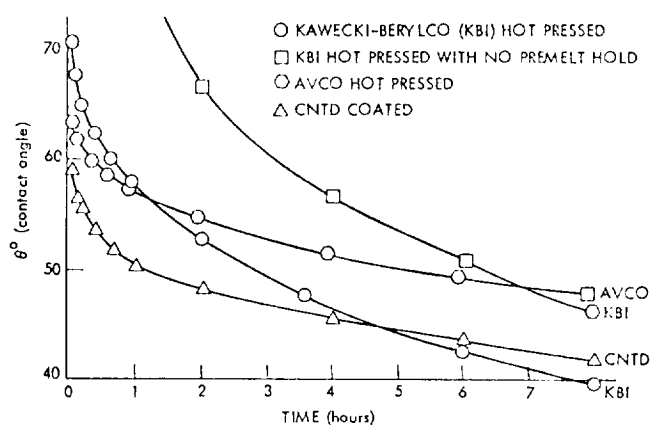

Figure 47. Contact Angle Versus Time for Silicon Sessile Drops on Silicon Nitride

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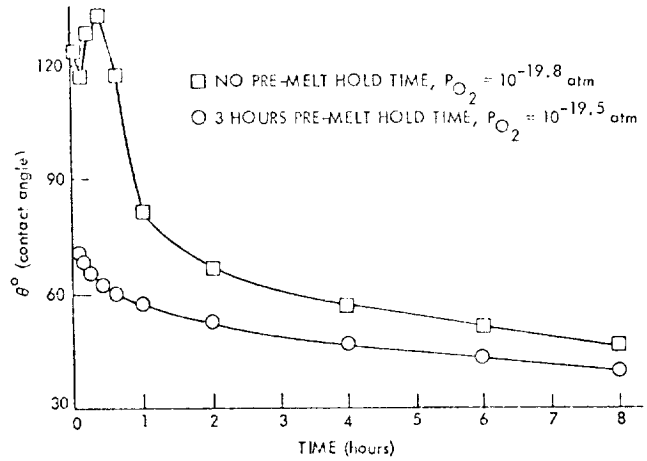


Figure 48. Contact Angle Versus Time for KBI Hot-Pressed Silicon Nitride

In the first category were two materials: (1) two varieties of hot-pressed silicon nitride (from Kawecki-Berylco and from AVCO), and (2) Controlled Nucleation Thermal Deposition (CNTD)[4] silicon nitride coated on hot-pressed silicon nitride. Because the silicon/CNTD silicon nitride contact angle agreed very well with previous measurements made on the same material, it provided a control for reproducibility verification. Although the final contact angle of molten silicon on the AVCO Si_3N_4 (after 8 h) was greater than for the Kawecki-Berylco Si_3N_4, the latter seemed to react more strongly with molten silicon.

Ultracarbon silicon-carbide-coated graphite and Battelle Sialons[5] fell in the category of materials upon which silicon did not form a true sessile drop. Subsequent examination proved that the SiC coating was not a completely integral surface, so molten silicon could seep through the coating to the underlying graphite.

A pseudo-sessile drop formed on the Battelle Sialon because a semi-rigid, skin-like coating with a high concentration of calcium that formed on the liquid silicon drop prevented attainment of equilibrium. The thickness of the coating, and thus its rigidity, depended on the length of time the sample was held just below the silicon melting temperature prior to melt, plus the time the sample was held after melting.

The key accomplishments of the UMR R&D are:

(1) The partial pressure of oxygen in the Mobil-Tyco ribbon furnace was measured, and the results led to further refinement of the system to control the furnace atmosphere.

(2) Atmosphere effects were established for candidate refractory die and container materials.

(3) Test sample/silicon interface areas were characterized for composition, phases, microstructure, and changes therein.

b. *Battelle Columbus Laboratories.* A RFP for investigations of "Die Materials for Silicon Ribbon Growth" was initiated by the Task in November 1976. Battelle Columbus Laboratories was awarded a contract in July 1967 for the development and evaluation of refractory die and container materials (Reference 66).

Considerable effort was expended in studies of solution thermodynamics of the interactions of molten silicon with selected refractory materials. The objective was to gain a more detailed understanding of the reaction processes and to identify possible die and container materials. The interaction of molten silicon with SiC, Si_3N_4, BeO, Al_2O_3, SiO_2, and a mullite composition was studied in a Knudsen cell, using a mass spectrometer to monitor the vapor species (Table 10). Evaluations of impurity levels in silicon after prolonged contact with these materials indicated that SiO_2 is the ceramic material most resistant to molten silicon attack. Other than SiO_2, BeO is by far the most stable metal oxide, and Si_3N_4 is more stable to molten silicon attack than is SiC.

Silicon metal oxynitrides were investigated in an effort to upgrade the mechanical properties of refractories while maintaining a low solubility to limit the contamination of the silicon. Candidate materials chosen for study were β'Sialon, O'Sialon and β'Sibeon. These selections were based on previous solution thermodynamic evaluations and literature studies. β'Sialon is a solid solution of β-Si_3N_4 and $Al_2O_3 \cdot AlN$. O'Sialon is a solid solution of Si_2N_2O and Al_2O_3. Sibeon is a solid solution of β-Si_3N_4 and Be_2SiO_4. Because none of these materials were available commercially, high-purity single-phase materials were produced in the laboratory. This required considerable effort, especially in the preparation of high-purity powders.

Assessment of the three silicon metal oxynitrides as potential die and container materials was performed using sessile drop tests, capillary rise of molten silicon, and Knudsen cell examination of the vapor species above molten silicon in contact with the refractory materials. It was shown that β'Sibeon and β'Sialon are very resistant to molten silicon attack, especially if they are used in an environment of an inert atmosphere.

[4]CNTD: A Chemetal Corp. acronym for their proprietary dense CVD coating.

[5]Of the several Sialons known, β'Sialon is a solid solution of β-Si_3N_4 and $Al_2O_3 \cdot AlN$, and O'Sialon is a solid solution of Si_2N_2O and Al_2O_3.

Table 10. Vapor Pressures of Main Species[a] Detected in the Knudsen Cell at 1430°C[b]

Species	Vapor Pressure (N/m^2) Over					
	SiO_2	BeO	Al_2O_3	SiC	Si_3N_4	Mullite Glass
Si	4.35×10^{-2}	2.02×10^{-2}	3.54×10^{-2}	4.65×10^{-4}	1.21×10^{-3}	8.40×10^{-3}
Si_2	1.41×10^{-4}	2.12×10^{-4}	1.41×10^{-6}	1.31×10^{-4}		
SiO	2.32	1.41	2.73		6.08×10^{-4}	1.52×10^{-1}
Be		1.31×10^{-2}				
Al_2O			7.80×10^{-3}			1.82×10^{-3}
AlO			1.01×10^{-3}			
Al			9.72×10^{-3}			3.24×10^{-4}
Si_2C				3.86×10^{-4}		
Si_2N					1.11×10^{-3}	
N_2					7.09×10^{-2}	

[a]Species confined to those detected above 1.013×10^{-4} N/m^2 (1×10^{-9} atm).
[b]Time at temperature, 3 h.

The following observations were noted with respect to their performance as die and container materials:

(1) *Mechanical Stability.* Sibeon and Sialon are both fabricated at 1750°C and are expected to be stable at temperatures around 1412°C, the melting point of silicon. These materials do not show phase changes below these temperatures.

(2) *Dimensional Stability.* For dies, a dimensional stability to 0.5 mil over a 24-h period is required. The Battelle study did not indicate any significant erosion of material, but enhanced erosion may occur with the use of flowing silicon. Silicon ribbon must be grown using these die materials to determine quantitatively the dimensional stability of the dies.

(3) *Chemical Stability in Molten Silicon.* In sessile drop tests, the beryllium and aluminum contents of 100 to 200 mg silicon samples were lower than found for any other metal cation-containing ceramic. Although these results were very encouraging, evaluation of silicon ribbon formed using these materials would be required before a complete assessment could be made.

(4) *Fabrication of Dies and Containers.* The Sibeon and Sialon materials were developed primarily for die applications. It was demonstrated that dies and containers could be made from these materials, but studies of the sinterability of their powder mixtures would be required (the dies were hot pressed).

(5) *Capillary Rise.* Wetting angles of Sibeon and Sialon are low enough (49 and 37 deg, respectively) to enable a capillary column of silicon 1 to 3 cm wide x 0.01 cm thick to be supported to a minimum height of 2.5 cm.

In summary, specific compositions of solid solutions of high-purity silicon-aluminum-oxynitride (Sialon) and silicon-beryllium-oxynitride (Sibeon) were shown to be promising refractory materials for containing molten solar-grade silicon during silicon ribbon growth.

Well-controlled processing schedules were developed for the fabrication of high-purity Sialon and Sibeon materials. Essentially, the impurity content of the hot-pressed ceramics originated only with the impurities that were present in the original starting powders. A ceramic shaping die successfully was formed by diamond machining of a hot-pressed blank.

Evaluation of the interactions of these ceramic materials in contact with molten silicon indicated that solid solutions based upon β-Si_3N_4 are more stable than those based on Si_2N_2O. Sibeon is more resistant to molten silicon attack than is Sialon. Both materials

preferably should be used in an inert atmosphere rather than under vacuum conditions because removal of oxygen (as SiO) from the silicon melt enhances the dissolution of aluminum and beryllium. The wetting angles of these materials are low enough (37 deg for X = 0.75 β'Sialon and 49 deg for X = 0.35 Sibeon) for these materials to be considered as both die and container materials.

Key Accomplishments. The key accomplishments of the Battelle Columbus Laboratories R&D are:

(1) A new material, silicon beryllium oxynitride, was developed and shows promise as a die material.

(2) Extensive thermodynamic data were generated concerning the interaction of molten silicon with refractory materials. These data give a better insight into the processes occurring between molten silicon and potential die and container materials.

c. *Coors Porcelain Company: Mullite Ceramic Development.* To support the development of the SOC process by the Honeywell Corp., it was found necessary to improve the compatibility of available ceramic materials with silicon. The variety of ceramics initially studied by Honeywell ranged from those that were incompatible to marginally acceptable. The most satisfactory performance of the available ceramic materials was exhibited by mullite ($2SiO_2 \cdot 3Al_2O_3$). This material has a melting point above 1800 °C and a thermal expansion of about 5.1 x 10^{-6}/°C compared to about 4.0 x 10^{-6}/°C for silicon. Thus, its primary properties generally are compatible. In the course of development of the SOC process, however, two substantial difficulties were encountered with conventional commercial mullite:

(1) The thermal expansion match was not adequate when perforated large sheets of mullite were used.

(2) Commercial purity was not adequate.

Consequently, a study was instituted with Coors Porcelain from October 1977 to April 1979 (Reference 67).

The Coors study consisted of the following developmental activities:

(1) Mullite composition variations.

(2) Mullite starting material variations.

(3) Manufacturing process cost analysis.

(4) Perforated sheet.

(5) Contact angle measurement.

(6) Preliminary crucible development.

The first five of the above items of the Coors study were in direct support of the Honeywell effort. The last item was an attempt to evaluate the potential of mullite as a reusable replacement for silica. Progress was made in all developmental areas with degrees of success ranging from good to excellent. The effort was terminated when it was realized that solar cells made from SOC sheet were unlikely to meet efficiency performance requirements. However, in the course of this study, a mullite composition was developed that had a thermal expansion that not only matched that of silicon, but continued to do so even as the thermal expansion of silicon changed with temperature. Perforated substrates were developed that enabled back contacts to be made to devices. At the melting point of silicon, the corrosion rate of mullite was determined to be less than 1 μm/h.

The technology development for compatible mullite compositions was complete and successful with good thermal expansion matches being achieved. Molten silicon was contaminated by the mullite, specifically with respect to aluminum that acted as an acceptor impurity. More information on this contamination problem is available in a description of the SOC process (see Reference 58). Manufacturing methods were developed capable of producing 12 cm x 1 m mullite sheets with about a 50% perforated area. These sheets were successfully coated by molten silicon. Cost projections for this manufactured material were generally consistent with the requirements of the SOC process. Sensitivity of the SOC product to variations in the ceramic substrate price, however, was quite high. The precision with which the ceramic manufacturing process could be projected was not sufficient to ensure the economic viability of the entire sequence.

Evaluation of these materials for use as crucibles led to the conclusion that aluminum contamination would limit their usefulness to situations in which the need for the chemical purity of silicon was less severe, such as for use in infrared optics.

d. *Tylan Corp.* From December 1977 to June 1979, Tylan Corp. was under contract to develop Vitre-Graf coatings on mullite (Reference 68). A technical and economic evaluation was made of this proprietary, glass-like, carbon coating applied to mullite and graphite that would be used either in silicon sheet manufacture or in containerware applications. Preliminary evaluations had indicated that the glassy carbon coating reacted with molten silicon to form a silicon carbide reaction layer that seemed to serve as a diffusion barrier to prevent further silicon reaction.

The technical evaluation consisted of manufacturing test samples of several materials using a variety of processing parameters with a preselected matrix. Tests (primarily of coating appearance, adherence, and silicon reaction behavior) were used to evaluate the coatings. These tests indicated that most graphite and carbonaceous materials used as substrates will produce a visually acceptable coating having excellent adherence over a wide range of processing param-

eters. No set of parameters, however, produced a coating that could withstand the chemical attack of molten silicon and prevent its reaction with a graphite substrate. The primary application of graphite components was for containerware that required long-time exposure to molten silicon. The conclusion of this study suggested that the glassy carbon coating might provide protection for periods of only 30 min or less and, therefore, was not suitable for the intended application.

Tests conducted on the glassy carbon glaze applied to a porous mullite formulation indicated that performance was satisfactory for manufacturing of SOC-based solar arrays. When this material was tested on Type K mullite, developed specifically for solar arrays, it was found that coating performance was generally insensitive to coating processing parameters, and the selected parameters could be cost-optimized. However, the SOC option did not meet cost or performance objectives and was not pursued.

e. *RCA Laboratories.* The original contract with RCA was for development of the Stepanov or the Inverted Ribbon Growth Process. It soon became apparent, however, that the die materials used in this process were a limiting component. Subsequently, RCA's work evolved into the development and evaluation of die materials for use in the growth of silicon ribbons by the inverted ribbon growth process. Work was conducted from 1977 to 1980 (Reference 69).

Efforts were primarily directed toward CVD Si_3N_4 and silicon oxynitride coatings. Si_3N_4 layers were deposited on various substrates by reaction between silane (SiH_4) and ammonia (NH_3). The carrier gas was either hydrogen or nitrogen and the deposition temperature was 1000 °C. Silicon oxynitride coatings were prepared in a similar manner except that nitrous oxide (N_2O) was introduced as the oxygen-containing reagent. Coatings were evaluated by both sessile drop and ribbon growth experiments. In addition, silicon ribbon was grown using a CVD Si_3N_4-coated die.

The thermal stability of CVD Si_xN_y layers in contact with molten silicon were studied by x-ray analysis. The results indicated that these layers were converted to the alpha and beta phases of Si_3N_4 with the beta phase predominating. The beta-phase content increases with time, as also was observed in tests on CVD Si_3N_4 layers. In the latter case, however, the alpha phase was the dominant phase. RCA results indicated that the beta phase is the more stable form in contact with molten silicon. This explains why CVD oxynitride layers seemed to be more stable in contact with molten silicon than are CVD Si_3N_4 layers. The oxygen present in the oxynitride layers apparently is removed during contact with the silicon melt with simultaneous conversion of oxynitride to Si_3N_4, principally the beta form.

f. *Eagle-Picher Industries, Inc.* In August 1977, EPI was awarded a contract to conduct a study to develop methods to process and fabricate selected refractory materials into forms resistant to the corrosive action of molten silicon (Reference 70). The materials also were to be amenable to the production of ribbon-forming dies and containers for molten silicon.

EPI assembled a team that served as the prime contractor with overall management and primary fabrication responsibilities. The Chemetal Corp. served as a subcontractor to apply selected coatings on substrates prepared by EPI. It would use a process-variant of CVD that Chemetal designated "Controlled Nucleation Thermal Deposition" (CNTD). The CNTD coatings have fine grains and were expected to be more dense and resistant to chemical attack than ordinary CVD coatings. UMR investigators explored the previously incomplete area of atmosphere control and characterization. They were to determine the effect of atmosphere control on reactions and interactions at the molten silicon/substrate interface.

The materials systems evaluated were less costly than other high-density, high-purity ceramics of interest because the substrate could be fabricated from less costly, relatively impure materials. The high-purity coatings were to provide the barrier to the molten silicon in one direction, and to autodoping by impurities in the other direction.

The primary candidate materials studied were silicon carbide and silicon nitride. The materials of secondary interest were aluminum nitride, silicon oxynitride, and the Sialons. The silicon carbide and silicon nitride CNTD coatings, hot-pressed over substrates of the same material, were quite resistant to the corrosive action of molten silicon. These coatings were characterized at EPI. They were uniform in thickness, dense, and fine grained. The adhesion of the coatings to the substrates was adequate for tests conducted by the program.

Sessile drop melting experiments were carried out on both SiC and Si_3N_4 coatings in an atmosphere of controlled partial pressure of oxygen in an inert gas ambience. In all tests, the contact angle reached an equilibrium value after about 40 min. For Si_3N_4 coatings, the initial contact angle ranged from about 90 to 65 deg, and finally equilibrated between 60 and 50 deg. For the SiC coatings, the initial range was 50 to 45 deg, finally equilibrating between 30 and 27 deg.

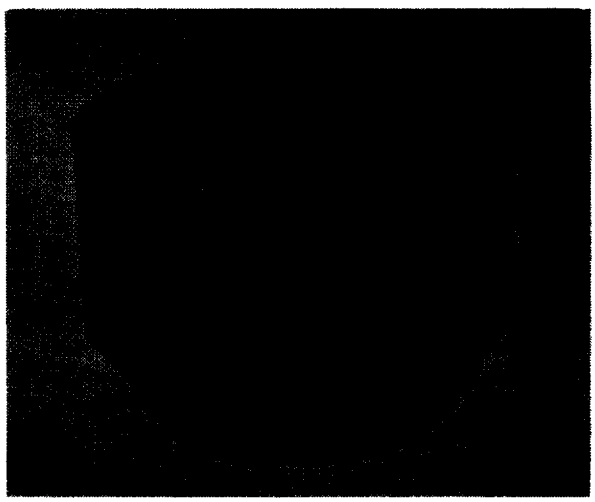
The contact angle for SiC was about 10 deg less than previously reported in the literature. It was noted there was a relationship between the contact angle and the oxygen partial pressure for both of these coating systems over the range of 10^{-16} to 10^{-19} atmosphere. These data suggested that the contact angle decreased with decreased oxygen partial pressure in the sessile drop environment.

Investigations were conducted to determine if the nature of the CNTD-coated surface changed during the sessile drop experiments. The coatings were analyzed outside the drop area by Auger spectroscopy to determine if the surface chemistry was altered. Silicon, nitrogen, carbon, and oxygen were detected as in the Si_3N_4 coatings. A detectable decrease in the nitrogen

content of the surface was found, suggesting that nitrogen loss from the coated surface occurred during the sessile drop experiments.

Photomicrographs of the molten silicon/CNTD SiC and Si_3N_4 interfaces supported the general macroscopic observation that the coatings underwent minimal corrosive penetration by molten silicon.

EPI fabricated crucibles of silicon nitride and silicon carbide, coated with like materials by the CNTD process, and delivered them to JPL (Figures 49 and 50). One-piece dies also were fabricated. Great difficulty was experienced, however, in coating the very narrow slots. A two-piece design was developed that then allowed dies to be fabricated and coated successfully.



(a) CNTD SiC ON HOT-PRESSED SiC (1 wt% B)

(b) CNTD Si_3N_4 ON HOT-PRESSED Si_3N_4 (4 wt% MgO)

Figure 49. CNTD-Coated Containers, as Delivered

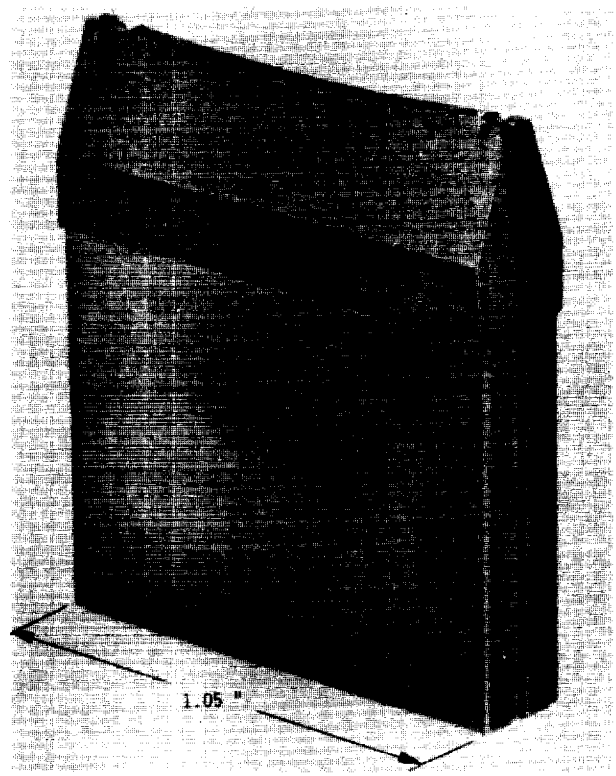


Figure 50. CNTD-SiC-Coated SiC (with 1% by Weight of Boron) Two-Piece Die, Assembled

g. *JPL In-House: Silicon/Refractory Material Compatibility.* Efforts were started at JPL in early 1976 to investigate the compatibility of various refractory materials that were to come in contact with molten silicon (References 71 and 72). Dies and containers for molten silicon were considered major limiting factors in the production of silicon sheet material. JPL efforts primarily involved:

(1) Sessile drop testing with in-situ (at temperature) photographs of molten silicon/substrate wetting angles (Figures 51 and 52). (In Figure 52, the total elapsed time is about 3 min; surrounding lines are reflections from heater element.) Subsequently, wetting angles were measured from these photographs (Figure 53).

(2) Post sessile drop test, cross-sectioning, and microstructural/interface examination.

(3) Quantitative chemical analysis of silicon that had been molten in contact with the refractory materials.

A goal of these activities was to screen numerous candidate materials for their potential use as die or die/container components in silicon crystal growth apparatus. For example, carbon dies used by both IBM and MSEC caused SiC formation in the growing silicon ribbon and subsequent degradation of solar cell efficiency.

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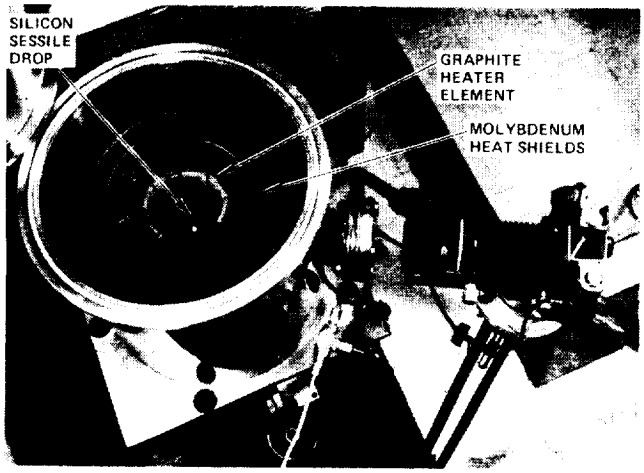

Figure 51. Sessile-Drop Test Equipment

More than a hundred sessile drop tests were performed over a 2 to 3 year period. Classes of materials tested included: carbon, carbides, nitrides, Sialons, oxides, and others. Most samples were procured commercially except for some Sialon material. Some material also was obtained through FSA subcontractors who were developing specialized materials for these applications. Sample fabrication techniques were quite varied and encompassed samples prepared by firing, siliconizing, reaction-sintering, pyrolysis, hot-pressing, CVD, and other preparative techniques. In all, more than 50 different material/processing combinations were subjected to the evaluation.

Examples of types of materials evaluated were: glassy carbon, silicon carbide, silicon nitride, boron nitride, Sialons, and mullite. Except for boron nitride and mullite, density played a key role in limiting the

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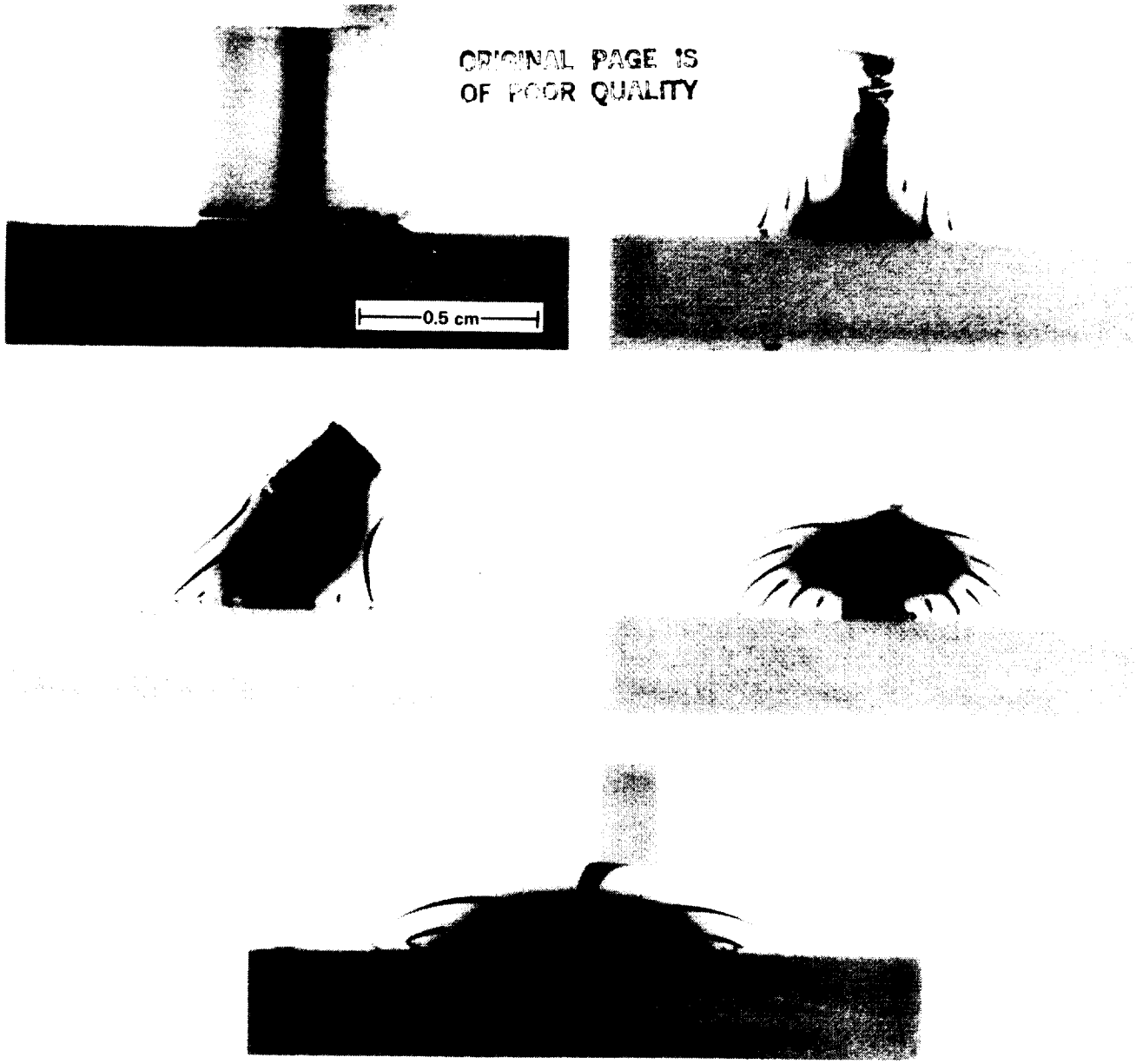


Figure 52. Silicon on Si_3N_4, Melting and Spreading to Mechanically Stable Contact Angle

extent of the interface reaction of these materials. Also important was the process by which the material was made.

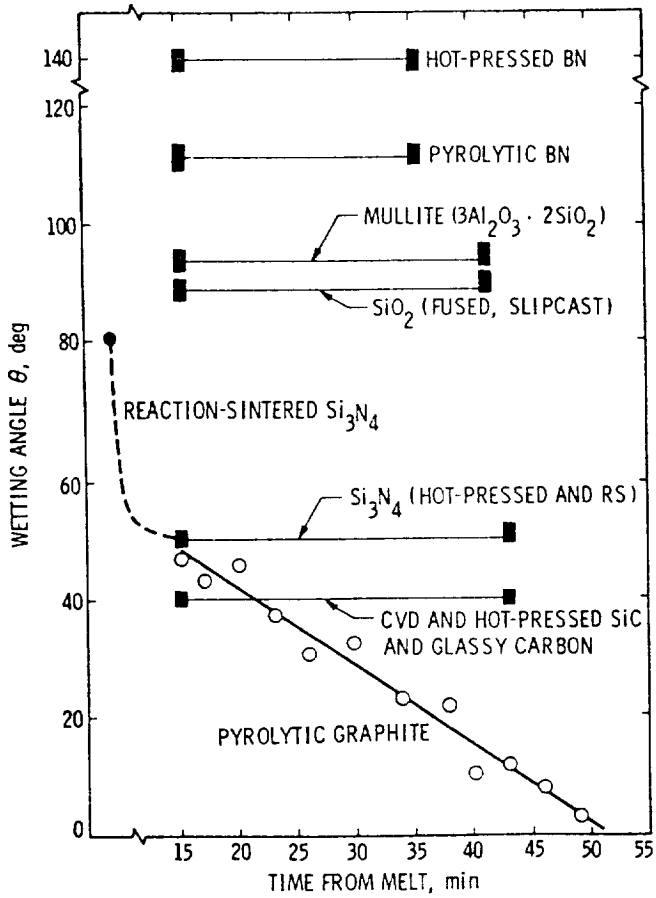


Figure 53. Wetting Angle Versus Time from Melt for Molten Silicon (1430 ± 10°C) on Various Refractory Materials

For example, SiC layers produced by CVD at 1400°C exhibited a much higher rate of degradation when in contact with molten silicon than did CVD SiC produced at or above 1600°C. Purity was another critical aspect of the refractory contact materials. Sintering aids used in hot-pressed or sintered materials would inevitably be dissolved by the silicon sessile drop. Highest-purity materials were produced by CVD.

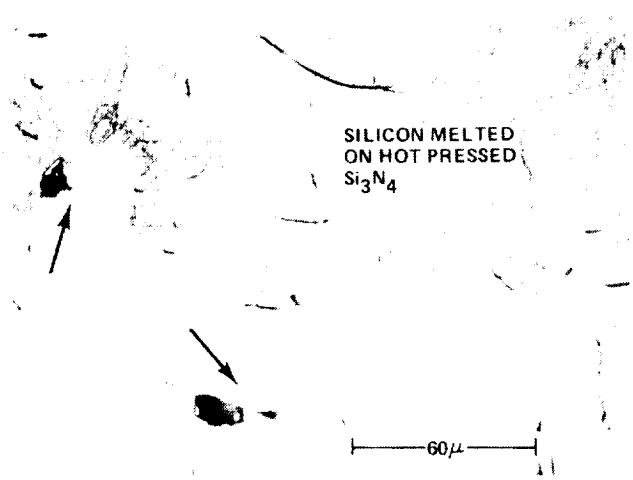
Screening tests consisted of a nominal 40-min, molten-silicon, contact time at 1430°C in a flowing-helium, graphite heater-element furnace.

Subsequently, each sample was sectioned, mounted, polished, and sometimes etched for study under a microscope. Nearly all samples showed some evidence of second-phase precipitations in the silicon matrix (Figure 54) and/or interface reaction as a result of contact (Figure 55). The intrinsic solvent nature of silicon was demonstrated. Best candidate materials (alternatives to fused silica) that emerged from this program were high-temperature chemical-vapor-deposited Si_3N_4 and SiC.

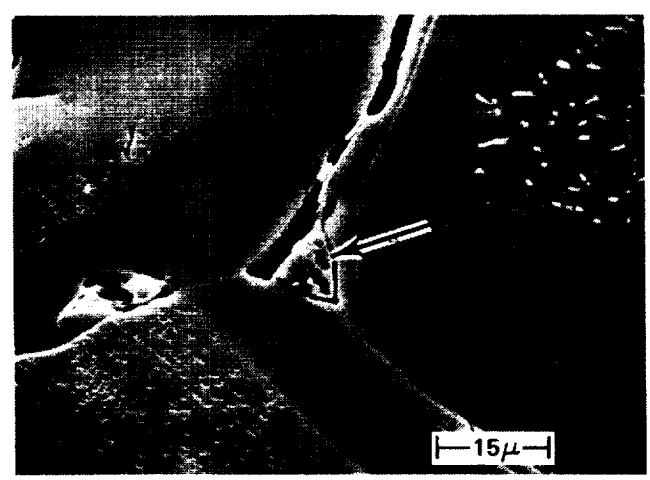
2. Characterization of Defects: Materials Research, Inc.

The main objective of this program was to develop imaging techniques allowing rapid, reproducible, and accurate quantitative evaluation of silicon sheet defect structure (References 73 and 74).

Defect data accumulated for many samples would allow potential cross-correlation among structures that revealed a specific sheet fabrication technique and/or a resultant cell efficiency. Quantified structural defects included grain and twin boundaries, precipitates, and dislocations. Quantitative characterization of these structural defects, revealed by etching the surface of silicon samples, was performed using a Quantimet 720 Image Ana-



(a) PHOTOMICROGRAPH OF SILICON MICROSTRUCTURE AFTER SIRTL ETCH. NOTE DISLOCATIONS AND IMPURITY PHASES (ARROWS)



(b) SCANNING ELECTRON MICROSCOPE PHOTOMICROGRAPH OF GRAIN BOUNDARY IMPURITY PHASE. EDAX READINGS IN AREA INDICATED BY THE ARROW SHOW: HIGH = Al, LOW = Si, AND VERY LOW = Cu

Figure 54. Photomicrographs Showing Second- Phase Precipitates in Silicon Matrix

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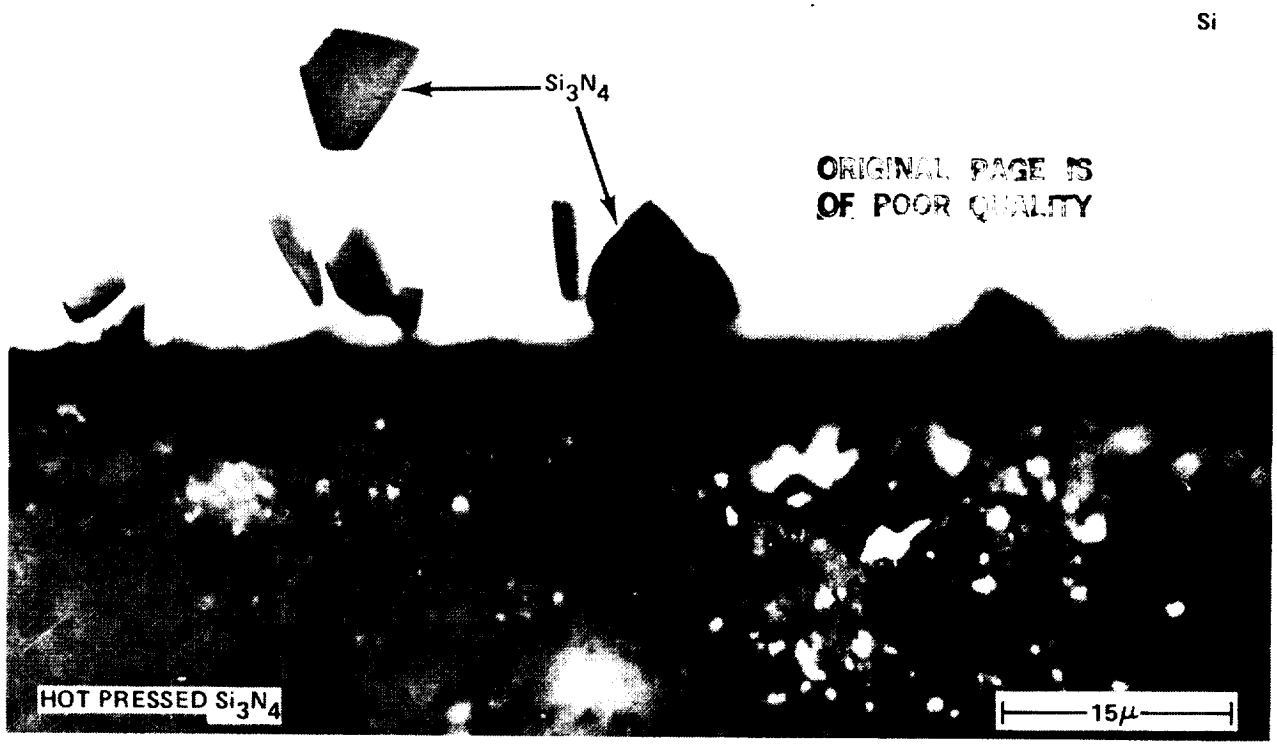

Figure 55. Particles Appearing as Si_3N_4 at Si/Si_3N_4 Interface and Slight Silicon Permeation into Substrate, Hot-Pressed Si_3N_4

lyzer and a reflective-light microscope stage. This optical imaging system could differentiate and count 64 grey levels between black and white. It also would characterize structural defects by measuring their length, perimeter, area, density, spatial distribution, and frequency distribution (in any preselected direction), and was programmable in these measurements. A program that automated the defect-counting procedure was developed for a PDP11 computer. The Quantitative Image Analyzer, however, was extremely sensitive to optical contrasts of various defects. To obtain reproducible results, therefore, the contrasts produced by various defects had to be similar and uniform for each defect type along the entire surface area of samples to be analyzed. To achieve this uniformity, a chemical cleaning and polishing technique was developed for the diverse silicon samples obtained from Mobil Tyco, Wacker, Motorola, and IBM.

3. Growth Process Studies: Solar Energy Research Institute

a. *Solid/Melt Interface Studies of High-Speed Silicon Sheet Growth.* The growth kinetics and growth forms of silicon sheet crystals nucleated at a small diameter were investigated during a 1-year study (July 1983 to July 1984) at SERI (Reference 75). Radial growth-rate anisotropies and limiting growth forms of point-nucleated, dislocation-free silicon sheets spreading horizontally on the free surface of a silicon melt were measured for (100), (110), (111), and (112) sheet planes. Movie photography (16 mm) was used to record the growth process. Analysis of the sheet edges led to predicted geometries for the tip shape of unidirectional, dislocation-free, horizontally growing sheets propagating in various directions within the abovementioned planes. Analysis also provided a crystallographic description of the radial leading edges of the solid/liquid interface during flat-top transition growth in Cz pulling. Similar techniques were used to study polycrystalline sheets and dendrite propagation. For dendrites, growth rates of 2.5 m/min and growth rate anisotropies on the order of 25 were measured.

Included in this study was a feasibility demonstration of a crucible-free horizontal (CFH) ribbon growth method. The top of a large-diameter, vertical, rotating silicon polycrystalline rod was melted by the energy emitted by a specially shaped RF induction coil. The coil shape provided a cool zone from which horizontal ribbon growth took place. The approach was a much simplified modification of the LASS technique (Section IV.B.5.a.). Replenishment was provided by slowly moving the pedestal rod upward. The liquid zone was shallow so that thermal convection effects were minimal. There was no contact of foreign materials with the liquid silicon so the sheet purity was comparable to that of FZ ingots. The polycrystalline silicon sheet that was produced had both large-grained and small-grained regions. Solar cells made from large-grained regions of the silicon sheet had performance characteristics (efficiencies) comparable to those of control cells made from Cz material. However, for CFH ribbon growth to be a viable method, more work is required to refine the hot-zone control, especially under the growing ribbon.

The investigations on idealized growth forms indicate that the (111) planes with low surface free-energies dominate the sheet tip geometry at the solid/liquid interface. They determine the growth form of radially growing sheet crystals (through their intersection with the sheet plane), and contribute to growth rate anisotropies because of the relative difficulty of new growth nucleation on the low free-bond-density (111) surface. These (111) planes also play a determining role in fast dendritic growth by virtue of the high free-bond density associated with reentrant edges at a (111) twin boundary. Earlier work on edge-supported pulling of silicon sheets showed that (111) twin planes can block the spreading of spurious random grains. A similar mechanism has recently been found to be important in stabilizing the crystal structure of horizontally grown sheets. In dendritic web growth, (111) twin planes are key elements of the growth process, and the (111) web surface is very high in quality. The equilibrium structure of long, multicrystalline silicon sheets is dominated by longitudinal grains with (111) boundaries and near <110> surface normals.

Conclusions of this research are:

(1) The properties of the (111) surface in silicon are of major importance for sheet crystal growth.

(2) The (111) plane faceting dominates the edge geometry for radially spreading growth during the flat-top transition phase of Cz crystal pulling.

b. *High-Purity Silicon Crystal Growth Investigations.* Using a high-purity growth technique such as float-zoning, SERI, in this 1984 to 1986 study, investigated silicon crystal growth parameter effects on minority carrier lifetime and solar cell efficiencies (Reference 76).

The goals of this SERI study were to:

(1) Optimize dopants and minority carrier lifetime in FZ material for high-efficiency solar cell applications, including alternative dopants, and the role of evaporation and growth-parameter variations.

(2) Improve the understanding of lifetime degradation mechanisms (point defects, impurities, thermal history, surface effects, etc.).

(3) Characterize lifetime-related crystallographic defects in silicon crystals via x-ray topography.

Float-zoning of high-purity, dislocation-free silicon was conducted both as a tool to study minority carrier lifetime dependence on various growth parameters, and also as a means of growing long-lifetime, heavily-doped, p-type silicon for use in solar cells. Lifetime values of 303 μs for 0.46 Ω-cm resistivity and 214 μs for 0.36 Ω-cm resistivity were achieved when gallium was used as the p-type dopant in <100> crystals. Dislocation-free crystals doped with boron, aluminum, indium, and gallium also were grown over a range of resistivities with dopant species as a parameter. Results of the doping study are summarized in Figure 56 where an envelope of upper and lower bounds is drawn for lifetime versus concentration. Gallium and boron seem to dominate the upper bound, and aluminum and indium dominate the lower. Heavy doping with dislocation-free growth was not achieved for indium, however, and there are not many points to evaluate in the figure. Two boron crystals behaved quite differently, one lying near the upper bound and one near the lower. The upper bound indicates that the following resistivity lifetime combinations are feasible with careful float-zoning, using gallium or possibly boron as a dopant:

Resistivity, Ω-cm	Lifetime, μs
1.0	600
0.5	340
0.2	110
0.1	40

The effect of crystal cooling rate on lifetime was determined from cooling rates ranging from 50 to 600°C/min. The lifetime decreased with increasing cooling rate for both dislocation-free and dislocated crystals. The presence of dislocations, however, had a much more dominant effect in degrading lifetime than did cooling rate. Figure 57 is a plot summarizing results of the lifetime versus cooling rate investigations.

Calculation techniques and pertinent property data were developed for a comparison of vacuum and gas ambients as they affect impurity concentration profiles in FZ and cold-crucible-grown crystals. Graphical impurity profiles were obtained for various segregation and evaporation coefficients in the general case and also for the specific impurities in silicon of Al, Sb, As, B, Cu, Ga, Au, In, Fe, Mn, and P. This exercise indicated that multiple pre-passes in vacuum prior to the crystal growth pass were helpful in reducing the concentration of most metallic impurities to negligible levels.

X-ray topography was used to examine both micro-defects in dislocation-free silicon crystals and dislocations and lattice-plane curvature in silicon ribbons grown by various methods. Improvements also were made in lifetime measurements of heavily-doped silicon.

Key Accomplishments. The key accomplishments of the SERI R&D are:

(1) Minority carrier lifetime values of >200 μs for 0.36 Ω-cm resistivity were achieved for Ga-doped (p-type) silicon.

(2) The lifetime decreased with increasing cooling rate for both dislocation-free and dislocated crystals.

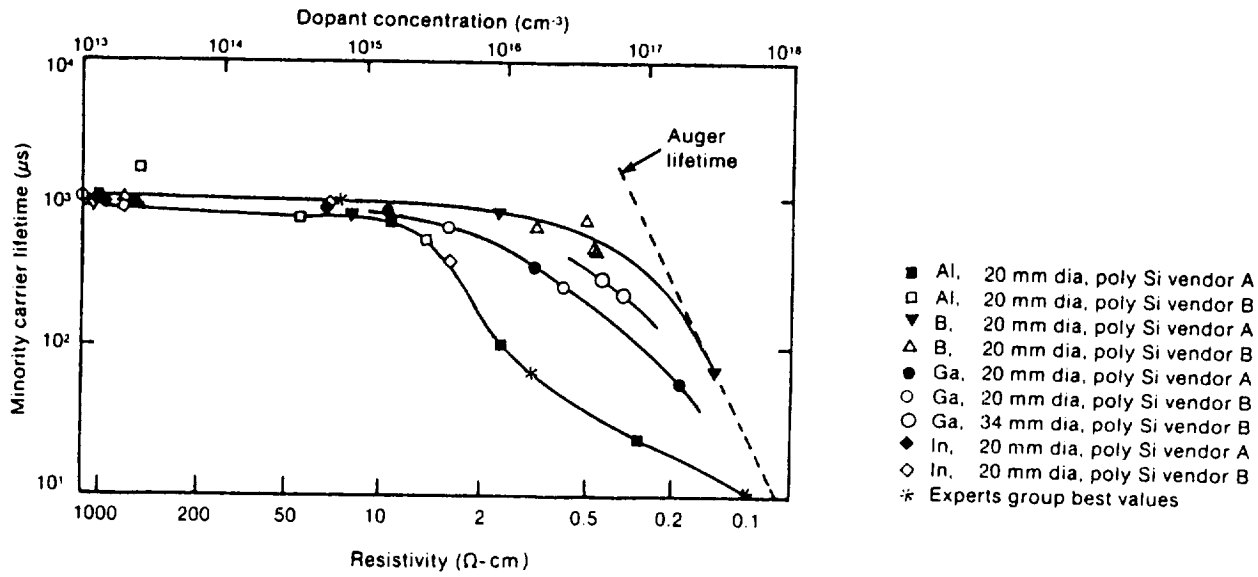

Figure 56. Minority-Carrier Lifetime as a Function of Dopant Concentration for Al, B, Ga, and In Dopants

(3) Multiple pre-passes in vacuum prior to FZ growth were found to reduce the content of most metallic impurities (by 2 to 4 orders of magnitude) to negligible levels.

(4) The effects of impurity redistribution, under the combined actions of segregation and evaporation during crystal growth, were investigated mathematically.

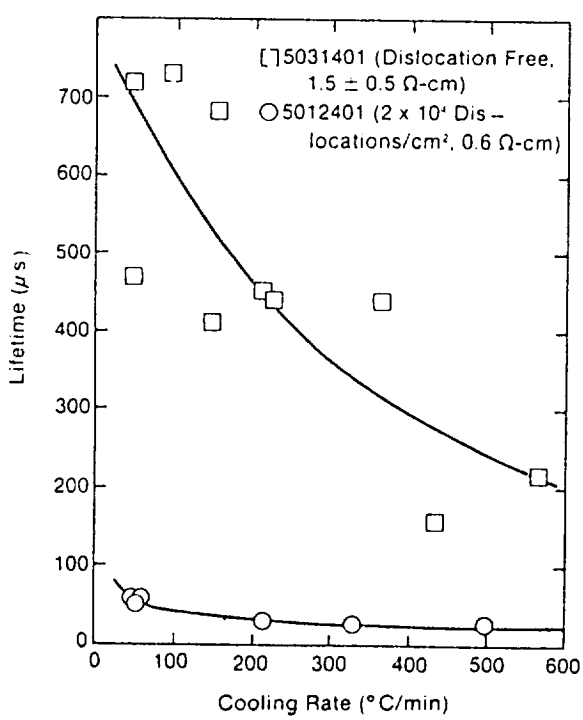

Figure 57. Bulk Minority Carrier Lifetime Versus Cooling Rate for Two Crystals

C. SUMMARY

Ten efforts in the category of Support of Materials Research were carried out by nine organizations. These included several activities for the development and evaluation of materials for use in contact with molten silicon, studies of gas-phase reactions involving silicon, and fundamental studies of crystallization behavior. These studies were valuable both in directly supporting the silicon sheet development efforts and providing contributions to the silicon technology base.

Materials development studies included mullite ($3Al_2O_3 \cdot 2SiO_2$), primarily in support of the Honeywell SOC process. Some crucible evaluation was included. Glassy carbon was developed and characterized at Tylan Corp. A variety of silicon carbides, silicon nitrides, and silicon oxynitrides were developed at Battelle Columbus, RCA Laboratories, and EPI.

Studies that emphasized characterization of materials and reactions included studies of gas-phase reactions at UMR and extensive contact-angle determinations at JPL. Methods to determine microstructure quantitatively were developed at Materials Research Institute. A study of fundamental crystallization front behavior for silicon from the melt was conducted at SERI.

The following major accomplishments were achieved in the Materials Research program:

(1) JPL conducted screening tests to determine the compatibility of molten silicon with more than 50 types of material/processing combinations. Potential materials for further detailed screening tests were identified, and the intrinsic solvent nature of molten silicon was demonstrated.

(2) UMR conducted investigations in the development of refractory dies and containers for use with molten silicon. The partial pressure of oxygen in MSEC's EFG ribbon furnace was measured, and the results led to further refinement of the furnace atmosphere control system. Test sample/silicon interface regions also were characterized for composition, phases, microstructure, and changes.

(3) In a study of die and container materials for molten silicon, Battelle Columbus Laboratories developed silicon beryllium oxynitride as a very promising but expensive die material.

(4) In support of Honeywell's study of the SOC process, the Coors Porcelain Company developed a mullite composition having a thermal expansion that closely matched that of silicon. The corrosion rate of mullite was determined to be low, less than 1 μm/h at the melting point of silicon.

(5) Tylan Corp. conducted a study of a proprietary glass-like carbon coating, Vitre-Graf, that was applied to mullite and graphite. It was demonstrated that coatings could be applied to different grades of mullite. Such coated mullite substrates were successfully coated with silicon in Honeywell's SOC process.

(6) RCA grew silicon ribbon using a CVD Si_3N_4-coated die and determined that the beta-phase of Si_3N_4 is most impervious to attack by molten silicon.

(7) In a program aimed at developing refractory materials for use with molten silicon, EPI produced dense, fine-grained coatings resistant to molten silicon. Prototype containers and dies were fabricated in a manner suitable for high-volume production.

(8) Materials Research, Inc. developed imaging techniques that allowed rapid, accurate, and reproducible measurements of twin and dislocation densities over large surface areas of silicon sheet.

(9) SERI showed that the properties of the <111> surface in silicon are of major importance for sheet crystal growth. Feasibility also was demonstrated for a CFH ribbon growth process.

(10) In a study of high-purity crystal growth, SERI achieved minority carrier lifetime values greater than 200 μs for 0.36 Ω-cm resistivity, gallium-doped (p-type) silicon. It was determined that the lifetime decreased with increasing cooling rate for both dislocation-free and dislocated crystals.

SECTION VII

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Supporting Research: Stress/Strain

A. INTRODUCTION

During the growth of a crystal directly from a pool of molten material, adjacent regions of the crystal will exist simultaneously at different temperatures. The various regions also will cool at different rates. Because local crystal-lattice dimensions depend directly on local temperatures, thermal gradients in the cooling crystals result in stresses between adjacent regions of the crystals. The magnitude of the stresses varies directly with the temperature gradients. In the case of slowly grown symmetrical crystals (e.g., Cz, FZ), these stresses effectively are negligible. However, the stress problem is critical in the case of asymmetrical ribbon crystals formed at high linear growth rates.

The existence of stress during cooldown manifests itself in the ribbon product in one or more of the following ways:

(1) Plastic strain results in buckling (Figure 58) or bowing (Figure 59) in the cooling ribbon. This yields non-flat wafers that are difficult and expensive to process into solar cells. The structural defects generated through accommodation of the stress also result in lowered minority carrier lifetime in the wafer. This, in turn, leads to reduced cell performance.

(2) To accommodate stresses, plastic strain may occur in the plane of the ribbon. This results in a flat, but highly defective ribbon (Figure 60) that is manageable through processing, but yields devices with poor performance.

(3) Ribbon which has deformed plastically can retain considerable residual stress. These ribbons are subject to catastrophic failure during processing or in the field (Figure 61).

(4) Ribbon can deform itself elastically during growth and bend away from the immediate area around the crucible. In doing so, the ribbon moves out of the proper thermal environment needed for continued steady state growth.

To overcome the problem of stress associated with defects, several modeling studies were supported in the Task to understand better the processes of stress development and strain and how to limit them. The mechanical properties of silicon at temperatures up to its melting point were measured to provide the boundary condition data for the modeling work. Studies were conducted by the University of Kentucky, UIC, JPL, and Westinghouse. Summaries of both the contract and in-house R&D tasks that addressed the problems of stress and strain in silicon ribbon growth are included in this Section.

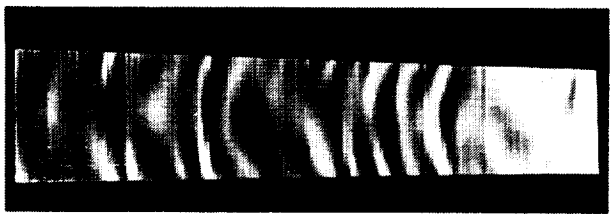

Figure 58. Buckled Silicon Ribbon

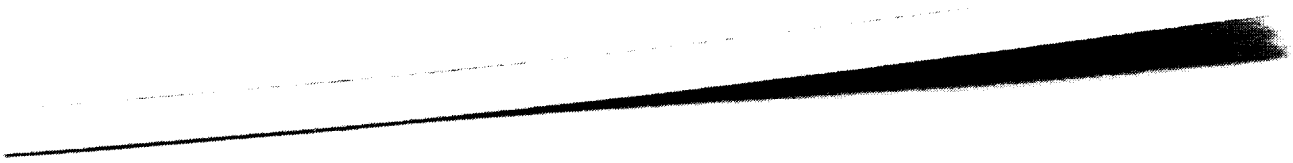

Figure 59. Bowed Silicon Ribbon

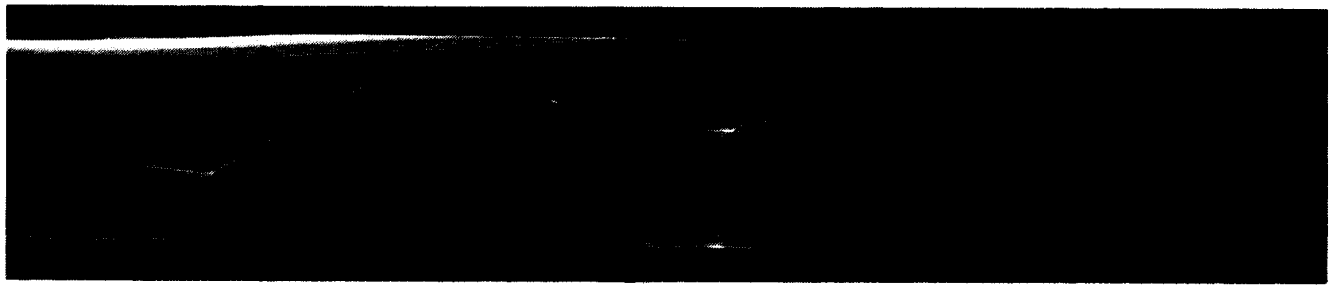

Figure 60. X-Ray Topograph of Defect Structure in Silicon Dendritic-Web Ribbon

Figure 61. Catastrophic Failure of Highly Stressed Ribbon

B. IMPLEMENTATION

1. Stress/Strain Analysis of Silicon Ribbon: University of Kentucky

This contract with the University of Kentucky, begun in 1982, focused on the problem of stress/strain during sheet growth (Reference 77). The three interrelated activities included:

(1) Elastic and plastic stress/strain modeling.

(2) Sheet-defect structure evaluation, such as dislocation mapping.

(3) High-temperature silicon sheet tensile tests, started in mid-1984.

A major goal of the silicon ribbon stress/strain modeling activities was to obtain improved predictions for stable ribbon growth that incorporate criteria for defect formation, plasticity, and creep. Based on work of Sumino and Haasen, a stress/strain model was developed to predict both structure generation (dislocation multiplication) and critical buckling parameters (ribbon thickness and width). Their results showed that some buckling modes grow in time, and others damp out and probably do not affect ribbon growth. This specific result is believed to be new in creep buckling of any general plate and reflects the fact that no external loads are applied.

Under the assumption that ribbon dislocation density must be relatively low to make good PV cells, the adequacy of an elastic-only analysis was demonstrated. Critical (minimum) buckling thickness can be arrived at by elastic analysis, thus saving the time and expense of more complicated plastic models.

The University of Kentucky dislocation and buckling models handle plasticity, creep, and dislocation generation in silicon as a function of strain rate, initial dislocation density, and oxygen concentration. One output of the above models was the dislocation density contour plot. It graphically indicates X and Y coordinate dislocation densities per square centimeter for ribbon grown from a specific thermal profile. An example of these plots is shown in Figure 62.

In the matter of making predictions about buckling, the University of Kentucky models were used to generate buckling mode shape outputs similar to that shown in Figure 63. The parameter λ^2 is positive and largest for this mode (dominant mode). Through use of a constant melt-face dislocation density and a specific thermal profile (such as one used to grow web dendritic material), critical or maximum ribbon widths also were calculated. When ribbon widths were analytically

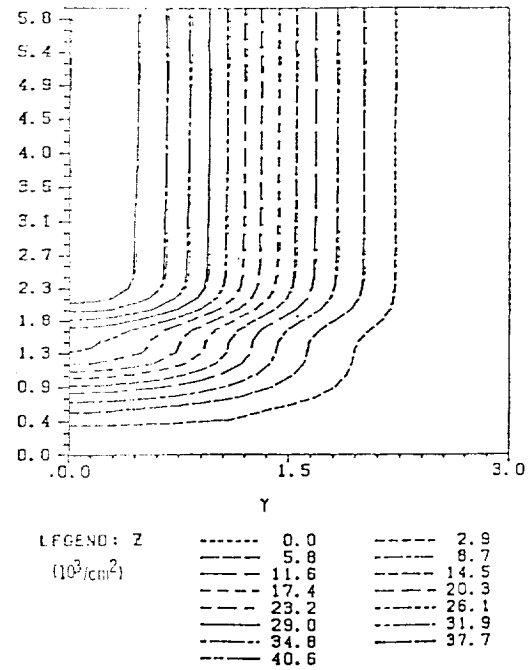

Figure 62. Distribution of Mobile Dislocations in a 6 x 6 cm Silicon Ribbon Subjected to a Modified EFG Thermal Profile and $N_O = 2 \times 10^{-7}/cm^2$

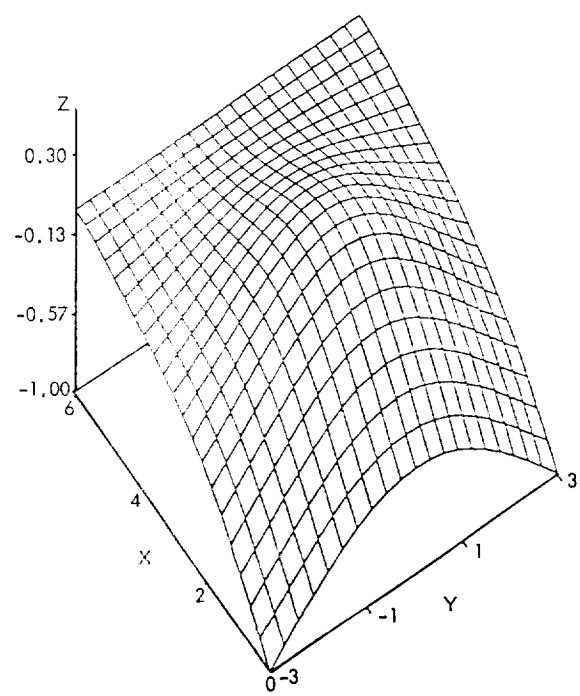

Figure 63. First Buckling Mode Shape for the Westinghouse Thermal Profile (6 x 6 cm Ribbon) and $N_O = 0.15/cm^2$

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varied and in-plane stresses were subsequently calculated, the model either predicts an uncontrolled growth in dislocation (model divergence) or a "small" increase in dislocation density (model convergence). Another important output of the University of Kentucky buckling model is the predicted critical ribbon thicknesses for buckling as functions of thermal profiles and ribbon geometry.

The University of Kentucky has documented a new buckling analysis for the "plastic" range of silicon ribbon. Once in-plane stresses are known, the new version of buckling analysis allows for prediction of buckling modes, if any.

The main limitation now is not in the buckling analysis itself, but in understanding the nature of in-plane stresses because of a lack of knowledge of high-temperature, stress-field, silicon-dislocation behavior. In this regard, the University of Kentucky has developed a model/computer program that will track the motion of a specific dislocation during ribbon growth. This model uses elastic stress field mechanics. In the area of dislocation mapping, dislocations are "inserted" at the ribbon melt interface at various Y positions. Subsequent motion of each dislocation is tracked as it moves through the thermal stress field. To date, evaluation of analytical results indicate that significant dislocation motion and multiplication occur within the first 0.5 cm of the 3-cm-wide ribbon melt interface. A present, limitation of the approach is the indeterminacy of the number and location of dislocations to be inserted.

University of Kentucky investigators also worked on predicting residual stresses developed in a ribbon grown in the temperature profile, $T(x) = 1372 - 99.83\,x + 40c^{-5x}$ (analytical representation of measured ribbon profile, provided by Westinghouse). Low residual stress values were obtained that were relatively consistent with Westinghouse split-width residual stress measurements. The maximum (critical) width to which ribbon could be grown in the same thermal profile was also calculated with zero starting dislocation ($N_0 = 0$). A critical width of about 6 cm is predicted. As the starting dislocation density increases, however, the critical width decreases. For example, for $N_0 = 3/cm^2$, the critical width is predicted to be about 3.5 cm.

High-temperature tensile tests of silicon were conducted as supportive analytical studies. Successful tensile tests on Westinghouse dendritic web and Cz samples were carried out at temperatures up to 1150 and 1200 °C, respectively. Reproducibility of test results seemed very good at 1100 °C and $10^{-4}\ s^{-1}$ strain rate. Flow stress values for dendritic-web material also were comparable with Cz data. Figure 64 shows some resolved shear stress data for dendritic-web material as functions of temperature and strain rate. The trend of high-temperature shear stress for web material is consistent with previous lower-temperature work done by Sumino on Cz material (starting dislocation density of $2 \times 10^4\ cm^{-2}$). Cz samples were used to study effects of laser-cut edges. In this study, significant differences in stress/strain behavior were noted for polished versus unpolished edges.

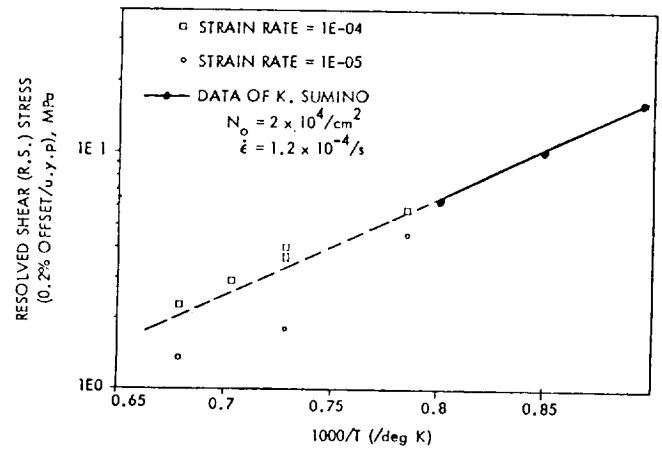

Figure 64. Resolved Shear Stress for Dendritic-Web Ribbon as Functions of Temperature and Strain Rate

The key accomplishments of the this effort were:

(1) An elastic buckling model was developed that predicts the critical silicon ribbon thickness, that corresponds to the onset of instability, as a function of ribbon width.

(2) A viscoplastic strain/stress model based on Sumino's work was used to generate elevated-temperature stress/strain curves, as well as to calculate mobile dislocation multiplication as a result of stress fields.

(3) Computer-generated dislocation maps for dendritic web material were very similar to actual as-grown-ribbon dislocation arrays revealed by x-ray topography.

(4) Successful high-temperature tests (900 to 1300 °C) on Cz and web material were performed. Resolved shear stress was obtained as a function of temperature.

2. Study and Analysis of High-Speed Growth of Silicon Sheets in Inclined Meniscus Configurations: Massachusetts Institute of Technology

A 2-year contract at MIT had the initial purpose of examining the relationship between material properties and transport phenomena during crystal growth in inclined-meniscus configurations at low and moderate growth speeds. The study goals included:

(1) Development of numerical analysis of heat transfer and capillarity in inclined growth configurations.

(2) Verification of this model with data supplied by experimental research groups supported by DOE.

(3) Development of a thermal stress model to be incorporated with the heat transfer analysis.

(4) Parametric studies for silicon growth in a variety of configurations to determine optimal conditions for growth of low-stress ribbon.

In addition to the above goals, the morphological structure of nonplanar silicon solidification surfaces was studied to understand the effects of small amounts of constitutional undercooling on the development of cellular interfaces.

The finite-element analysis used for the detailed model for studying heat transfer and capillarity in meniscus-defined systems was based on the methodology already used by MIT for optimizing the EFG process. This general-purpose model was designed to model the essential heat transfer and capillarity effects in configurations ranging from vertical and slightly inclined edge-supported systems to low-angle growth processes. The program was used to study the parametric sensitivity of various growth geometries with respect to:

(1) Thermal control and growth rate.

(2) Dopant segregation.

(3) Thermal stress.

(4) Interface morphology and stability.

The finite-element analysis program was extended to include silicon sheet growth in inclined-meniscus configurations. This program was useful in predicting the optimized growth conditions that included the determination of the melt/solid interface shape, the melt/gas interface shape to satisfy the hydrostatics equation, and the sheet thickness to satisfy the equilibrium growth angle.

The conclusions of this analysis indicated that, as far as material quality was concerned, there was little to be gained and much to lose in modifying the EFG and dendritic-web systems to incorporate an inclined-meniscus configuration. With this result, and with the intensified Project emphasis on web technology, additional work on an inclined growth system was dropped and the work was redirected to analyze the web system.

The thermal-capillary model for silicon sheet growth then was extended to account for the faceted growth and accompanying growth rate kinetics found in the dendritic web growth system. The crystal thickness was predicted as a function of the pull speed and the location of the controlling nucleation point along the interface. For an idealized thermal ambient, sheet thicknesses were predicted that were extremely close to results for a melt/ solid interface in thermal equilibrium. These results imply that the local undercooling along the interface does not substantially alter the thermal environment for the ribbon as compared to that for an edge-supported growth system without the facet.

Because of a funding cutback, the contract was terminated prior to completion of the research, and no final report was published. In addition, the accuracy of the model developed for the web system has not been tested and verified against the experimental results, as it was for the EFG system.

3. Residual Stresses in Sheet Silicon: University of Illinois at Chicago

A noncontact, nondestructive, room-temperature technique was developed to determine in-plane residual stress over large spatial areas in short, flat, thin, silicon plates (Reference 40). This technique (shadow moiré and laser interferometry) was applied to circular (Reference 78) and rectangular plates (Reference 79). The measurement was compared with an analytical result, and differences between the two results were ascribed to in-plane residual stresses. The measured strains were used in an analysis to obtain the residual stresses. A code was developed that produces a three-dimensional plot of the residual stresses over the measured area.

EFG and dendritic web sheet silicon samples were examined by this technique, and Figures 65 and 66 show the residual stress distribution for these two cases. It should be noted that the edges of the sheet are in compression and the central region is in tension. The EFG samples have a consistently higher residual stress (5 to 10 megapascals) than the dendritic web sheet samples (0.5 MPa).

4. Stress Determination by X-Ray Diffraction (Bond Technique): University of California, Los Angeles

This study evaluated the suitability of the bond x-ray diffraction technique in determining small, local changes in the bond lengths within silicon as a result of residual stresses (Reference 80). The technique, which requires an accuracy of measurement to 8×10^{-5} Å was applied to EFG ribbon. Results indicated that measurements could be made within an approximate precision of ± 10 MPa. Measurements that were obtained indicated a maximum value of 115 MPa (about the fracture stress of silicon and one order of magnitude greater than the results cited earlier for the study by the UIC). Because the method was found to be extremely tedious and time consuming, it is not recommended as a routinely useful method.

5. In-House Supporting Stress/Strain Research: JPL

Research at JPL in support of the Silicon Sheet Task included measurement of the mechanical properties of silicon as a function of temperature, a finite-element analysis of stress and strain in silicon ribbon during the growth process, and a study of the fracture mechanics of silicon sheet.

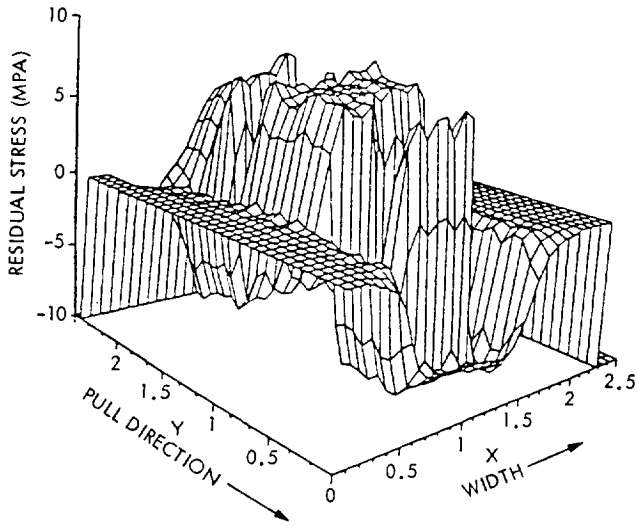

Figure 65. In-Plane Residual Stress Variation Over a 2 x 4 in. EFG Sheet

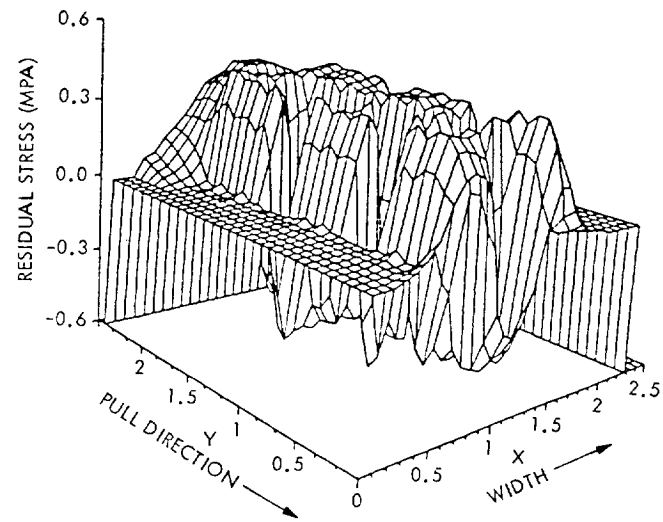

Figure 66. In-Plane Residual Stress Variation Over a 2 x 2 in. Dendritic-Web Sheet

a. *Mechanical Properties Studies.* Mechanical property data on silicon were obtained on Cz material (as-cut and mechanically polished) and Westinghouse dendritic-web ribbon. Wide scatter was characteristic of most literature data (References 81 through 87) and JPL data. Attempts to relate this scatter to dislocation density have not proven successful. Some of the scatter in the JPL data can be a result of evolving methods for specimen cutting, handling, loading, heating, and instrumentation. As a result, the data must be regarded as very preliminary.

Testing was done in argon from 800 to 1375 °C at strain rates from 6 x 10^{-7}/s to 1 x 10^{-3}/s. Crystal orientation of the material also was varied. Dendritic-web ribbon for testing was cut with the tensile axis in the 211 direction. Cz material also was tested in this orientation, 111 face with 211 tensile axis, with the faces mechanically polished. As-cut Cz material was tested with a 110 face in the 211 direction and with a 111 face in a 110 direction. An extensiometer was used to obtain strain rate/displacement data, which varied as a result of sample distortion in the grips, although crosshead travel speed remained constant. The available literature data from JPL and from Schroter, et al. (Reference 82), Yonenaga and Sumino (Reference 86), and Siethoff (Reference 87) are linearly extrapolated in Figure 67. The JPL data are 0.2% offset data, and the literature lines are lower yield point (σ_{LYP}). JPL data obtained at 800, 900, 1000, and

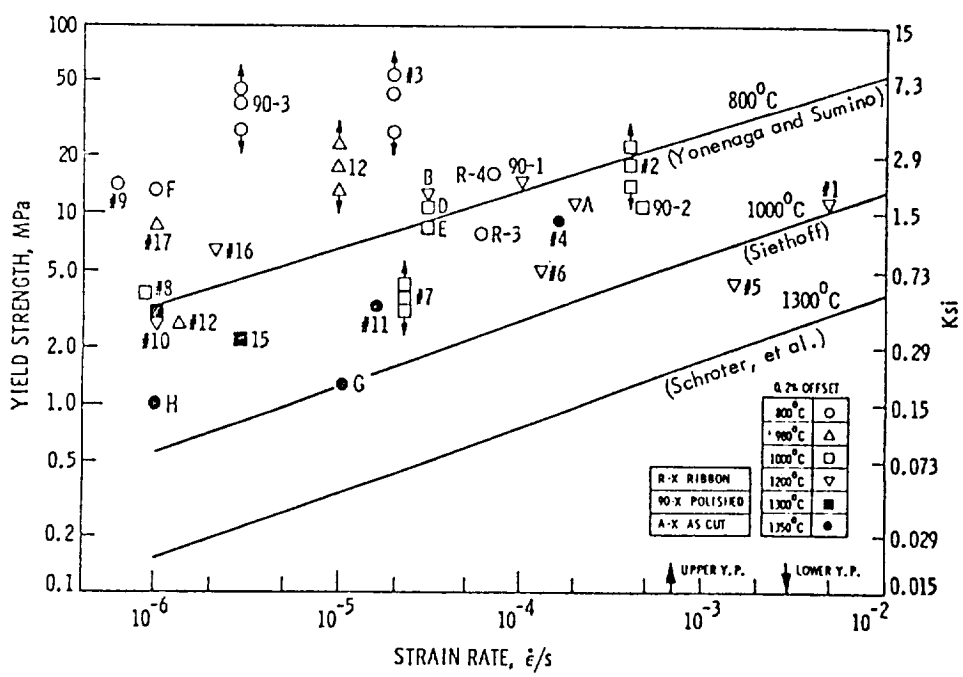

Figure 67. Silicon Yield Strength Versus Strain Rate

1350 °C on polished Cz silicon are displaced above the literature values. Data obtained at 1200 °C show significantly more scatter. It is possible to speculate that the 1200 °C scatter is caused by the rate of precipitation and/or formation of SiO_2 particles and is caused by heating rates for the sample or holding time at 1200 °C. The two data points obtained for Westinghouse ribbon (R-3 and R-4) at 800 °C fall almost on the literature value lines for 800 °C. Thus, there seems to be significant differences between the Cz and the Westinghouse ribbon as measured by 0.02% offset yield strength.

Young's modulus is independent of strain rate and is a function of temperature and crystal orientation. JPL data indicate the observed modulus to be a function of strain rate. The values obtained, therefore, are not a true Young's modulus, but rather a pseudo-modulus. These data are plotted in Figure 68 (the literature room-temperature modulus is about 20 x 10^6 psi).

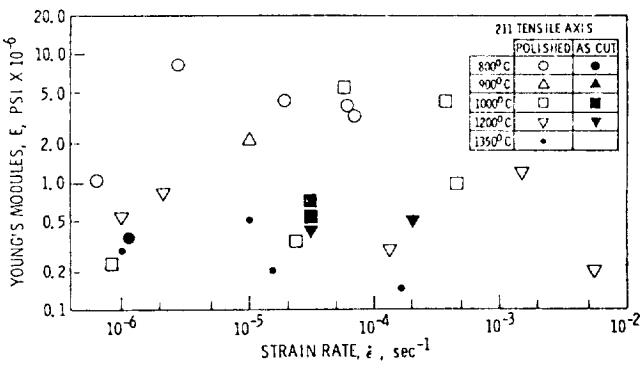

Figure 68. Pseudo Modulus of Silicon as Measured at JPL

b. *Study on Annealing Effects in Low- and High-Stress Dendritic-Web Ribbon.* A systematic study (Reference 88) was conducted involving measurement of the structural and electrical characteristics of low- and high-stress silicon dendritic-web ribbon as a function of annealing temperature in the 450 to 1050 °C range. The lower-stress ribbon had residual stresses ranging from 1.0 to 9.3 Mdyn/cm^2, and the residual stresses for the higher-stress material were measured to be between 38 and 40 Mdyn/cm^2. These stresses were measured by Westinghouse.

The results indicated the minority carrier lifetime of dendritic-web ribbon silicon can be improved with annealing. The magnitude of the improvement in lifetime depended on the annealing temperature and the residual stress of the material. On average, material with lower residual stress improved by an order of magnitude, and the higher-stress material improved by a factor of six. The peak in the lifetime improvement for the higher stress material occurred at a lower annealing temperature than for the low-stress ribbon. In both cases, the peak lifetime was at a temperature lower than the usual processing temperature for $n^+ - p$ junction formation, implying that to optimize fully the solar cell performance, the devices should be processed at a temperature other than the standard temperature used.

c. *Finite-Element Stress/Strain Analysis.* A finite-element analysis was used to identify and evaluate the following significant web parameters that would negatively affect the rapid growth of usable dendritic web ribbon: elastic, plastic, and creep material properties; influence of the size of the dendrites; influence of the ribbon geometry; and the influence of the axial and lateral temperature distributions. The effects of these parameters on the buckling, in-process thermal stresses and residual stresses were evaluated.

A nonlinear analysis was required to predict accurately the thermal stresses and accurate material properties up to the melting temperature of the silicon. A nonlinear simulation of the growth of the silicon ribbon indicated that the strain and stress history of the silicon is important in the determination of the stresses in the ribbon.

To establish a more efficient and better simulation code to predict the desired parameters of the ribbon, a special, finite-element code development was initiated. The code predicts the desired responses of the ribbon to the parameters. It also permits the calculation of the shear stresses in the slip directions of interest to the silicon, the stress redistribution when the ribbon is arbitrarily cut, and the lateral thermal profile that will minimize the thermal stresses for any specified axial temperature distribution.

The simulation program was developed to predict the relevant stress/strain parameters for any geometry (e.g., ribbon, nonagon, cylinders, etc.) at any inclination.

d. *Fracture Mechanics Study.* A program dealing with fracture mechanics of silicon was initiated in 1977. Since then, more than 30 papers have been published in the area, and four NASA Tech Brief Awards have been awarded. The highlights of the fracture mechanics of the silicon program are summarized as follows:

(1) Developed a standard test method for the strength of silicon wafers and solar cells (Reference 89). The mechanical strength and the nature of the flaws in silicon wafers and solar cells (chips and cracks) were evaluated by applying stresses in four-point twisting, as shown in Figure 69. This unique test method has been widely accepted by international and domestic PV industries for quality control and production-line/proof-testing (References 90, 91, and 92). The test, which can be used to eliminate defective wafers prior to cell processing and thereby reduce costs significantly, has been implemented by Heliotronic GmbH, Applied Solar Energy Corp., ARCO Solar, Inc., Motorola, Inc., Mobil Solar Energy Corp., Spectrolab, Inc., and Texas Instruments, Inc.

(2) Developed test methodology and generated data in the area of fracture mechanics of silicon (References 93 through 98). The fracture toughness (K_{IC}) values on the major planes of

Figure 69. Four-Point Twisting Test of Silicon Wafer

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single-crystal and polycrystalline silicon were determined and are shown in Table 11. Crack-growth study in single-crystal silicon indicated lack of subcritical crack propagation at room temperature in air. Results of this effort have been used by MSEC, Motorola, and IBM to enhance production yields, improve solar cell reliability and durability, and establish mechanical design criteria.

Table 11. K_{IC} Values of Silicon

Single crystal	<100> :	0.95 $MN/m^{3/2}$
	<110> :	0.90 $MN/m^{3/2}$
	<111> :	0.82 $MN/m^{3/2}$
Polycrystalline	:	0.75 $MN/m^{3/2}$

(3) Applied fracture mechanics to predict allowable crack size of solar cells for solar module design (Reference 99) and performed failure analysis (References 100 and 101). A fracture mechanics technique was used to model silicon ingot wafering, to predict thickness and diameter limits for wafering, and to postulate improved methods (see References 36 through 39).

(4) Fracture mechanics of silicon technology have been recently extended to evaluate other semiconductor materials such as GaAs (References 102 through 105).

C. SUMMARY

The work supported by the FSA Project to solve the problem of stress and strain in silicon ribbon growth continued until the end of FY 86. It was not completed at that time, but substantial progress was achieved toward understanding the processes at work.

Mechanical property data for specific types of silicon up to 1200 °C are now adequate to support the modeling work, although the data for temperatures greater than 1200 °C are still inadequate. Additional data or confirming data for each specific type of silicon may be required. Control of plastic buckling will require this higher-temperature information.

Data taken in the program generally correlate well with earlier Sumino data. The computer models now show good correlation with observed dislocation generation and distributions, although observed dislocation densities are generally lower than calculated. Good agreement is now seen among the stress calculations of all Project researchers. At this time, however, the effect of creep relaxation on the modeling results remains in question. Application of the results of the modeling work, especially regarding growth interface thermal profiles, has led to growth of ribbon with reduced levels of residual stress and buckling.

Some modeling results predict that critical maximum values of ribbon width and pull speed may exist that are only slightly higher than presently achieved values. Various ribbon growth process approaches remain that may mitigate the problem, including solid solution hardening, controlled temperature profiles across the ribbon width, non-perpendicular crystallization front, and control of strain distribution. Although there is still some uncertainty, the final prognosis is that increases could be attainable in ribbon area growth speed that would make widespread use of photovoltaics possible.

Major accomplishments of the silicon ribbon stress/strain program include the following:

(1) The University of Kentucky developed an elastic buckling model that predicts the critical ribbon thickness, corresponding to the onset of instability as a function of ribbon width. A viscoplastic stress/strain model also was developed and used to calculate elevated-temperature stress/strain curves, as well as calculate mobile dislocation multiplication as a result of stress fields.

(2) JPL conducted a study of silicon fracture mechanics, finite-element analysis of stress/strain, and measurements of silicon mechanical property data. A standard method was developed for testing the strength of silicon sheet and solar cells, using four-point twisting. An annealing study of dendritic-web ribbon showed that annealing can improve minority carrier lifetime, with the degree of improvement dependent upon the annealing temperature and the residual stress of the material.

(3) MIT completed a finite-element analysis program to predict the optimized operating conditions for an idealized inclined-growth system.

(4) UCI developed a noncontact, non-destructive, room-temperature technique to determine in-plane residual stress over large areas in sheet material.

SECTION VIII

Conclusions and Assessment

At the beginning of the Silicon Sheet Task Technology Development program, technical goals were established for the Silicon Sheet Task to meet the Project's price goal of $0.50/W_p$ (1975 dollars). The Price Allocation Guidelines for both ingot and non-ingot technologies are presented in Table 12.

The degree of technical success was measured by the performance of the various technologies against the goals and schedule of the Project. Individual silicon sheet technologies received support based not only on their potential to achieve the Project's goals, but also on their performance against the Project's goals once the technologies were funded. In 1982, when the Project was redirected to emphasize generic research, the program shifted to focus on the technical barriers that prevented the various sheet technologies from achieving the $0.50/W_p$ (1975 dollars) goal.

The commercial scene clearly reveals the present status of silicon sheet technology used for terrestrial photovoltaics. Although thin-film PV modules (specifically, α-Si) are being used for terrestrial power generation applications, the vast majority of modules produced and sold still use crystalline silicon solar cells. Most of these are produced from either Cz or cast polycrystalline wafers. One family of modules, produced from ribbon silicon sheet, is offered by MSEC. Although the cost of crystalline silicon modules is significantly reduced today, the market price of Cz silicon wafers is about what it was in 1975. Thus, the cost of Cz wafers actually has come down in terms of real dollars. No low-cost, "high-efficiency" sheet, however, is available in the marketplace.

Both the achievements of the Silicon Sheet Task and the present status of the individual silicon sheet technologies are summarized in the preceding sections of this report. Although the allocated goals of the Project were not attained, the technical achievements of the Task are considerable. Ingot technology, for example, is significantly improved today as compared to where it was at the inception of the Project (Table 13).

The FSA Silicon Sheet Task is directly responsible for the semiconductor industry's scaling-up of ingot size from 3-in.-diameter (1975) to the current production diameters of 4 to 6 in. and to the 8- to 12-in.-diameter ingots grown on a nonroutine basis by the silicon manufacturers. Now used commercially, semicontinuous ingot growth (more than one ingot from a single crucible) was recommended and developed by the Task. In addition, the Task was responsible for the development of fully automated Cz growth and wafering processes. Three FSA-supported ingot technologies (Cz, HEM, and UCP) are used in commercial processes today.

Since 1975, ribbon technology has improved even more dramatically than ingot technology. Progress in development of dendritic-web technology is shown in Figures 36 through 38. EFG ribbon material is commercially available today in modules, and all five processes listed in Table 14 now are being developed with private funds.

Historically, it had been anticipated that silicon-ingot technology, the first to be commercialized, would be replaced by the lower-cost, silicon-ribbon PV systems. However, changing module performance requirements by the utilities, changes in DOE program scope, focus, and funding, and frequently disappointing rates of development of both silicon-ribbon and thin-film technologies have made it difficult to predict the future for PV materials technologies.

The requirements demanded by utilities for cost versus performance of PV modules for large-scale applications have been calculated and published recently (see References 4, 106, and 107). Although the results vary in detail, they are of similar magnitude and lead to the following two conclusions shared by all the publications' authors:

(1) Product acceptability is dependent upon trade-off between area cost and module efficiency. Only by achieving high module efficiencies can high module area cost fall within an acceptable range.

(2) There are three competing module options being considered with no clear-cut, most-successful contender identified. The three module options are concentrator systems, crystalline silicon flat-plate systems, and tandem-junction thin-film systems.

To compete successfully, silicon sheet must be capable of achieving both the performance and cost criteria presented in Table 12. Performance is a function of material perfection.

A conversion efficiency of 20% has been reported for crystalline silicon solar cells fabricated from highly perfect FZ silicon wafers, and >18% efficiency has been reported for devices fabricated from Cz wafers. Yet, for these ingot-based sheet production processes, the required price goals are currently unattainable because of the materials utilization inefficiency involved in wafering.

Of the existing ribbon growth processes, only one seems to have the potential to achieve both the high-efficiency performance and cost targets demanded by the utilities. With reassuring repeatability, dendritic-web

Table 12. Price Allocation Guidelines for Ingot and Non-Ingot Technologies (in 1975 dollars)

Ingot Technology						
Efficiency		1978	1980	1982	1984	1986
Encapsulated Cell		11.5	13	14	15	16.9
Module		8.6	10.1	11.2	12.8	14.4
		Estimate	Guidelines			Goals
Silicon	$/kg	65	60	40	17	10
	$/$W_p$	1.42	1.10	0.47	0.19	0.095
Sheet (value added)	$/m^2 sheet	214	129	90	54	18
	$/$W_p$	2.33	1.24	0.72	0.38	0.112
Cells (value added)	$/m^2 cell	200	120	52	30	22
	$/$W_p$	1.74	0.92	0.37	0.20	0.130
Encapsulation materials	$/m^2 module	30	25	15	10	8
	$/$W_p$	0.35	0.25	0.13	0.08	0.055
Module (value added)	$/m^2 module	100	50	34	20	15.5
	$/$W_p$	1.16	0.49	0.31	0.15	0.108
Total	$/$W_p$	7.00	4.00	2.00	1.00	0.50

Non-Ingot Technology						
Efficiency		1978	1980	1982	1984	1986
Encapsulated Cell		—	11	12	13	14
Module		—	9.9	10.8	11.8	12.9
		Estimate	Guidelines			Goals
Silicon	$/kg	65	60	40	17	10
	$/$W_p$	—	0.40	0.20	0.07	0.030
Sheet (value added)	$/m^2 sheet	—	154	98	55	17.4
	$/$W_p$	—	1.75	0.91	0.45	0.131
Cells (value added)	$/m^2 cell	200	120	52	30	22
	$/$W_p$	—	1.09	0.43	0.23	0.157
Encapsulation materials	$/m^2 module	30	25	15	10	8
	$/$W_p$	—	0.25	0.14	0.08	0.062
Module (value added)	$/m^2 module	100	50	34	20	15.5
	$/$W_p$	—	0.51	0.32	0.17	0.120
Total	$/$W_p$	7.00	4.00	2.00	1.00	0.50

Table 13. Status of Silicon Ingot Growth and Wafering

Growth Technology	Present Status
Czochralski	Ingots, 20-cm-diameter, being grown at 5 cm/h (3.7 kg/h), versus 7.5-cm-diameter at 5 cm/h in 1975
	Fully automated ingot growth machine in production (versus fully manual machine in 1975)
Heat exchange method	Ingots 33 x 33 x 15 cm being grown, then cut into 10 x 10 x 15 cm bars
Semix process	In full commercial production, but details are unavailable

Wafering Technology	Present Status
Czochralski	Ingots, 20-cm-diameter, sliced with ID saw at 8 min/wafer
	Cycle time to next cut: 10 s
Heat exchange method	Fixed-Abrasive Sawing Technique being developed under funding by DARPA
	48 wafers per inch (14 mil thick) being routinely cut
	64 wafers per inch (10 to 11 mil) wafering demonstrated

silicon has been used to produce solar cells with efficiencies greater than 16%. There is confidence that with improvement in both growth and device processes, cell performance also can be improved even in the production environment. For the growth process, uncertainty lies in the ability to achieve the cost goals (see Reference 4). The single most important cost driver for the dendritic-web process is the area throughput rate. Various cost analyses set the threshold to attain the $0.70/$W_p$ (1980 dollars) module price goal at an area growth rate of 13 to 25 cm^2/min (see Reference 1) as compared to the presently demonstrated capability of about 6 cm^2/min for the growth of long ribbons. The best demonstrated weekly throughput observed at Westinghouse for a single machine in a quasi-pilot-production mode is about 50,000 cm^2, as compared to the Westinghouse internal goal of 180,000 cm^2.

Whisnant (Reference 106) also concludes that attainment of dendritic web's considerable potential for market contention will be determined by achievement of 15 to 20 cm^2/min growth rates with module efficiencies near 15%. DeMeo and Taylor (see Reference 4) point out that efficiency and cost goals may not be mutually attainable, and that "the advanced processes invariably trade off efficiency for lower cost of production." They urge parallel research to ensure a threefold achievement: (1) continuous operation, (2) a sufficiently high ribbon or sheet growth rate, and (3) a high yield of cells with target efficiencies.

The Silicon Sheet Task concluded:

(1) Single-crystal ingot technology easily can achieve the required efficiencies. However, ingot technology cannot become a contender unless there is a breakthrough in wafering technology, which is unlikely without additional funding.

(2) Of the existing ribbon technologies, only one (dendritic-web ribbon) has the potential to achieve the utilities-demanded efficiencies, but even this ribbon technology will require process improvement. The present product is too imperfect to achieve the efficiencies of Cz wafers processed today. At present, the dendritic-web process does not achieve the necessary throughput rates to meet the cost goals. Technology development, in the form of increased linear pull speeds or ribbon widths to yield larger area growth rates, is needed to achieve the throughput goals. Increases in area growth rates, however, may result in reduced cell efficiency because of increased defect density or reduced yield caused by increased stress and strain (see Chalmer's "speed limit" in Workshop on High-Speed Growth and Characterization of Crystals for Solar Cells, Appendix B, No. 2.). Numerous technical problems remain to be solved to overcome successfully the barriers to higher growth rates. These problems include achievement of control of the processes of heat flow in the growing ribbon, thermal stress and strain generation, impurity redistribution, and interface stability in a thermally and chemically dynamic environment. Each of these, by itself, is a challenging research problem that requires not only the resources of appropriate research tools, money, and people, but also the time to establish a useful understanding of the operating phenomena.

(3) Concentrators and thin films, as contending technologies, are not without serious problems themselves. Because they are less mature technologies, they also may hold unexpected pitfalls. Thus, crystalline silicon technology may yet find a permanent place in large-scale terrestrial PV applications; however, it is not yet clear which crystalline silicon technology will be most successful.

*Table 14. Present Status of Silicon Ribbon Technology**

Growth Data					
Technology	Thickness, μm	Width, cm	Length, m	Linear Growth Rate, cm/min	Area Growth Rate, cm^2/min
EFG	150-300	45 (nonagon circumference)	7 maximum	2.2	100
Dendritic web	150 nominal	6.7 maximum	11 maximum	1.7 sustained	7 (meters of length) 8.5 (1 m length)
LASS	500-1500	15 maximum	46 maximum	20-40 typical	600 typical maximum
ESR	250-325	5.5	Limited by filament length	1.9-2.5	14 maximum
RTR	150-250	5-10	0.15-0.3	2.5-3.8	13-38

Cell and Module Efficiencies		
Technology	Cell Efficiency, AM1	Module Efficiency
EFG (commercialized)	5 x 10 cm: 12-13% average 14.7-14.8% peak	16 x 35.5 in.: little over 11% 4 x 6 ft: 10-11%
Dendritic web	1 cm^2 17.3% maximum 25 cm^2: 16.4% maximum 14.0% average	16 x 48 in.: 14% maximum
LASS	4 x 4 cm: 12.0% maximum 10.5% average	No modules made
ESR	5 x 10 cm: 12.6% (average of 40 cells)	Information not available
RTR	Information not available	Information not available

*There is considerable variation in ribbon quality and cost for these technologies.

SECTION IX

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APPENDIX A

Modeling: Sheet Price Estimation Guidelines

At the beginning of the FSA Project, the Project Analysis and Integration Area (PA&I) established price goals for the power developed through flat-plate solar arrays in terms of $\$/W_p$ and $\$/M^2$ of module in order to meet the Project objective of developing the technology to make photovoltaic (PV) energy an economically viable alternative energy source. The price goals were, in turn, translated by the PA&I into various technology related goals in terms of throughput, efficiency, material consumption, and yields appropriate for each process step. The process steps themselves depend upon various alternative technologies for material processing, such as ingot and ribbon technologies. Various options were explored for each of these alternatives. The price allocation guidelines were established for each of the options developed.

Economic analysis was used as a tool for identifying the primary cost drivers so that the developmental efforts through innovative ideas may be concentrated in those areas in order to meet the price goals. In-house studies were conducted to guide the developmental efforts.

In order to achieve the goal, a certain production rate and sheet quality are required. Production parameters such as ribbon width, growth rate, run length time, ribbons per furnace, production yield, and duty cycle are process dependent. Annual Manufacturing Cost (AMC) of producing certain quantity of silicon sheet per year is expressed as a function of five cost parameters by the Interim Price Estimation Guidelines (IPEG). These parameters are equipment cost, space required, direct labor, materials and supplies, and utilities.

The process add-on price in terms of $\$/m^2$ is obtained by the ratio of AMC ($/year) to the quantity of sheet produced per year (m^2/year). A program named Sensitivity Analysis using IPEG (SAIPEG) was developed with special codes specific to each process for computing various parameters, as well as for computing yearly throughput based on production parameters. The SAIPEG program was very helpful in understanding the relative importance of cost parameters, and add-on price sensitivity to each of them, so that developmental efforts could be directed appropriately. This analysis would give an estimate of how much throughput is essential to achieve the price goal.

One of the studies was "Cost of Czochralski Wafers as a Function of Diameter" (Reference A-1). Results indicate a small but continuous decrease in sheet cost with increasing ingot size. Sheet costs including silicon are projected to be $50 to $60/$m^2$ (1980 dollars) depending upon techniques used.

Another related study (Reference A-2) discusses the (FSA) Flat-Plate Solar Array Project perspective of high-speed growth of silicon crystals. The cost of materials dominate the cost of PV modules; hence, the PV technology has to be based on unique material conserving sheet growth processes. The direction of development of sheet technologies pursued by the FSA Project had been toward minimizing material use while achieving maximum throughput and higher sheet quality within the bounds of low-cost requirements. Figure A-1 shows add-on price sensitivity to various cost parameters of the dendritic-web growth process.

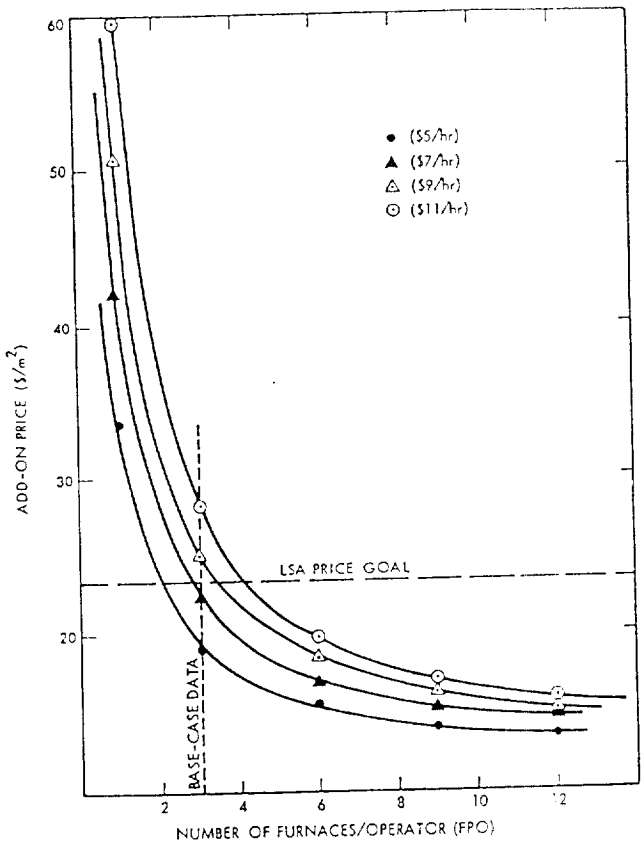

Figure A-1. EFG Process Direct Labor Cost Versus Add-on Price

Similar studies performed for the price estimates for production of wafers from silicon ingots are discussed in detail in References A-3 and A-4. Most solar cells, however, are produced from wafers sliced from crystalline silicon ingots. The cost of the slicing process is a major part of the cost of producing silicon sheet. The less expensive wafering technologies are therefore, of great importance in reducing the cost of PV modules. The add-on price estimates for three wafering technologies, namely, inside diameter (ID) sawing, (MBS) sawing, and fixed abrasive slicing technique (FAST) are discussed in these references. The analysis indicated that both ID and FAST technologies were expected to achieve the price allocation provided the assumptions implied in the input data are realized. The MBS technology projections, however, indicated that its progress would not be sufficient to achieve the allocated price goal before 1986.

Trade-offs in ingot shaping and price of solar PV modules were studied (Reference A-5). Growth of round ingots is cost effective for sheets, but leaves unused space when round cells are packed into a module. This reduces the packing efficiency from 95% for square cells to about 78%. Shaping these ingots into squares with regrowth of cut silicon improves the packing factor, but increases growth cost. It is shown that shaping results in cost savings of up to 21% for a 15-cm-diameter ingot.

Sensitivity analysis study results for the add-on price estimate for the edge-defined film-fed growth (EFG) process are described in detail in Reference A-6. The study indicated that direct labor was the primary cost driver, and a representative sample of the sensitivity analysis results is shown in Figure A-2. It represents the add-on price sensitivity of the EFG

process to the direct labor cost. The study results indicated that the add-on price goal for the EFG process can be met if all the assumptions implied in the input data can be achieved.

Similarly, sensitivity analysis results for the add-on price estimate for the web process are described in detail in Reference A-7. The direct labor cost was also identified to be the primary cost driver for the web process. A representative sample of add-on price sensitivity to silicon price is shown in Figure A-3.

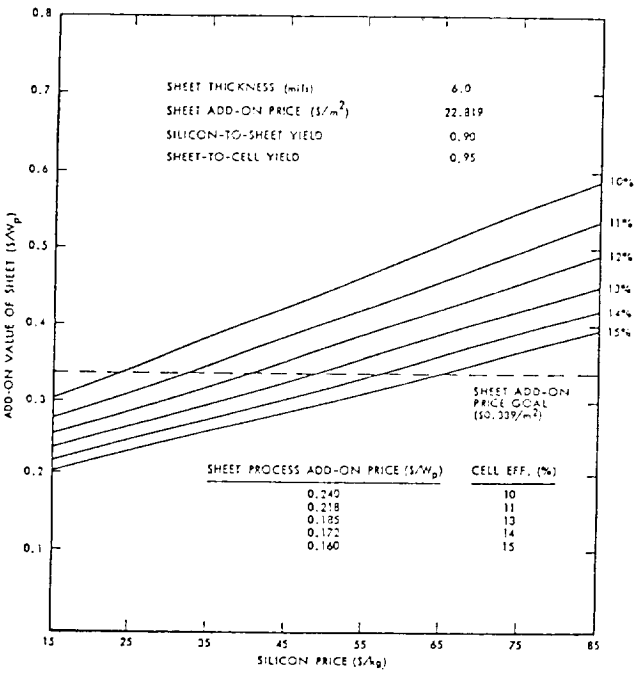

Figure A-2. Add-on Price Versus Silicon Price for Sheet Using Dendritic-Web Process for Sheet Thickness of 6 mils

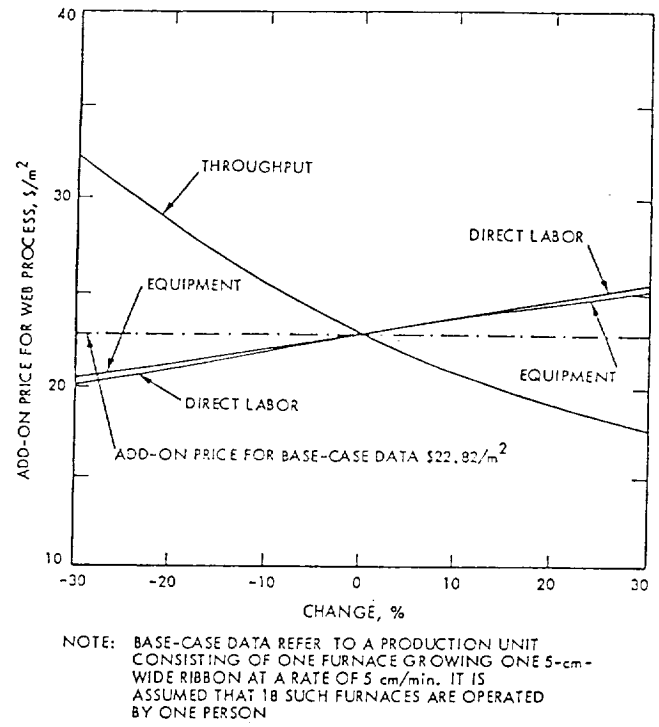

Figure A-3. Add-on Price Sensitivity to Throughput and Some Cost Parameters of the Dendritic-Web Ribbon Growth Process

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APPENDIX B

Workshop Summaries

I. WAFERING WORKSHOP, JUNE 1981

The ability of any ingot-based PV technology to compete in the future marketplace will depend upon the development of economical silicon- efficient wafering methods. The Low-Cost Solar Array Project at the Jet Propulsion Laboratory has supported the development of ingot wafering technology since 1975.

By the middle of 1980, it was clear that further technical breakthroughs in the wafering processes would be required to achieve the economic goals set by the LSA Project. As a first step toward giving the program new energy, a workshop on the wafering of silicon and related topics was planned.

The Workshop on ingot wafering was held on June 8-10, 1981, at the Pointe, Phoenix, Arizona, under the sponsorship of the Low-Cost Solar Array JPL Project. Objectives were to clarify and define the state of the art in silicon wafering, to solicit and explore innovative ideas in wafering, and to stimulate a productive exchange of technology within the slicing community. The approach was to hold an intensive Workshop with invited and submitted papers on the various aspects of ingot wafering, to invite acknowledged experts in the field who would lend perspective to the subject as well as their technical expertise, and to provide an atmosphere that would give ample opportunity for discussion.

More than 80 specialists representing five countries came to Phoenix to participate in an information-packed 3-day meeting. Often, for the first time, wafering empiricists were exposed to the theories underlying their wafering processes and theoreticians were given an accurate perspective of sawing as a business. Martin Wolf observed that the Workshop "fulfilled the task of bringing the diverse workers in the field to a common level of up-to-date information on all aspects of this area, making them aware of the accomplishments, the unknowns, and needs in setting the stage for further fruitful work as well as further information exchange." In fact, it seemed that everyone went home with new contacts and new ideas based on a better technical foundation. We saw new partnerships forming for research studies. We identified as important overlooked aspects of wafering technology for which R&D support is clearly needed. Based on the work presented at the conference and contained in these proceedings, we were able to understand better the potential of the technology.

The Workshop consisted of seven sessions covering all aspects of ingot wafering, including fixed- and free-abrasive sawing, wire, ID, and multiblade sawing, materials, mechanisms, characterization, innovative concepts, and economics. The Workshop Proceedings were published by the Project as JPL Publication 82-9, JPL Document 5101-187, Jet Propulsion Laboratory, Pasadena, California, February 1, 1982.

II. RESEARCH FORUM ON THE HIGH-SPEED GROWTH AND CHARACTERIZATION OF CRYSTALS FOR SOLAR CELLS, JULY 1983

The Research Forum on High-Speed Growth and Characterization of Crystals for Solar Cells was held at the Sandpiper Bay Hotel in Port St. Lucie, Florida, July 25-27, 1983. There were 68 participants, and 35 technical presentations

were made. Meeting attendance was broad-based, as evidenced by the source breakdown of papers: 16 from industrial laboratories, 13 from universities, and 6 from U.S. Government laboratories. The Forum was sponsored by the Flat-Plate Solar Array Project of the Jet Propulsion Laboratory.

The objectives of the Forum were to address theoretical and experimental phenomena, applications, characterization and all problem areas related to high-speed crystal growth, to define future areas of research, and to provide the opportunity for unrestricted technology exchange among those attending. The format used to achieve these objectives involved eight intensive sessions, consisting of four to five papers each, during the 3-day period. Time for each paper was equally divided between presentation and discussion periods. This format provided a successful exchange of ideas.

The Proceedings document (JPL Publication 84-23, JPL Document 5101-238, Jet Propulsion Laboratory, April 15, 1984) includes each speaker's manuscript and a transcript of the discussion period following each paper. Each of the manuscripts was printed, without changes, as received from the author.

III. WORKSHOP ON CRYSTAL GROWTH FOR HIGH-EFFICIENCY SILICON SOLAR CELLS

The Crystal Growth for High-Efficiency Silicon Solar Cells Workshop was held in San Diego, California, on December 3 and 4, 1984. Representatives from industrial laboratories, universities, and U.S. Government laboratories participated in the meeting and contributed to research planning activities. The Workshop was sponsored by the Flat-Plate Solar Array Project of the Jet Propulsion Laboratory.

The objectives of the Workshop were to define the requirements for silicon sheet suitable for processing into high-efficiency solar cells, to review the state of the art of silicon crystal growth technology (emphasizing the growth-related phonemena that limited device performance), and to identify the future research necessary to produce silicon sheet suitable for fabrication into high-efficiency solar cells. The schedule for this topical meeting divided each speaker's time equally between a formal presentation and a discussion period. In the final session, a panel of experts opened a general discussion of the future research activities necessary to achieve the growth of high-quality silicon crystals. The format for the meeting successfully provided the opportunity for unrestricted technology exchange among those attending.

This Proceedings document (JPL Publication 85-59, JPL Document 5101-272, Jet Propulsion Laboratory, August 15, 1985) includes speaker's presentation material and a transcript of the discussion period following each paper. A transcript of the entire panel and general discussion is also included.

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APPENDIX D

Acquisition of References

Most of the references used in this report fall into one of four generic types: (1) JPL published reports, (2) reports prepared for JPL by an outside contractor, (3) articles in the proceedings of professional meetings, and (4) articles in professional journals.

JPL PUBLISHED REPORTS

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APPENDIX E

Glossary

AGILE	Automatic Grower Logic
AM	air mass
AR	antireflective
ASEC	Applied Solar Energy Corp.
ASU	Arizona State University
CAST	capillary action shaping technique
CFH	crucible-free horizontal (ribbon growth)
CLF	continuous liquid feed
CNTD	Controlled Nucleation Thermal Deposition
CSI	Crystal Systems, Inc.
CVD	chemical vapor deposition
Cz	Czochralski
DARPA	Defense Advanced Research Projects Agency
DOE	U.S. Department of Energy
DTM	dendrite thickness monitor
EFG	edge-defined film-fed growth
EMC	Energy Materials Corp.
EPI	Eagle-Picher Industries
epi	epitaxial growth
EPRI	Electric Power Research Institute
ESP	edge-supported pulling
ESR	edge-stabilized ribbon
FAST	fixed-abrasive slicing technique
FF	fill factor (of I-V curve)
FSA	Flat-Plate Solar Array (Project)
FZ	float-zone, float zoning
GE	General Electric Company
HEM	heat exchange method
IBM	International Business Machines Corp.
ID	internal diameter
IPEG	Improved Price Estimation Guidelines
I-V	current-voltage
JPL	Jet Propulsion Laboratory
J_{sc}	short-circuit current density (mA/cm^2)
KBI	Kawecki-Berylco, Inc.
LASS	low-angle silicon sheet
L_D	minority carrier diffusion lengths
LPE	liquid-phase epitaxy
LY_p	lower yield point
MBS	multiple-blade slurry (sawing)
MIT	Massachusetts Institute of Technology
MOS	metal-oxide-semiconductor
MP_a	megapascals
MSEC	Mobil Solar Energy Corp.
MWS	multiple-wire slurry (sawing)
NASA	National Aeronautics and Space Administration
OCLI	Optical Coating Laboratory, Inc.
OCT	oscillating crucible technique
PECAN	Photovoltaic Energy Conversion Analysis (program)
PV	photovoltaic(s)
R&D	research and development
RF	radio frequency
RFP	Request for Proposal
RGA	residual gas analyzer
RS	resolved shear
RTR	ribbon-to-ribbon
SAMICS	Solar Array Manufacturing Industry Costing Standards
SCIM	Silicon Coating by Inverted Meniscus
SEM	scanning electron microscope
SERI	Solar Energy Research Institute
SIMS	secondary ion mass spectroscopy
SOC	silicon-on-ceramic
SRI	Stanford Research Institute International
STC	Silicon Technology Corp.
TD	technology development
TEM	transmission electron microscopy
TR	technology readiness
UCLA	University of California, Los Angeles
UCP	Ubiquitous Crystallization Process
UIC	University of Illinois at Chicago
UMG	upgraded metallurgical grade
UMR	University of Missouri-Rolla
V_{oc}	open-circuit voltage

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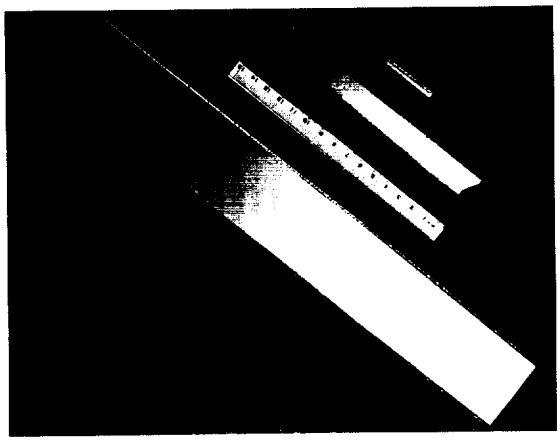
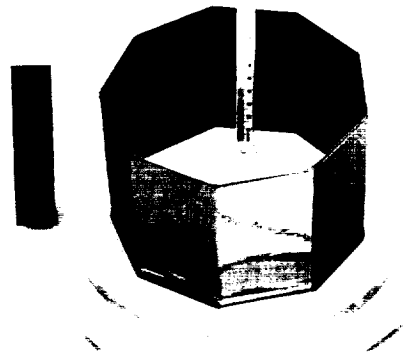
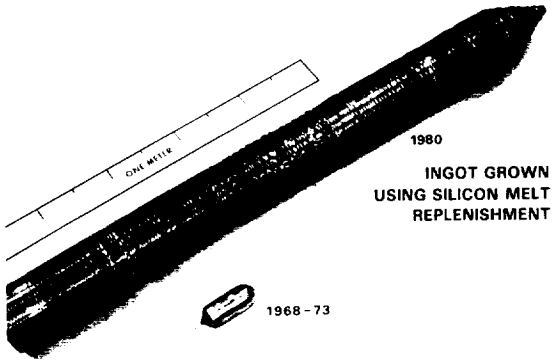
More Technology Advancements



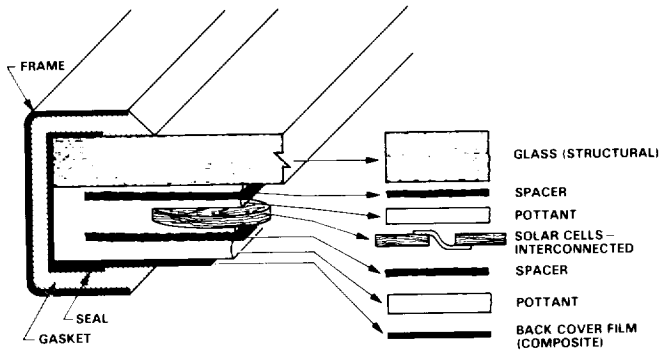
Dendritic web silicon ribbons are grown to solar-cell thickness. Progress is shown by experimental ribbons grown in 1976 and 1978 and a ribbon grown in a Westinghouse Electric Corporation pilot plant.



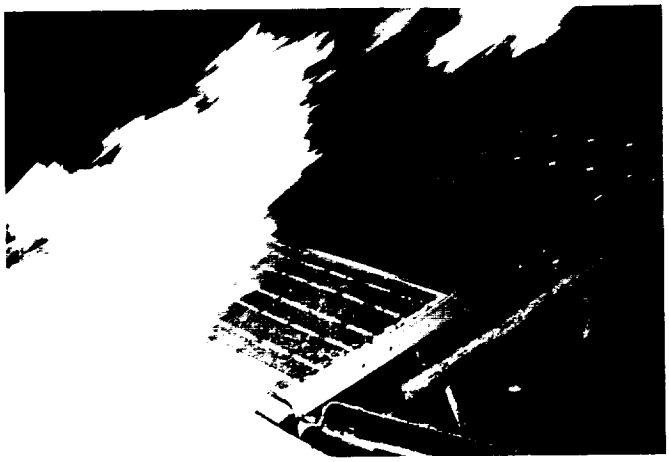
The edge-defined film-fed growth silicon ribbons are grown to solar-cell thickness. A DOE/FSA-sponsored research ribbon grown in 1976 is shown next to a nine-sided ribbon grown in a Mobil Solar Energy Corporation funded configuration.



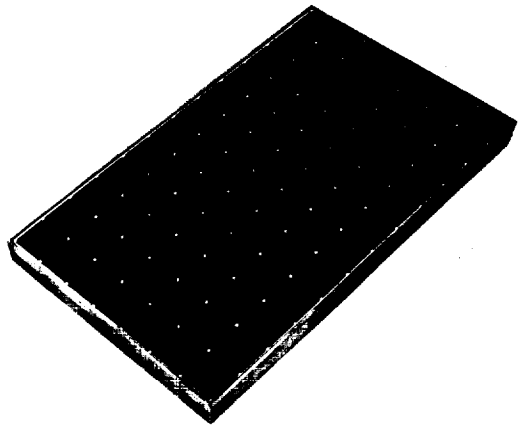
Czochralski silicon crystals as grown are sawed into thin circular wafers. (Support for this effort was completed in 1981.)



Typical superstrate module design is shown with the electrically interconnected solar cells embedded in a laminate that is structurally supported by glass. Materials and processes suitable for mass production have been developed using this laminated design.



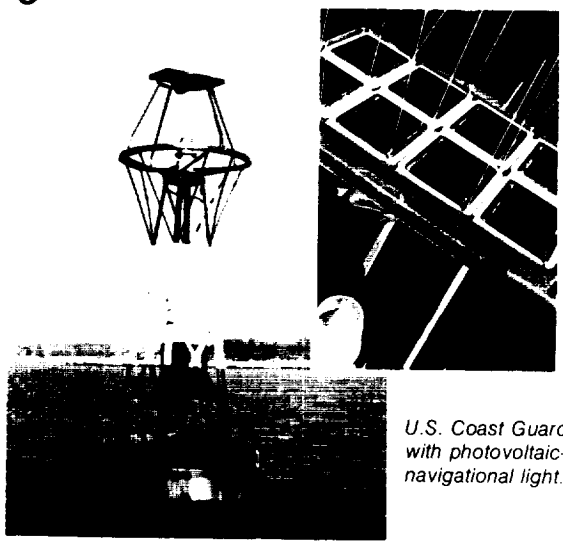
Prototype modules have passed UL 790 Class A burning brand tests which are more severe than this spread of flame test.



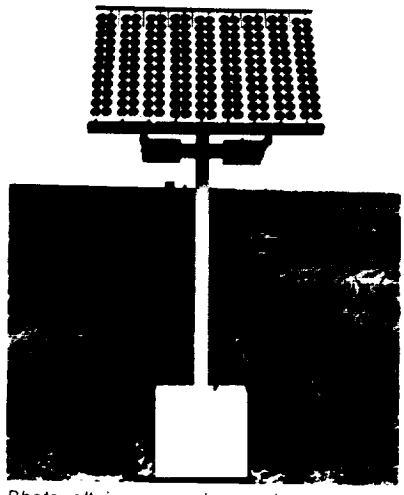
A 15.2% efficiency prototype module (21 x 36 in.) was made by Spire Corp. using float-zone silicon wafers. Recently, similarly efficient modules were fabricated from Czochralski silicon wafers.

Photovoltaic Applications

1975

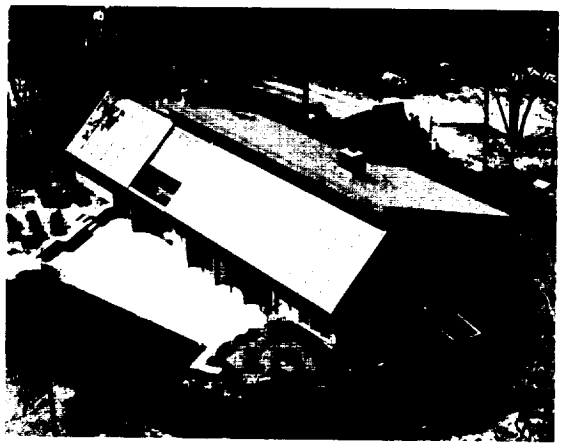


U.S. Coast Guard buoy with photovoltaic-powered navigational light.

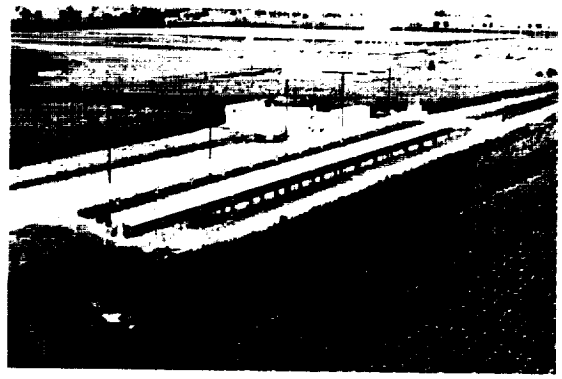


Photovoltaic-powered corrosion protection of underground pipes and wells.

Later...

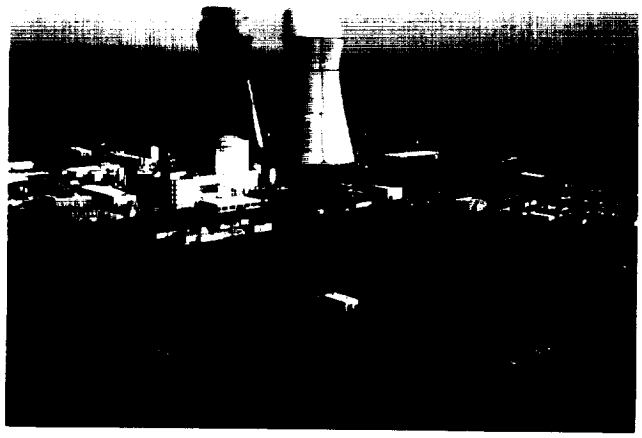


House in Carlisle, Massachusetts, with a 7.3-kW photovoltaic rooftop array. Excess photovoltaic-generated power is sold to the utility. Power is automatically supplied by the utility as needed.



A 28-kW array of solar cells for crop irrigation during summer, and crop drying during winter (a DOE/University of Nebraska cooperative project).

1985



1.2 MW of photovoltaic peaking-power generation capacity for the Sacramento Municipal Utility District. (The 8 x 16 ft panels are mounted on a north-south axis for tracking the sun.)