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FINAL TECHNICAL REPORT

Continuation of D.C. Partial Discharge Testing and Circuit Research Studies

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Table of Contents

		Page
i	Acknowledgments	1
ii	Abstract	3
1.	Description of Work Performed	4
2.	Integrated Circuit Pulse-width-Modulators	5
3.	Power FETs	12
4.	Active Filters	19

Appendices

1.	Analysis of some interesting active filters	A1
	a. Non Inverting VCVS	A1
	b. Infinite Gain Multiple Feedback Circuit	A3
	c. State Variable Filter	A5
	d. Bi Quad Active Filter	A10
2.	Circuit Diagram for Tuned Circuit Studies	A13
3.	Ramp Generator Circuit	A14

Abstract

In this report, additional information on tuned circuit studies is given, as well as a treatment of the integrated circuit pulse width modulator and a study of the power FET. In addition, work on active filters is described, and a ramp generator circuit of potential interest in partial discharge studies is given.

Description of Work Performed

The partial discharge work has been described in earlier reports and thus will not be treated here.

Theory related to tuned circuits studies was given in an earlier report. The circuit receiving most experimental attention is given in the Appendix.

A description of work on the integrated circuit pulse width modulator is included, along with some experimental data.

A chapter on Power FETs, as mentioned in the January 31, 1983 report, is included here.

Studies on active filters are presented, in which the longer term purpose is to analyze and measure low noise active circuit configurations, filters and amplifiers of particular interest in the 1 hz to 1 khz frequency region.

Experimental work was performed on the use of operational amplifier curcuitry for the development of high voltage power supplies. The aim here was to use them to generate accurate range voltages which would drive programmable power supplies. The circuitry employed is given in an appendix.

Pulse Width Modulated Switching Regulator

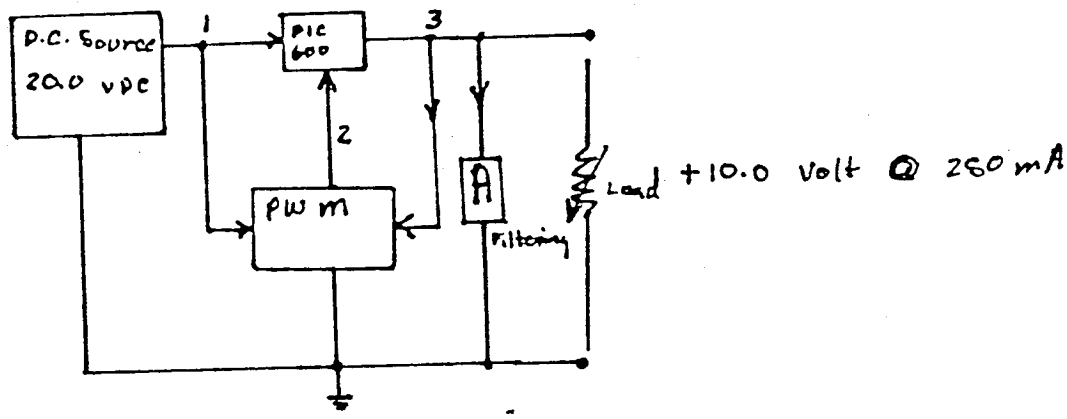
Technical Description

The Pulse Width Modulated Switching Regulator circuit is implemented from a SG 1524 Pulse Width Modulator and a PIC 600 Switching regulator. The SG 1524 is a monolithic 16 pin I.C. fabricated in a dip package and contains a voltage reference, error amplifier, osillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches, current limiting and shut down circuitry. The SG 1524 is designed to Military Specs. for temperature operation ($-55^{o}c$- $+125^{o}c$). The PIC 600 is a four pin I.C. switching regulator implimented using a clamped Darlington configuration for higher gain and reduced drive requirements.

The circuit is constructed using wire wrap techniques and dip headers, for quick and easy testing and replacement of parts and modifications. A 20 volt d.c. source powers the P.W.M.S.R. and can deliver an output current up to 250 mA at 10.0 vdc before current limiting.

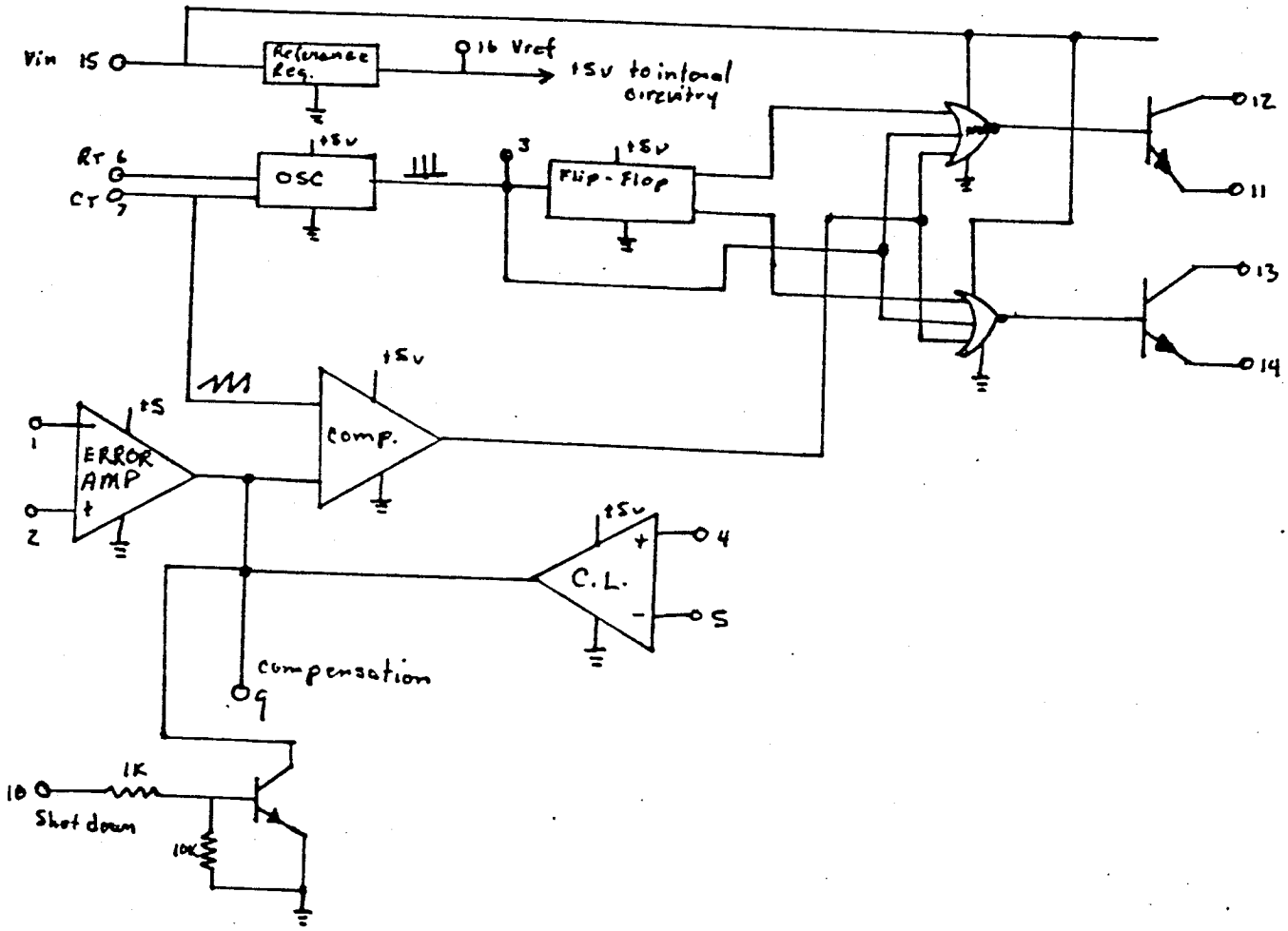
Theory of Operation

The Pulse Width Modulated Switching Regulator is somewhat analogous to almost any typical closed loop series regulating system. The PIC 600 controls the output voltage and the SG 1524 senses voltage variation in the output voltage and applies corrective pulses to the PIC 600 to maintain a constant output voltage over a wide range of load conditions at a greater efficiency than coventional regulators. A block diagram of the P.W.M.S.R. is shown on the next page.



The 20.0 volt Source Powers the pulse width modulator which applies a pulse to the PIC 600 series switching regulator. An output voltage is developed across point 3 and the filtering network (A) smoothes the ripple and stores up a charge. The pulse width modulator then senses the voltage level at point 3 and when it approaches a defined level (10.0 volts) the pulse is removed and the output voltage is maintained by the charge stored by the filtering network. As the charge stored by the filtering network drops off, the P.W.M. senses the reduced output voltage and applies another pulse to the PIC 600 to replenish the charge on the filter network and to maintain the desired output voltage. The duration of the pulse is a function of the filter network and the load current.

BLOCK Diagram P.W.M.



A block diagram of the P.W.M. is shown on the preceeding page. By referring to the diagram we will attempt to give a functional explanation of how the P.W.M. works. The oscillator supplies a pulse train to the steering flip-flops and a ramp signal to the comparator. The ramp signal acts as a reference for the comparator and the pulse train simply clocks the flip-flops and acts as a strobesignal or blanking pulse to ensure that only one transistor is turned on at any instant.

A reference voltage is applied to the noninverting input of the error amplifier and the feedback voltage is applied to the inverting input of the error amplifier. The difference between the feedback voltage and the reference voltage is applied to the comparator along with the reference ramp signal. If there is no error a nullsignal from the error amplifier is compared to the ramp signal and the output of the comparator saturates at +5 volt, thus driving both NOR gates low and both transistors off.

The pulse train also works as a blanking pulse that inhibits the NOR gates while the flip-flops change states. If an error is sensed at the error amplifier, the output of the error amplifer is driven high and compared with the ramp signal. The output of the comparator will be driven low and NOR-ed with the flip-flops and the pulse train. The state of the flip-flops determines which transistor will be turned on and only for the duration of time between the pulses of the pulse train. Therefore a transistor is turned on only when the error

amplifier sends an error, forces the comparator output low, and the pulse train is in a low state. The steering flip-flop low output determines which NOR to enable and thus turns on the transistor it drives. This in turn drives the PIC 600, which replenishes the charge on the filter network and regulation is achieved. Our circuit operates in the single ended mode with the two output transistors of the SG 1524 connected in parrallel.

Testing and Modification

Modifications: The original circuit was taken from the Silicon General Product Catalog 1979, page 23. It was initially designed to operate from a 28 volt source, with an output voltage of +5 UDC. It also used a PIC 600. The low operating voltage of 5 volts gave rise to stability problems, and so was modified to operate from a 20 UDC source and to deliver 10 VDC at 250 mA to the output before current limiting.

To achieve our 10 volt output we double the amount of negative feedback applied to the error amplifer by changing the 5K feedback resistor to a 2.5K resistor. We also change the current sensing resistor of the current limiter to 0.5Ω to limit our current at 250 mA. These changes allow this circuit to operate at around 13 volts by reducing the base resistor supplying the drive current to the PIC 608.

Load regulation tests have been completed and plans for testing line regulation, temperature stability, common mode voltage ratios, duty cycle, saturation voltage, rise time, fall time, and response characteristics were completed.

Test results on most regulation appear below. Work has also been done on line regulation, common mode voltage ratio , duty cycle, saturation voltage, rise time, fall time, and response characteristics.

Regulating Pulse Width Modulating Regulator

LOAD REGULATION TEST

V_{in} = 20.0 VDC

R LOAD	V out		I out		I in	
Open Circuit	10.0	V			23.0	mA
450 Ω	10.0	V	22.3	mA	23.0	mA
400 Ω	10.0	V	25.0	mA	25.0	mA
350 Ω	10.0	V	29.0	mA	27.0	mA
300 Ω	10.0	V	33.5	mA	30.0	mA
250 Ω	10.0	V	40.0	mA	34.00	mA
200 Ω	10.0	V	50.0	mA	40.0	mA
150 Ω	10.0	V	65.0	mA	49.0	mA
100 Ω	10.0	V	100.0	mA	68.0	mA
50 Ω	9.99	V	198.0	mA	129.0	mA
40 Ω	9.98	V	245.0	mA	149.0	mA
30 Ω	9.90	V	998.0	mA	188.0	mA
20 Ω	8.16	V	1.20	A	6000	mA
15 Ω				mA		mA
10 Ω	3.98	V	1.24	A	115.0	mA
short circuit 0 Ω	0.17	V	1.34	A	33.0	mA

Some associated problems that were encountered during the construction and familiarization period are switching noise, accidental shorts, isolation, shielding, and instability. Some of these problem have been reduced by using better insulation, shielding, eliminating ground loops, and isolating wire wrap pins.

POWER FETS

Introduction

Since the introduction of power MOSFETs some years ago, a number of important improvements have been made. The applications of these devices have centered around microwave amplifiers, high voltage switching and high speed logic. Most of these devices are fabricated by double diffusion through the same mask window, similar to bipolar processing to achieve short channel lengths. Because of this short channel length, the power MOSFET is capable of extremely high gains at microwave frequencies with standard mask alignment. This report will discuss a number of items of particular interest to GSFC.

MOSFET Structure

A variety of structures for implementing a power MOSFET have been proposed and fabricated. Of these, only two structures, the flat bottom V-groove (VMOS) and the vertical D MOS (VDMOS) structures are currently available as power switches. A cross-sectional view of V groove is shown in Figure 1, while the cross-sectional view of VDMOS is shown in Figure 2.

VDMOS devices are very similar to V-groove devices except that no groove is used, and the gate structure is planar. Manufactures have given the VDMOS devices a variety of names, such as HEXFET, IMOS, XMOS, ZMOS, etc. These are all basically the same structure,

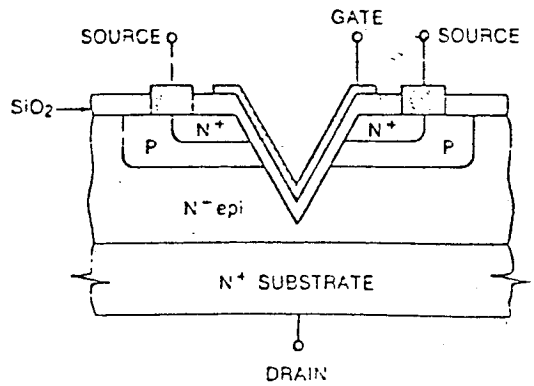


Figure 1 V-groove structure

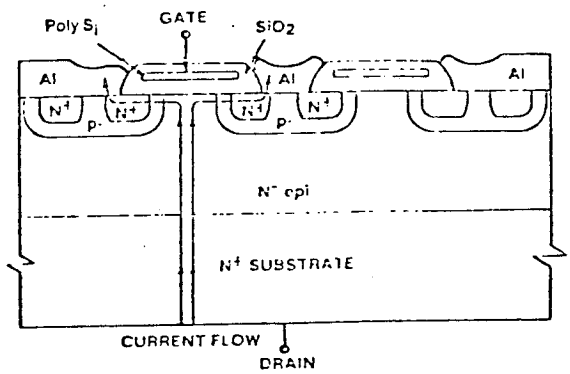


Figure 2 Vertical DMOS transistor

with variations in the shape of the P diffusions and the cell interconnections.

Drawbacks of VMOS

1. The sharp bottom of the V-groove produces a strong field concentration between the gate and the drain.

2. There is a tendency for the oxide layer to thin out around the tip of the V. The result of this is limited high voltage capability due to gate-oxide breakdown even though the gate does not see the full drain source voltage.

3. The use of an aluminum gate can cause long term reliability problems due to ion migration (principally sodium) through the gate oxide layers, which leads to variations in the device threshold voltage.

4. A channel is formed on each side of the V-groove. If the groove does not extend past the P region into the epi-layers, it is possible to experience excessive current densities which may cause injected avalanche breakdown in high power devices.

AVMOS alleviates these problems

Advantages of VDMOS over BJT s

1. They have extremely high input impedance, because of the low input drive current to the gate.

2. There is no prob lem of current hogging. If the current density at a particular location or channel region between the source and drain increases above that of other channel regions , the temperature at this point rises. The resulting reduced carrier mobility then tends to decrease the current, and so the current density throughout

the channel tends to equalize. In the case of bipolars, however the positive temperature coefficient of the collecter current gives serious current hogging.

3. Second breakdown and thermal runaway can occur in power BJT's from localized heating and hot spots. No such problems are encountered with FET's, which are thus much more rugged.

4. Class B power amplifiers using bipolar transistors require emitter resistors of about 0.3 ohms. FET devices in similar service do not need source resistors.

5. FET devices have no charge storage problems, and thus power switching can occur at much faster rates in FET's than in bipolar transistors.

6. For high power levels it is possible to parallel FET devices. This is considerably more difficult with bipolars. The parallel switches must share current equally, not only during the conduction interval but also while switching. In the case of bipolar transistors, a large number of parameters must be matched, which is usually not practicable.

7. For higher voltages devices may be connected in series. This is a reasonable procedure for MOSFET's if the stray capacitance is kept uniform within the string and the gate devices are identical. At 200 khz, the dynamic problems of seriesing bipolars are almost insoluble, so that series bipolar switches above 100 khz are not used.

8. The stability of the gain and response time characteristics over a wide range of temperatures is outstanding.

9. The extremely low current drive requirements of the power MOSFET, and the associated extremely high power gain, are another advantage over the conventional bipolar transistor or Darlington. This feature often makes it possible to drive power MOSFETs directly fr CMOS or TTL integrated circuit logic.

Parallel and Series Operations of VDMOS Transistors

The current capacity of power FETs is easily increased by connecting several devices in parallel. For example, if a VDMOS transistor has a maximum allowable current of 4A, three of these in parallel will give a current capacity of 12A. This is done by connecting the three drain terminals to form a single drain terminal, and similarly for the gates and source terminals. The transconductance of the composite device is the sum of the parallel individual transconductance and the incremental drain resistance is the parallel equivalent of the individual drain resistances.

No ballasting resistors or thermal matching networks are needed because, as already noted, the currents tend to equalize if a particular device starts to draw more current than it otherwise would. As an example an initial imbalance of 20% (a typical worst case figure) will reduce to 14% if the junction temperatures approach their maximum limits. Because of the high frequency responce of MOSFETs, small valued resistors ($\sim 100\Omega$ to $1k\Omega$)

in series with each gate are necessary to suppress spurious high frequency (~300 Mhz) oscillations.

A series switching circuit with a supply voltage of 100 volts is shown below. Each of these two transistors has a breakdown voltage of about 60 volts. For a VMOS device to enter breakdown there must be a drain current in the circuit. This is possible only if both transistors conduct. Therefore with the switch off the supply voltage is divided so neither transistor is in breakdown. The resistors R1 and R2 are larger because the drive current to the gate of Q2 is small. C1 and C2 form a capacitive divider which dynamically balances the gate drive and also insures fast switching the ratio C1:C2 should be approximately R2:R1, with allowance for stray capacitance and the enhancement of Q2. The 15 volt of the bottom of the string has the purpose of providing adequate positive voltage for Vgs2 when the switch is on. Proper selection of R's and C's allows any number of VMOS devices to be connected in series.

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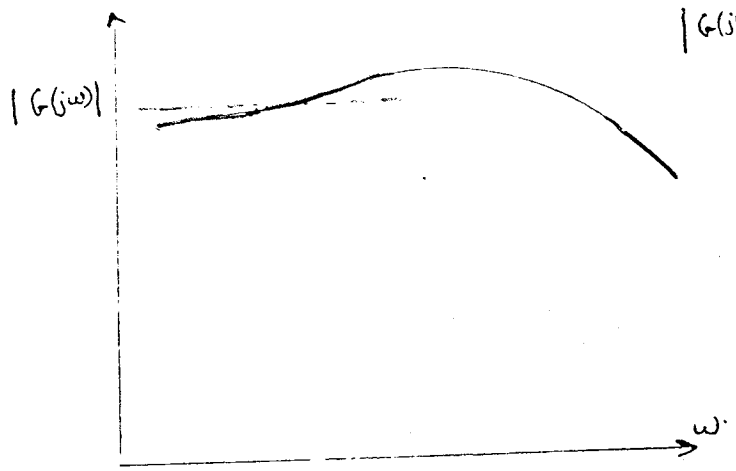
Active Filters

As noted earlier Goddard Space Flight Center (GSFC) is interested in active filters for low noise, low frequency circuit configurations. The Sallen-Key non-inverting voltage controlled voltage source (NIVCVS) and the multifeedback network (MFN) are of particular interest. In addition, other approaches such as the state variable and the biquadratic active filters were investigated for more general applications. Derivations of their transfer functions are given in an appendix of this report and a list of useful references (some mentioned in the text of this chapter) appear at the end of this chapter.

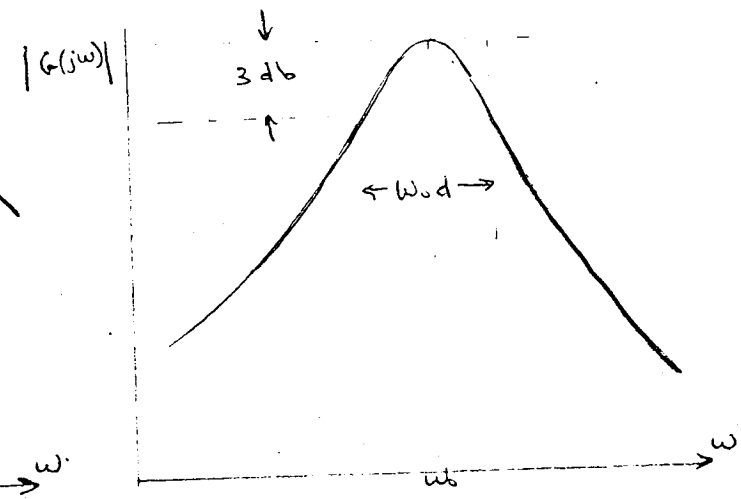
In general, a useful design emphasizes structures which minimize the number of passive elements, particularly capacitors, for a given order transfer function. Synthesis of second order transfer functions of standard form for low-pass (LP), band-pass (BP) and high-pass (HP) cases, to alleviate pole sensitivity position, is usually desired. Higher order transfer functions, necessary for, say, maximally flat (Butterworth) or other desired behavior, are achieved by cascading first and second order sections. When outputs are taken from voltage controlled sources, isolation between the sections is unnecessary. All the configurations studied here have this isolation property.

We begin by noting some general properties, fundamental considerations, equivalent notations and points of view used in active filter literature.

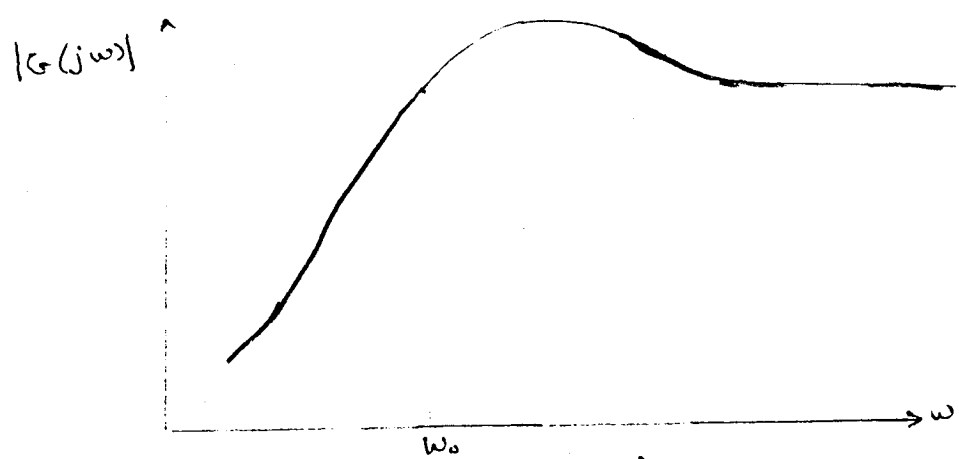
Second order active networks have frequency response characteristics for the low-pass, band-pass, and high-pass cases as shown below, where the notation is that of Sallen-Key (and radial frequency-normalized gain response is used).



L.P. $G(s) = \dfrac{1}{s^2 + ds + 1}$



B.P. $G(s) = \dfrac{s}{s^2 + ds + 1}$



H.P. $G(s) = \dfrac{s^2}{s^2 + ds + 1}$

Low Pass Case

Some other notations for the second order transfer function L.P. case are

$$H(s) = \frac{H_0 \omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}$$

$$A_v(s) = \frac{A_0}{s^2 + 2\zeta\omega_0 s + \omega_0^2}$$

$$H(s) = \frac{H_0 \omega_0^2}{s^2 + \alpha\omega_0 s + \omega_0^2} \quad *$$

(and thus the D.C. gain is H_0)

It is clear that the connection relations are

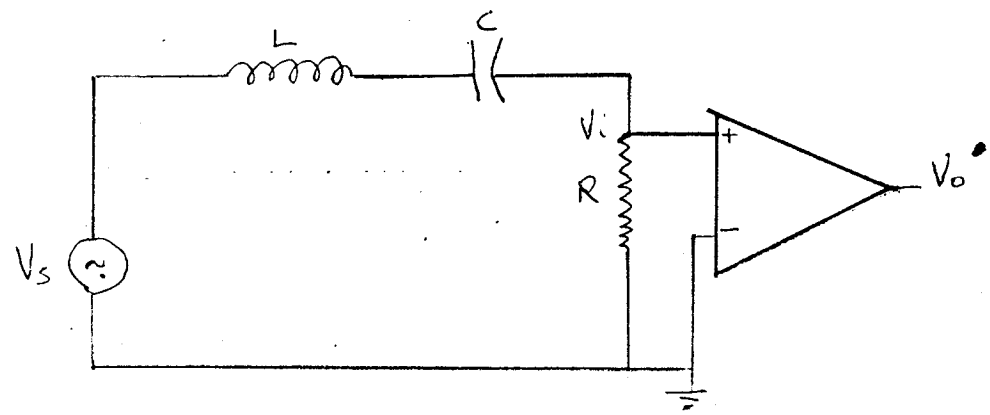
$$Q = \frac{1}{2\zeta} = \frac{1}{\alpha}$$

It is worth noting that the increase in response with frequency occurs only for $\alpha < 1.414$ or $\zeta \doteq 0.707$ (the value for the second order maximally flat filter).

*These forms are given in Graeme, Tobey, and Huelsman p.286 and Stout and Kaufman p.104.

Band Pass Case

Consider the active resonant band-pass filter, as given by *



If one defines the quantities

(1) (1) $$\omega_0^2 = \frac{1}{LC}, \quad Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC}$$

$$\left(\text{whence } \frac{L}{R} = \frac{Q}{\omega_0}\right)$$

(2) (2) $$A_V \equiv \frac{V_o}{V_s},$$

$$A_V = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s} = A_o \frac{R}{R + j\left(\omega L - \frac{1}{\omega C}\right)}$$

(3) $$= \frac{A_o}{1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)}$$

and if we write $s = j\omega$,

*Millman, p. 588

we get

$$(4) \qquad A_v(s) = \frac{R}{L} \frac{A_o s}{s^2 + s\frac{R}{L} + \frac{1}{LC}} = \frac{\omega_o}{Q} \frac{A_o s}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}$$

by relation (1)

It is easy to show* that if f_1 and f_2 are the 3db gain drop off frequencies, and the band width B is defined as $B = f_2 - f_1$ then

$$B = \frac{f_o}{Q}$$

Also, f_1 and f_2 have the geometric mean property $f_o^2 = f_1 f_2$ and thus will have symmetry about f_o on a logarithmic plot.

Noting that $\alpha = \frac{1}{Q_o}$ we get the alternative form for equation (4)

$$(5) \qquad H(s) = \frac{H_o \alpha \omega_o s}{s^2 + \alpha \omega_o s + \omega_o^2}$$

*Millman, p.588

Experimental Results

As has already been mentioned in this report the behavior and low noise properties of the non-inverting VCVS circuit, and the multi-feedback network (MFN) were of particular interest to GSFC, and therefore magnitude and phase measurements of the sort usually given in bode plots were carried out. The two circuits, and the component values used, are given below.

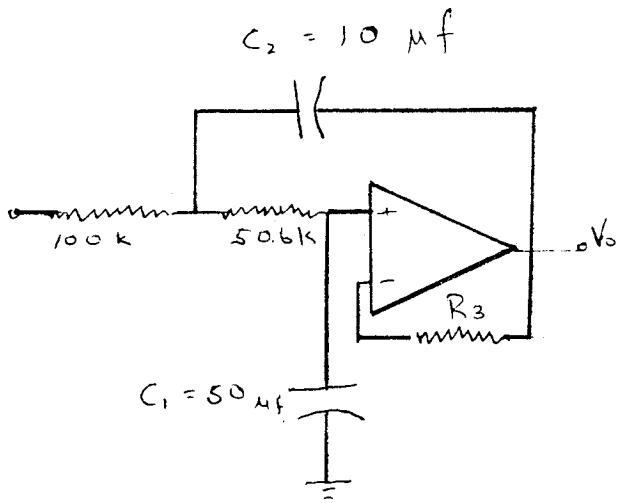


Fig 1 : NIVCVS

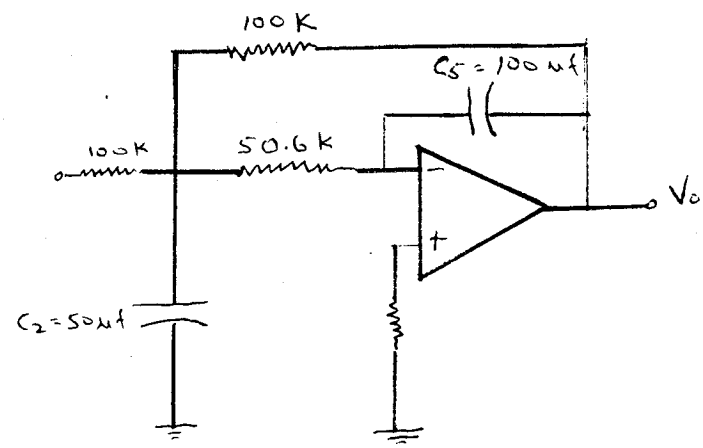


Fig 2 : MFN

Properties of Fig 1: (NIVCVS)

We can ignore R3 in fig 1, since in the ideal op-amp no current flows through it, and thus $V_o = V^-$. If we make use of the transfer function for fig 1 which is given in the appendix on page A2 we find that

$$f_o = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} = 0.100 \text{ Hz}.$$

$$\zeta = \left(\frac{C_1}{C_2}\right)^{1/2} \frac{(R_1 + R_2)}{2\sqrt{R_1 R_2}} = 2.37$$

and the DC gain is 1,

for R1 = 100K, R2 = 50.6K. C1 = 50μf, and

C2 = 10μf.

For this network, the poles are the roots of the denominator of

$$\frac{\omega_0^2}{S^2 + 2\zeta\omega_0 S + \omega_0^2} = \frac{(0.628)^2}{S^2 + 2 \times 2.37 \times 0.628 + (0.628)^2}$$

$$= \frac{0.395}{S^2 + 2.98\,S + 0.395}$$

with roots S = -0.171, and -2.31

A plot of the frequency dependence is given in Fig. 3 on the next page. Further measurements were made for approximately the same 5:1 ratios of C_1:C_2, where C_1 = 4.6 and C_2 = 1.0, C = 0.46 and 0.1, C = 0.05 and 0.01 (all in microfarads), and thus the "cut-off" frequency is successively increased by factors of 10 while keeping the same damping ratio ζ. In all cases the plots showed the second order low pass behavior (i.e. 40 db/decade) satisfactorily.

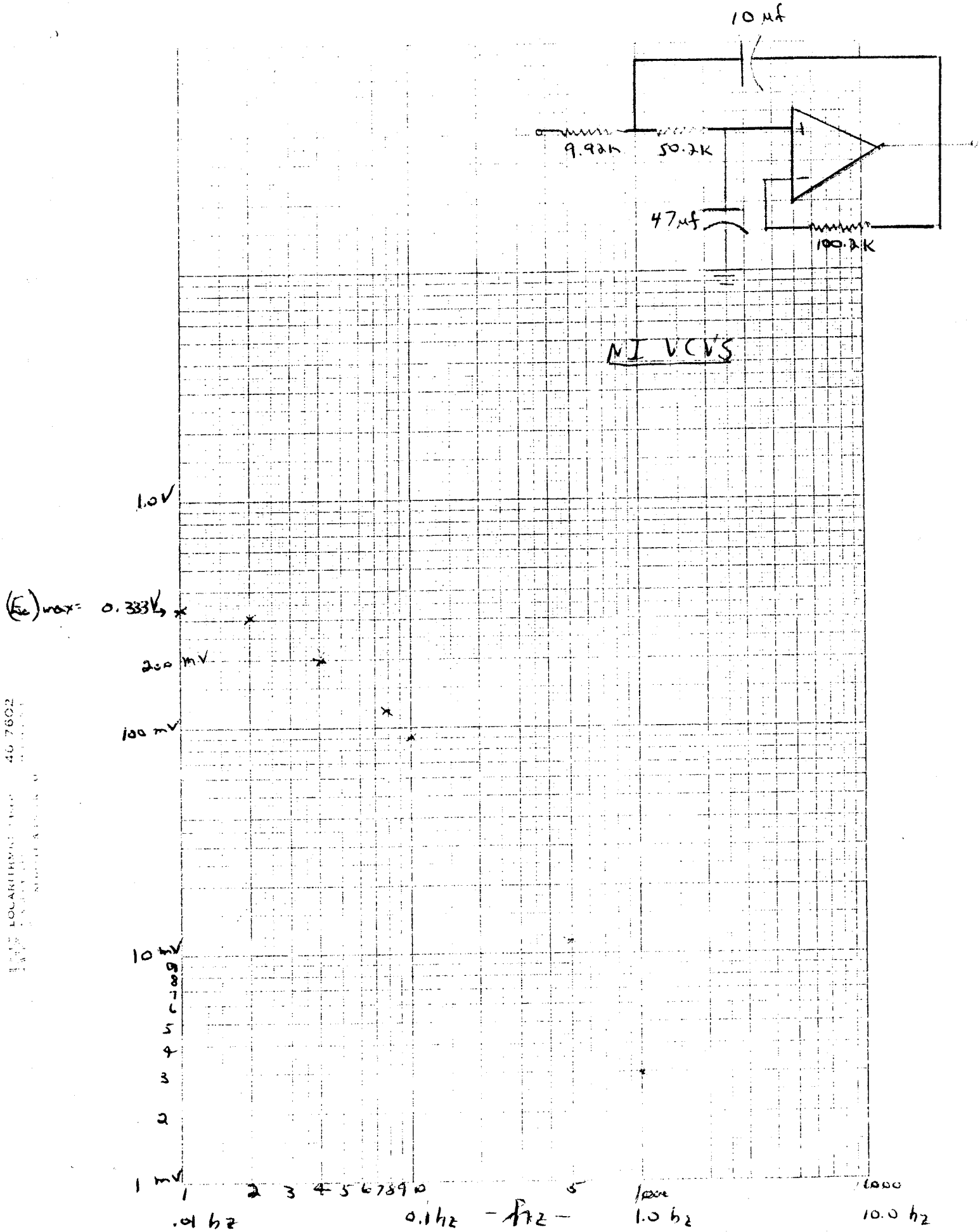

10 µf
9.92K
50.2K
47µf
100.2K
NI VCVS
1.0V
(Ec) max = 0.333V
200 mV
100 mV
10 mV
1 mV
.01 hz
0.1 hz
1.0 hz
10.0 hz
1000

Figure 3

Properties of Fig 2: (MFN)

If we now use the transfer function for fig A2, given on page A4 of the appendix, we find that

$$f_o = \frac{1}{2\pi\sqrt{R_3 R_4 C_2 C_5}} = 0.100 \text{ hz}$$

$$\zeta = \frac{1}{2}\left(\frac{C_5}{C_2}\right)^{1/2}\left[\frac{\sqrt{R_3 R_4}}{R_1} + \sqrt{\frac{R_4}{R_3}} + \sqrt{\frac{R_3}{R_4}}\right] = 0.634$$

and Gain (DC) $= -\frac{R_4}{R_1} = -1$

for R1 = 100K, R3 = 50.6K, R4 = 100K, C2 = 50 μf and C5 = 10 μf.

In this case the transfer function becomes

$$-\frac{0.395}{S^2 + 0.796S + 0.395},$$

with poles at $-0.40 \pm 0.98j$.

A plot of the data for C_1 = 47 μf, C_2 = 10 μf and for C_1 = 4.7 μf, C_2 = 1.0 μf is shown in Fig 4 for this circuit. In both cases the expected second order low pass fall off, at the correct f_o, is shown. Similar agreement was obtained for smaller capacitors with the same 4.7 : 1 ratio at cut-off frequencies (f_o) out to 1 khz. Also, the expected phase lag behavior (0 to near 180° with increasing frequency) for this second order low pass transfer function was observed, when the input and output waveforms were displayed on a dual-trace scope.

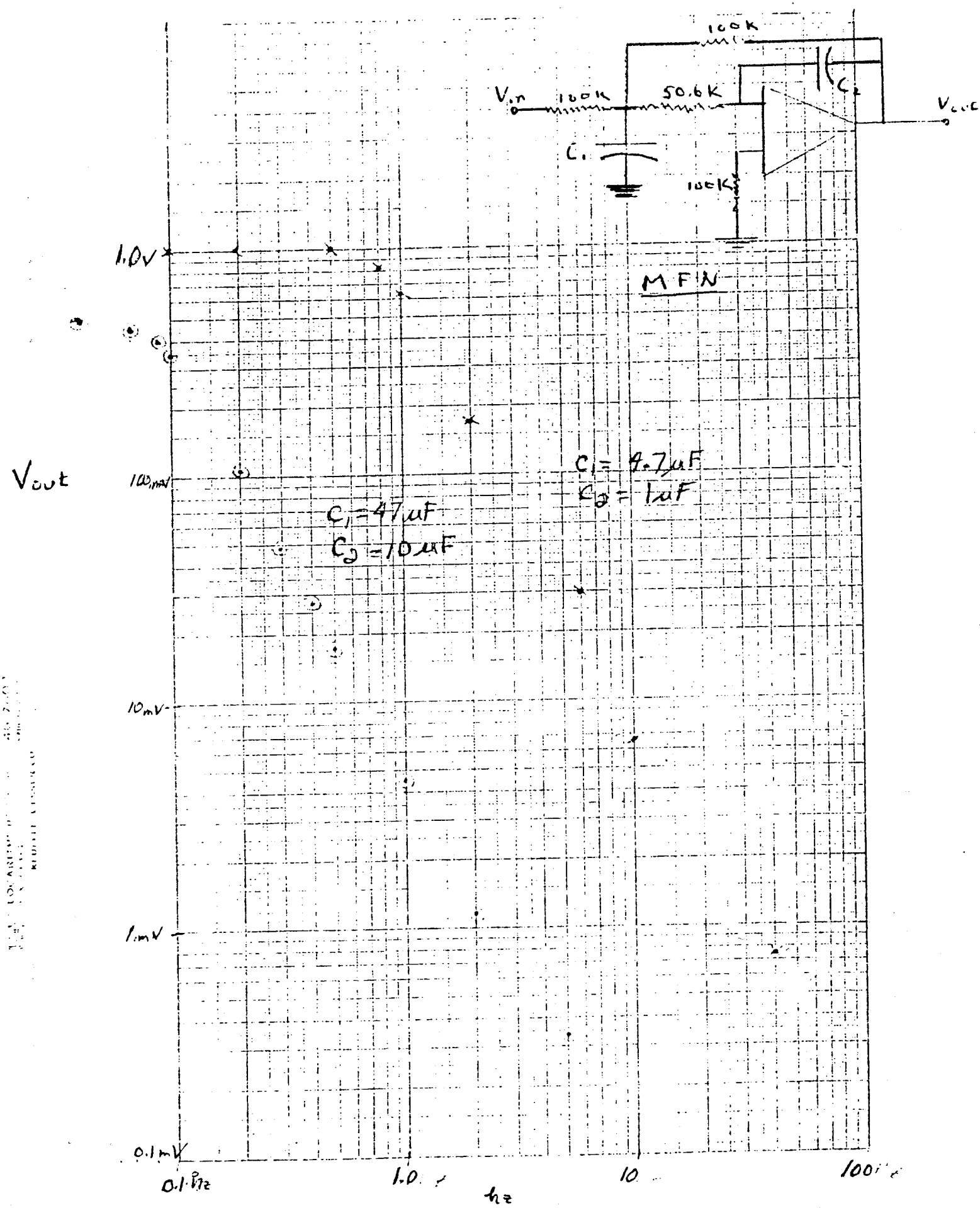

100K
V_{in}
100K
50.6K
C_2
V_{out}
C_1
100K
MFN
1.0V
V_{out}
100mV
$C_1 = 4.7\mu F$
$C_2 = 1\mu F$
$C_1 = 47\mu F$
$C_2 = 10\mu F$
10mV
1mV
0.1mV
0.1 Hz
1.0
10
100
hz

Figure 4

Because of GSFC's interest in low noise ($\sim \frac{20nV}{\sqrt{hz}}$ spectral density) low frequency ($\sim$ 1hz to 1khz) active circuit configurations, attempts were made to simulate noise associated with the outside feedback resistor (ie R_4 of Figure A2) by injecting a coherent signal into this arm with a transformer. These were not successful at the low frequencies of interest ($\sim$ 0.1 to 1 hz), presumably because of difficulties with the transformer response used at these frequencies. The effect of the active filter circuit on Johnson and other noise generated in this circuit could probably be more successfully simulated at higher frequencies, and the result extrapolated downward in frequency.

The State Variable - Bi Quadratic Active Filter

These filters, whose analysis appears in the appendix, involve more active and passive elements thor the VCVS and the MEN types.* Our particular second order state variable filter has separate terminals for low pass hard pass and high-pass outputs, but more importantly the cut-off or resonant frequency is independently adjustable from the circuit and the D.C. gain. Thus it is much easier to adjust and is much more stable. The extra parameters allow the achievement of other properties such as the possibility of having a constant bandwidth over a range of frequencies.

*It should be noted that the terms state variable and biquadratic are used somewhat interchangeably in the literature. We use Van Dolsen's nomenclature.

R_{POT} 10K Ω

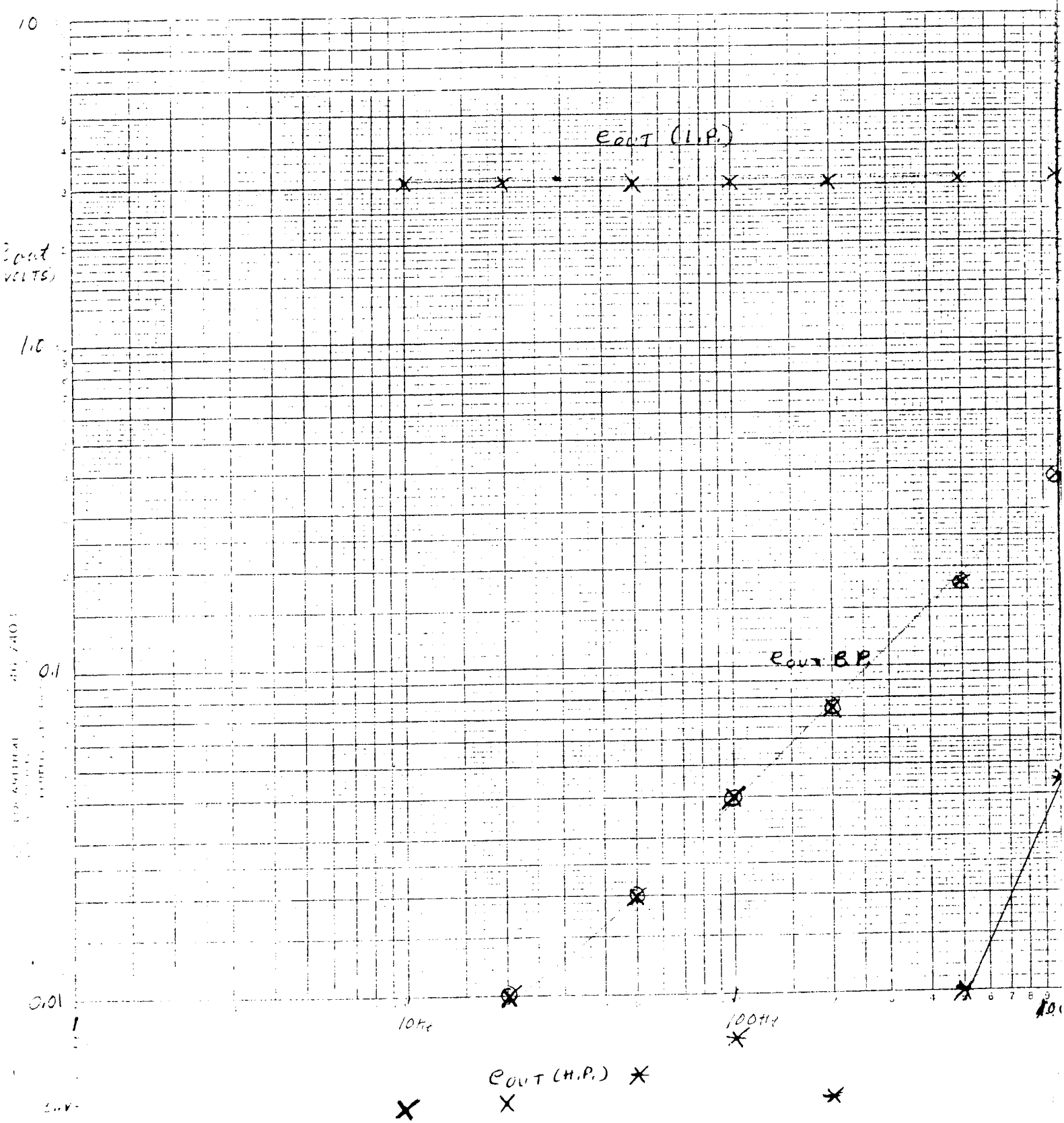


Figure 5

State Variable Filter

Measurements were made on the state variable filter circuit shown in Fig A3, with component values R = 10K, R_F = 1.6K, R_g = 10K and C = 0.01 μf. R_d was given the 2 values of 2k and 10k.

For these values

$$\omega_0 = \frac{1}{2\pi R_F C} = 9.95 \text{ Khz}$$

and α is 0.25 and 0.8 .

The data for the low-pass, band pass and high pass cases are plotted in Figures 5,6, and 7. As expected, all the plots show a rise in the vicinity of 10khz (since for both cases, the damping ratio ζ is less that 0.707). Further the data is found to be insensitive to the value of ζ except in a range of about $\pm$ 5khz around 10khz. Thus the rather marked peaking at resonance for all three frequency outputs (LD,BP,HP) is shown as ζ (= $\frac{\alpha}{2}$) decreases from 0.4 to 0.125.

STATE VARIABLE USING
741 OP AMPS

$R_{POT} = 10K\Omega$

$e_{in} = 3.10 V_{p-p}$

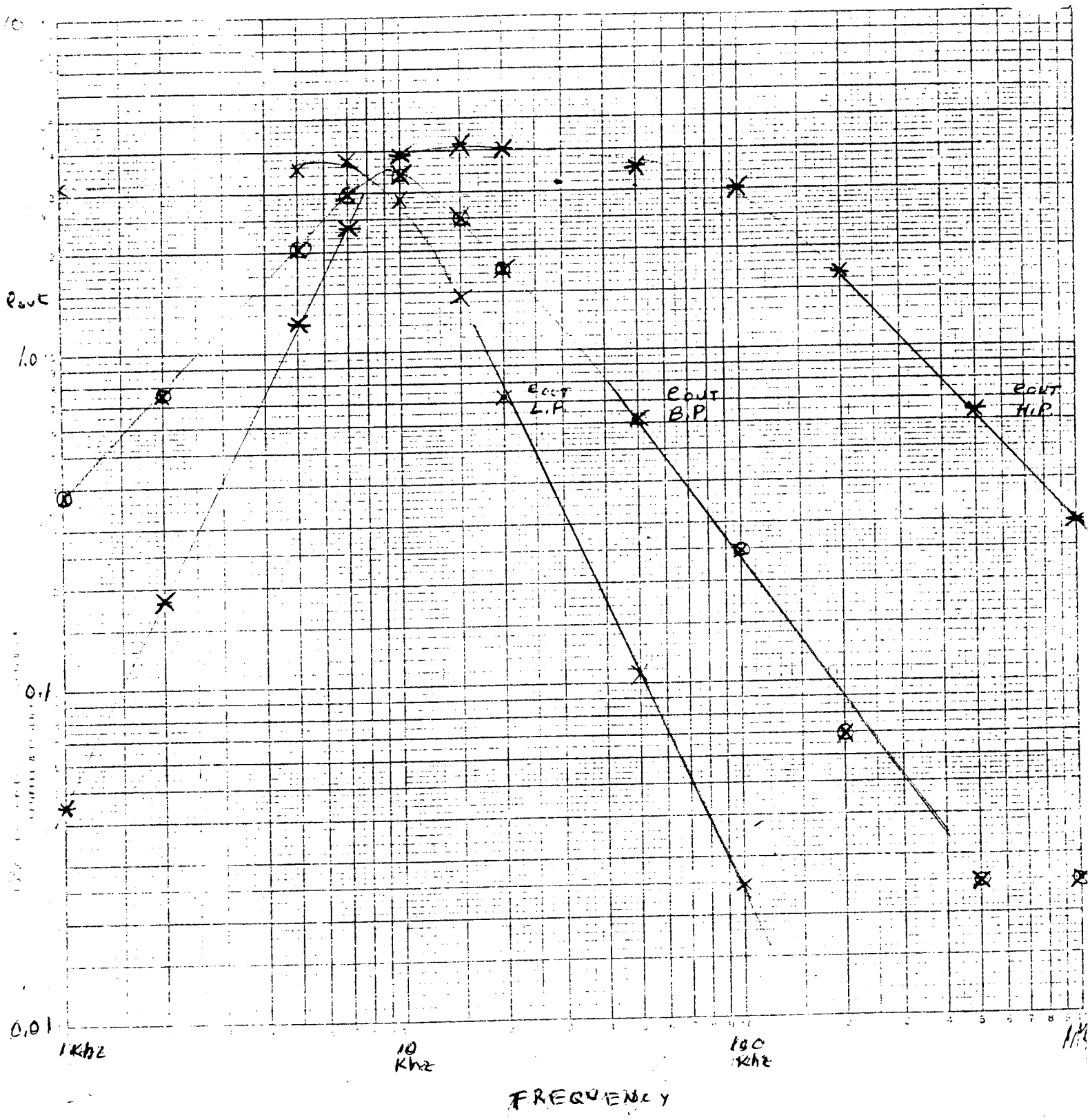


Figure 6

REGION WHERE R_{POT} AFFECT E_{OUT} VALUES
- STATE VARIABLE, VARIABLE GAIN

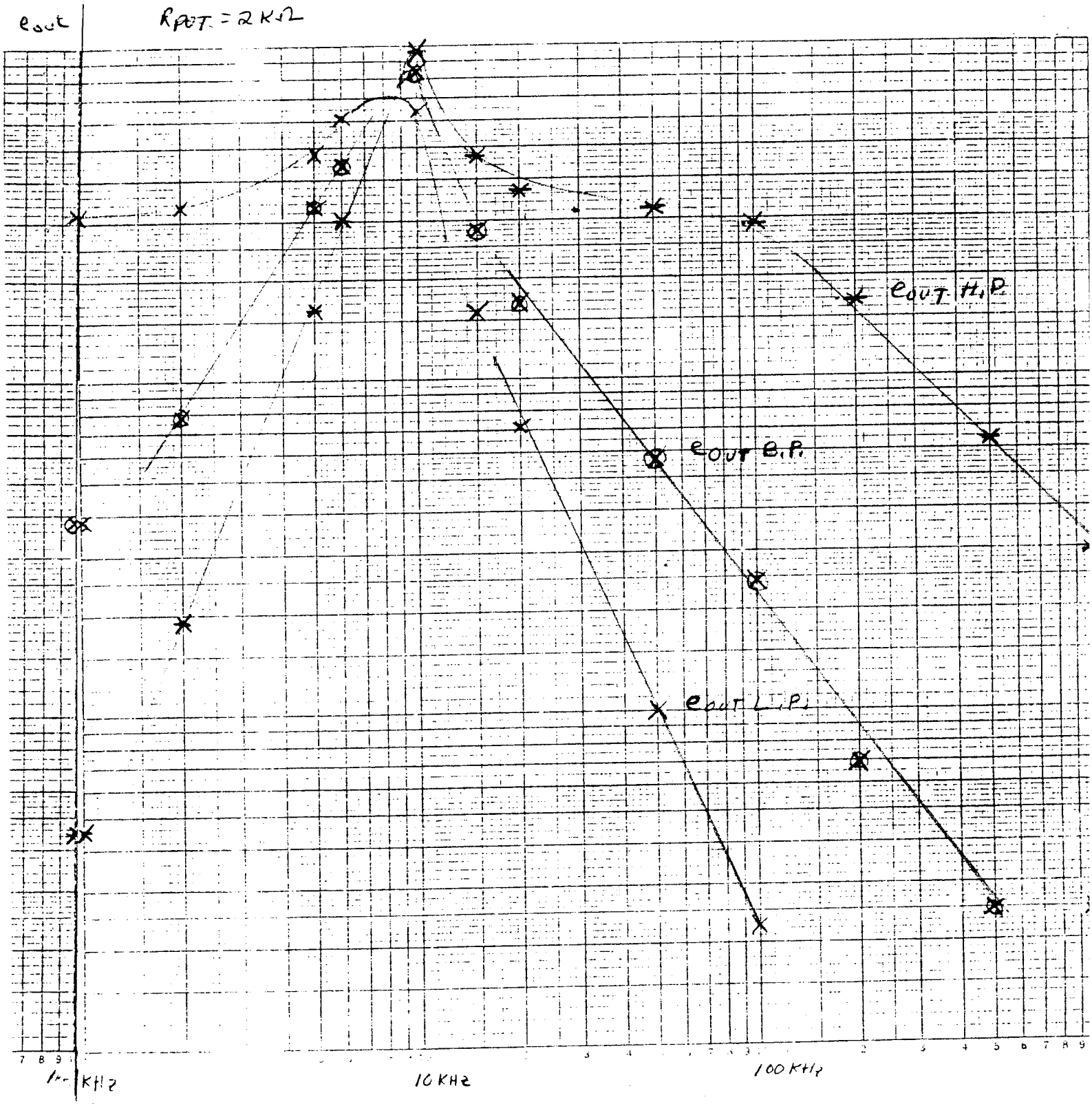


Figure 7

Biquad Measurements

Experiments were carried out to verify properties given by formulas for the transfer function, ω_o and Q, as given on pages A12 and A13.

Thus, in the biquad circuit of page A10, component values were selected to give interesting values for f_o and Q, to wit

$$R_3 = R_1 = 100\,K$$
$$C = C_1 = C_2 = 0.1\ \mu f$$
$$R = R_5 = R_6 = 170\ K$$

whence

$$f_o = \frac{\omega_o}{2\pi} = \frac{1}{2\pi RC} = 9.36\ hz$$

For the interesting band pass low frequency case, where f_o for maximum gain was measured at ~8 hz, data was taken on the effect of the ratio $\frac{R_L}{R_1}$ on the band width.

Here R_1 was fixed at 100k, and R_2 was varied from 100K to 800K. For each value of R_2, the peak voltage was measured, the 0.707 values on either side were determined and the frequencies determined which gave those 3db voltages. The band width so measured agreed to about 15% with the result obtained by calculating the band width via $B = \frac{f_o}{Q}$ where Q is calculated by (8) on p. A13.

For example, with R_2 set at 350K, the 3db frequencies were measured as 6.21 hz and 10.4 hz, or Δf = 4.2 hz. Formula (8) gives

$$Q = \frac{1}{2}\left(1 + \frac{350}{100}\right) = 2.25, \text{ and } \qquad B = \frac{8}{2.25} = 3.6\ hz$$

Curves are given for the measured frequency behavior at the 3 terminals (LP, BP and HP) in Figure 8. Phase shift data, as required for Bode plots, were also obtained and showed satisfactory agreement with results expected from the transfer functions.

Biquad Active Filter

$R_2 = 100\ K$

□ L.P.

⊙ H.P.

X B.P.

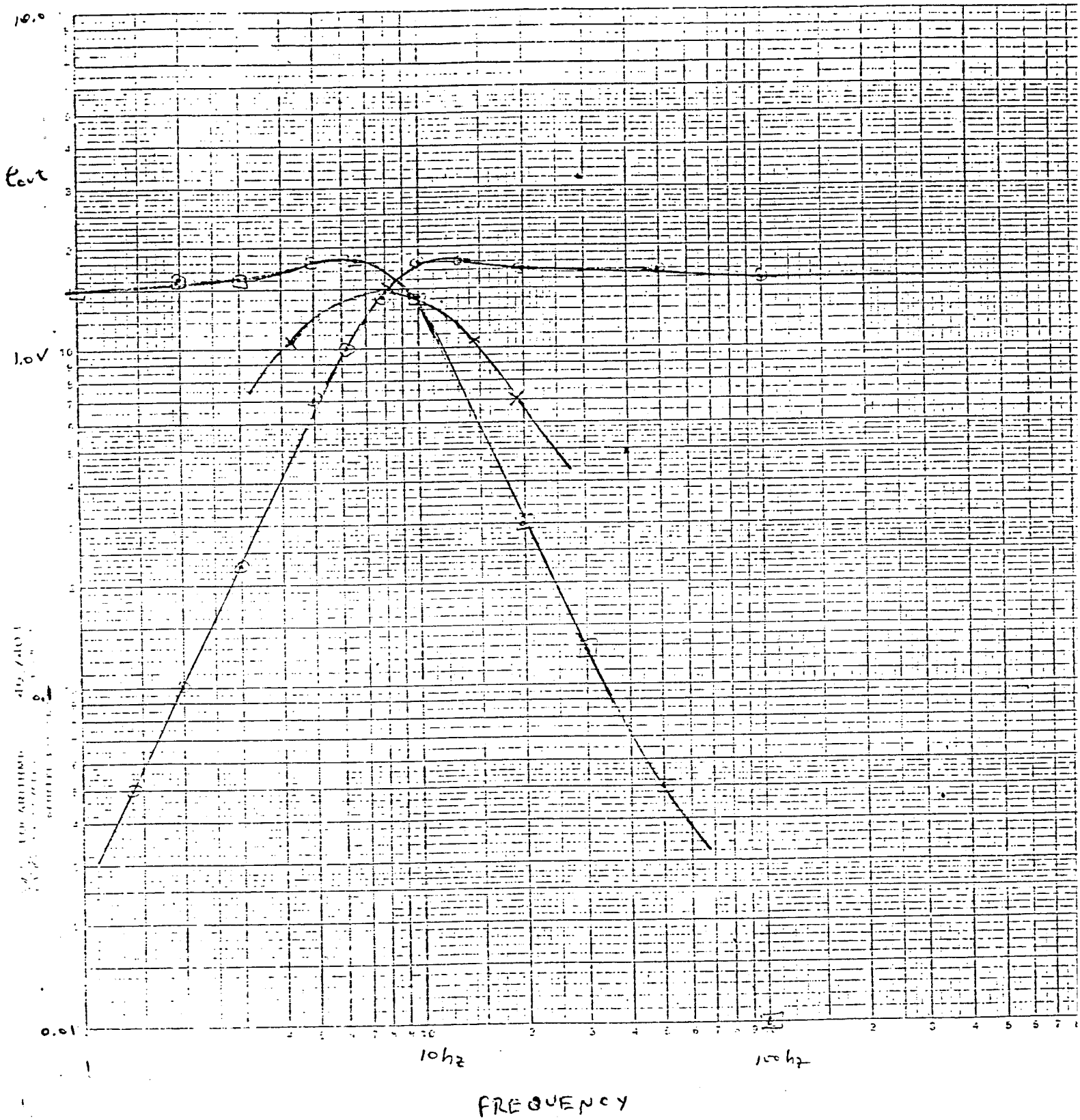


Figure 8

Active Filter References

1. J.G. Graeme, G.E. Tobey and L.P. Huelsman, "Operational Amplifiers-Design and Application" McGraw Hill, 1971, Chapter 8 (Active Filters)

2. J.J. Friend, C.A. Harris, and D.Hilberman, "STAR: An Active Biquadratic Filter Section", IEEE Trans. Circ. Syst. CAS-22(2), 1975, p 115

3. J.L. Hilburn and D.E. Johnson, "Manual of Active Filter Design", 2nd ed MCGraw Hill, 1983

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5. W.J. Kerwin, L.P. Huelsman and R.W. Newcomb, "State Variable Synthesis for Insensitive Circuit Transfer Functions", IEEE J. Solid State Circ SC-2(3), 1967, p 87

6. J. Millman, "Microelectronic" McGraw Hill, 1979, pp 582-593

7. R.P. Sallen and E.L. Key, "A Practical Method of Designing RC Active Filters", IRE Trans Circ Theory, CT-2(1), 1955, p 74

8. L.C. Thomas, "The Biquad: Part-1 Some Practical Design Considerations" IEEE Trans Circ Theory, CT-18(3), 1971, p350

9. L.C. Thomas, "The Biquad" Part II-A Multipurpose Active Filtering System", IEEE Trans Circ Theory CT-18(3), 1971, p358

10. J. Tow, "Active RC Filters-A State Space Realization", Proceedings of the IEEE, Letters, June 1968, p 1137

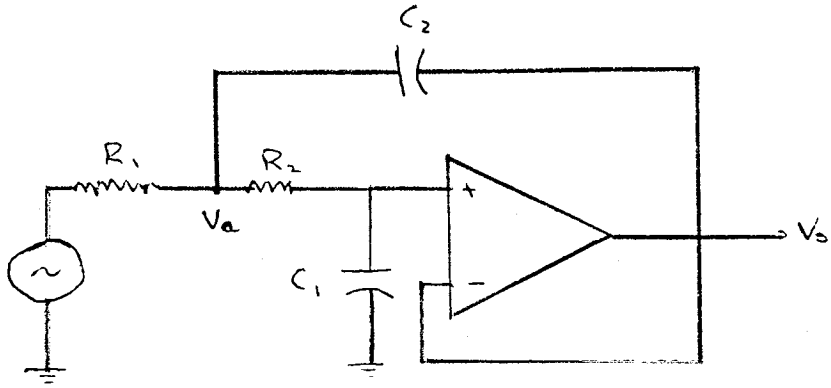
11. J. Tow, "Design Formulas for Active RC Filters Using Operational Amplifier Biquads" Electron Lett, 5(15), 1969, p 339

12. D. Van Dalsen, EDN, Nov 5, 1978, p 105. Subject: Active Filter Design Aids

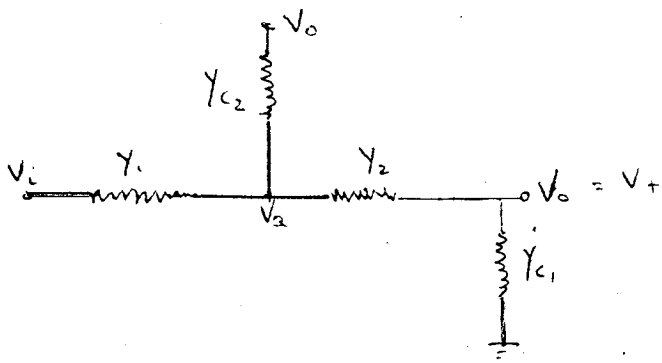
13. A.B. Williams, "Electronic Filter Design", McGraw Hill, 1981

Appendix 1 Analysis of some interesting Active Filters

Non Inverting VCVS



We note that $V^+ = V^- = Vo$ here. In order to apply the circuit to a number of operational modes (HP,LP, etc), we replace the R and C components by more general admittances, as shown.



For the node at Va, KCL (or nodal analysis) gives

(1) $$(V_a - V_o)\,Y_{c_2} + (V_a - V_o)\,Y_2 + (V_a - V_i)\,Y_1 = 0$$

(1a) For the node at V+, $$(V_o - 0)\,Y_{c_1} + (V_o - V_a)\,Y_2 = 0$$

whence $$V_a = \frac{(Y_{c_1} + Y_2)\,V_o}{Y_2}$$

From (1) and (1a), Vi $$V_i = \left[\frac{(Y_{c_1} + Y_2)}{Y_2}(Y_{c_2} + Y_2 + Y_1) - \frac{(Y_{c_2} + Y_2)}{Y_1}\right] V_o$$

$$= \frac{Y_{c_1}(Y_{c_2} + Y_2 + Y_1) + Y_1 Y_2}{Y_1 Y_2}\,V_o .$$

(2) Therefore $$\frac{V_o}{V_i} = \frac{Y_1 Y_2}{Y_{c_1}(Y_{c_2} + Y_2 + Y_1) + Y_1 Y_2}$$

From this, we get the transfer function

$$(3) \qquad T.F.(s) = \frac{V_o(s)}{V_i(s)} \qquad \frac{\frac{1}{R_1 R_2}}{sC_1\left(sC_2 + \frac{1}{R_1} + \frac{1}{R_2}\right) + \frac{1}{R_1 R_2}}$$

where we have now specialized by setting

$$Y_1 = \frac{1}{R_1}, \quad Y_2 = \frac{1}{R_2}, \quad Y_{c_1} = sC_1, \qquad Y_2 = sC_2$$

(3) Then becomes

$$\frac{V_o(s)}{V_i(s)} = \frac{\frac{1}{R_1 R_2 C_1 C_2}}{s^2 + s\left(\frac{1}{R_2 C_2} + \frac{1}{R_1 C_2}\right) + \frac{1}{R_1 R_2 C_1 C_2}}$$

Setting S = 0 gives the DC gain of 1. Comparison with the form

$$\frac{1}{s^2 + 2\zeta\omega_o s + \omega_o^2} \quad \text{then gives}$$

$$\omega_o = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

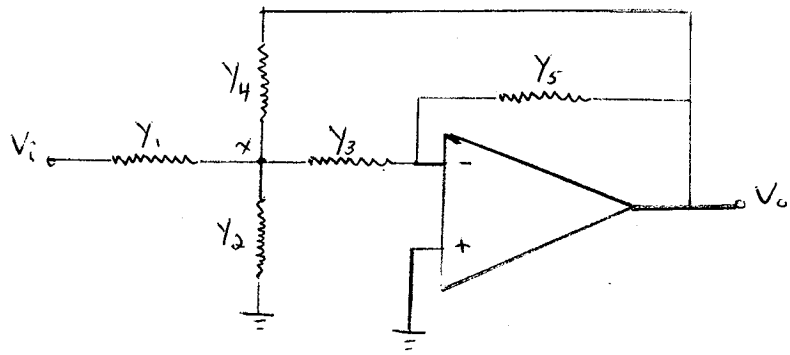
and

$$\zeta = \frac{\frac{1}{R_2 C_2} + \frac{1}{R_1 C_2}}{2\omega_o}$$

$$= \frac{1}{2C_2} \frac{(R_1 R_2 C_1 C_2)^{1/2}}{} \cdot \left(\frac{R_1 + R_2}{R_1 R_2}\right)$$

$$= \left(\frac{C_1}{C_2}\right)^{\frac{1}{2}} \cdot \frac{(R_1 + R_2)}{2\sqrt{R_1 R_2}}$$

Infinite Gain Multiple Feedback Circuit (MFN)



For generality we consider the above network. Again we assume an ideal op-amp (so $V_- = V_+ = 0$, and $I_{in} = 0$).

Then KCL at node x gives

(1) $$(V_x - V_i)\,Y_1 + (V_x - V_o)\,Y_4 + (V_x - 0)\,Y_3 + (V_x - 0)\,Y_2 = 0$$

The node at the inverting input gives

$$(V_x - 0)\,Y_3 + (V_o - 0)\,Y_5 = 0,$$

(2) $$\text{whence} \quad V_x = -V_o \cdot \frac{Y_5}{Y_3}$$

From (1),

$$V_i = V_x\left(\frac{Y_1 + Y_4 + Y_3 + Y_2}{Y_1}\right) - \left(\frac{Y_4}{Y_1}\right)V_o$$

$$= -\left[\frac{Y_5}{Y_3}\left(\frac{Y_1 + Y_4 + Y_3 + Y_2}{Y_1}\right) + \frac{Y_4}{Y_1}\right]\cdot V_o$$

Therefore

$$\frac{V_o}{V_i} = -\frac{Y_1 Y_3}{Y_5\left(Y_1 + Y_2 + Y_3 + Y_4\right) + Y_3 Y_4}$$

Next we specialize to the case of

$$Y_1 = \frac{1}{R_1}, \quad Y_2 = sC_2, \quad Y_3 = \frac{1}{R_3}, \quad Y_4 = \frac{1}{R_4}, \quad Y_5 = sC_5$$

This gives for the transfer function

$$T.F(s) = \frac{V_o(s)}{V_i(s)} = -\frac{\dfrac{1}{R_1 R_3}}{s C_5\left(\dfrac{1}{R_1} + \dfrac{1}{R_3} + \dfrac{1}{R_4} + sC_2\right) + \dfrac{1}{R_3 R_4}}$$

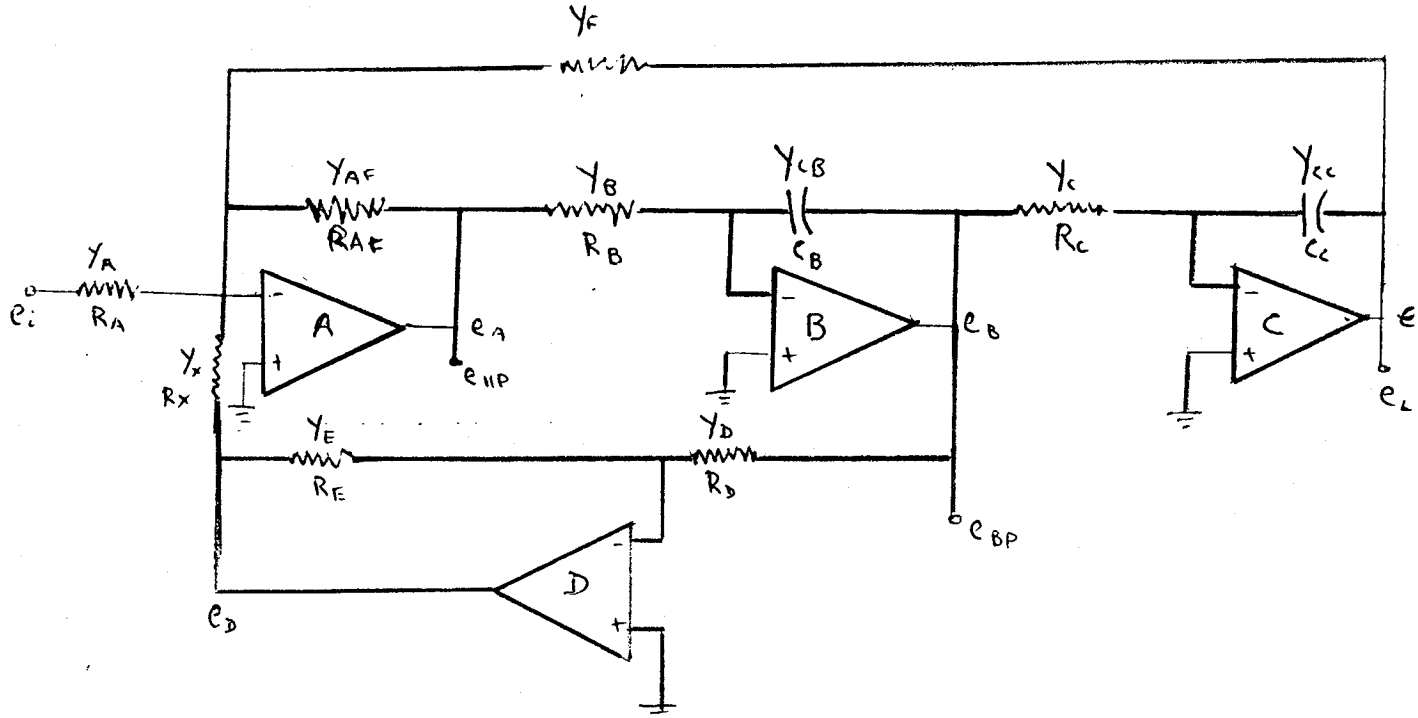
$$= -\frac{\dfrac{1}{R_1 R_3 C_2 C_5}}{s^2 + \dfrac{s}{C_2}\left(\dfrac{1}{R_1} + \dfrac{1}{R_3} + \dfrac{1}{R_4}\right) + \dfrac{1}{R_3 R_4 C_2 C_5}}$$

Thus the DC gain (if set s=0) is $-\dfrac{R_4}{R_1}$, $\omega_o = \dfrac{1}{(R_3 R_4 C_2 C_5)^{1/2}}$

and $\zeta = \dfrac{\text{coefficient of } s}{2\omega_o} = \dfrac{1}{2}(R_3 R_4 C_2 C_5)^{1/2} \dfrac{1}{C_2}\left(\dfrac{1}{R_1} + \dfrac{1}{R_3} + \dfrac{1}{R_4}\right)$

$$= \frac{1}{2}\left(\frac{C_5}{C_2}\right)^{1/2}\left[\frac{\sqrt{R_3 R_4}}{R_1} + \left(\frac{R_4}{R_3}\right)^{1/2} + \left(\frac{R_3}{R_4}\right)^{1/2}\right]$$

State Variable Filter



We use the general ideal op-amp property that all inputs draw no current, and all the above inverting inputs are at virtual ground.

Node

(1) V_A^- $\quad (0 - e_i) Y_A + (0 - e_A) Y_{AF} + (0 - e_D) Y_x + (0 - e_c) Y_F = 0$

(2) V_B^- $\quad (0 - e_A) Y_B + (0 - e_B) Y_{CB} = 0$

(3) V_C^- $\quad (0 - e_B) Y_C + (0 - e_c) Y_{CC} = 0$

(4) V_D^- $\quad (0 - e_D) Y_E + (0 - e_B) Y_D = 0$

whence

(5) $$Y_{AF}\, e_A + Y_F\, e_c + Y_x\, e_D = -Y_A\, e_i$$

(6) $$e_A = -\frac{Y_{CB}}{Y_B}\, e_B$$

(6a) $$e_c = -\frac{Y_c}{Y_{cc}} e_B$$

(6b) $$e_D = -\frac{Y_E}{Y_D} e_B$$

Substituting for all the other variables in terms of e_B in (5), we get

$$e_B\left[Y_{AF}\left(-\frac{Y_{CB}}{Y_B}\right) + Y_F\left(-\frac{Y_c}{Y_{cc}}\right) + Y_x\left(-\frac{Y_D}{Y_E}\right)\right. = -Y_A e_i$$

whence

$$\frac{e_B}{e_i} = \frac{Y_A}{\frac{Y_{AF}Y_{CB}}{Y_B} + \frac{Y_F Y_c}{Y_{cc}} + \frac{Y_D Y_x}{Y_E}}$$

$$= \frac{Y_A Y_B Y_{cc} Y_E}{Y_{AF} Y_{CB} Y_{cc} Y_E + Y_F Y_c Y_B Y_E + Y_B Y_D Y_{cc} Y_x}$$

Next we set $Y_A = \frac{1}{R_A}$, $Y_B = \frac{1}{R_B}$, $Y_c = \frac{1}{R_c}$, $Y_D = \frac{1}{R_D}$,

$Y_E = \frac{1}{R_E}$, $Y_{AF} = \frac{1}{R_{AF}}$, $Y_{CB} = SC_B$, $Y_{cc} = SC_c$, $Y_F = \frac{1}{R_F}$,

$Y_x = \frac{1}{R_x}$,

$$\frac{e_B}{e_i} = \frac{\frac{SC_c}{R_A R_B R_E}}{\frac{S^2 C_B C_c}{R_{AF} R_E} + \frac{1}{R_F R_B R_c R_E} + \frac{SC_c}{R_E R_D R_x}}$$

(7) $$= \frac{\frac{R_{AF}}{R_A} \cdot R_c R_D R_F R_x SC_c}{S^2 C_B C_c R_B R_c R_D R_F R_x + SC_c R_{AF} R_c R_E R_F + R_{AF} R_D R_x},$$

which shows the usual form of the band-pass filter.

We proceed to simplify this expression by specializing to the case where

$$R_B = R_C \equiv R'_F,$$

$$R_F = R_{AF} = R_A = R_D \equiv R,$$

$$R_A = R_g, \quad R_E = R'_d \quad \text{and} \quad C_B = C_C \equiv C.$$

Then (7) reduces to

$$\frac{e_B}{e_i} = \frac{R}{R_g} \frac{R'_F R \cdot R \cdot R \cdot SC}{S^2 C^2 R'^2_F R^3 + SC R'_F R^2 R_d + R^3}$$

$$= \frac{R}{C R_g R'_F} \frac{S}{S^2 + \frac{R_d}{C R'_F R} S + \frac{1}{C^2 R'^2_F}} \tag{8}$$

This is clearly in the form given by Van Dalsen.*

Equations (6) for e_A and e_C allow us to find the outputs at the high pass and the low-pass terminals and are clearly of the correct form in their s dependence (i.e. $e_A \sim \frac{S^2}{Q(s)}$ and $e_C \sim \frac{1}{Q(s)}$ where Q(s) is quadratic in s)

For clarity this circuit is redrawn on the next page in the new notation, with the useful simplifications made and the primes on R'_f and R'_d dropped.

*D. Van Dalsen, EDN, Nov. 5, 1978, p. 106, a particularly useful reference in GSFC's work.

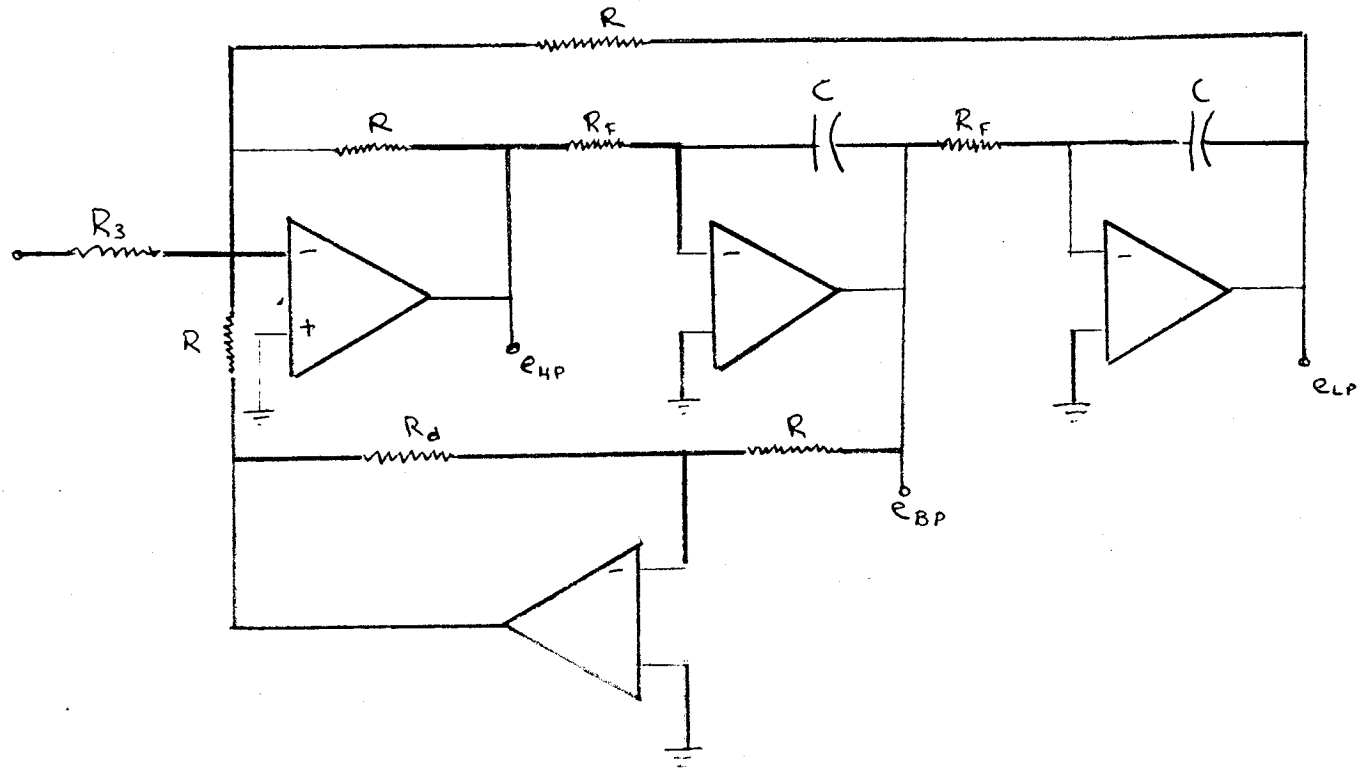


Fig A3

If this form (equation (8)) is identified with equation (5) of the band-pass case on page 23, it follows that

$$\omega_0 = \frac{1}{R_F C}$$

Further

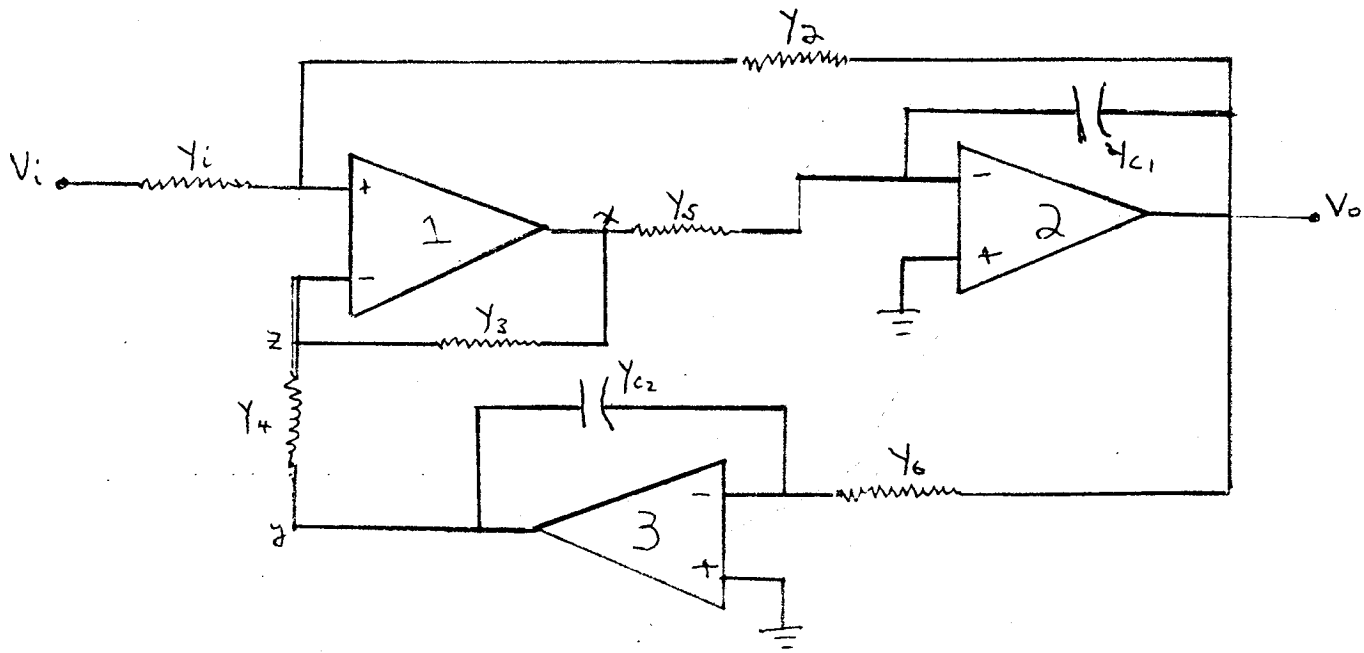
$$\alpha \omega_0 = \frac{R_d}{C R_F R},$$

whence

$$\alpha = \frac{R_d}{R},$$

which allows the damping or bandwidth to be set independently by Rd, and the DC gain to be set by the input resistor Rg.

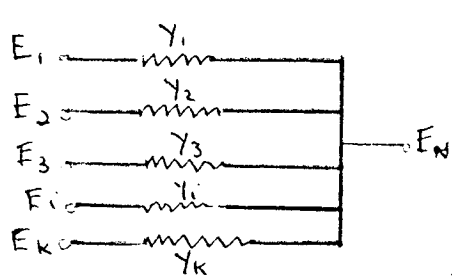
BiQuad Active Filter



As an instructive and more complex example of a very useful active filter analyzed without the use of Cramer's Rules, we here consider the above biquad active filter. We again follow the spirit of earlier examples in that we express all easily obtained node variables as a function of V_i or V_o, and thus eliminate them in in the ramaining nodal relations. The transfer function of the system, and finally the transfer function between the input and any node follows immediately. This then allows properties at various nodes to be examined as additional useful outputs.

We make use of Millman's Theorem* at the various nodes indicated

*



One proves immediately from KCL that

$$E_N\left(\sum_{i=1}^{K} Y_i\right) = \sum_{i=1}^{K} E_i Y_i$$

Node

$V_1^+ = V_z$ (1) $V_i Y_i + V_o Y_2 = V_z(Y_1 + Y_2)$, or

(1a) $(Y_1 + Y_2) V_z - Y_2 V_o = Y_i V_i$

$V_2^- = 0$ (2) $V_o Y_{c1} + V_x Y_5 = 0$, $V_x = -\frac{Y_{c1}}{Y_5} V_o$

$V_3^- = 0$ (3) $V_o Y_6 + V_y Y_{c2} = 0$, $V_y = -\frac{Y_6}{Y_{c2}} V_o$

V_z (4) $V_x Y_3 + V_y Y_4 = V_z (Y_3 + Y_4)$

Substitution from (2) and (3) into (4) gives

(5) $$V_z = \frac{1}{(Y_3 + Y_4)}\left[Y_3 \cdot \left(-\frac{Y_{c1}}{Y_5} V_o\right) + Y_4\left(-\frac{Y_6}{Y_{c2}}\right) V_o\right]$$

$$= -\frac{1}{(Y_3 + Y_4)}\left[\frac{Y_3 Y_{c1}}{Y_5} + \frac{Y_4 Y_6}{Y_{c2}}\right] V_o$$

Then using (5) in (1a), we get

(6) $$\left\{-\frac{(Y_1 + Y_2)}{(Y_3 + Y_4)}\left[\frac{Y_3 Y_{c1}}{Y_5} + \frac{Y_4 Y_6}{Y_{c2}}\right] - Y_2\right\} V_o = Y_i V_i$$

This gives the transfer function

(6a) $$\frac{V_o}{V_i}(s) = -\frac{Y_i}{\left(\frac{Y_1 + Y_2}{Y_3 + Y_4}\right)\left[\frac{Y_3 Y_{c1}}{Y_5} + \frac{Y_4 Y_6}{Y_{c2}}\right] + Y_2}$$

Next we specialize to the admittances

$$Y_i = \frac{1}{R_1}, \quad Y_2 = \frac{1}{R_2}, \quad Y_3 = \frac{1}{R_3}$$

$$Y_4 = \frac{1}{R_4}, \quad Y_5 = \frac{1}{R_5}, \quad Y_6 = \frac{1}{R_6}$$

$$Y_{c1} = sC_1, \quad Y_{c2} = sC_2.$$

Then (6a) gives

$$\frac{V_o}{V_i}(s) = -\frac{\frac{1}{R_1}}{\left(\frac{\frac{1}{R_1}+\frac{1}{R_2}}{\frac{1}{R_3}+\frac{1}{R_4}}\right)\left(\frac{R_5}{R_3}sC_1 + \frac{1}{R_4R_6sC_2}\right)+\frac{1}{R_2}}$$

If we now set

$$p = \frac{\frac{1}{R_3}+\frac{1}{R_4}}{\frac{1}{R_1}+\frac{1}{R_2}} = \left(\frac{R_3+R_4}{R_1+R_2}\right)\cdot\frac{R_1R_2}{R_3R_4}$$

then

$$\frac{V_o}{V_i}(s) = -\frac{\frac{1}{R_1}}{\frac{1}{p}\left(\frac{R_5}{R_3}sC_1 + \frac{1}{R_4R_6sC_2}\right)+\frac{1}{R_2}}$$

$$= -\frac{p}{R_1}\left[\frac{1}{\frac{R_5}{R_3}sC_1 + \frac{1}{R_4R_6sC_2} + \frac{p}{R_2}}\right]$$

$$= -\left(\frac{R_3+R_4}{R_1+R_2}\right)\left(\frac{R_2}{R_3R_4}\right)\left(\frac{R_2R_3R_4R_6sC_2}{R_2R_4R_5R_6s^2C_2C_1 + R_2R_3 + pR_3R_4R_6s}\right)$$

(7) $$= -\left(\frac{R_3+R_4}{R_1+R_2}\right)\left(\frac{R_2}{R_4R_5C_1}\right)\left(\frac{s}{s^2 + \frac{pR_3}{R_2R_5C_1}s + \frac{R_3}{R_4R_5R_6C_1C_2}}\right)$$

If we further set

$$B = \frac{pR_3}{R_2R_5C_1}, \quad C = \frac{R_3}{R_4R_5R_6C_1C_2}$$

so that the denominator can be compared with the form

$$\frac{1}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}$$

we see that $$\omega_o = C^{1/2} = \left(\frac{R_3}{R_4R_5R_6C_1C_2}\right)^{1/2}$$

and

$$Q = \frac{\omega_0}{\text{coefficient of } S} = \frac{\omega_0}{B} = \frac{R_2}{P}\left(\frac{R_5 C_1}{R_3 R_4 R_6 C}\right)^{1/2}$$

$$= R_2\left(\frac{R_1 + R_2}{R_3 + R_4}\right)\left(\frac{R_3 R_4}{R_1 R_2}\right)\left(\frac{R_5 C_1}{R_3 R_4 R_6 C_2}\right)^{1/2}$$

$$= \frac{1 + \frac{R_2}{R_1}}{1 + \frac{R_3}{R_4}}\left(\frac{R_3 R_5 C_1}{R_4 R_6 C_2}\right)^{1/2}$$

If one simplifies the design by taking R3 = R4, R = R5 = R6, and C = C1 = C2, the useful results

$$f_0 = \frac{1}{2\pi RC}$$

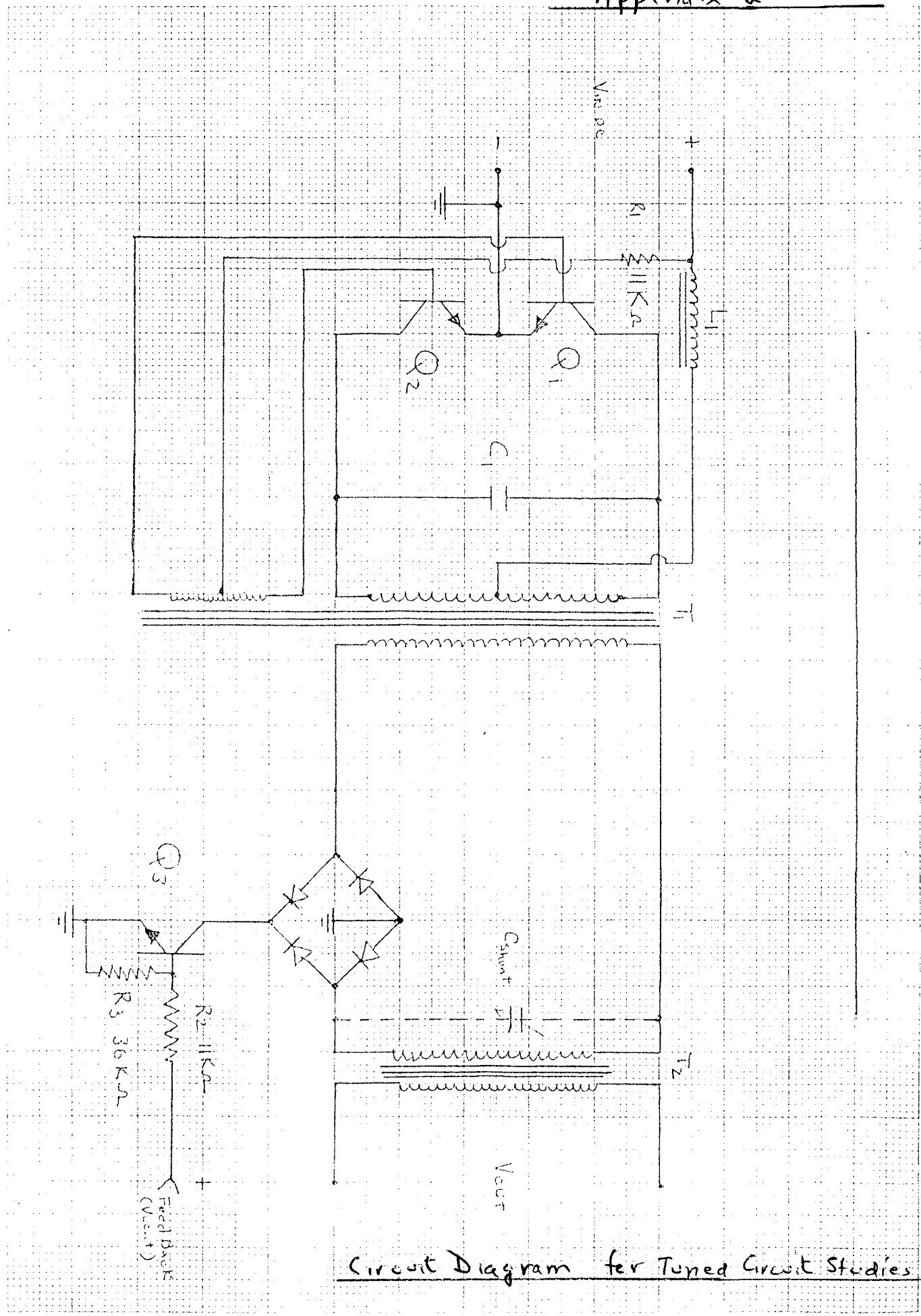
(8) and

$$Q = \frac{1}{2}\left(1 + \frac{R_2}{R_1}\right)$$

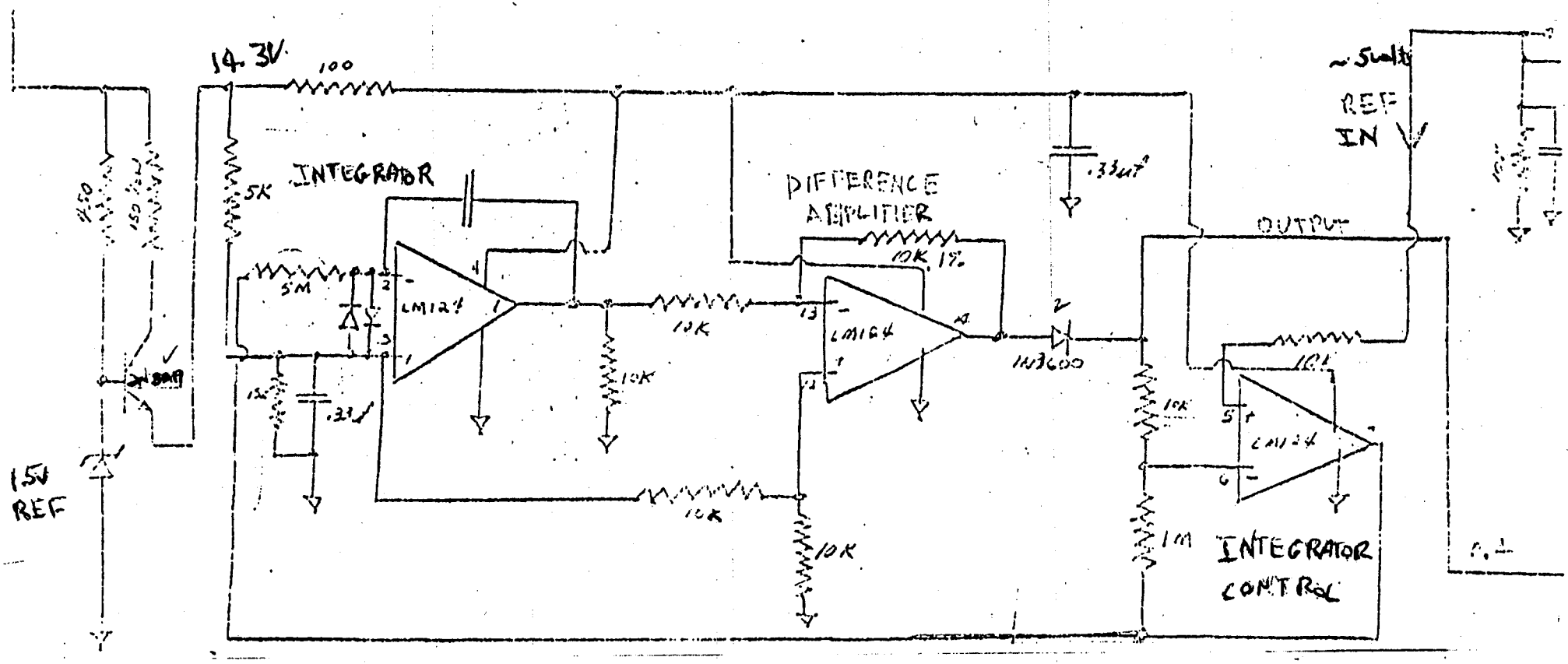
are obtained.

It is clear from equations (2) and (3) that point x is a high-pass output and point y is a low-pass output.

Appendix 2



Circuit Diagram for Tuned Circuit Studies

Appendix 3

Ramp Generator Circuit