TEST CHIPS FOR ASIC QUALIFICATION

TEST CHIP AND FABRICATION RUN N06J RESULTS

HIRIS DATA COMPRESSOR CHIP

STANDARD CELL AND SEU SRAM CHIP RESULTS

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HDCC12-1b

MOSIS FABRICATION RUN N06J
INTRODUCTION

THE HIRIS DATA COMPRESSOR CHIP (HDCC) AND A JPL STANDARD CELL TEST CHIP WERE FABRICATED AT A SILICON FOUNDRY THROUGH THE MOSIS PROTOTYPING SERVICE.

THE VLSI TECHNOLOGY GROUP SUBMITTED ITS FULL SUITE OF TEST STRUCTURES ON THE RUN AND THIS REPORT CONTAINS THE RESULTS OF THE TEST STRUCTURE ANALYSIS.

THE SEU/TD RADIATION MONITOR WAS INCLUDED ON THE HDCC FABRICATION RUN. THESE CHIPS WERE PACKAGED, SCREENED, AND DELIVERED TO THE MIT LINCOLN LABORATORY AND WILL BE LAUNCHED ON THE MSX (MID-COURSE SPACE EXPERIMENT) SATELLITE IN 1992.

OUTLINE

- ASIC FAMILY
  - EXECUTIVE SUMMARY OF RESULTS _ _ _ _ _ _ _ _ _ _ 4a
  - ASIC (HDCC) _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ 5a
  - JPL STANDARD CELL TEST CHIP _ _ _ _ _ _ _ _ _ _ 6a
- TEST CHIP FAMILY
  - EXECUTIVE SUMMARY OF RESULTS _ _ _ _ _ _ _ _ _ 4b
  - FAULT CHIP _ 8a
  - PROCESS MONITOR _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ 14a
  - RELIABILITY CHIP _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ 18a
  - TOTAL IONIZING DOSE CHIP _ _ _ _ _ _ _ _ _ _ _ 23a
  - SEU/TD RADIATION MONITOR _ _ _ _ _ _ _ _ _ _ _ 29a
  - SEU SRAM _ 37a
- VLSI TECHNOLOGY GROUP _ _ _ _ _ _ _ _ _ _ _ 39b

PRODUCT ASSURANCE TECHNOLOGY PROGRAM

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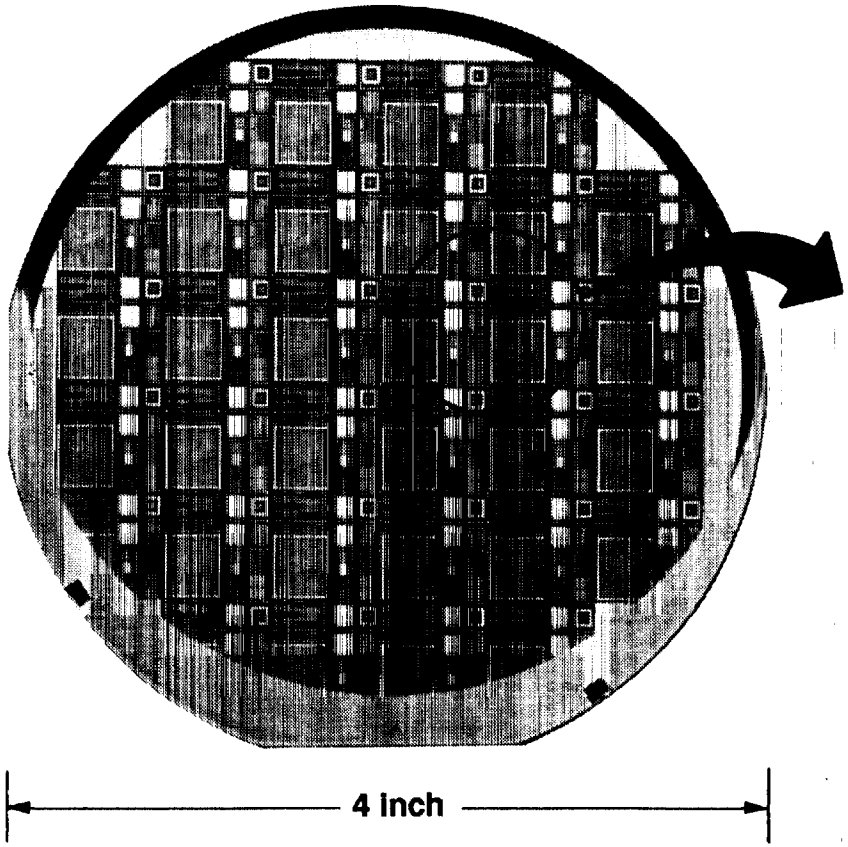
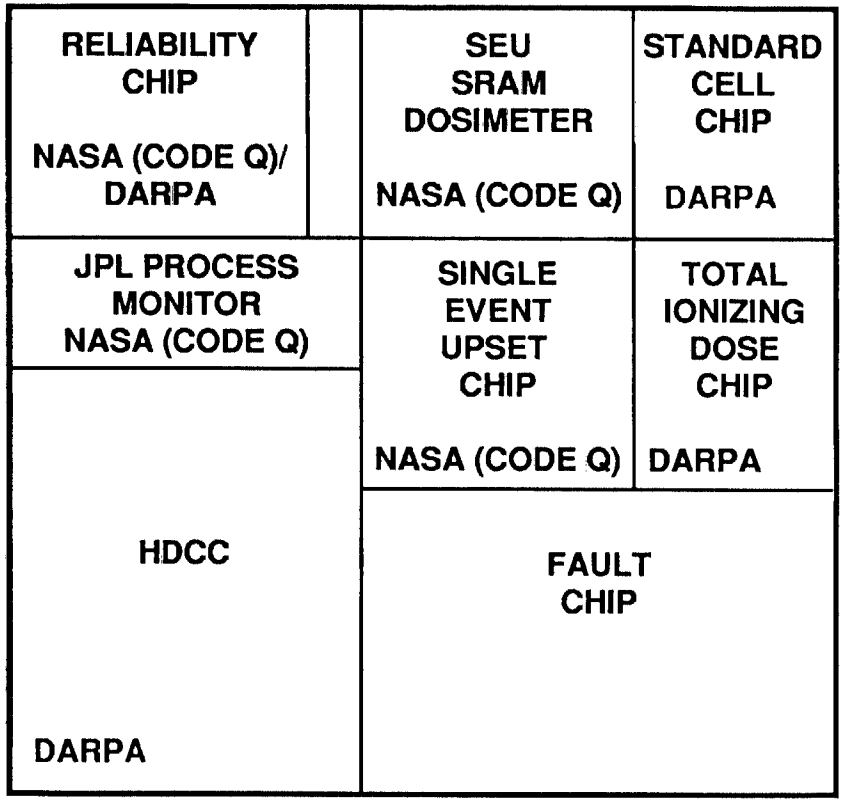
MICROELECTRONIC TEST CHIPS FOR SPACE QUALIFIED APPLICATION SPECIFIC ICs



1.6 μm CMOS CHIP FLOOR PLAN



- TEST STRUCTURES FOR PARTS PROCUREMENT NASA (CODE Q) TASK PROVIDES IMPLEMENTATION
- SILICON MANUFACTURING SCIENCE NASA (CODE Q) TASK PROVIDES INSIGHT INTO FUTURE TECHNOLOGY (0.5 μm CMOS)

HDCC12-3a

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MOSIS PROTOTYPE PART FAB RUN N06J FUNCTIONAL YIELD SUMMARY

- HIRIS DATA COMPRESSOR CHIP:
  - FUNCTIONAL YIELD = 80%
- STANDARD CELL TEST CHIP:
  - FUNCTIONAL YIELD = 97.3%
  - NON-FUNCTIONAL CHIPS EXHIBITED "STUCK AT" FAILURES
- RADIATION MONITOR
  - FUNCTIONAL YIELD = 94.6%
  - FAILURE TYPES INCLUDED STUCK MEMORY CELLS, LARGE CHIP STAND-BY LEAKAGE CURRENT, LARGE TRANSISTOR LEAKAGE CURRENT
- SEU SRAM
  - FUNCTIONAL YIELD = 84%
  - FAILURE TYPES INCLUDED STUCK MEMORY CELLS AND LARGE CHIP STAND-BY LEAKAGE CURRENT

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HIRIS DATA COMPRESSOR CHIP (HDCC) EXECUTIVE SUMMARY (FABRICATION RUN N06J)

- HDCC:
  - HDCC CONTAINS 49000 TRANSISTORS ON A CHIP THAT IS 9.3 mm BY 7.7 mm
  - HDCC CONTAINS APPROXIMATELY 125,000 ACTIVE, 14,000 POLY AND 43,000 VIA CONTACTS.
    - DESIGNED USING MENTOR GRAPHICS SYSTEM AND JPL STANDARD CELLS
    - FABRICATED THROUGH MOSIS AT A 1.6-μm n-WELL CMOS/BULK PROCESS
    - FABRICATED AT A "PROTOTYPE PART" FOUNDRY DESIGNED FOR QUICK TURNAROUND NOT HIGH RELIABILITY

- HDCC TEST RESULTS:
  - HDCC TESTED TO BE FULLY FUNCTIONAL
    - 80% YIELD WAS OBSERVED

- STANDARD CELL LIBRARY TEST CHIP RESULTS:
  - 50 CHIPS WERE FABRICATED AND 1 TESTED PARTIALLY BAD
  - STANDARD CELL TEST CHIP YIELD WAS 98%
  - STANDARD CELL CHIPS WERE TESTED USING AN IMS TESTER

- CONCLUSION:
  - GOOD YIELDS ARE BEING ATTAINED FOR COMPLEX CIRCUITS THROUGH MOSIS PROTOTYPE PART FABRICATION SERVICES

TEST STRUCTURE EXECUTIVE SUMMARY
MOSIS FABRICATION RUN N06J

- **PROCESS MONITOR:**
  - THE DISTRIBUTIONS OF THE CONTACT RESISTANCE MEASUREMENTS WERE UNACCEPTABLE.
- **FAULT CHIP:**
  - FOUND 15 METERS OF UNBROKEN, UNSHORTED METAL-1 WIRE. FOUND 1 SHORT IN 10 METERS OF METAL-2. FOUND 2 SHORTS AND 1 OPEN AT ONE SITE IN 25 METERS OF POLY. DEFECTIVE SITES WILL BE SUBMITTED FOR FAILURE ANALYSIS.
  - TESTED 30 MILLION TRANSISTORS AND FOUND 13 GATE OXIDE SHORTS.
  - INVERTER MATRIX VT_{inv}, MINIMUM VOLTAGE STANDARD DEVIATION = 2 mV.
  - CONTACT MATRIX DATA CORROBORATED PROCESS MONITOR FINDINGS THAT CONTACT CONDUCTANCES HAD WIDE DISTRIBUTIONS ACROSS THE LOT HOWEVER VARIABILITY WAS LOWER ACROSS EACH CHIP.
- **RELIABILITY CHIP:**
  - METAL ELECTROMIGRATION PARAMETERS WERE CONSISTENT AS MEASURED ON SEVERAL CHIPS.
- **TOTAL IONIZING DOSE CHIP:**
  - CIRCUITS FAILED IN THE n-MOSFET SIDE OF THE MOSFET MATRIX WHICH CORRELATES TO THE PROCESS MONITOR DATA SHOWING POOR M1/n+ DIFFUSION CONTACT RESISTANCE.
- **SEU CHIP:**
  - 50 EXPERIMENTAL SEU SRAM CHIPS WERE FABRICATED WITH A YIELD = 84%.
  - THIS YIELD WAS VERY CLOSE TO THE ASIC YIELD OF 80%.
- **RADIATION MONITOR CHIP:**
  - 75 EXPERIMENTAL SEU SRAM CHIPS WERE PACKAGED AND 50 WERE SCREENED USING A SUBSET OF THE MIL-STD-883C GUIDELINES.
  - THE RADIATION MONITOR CHIP YIELD WAS 94.6% BEFORE AND 85.3% AFTER BURN-IN.
  - MOSFET THRESHOLD VOLTAGES WERE WAFER DEPENDENT.

HDCC12-4b

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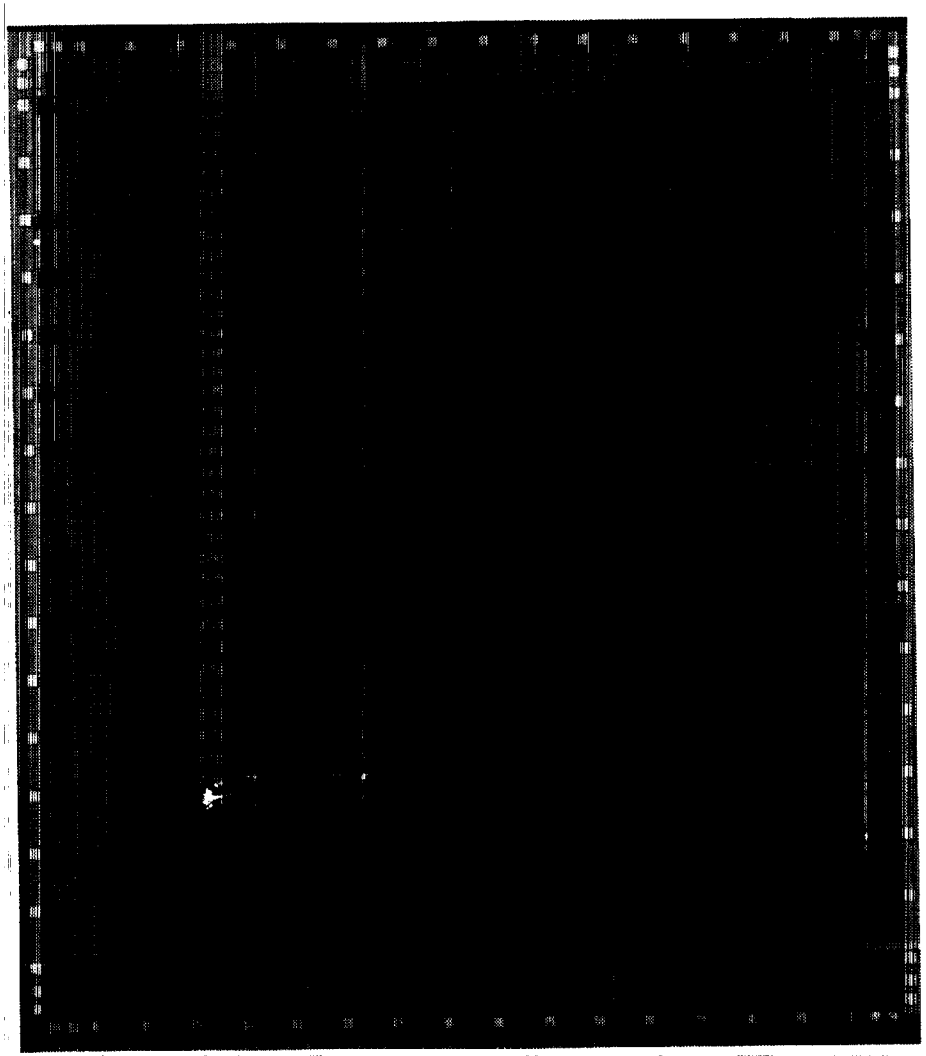
HIRIS DATA COMPRESSOR CHIP
1.6 μm n-WELL CMOS/BULK



CHIP SIZE = 9.3 mm x 7.7 mm

HDCC12-5a

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HIRIS DATA COMPRESSOR CHIP (HDCC) (MOSIS FABRICATION RUN N06J)

- HDCC:
  - HDCC IS A NOISELESS IMAGE COMPRESSION CHIP WHICH ACCEPTS PIXEL DATA (12-BIT WORD FORMAT) AT A 5-MHz RATE

- HDCC CHARACTERISTICS
  - FABRICATION PROCESS = 1.6 μm n-WELL CMOS/BULK
  - NO. TRANSISTORS = 49,000
  - CHIP SIZE = 9.3 mm x 7.7 mm
  - DESIGN APPROACH = SCHEMATIC CAPTURE, STANDARD CELLS

- DESIGN SYSTEM:
  - APOLLO AND MENTOR GRAPHICS CAD SYSTEMS

- DESIGN, FABRICATION, AND TEST SEQUENCE:

— SPECIFICATIONS BEGAN	JULY, 1989
— LOGIC DESIGN COMPLETED	DECEMBER, 1989
— SIMULATION COMPLETED	FEBRUARY, 1990
— MOSIS SUBMISSION	JUNE 11, 1990
— RETURN FROM FABRICATION	AUGUST 20, 1990
— TEST COMPLETION	AUGUST 20, 1990

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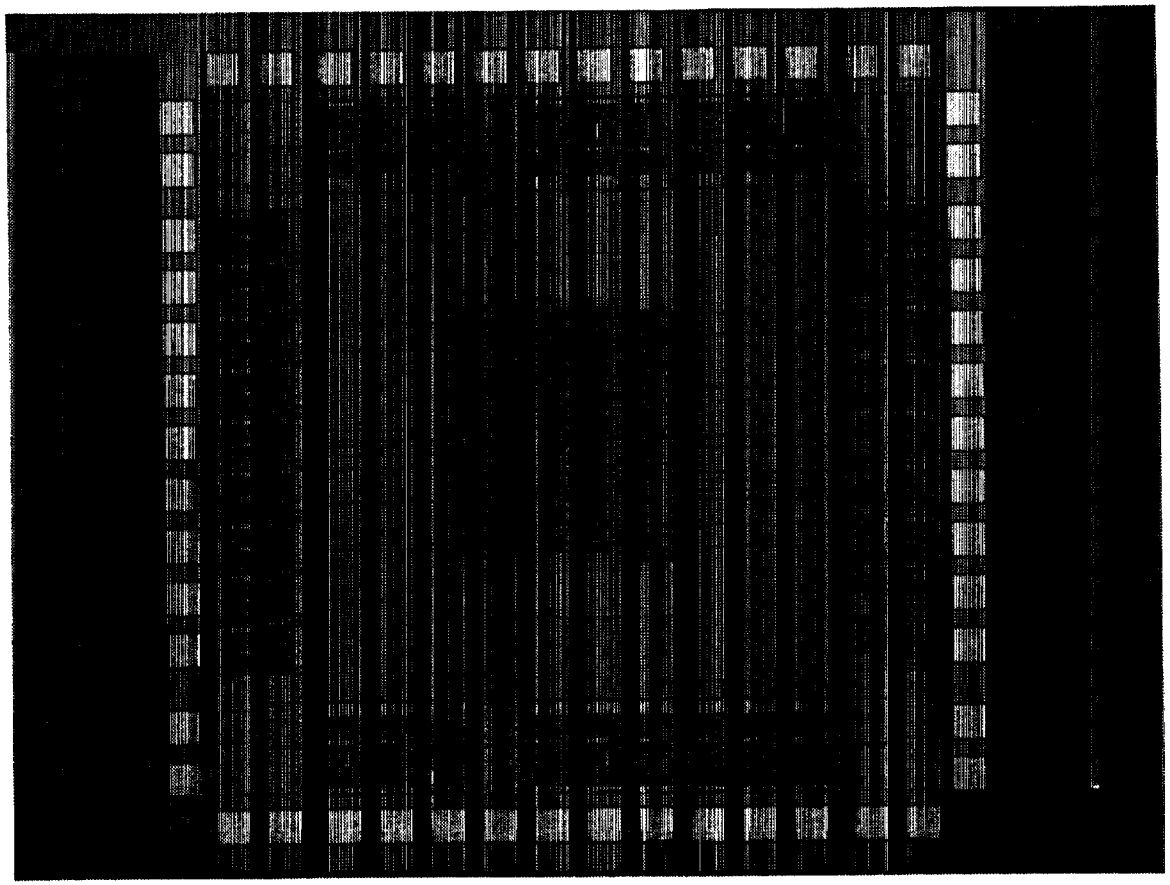
STANDARD CELL TEST CHIP



CHIP SIZE = 3.1 mm x 2.6 mm

HDCC12-6a

STANDARD CELL TEST CHIP (N06J) TEST SUMMARY

- 50 STANDARD CELL TEST CHIPS WERE FABRICATED ON ON MOSIS RUN N06J
- CHIP YIELD = 98%
- FAILURE TYPE = STUCK LATCH
- THE CIRCUIT CONTAINED SEVERAL LATCHES AND MASTER-SLAVE FLIP FLOPS TAKEN FROM THE SANDIA SCALABLE CELL LIBRARY
- NUMBER OF STANDARD CELLS EVALUATED = 15
- NUMBER OF TRANSISTORS/CHIP = 746
- FAILURES OF THIS TYPE WERE EXPECTED SINCE BOTH THE TID CHIP AND THE PROCESS MONITOR DETECTED PROBLEMS WITH THE n+ DIFFUSION TO METAL 1 CONTACTS ON RUN N06J

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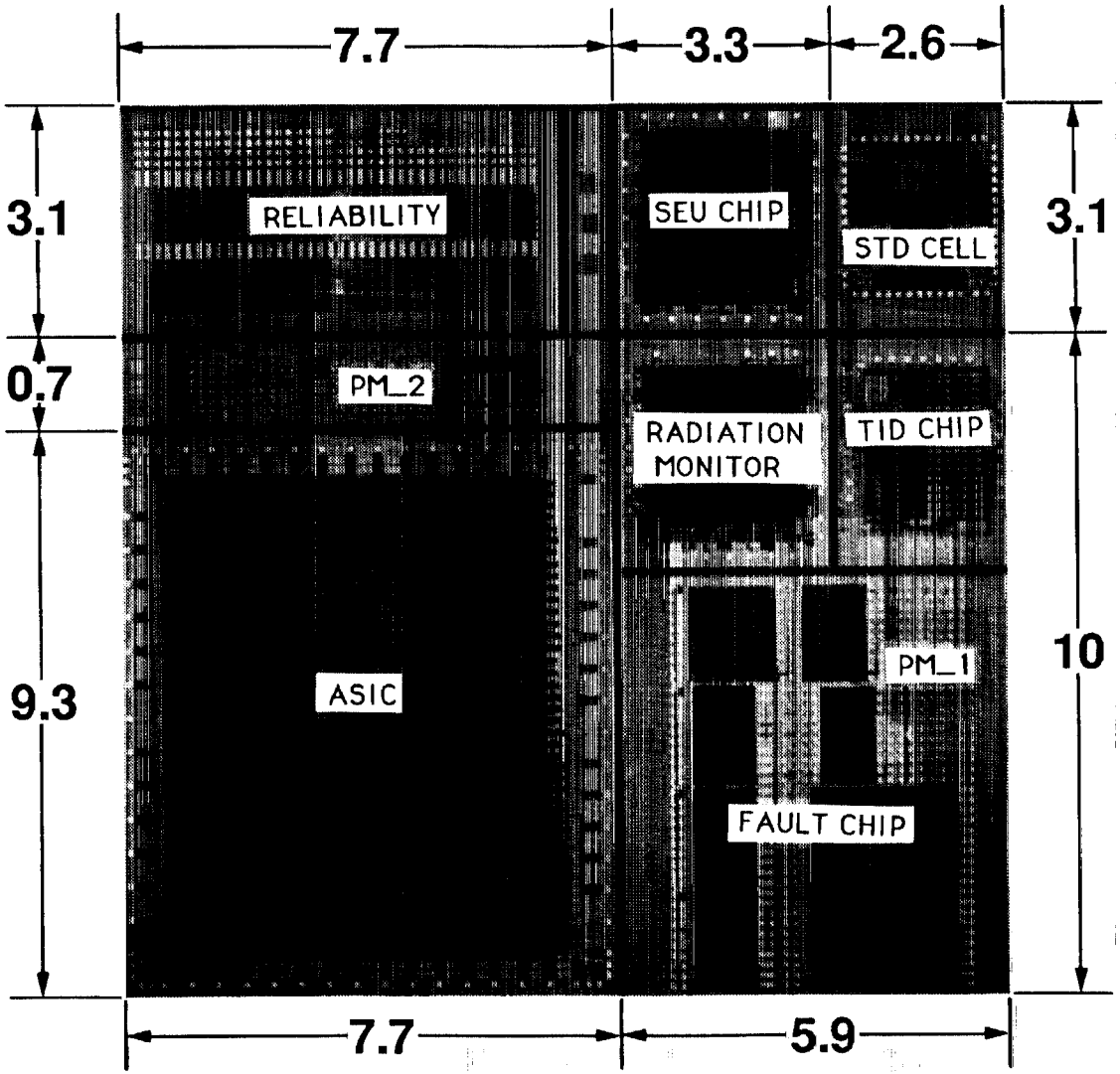
MOSIS N06J HDCC FABRICATION RUN
1.6-μm n-WELL CMOS/BULK



DIMENSIONS IN mm

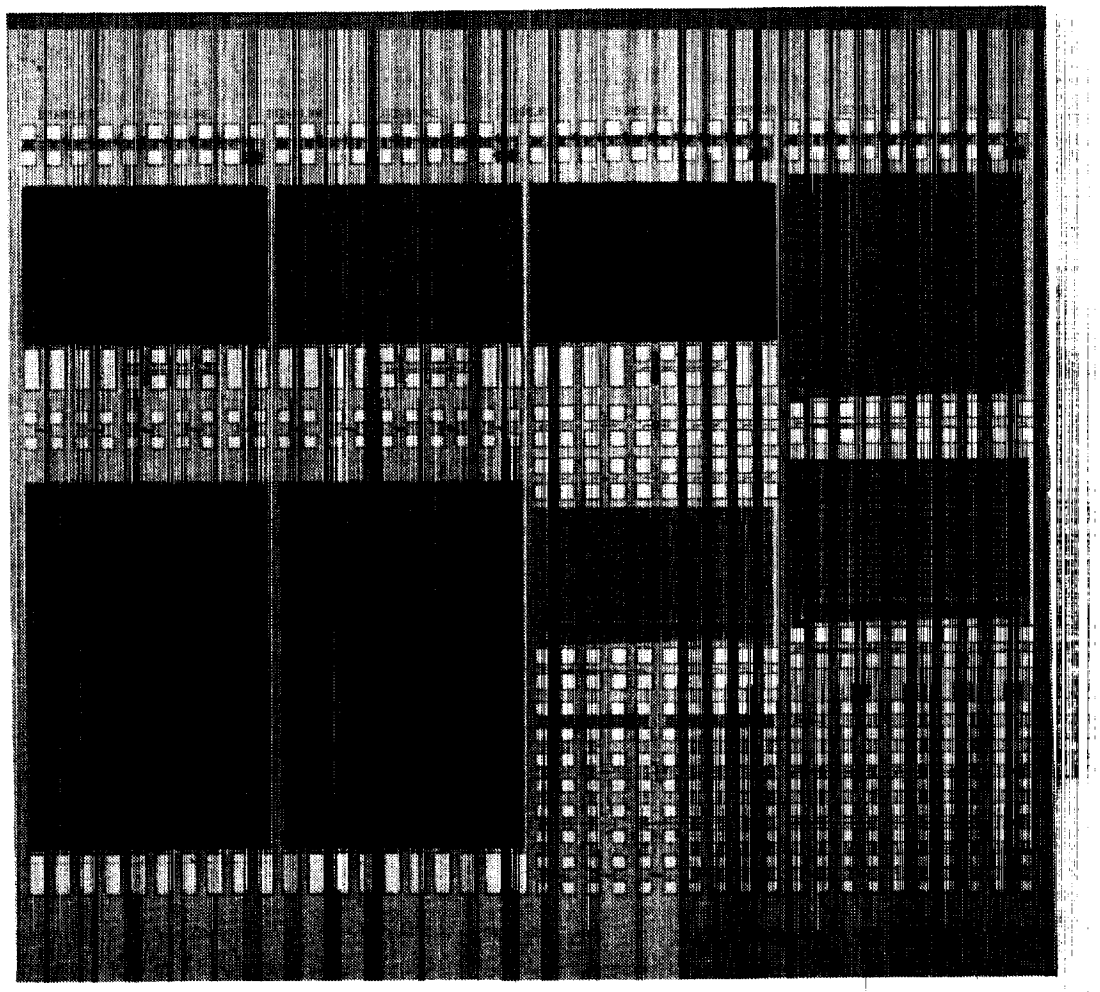
HDCC12-7a

MOSIS RUN N06J COST SUMMARY

PROJECT	SIZE	QUANTITY	COST ($)
EMCHIP	18.18 sqmm	50	8,364.00
SRAM10	10.26 sqmm	50	6,720.00
TIDCHIP	7.48 sqmm	50	5,439.00
FAULT CHIP/PM	30.75 sqmm	75	14,146.00
SRAM9 (LL)	8.58 sqmm	75	5,704.00
HDCC (ASIC)	71.6 sqmm	50	35,200.00
STD CELL (ASIC)	6.28 sqmm	50	4,888.00

TEST CHIP TOTAL COST = $40,088.00
ASOF TOTAL COST = $40,373.00
FABRICATION RUN N06J TOTAL COST = $80,461.00

JPL 1.6μm n-WELL CMOS/BULK FAULT CHIP AND PROCESS MONITOR



CHIP SIZE = 6.9 mm x 5.9 mm

HDCC12-8a

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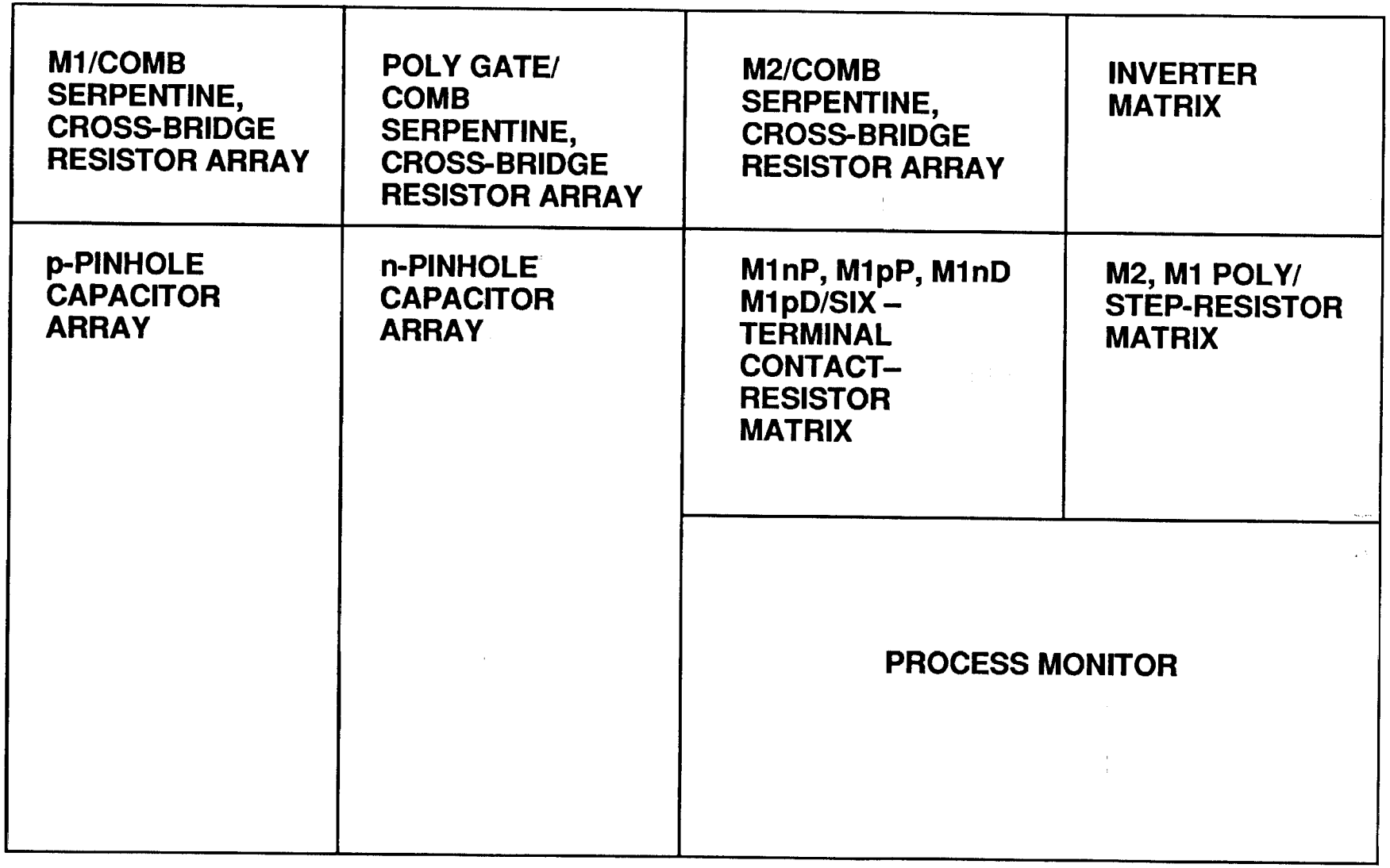
FAULT CHIP FLOOR PLAN



HDCC12-8b

FAULT CHIP DESCRIPTION

THE FAULT CHIP IS A SET OF TEST STRUCTURES WHICH PROVIDE STATISTICS ON VLSI DEFECT DENSITIES AND DISTRIBUTIONS OF COMPONENT CHARACTERISTICS.

BOTH THE DENSITIES OF PARTICULAR TYPES OF COMPONENT DEFECTS AND THE DISTRIBUTIONS OF COMPONENT CHARACTERISTICS GIVE INSIGHT INTO THE FACTORS AFFECTING ASIC YIELD.

EXAMPLES OF DEFECT DENSITIES MEASURED ON THE FAULT CHIP ARE:

- SHORTS BETWEEN LINES OF INTERCONNECT FOR PARTICULAR MATERIAL LAYERS
- BREAKS IN INTERCONNECT DUE TO POOR PROCESSING
- PINHOLES IN THE GATE OXIDE

EXAMPLES OF MEASURED DISTRIBUTIONS OF COMPONENT CHARACTERISTICS INCLUDE:

- QUALITY OF INTERLAYER CONTACTS
- INVERTER CIRCUIT CHARACTERISTICS
- QUALITY OF INTERCONNECT LINES GOING OVER THREE DIMENSIONAL STRUCTURES (STEP COVERAGE)

HDCC12-9a

FAULT CHIP SPECIFICATIONS

Table 1: Defect Density Test Structures. Analysis Determines Elements/Defect.

STRUCTURE	DEFECT	ELEMENT	ELEMENTS/SUBARRAY
p-Pinhole Array Capacitor	Gate-Oxide Pinhole	Transistor	18564/27608/57596/117096
n-Pinhole Array Capacitor	Gate-Oxide Pinhole	Transistor	18564/27608/57596/117096
p-Pinhole Array Capacitor	pPoly-Metal1 Pinhole	Overlap Length [μm]	89076/132472/27364/561864
n-Pinhole Array Capacitor	nPoly-Metal1 Pinhole	Overlap Length [μm]	89076/132472/27364/561864
Comb/Serpentine/Cross-Bridge	Poly-Poly Short	Adjacent Length [μm]	79925/159850
Comb/Serpentine/Cross-Bridge	Metal1-Metal1 Short	Adjacent Length [μm]	51868/105731
Comb/Serpentine/Cross-Bridge	Metal2-Metal2 Short	Adjacent Length [μm]	43888/89772
Comb/Serpentine/Cross-Bridge	Poly Wire Open	Step [4.8 μm / step]	16480/32960
Comb/Serpentine/Cross-Bridge	Metal1 Wire Open	Step [4.8 μm / step]	9152/18656
Comb/Serpentine/Cross-Bridge	Metal2 Wire Open	Step [4.8 μm / step]	6732/13770

Table 2: Parameter Variability Matrix Structures. Analysis Determines Parameter Distributions, and Calculates Probability of Parameter Exceeding Acceptable Range.

STRUCTURE	PARAMETER	ELEMENTS
6-Terminal Contact Matrix	Metal1-pPoly Contact Resistance	82
6-Terminal Contact Matrix	Metal1-nPolyContact Resistance	82
6-Terminal Contact Matrix	Metal1-pDiff Contact Resistance	82
6-Terminal Contact Matrix	Metal1-nDiff Contact Resistance	82
Linewidth/Step Matrix	Poly Linewidth	216
Linewidth/Step Matrix	Metal1 Linewidth	216
Linewidth/Step Matrix	Metal2 Linewidth	216
Inverter Matrix	V_{Tinv}, V_{Low}, V_{High}, GAIN	484

FAULT CHIP TEST RESULTS

1.6-μm CMOS/BULK n-WELL PROCESS (N06J)

CHIP PARAMETER VARIABILITY ANALYSIS (RUN NO. N06J)

Parameter	(dimension)	Average Value	Average of Standard Deviation		Points Included/Total
6-Terminal Contact Matrix: 49 of 60 matrix structures are included.				Contact Resist. %	
Contact size = 1.6μm x 1.6μm					
p-Poly Contact resistance	(Ohms)	16.3	1.63	10.00	3884/3884
n-Poly Contact resistance	(Ohms)	6.1	0.73	11.90	3936/3936
p-Diff Contact resistance	(Ohms)	17.5	0.27	1.54	3992/3992
n-Diff Contact resistance	(Ohms)	25.9	2.58	9.96	3882/3882
Linewidth/Step Matrix: 20 of 71 matrix structures are included.				Step Resist. %	
Metal1 Linewidth, down	(2.4um)	2.27	0.032		1440/1440
Metal1 Linewidth, up	(2.4um)	2.39	0.038		1438/1440
Metal1 Linewidth, step	(2.4um)	2.26	0.065	1.57	1404/1440
Metal2 Linewidth, down	(2.4um)	2.27	0.038		1440/1440
Metal2 Linewidth, up	(2.4um)	2.36	0.043		1440/1440
Metal2 Linewidth, step	(2.4um)	2.24	0.045	1.69	1440/1440
p-Poly Linewidth, down	(1.6um)	1.36	0.036		1440/1440
p-Poly Linewidth, up	(1.6um)	1.39	0.036		1440/1440
p-Poly Linewidth, step	(1.6um)	1.32	0.039	2.05	1440/1440
Inverter Matrix: 66 of 71 matrix structures are included.					
W_n / L_n = 2.4μm/1.6μm, W_p / L_p = 2.4μm/1.6μm					
VTinv	(Volts)	1.99	0.008		5808/5808
Vhigh	(Volts)	5.00	0.000		5808/5808
Vlow	(mVolts)	1.41	0.157		5808/5808
GAIN		17.64	0.549		5808/5808
NOISE MARGIN	(Volts)	1.88	0.008		5808/5808

Contact Resist. % = (Average of Standard Deviation) / (Average Value)

$$\text{Step Resist. \%} = \frac{1}{2}\left(\frac{\text{Width}_{down}}{\text{Width}_{step}} - \left(\frac{\text{Length}_{up}\text{Width}_{down}}{\text{Length}_{total}\text{Width}_{up}} + \frac{\text{Length}_{down}}{\text{Length}_{total}}\right)\right)$$

HDCC1210a

FAULT CHIP TEST RESULTS

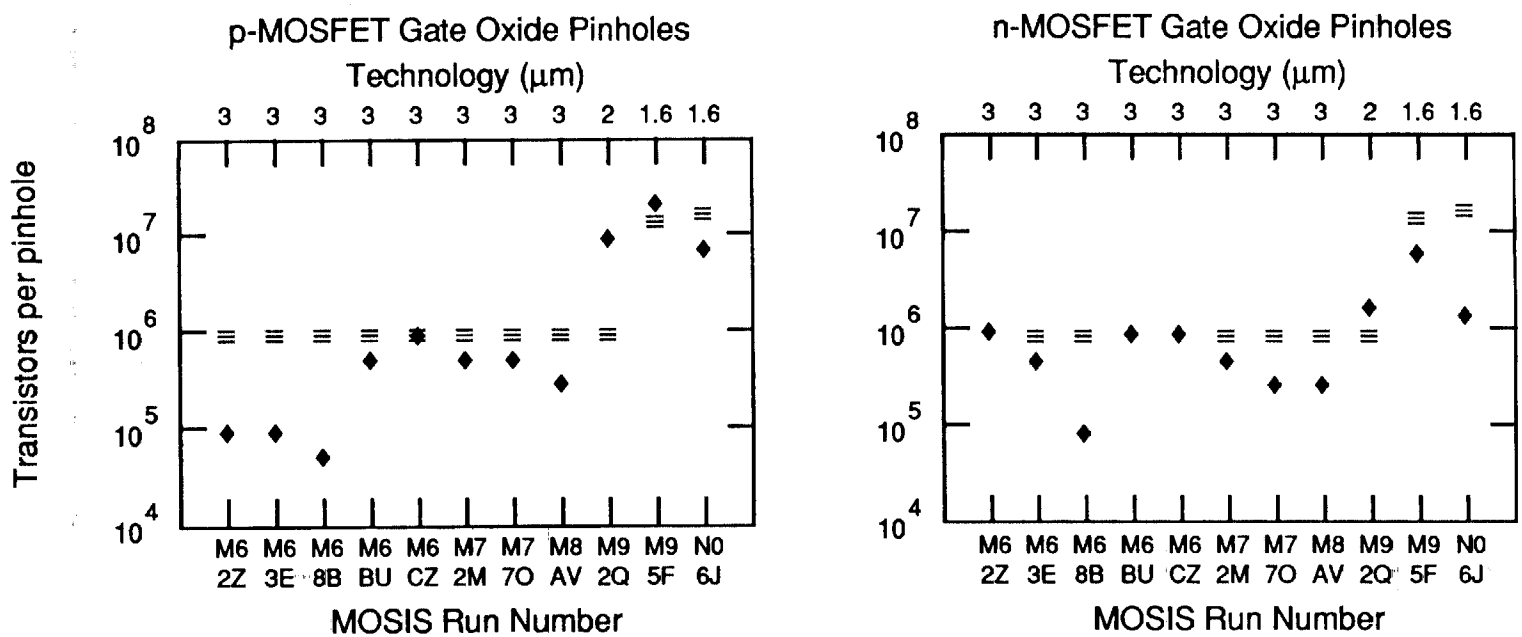
1.6-µm CMOS/BULK n-WELL PROCESS (N06J)

SUBARRAY DEFECT ANALYSIS

Defect Type	E-Value (Elements/Defect)	Standard Deviation	Subarrays #Bad/Total	Total #Elements	Element
Comb Resistor:					
Metal1-Metal1 Shorts	> 7.00 E+6	-	0/171	17966286	length (1 µm)
Metal2-Metal2 Shorts	1.75 E+7	1.37 E+7	1/171	15237240	length (1 µm)
Poly-Poly Shorts	1.58 E+7	6.84 E+6	2/171	27334350	length (1 µm)
Serpentine Resistor:					
Metal1 Wire Opens	> 8.96 E+5	-	0/114	1604094	step (5.6 µm)
Metal2 Wire Opens	> 6.65 E+5	-	0/114	1190331	step (6.4 µm)
Poly Wire Opens	4.70 E+6	4.70 E+6	1/114	2847321	step (4.8 µm)
p-PAC:					
Metal1-Poly Shorts	2.6 E+8	6.1 E+8	1/284	75244096	length (1 µm)
Gate Oxide Defects	9.1 E+6	4.6 E+6	3/284	15681344	transistor
n-PAC:					
Metal1-Poly Shorts	> 3.2 E+7	-	0/284	75244096	length (1 µm)
Gate Oxide Defects	1.6 E+6	3.4 E+5	10/284	15681344	transistor

HDCC1210b

CMOS GATE OXIDE SHORTS



♦ Transistors per pinhole
≡ Estimated Upper Limit of Measurement

MOSIS Run N06J is comparable to fabrication run M92Q

HDCC12-11a

INVERTER MATRIX PARAMETER VARIATIONS

Threshold Voltage Analysis:

$$VT_{inv} = \frac{VDD + \sqrt{\beta_r} \cdot VT_n - |VT_p|}{1 + \sqrt{\beta_r}}$$

Where $\beta_r = \beta_n / \beta_p$, $\beta = KP \cdot \frac{W_e}{L_e}$, VT_{inv} is the threshold voltage, W_e and L_e are the effective channel width and length, respectively. From P_oE and $\beta_r = 1$:

$$\delta VT_{inv}^2 = \frac{1}{4}\left[\delta VT_n^2 + \delta VT_p^2 + \left[\frac{VDD - VT_n - |VT_p|}{4}\delta\beta_r\right]^2\right]$$

$$\left[\frac{\delta\beta_r}{\beta_r}\right]^2 = \left[\frac{\delta W}{W_{en}}\right]^2 + \left[\frac{\delta L}{L_{en}}\right]^2 + \left[\frac{\delta W}{W_{ep}}\right]^2 + \left[\frac{\delta L}{L_{ep}}\right]^2$$

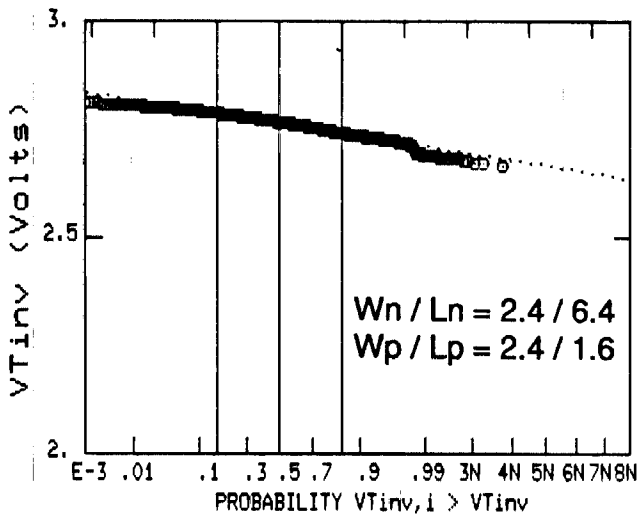
This shows the dependence of δVT_{inv} on MOSFET threshold voltages and dimensions. Note that δVT_{inv} is as low as 2 mV.

Sample size = 484 inverters/chip. Dimensions in µm.

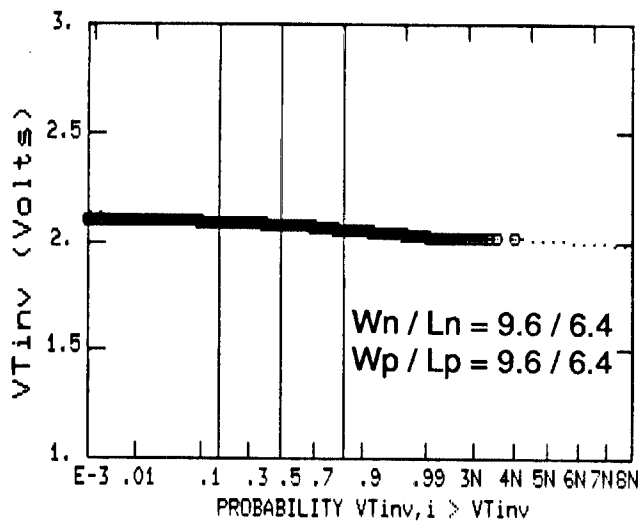
Sample Data from chip (2,7)

$\frac{W_n}{L_n}$	$\frac{W_p}{L_p}$	VT_{inv} (Volts)
$\frac{2.4}{1.6}$	$\frac{9.6}{1.6}$	2.86±0.008
$\frac{2.4}{1.6}$	$\frac{2.4}{1.6}$	2.00±0.008
$\frac{9.6}{6.4}$	$\frac{9.6}{6.4}$	2.08±0.002
$\frac{2.4}{6.4}$	$\frac{9.6}{1.6}$	3.50±0.006
$\frac{2.4}{6.4}$	$\frac{2.4}{1.6}$	2.76±0.008
$\frac{9.6}{1.6}$	$\frac{2.4}{6.4}$	1.09±0.003
$\frac{9.6}{1.6}$	$\frac{2.4}{1.6}$	1.42±0.004
$\frac{2.4}{1.6}$	$\frac{2.4}{6.4}$	1.42±0.006

INVERTER MATRIX VOLTAGE THRESHOLD DISTRIBUTION



Sample Size = 2810



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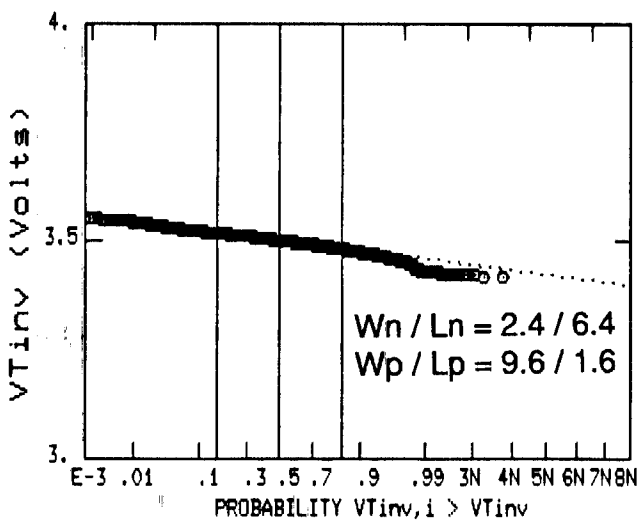

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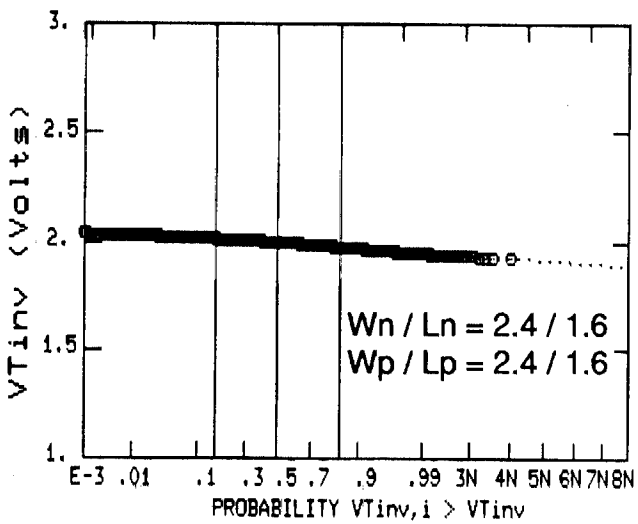

Sample Size = 5598

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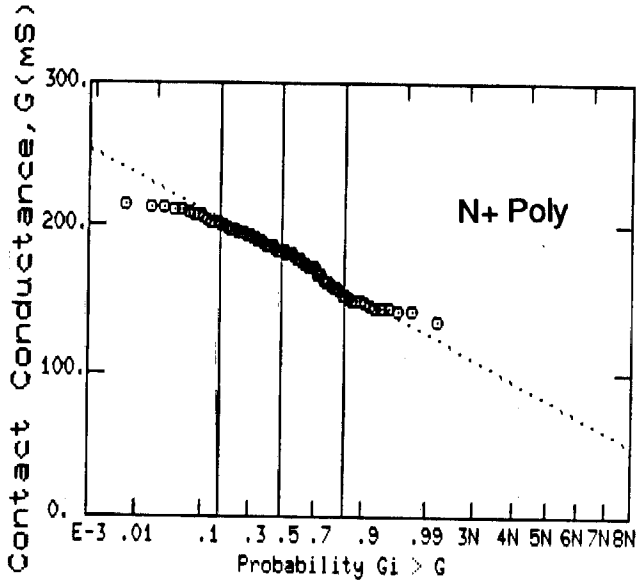
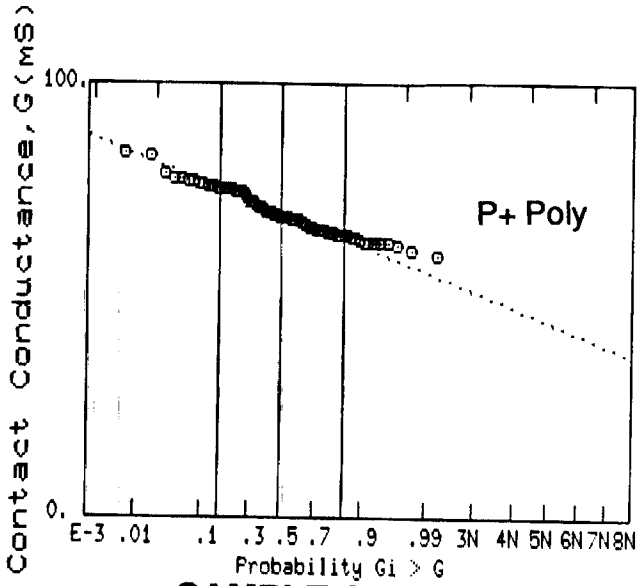
CONTACT MATRIX CONDUCTANCE



SAMPLE SIZE = 82



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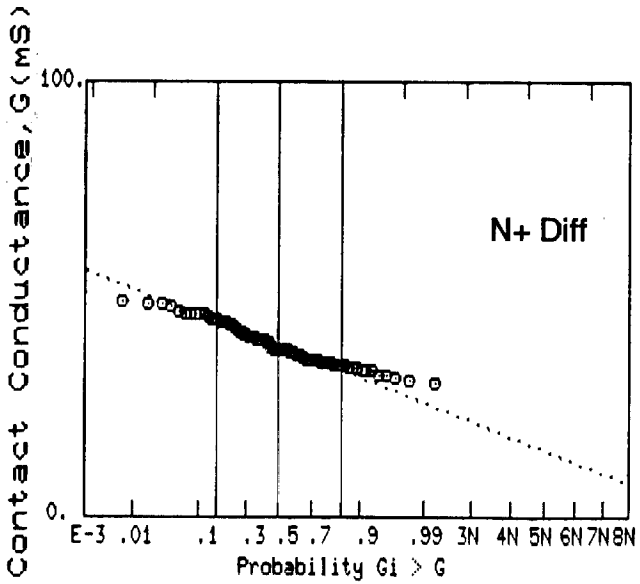

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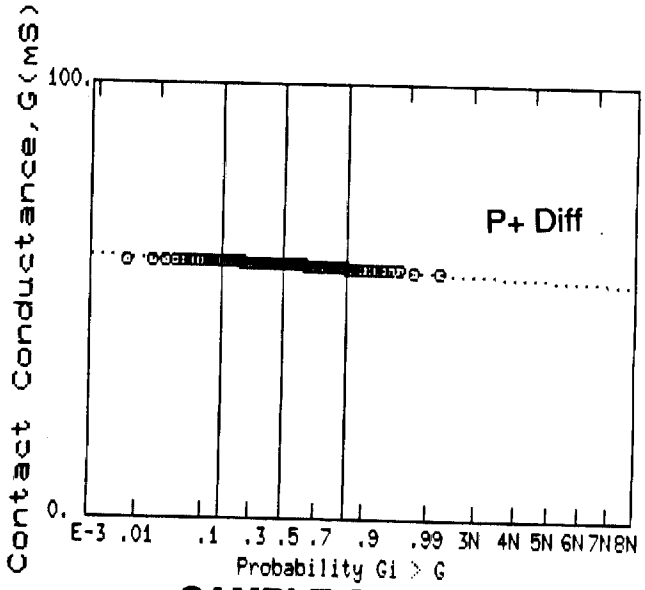

SAMPLE SIZE = 82

HDCC12-12b

FAULT CHIP CONCLUSIONS

- Found 15 meters of unbroken, unshorted metal-1 wire. Found 1 short in 10 meters of metal-2. Found 2 shorts and 1 open at one site in 25 meters of poly. Defective sites will be submitted for failure analysis.
- Found 13 oxide shorts in 30 million transistors.
- Found smallest inverter threshold voltage standard deviation at 2 mV.
- Corroborated Process Monitor findings that n+ diffusion contact conductances had the widest distribution and the probability of an open contact of this type is less than 6 nines. The p+ diffusion contact had the tightest statistical variation.

HDCC12-13a

HDCC12-13b

PROCESS MONITOR DESCRIPTION

THE PROCESS MONITOR CHIP IS A SET OF TEST STRUCTURES WHICH PROVIDE IMPORTANT PROCESS AND DEVICE PARAMETERS. BY PERFORMING ELECTRICAL TESTING OF SPECIFIC STRUCTURES, OVER THIRTY PROCESS PARAMETERS CAN BE COLLECTED. THESE PARAMETERS CHARACTERIZE THE QUALITY OF INTERCONNECTS, DIELECTRICS, CONTACTS, TRANSISTORS, AND INVERTERS.

HDCC1244a

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JPL

PROCESS MONITOR FLOOR PLAN AND SPECIFICATION

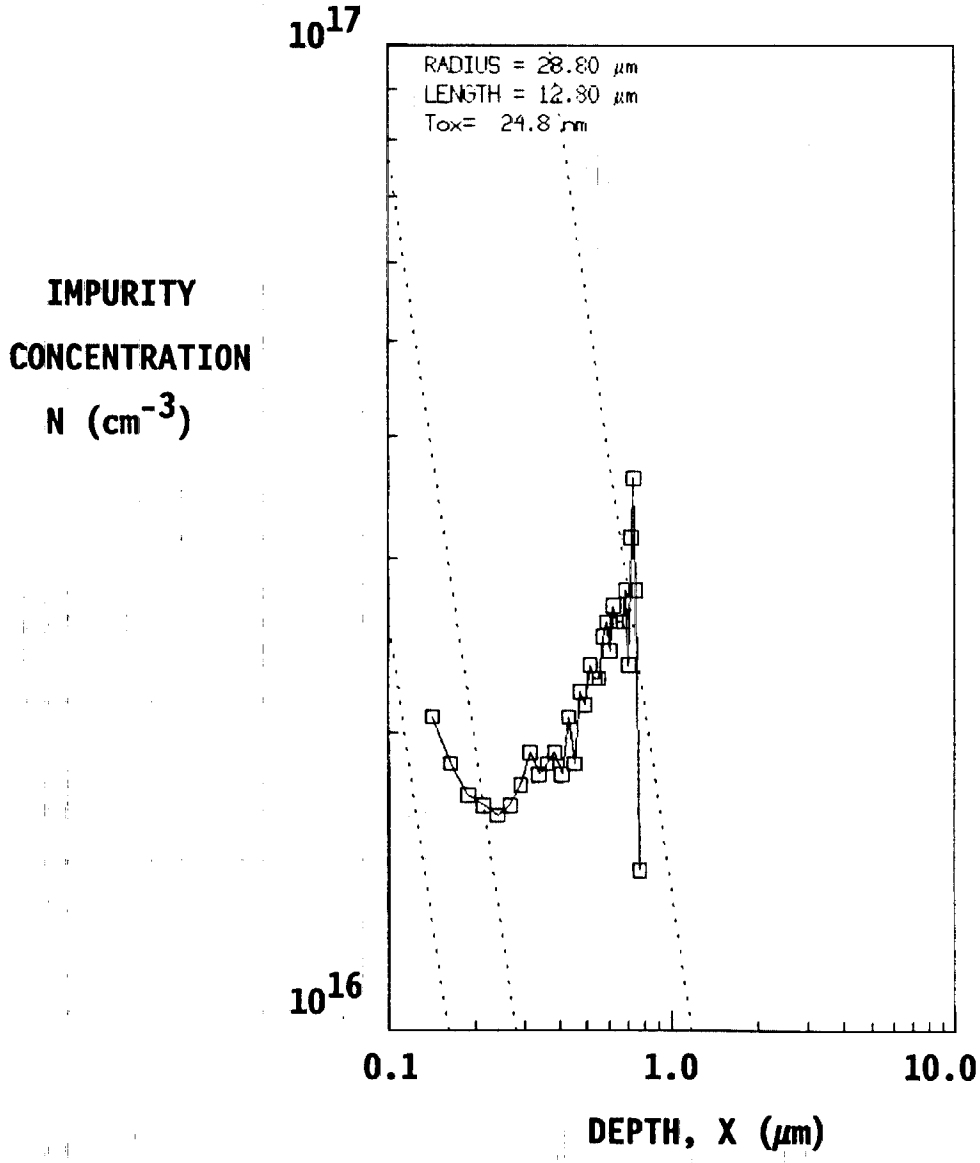
n-RCAP W = 1360 L = 3.2			p-RCAP W = 1360 L = 3.2		INV (W/L)n = 2.4/1.6 (W/L)p = 7.2/1.6	p-FETCAP R = 28.8 L = 3.2	n-FETCAP R = 28.8 L = 3.2	p-FETCAP R = 28.8 L = 12.8	p-FETCAP R = 28.8 L = 12.8
M1nP/CR 1.6x1.6	M1pP/CR 1.6x1.6	M1nD/CR 1.6x1.6	M1pD/CR 1.6x1.6	M1M2/CR 1.6x1.6	M1/SXBR WB = 7.2, LB = 120 WS = 2.4, LS = 160		M2/SXBR WB = 8.0, LB = 120 WS = 3.2, LS = 160		p-M1FOX W = 8.0 L = 2.4
n+P/SXBR WB = 4.8, LB = 120 WB = 1.6, LS = 160		p+P/SXBR WB = 4.8, LS = 120 WS = 1.6, LS = 160		n-P/FOX W = 8.0 L = 2.4	n+D/SXBR WB = 7.2, LB = 120 WS = 2.4, LS = 160		p+D/SXBR WB = 7.2, LB = 120 WS = 2.4, LS = 160		p-PFOX W = 8.0 L = 2.4
n-MOSFET (W/L)					p-MOSFET (W/L)				
2.4/1.6	7.2/1.6	7.2/4.8	2.4/4.8	4.8/3.2	2.4/1.6	7.2/1.6	7.2/4.8	2.4/4.8	4.8/3.2

DIMENSIONS IN μm
MOSFET: GATE-OXIDE TRANSISTOR
SXBR: SPLIT-CROSS-BRIDGE RESISTOR
CR: CONTACT RESISTOR
RCAP: RACETRACK CAPACITOR
FETCAP: TRANSISTOR CAPACITOR
INV: INVERTER

M1: METAL 1, M2 = METAL 2, p-POLY, D = DIFFUSION (INPLANT), p=p-TYPE, n=n-TYPE

HDCC12-14b

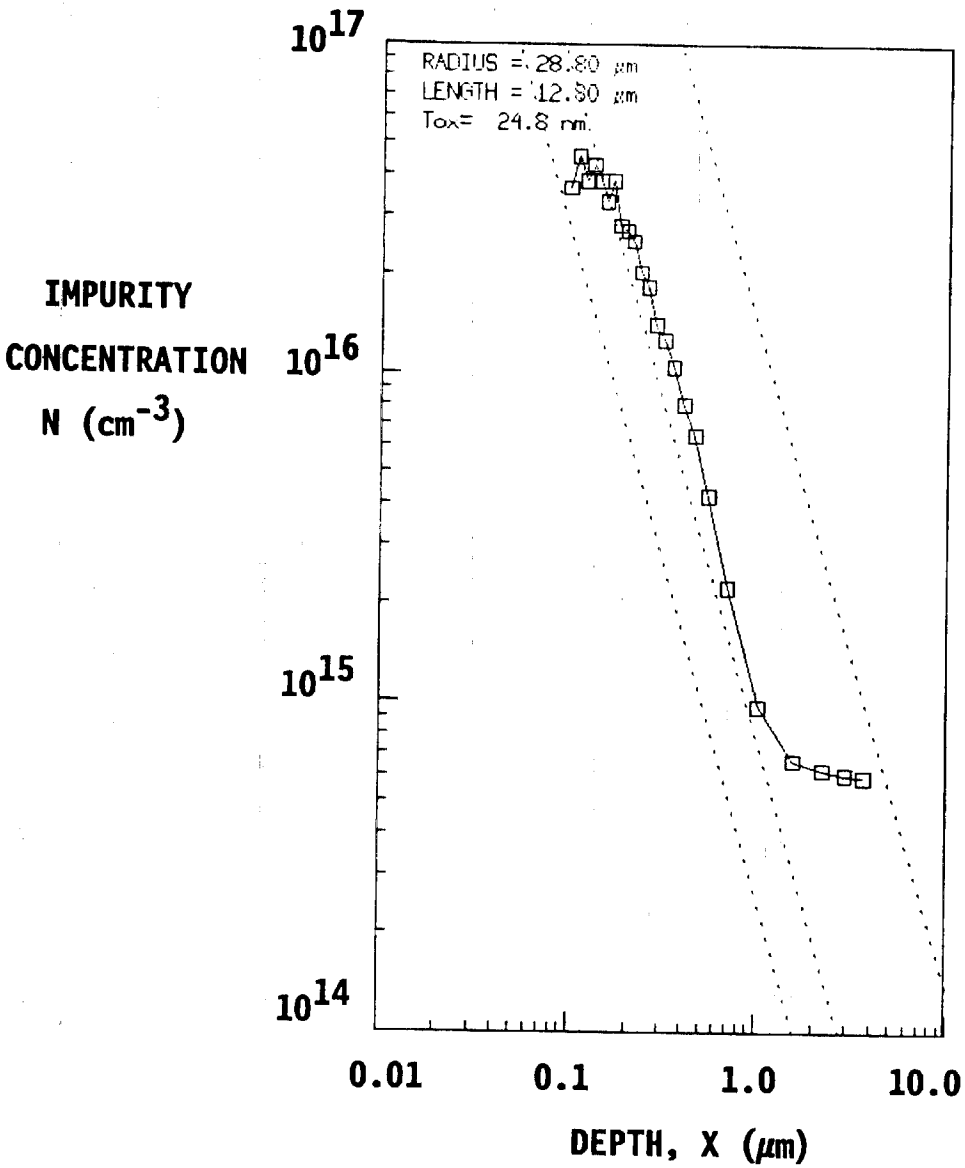
DOPANT PROFILE OF p-MOSFET (N06J)



MOSFET DONUT
L = 12.8 μm
R = 28.8 μm
ID = 1 μA
Tox = 24.8 nm
BACKGROUND DOPING
n-TYPE
$N_d = 1.8 \times 10^{16}$ (cm^{-3})

HDCC12-15a

DOPANT PROFILE OF n-MOSFET (N06J)



MOSFET DONUT
L = 12.8 μm
R = 28.8 μm
ID = 1 μA
Tox = 24.8 nm

IMPLANTATION
p-TYPE
PEAK DOPING = 4×10^{16} (cm^{-3})
DEPTH = 0.12 μm

BACKGROUND DOPING
p-TYPE
$N_a = 6 \times 10^{14}$ (cm^{-3})

HDCC12-15b

PROCESS MONITOR (HDCC/NO6J)
$1.6 - \mu m$ n-WELL CMOS

MOSFET CAPACITOR Parameters	n-MOS Radius=28.8 μm Sample Size=78	p-MOS Radius=28.8 μm Sample Size=78	INVERTER Parameters	$(W/L)_n = 2.4/1.6\ \mu m/\mu m$ $(W/L)_p = 7.2/1.6\ \mu m/\mu m$ Sample Size=78
$\Delta Radius(\mu m)$	12.8, 3.2	12.8, 3.2	$V_{INV}(V)$	1.824 ± 0.021
$T_{ox}(nm)$	24.8 ± 0.31	25.5 ± 1.19	GAIN	15.04 ± 0.44
$C_{ox}(fF/\mu m^2)$	1.391 ± 0.017	1.358 ± 0.049	$V_H(V)$	5.0 ± 0.0
$C_{go}(fF/\mu m)$	0.0851 ± 0.0118	0.0947 ± 0.0141	$V_L(\mu V)$	38.0 ± 49.5
$\Delta L(\mu m)$	0.495 ± 0.043	0.475 ± 0.160	NM (V)	2.194 ± 0.023

LAYER	Split-cross-bridge resistor Sample size=79		Contact resistor, metal-1 to LAYER Sample size=79, Contact size $2.56\mu m^2$	
	Sheet resistance ($\Omega/\square$)	Width variation $\Delta W = W_{drawn} - W_{measure}$ (μm)	Contact resistance (Ω)	# of NINES
p+poly	27.85 ± 1.87	0.31 ± 0.03	16.93 ± 3.39	7.44
n+poly	25.62 ± 1.21	0.36 ± 0.03	6.60 ± 1.12	7.04
p+diff	134.7 ± 3.88	0.36 ± 0.05	19.41 ± 1.60	> 15
n+diff	66.59 ± 1.93	0.20 ± 0.04	31.22 ± 6.48	5.77
metal-1	0.055 ± 0.0011	0.027 ± 0.065	N/A	N/A
metal-2	0.0299 ± 0.0015	0.0056 ± 0.25	0.036 ± 0.0048	12.42

HDCC12-16a

PROCESS MONITOR MOSFET RESULTS (NO6J)

MOSFET PARAMETERS	n-MOS Sample Size= 33	p-MOS Sample Size= 70
$Nsub(cm^3)$	$2.01 \times 10^{16} \pm 1.31 \times 10^{15}(0.07\%)$	$1.53 \times 10^{16} \pm 4.94 \times 10^{14}(0.03\%)$
$2\Phi f(V)$	$0.731 \pm 0.003(0.00\%)$	$0.717 \pm 0.002(0.00\%)$
$KP(\mu A/V^2)$	$74.729 \pm 2.173(0.03\%)$	$28.807 \pm 0.566(0.02\%)$
$\Delta W(\mu m)$	$0.485 \pm 0.074(0.15\%)$	$0.780 \pm 0.035(0.04\%)$
$\Delta L(\mu m)$	$0.409 \pm 0.064(0.16\%)$	$0.139 \pm 0.028(0.20\%)$
$VTf_O(V)$	$0.844 \pm 0.031(0.04\%)$	$0.684 \pm 0.025(0.04\%)$
$VFB(V)$	$0.314 \pm 0.045(0.14\%)$	$-0.504 \pm 0.029(0.06\%)$
$\Gamma(\sqrt{V})$	$0.592 \pm 0.019(0.03\%)$	$0.530 \pm 0.009(0.02\%)$
$KLG(V * \mu m)$	$0.184 \pm 0.028(0.15\%)$	$0.172 \pm 0.025(0.14\%)$
$KWG(V * \mu m)$	$0.013 \pm 0.038(2.95\%)$	$0.189 \pm 0.024(0.13\%)$
$\delta_0(\sqrt{V})$	$0.252 \pm 0.022(0.09\%)$	$0.235 \pm 0.008(0.03\%)$
$KLD(\mu m)$	$0.556 \pm 0.044(0.08\%)$	$0.324 \pm 0.013(0.04\%)$
$KWD(\mu m)$	$0.067 \pm 0.041(0.61\%)$	$0.087 \pm 0.015(0.17\%)$
$\Theta_0(1/V)$	$0.062 \pm 0.021(0.34\%)$	$0.132 \pm 0.005(0.04\%)$
$KLT(\mu m/V)$	$0.047 \pm 0.027(0.58\%)$	$0.008 \pm 0.009(1.18\%)$
$KWT(\mu m/V)$	$0.082 \pm 0.062(0.76\%)$	$0.081 \pm 0.010(0.12\%)$
$\Theta_{b0}(1/V)$	$-0.008 \pm 0.021(2.67\%)$	$-0.089 \pm 0.002(0.02\%)$
$KLTB(\mu m/V)$	$-0.002 \pm 0.023(12.83\%)$	$0.019 \pm 0.004(0.20\%)$
$KWTB(\mu m/V)$	$-0.050 \pm 0.053(1.06\%)$	$-0.016 \pm 0.003(0.19\%)$
$\eta_0(1/V)$	$-0.051 \pm 0.033(0.65\%)$	$0.021 \pm 0.026(1.19\%)$
$KLH(\mu m/V)$	$0.011 \pm 0.034(3.21\%)$	$-0.039 \pm 0.016(0.42\%)$
$KWH(\mu m/V)$	$0.051 \pm 0.093(1.83\%)$	$0.006 \pm 0.016(2.44\%)$
$\epsilon_0(1/V)$	$0.083 \pm 0.030(0.36\%)$	$0.058 \pm 0.005(0.08\%)$
$KLE(\mu m/V)$	$0.493 \pm 0.040(0.08\%)$	$0.164 \pm 0.007(0.04\%)$
$KWE(\mu m/V)$	$0.029 \pm 0.098(3.33\%)$	$0.012 \pm 0.007(0.54\%)$
$\lambda_0(1/V)$	$0.006 \pm 0.003(0.50\%)$	$0.003 \pm 0.001(0.22\%)$
$KLL(\mu m/V)$	$0.059 \pm 0.005(0.09\%)$	$0.095 \pm 0.003(0.03\%)$
M_0	$0.783 \pm 0.059(0.07\%)$	$1.062 \pm 0.047(0.04\%)$
$Vit(V)$	$-0.079 \pm 0.021(0.27\%)$	$0.022 \pm 0.017(0.76\%)$
$\Gamma_M(\sqrt{V})$	$1.386 \pm 0.075(0.05\%)$	$1.189 \pm 0.115(0.10\%)$
$\Gamma_Z(\sqrt{V})$	$3.933 \pm 0.384(0.10\%)$	$4.490 \pm 0.337(0.08\%)$

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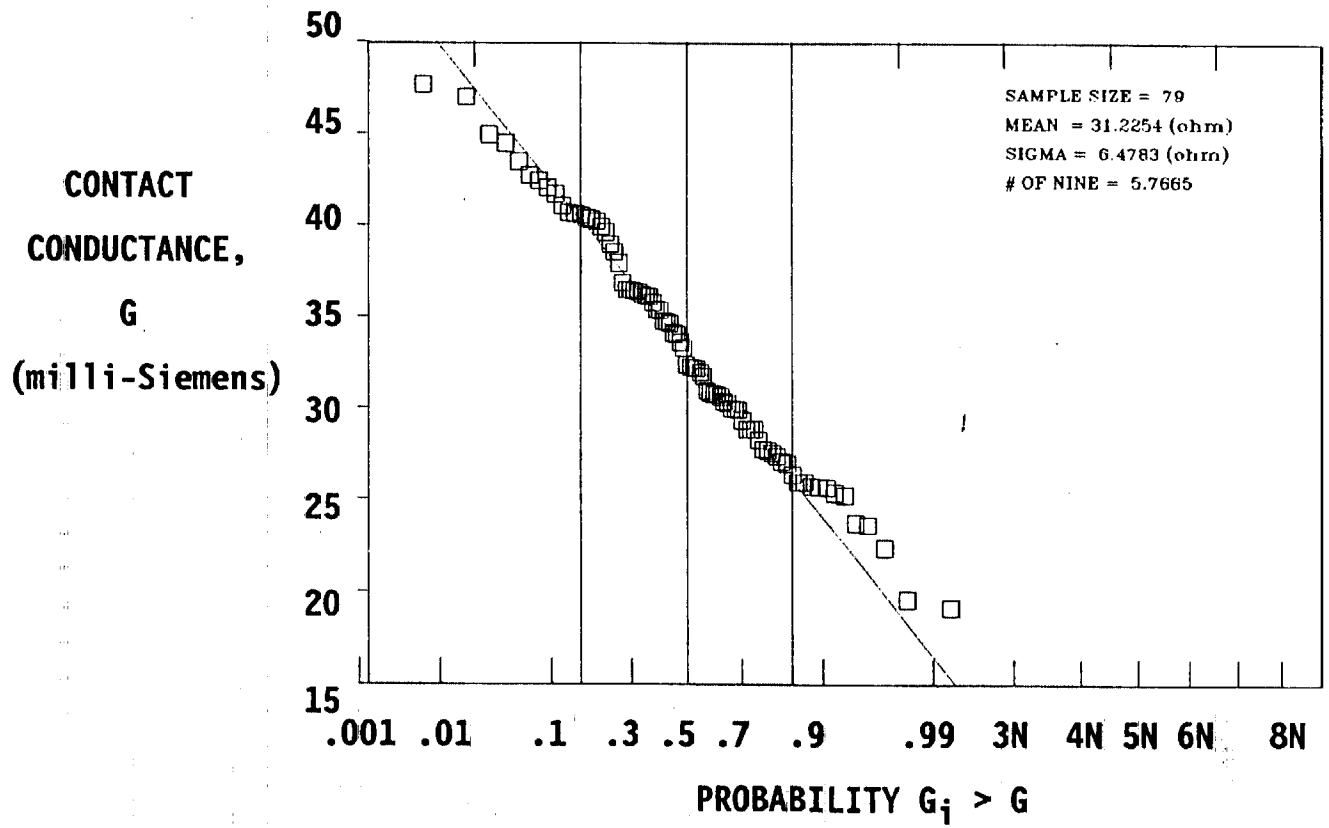
n+DIFF TO METAL-1 CONTACT RESISTANCE STAND-ALONE TEST STRUCTURES (RUN N06J TEST RESULTS)



HDCC12-17a

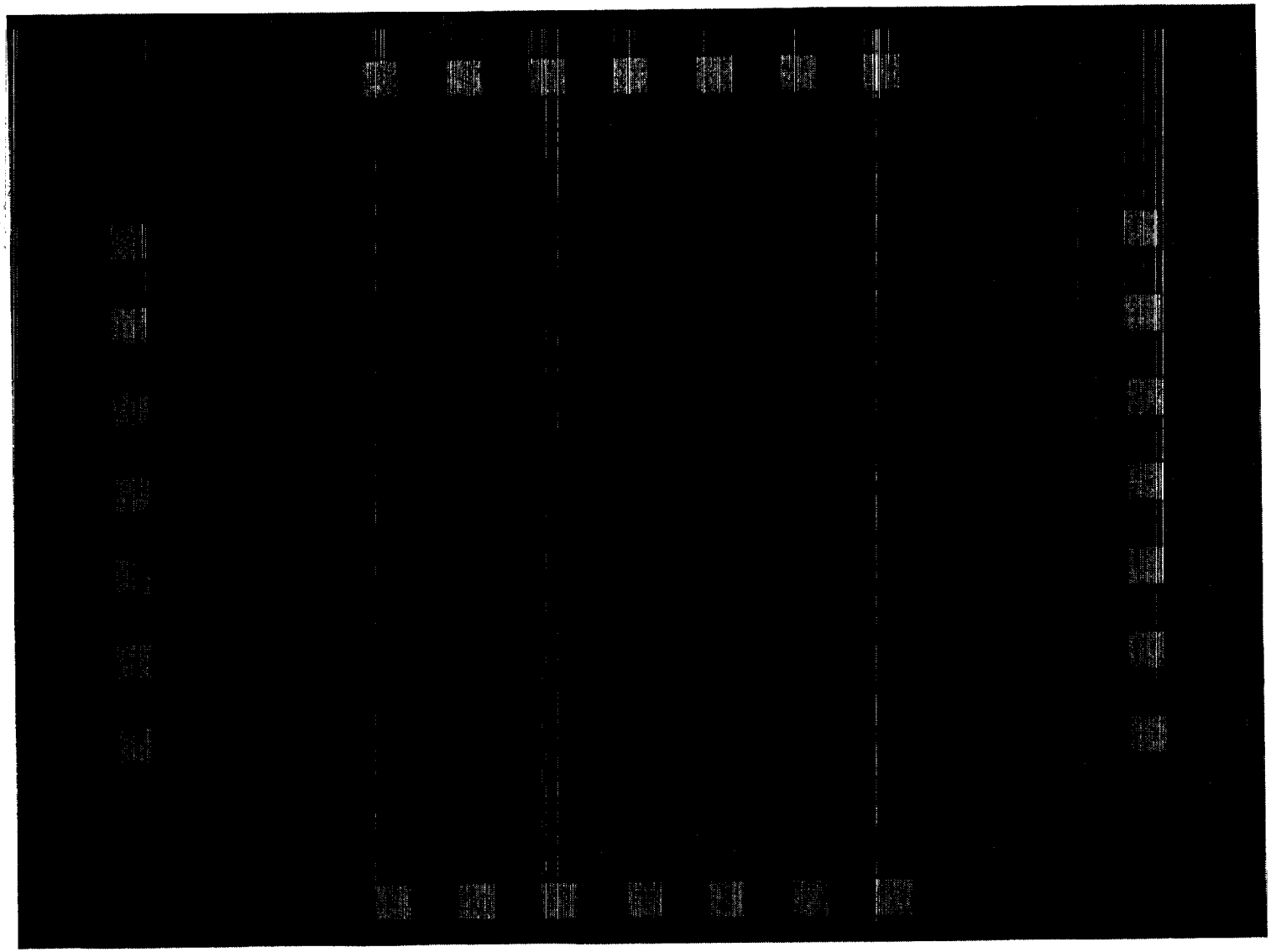
PROCESS MONITOR CONCLUSIONS

- ISSUE: THE PROBABILITY OF AN OPEN CONTACT FOR n+ DIFFUSION TO METAL 1 IS LESS THAN 6 NINES ACROSS THE ENTIRE WAFER LOT

- SIGNIFICANCE: OPEN CONTACTS WILL MOST PROBABLY CAUSE A "STUCK HIGH" CONDITION IN CMOS DIGITAL CIRCUITS

JPL

TOTAL IONIZING DOSE (TID) CHIP
1.6 μm n-WELL CMOS/BULK



HDCC12-18a

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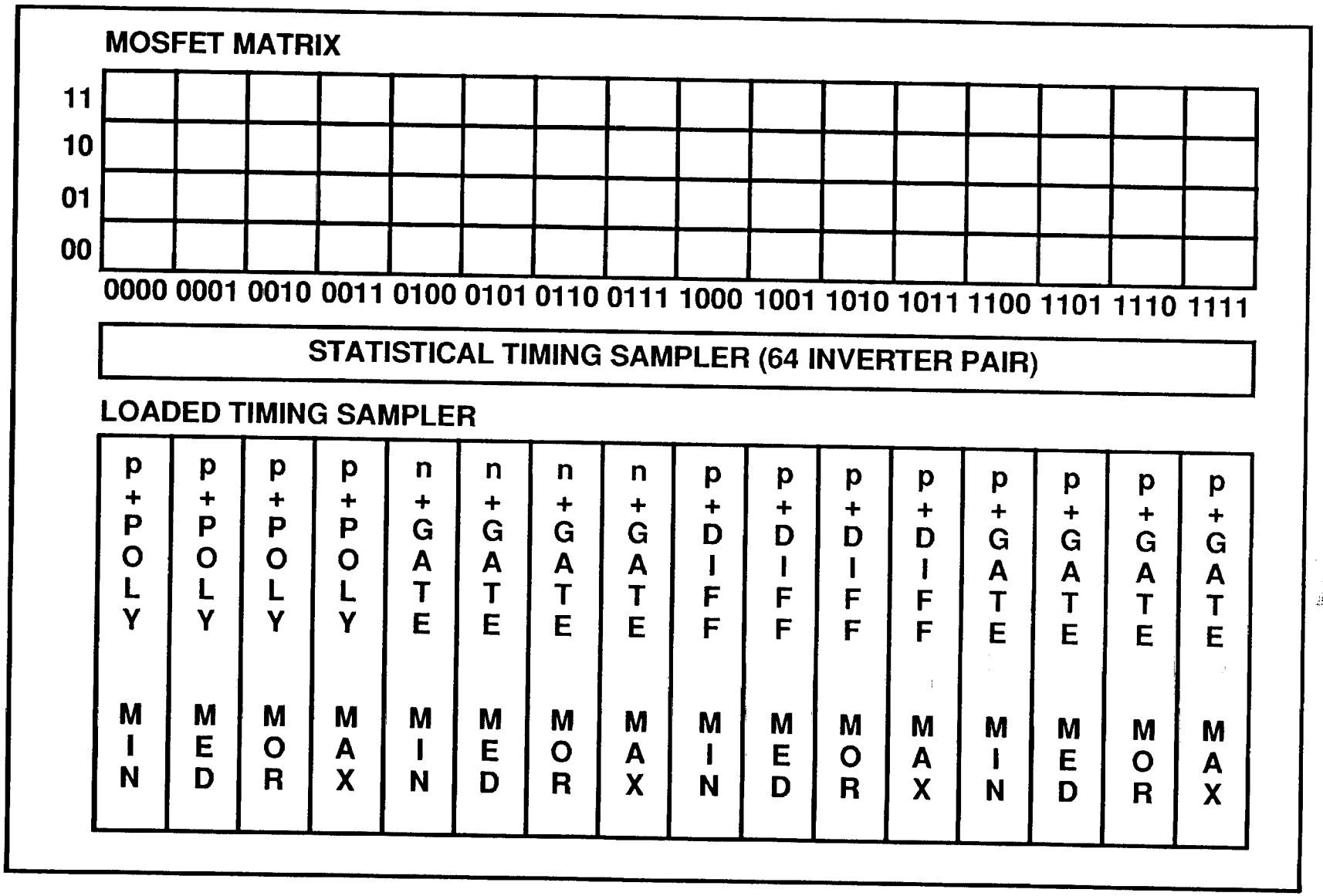
TID CHIP FLOOR PLAN



HDCC12-18b

TID CHIP DESCRIPTION

THE TID CHIP WAS DEVELOPED TO MONITOR THE EFFECTS OF RADIATION ON MOSFET PARAMETERS AND INVERTER PROPAGATION DELAY. THE CHIP WAS DESIGNED TO FLAG "WORST CASE" RADIATION-ANNEAL BIAS CONDITIONS. THE "WORST CASE" CONDITIONS ARE THOSE WHICH PRODUCE THE LARGEST PARAMETER SHIFTS.

HDCC12-19a

PM MOSFET AND TID CHIP MOSFET MATRIX RESULT (NO6J) COMPARISON

MOSFET PARAMETERS	PM, n-MOS Sample Size= 33	TID, n-MOS Sample Size= 39	PM, p-MOS Sample Size= 70	TID, p-MOS Sample Size= 40
$Nsub(cm^3)$	2.01×10^{16}	1.96×10^{16}	1.53×10^{16}	1.53×10^{16}
$2\Phi f(V)$	0.731	0.730	0.717	0.717
$KP(\mu A/V^2)$	74.729	75.436	28.807	29.161
$\Delta W(\mu m)$	0.485	0.405	0.780	0.556
$\Delta L(\mu m)$	0.409	0.408	0.139	0.149
$VTf_O(V)$	0.844	0.842	0.684	0.687
$VFB(V)$	0.314	0.345	−0.504	−0.556
$\Gamma(\sqrt{V})$	0.592	0.584	0.530	0.531
$KLG(V * \mu m)$	0.184	0.169	0.172	0.174
$KWG(V * \mu m)$	0.013	0.016	0.189	0.202
$\delta_0(\sqrt{V})$	0.252	0.254	0.235	0.223
$KLD(\mu m)$	0.556	0.562	0.324	0.303
$KWD(\mu m)$	0.067	0.090	0.087	0.089
$\Theta_0(1/V)$	0.062	0.052	0.132	0.134
$KLT(\mu m/V)$	0.047	0.038	0.008	0.016
$KWT(\mu m/V)$	0.082	0.057	0.081	0.091
$\Theta_{b0}(1/V)$	−0.008	−0.019	−0.089	−0.090
$KLTB(\mu m/V)$	−0.002	−0.003	0.019	0.019
$KWTB(\mu m/V)$	−0.050	−0.036	−0.016	−0.015
$\eta_0(1/V)$	−0.051	−0.034	0.021	0.061
$KLH(\mu m/V)$	0.011	0.043	−0.039	0.005
$KWH(\mu m/V)$	0.051	0.036	0.006	−0.004
$\epsilon_0(1/V)$	0.083	0.076	0.058	0.053
$KLE(\mu m/V)$	0.493	0.521	0.164	0.163
$KWE(\mu m/V)$	0.029	−0.006	0.012	0.010
$\lambda_0(1/V)$	0.006	0.006	0.003	0.003
$KLL(\mu m/V)$	0.059	0.059	0.095	0.093
M_0	0.783	0.887	1.062	1.216
$Vit(V)$	−0.079	−0.041	0.022	0.077
$\Gamma_M(\sqrt{V})$	1.386	1.242	1.189	1.117
$\Gamma_Z(\sqrt{V})$	3.933	3.903	4.490	4.409

HDCC12-19b

MOSFET MATRIX CELLS AS-DRAWN GEOMETRIES

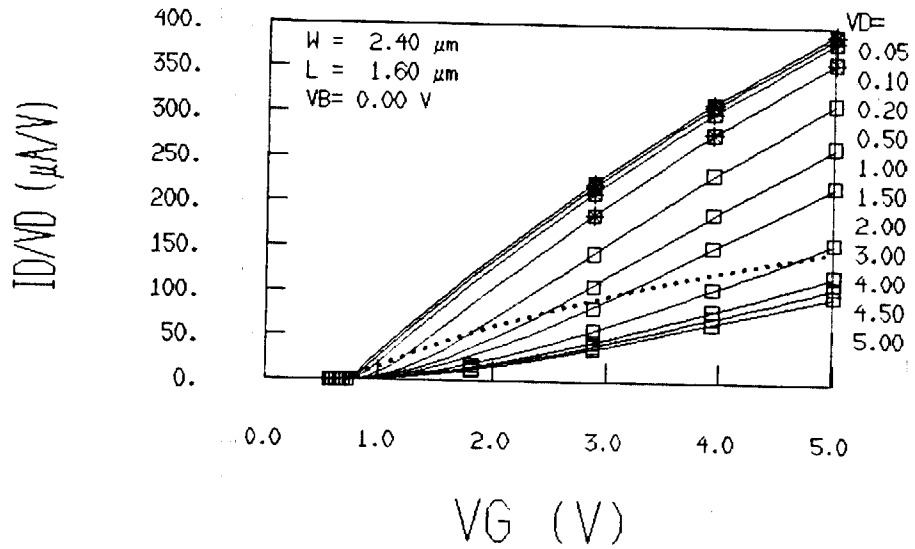
Row	Column (C_0, C_1, C_2, C_3), Cell size= channel width (μm)/channel length (μm)							
	0,0,0,0	0,0,0,1	0,0,1,0	0,0,1,1	0,1,0,0	0,1,0,1	0,1,1,0	0,1,1,1
R_1, R_0	p-MOS	p-MOS	p-MOS	p-MOS	p-MOS	p-MOS	p-MOS	p-MOS
1, 1 (V_{G4})	blank	$\frac{4.8}{1.6}$	$\frac{4.8}{3.2}$	$\frac{2.4}{1.2}$	$\frac{7.2}{4.8}$	$\frac{2.4}{4.8}$	$\frac{2.4}{1.6}$	$\frac{7.2}{1.6}$
1, 0 (V_{G3})	blank	$\frac{4.8}{1.6}$	$\frac{4.8}{3.2}$	$\frac{2.4}{1.2}$	$\frac{2.4}{4.8}$	$\frac{2.4}{1.6}$	$\frac{7.2}{1.6}$	$\frac{7.2}{4.8}$
0, 1 (V_{G2})	M1-FOX	$\frac{4.8}{1.6}$	$\frac{4.8}{3.2}$	$\frac{2.4}{1.2}$	$\frac{2.4}{1.6}$	$\frac{7.2}{1.6}$	$\frac{7.2}{4.8}$	$\frac{2.4}{4.8}$
0, 0 (V_{G1})	P-FOX	$\frac{4.8}{1.6}$	$\frac{4.8}{3.2}$	$\frac{2.4}{1.2}$	$\frac{7.2}{1.6}$	$\frac{7.2}{4.8}$	$\frac{2.4}{4.8}$	$\frac{2.4}{1.6}$

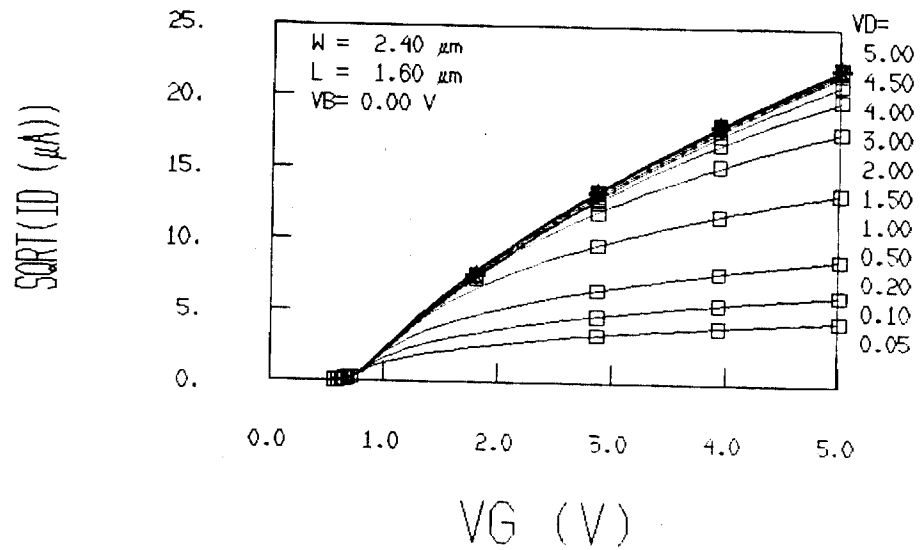
Row	Column (C_0, C_1, C_2, C_3), Cell size= channel width (μm)/channel length (μm)							
	1,0,0,0	1,0,0,1	1,0,1,0	1,0,1,1	1,1,0,0	1,1,0,1	1,1,1,0	1,1,1,1
R_1, R_0	n-MOS	n-MOS	n-MOS	n-MOS	n-MOS	n-MOS	n-MOS	n-MOS
1, 1 (V_{G4})	$\frac{7.2}{4.8}$	$\frac{2.4}{4.8}$	$\frac{2.4}{1.6}$	$\frac{7.2}{1.6}$	$\frac{4.8}{1.6}$	$\frac{4.8}{3.2}$	$\frac{2.4}{1.2}$	blank
1, 0 (V_{G3})	$\frac{2.4}{4.8}$	$\frac{2.4}{1.6}$	$\frac{7.2}{1.6}$	$\frac{7.2}{4.8}$	$\frac{4.8}{1.6}$	$\frac{4.8}{3.2}$	$\frac{2.4}{1.2}$	blank
0, 1 (V_{G2})	$\frac{2.4}{1.6}$	$\frac{7.2}{1.6}$	$\frac{7.2}{4.8}$	$\frac{2.4}{4.8}$	$\frac{4.8}{1.6}$	$\frac{4.8}{3.2}$	$\frac{2.4}{1.2}$	M1-FOX
0, 0 (V_{G1})	$\frac{7.2}{1.6}$	$\frac{7.2}{4.8}$	$\frac{2.4}{4.8}$	$\frac{2.4}{1.6}$	$\frac{4.8}{1.6}$	$\frac{4.8}{3.2}$	$\frac{2.4}{1.2}$	P-FOX

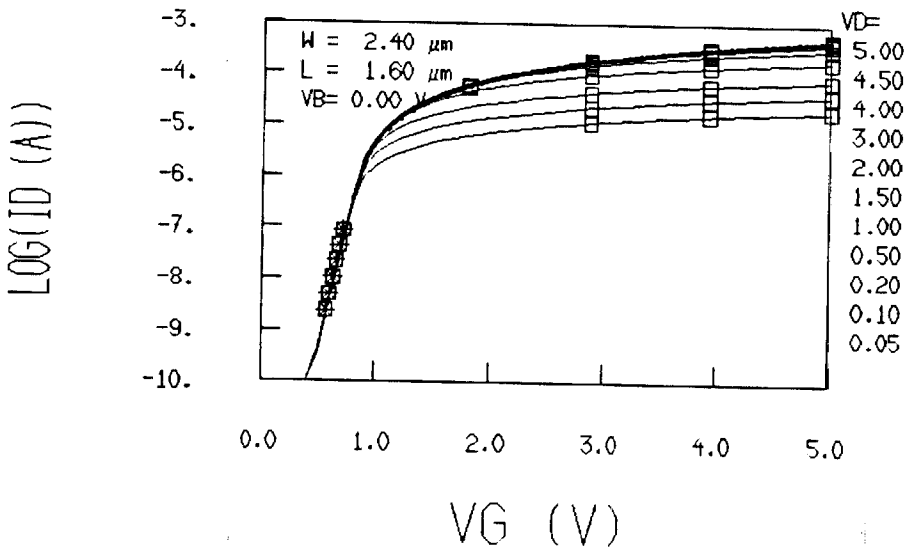
HDCC12-20a

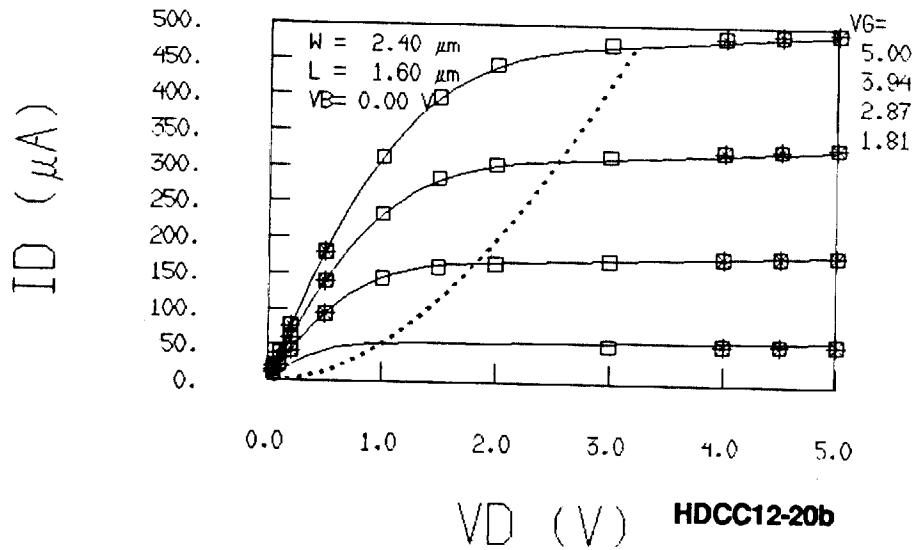
TID CHIP n-MOSFET RESULTS (HDCC/NO6J)

[SANG.NO6J.TID]C160N03000.019 CREATED:13-NOV-90 11:26:16
TID CHIP, NO6J RUN (HDCC), 1.6um CMOS n-well process
N-CH XT, IND. FIT, TEMP= 27.0 C, DOSE= 0.0 krad/Si









HDCC12-20b

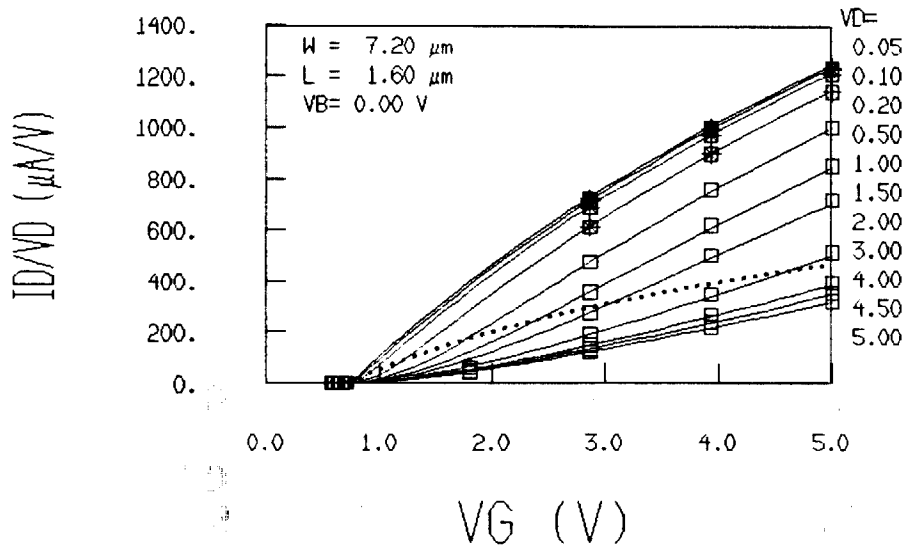
TID CHIP MOSFET MATRIX RESULTS (NO6J)

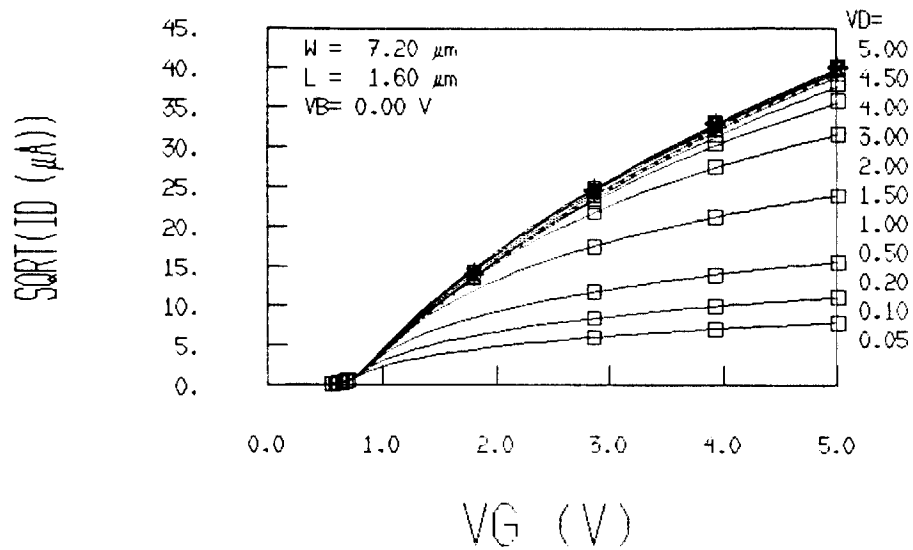
MOSFET PARAMETERS	n-MOS Sample Size= 39	p-MOS Sample Size= 40
$Nsub(cm^3)$	$1.96 \times 10^{16} \pm 1.23 \times 10^{15}(0.06\%)$	$1.53 \times 10^{16} \pm 4.08 \times 10^{14}(0.03\%)$
$2\Phi f(V)$	$0.730 \pm 0.003(0.00\%)$	$0.717 \pm 0.001(0.00\%)$
$KP(\mu A/V^2)$	$75.436 \pm 0.901(0.01\%)$	$29.161 \pm 0.543(0.02\%)$
$\Delta W(\mu m)$	$0.405 \pm 0.032(0.08\%)$	$0.556 \pm 0.025(0.05\%)$
$\Delta L(\mu m)$	$0.408 \pm 0.015(0.04\%)$	$0.149 \pm 0.022(0.15\%)$
$VTf_O(V)$	$0.842 \pm 0.016(0.02\%)$	$0.687 \pm 0.013(0.02\%)$
$VFB(V)$	$0.345 \pm 0.025(0.07\%)$	$-0.556 \pm 0.022(0.04\%)$
$\Gamma(\sqrt{V})$	$0.584 \pm 0.018(0.03\%)$	$0.531 \pm 0.007(0.01\%)$
$KLG(V * \mu m)$	$0.169 \pm 0.012(0.07\%)$	$0.174 \pm 0.018(0.11\%)$
$KWG(V * \mu m)$	$0.016 \pm 0.018(1.12\%)$	$0.202 \pm 0.020(0.10\%)$
$\delta_0(\sqrt{V})$	$0.254 \pm 0.010(0.04\%)$	$0.223 \pm 0.007(0.03\%)$
$KLD(\mu m)$	$0.562 \pm 0.010(0.02\%)$	$0.303 \pm 0.011(0.04\%)$
$KWD(\mu m)$	$0.090 \pm 0.018(0.20\%)$	$0.089 \pm 0.013(0.15\%)$
$\Theta_0(1/V)$	$0.052 \pm 0.001(0.03\%)$	$0.134 \pm 0.002(0.01\%)$
$KLT(\mu m/V)$	$0.038 \pm 0.002(0.05\%)$	$0.016 \pm 0.003(0.17\%)$
$KWT(\mu m/V)$	$0.057 \pm 0.003(0.05\%)$	$0.091 \pm 0.003(0.03\%)$
$\Theta_{b0}(1/V)$	$-0.019 \pm 0.002(0.10\%)$	$-0.090 \pm 0.002(0.02\%)$
$KLTB(\mu m/V)$	$-0.003 \pm 0.003(0.87\%)$	$0.019 \pm 0.003(0.18\%)$
$KWTB(\mu m/V)$	$-0.036 \pm 0.004(0.11\%)$	$-0.015 \pm 0.003(0.19\%)$
$\eta_0(1/V)$	$-0.034 \pm 0.005(0.14\%)$	$0.061 \pm 0.028(0.46\%)$
$KLH(\mu m/V)$	$0.043 \pm 0.007(0.15\%)$	$0.005 \pm 0.011(2.41\%)$
$KWH(\mu m/V)$	$0.036 \pm 0.008(0.21\%)$	$-0.004 \pm 0.012(3.22\%)$
$\epsilon_0(1/V)$	$0.076 \pm 0.006(0.07\%)$	$0.053 \pm 0.003(0.05\%)$
$KLE(\mu m/V)$	$0.521 \pm 0.009(0.02\%)$	$0.163 \pm 0.004(0.02\%)$
$KWE(\mu m/V)$	$-0.006 \pm 0.015(2.43\%)$	$0.010 \pm 0.006(0.58\%)$
$\lambda_0(1/V)$	$0.006 \pm 0.001(0.12\%)$	$0.003 \pm 0.000(0.14\%)$
$KLL(\mu m/V)$	$0.059 \pm 0.001(0.02\%)$	$0.093 \pm 0.001(0.01\%)$
M_0	$0.887 \pm 0.059(0.07\%)$	$1.216 \pm 0.040(0.03\%)$
$Vit(V)$	$-0.041 \pm 0.022(0.52\%)$	$0.077 \pm 0.014(0.19\%)$
$\Gamma_M(\sqrt{V})$	$1.242 \pm 0.104(0.08\%)$	$1.117 \pm 0.085(0.08\%)$
$\Gamma_Z(\sqrt{V})$	$3.903 \pm 0.374(0.10\%)$	$4.409 \pm 0.313(0.07\%)$

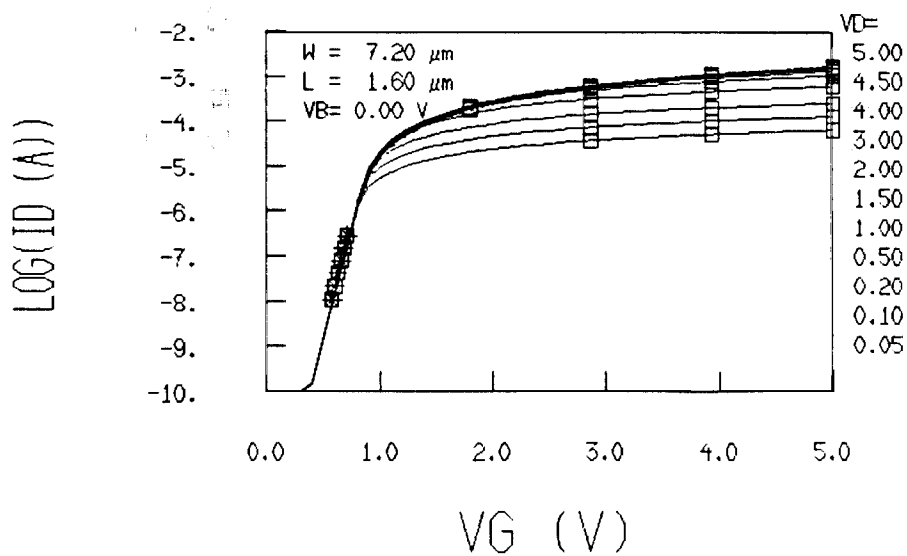
HDCC12-21a

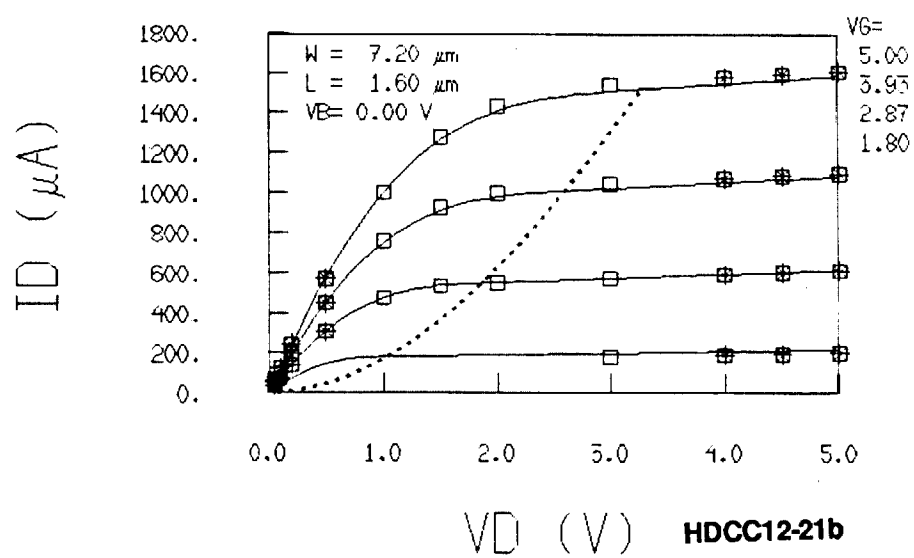
TID CHIP n-MOSFET RESULTS (HDCC/NO6J)

[SANG.NO6J.TID]C160N03000.019 CREATED:13-NOV-90 11:26:16
TID CHIP, NO6J RUN (HDCC), 1.6um CMOS n-well process
N-CH XT, IND. FIT, TEMP= 27.0 C, DOSE= 0.0 krad/Si









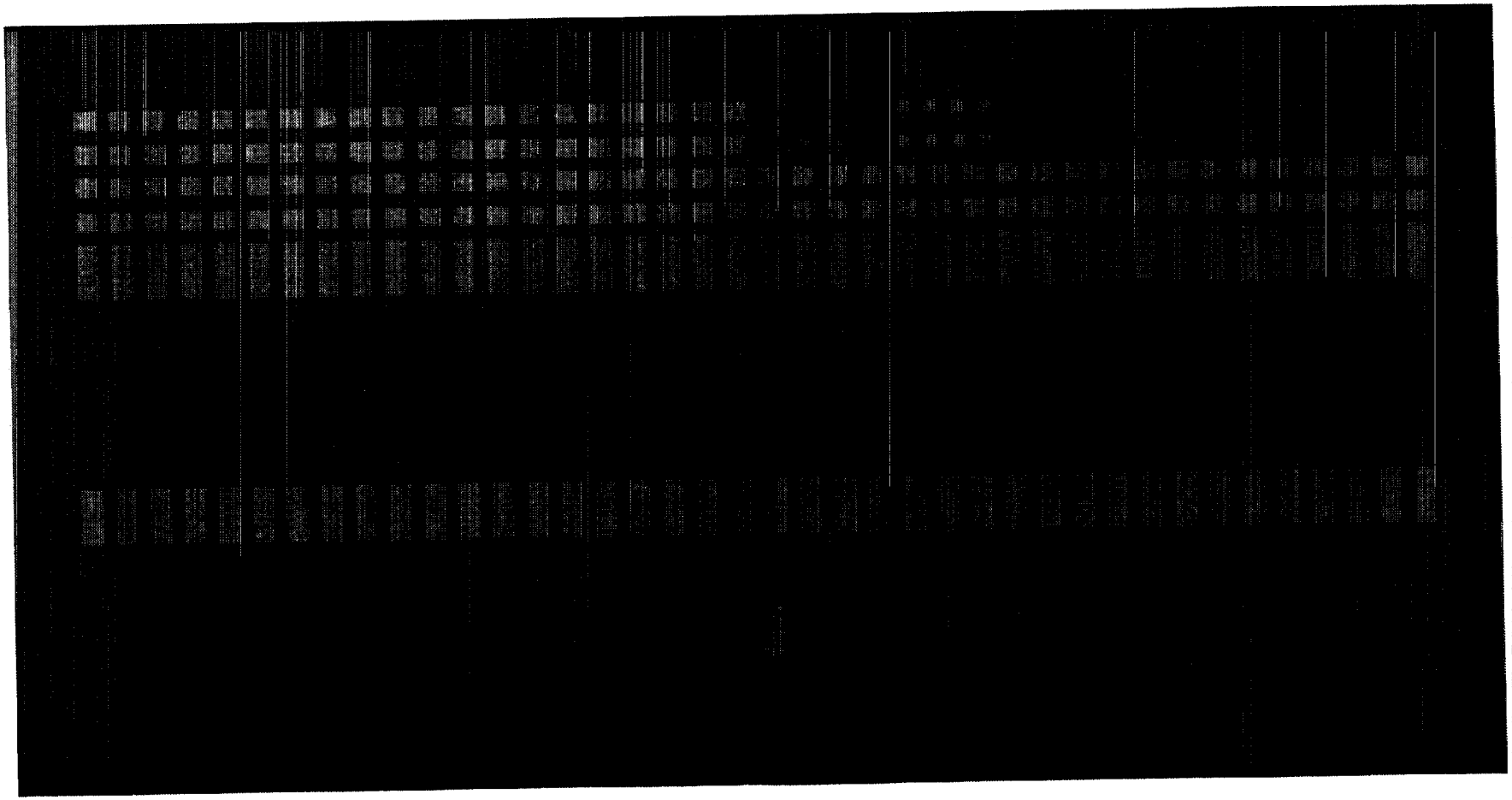
HDCC12-21b

TID CHIP CONCLUSIONS AND PLANS

- ISSUE: TEST YIELD WAS 90 PERCENT. THE CIRCUITS THAT FAILED WERE IN THE n-MOSFET SIDE OF THE MOSFET MATRIX.
- CONCLUSION: THIS FAILURE CORRELATES WITH PROCESS MONITOR DATA THAT SHOWS n+ DIFFUSION TO METAL 1 CONTACTS ARE POOR.
- ISSUE: MOSFET RESULTS OF THE PROCESS MONITOR AND THE TID CHIP ARE CONSISTENT.
- CONCLUSION: THE TID CHIP CAN SERVE AS AN INDUSTRIAL STANDARD TEST CHIP.

JPL

RELIABILITY CHIP
1.6-μm n-WELL CMOS/BULK



CHIP = 3.08 mm x 6.37 mm

HDCC12-23a

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JPL

RELIABILITY CHIP FLOOR PLAN AND SPECIFICATION

M1nD/CONTACT RESISTOR CHAIN 16-2μmx2μm		M1,M2,POLY/SPLIT-CROSS-BRIDGE RESISTOR
M1nD/CONTACT RESISTOR CHAIN 16-2μmx2μm		M1nD/CONTACT RESISTOR CHAIN 16-2μmx2μm
M1/SERPENTINE 18 SEGMENTS, 8000 μm LONG	M2 SXBR	M2/SERPENTINE 18 SEGMENTS. 8000 μm LONG
M2/SERPENTINE 18 SEGMENTS, 8000 μm LONG	THICKNESS MONITOR	M1 SERPENTINE 18 SEGMENTS, 8000 μm LONG

HDCC12-23b

RELIABILITY CHIP DESCRIPTION

- THE RELIABILITY CHIP IS INTENDED TO BE USED TO CHARACTERIZE ELECTROMIGRATION IN METAL-1, OR METAL-2 AND METAL-1 TO DIFFUSION CONTACTS.

- ELECTROMIGRATION IN METALS IS A WEAR-OUT MECHANISM FOUND IN THE INTERCONNECTS OF INTEGRATED CIRCUITS. THIS MECHANISM IS ACCELERATED BY HIGH TEMPERATURES AND HIGH CURRENT DENSITIES. IT IS THEREFORE CHARACTERIZED BY AN ACTIVATION ENERGY, E_a , AND A CURRENT DENSITY, J^{-n} ,FOUND IN BLACK'S EQUATION FOR THE TIME TO FAILURE:

$$t_p = A \cdot J^{-n} \, e^{E_a/kT}$$

HDCC12-24a

HISTORICAL METAL-2 ELECTROMIGRATION DATA

TECH. (μm)	VENDOR	RUN NO.	CHIP NO.	E_a (eV)	n	σ	OPERATING t_{50} (YEARS) 55°C	125°C	R (Ω)
3	B	M78W	-	0.36±0.05	1.50±0.20	0.32±0.02	30.0	3.00	-
3	D	M88F	-	0.33±0.02	1.37±0.08	0.18±0.01	0.50	0.06	-
2	C	M92P	1	0.47±0.02	3.72±0.20	0.37±0.02	2.5E4	1.3E3	-
1.6	A	M95F	1	0.50±0.02	1.80±0.10	0.34±0.02	9.1	0.40	1515
1.6	A	M95F	19	0.19±0.05	6.70±0.30	0.70±0.05	2.4E6	7.0E5	1400
1.6	A	M9AD	1	0.54±0.04	3.30±0.21	0.51±0.04	2300.	80.	1490
1.6	A	M9AD	10	0.42±0.04	3.09±0.04	0.58±0.03	350.	25.	1470
1.6	A	N06J	18	0.49±0.04	4.19±0.23	0.70±0.04	8.0E4	4.0E3	1540
1.6	A	N06J	15	0.50±0.09	4.32±0.5	0.68±0.09	9.0E4	5.0E3	1560

METAL-2 ALUMINUM WITH ≈ 2 PERCENT SILICON. $J_{OPER} = 2 \times 10^5$ A/cm^2.

FAILURE MODEL: $t_p = A_p\, J^{-n}\, e^{E_a/kT}$. p IS PERCENTAGE OF SEGMENTS FAILED.

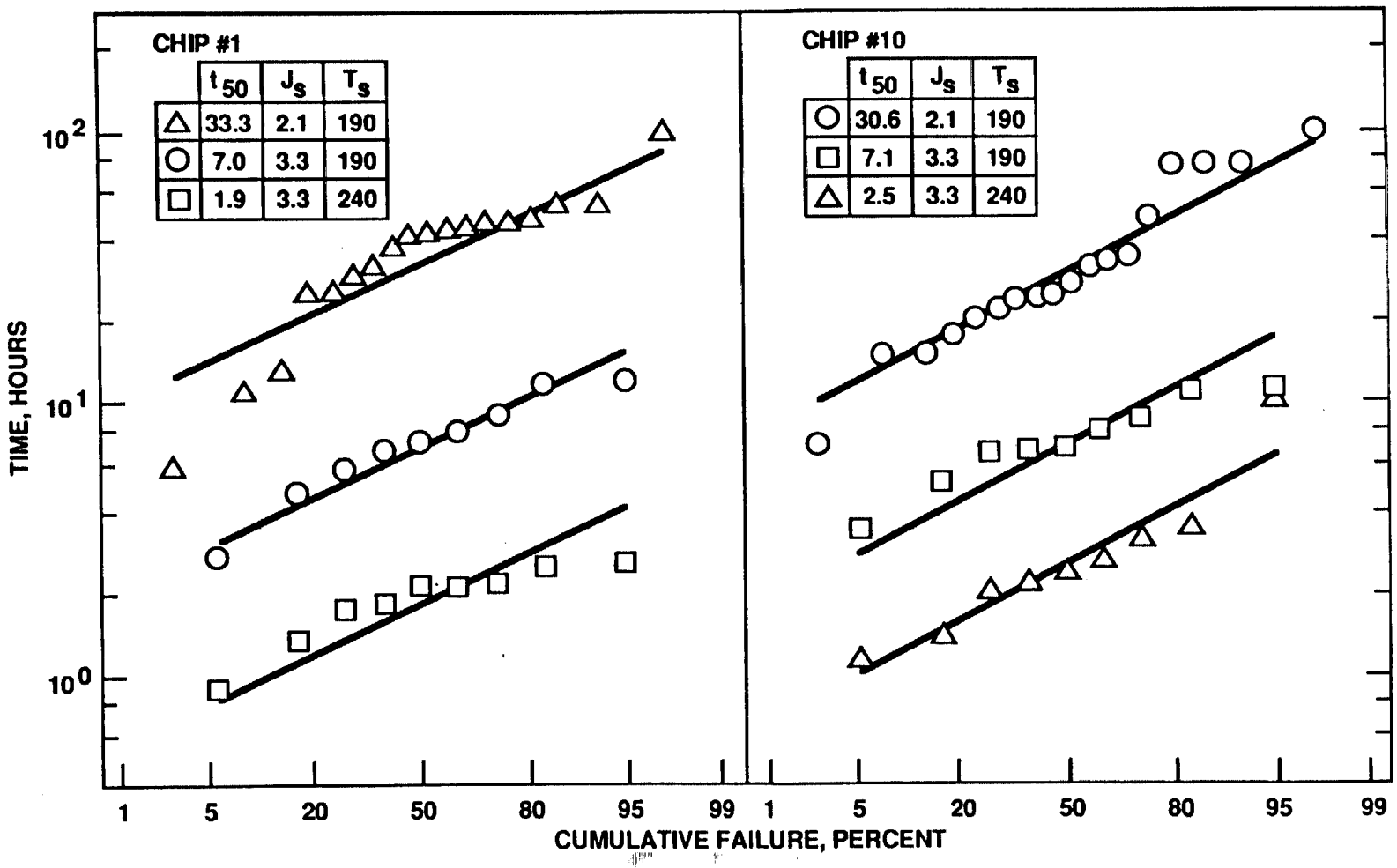
CONCLUSIONS:

- o N06J RESULTS ARE WELL BEHAVED – CONSISTENT RESULTS ARE OBTAINED FROM SEVERAL TEST CHIPS.
- o M9AD RESULTS ALSO WELL BEHAVED WITH SOMEWHAT DIFFERENT PARAMETERS.
- o M95F RESULTS ARE ERRATIC.

HDCC12-24b

JPL

METAL-2 ELECTROMITRATION
(RUN M9AD TEST RESULTS)



HDCC12-25a

METAL-2 ELECTROMIGRATION

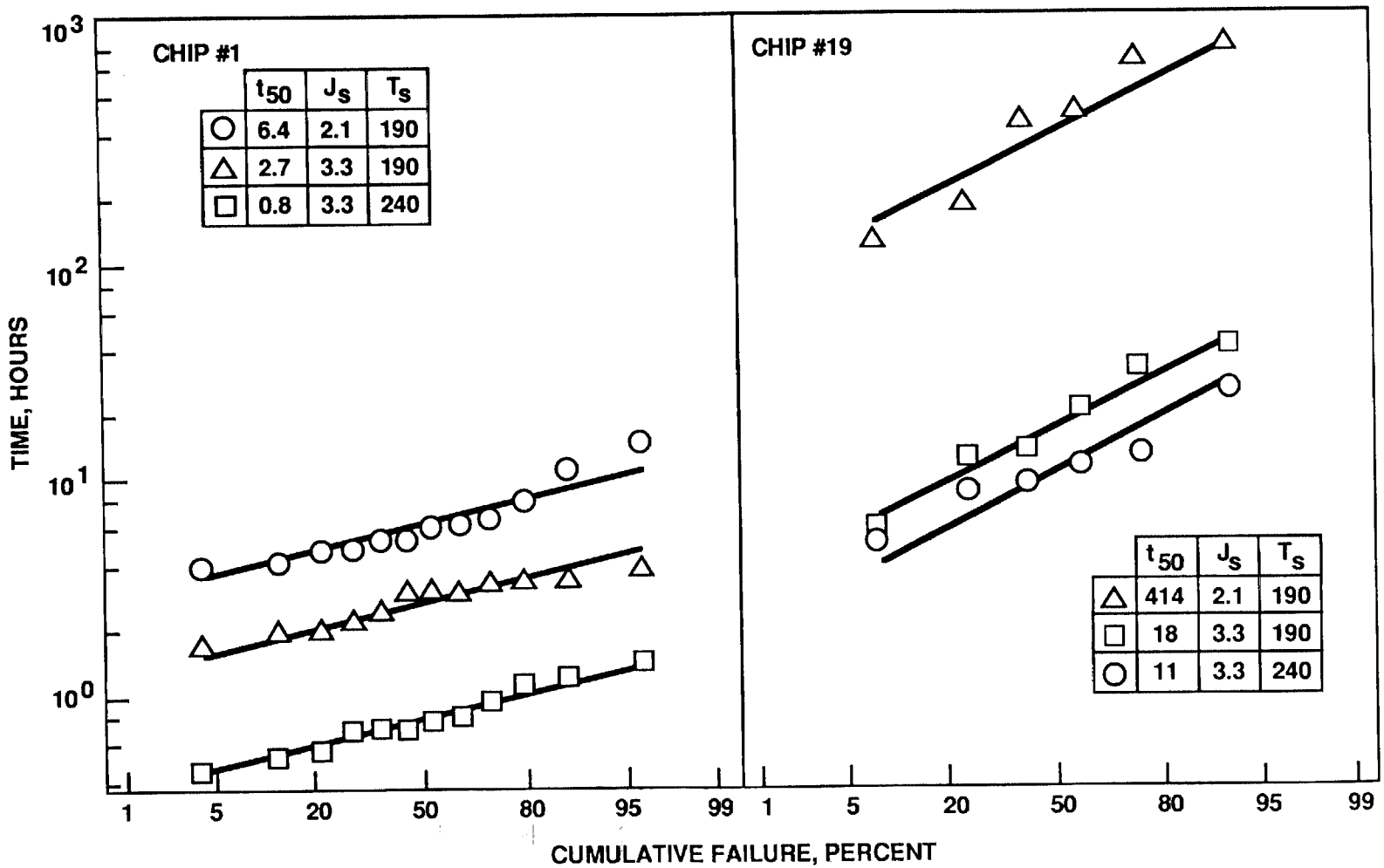
(RUN M9AD PARAMETERS)

J_{STRESS} $\frac{MA}{cm^2}$	t_{50} (HOURS) T_{STRESS} 190°C	240°C	CHIP NO.	E_a (eV)	n	σ	OPERATING MTTF (YEARS) $J_{OPER} = 2x10^5 (A/cm^2)$ 55°C	125°C	R (Ω)
2.1	33.3	-							
			1	0.54±0.05	3.30±0.21	0.51±0.04	2300.0	80.00	1490
3.3	7.0	1.9							
2.1	30.6	-							
			10	0.42±0.04	3.09±0.04	0.58±0.03	350.0	25.00	1470
3.3	7.1	2.5							

FAILURE MODEL $t_{50} = A \cdot J^{-n} \exp(E_a/kT)$. METAL-2 ALUMINUM WITH ≈2 PERCENT SILICON

CONCLUSION: M9AD RESULTS ARE WELL BEHAVED.

METAL-2 ELECTROMIGRATION TEST RESULTS
(RUN M95F TEST RESULTS)



	t_{50}	J_s	T_s
○	6.4	2.1	190
△	2.7	3.3	190
□	0.8	3.3	240

	t_{50}	J_s	T_s
△	414	2.1	190
□	18	3.3	190
○	11	3.3	240

HDCC12-26a

METAL-2 ELECTROMIGRATION

(RUN M95F PARAMETERS)

J_{STRESS} MA/cm^2	t_{50} (HOURS) T_{STRESS} 190°C	240°C	CHIP NO.	E_a (eV)	n	σ	OPERATING MTTF (YEARS) $J_{OPER} = 2x10^5$ (A/cm^2) 55°C	125°C	R (Ω)
2.1	6.4	-							
			1	0.50±0.02	1.80±0.10	0.34±0.02	9.1	0.40	1515
3.3	2.7	0.8							
2.1	413.9	-							
			19	0.19±0.05	6.70±0.30	0.70±0.05	2.4E6	7.0E5	1400
3.3	17.6	10.9							

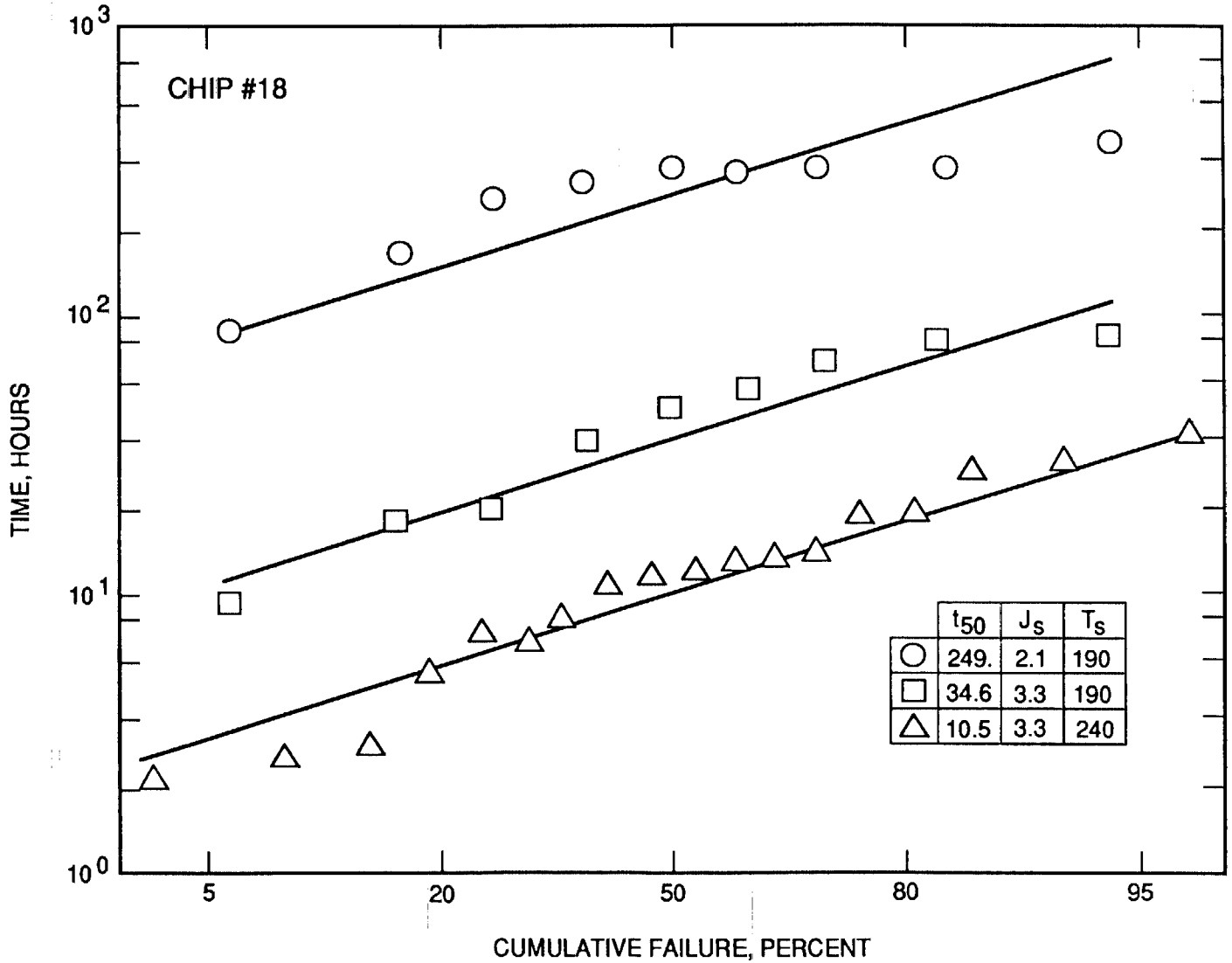
FAILURE MODEL $t_{50} = A \cdot J^{-n} \exp(E_a/kT)$. METAL-2 ALUMINUM WITH ≈2 PERCENT SILICON

CONCLUSION: M95F ELECTROMIGRATION RESULTS ARE ERRATIC.

HDCC12-26b

JPL

METAL-2 ELECTROMIGRATION TEST RESULTS
(RUN N06J TEST RESULTS)



t_{50} IS IN HOURS, J_S IN MA/cm^2, AND T_S IN °C.

HDCC12-27a

METAL-2 ELECTROMIGRATION

(RUN N06J PARAMETERS)

J_{stress} MA/cm^2	t_{50} (HOURS) T_{stress} 190°C	240°C	CHIP NO.	E_a (eV)	n	σ	OPERATING t_{50} (YEARS) 55°C	125°C	R (Ω)
2.1	248.6	–							
			18	0.49 ±0.04	4.19 ±0.23	0.70 ±0.04	8.0E4	4.0E3	1540
3.3	34.6	10.5							

METAL-2 ALUMINUM WITH ≈ 2 PERCENT SILICON. $J_{OPER} = 2 \times 10^5$ A/cm^2.

FAILURE MODEL: $t_p = A_p\, J^{-n}\, e^{E_a/kT}$. p IS PERCENTAGE OF SEGMENTS FAILED.

HDCC12-27b

JPL

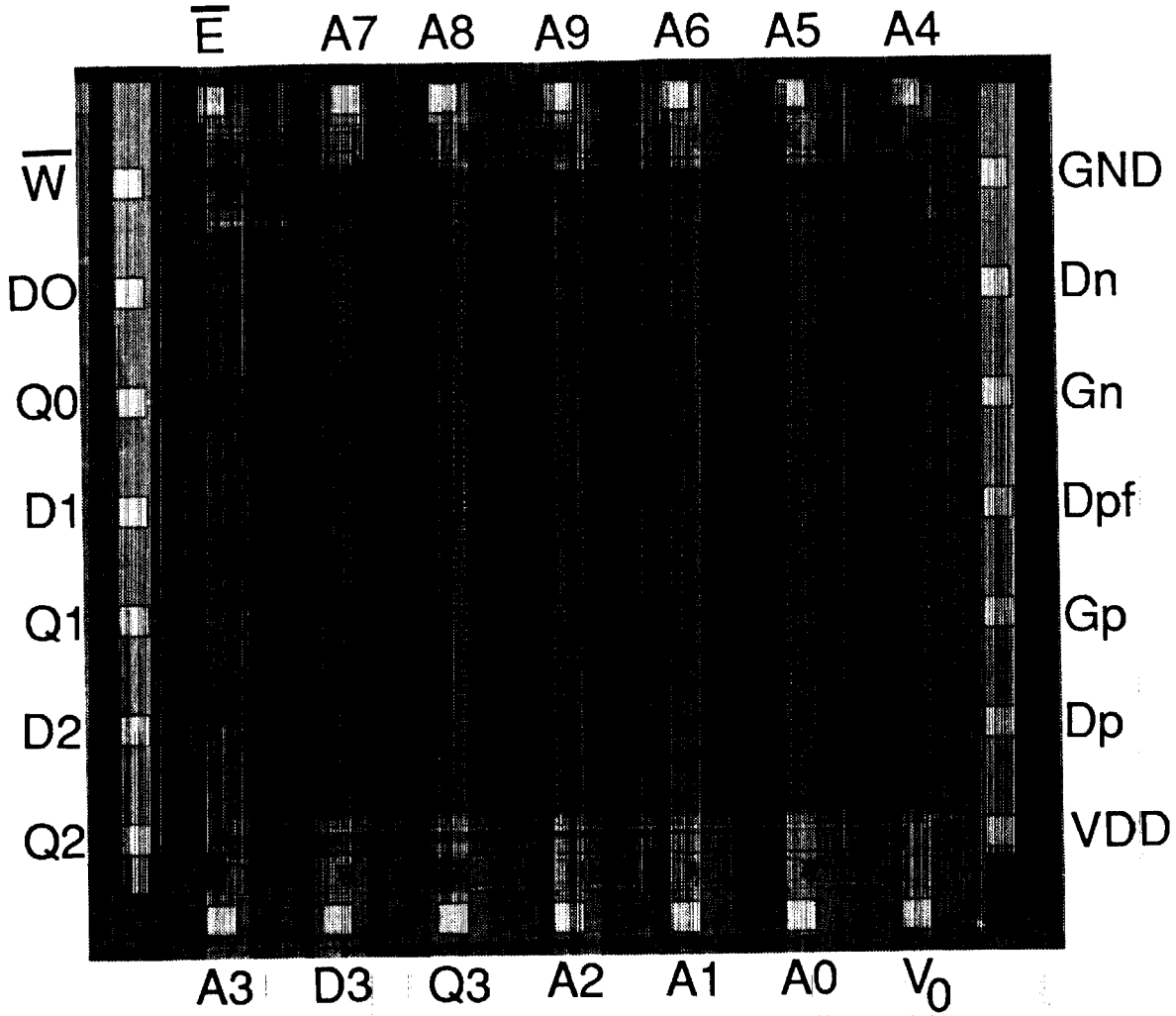
RELIABILITY CHIP CONCLUSIONS

- ISSUE: METAL ELECTROMIGRATION ON N06J RUN IS WELL BEHAVED.
- ISSUE: METAL ELECTROMIGRATION ON M9AD RUN IS ALSO WELL BEHAVED, BUT EM PARAMETERS WERE SOMEWHAT DIFFERENT.
- ISSUE: METAL ELECTROMIGRATION ON M95F RUN IS VERY ERRATIC.
- METHODOLOGY: REQUIRES A CONSISTENCY CHECK, THAT IS, MUST EVALUATE SEVERAL TEST CHIPS.
- METHODOLOGY: REQUIRES ESTABLISHING A DATABASE IN ORDER TO JUDGE QUALITY AND TO SET ACCEPTANCE CRITERIA.
- SIGNIFICANCE: THESE NUMBERS FEED MIL-HDBK-217 AND ALLOW EVALUATION OF ASIC RELIABILITY.

HDCC12-28b

JPL

SEU/TD RADIATION MONITOR



CHIP SIZE = 3.29mm x 3.12mm

HDCC12-29a

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SEU/TD RADIATION MONITOR DESCRIPTION, HISTORY AND PLANS

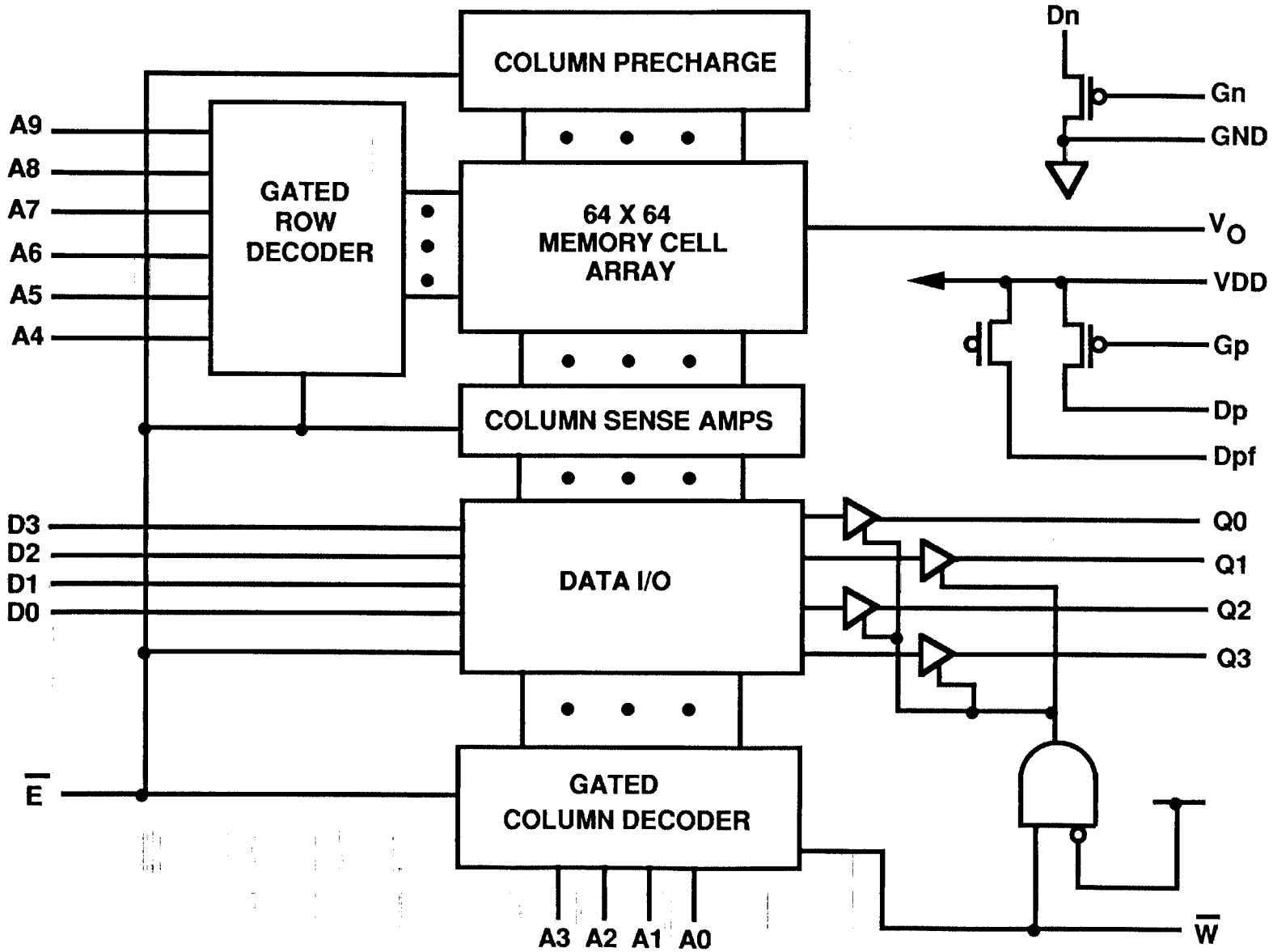
THIS CHIP IS A SINGLE EVENT UPSET (SEU) AND TOTAL DOSE (TD) RADIATION MONITOR WHICH WILL BE USED TO MEASURE THE RADIATION ENVIRONMENTS ON SPACECRAFT. WHEN FULLY DEVELOPED, IT IS ANTICIPATED THAT THIS CHIP WILL BE USED ON ALL SPACECRAFT TO ALERT THE SYSTEM TO RADIATION HAZARDS AND TO EXPLAIN RADIATION-INDUCED SATELLITE SYSTEM UPSETS. ACCUMULATED DATA FROM THIS CHIP CAN MAP THE NEAR-EARTH PARTICLE ENVIRONMENT AND COSMIC-RAY FLUX.

THE SEU/TD RADIATION MONITOR CONTAINS A CUSTOM 4096 BIT SRAM AND AN ISOLATED FLOATING GATE MOSFET EXPERIMENT. THE SRAM WAS DESIGNED WITH AN OFFSET VOLTAGE WHICH ALLOWS ITS SENSITIVITY TO UPSET TO BE ADJUSTED. IT IS FABRICATED USING THE SAME TECHNOLOGY AS THE FLIGHT CIRCUITS IN ORDER TO PROVIDE RELEVANT DATA. THE RADIATION DATA CAN BE COMPARED TO GROUND TEST DATA TO IDENTIFY DISCREPANCIES.

THE N06J SEU/TD RADIATION MONITOR WILL BE USED TO MONITOR THE TOTAL DOSE AND SEU RATE ON A SIGNAL PROCESSOR PACKAGE TO BE FLOWN ON THE MSX (MID COURSE SPACE EXPERIMENT) SATELLITE SCHEDULED TO LAUNCH IN 1992.

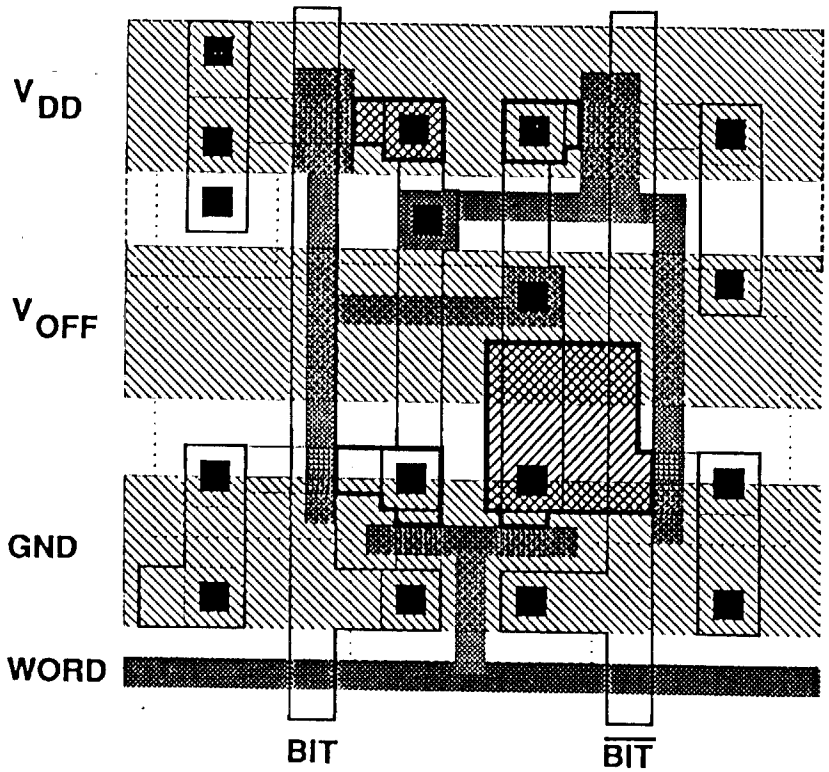
THIS IS THE SECOND TIME THAT THE VLSI TECHNOLOGY GROUP HAS DELIVERED FLIGHT PARTS. THE FIRST TIME WAS IN 1986 WHEN 12 TEST CHIPS WERE DELIVERED TO AFGL AND INCLUDED ON THE CRRES (COMBINED RADIATION RELEASE EFFECTS SATELLITE) LAUNCHED IN 1990. NEGOTIATIONS ARE CURRENTLY UNDER WAY TO PROVIDE GODDARD WITH RADIATION MONITORS FOR THE CRUX (COSMIC RAY EXPERIMENT) TO BE FLOWN ON THE APEX (ADVANCED PHOTOVOLTAICS AND ELECTRONICS EXPERIMENTS) SATELLITE.

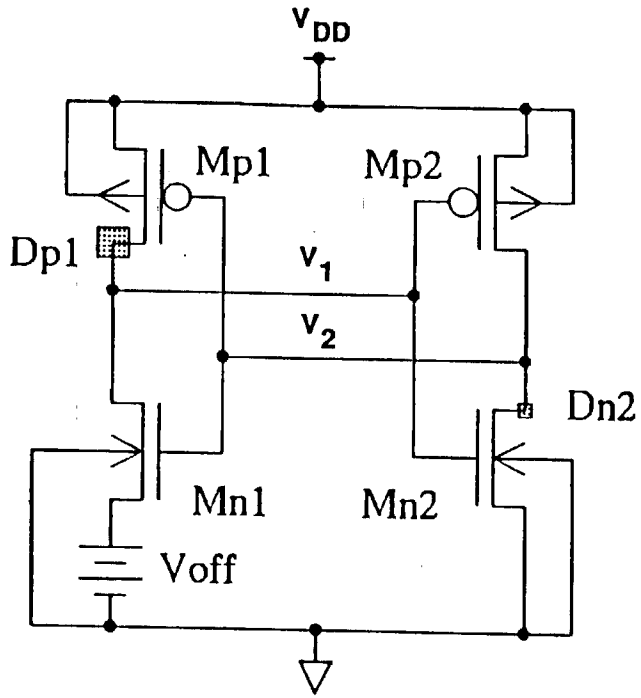
SEU/TD RADIATION MONITOR BLOCK DIAGRAM



HDCC12-30a

1.6 μm n-WELL CMOS BULK SEU SRAM CELL (N06J)





- METAL 1
- METAL 2
- DIFFUSION
- POLY
- CONTACT

DEVICE	L (μm)	W (μm)	Ad (μm²)
Mn1	1.6	2.4	17.92
Mn2	1.6	3.2	74.88
Mp1	3.2	2.4	14.08
Mp2	3.2	2.4	12.16

HDCC12-30b

SEU/TD RADIATION MONITOR TEST RESULTS

- SEU CHIP STATISTICS:
  - SRAM CELL TYPE = SIX TRANSISTOR CELL
  - NO. OF TRANSISTORS/CHIP = 26,000
  - NO. OF CHIPS FUNCTIONALLY TESTED = 75
  - TOTAL NUMBER OF TRANSISTORS TESTED = 1,950,000
  - NO. OF CHIPS HERMETICALLY SEALED AND BURNED-IN = 50

- SEU/TD RADIATION MONITOR YIELD SUMMARY
  - SEU CHIP FUNCTIONAL YIELD = 94.6%
  - 71 SRAMS PAST POWER UP, WALKING ONES, CHECKER-BOARD, ACCESS TIME, AND STANDBY POWER TESTS
  - 50 SRAMS AND 41 COMPLETE MOSFET EXPERIMENTS PASSED A 24 HOUR BURN-IN AT 125°C
  - 43 SRAMS AND 14 COMPLETE MOSFET EXPERIMENTS PAST HERMETICITY AND FINAL ELECTRICAL TESTS

NOTE: THE MOSFET EXPERIMENT WAS INTENTIONALLY DESIGNED WITHOUT INPUT PAD PROTECTION TO ALLOW ACCURATE CURRENT MEASUREMENT. NORMAL ESD PREVENTION PRACTICES WERE NOT SUFFICIENT TO PROTECT MANY OF THESE DEVICES DURING SCREENING.

SEU/TD RADIATION MONITOR SCREENING PROCEDURES

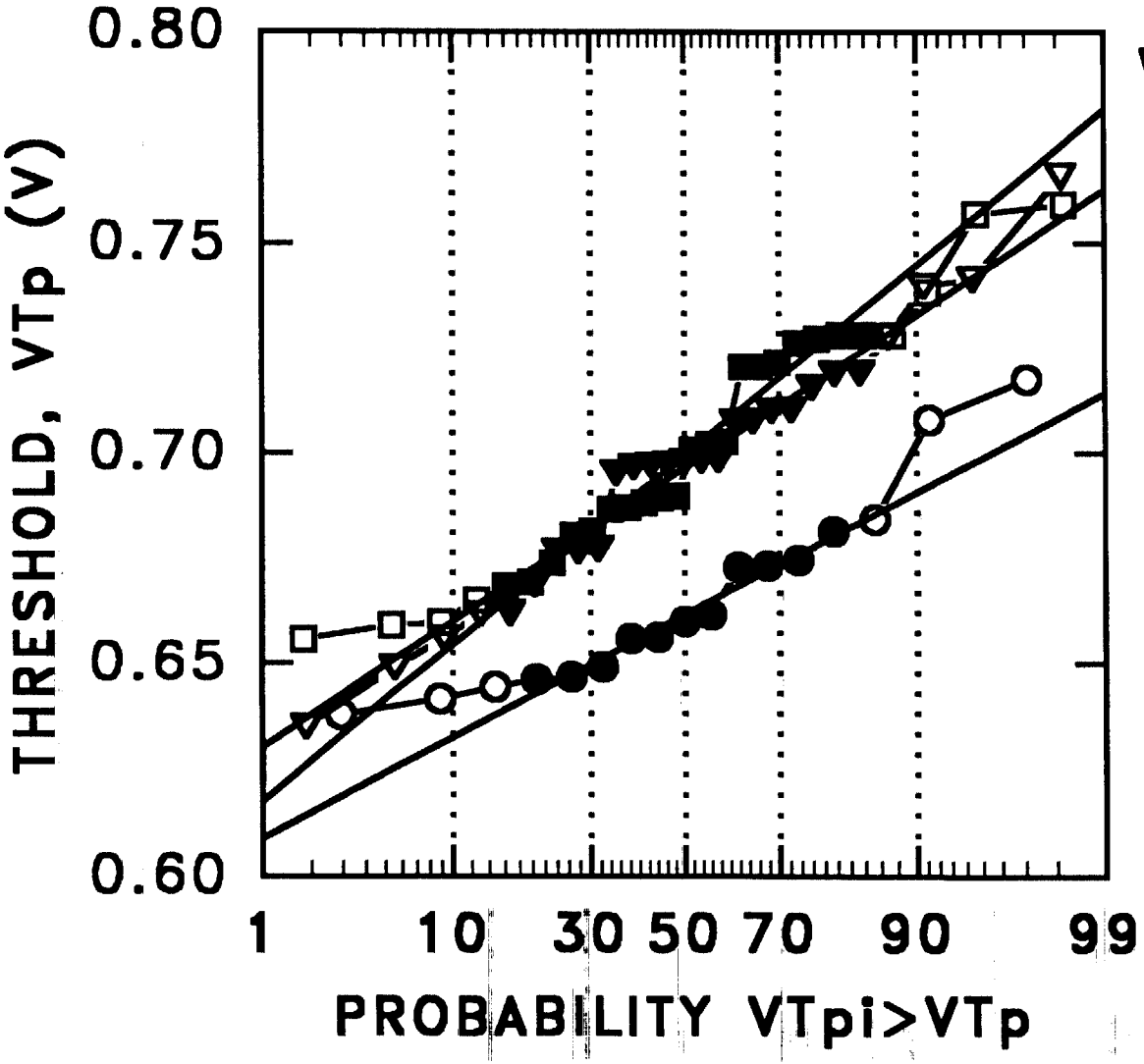
SUBSET OF MIL-STD-883C SCREENING REQUIREMENTS

- NONDESTRUCTIVE BOND PULL (METHOD 2032)
- INTERNAL VISUAL INSPECTION (METHOD 2010)
- EXTERNAL (PACKAGE) VISUAL INSPECTION
- PRE-BURN-IN STATIC AND DYNAMIC TEST
- BURN IN (24 HOURS AT 125°C) ALL LEADS SHORTED
- POST BURN-IN STATIC AND DYNAMIC TEST
- POST HERMETIC SEAL STATIC AND DYNAMIC TEST
- HERMETICITY TEST (METHOD 1014)
- FINAL EXTERNAL VISUAL INSPECTION
- PRE-SHIP REVIEW

HDCC12-31b

JPL

p–MOSFET THRESHOLD VOLTAGE (N06J)

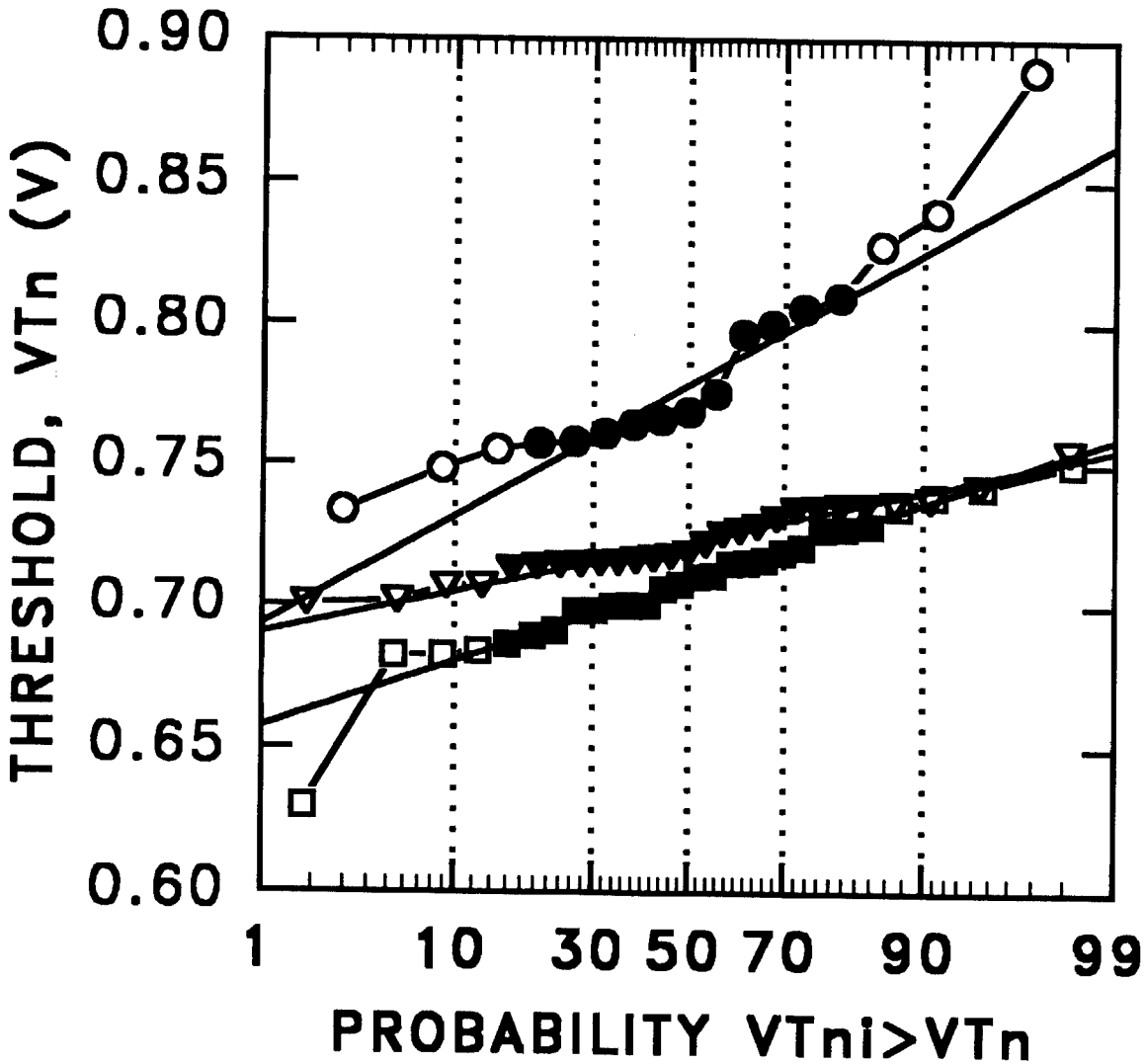


WAFER	$VT_{\mu}(V) \pm VT_{\sigma}(V)$
● 2	0.662±0.023
▼ 11	0.696±0.029
■ 12	0.700±0.036

HDCC12-32a

JPL

n–MOSFET THRESHOLD VOLTAGE (N06J)

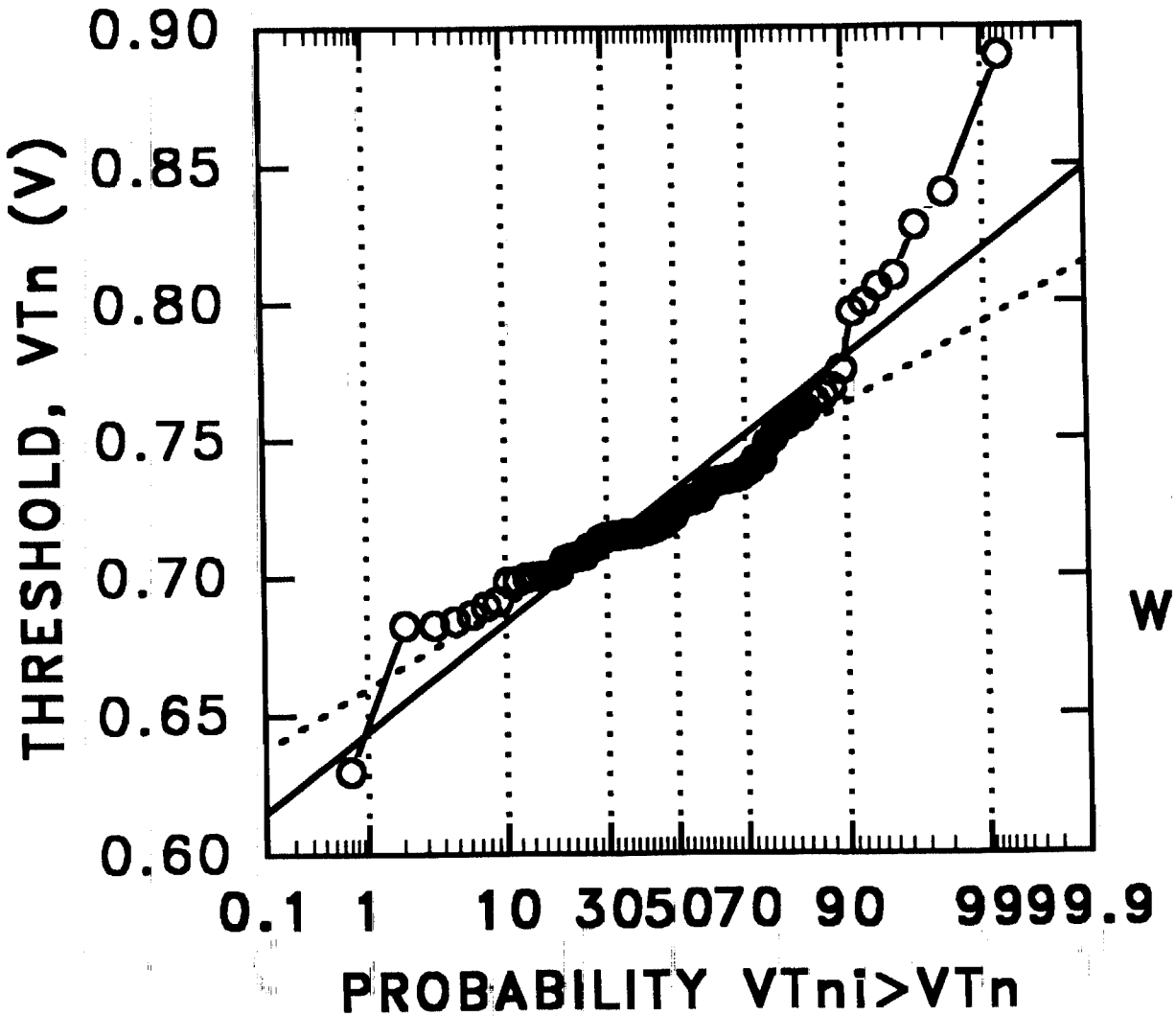


WAFER	$VT_{\mu}(V) \pm VT_{\sigma}(V)$
● 2	0.778±0.037
▼ 11	0.722±0.014
■ 12	0.708±0.022

HDCC12-32b

JPL

n–MOSFET THRESHOLD VOLTAGE (N06J)



$V_{\mu}(V) \pm VT_{\sigma}(V)$

- ±1 SIGMA DATA
  0.726±0.029

- ALL DATA
  0.732±0.038

WAFER = 2, 11 & 12

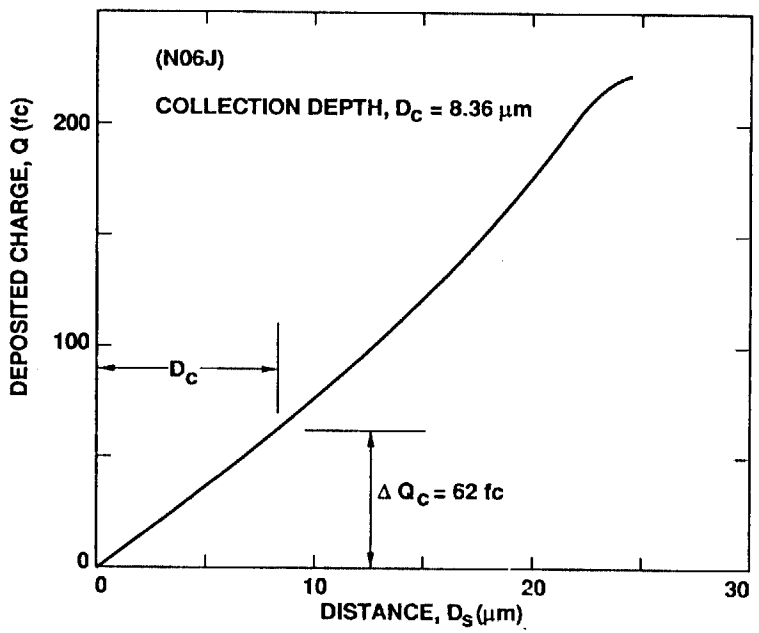
HDCC12-33a

SEU/TOTAL DOSE RADIATION MONITOR SUMMARY OF MOSFET ANALYSIS

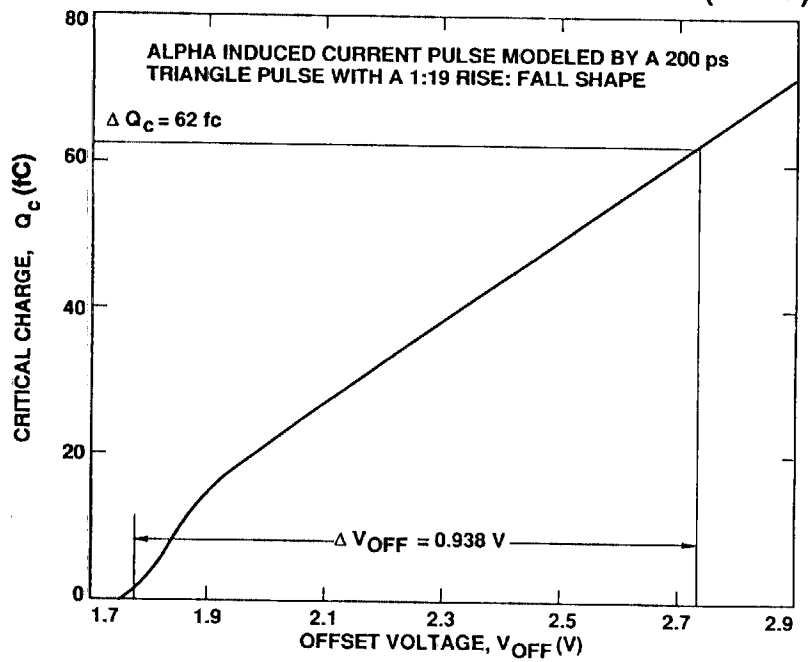
- THE ANALYSIS OF WAFERS #2, #11, AND #12 SHOWS THE IMPORTANCE OF EVALUATING WAFERS INDIVIDUALLY.
  - WAFER #2 THRESHOLD VOLTAGES DIFFER FROM THE LOT. CHIPS TESTED FROM THIS WAFER HAD HIGHER VT_n AND LOWER VT_p.
  - THE THRESHOLD VOLTAGE STANDARD DEVIATIONS FOR THE LOT WERE 38 mV BUT ONLY 14 mV FOR WAFER #11.

SEU/TD RADIATION MONITOR

DEPOSITED CHARGE PROFILE OF 5-MeV ALPHA PARTICLE IN SILICON

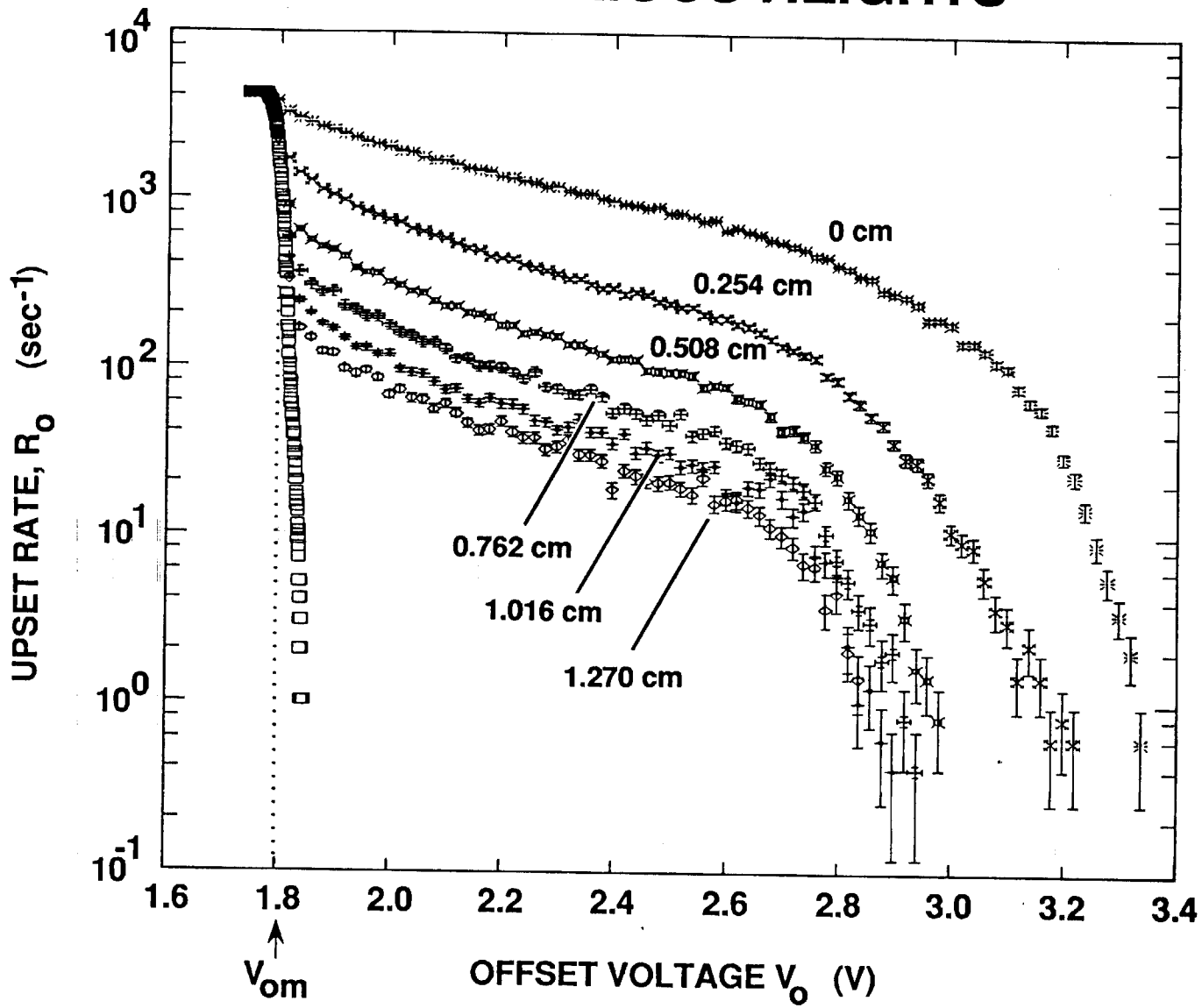


SPICE ANALYSIS OF CRITICAL CHARGE (N06J)



HDCC12-34a

TEST SRAM UPSETS FOR Am-241 SOURCE AT VARIOUS HEIGHTS



OVERLAYER THICKNESS MEASURED AT 7.59 μm.
COLLECTION DEPTH MEASURED AT 6.09 μm.

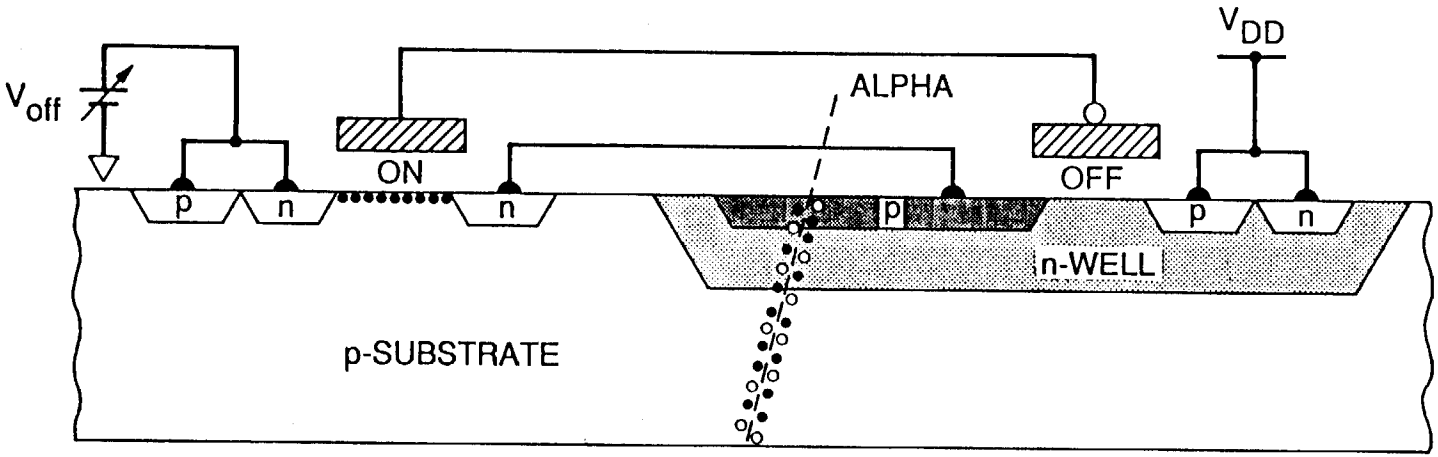
HDCC12-34b

SRAM CROSS SECTION RESULTS
(M95F AND N06J)

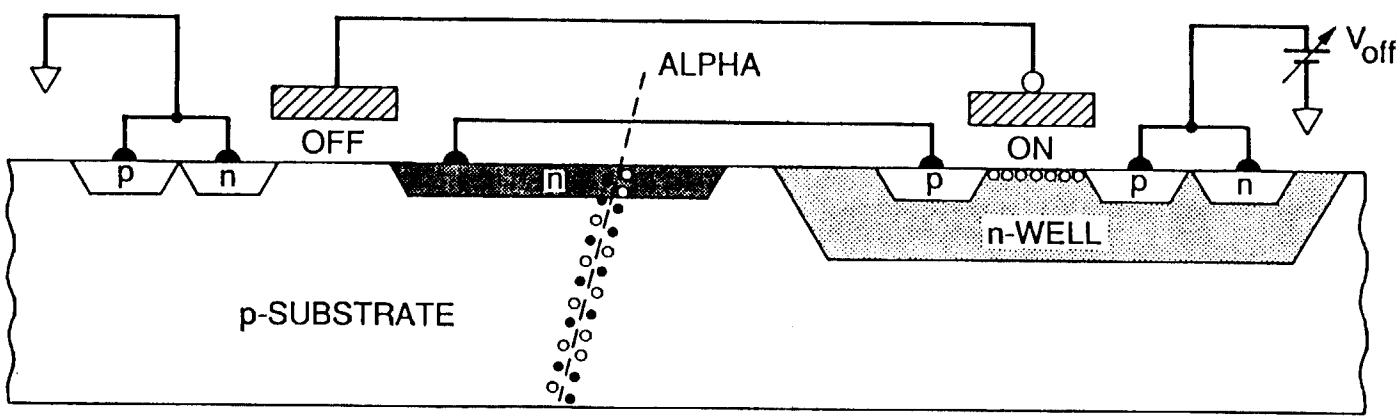
- M95F SRAM WAS DIFFICULT TO UPSET WITH ALPHA PARTICLES
- REASON: THE BLOATED p-DRAIN WAS PLACED IN THE n-WELL WHICH TRUNCATES THE ALPHA PARTICLE TRACK
- SOLUTION: DESIGN BLOATED DRAIN IN SUBSTRATE TO INCREASE CHARGE COLLECTION DEPTH
- RESULT: N06J SRAM BLOATED DRAIN IS IN THE SUBSTRATE WHICH HAS MADE THIS SRAM SENSITIVE TO ALPHA PARTICLES

HDCC12-35a

SRAM CROSS SECTION
(M95F AND N06J)



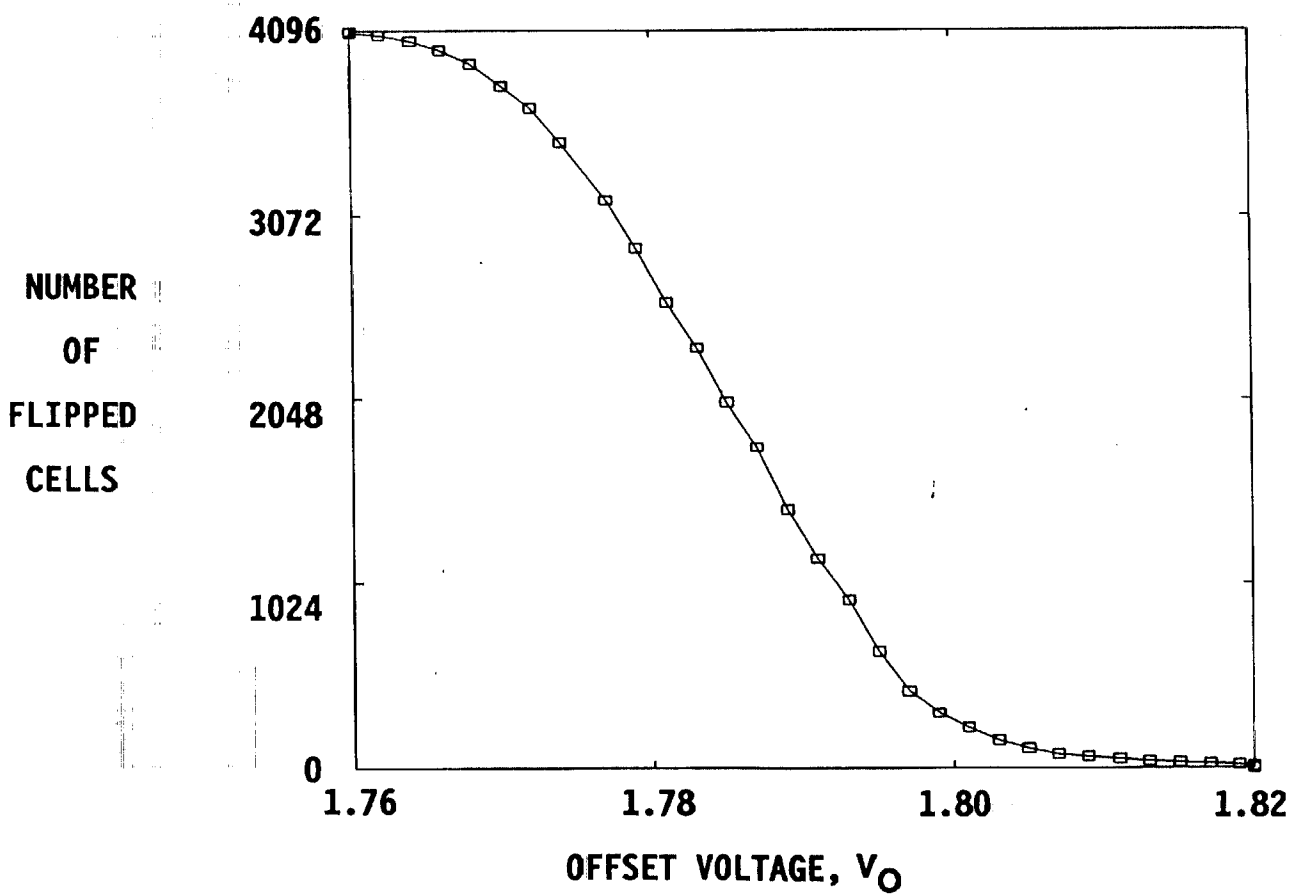
M95F BLOATED p-DRAIN WAS PLACED IN THE n-WELL WHICH TRUNCATES THE ALPHA PARTICLE TRACK



N06J SRAM BLOATED DRAIN IS IN THE SUBSTRATE

HDCC12-35b

SEU/TD RADIATION MONITOR SPONTANEOUS FLIP RESPONSE (RUN N06J TEST RESULTS)



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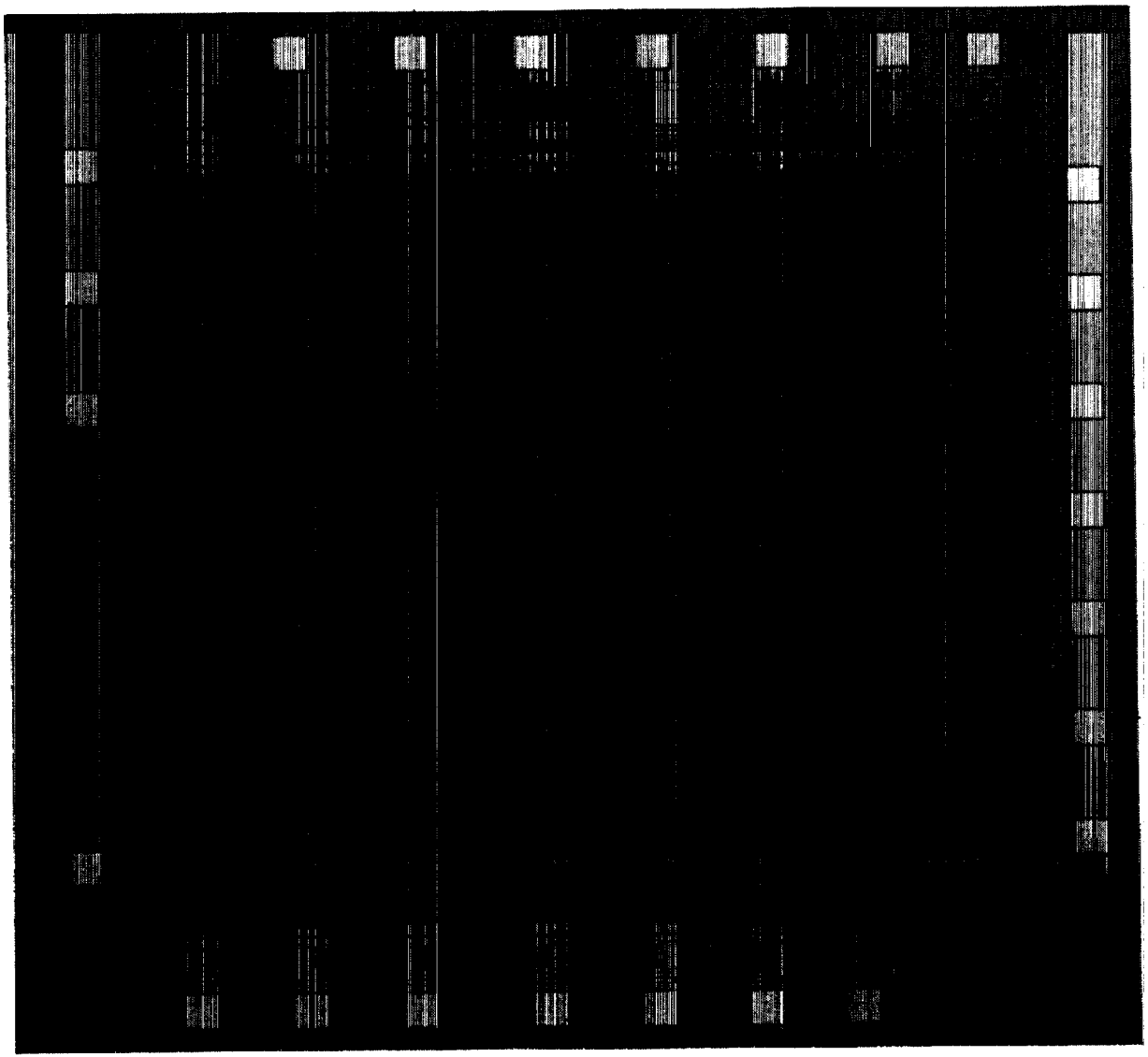
HDCC12-36a

HDCC12-36b

JPL

SEU SRAM CHIP
1.6 μm n-WELL CMOS/BULK



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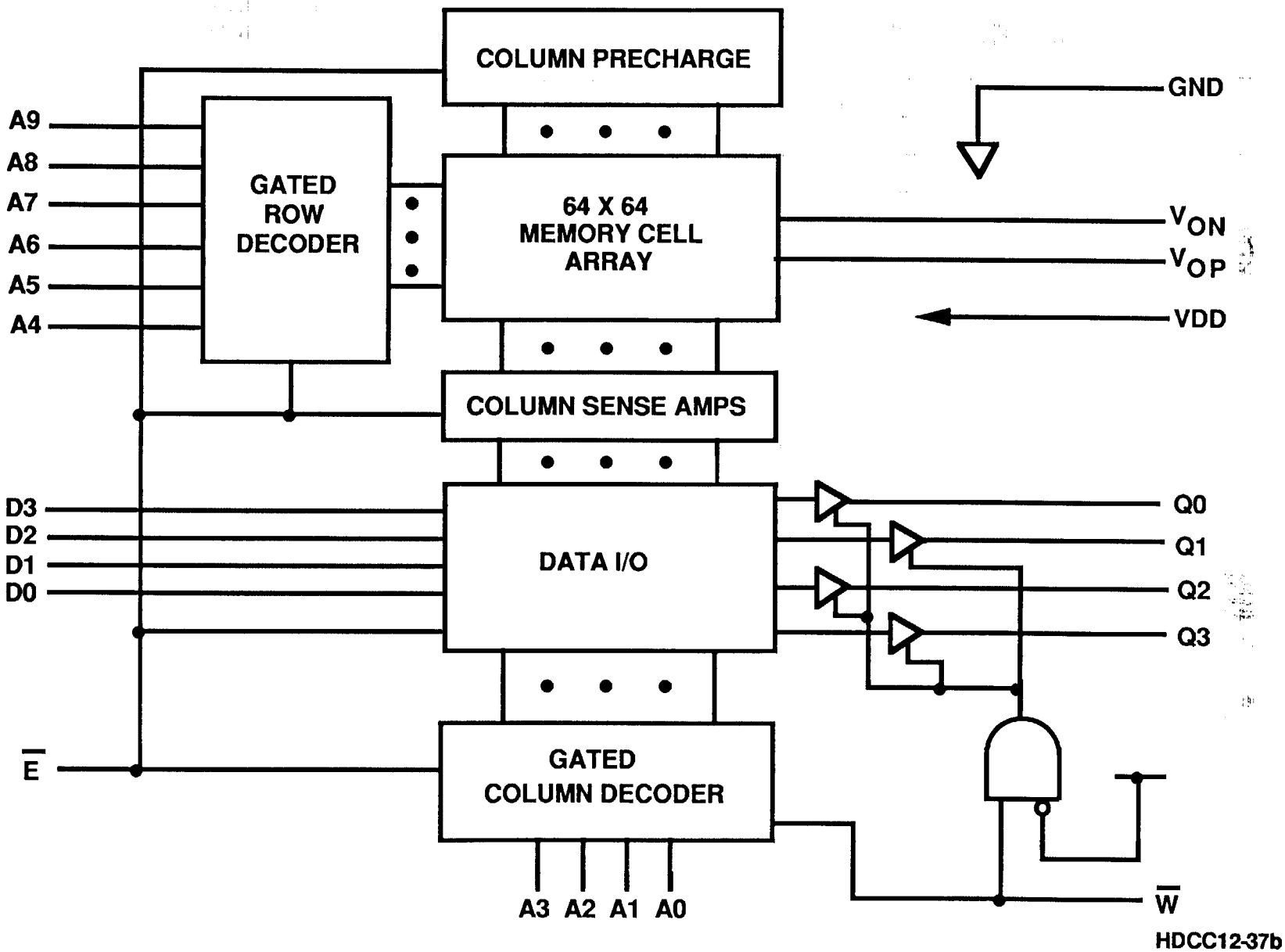
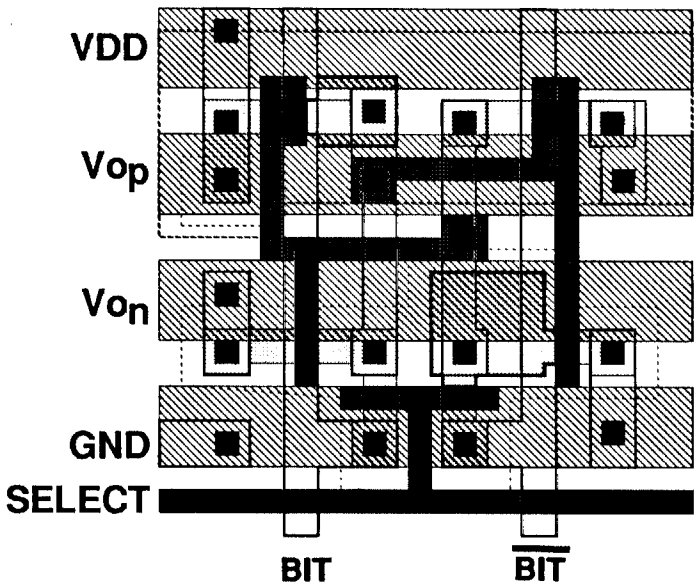
JPL

SEU SRAM CHIP BLOCK DIAGRAM

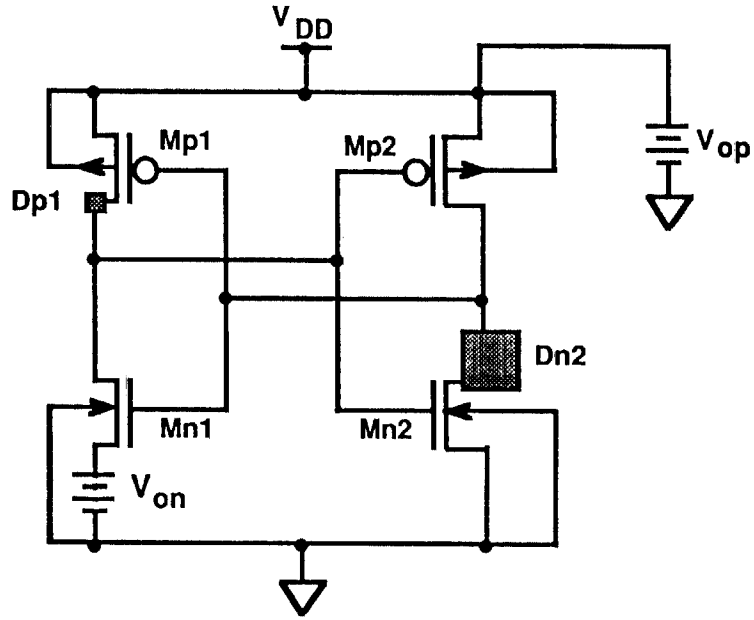


HDCC12-37b

1.6-μm SEU SRAM CELL (N06J)



A-CELL LAYOUT



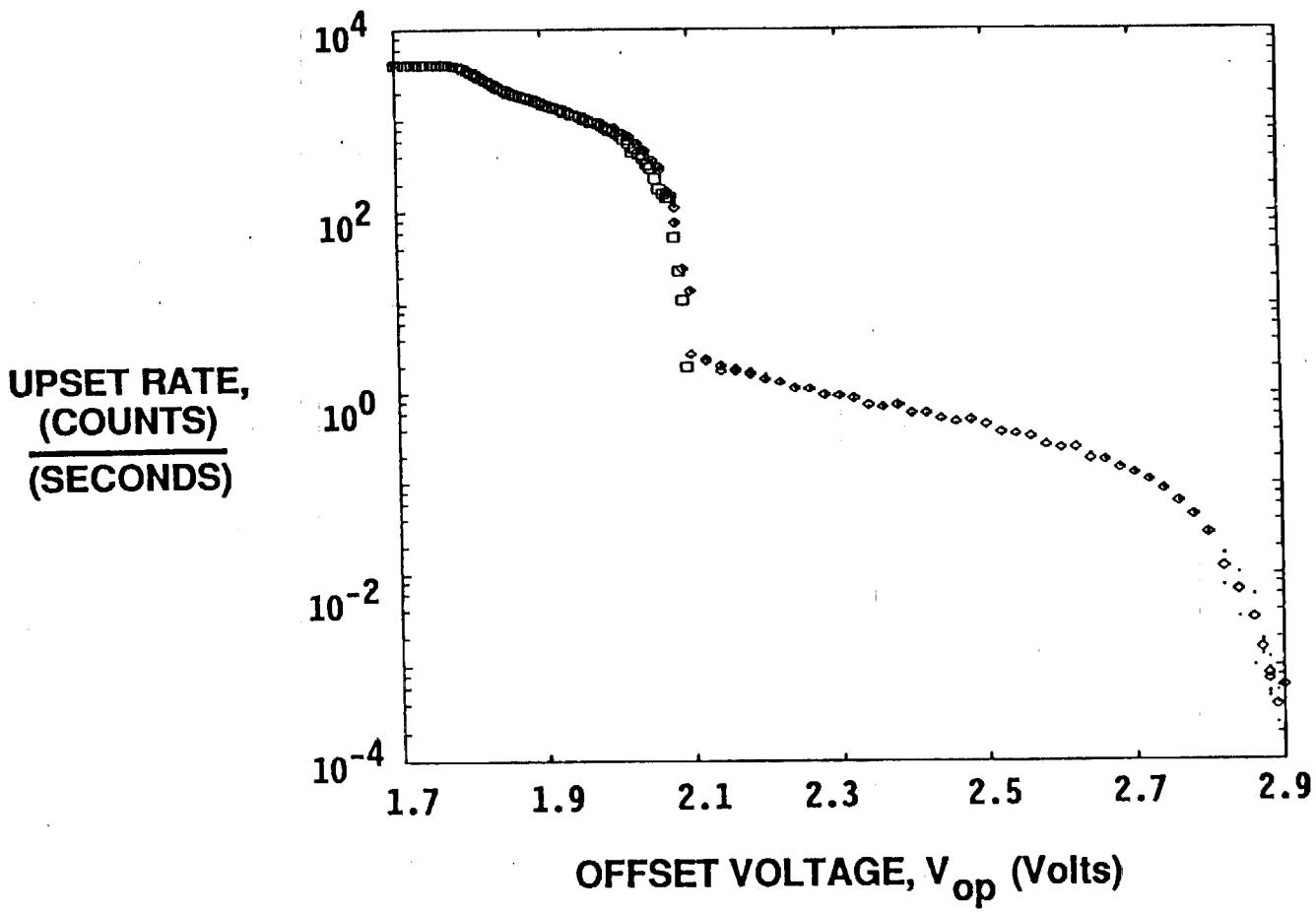
- METAL 1
- METAL 2
- DIFFUSION
- POLY
- CONTACT

DEVICE	L (μm)	W (μm)	A-CELL Ad (μm^2)	B-CELL Ad (μm^2)
Mn1	1.6	2.4	17.92	17.92
Mn2	1.6	2.4	61.44	17.92
Mp1	3.2	2.4	30.72	17.92
Mp2	3.2	2.4	17.92	17.92

SRAM CONSISTS OF 2048 A-CELLS AND 2048 B-CELLS ARRANGED IN A CHECKERBOARD PATTERN

HDCC12-38a

SEU SRAM CHIP
ALPHA PARTICLE RESPONSE
(RUN N06J TEST RESULTS



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SEU SRAM RESULTS (N06J)

- THE SEU SRAM DOSIMETER SERVES AS A STANDARD EVALUATION CHIP (SEC) BECAUSE OF ITS EXCELLENT TESTABILITY.
- THE STATISTICS OF THE SRAM CELL FLIPPING THRESH - OLD CAN BE MEASURED THROUGH THE USE OF THE OFFSET VOLTAGE, Voff.
- THE FLIPPING THRESHOLD SPREAD OF THE SEU SRAM DOSIMETER = 50mV.
- THE FLIPPING THRESHOLD SPREAD OF THE EXPERI - MENTAL SEU SRAM = 300 mV. THIS EXCESSIVE VALUE WAS DUE TO IR DROPS ON THE GROUNDED Von BUS, AS REVEALED BY NON RANDOM BIT MAP PATTERNS.
- A COLLECTION DEPTH FOR 5.0 MeV NORMAL INCIDENT ALPHA PARTICLES WAS FOUND TO BE 8.36 μm.

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- TOTAL DOSE CHIP
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