Some prototype parts of a digital beam-forming (DBF) receiver that would operate at multigigahertz carrier frequencies have been developed. The beam-forming algorithm in a DBF receiver processes signals from multiple antenna elements with appropriate time delays and weighting factors chosen to enhance the reception of signals from a specific direction while suppressing signals from other directions. Such a receiver would be used in the directional reception of weak wideband signals — for example, spread-spectrum signals from a low-power transmitter on an Earth-orbiting spacecraft or other distant source.

The prototype parts include superconducting components on integrated-circuit chips, and a multichip module (MCM), within which the chips are to be packaged and connected via special inter-chip-communication circuits. The design and the underlying principle of operation are based on the use of the rapid single-flux quantum (RSFQ) family of logic circuits to obtain the required processing speed and signal-to-noise ratio. RSFQ circuits are superconducting circuits that exploit the Josephson effect. They are well suited for this application, having been proven to perform well in some circuits at frequencies above 100 GHz. In order to maintain the superconductivity needed for proper functioning of the RSFQ circuits, the MCM must be kept in a cryogenic environment during operation.

The DBF and cryogenic aspects of the receiver design make it possible to overcome the limitations of both (1) the inherently narrow-band nature of analog beam-forming circuits in which the differential time delays needed for beamforming (including beam steering) are implemented via phase shifts and (2) the relatively slow speeds of room-temperature digital signal processors. A typical fully developed DBF receiver would have to contain more than two input-signal-processing channels for effectiveness in beam forming. For demonstrating feasibility at the present early stage of development, the prototype MCM is designed to accommodate two input-signal-processing channels.

The complete two-channel MCM would contain five chips: two analog-to-digital converter (ADC) chips, two multiplier chips, and an adder/driver chip (see figure). The ADC in each channel is designed to digitize the incoming signal to two bits at a sampling rate of 10 GS/s. The ADC chip includes a digital mixer and anti-aliasing filters that shift the signal frequency down to a bandwidth of 2.5 GHz and separate the signal into in-phase (I) and quadrature (Q) components. The multiplier in each channel is designed to introduce weighting and delay factors for steering. The adder portions of the adder/driver chip are designed to combine the I and Q signal components from the two channels. The driver portion is needed to amplify the outputs of the adders to avoid errors that could otherwise occur if one were to couple the low-level adder outputs directly to external room-temperature circuits.

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Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Commercial Technology Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-16935.