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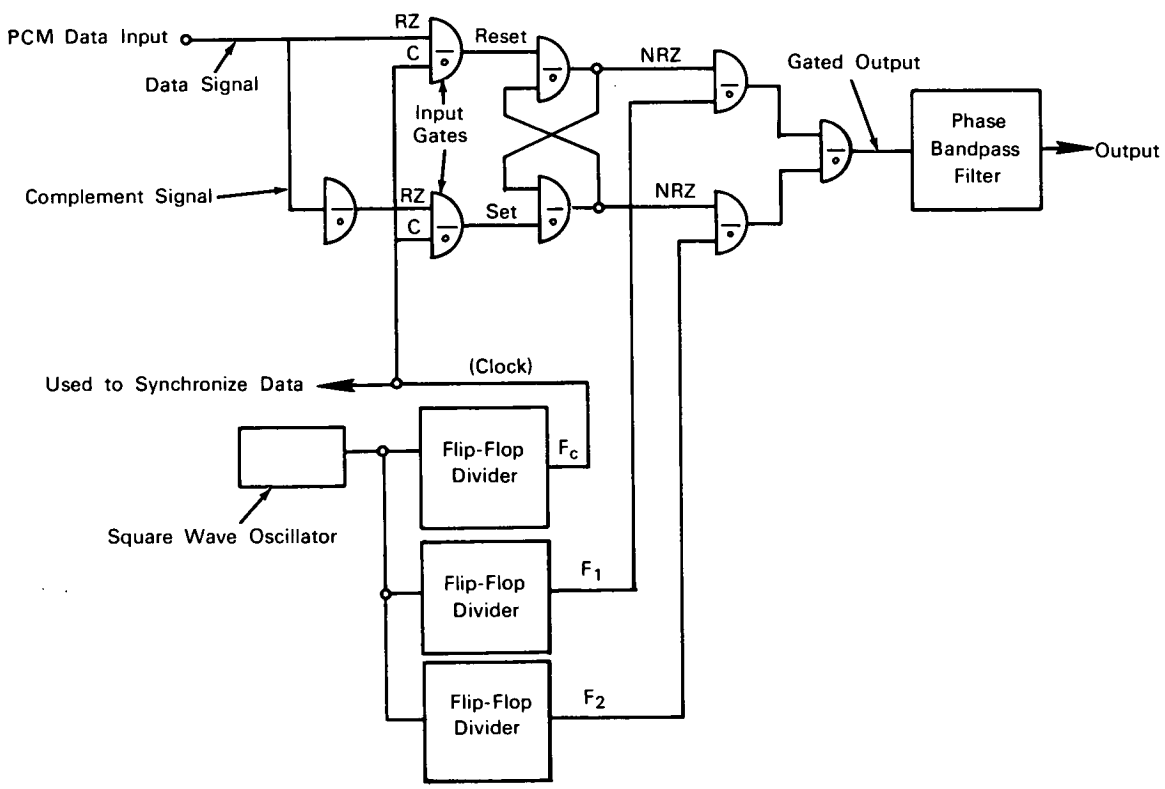
Brief 63-10511

NASA TECH BRIEF

Frequency-Shift-Keyer Circuit Improves PCM Conversion for Radio Transmission



The problem: In using pulse code modulated (PCM) data to shift between two fixed-frequency oscillators, it is possible to shift from any point in the cycle of one frequency to a different point in the cycle of the other frequency. When this occurs, the resulting noncoherent output wave contains high-frequency components. These high-frequency components cause ringing in the bandpass filters used to limit the bandwidth in both transmitting and receiving equipment.

The solution: A data logic circuit in which flip-flop gates are substituted for diode-balanced modulators. The circuit is, in addition, a simplified method for PCM frequency conversion.

How it's done: A fixed-frequency, square-wave oscillator is used to derive a data rate signal and two shift frequencies, F_1 and F_2. The data bit rate signal becomes the clock rate, F_C, and F_1 and F_2 become control signals. The three divider networks are

(continued overleaf)

designed so that the two shift frequencies are integer multiples of the clock rate. Control signals, the clock signal, and the shift frequencies are all synchronized.

PCM data and its complement are fed into two gates that have a clock input. Clock signal C, is used to gate the PCM data and its inverse through two input gates which are also connected to the Set and Reset inputs of a flip-flop. "Zero" output of the flip-flop is used to gate one shift frequency, F_1, to the output. The "one" output of the flip-flop gates the frequency F_2 to the output.

This circuit allows the shifting from one frequency to the other to take place at the end of a whole number of cycles of one shift frequency and at the beginning of a cycle of the second shift frequency. A constant time delay bandpass filter extracts the fundamental frequency from the square waves.

Notes:

1. This technique can be used with either return to zero (RZ) or with nonreturn to zero (NRZ) PCM data, but the clock pulse must be equal to or shorter than the data pulse. Clock pulses must also be properly synchronized.
2. The circuit in this innovation is applicable to any pulse code modulation communications system or to the digital computer field. It reduces the required bandwidth to an absolute minimum and provides a smooth transition in or out of two frequencies.
3. For further information about this innovation inquiries may be directed to:
   Technology Utilization Officer
   Goddard Space Flight Center
   Greenbelt, Maryland 20771
   Reference: B63-10511

Patent status: NASA encourages the immediate commercial use of this invention. It is owned by NASA and inquiries about obtaining royalty-free rights for its commercial use may be made to NASA Headquarters, Washington, D.C., 20546.

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