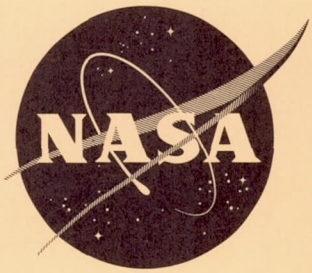

TECHNICAL NOTE

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MICROPOWER TRANSISTOR LOGIC CIRCUITS

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CONTENTS

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SUMMARY

Low-power logic, as discussed in the few available references, is primarily concerned with computer-type applications in which high operating rate is the dominant prerequisite. Logic circuits for satellite and space-vehicle use are less demanding of speed but considerably more limited in power consumption. An analysis of the logic circuits suitable for the latter type of application and experimental results to verify the analysis are presented.

Conventional logic circuits and the limitations of scaling them down to micropower operation are discussed. Special attention is given to two basic circuits differing from those normally used in that their output is not limited by a resistor forming the direct-current load of the stage. Instead, two transistors alternately clamp the output to the supply voltage or to ground. One of these circuits is an adaptation of a high-efficiency multivibrator design; the other is an original circuit specifically developed for micropower use.

A detailed analysis of these two circuits is presented, and a variety of logic elements is derived from them. Sufficient information on the limitations of these circuits, device parameters and their variation, and design criteria are presented for the design of a number of useful micropower circuits suitable for space applications. Operating rates of these circuits range from 1 to 100 kilocycles and power levels from 1 to several hundred microwatts.

INTRODUCTION

The use of transistors as the active elements in logic circuits has brought about considerable improvement in their reliability, size, speed of operation, and power dissipation. There are still, however, a number

[1]Information presented herein was offered as part of a thesis in partial fulfillment of the requirements for the degree of Master of Science to Case Institute of Technology, Cleveland, Ohio, June 1962.

of applications in which the tens to hundreds of milliwatts dissipated by conventional transistor logic circuits are much too great. These applications fall into two distinct groups - those in which the dominant factor is thermal dissipation and those in which power consumption per se must be minimized.

Problems concerning thermal dissipation result largely from the desire to miniaturize equipment. Techniques for microminiaturization presently being developed promise component densities approaching 1 million per cubic foot. If this microminiaturization were accomplished with conventional circuitry, the resultant power densities would reach several kilowatts per cubic foot. Cooling problems for such a system become formidable and necessitate additional equipment, which thereby defeats the original objective of small size. Alternatively, circuit elements capable of very high temperature operation might be employed. At present, neither of these alternatives is particularly promising. The only remaining approach is to decrease power consumption per element, preferably by several orders of magnitude. This solution has the additional advantage of a gain in reliability because the failure rate for components is approximately halved for every 10° C decrease in temperature. Since most of the thermally limited applications occur in computing equipment in which no loss of speed can be tolerated, large power savings will be difficult to attain in this area.

The second important need for low-power circuitry has resulted from man's exploration of space. As the expected life of satellites has been increased, so has the total power required. The satellite experiments now being planned demand a considerable amount of logic circuitry to handle this data (ref. 1). Even with the larger payloads soon to be available, there are still considerable advantages to be gained through decreasing power requirements. The prospect in this area is more promising than in the computer field since the fact that speed requirements are not so high allows trading some speed for a considerable reduction of power. Lower-power operation can also lead to improvement of reliability, which possibly might foster further savings from a decrease in the required system redundancy.

Deep-space probes are even more critical of power requirements. The fact that, as the distance from the sun increases, available solar power decreases makes it necessary either to carry an auxiliary power source or to reduce power consumption drastically. It is usually desired to make some continuous measurements, to record the data, and to transmit it back to earth. Since much of the data may be highly redundant, considerable power is wasted in storing and transmitting it. The next generation of space data systems will therefore probably include special-purpose computers to reduce the data before transmission. If suitable low-power logic is available for the design of these computers, considerable savings of overall system power could probably be effected concomitant with an increase in data capacity.

Data systems is only one of the areas that will benefit from micropower logic. A growing demand exists for space-vehicle control systems. Included are command systems for ground control, as well as equipment for on-board guidance computation and control (ref. 2). When these systems become more complex, as they must for missions such as a lunar landing, the need for micropower logic will become increasingly urgent.

This specific study was motivated by a requirement for a low-power satellite data system for micrometeorite detection. Since the requirements of this system are much the same as those of other space systems, a general investigation of micropower circuitry suitable for space applications was pursued. Results of this study can be applied to the design of general logic blocks suitable not only for this specific system but also for any general digital system, including those for on-board computation and control. In this report, various means of attaining micropower operation are surveyed, several are considered in detail, and design procedures are shown for a few specific logic blocks suitable for space use.

Environmental conditions in space will necessarily limit this investigation to components operable over a wide temperature range, namely, those fabricated of silicon and possibly gallium arsenide. Saturated logic circuits operating at repetition rates of 1 to 100 kilocycles will be considered. These circuits must be capable of operation at power levels below 1 milliwatt per stage; hence, these low power levels justify the name of micropower logic.

PRESENT STATE OF THE ART

Computer Field

The first area of application for low-power logic to be considered is the computer field. This area, in which low power is sought as a means of circumventing thermal problems, represents the larger portion of the work in the field. Because little or no speed reduction can be tolerated, operating power levels have been decreased only to the 1- to 10-milliwatt range in most cases. The operation rate, which is in the range of 1 to 10 megacycles, results in a power-per-operation figure somewhat comparable with that of micropower circuits. Many of these circuits are conventional logic circuits that have been scaled down to operate at lower supply voltages and operating currents.[2] This approach can be effective within certain limits. The supply voltage for a given circuit is usually decreased to the limit imposed by the coupling

[2]The term conventional circuits as used herein refers to circuits that provide their output from the collector of a single transistor that has a pure resistance as its direct-current load.

networks or the transistors. Component values can then be adjusted to minimize the limitations imposed by circuit time constants. Using this approach with transistors selected for their low-power performance results in considerable power reduction and little loss of speed.

Scaled-down circuits using this approach are described in references 3 and 4. These references give designs that use a special low-power germanium transistor, draw 1 to 7 milliwatts, operate between 200 kilocycles and 10 megacycles, and use various forms of logic, including RCTL and DCTL. A considerable improvement in performance was obtained by using a hybrid transistor-tunnel diode circuit (ref. 5). A NOR circuit of this type (fig. 1) with a fan-in of 2 and a fan-out of 4 was operated from a 1.5-volt supply with a dissipation of 3.5 milliwatts. The repetition rate was approximately 15 megacycles. Another new circuit, reported in reference 6, uses backward diodes to couple stages (fig. 2). Because of the low voltage buildup required by backward diode coupling, this circuit has the lowest potential operating voltage of any. Maximum operating rate of a typical stage operating at 10 microamperes and 3 volts is 100 kilocycles to 1 megacycle.

True Micropower Circuits

All the aforementioned circuits employ transistors not too different from conventional types. In only one case has an attempt been made to fabricate a transistor specifically suited for true micropower operation (ref. 7). This developmental silicon transistor is reported to have a current gain greater than 0.9 at a collector current of 1 microampere and extremely small input and output capacitances. A number of conventional logic circuits using this transistor have been built that require a current of 1 microampere per stage at a voltage of 1 volt. The operating rate is about 1 kilocycle.

Comparison of Logic Circuits

It has been demonstrated (ref. 7) that the direct-current operation of logic elements can be extended to extremely low power levels. A number of practical limitations exist at these levels. Large collector load resistors must be used to attain the low currents mandatory at micropower levels. As the operating current decreases, the output impedance of the circuit must increase; the input impedance also rises. It is now possible that externally generated noise will affect circuit operation. Coupling also is more difficult because of low voltage swings.

As power levels are decreased below a few milliwatts, the circuit speed becomes limited by its time constants, rather than by the rise time of the transistor. The rise time of the circuit, which is the

turn-on time of the transistor, is still relatively fast. The fall time, however, is determined by the time constant of the load in parallel with the collector resistor, collector capacitance, and any distributed circuit capacitance. With a 1-megohm collector resistor and a somewhat larger load resistor, it is easy to see why time constants of many microseconds can prevail. Another way of looking at this same problem is on the basis of impedances. In the on state, the transistor presents a low output impedance. Unfortunately, in conventional circuits, this state is not the one in which power is being delivered to the load. With the transistor off, the output impedance is that of the collector resistor, in this case, high. This state is also the one that must furnish power to the load. The power output can therefore never be more than one-fourth that dissipated with the transistor on; power efficiency is low.

One solution to these problems is to replace the load resistor with an element that would have a large impedance when the transistor is on and a low impedance in the opposite state (refs. 8 and 9). The power wasted with the transistor on would be minimized and the circuit could deliver maximum power to the load. This can be accomplished by using a second transistor as the load for the first. If the two transistors are of a complementary type, the same signal swing that will turn one on will turn the other off. Since both the rise and the fall times of the circuit will be the time of turning on a transistor, they can be short, regardless of the circuit power level. Such a circuit has been used as a high-efficiency multivibrator and forms the basis of the work presented in the section COMPLEMENTARY TRANSISTOR LOGIC CIRCUITS. A second possibility would be to use two transistors of a similar type in a comparable connection. The details of this circuit design and the performance will be presented subsequently.

Another approach to higher-efficiency, low-power circuits is to use a nonlinear collector resistor. Suitable nonlinear resistances for this application could be fabricated by using either tunneling- or field-effect devices (refs. 10 and 11). Operating speed, particularly with the tunneling-effect device, would be potentially fast. The same devices could also be used to improve coupling between stages and to implement logic functions (ref. 12).

Three general types of logic circuits have been mentioned: conventional circuits using resistive loads, circuits using nonlinear collector loads, and "active-load" circuits that lend themselves to fast low-power operation, although not without a number of difficulties. Primarily the latter-type circuits, as well as general limitations of coupling, operating speed, and minimum power, will be considered herein.

TRANSISTOR LIMITATIONS AND SELECTION CRITERIA

From a consideration of the passive part of the circuit by itself, it is evident that logic circuits can be scaled down for low-power operation to a degree primarily dependent on the characteristics of the transistors employed. Decreasing the supply voltage will in no way affect the passive time constants. It will, however, change the currents, which in turn govern transistor operation. It is therefore necessary to consider the effects of the operating conditions on the transistor response.

Direct-Current Operation

Two parameters are dominant in determining the limits on direct-current operation: current gain and leakage current. The latter parameter is the one that limits the type of device to be used for micropower operation. The section PRESENT STATE OF THE ART cites several low-power circuit designs, most of which use germanium transistors. Collector leakage current for a low-leakage germanium transistor is typically 20 microamperes at 55° C. Germanium transistors are obviously eliminated for micropower use in cases in which operating currents will be in this same range or lower.

In order to assure stable operation of a logic circuit, the transistor leakage current should be at least an order of magnitude below the operating current at maximum temperature. Of the presently available silicon transistors, the best ones exhibit leakages of the order of 10^{-4} microampere at 80° C. Even if a large safety factor is allowed to compensate for end-of-life degradation, such a transistor will permit operation at collector currents well under 1 microampere. Levels this low may not be practical for other reasons.

The second major limitation on micropower operation has been the direct-current gain. This gain is a function of collector current that shows a maximum in the range of 1 to 10 milliamperes for most low-power transistors. At collector currents much below about 100 microamperes, the current gain of most transistors falls to unusable values. This fall off is not nearly so pronounced in the recently introduced planar transistor. Selected silicon planar transistors can be obtained that exhibit useful current gains below a collector current of 0.1 microampere. In addition, the fact that the temperature dependence of gain is not too large allows low-temperature operation. Typical transistor data sheets specify a decrease in current gain of only two to one at -55° C.

One other factor that could conceivably limit the minimum operating voltage is the dependence of current gain on collector voltage. Whereas some transistors show a drop of gain at voltages of 1 or 2 volts, the silicon planar units mentioned previously for collector currents below

1 milliampere operate efficiently at any collector voltage large enough to permit coupling between successive stages.

This brief consideration indicates that it should be possible to operate presently available silicon transistors at extremely low power levels (<1 μw) if only direct-current operation is considered. Selection criteria and detailed transistor specifications will be discussed subsequently.

Switching-Speed Limitations

As the operating current of a circuit is decreased below a certain minimum, the transistor time constants tend to increase. This result is predominantly due to the increasing effects of transistor capacitances, as readily shown by considering the transistor as a charge controlled device (refs. 3, 13, and 14). When this concept is used, it is apparent that in order to turn on the transistor sufficient energy must be supplied to charge the input capacitance to the required voltage level for conduction. For the common-emitter connection, this input capacitance consists of two parts. One is the transition capacitance formed by the junction depletion layer that is bounded by charged regions forming the capacitor "plates." Since the thickness of this depletion layer varies with junction voltage, the transition capacitance is nonlinear. It is approximately proportional to $V_j^{-1/2}$ for abrupt junctions and $V_j^{-1/3}$ for gradual junctions. The second capacitive effect is due to the minority carrier charge stored in the base region and is directly proportional to the current. Together, these two effects form a capacitor, which must be charged to the voltage required for transistor turn on.

Figure 3 relates the required turn-on charge to the value of speedup capacitor required for various values of direct-current bias. Not only must the base-emitter capacitance be minimized, but so must the reverse turn-off voltage, if maximum speed is desired. Ideally, on the basis of minimum turn-on time, the transistor should be slightly forward biased, but not sufficiently to cause conduction. A convenient value for silicon transistors is 0.1 to 0.2 volt, which corresponds to the collector saturation voltage. This voltage allows the elimination of the reverse bias supply and at the same time minimizes the value of speedup capacitor required.

Another capacitance of interest is the collector-base capacitance C_{ob}. Since C_{ob} is a transition capacitance, it behaves in the same manner as the base-emitter transition capacitance. In high-frequency transistors, C_{ob} may be of approximately the same size as C_{ie}. The effect of C_{ob} on the transient response time can be much larger, however, particularly for the common-emitter configuration, as a result of

the Miller effect, which multiplies its capacitive effect by the voltage gain of the circuit. It is therefore important to select a transistor with as low a value of C_{ob} as possible and also to use every precaution to minimize any external capacitance from collector to base. Lowering the supply voltage will increase C_{ob} slightly, as shown in figure 4.[3] If power is to be decreased without a loss of speed, the value of the collector resistor would need to be decreased.

The limitations imposed by these capacitances show that any increase in circuit resistance that causes the RC (resistance-capacitance) time constant concerned to approach or to exceed the response time of the transistor will decrease the output response time.

Most true micropower circuits will operate at such levels that they will be limited by these RC time constants and not by the intrinsic transistor parameters. For this reason, the specified alpha and beta cutoff frequencies are poor measures of the suitability of a device for micropower use. If these parameters are calculated from the equivalent circuit, including all capacitive effects, they then become a valid means of comparison.

Transistor-Selection Criteria

Summarizing the results of the preceding analysis leads to the following selection criteria for a micropower transistor:

(1) Direct-current gain should be as high as possible at the required operating current. This parameter in conjunction with leakage will determine the lower limit of direct-current operation.

(2) Collector leakage current should be at least an order of magnitude below the required operating current at the maximum operating temperature.

(3) Input capacitance C_{ie} and output capacitance C_{ob} should be the lowest attainable, as they limit the maximum operating rate and transient response. For the common-emitter connection, C_{ob} should be minimized at the expense of C_{ie}, if necessary, since the Miller effect makes its contribution to circuit response large.

(4) Base-emitter voltage V_{BE} and collector saturation voltage V_{CE} should be low at the required operating conditions. These parameters are not so important as the three preceding parameters. Their

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[3] A number of transistor and diode characteristics are included in reference 15; a few are presented herein. Further work characterizing semiconductor devices for micropower applications is currently in progress at the Lewis Center.

effects predominantly limit the coupling requirements, as will be shown in the next section. A low temperature coefficient of V_{BE} is also desirable.

(5) For saturated operation, the storage time constant τ_s should be small. In most cases, transistors meeting the low capacitance requirements will be high-frequency units and therefore will also meet the requirement of low τ_s.

A number of transistors have been evaluated for micropower operation. The original selection of which to evaluate was somewhat hampered by the lack of published specifications of the parameters of interest, particularly at low voltage and current levels. Originally, transistors were selected on the basis of high current gain and were then evaluated at low operating currents. From an evaluation of 25 transistors, one PNP, the Fairchild S-4528, and one NPN, the S-4529, were selected as being the best, and complete tests were run to determine the necessary parameters. All experimental work reported herein used these two types of transistor.

COUPLING LIMITATIONS AND COMPENSATION METHODS

Factors Limiting Minimum Supply Voltage

Operation of logic circuits at the lowest possible voltage level is desirable in order to minimize power consumption. This level will be primarily determined by the requirements of the coupling circuit. Sufficient output voltage must be available to turn on the next stage, with allowances made for losses in the coupling network. Determining factors are the input voltage necessary to turn on a stage, the voltage drop in the coupling network, the voltage drop across a current-limiting element if one is present, and the output voltage drop due to loading. Just as important as the values of these factors are their tolerances and their variations with temperature and time. The effect of tolerances is to increase the minimum permissible power level of a circuit (refs. 16 and 17). Variations with temperature have the same effects and in practice become much more limiting for circuits that must operate over a wide temperature range. The effect of each of these variables will be discussed next, and typical values will be given. Finally, approximate lower limits on voltage will be determined for some typical circuit configurations.

Variables and Typical Values

Starting at the input of a logic stage, the first variable of interest is the base-emitter voltage V_{BE}. Figure 5 shows the variation

of V_{BE} with base current and temperature. It should be noted that there is considerable variation of V_{BE} with temperature. This variation, along with variations between transistors, makes it desirable to use a current source for drive. If the output voltage of the preceding stage is large compared with V_{BE}, a resistor is all that is necessary. This solution is the usual one. With this approach, the lower limit on drive voltage is determined by the allowable base-current variation. The minimum drive voltage for a given variation in base current is given by the formula

$$V_1 = \frac{k\overline{V_{BE}} - \underline{V_{BE}}}{k - 1} \qquad (1)$$

where k is the ratio of maximum to minimum base currents and the overbars and underbars denote maximum and minimum values of the variable, respectively.

Decreasing the base current has the effect of increasing the temperature coefficient of V_{BE}, which appears to reach a maximum of nearly 2 millivolts per ^{o}C for currents of the order of 0.5 microampere for both the PNP and the NPN transistors. This value is somewhat lower than that for other silicon transistors, which may approach 3 millivolts per ^{o}C. It is evident from equation (1) that both the temperature coefficient and the absolute value of V_{BE} should be small to minimize the required drive voltage. The decrease in absolute value of V_{BE} with decreasing drive current is large enough to compensate for the increase in temperature variation so that the drive voltage required will decrease for decreasing base currents.

As a typical example, the following operating conditions may be considered:

Base current, I_B, μa	0.5
Maximum base-emitter voltage (at 0° C), $\overline{V_{BE}}$, v	0.590
Minimum base-emitter voltage (at 50° C), $\underline{V_{BE}}$, v	0.505
Ratio of maximum to minimum base currents, k	1.5

For these values, equation (1) gives a minimum drive voltage of 0.76 volt. The value used for the constant k must be determined by the allowable variation in power dissipation. If this variation is very critical, a value of 1.5 may be too large, since, for a negative temperature coefficient of V_{BE}, the maximum dissipation occurs at maximum operating temperature.

If diode logic is used in coupling transistor stages, the same considerations must be applied to the diode. A typical circuit of this type is shown in figure 6. In general, the variations will be very

similar to those of V_{BE}, as shown in figure 7. The forward drop across a high conductance diode can be about half as large as the transistor V_{BE} at the same current. The temperature coefficient is larger, however, and reaches a maximum of nearly 3 millivolts per °C at a current of 1 microampere for the silicon diodes tested.

For circuits that are to be operated over a wide temperature range, some improvement can be obtained by using gallium arsenide diodes. Their forward current-voltage characteristic shows that they exhibit a significantly smaller temperature coefficient than silicon diodes, as shown in figure 8. A value of 1.8 millivolt per °C was observed at a current of 0.5 microampere. At present, the temperature coefficient varies considerably from unit to unit. Since these diodes are quite new and only in pilot production, this variation can be attributed to process variations and may disappear as manufacturing processes improve.

The same equation for drive voltage used with V_{BE} can be used if the sum of base-emitter voltage and diode drop is substituted for V_{BE}. Alternatively, the values of diode drop can be substituted for V_{BE}, in which case the resultant voltage will be that which must be added because of the coupling diode.

As an example, the additional voltage drop necessary to compensate a type FD-600 diode is calculated by using the following values:

Diode current, I_D, μa	0.5
Maximum diode voltage (at 0° C), $\overline{V_D}$, v	0.324
Minimum diode voltage (at 50° C), $\underline{V_D}$, v	0.174
Ratio of maximum to minimum base currents, k	1.5

Using equation (1) gives the value of 0.624 volt. If a gallium arsenide diode with a 1.8 millivolt per °C temperature coefficient had been used, the voltage would have been 0.44 volt.

Diodes used in coupling circuits impose a second practical limit on low-level operation. Presently available diodes have reverse leakages about three orders of magnitude greater than the lowest transistor leakage currents. The minimum current level will thus be limited to the microampere range, particularly since several diodes are usually used together in the base circuit of a transistor in which drive currents are proportionally small. If it is practical to make transistors with leakages in the picoampere range, it is also practical to make equally good diodes. This limit is therefore temporary, as planar passivated diodes of similar construction and performance as the transistors used in this study should soon be available.

Backward diodes can also be used as coupling devices, as shown in figure 2. Their very low forward drop, of the order of 0.1 volt, makes them attractive for low-level logic. In addition, the temperature coefficient of forward drop is small enough to be neglected. Characteristics in the reverse direction, however, are not nearly so ideal. As shown in figure 9, the reverse characteristics are similar to the forward characteristics for a conventional diode, with the exception of the small peak at low reverse voltage. This peak limits the permissible reverse voltage to about 0.5 volt for a silicon device and to a slightly higher value for gallium arsenide. The minimum reverse peak leakage current available is approximately 1 to 2 microamperes, which somewhat limits present applications.

In the case of logic circuits in which the output is derived from a saturated transistor connected to the supply voltage, one further variable needs to be considered, the transistor saturation voltage drop V_{CE}. Typical values are 0.1 to 0.2 volt, depending on the amount of excess base drive used. The variation of saturation voltage with temperature is small enough to be neglected, compared with the other parameter variations. It is then necessary only to add the saturation voltage to the required drive voltage to obtain the supply voltage.

Minimum Voltage Levels

All logic circuits can be grouped by considering the number of elements requiring compensation that appear in series. As an example, a single transistor inverter would be characterized as one V_{BE} drop. This grouping then becomes a convenient way of specifying the minimum voltage necessary. The following table shows the computation of minimum supply voltages necessary for a variety of circuit groups by using the characteristics for the S-4529 transistor and the FD-600 or the DGS-54 diode:

Ratio of maximum to minimum base currents, k	Temperature difference, ΔT, ^{o}C	Minimum supply voltage required for temperature compensation, v		
		Transistor V_{BE}	V_{BE} + silicon diode	V_{BE} + gallium arsenide diode
1.5	50	0.75	1.37	1.18
	100	1.04	2.07	1.69
1.2	50	1.01	2.11	1.71
	100	1.66	3.65	2.86

The supply voltage is assumed to be fixed, and all compensation is due to the drop across a coupling resistor. Approximately 0.1 volt should be added to each of the voltages in the table if the output is supplied from a saturated transistor.

Speedup Capacitors

In order to maintain fast response through the coupling network, the series coupling resistor is usually bypassed. The necessary capacitor value is determined by the voltage drop across the coupling resistor and the charge necessary to turn on the next stage. As shown in figure 3, the required value of speedup capacitor varies only slightly as the current is changed. The coupling resistor, however, varies inversely as the base current. Decreasing the operating current causes a rapid increase in the RC time constant, which in turn limits the maximum repetition rate of the circuit. On first consideration, reducing the value of the coupling resistor by decreasing the voltage drop across it would appear to decrease the coupling circuit time constant, but this is not the case. The speedup capacitor must supply a fixed charge determined by the turn-on requirements of the transistor. Since this charge is equal to the product of the coupling resistor drop and the capacitance, decreasing the resistance will decrease the voltage drop and thus require a proportional increase in capacitance. The time constant is left unchanged. Decreasing the supply voltage while maintaining the operating current will therefore not result in any increase in maximum operating rate. This rate is fixed once the base current and transistor are chosen.

Equating the charge stored in the speedup capacitor to that necessary to turn the transistor on results in the expression for the coupling circuit time constant:

$$R_C C_C = \frac{V_{BE} C_{IN}}{I_B}$$

$$= \frac{Q_{ON}}{I_B} \qquad (2)$$

where R_C is the coupling resistor, C_C is the speedup capacitor, V_{BE} is the base-emitter voltage for turn on, and C_{IN} is the sum of all capacitances acting between the base and the ground. The second form of the equation is convenient if the value of charge necessary to turn on the transistor Q_{ON} is specified. The value of I_B/Q_{ON} is therefore proportional to the maximum repetition rate attainable, and Q_{ON} for a given base current can be used as a figure of merit for comparing transistors.

Logic Forms and Their Limitations

Logic circuits can be separated into two classes on the basis of the coupling circuits used. In the one case, no logical function is accomplished by the coupling network, which serves only as a link between successive logic elements. The best example of this class is all-transistor logic, which uses a separate transistor for each input. Such a configuration has good low-voltage characteristics since the coupling drop need be sufficient only to compensate for variations in the transistor base-emitter voltage. If this drop can be made sufficiently low, a single resistor is all that is necessary for coupling. The more widely used logic circuits fall into the second category, in which the coupling network provides the desired logic function and the transistor provides gain and inversion.

A widely used form of logic, which is a form of NAND or NOR logic, uses resistors in a Kirchhoff adder configuration to obtain the AND and OR functions and a transistor for inversion. The resistive adder circuit is particularly inefficient since the off inputs load the one that is on. Also, for a fan-in of M, the drive voltage must be larger than MV_{BE}, which necessitates much higher voltages than desirable. This type of circuit is therefore not well suited to micropower logic.

Direct-coupled logic would seem to be good at micropower levels because of the low voltage required, but this is not the case in practice. Since several bases are tied directly together in interconnecting logic elements, their voltages must be the same. Small variations in the transistor base-emitter characteristic will therefore cause large variations in base current. Since sufficient current must be provided to turn on all transistors, some will be considerably overdriven and power will be wasted.

A much more practical logic form for micropower circuits is diode logic, which was shown in figure 6. The use of a unilateral device eliminates the shunting effect of the off inputs and reduces the input drive voltage required. One disadvantage for micropower use, however, is that removing the inputs does not drive the transistor off. With the inputs at ground potential, the diodes cease to conduct and therefore leave the base circuit isolated from the previous stage. The transistor input capacitance and any stray circuit capacitance must be discharged before the transistor will turn off. If the transistor is overdriven on, there will be sufficient charge stored on the transition capacitance and as excess minority carriers in the base to maintain conduction after the input is removed. To dissipate this charge quickly, R_1 and R_2 must be relatively small. At low power levels, a value of R_1 that will ensure fast turn off may be small enough to shunt a large part of the input current away from the base. The design of this type of circuit will therefore require a compromise between speed and power.

Current Stabilization

Previous sections have indicated that the lower limit on drive voltage is a function of the variation in base-emitter drop, diode forward voltage, and circuit tolerances. The fact that no particular difficulty exists in holding the latter to about 1 percent suggests that drive voltage could be lowered if the semiconductor temperature effects can be compensated for. Several methods of compensation will be suggested.

All the temperature effects mentioned previously have a negative variation with temperature. Substitution of a positive temperature coefficient resistor for the coupling resistor could therefore compensate the circuit. A suitable device for this purpose is manufactured by Texas Instruments under the name Sensistor. It is a silicon resistor with a positive temperature coefficient of 0.7 percent per ^{o}C. For full compensation, the voltage drop across the resistor must be properly chosen. Compensating for a temperature variation of 2 millivolts per ^{o}C would require a drop of 0.286 volt across the Sensistor to give zero change in operating current. If perfect compensation is not necessary, it will be possible to lower the coupling resistance considerably and still to maintain a small current variation.

Ideally, the coupling network should provide a constant current drive to the following stage or possibly a slightly increasing drive with decreasing temperature to compensate for loss of gain. Using a temperature-dependent element to control the supply voltage is one way to achieve this objective, but this will help only slightly for space-type applications in which the power drain from a fixed-voltage supply must be minimized. Conversely, in computer applications, in which the dissipation within the logic element is important, it will be quite effective. In this application, the supply voltage would be lowered at increased temperatures while the same current is maintained, which would decrease the dissipation when that decrease is most desirable.

A third means of compensation is the use of a device with an inherent constant-current characteristic. Two such devices exist, although lack of information on their temperature characteristics makes their value questionable (refs. 10, 11, and 18). One of these devices uses the field effect, the other, tunneling to obtain a region of relatively constant current. Both devices are still laboratory curiosities and little data on them are currently available. A tunneling-effect device similar to the backward diode appears promising since it should have both low sensitivity to temperature and fast response.

SIMILAR TRANSISTOR LOGIC CIRCUITS

With the requirements for an ideal low-power logic circuit considered, an attempt was made to develop a new circuit fulfilling as many of these requirements as possible. Particular emphasis was placed on using only one polarity of transistor (PNP or NPN) for two reasons: (1) At the time this project was undertaken, it was impossible to obtain complementary silicon transistors with sufficiently good parameters. There were several good NPN transistors on the market but no comparable PNP transistors. (2) The radiation resistance of NPN transistors is thought to be superior to that of comparable PNP transistors, which makes them more suitable for space environments.

Basic Inverter Circuit

The basic form of the circuit developed is shown in figure 10. It is an inverter circuit from which can be built all necessary digital logic blocks. Operation is as follows: The input is assumed to be at ground potential. Transistor Q_1 is therefore turned off except for leakage current, which can be neglected. Current from supply V_{BB} flows through R_1 and into the base of transistor Q_2 and turns it on. If V_{BB} is sufficiently larger than V_{CC}, Q_2 can be driven to saturation, which clamps the output to very nearly V_{CC} and provides a low output impedance. This condition will be referred to as the "on state." It should be noted that in the on state there is no path to ground other than that provided by the load, which results in 100-percent efficiency of current transfer to the load. For low-power use, it is important that none of the drive current for Q_2 be bypassed around the transistor. This is accomplished, while proper coupling is maintained, by conventional diode D_1 and backward diode D_2, which provide essentially an open circuit from base to emitter.

If a positive voltage is now applied to the input, transistor Q_1 will turn on. The negative-going signal appearing at the collector of Q_1 is coupled to the base of Q_2 by diode D_1, which behaves as a constant-voltage-drop coupling device. This signal cuts off transistor Q_2, and it ceases to supply load current. Simultaneously, the drop in voltage at the collector of Q_1 discharges the load capacitance through back diode D_2. Without diode D_2, the fall time of the output would be determined by the time constant of the load and any stray capacitance present. The input is again grounded and transistor Q_1 is cut off. Resistor R_1 pulls the base of transistor Q_2 toward V_{BB}. Transistor Q_2 now acts as an emitter follower and provides a large current gain to drive the load.

Output impedance of this circuit is always low. In the on state, it is the impedance of a saturated transistor; in the off state, it is

that of a saturated transistor in series with a backward diode. This low impedance not only provides good rise and fall times, but also provides an output swing that is tightly clamped to fixed levels in both on and off states. Since the power efficiency of the circuit is high, it can deliver several times its standby power to the load. A further advantage is that the input is into a single transistor, which allows a number of useful modifications.

Direct-Current Analysis

The direct-current-output capabilities of this circuit are extremely good. Since two stages, each capable of current amplification, are cascaded, very little input current is necessary. Alternatively, transistors with lower gains may be used or operation at lower currents, at which H_{fe} drops, may be practical.

The only serious limitation on minimum operating current is imposed by the reverse peak current of the backward diode used. Of the backward diodes currently available, the lowest reverse peak currents are approximately 1 microampere. This value, then, constitutes the amount of base drive that will be bypassed around the upper transistor and sets the lower limit of the base drive. In the following analysis, an ideal backward diode will be assumed for simplicity.

The minimum collector supply voltage V_{CC} that can be used in a particular application will be determined predominantly by the method of interstage coupling as has been shown. If it is assumed that this voltage is already determined, it is then necessary to select a value for V_{BB}. For minimum power dissipation and a given base current in the on state, V_{BB} should be only slightly greater than $V_L + V_{BE}$, which leads to a small value of R_1, which in turn causes a high dissipation when transistor Q_1 is turned on. These two conflicting requirements indicate that there must be an optimum voltage for V_{BB}. Appendix A shows that this optimum value is given by

$$\left(V_{BB}\right)_{opt} = V_{BE} + V_L + \sqrt{\frac{1}{2} V_L(V_L + V_{BE})} \qquad \text{(A11)}$$

If only the dissipation in R_1 is considered, a somewhat simpler approximation results, which is the same as the exact value with the V_{BE} term under the radical eliminated. This equation then simplifies to

$$\left(V_{BB}\right)_{opt} \cong 1.7\ V_L + V_{BE} \qquad (3)$$

which should not be used for determining $\left(V_{BB}\right)_{opt}$ for circuit design but is convenient to use in making other approximations. In practice,

the values obtained from these two equations will differ by a few tenths of a volt at most.

The dissipation from the V_{BB} supply that does not contribute to the output (eq. (A6)) is plotted against V_{BB} in figure 11 for some typical circuit values. Note that the minimum, which is quite broad, makes it possible to modify the choice of V_{BB} somewhat to meet other requirements without paying a large penalty in power dissipation.

For a given input current $I_{b,1}$, the maximum load current is

$$\overline{I}_L = I_{b,1}\left(\frac{V_{BB} - V_{BE} - V_L}{V_{BB} - V_D - V_{CE}}\right)H_{fe}(1 + H_{fe}) \tag{4}$$

where H_{fe} is chosen as the forced gain necessary to provide the desired degree of saturation. Using equation (3) and letting $V_{BB} = V_D + V_{CE}$ simplifies the expression to

$$\overline{I}_L \cong 0.4\ I_{b,1}H_{fe}(1 + H_{fe}) \tag{5}$$

If R_1 is considered to be the load resistor for Q_1, it is much the same as a conventional inverter circuit. Transistor Q_2 adds to this stage a current gain of $H_{fe} + 1$ and shows that for the same input current this circuit is capable of approximately $H_{fe} + 1$ times the output current of a conventional common-emitter inverter. Full advantage of this high current gain through the circuit cannot be taken if the minimum fall time is desired. In this case, the two base currents must be more nearly equal.

Power Efficiency

Power efficiency will be defined as the power actually delivered to the load divided by the total power input and will be calculated for the case of a 50-percent duty cycle. The total dissipation from the power supplies, not including that of the load, is

$$P_{loss} = \frac{I_{b,2}}{2}\left[\frac{V_{BB}(V_{BB} - V_D - V_{CE})}{V_{BB} - V_L - V_{BE}} + V_{BB} - V_L\right] + \frac{V_{CE}I_L}{2} \tag{6}$$

and the output power is

$$P_{out} = \frac{1}{2}V_L I_L \tag{7}$$

Using equation (3) and letting $V_{BE} = V_D + V_{CE}$ leads to

$$\eta = \frac{V_L(1 + H_{fe})}{V_L(5.8 + H_{fe}) + 3.4\ V_{BE} + V_{CE}(1 + H_{fe})} \tag{8}$$

which is a reasonable approximation for the circuit efficiency under direct-current conditions. The H_{fe} used must be the forced value determined by the operating conditions. Actual efficiencies will vary somewhat from this value because of capacitive loading effects, particularly at high repetition rates.

Transient Response

The direct-current design for this type of circuit is relatively straightforward and can be accomplished with the preceding formulas and data. Characterization of the transient response is not nearly so simple. The derivation of an expression for the turn-on time is presented in appendix A. By making a number of simplifications, justified on the basis of relative circuit values, an explicit expression for turn-on time is obtained:

$$t_r = -R_1C_1 \left(\frac{1.2 + \beta}{4.33 + \beta}\right) \ln \left(\frac{V_{BB} - 0.9\ V_L - V_{BE}}{V_{BB} - V_{BE}}\right) \tag{A22}$$

This equation clearly shows the desirability of making R_1 small. Where minimum rise time is required, V_{BB} and R_1 should be decreased as much as allowed by the increased power loss and decreased current stability with variation in V_{BE}.

Calculation of the fall time for this circuit is considerably more complicated than that of the turn-on time. Turn on of Q_1 will quickly pull the base of Q_2 toward ground and also start to discharge the load capacitance. Transistor Q_2, having been saturated, will exhibit a storage effect. During this period, Q_2 will still supply load current, while Q_1 tries to pull the output to ground. The result is that a large current is drawn from the supply until the upper transistor turns off. It is impractical to attempt an exact solution for the fall time since this solution would involve both transistors and most circuit components. The number of simplifications necessary in order to obtain a workable solution defeats the analysis. Attempts at simplified solutions have resulted in fall times much shorter than those determined experimentally.

Basic Inverter Data

Several inverters were "breadboarded" and tested to check the equations derived by using the circuit of figure 10. Operation over a wide range of power levels was achieved by determining the circuit constants at midrange and then increasing or decreasing all resistor values in proportion. This procedure made the experimental work, as well as the calculations, somewhat easier and gave a check on the effects of off-design operation for comparison with the calculated values.

The output voltage was selected as 0.9 volt, which is about as low as is practical over the range of currents used in this test. Adding 0.1 volt for V_{CE} dictates a value of 1.0 volt for V_{CC}. Assuming a nominal value of 0.6 volt for V_{BE} results in an optimum base-supply voltage of 2.32 volts from equation (All); the value used was 2.0 volts. As operating rate is usually important in low-power designs, an attempt was made to keep it high by using equal base currents for fast turn off as well as turn on. The value of speedup capacitor was estimated from figure 12 and the load was chosen to approximate a fan-out of three. Actually, the loading was somewhat greater, because the load was returned to ground instead of to the base of a transistor. The observed and computed rise times are compared in figure 13. A tabulation of the results of this test is shown in the following table:

Experimental data								Calculated rise time, t_r, μsec
Resistance, $R_1 = R_2$, ohms	Capacitance, C_1, pf	Current, I_L, μa	Capacitance, C_L, pf	Rise time, t_r, μsec	Fall time, t_f, μsec	Total power, μw	Base current, I_b, μa	
2.2M	--	1.3	---	----	---	----	0.254	25.6
1.0M	--	2.7	---	----	---	----	.52	12.1
470K	--	6.0	---	----	---	----	1.06	5.85
220K	20	13	60	3.3	7.6	19	2.18	2.83
100K	22	27	78	1.9	2.7	39	4.5	1.32
47K	25	60	110	.8	1.2	86	9.14	.63
22K	25	130	110	.45	.9	170	18.6	.31
10K	35	270	160	.2	.3	426	39	.14
4.7K	50	600	210	.1	.3	760	79	.07
2.2K	50	1300	210	.05	.1	1330	159	.03

The rise times were computed by using equation (A22). A possible explanation for the discrepancy between experimental and calculated data may be found in the determination of the C_1 term in this equation. It is composed of $C_{b'c}$ of the upper transistor, all distributed circuit capacitance appearing at its base, and the capacitance appearing at the

collector of the lower transistor. The value of $C_{b'c}$ increases as the collector junction goes from reverse bias to forward bias.

The value of $C_{b'c}$ was therefore taken as the value at zero bias, which is 7.0 picofarads. Distributed circuit capacitance was estimated from approximate measurements as 4 picofarads and the capacitance at the collector of the lower transistor as 4 picofarads. In retrospect, it appears that the value of $C_{b'c}$ should have been taken at some small value of forward bias or that the distributed capacitance was larger than that obtained by approximate measurement, more probably the latter. In either case, the values of these capacitances are small enough that an error of several picofarads could easily have been made. This error would be sufficient to bring the experimental and calculated rise times into close agreement. More important is the fact that there is good correspondence over two decades of base current and that the error is approximately a constant percentage. This fact substantiates the assumptions made in the derivation of equation (A22).

The power efficiency of these particular inverters should not be expected to be particularly good, since they are capable of driving a far larger direct-current load than is required for a fan-out of 3. Nevertheless, the values observed ranged from 45 to 55 percent with the exception of circuit 10, which was 32 percent. Circuit 6 was checked at an output current load of 410 microamperes, which corresponds to a fan-out of 20. Operation was still satisfactory, and the power efficiency was increased to 81.7 percent, as contrasted to 46 percent at the lower power level. Calculated values of efficiency for the same conditions are 89 percent and 48.4 percent, respectively, as obtained from equation (8). The experimental and calculated values are in excellent agreement when it is considered that the resistors used in constructing the circuit were of 10-percent tolerance.

It was mentioned previously that it has not been possible to obtain a reasonable expression for calculating the fall time of this circuit. A comparison was therefore made experimentally between the fall times with and without the backward diode in the circuit. It was observed that the fall time to 10 percent of the final value with the backward diode was approximately two to three times faster than the fall time without the diode.

Other Similar Transistor Circuits

The similar transistor inverter circuit can be modified to provide a large number of useful logic circuits, principally because of the simple coupling arrangement into a single transistor. Paralleling the lower transistor with a second one provides a two-input NOR circuit, as shown in figure 14. Isolation between the inputs is provided by the

transistors themselves, so that no diodes or other special devices need be used for coupling. The fact that no base-to-ground shunting resistor is required makes possible coupling with a single resistor and speedup capacitor. Full output current is transferred to the transistor input by this arrangement, which makes it more attractive than diode coupled logic for micropower use. Without a diode in the coupling circuit, both the rise and the fall of the preceding stage are coupled directly to the base of the input transistor. The result is that speed is then limited primarily by the transistor and not by the coupling circuit. Figure 14 shows the NOR circuit construction and the resulting waveforms. Operation was much the same as for the basic inverter circuit with the exception of a somewhat longer rise time, which can be directly attributed to the added capacitance of the extra transistor and associated wiring. Since it is a universal logic element, the NOR circuit can be used to implement all logic functions.

A second universal logic element is the NAND, which consists of an AND gate and an inverter. By using two transistors in series as the lower stage of a similar transistor inverter, a two-input NAND is obtained (see fig. 15). In order to maintain the output at ground potential in the off state, compensation must be provided for the additional collector-emitter saturation voltage of the second transistor. Selection of a diode with a lower forward drop for coupling to the upper transistor base easily provides this compensation. Available diodes make a two-input NAND readily possible, but an extension to three inputs would require a careful selection of transistors for low V_{CE} and a very low forward-drop diode. Operation over a wide temperature range would probably be impossible. Note in comparing this circuit to the preceding one that the rise time is not longer than that of the simple inverter.

An alternative configuration for a NOR circuit is the use of a diode OR gate followed by an inverter. This configuration is not so desirable for micropower applications as the aforementioned circuits since it may be necessary to shunt an appreciable portion of the input current to ground through the OR gate resistor. This circuit is shown in figure 16 with its output waveforms. The supply voltages have been increased over the voltages of the previous circuits to allow for the voltage drop in the coupling diodes. The additional resistor to ground necessary in this circuit increases the input current necessary by a factor of two over that required for the same circuit with direct-base input. The additional voltage necessary with diode coupling also increases the power level of the circuit. Operating this circuit at the same base drive as that of figure 14 results in an increase in power of more than four times that of the previous circuit for the same fan-out. Another detrimental effect made worse by diode coupling is evident in the photograph showing the rise time (fig. 16). There is a delay of nearly 1/2 microsecond between the fall of the input and the time that the output starts to rise. This delay is the time required for the transistor input and the diode

capacitances to be discharged to the point that the transistor stops conducting. Decreasing the value of the 100-kilohm shunt resistor will decrease this delay at the expense of drive power. Except for these disadvantages, the performance of this circuit is fully comparable with the others described previously.

Two inverter circuits can be coupled together to form a multivibrator. Coupling similar transistor inverters results in the configuration of figure 17, which is a monostable multivibrator or one-shot. The accompanying waveforms show that the output from both sides is more nearly ideal than that of a conventional circuit. Also, both outputs can be fully loaded with negligible effect on the pulse width. Other characteristics of this circuit were the same as the basic inverter from which it was derived. Bistable and astable multivibrators were also constructed with similar results. Some difficulty was experienced with the astable circuit. It did not start readily, tended to stall, and sometimes failed to restart if overloaded.

COMPLEMENTARY TRANSISTOR LOGIC CIRCUITS

Basic Circuit Description

A second circuit configuration combining the advantages of high efficiency, low output impedance, and fast rise and fall times can be constructed by using a complementary pair of transistors (refs. 8 and 9). A basic inverter circuit using this configuration is shown in figure 18. It can be considered as two common-emitter inverter circuits, each of which acts as the load for the other. An input that is of the proper polarity to turn one transistor on will also turn the other off. For input voltage swings between ground and supply voltage, one transistor will always be saturated and the other cut off. The circuit can drive equally well loads returned either to the ground or to the collector supply voltage.

Direct-Current Analysis

The direct-current performance of this circuit is as good as can be obtained from any relatively simple configuration. With Q_2 on, the output can supply a maximum current of $I_{b,1}H_{fe,2}$ at a voltage level of $V_{CC} - V_{CE}$. With transistor Q_1 conducting, the output can support a load current of $I_{b,2}H_{fe,1}$ from a positive source. If leakage effects can be neglected, the direct-current design merely requires that sufficient base drive be provided under the worst case conditions so that its product with the saturated current gain is equal to the maximum load current. For the case in which leakage must be considered, the required

value of shunt resistance from base to emitter can be calculated from the approximate formula given in reference 19. Rearranged in suitable form this formula is

$$R = \frac{\frac{KT}{q}\frac{(1 - \alpha_N\alpha_I)}{I_{EO}}\left[(1 - \alpha_N\alpha_I)\frac{I_C}{I_{CO}} - 1\right]}{\alpha_N(1 - \alpha_I) - (1 - \alpha_N)\left[(1 - \alpha_N\alpha_I)\frac{I_C}{I_{CO}} - 1\right]} \tag{9}$$

where α_N and α_I are the normal and inverted current gains and I_C is the maximum permissible collector leakage current at maximum temperature. The transistors used in this experimental work have negligible leakage currents and the equation is included herein solely for completeness.

This circuit is also tolerant of leakage currents. If the off transistor is not turned off completely, or some collector leakage current is present, the on transistor has only to conduct that much more current. Until this leakage current becomes comparable in magnitude with the output current, it will have no noticeable effect. Even then the only effect will be an increase in power dissipation and a proportional decrease in output capacitance. It is therefore possible to design circuits of this type that will operate at high temperatures with inexpensive transistors and no reverse bias supply.

Power efficiency of this circuit is good. The only power loss is in the base drive circuit and the collector saturation voltage drop, both of which are small compared with the output capability, where

$$\text{Base circuit loss} = V_{CC}I_b$$

$$\text{Collector saturation loss} = H_{fe}I_bV_{CE}$$

$$\text{Power output} = (V_{CC} - V_{CE})H_{fe}I_b$$

From these terms, the power efficiency is

$$\eta = \frac{(V_{CC} - V_{CE})H_{fe}}{(H_{fe} + 1)V_{CC}} \tag{10}$$

which is somewhat better than the efficiency of the similar transistor inverter given by equation (8).

Transient Response

During the switching interval, complementary transistor circuits behave much the same as similar transistor circuits in that they have both transistors conducting for a very short time. This time, typically about 0.1 microsecond, is so short that the power dissipated is negligible. The effect, however, is to delay the output transition by the storage time of the transistor. For micropower circuits, this small delay is usually negligible since the operating rate is relatively low. The storage time, as well as the rise and fall times, can be calculated by using the standard equations for a common-emitter switching circuit that include the effects of collector capacitance (ref. 20). Their combined effect is typically less than 1 microsecond if the switching speed is not limited by the input-circuit time constant. If the latter is the limiting factor, which is commonly the case in diode-coupled circuits, the switching time can be approximated from the time constant involved; if not, it will probably be short enough that it can be neglected for practical micropower circuits. The transition time may, in fact, be so fast as to cause false triggering because of capacitive feed through.

Complementary Inverter Circuit

Application of the basic complementary inverter circuit is limited. It can, of course, be used as an inverter or logical NOT circuit and also as an amplifier to provide a large power gain. Figure 19 shows a circuit of this type designed to provide an output of 12 microamperes. Design values of H_{fe} used for this circuit were 30 and 60 for the PNP and the NPN transistors, respectively. These values allowed a considerable margin to ensure a low saturation drop in the on state. The actual value of load resistor used was 68 kilohms, which resulted in an output loading of 13.2 microamperes at 0.94 volt. For a 50-percent duty cycle, the no-load current drain was 0.4 microampere and the loaded drain was 6.4 microamperes, which resulted in a measured efficiency of 94 percent compared with 91 percent calculated from equation (10). No-load power consumption was 0.4 microwatt compared with a full-load value of 6.4 microwatts.

The output waveforms included in figure 19 show clearly the very fast transition times attainable. The transition times are not, however, a measure of the maximum repetition rate; this rate is determined by the RC time constant of the coupling circuit. For this case, the time constant of the lower coupling circuit is larger, 100 microseconds. Pulse spacings approaching this value will therefore cause insufficient drive during turn on and will result in longer transition times. This condition is evident in the fall time of the circuit, which is controlled by the lower transistor and which otherwise would have been at least as fast as the rise time. Maximum operating rate for this circuit is therefore approximately 10 kilocycles.

Coupling Circuit Limitations

Complementary transistor circuits have one major disadvantage. The addition of logical coupling between stages results in an increase in the required drive power. In order to turn off the NPN transistor, the input voltage must be no more than about 0.3 volt for silicon transistors. If the input is driven from a similar stage, no problem exists; however, this is impossible if logical gating is to be incorporated in the coupling network, as shown in figure 20. The addition of a diode gate at the input of a stage requires a shunting resistor to return the input to the proper potential when the diodes are all back biased, as discussed previously. This resistor must be smaller for a complementary circuit than for a comparable conventional one because it must discharge the input "capacitance" of the off-going stage and also supply drive current to turn on the other transistors.

An analysis of the power loss in diode coupling circuits is contained in appendix B, which also indicates the type most desirable for low power loss. The diode input NAND circuit of figure 21 is of this type. This particular configuration takes advantage of the fact that a larger base drive must be supplied to the lower gain PNP transistor. The lower values of the coupling resistors for the PNP stage are utilized to provide the fast recovery required when the input signal is removed. In this case, a NAND circuit is more efficient than a NOR circuit.

The circuit was designed to drive and did drive a 36-kilohm load at a 50-percent duty cycle with a total current drain of 27 microamperes compared with a no-load current drain of 4.5 microamperes. The result was an actual efficiency of 80 percent. Increasing the load to 15 kilohms caused a drop in output level of only a few millivolts and increased the efficiency to 89 percent. Drive current at the input was slightly more than 5 microamperes, which produced a base current of 2 microamperes in the upper transistor. Although this circuit does not appear particularly efficient, it is several times better than a comparable circuit with a conventional diode gate followed by a complementary inverter.

Multivibrator Circuits

Several multivibrators were constructed to demonstrate some of the other circuits based on the complementary inverter. The first is shown in figure 22 with its output waveforms. In the quiescent state, the lower-left and upper-right transistors are saturated and provide complementary outputs at points 1 and 2. In this configuration, the two upper transistors form a conventional monostable multivibrator and the lower ones are slaved to them to provide an active load. The no-load current drain for the circuit was 5 microamperes. With operation into a

33-kilohm load at output 2, the input current rose to 30 microamperes, at which condition the accompanying waveform was recorded.

A slightly different configuration of the same basic circuit was constructed to operate on a positive trigger pulse (fig. 23). The accompanying waveforms are similar to those of the preceding circuit, as is the performance. Both circuits triggered reliably on a wide variety of input pulses. Pulse widths from less than 1 microsecond up to square waves were used with approximately the same results. The only effect was a small amount of feed through from the decay of long input pulses, evident as a small pip on the output.

Long delay times are easily obtained with these circuits. It is actually more difficult to design a circuit for very short delays and still keep the power very low. The smallest usable timing capacitor must be large enough to turn off the associated transistor reliably when the circuit is triggered. In order to obtain very short delays, it is then necessary to decrease the value of the resistor that discharges the timing capacitor and sets the quiescent operating condition. Decreasing this value increases the base current and, therefore, power dissipation. One solution to this problem is to reverse the normal operation of the timing circuit so that the timing capacitor is discharged into the transistor base and the quiescent state is determined by a separate network. Pulse width of the resulting circuit will then be dependent on the transistor parameters and could be expected to vary considerably with temperature.

Ease of triggering this type circuit makes it attractive for a bistable multivibrator or flip-flop circuit. A set-reset flip-flop circuit and its output waveforms are shown in figure 24. This particular circuit has been modified to improve the triggering and to decrease the switching time. Addition of a 4.7-kilohm resistor in series with each of the coupling networks decreases the shunting effect of the speedup capacitors on the leading edge of the trigger pulse. The improvement in performance made by this resistor is admittedly small; it is worthwhile, however, for operation at or near the maximum pulse rate.

A second modification, the addition of a 100-picofarad capacitor between the bases of corresponding PNP and NPN transistors, is more effective. The voltage swing at these two bases is in the same direction during the transition interval. Addition of the aforementioned resistors and capacitors therefore couples a larger portion of the trigger pulse to the base of the NPN transistor. The effect is to decrease the transition time and, therefore, the time during which both transistors conduct.

These modifications also improve the resolution time. The maximum repetition rate of this circuit for equally spaced set and reset pulses

is determined by the coupling network time constants. The same limitation does not apply to nonrecurrent set-reset pulse pairs. In this case, the resolution time can be considerably shorter than the minimum spacing for repetitive pulses if sufficient time is allowed between pulse pairs for the speedup capacitors to reach equilibrium. Operation under these conditions is depicted in the lower photograph of figure 24, which shows the output for a pair of set-reset pulses spaced approximately 2 microseconds apart. For applications where resolution time is important but the repetition rate is low, this circuit can be designed to operate at considerably lower power levels than would be necessary otherwise.

Minimum-Power Multivibrator

An attempt was made to determine experimentally the minimum operating power for a circuit of this type by using the S-4528 and S-4529 transistors. In order to eliminate the effects of coupling circuits from the problem, the circuit chosen was an astable multivibrator. Frequency of operation was to be at least 1 kilocycle. The resulting circuit and output waveforms are shown in figure 25.

With no load and a collector supply voltage of 2.0 volts, the total current drain was 0.5 microampere, which resulted in a power dissipation of 1.0 microwatt. As shown in the accompanying photograph, the rise and fall times were equal and fast and produced a very clean output. Each side was then loaded with 2 megohms to ground not including the 10-megohm and 10-picofarad loading of the scope probe. This loading increased the current drawn to 1.7 microamperes and the dissipation to 3.4 microwatts and produced a power transfer efficiency of 70 percent. No appreciable degradation in waveform was observed. Operating frequency was 2 kilocycles.

At an operating voltage of 2 volts, the charge carried by the timing capacitors was only slightly larger than necessary for good switching of the transistors. Nevertheless, the supply voltage was decreased to determine just how low a voltage the circuit would operate. Operation ceased slightly below 1 volt. At 1 volt, the waveform was considerably degraded, but the circuit still operated reliably at a total no-load dissipation of 0.27 microwatt. Loading each side with a 5-megohm resistor caused a small shift in frequency and an increase in total power to 0.57 microwatt. Even at this extremely low current the power efficiency was 53 percent. Increasing the size of the timing capacitors would have undoubtedly improved the waveshape but with a decrease in frequency.

Because of the symmetry of this circuit, it produces two complementary outputs that can be used to provide a two-phase clock for timing logic circuits. In addition, the low output impedance and high power

efficiency make it ideal for this application. Another advantage is that the circuit is inherently self-starting.

CONCLUDING REMARKS

A number of logic circuits derived from the basic similar and complementary transistor circuits were constructed and their performance was demonstrated over a variety of operating conditions. When operated at micropower levels, all these circuits were limited in operating rate by the RC (resistance-capacitance) time constants of the circuit in conjunction with the input and the output capacitances of the transistor. Decreasing the power level for a given logic circuit resulted in a nearly proportional decrease in the maximum operating rate. These limitations are much the same as those for most conventional circuits when they are operated at low power levels.

Each of the two basic circuit types discussed in detail had a number of advantages over conventional logic circuits. These advantages included low output impedance in both the on and the off states, high power efficiency, fast transition times, and extremely good fan-out capability.

They operated efficiently at microwatt power levels with pulse rates as high as several hundred kilocycles. Compared with commercially available logic modules and other low-power logic forms discussed, these circuits showed a considerable improvement. Approximate operating capabilities of a number of circuits are compared in the following table, where values given are approximate in that operating rate was estimated from transition-time data in the cases in which it was not specified.

Circuit	Commercial germanium logic elements		Commercial silicon low-power digital modules		Complementary transistor logic circuits		Similar transistor logic circuits	
	Power consumption, mw	Pulse rate, kc	Power consumption, mw	Pulse rate, kc	Power consumption, μw	Pulse rate, kc	Power consumption, μw	Pulse rate, kc
Monostable multivibrator	60	250	10	25	30	22	90	200
Flip-flop	48	300	<10	100	7	30	--	---
Inverter	--	---	<10	1000	6	10	20	50
Astable multivibrator	66	380	8	125	3.5	2	--	---
NOR or NAND	--	---	---	---	8.5	70	45	200

Both the similar and the complementary transistor circuits showed definite promise for space-oriented applications. The similar circuit was more efficient in logical gating applications, where, through the use of multiple transistor inputs, coupling diodes could be eliminated for good performance at low supply voltages. Circuits such as multivibrators, which are not limited in performance by the necessity for a number of logical inputs, appeared to be ideally implemented with complementary transistor circuits. The ease of triggering these circuits was a secondary reason for their choice.

Operating levels and output characteristics of these two circuits were sufficiently similar that compatible operation from the same collector supply was possible. The best features of each circuit could therefore be utilized in the design of a complete logic system.

Circuit design can be accomplished by use of the procedures and equations presented herein. Thus, it is possible to predict the circuit transition times, required power level for a given operating rate, minimum supply voltage, and direct-current performance, including fan-out and efficiency. With these techniques, it should be possible to design a complete logic system for operation at a pulse rate of 10 kilocycles and with a power consumption of 10 microwatts or less per stage. Such a system would be of definite value for space-vehicle applications.

Lewis Research Center
National Aeronautics and Space Administration
Cleveland, Ohio, August 21, 1962

APPENDIX A

DERIVATION OF EQUATIONS FOR SIMILAR TRANSISTOR INVERTER

Optimum Base-Supply Voltage

In the on state of the similar transistor inverter (fig. 26), the power drawn from the base supply V_{BB} that is not delivered to the load is given by the product of base current times the voltage drop from V_{BB} to V_L:

$$P_{ON} = I_{b,2}(V_{BB} - V_L) \tag{A1}$$

Similarly, for the off state, where I_B is the total current drawn from V_{BB} with the lower transistor saturated,

$$P_{OFF} = V_{BB}I_B \tag{A2}$$

$$I_B = \frac{V_{BB} - V_D - V_{CE}}{R_1} \tag{A3}$$

From the required base drive in the on state,

$$R_1 = \frac{V_{BB} - V_L - V_{BE}}{I_{b,2}} \tag{A4}$$

Therefore,

$$P_{OFF} = \frac{I_{b,2}V_{BB}(V_{BB} - V_D - V_{CE})}{V_{BB} - V_L - V_{BE}} \tag{A5}$$

It is reasonable to assume that the stage will be on half of the time. Total power for a 50-percent duty cycle is then

$$(P_T)_{50\%} = \frac{I_{b,2}}{2}\left[V_{BB}\left(\frac{V_{BB} - V_D - V_{CE}}{V_{BB} - V_L - V_{BE}}\right) + V_{BB} - V_L\right] \tag{A6}$$

The value of V_{BB} that results in the minimum power dissipation is now obtained by finding the derivative of power with respect to V_{BB} and

setting it equal to zero. For simplifying the manipulation, let $A = V_L + V_{BE}$ and $B = V_D + V_{CE}$:

$$\frac{\partial P_T}{\partial V_{BB}} = \frac{I_{b,2}}{2}\left[\frac{V_{BB} - B}{V_{BB} - A} + \frac{V_{BB}}{V_{BB} - A} - \frac{V_{BB}(V_{BB} - B)}{(V_{BB} - A)^2} + 1\right] \tag{A7}$$

$$0 = \frac{I_{b,2}}{2}\left[\frac{(V_{BB} - B)(-A) + V_{BB}(V_{BB} - A) + (V_{BB} - A)^2}{(V_{BB} - A)^2}\right] \tag{A8}$$

$$0 = 2V_{BB}^2 - 4AV_{BB} + A^2 + AB \tag{A9}$$

Therefore,

$$V_{BB} = A \pm \sqrt{\tfrac{1}{2}A^2 - \tfrac{1}{2}AB}$$

$$= V_L + V_{BE} \pm \sqrt{\tfrac{1}{2}\left(V_L^2 + 2V_LV_{BE} + V_{BE}^2\right) - \tfrac{1}{2}(V_L + V_{BE})(V_D + V_{CE})} \tag{A10}$$

If the output of the circuit is to be at ground potential in the off state, it is necessary that the sum of V_{CE} and V_D be equal to V_{BE}. Application to equation (A10) simplifies it to

$$\left(V_{BB}\right)_{opt} = V_{BE} + V_L + \sqrt{\tfrac{1}{2}V_L(V_L + V_{BE})} \tag{A11}$$

where the positive square root has been selected as the one that gives a physically valid result.

Rise-Time Calculation

Calculation of the rise time for this circuit assumes that transistor Q_1 is quickly turned off, and that transistor Q_2 is being turned on. Transistor Q_1 can be characterized as a capacitance seen through D_2 and its effect included in C_3. Diodes D_1 and D_2 represent a high impedance in this state and are characterized by a small capacitance, which can be added to the transistor base-emitter capacitance.

The hybrid Π equivalent circuit is used to represent the transistor since it includes the effects of the various capacitances that are important in micropower operation. The complete equivalent circuit and its parameters and a simplified form suitable for this analysis are shown in figure 27. Transforming to a voltage source equivalent circuit, adding the external circuit, and simplifying leads to the model of figure 28, which will be used for calculating the rise time. The equations for this circuit are, in transformed matrix form,

$$\begin{bmatrix} \frac{e_1}{S} \\ -g_m v_{b'e} R_3 \\ 0 \\ g_m v_{b'e} R_3 \end{bmatrix} =$$

$$\begin{bmatrix} R_1 + \frac{1}{C_1 S} & -\frac{1}{C_1 S} & 0 & 0 \\ -\frac{1}{C_1 S} & \frac{1}{C_1 S} + r_{b'e} + R_3 & -r_{b'e} & -R_3 \\ 0 & -r_{b'e} & r_{b'e} + \frac{1}{C_2 S} & 0 \\ 0 & -R_3 & 0 & R_3 + \frac{1}{C_3 S} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \qquad \text{(A12)}$$

Transferring the controlled source into the coefficient matrix yields

$$\begin{bmatrix} \frac{e_1}{S} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_1 + \frac{1}{C_1 S} & -\frac{1}{C_1 S} & 0 & 0 \\ -\frac{1}{C_1 S} & \frac{1}{C_1 S} + r_{b'e} + R_3 & \frac{g_m R_3}{C_2 S} - r_{b'e} & -R_3 \\ 0 & -r_{b'e} & r_{b'e} + \frac{1}{C_2 S} & 0 \\ 0 & -R_3 & -\frac{g_m R_3}{C_2 S} & R_3 + \frac{1}{C_3 S} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix}$$

(A13)

The output voltage e_{out} is equal to i_4/C_3S. Solving for i_4 gives

$$i_4 = \frac{\begin{vmatrix} R_1 + \frac{1}{C_1S} & -\frac{1}{C_1S} & 0 & \frac{e_1}{S} \\ -\frac{1}{C_1S} & \frac{1}{C_1S} + r_{b'e} + R_3 & \frac{g_mR_3}{C_2S} - r_{b'e} & 0 \\ 0 & -r_{b'e} & r_{b'e} + \frac{1}{C_2S} & 0 \\ 0 & -R_3 & -\frac{g_mR_3}{C_2S} & 0 \end{vmatrix}}{\Delta} \qquad \text{(A14)}$$

Add row 4 to row 1 and expand in minors of the first column (note that the first one will be zero):

$$e_{out}(S) = \frac{i_4}{C_3S} = \frac{\frac{1}{C_3SC_1S}\begin{vmatrix} -\frac{1}{C_1S} & 0 & \frac{e_1}{S} \\ -r_{b'e} & r_{b'e} + \frac{1}{C_2S} & 0 \\ -R_3 & \frac{-g_mr_3}{C_2S} & 0 \end{vmatrix}}{\Delta} \qquad \text{(A15)}$$

$$e_{out}(S) = \frac{\frac{e_1R_3}{S}\left(r_{b'e} + \frac{1}{C_2S} + \frac{g_mr_{b'e}}{C_2S}\right)}{(R_1C_1S + 1)\left[R_3\left(r_{b'e} + \frac{1}{C_2S}\right) + \frac{r_{b'e}}{C_2S}(R_3C_3S + 1) + \frac{g_mr_{b'e}R_3}{C_2S}\right] + R_1\left[\left(r_{b'e} + \frac{1}{C_2S}\right)(R_3C_3S + 1)\right]} \qquad \text{(A16)}$$

Substituting $\beta = g_mr_{b'e}$ into equation (A16) and simplifying yield

$$e_{out}(S) = \frac{e_1R_3(r_{b'e}C_2S + 1 + \beta)}{S\left\{(R_1C_1S + 1)[r_{b'e}(R_3C_3S + 1) + R_3(\beta + 1 + r_{b'e}C_2S)] + R_1(r_{b'e}C_2S + 1)(R_3C_3S + 1)\right\}} \qquad \text{(A17)}$$

If the time domain solution of this equation were found, it would contain the sum of two different exponentials, which would make it impossible to solve explicitly for the rise time. It is therefore evaluated with the effects of each capacitor considered separately. Setting C_2 and C_3 equal to 0 in equation (A17) reduces it to

$$e_{out}(S) = \frac{e_1 R_3(\beta + 1)}{S\left\{(R_1 C_1 S + 1)\left[r_{b'e} + R_3(\beta + 1)\right] + R_1\right\}}$$

$$= \frac{e_1 R_3(\beta + 1)}{S\left\{S\left[R_1 C_1 r_{b'e} + (\beta + 1)R_3 R_1 C_1\right] + r_{b'e} + R_3(\beta + 1) + R_1\right\}}$$

$$= \frac{e_1 R_3(\beta + 1)}{r_{b'e} + R_1 + R_3(\beta + 1)}\left(\frac{1}{S}\left\{\frac{1}{\frac{S\left[R_1 C_1 r_{b'e} + R_3(\beta + 1)\right]}{r_{b'e} + R_3(\beta + 1) + R_1} + 1}\right\}\right) \tag{A18}$$

$$e_{out}(t) = \frac{e_1 R_3(\beta + 1)}{r_{b'e} + R_1 + R_3(\beta + 1)}\left\{1 - \exp\left[-\frac{t}{\frac{R_1 C_1(r_{b'e} + \beta R_3 + R_3)}{r_{b'e} + R_1 + \beta R_3 + R_3}}\right]\right\} \tag{A19}$$

This solution is based on the use of small signal parameters to characterize the transistor within the active region. It should give a good indication of the transient response, but it can not be used to obtain steady-state values. The first portion of the right side of equation (A19) must therefore be deleted, and the proper steady-state limits imposed. The time-constant portion of the exponent can be simplified in the case of a particular circuit. The relations between variables from the circuits investigated experimentally are

$$R_L = R_3$$

$$r_{b'e} = \frac{0.03}{I_b}$$

$$R_3 = 0.32\ R_1$$

$$r_{b'e} = 0.066\ R_1$$

(The value of $r_{b'e}$ was obtained from fig. 29.) Substituting these relations into the time-constant portion of the exponential in equation (A19) yields

$$\frac{R_1C_1(r_{b'e} + \beta R_3 + R_3)}{r_{b'e} + R_1 + \beta R_3 + R_3} = \frac{R_1C_1(0.066\ R_1 + 0.32\ R_1\beta + 0.32\ R_1)}{0.066\ R_1 + R_1 + 0.32\ R_1\beta + 0.32\ R_1}$$

$$= \frac{R_1C_1(0.386 + 0.32\ \beta)}{1.386 + 0.32\ \beta}$$

$$= R_1C_1\left(\frac{1.2 + \beta}{4.33 + \beta}\right) \tag{A20}$$

When the circuit turns on, the output rises toward a final value of $V_{BB} - V_{BE}$, although it never gets there. It can rise only as far as V_L, at which point the output is clamped to the collector supply voltage. Finding the rise time to the 90-percent point necessitates equating the voltage at this point divided by the driving voltage to the portion of equation (A19), which gives the transient solution:

$$\frac{0.9\ V_L}{V_{BB} - V_{BE}} = 1 - \exp\left[-\frac{t}{R_1C_1\left(\frac{1.2 + \beta}{4.33 + \beta}\right)}\right] \tag{A21}$$

Solving this expression for t yields an expression for the rise time:

$$t_r = -R_1C_1\left(\frac{1.2 + \beta}{4.33 + \beta}\right) \ln\left(\frac{V_{BB} - 0.9\ V_L - V_{BE}}{V_{BB} - V_{BE}}\right) \tag{A22}$$

This result has been obtained by neglecting the contribution of C_2 and C_3. Either it must be shown that they are indeed negligible, or the preceding result must be modified. Equation (A18) is therefore evaluated as was done previously for the case $C_1 = C_3 = 0$. The resulting time-constant term is

$$r_{b'e}C_2\left(\frac{19.95}{20.95 + 4.85\ \beta}\right) \tag{A23}$$

If in this case β is at least 40, the time constant of the circuit will be an order of magnitude below $r_{b'e}C_2$. A similar process for the case $C_1 = C_2 = 0$ yields the time-constant term:

$$R_3C_3\left(\frac{3.33}{\beta + 4.33}\right) \tag{A24}$$

The effect of the R_3C_3 time constant is therefore similarly reduced by at least an order of magnitude for a β of at least 30.

Values of these time constants for the circuits investigated experimentally had the following approximate maximum values corresponding to the lowest operating current:

$$R_1C_1 = 2.8\times10^{-5}$$

$$R_2C_2 = 10^{-6}$$

$$R_3C_3 = 2.5\times10^{-6}$$

Since the effects of the R_2C_2 and R_3C_3 time constants are both decreased, as shown previously, it is valid to neglect C_2 and C_3 in the rise-time calculation over the whole range of currents investigated.

APPENDIX B

COMPLEMENTARY LOGIC COUPLING NETWORK ANALYSIS

In order to take full advantage of complementary transistor logic, it is necessary to optimize the coupling circuit for minimum loss. It is assumed that some form of diode logic will be used so that the coupling circuit must determine the output state in the absence of an input.

The generalized circuit is shown in figure 30. Drive voltage into the diodes is assumed to be from a similar stage so that it will swing from a low of V_{CE} to a high of $V_{CC} - V_{CE}$. With an input present at any one of the diodes, the junction of R_1 and R_2 will be raised to $V_{CC} - V_{CE} - V_D$, which is nearly equal to $V_{CC} - V_{BE}$. To ensure that the upper transistor is cut off under this condition, its base is driven by way of R_1 and R_4, which form a voltage divider. Only a small voltage drop is necessary in R_1, mainly as a safety factor to ensure that transistor Q_2 is held off. Therefore, let $R_4 = 2R_1$. An equation relating the circuit constants and drive current with an input present can then be written for the lower transistor:

$$I_{b,1} + \frac{V_{BE,1}}{R_5} = \frac{V_{CC} - V_{CE} - V_D - V_{BE,1}}{R_2} \tag{B1}$$

With all inputs removed, sufficient base current must be provided through R_1, R_3, R_2, and R_5 to saturate Q_2. At the same time, the voltage at the base of Q_1 must be below V_{BE} to ensure that it is cut off. Under these conditions, no current can flow in the base of Q_1. These requirements lead to a second equation:

$$I_{b,2} + \frac{V_{BE,2}}{2R_1} = \frac{V_{CC} - V_{BE,2}}{\frac{R_3(R_2 + R_5)}{R_3 + R_2 + R_5} + R_1} \tag{B2}$$

Choosing the off voltage at the base of Q_1 equal to $V_{BE}/2$ leads to

$$\frac{V_{BE}}{2} = \frac{R_3R_5(V_{CC} - V_{BE,2})}{R_3(R_2 + R_5) + R_1(R_3 + R_2 + R_5)} \tag{B3}$$

The input current required is given by

$$I_{IN} = \frac{V_{CC} - V_{CE} - V_D - V_{BE}}{R_2} + \frac{V_{CC} - V_D - V_{CE}}{R_3} \tag{B4}$$

It is now theoretically possible to eliminate three of the four unknown resistances among the first three equations, and then to find the optimum values for the fourth that minimizes equation (B4). This is not a practical method of obtaining an analytical solution, as the determination of the optimum resistor values requires the solution of a cubic equation involving large and complicated algebraic expressions. It might be assumed that the minimum drive current requirement might correspond to the case with either R_3 or R_5 removed completely. With R_3 removed, three circuit equations are sufficient to fully determine all remaining resistors. Equations (B1) and (B4) are unchanged, and the two other equations can be written by inspection as

$$I_{b,2} + \frac{V_{BE,2}}{2R_1} = \frac{V_{CC} - V_{BE,2} - \frac{1}{2} V_{BE,1}}{R_1 + R_2} \tag{B5}$$

$$I_{b,2} + \frac{V_{BE,2}}{2R_1} = \frac{\frac{1}{2} V_{BE,1}}{R_5} \tag{B6}$$

If, instead of R_3, R_5 is removed, the circuit is defined by

$$I_{b,1} = \frac{V_{CC} - V_{CE} - V_D - V_{BE}}{R_2} \tag{B7}$$

$$I_{b,2} + \frac{V_{BE,2}}{2R_1} = \frac{V_{CC} - V_{BE,1}}{R_1 + R_3} \tag{B8}$$

$$I_{b,2} + \frac{V_{BE,2}}{2R_1} = \frac{\frac{1}{2} V_{BE,1}}{R_3} \tag{B9}$$

$$I_{IN} = \frac{V_{CC} - V_{BE,2}}{R_3} + I_{b,1} \tag{B10}$$

These equations can be solved for specific circuit values with a nominal amount of difficulty. This was the approach taken for two cases with $I_{b,1} = 2I_{b,2}$ and $I_{b,1} = \frac{1}{2} I_{b,2}$, which reflect the fact that the NPN transistor used had approximately twice the gain of the PNP and required only half as much drive current for the same output. In each case, the minimum value of I_{IN} occurred with R_3 removed.

The condition of $I_{b,2} = 2I_{b,1}$ corresponds to the case of the NOR circuit shown in figure 30. For values of $V_{CC} = 1.9$ volts, $V_D = 0.4$ volt, $V_{BE} = 0.6$ volt, $V_{CE} = 0.1$ volt, $I_{b,1} = 1$ microampere, and

$I_{b,2}$ = 2 microamperes, the resulting drive current I_{IN} was approximately 7.6 microamperes with R_3 removed. Increasing R_5 somewhat from the previously determined value and adding the necessary R_3 to satisfy the circuit equations resulted in a very small increase in I_{IN}, which indicates that it may be possible to decrease the transistion time by proper choice of R_3 and R_5.

Following through the same analysis for $I_{b,2}$ = 1 microampere and $I_{b,1}$ = 2 microamperes with all the other values unchanged results in a value for I_{IN} of 5.1 microamperes with R_3 removed. This condition represents a definite minimum as I_{IN} increases monotonically to 14.5 microamperes for $R_5 = \infty$. This second case corresponds to a NAND circuit obtained by interchanging the PNP and the NPN transistors. The circuit corresponding to these values has been presented in figure 21. No further work was done to optimize the NOR circuit since the NAND is clearly superior on the basis of input current requirements.

Generalizing the preceding results indicates that the transistor with the higher gain should be turned on by the coupling network in the absence of an input. In this way, the smaller resistors in the network will determine the time constant that limits the transition time when all inputs are removed. This provides the fastest switching for a minimum input power.

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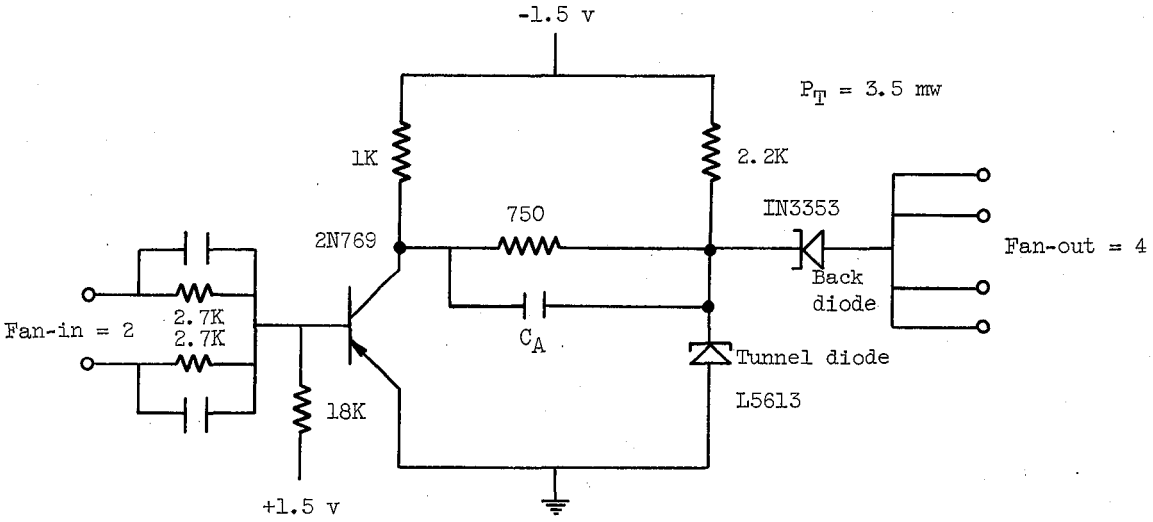


Figure 1. - Tunnel diode coupled NOR.

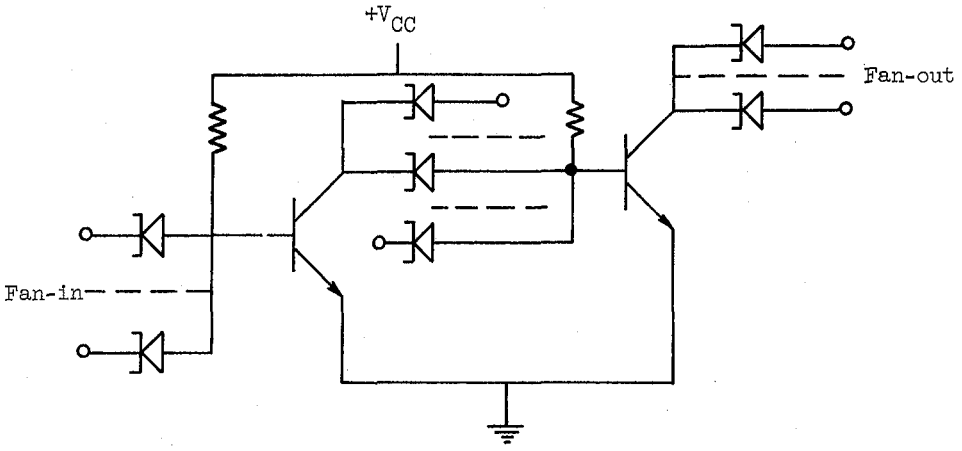


Figure 2. - Backward diode-transistor NAND logic circuit.

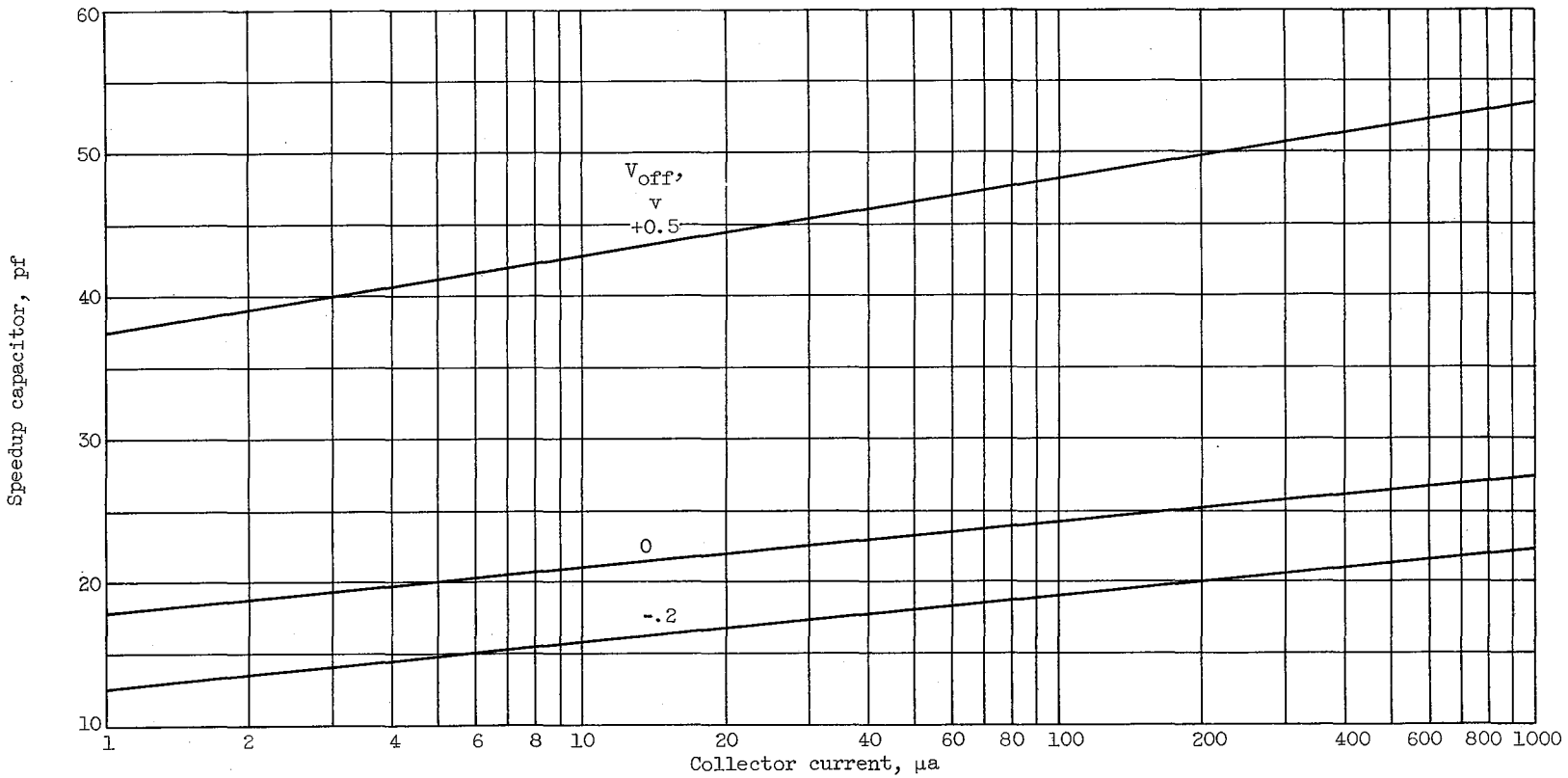


Figure 3. - Variation of required speedup capacitor with collector current. Type S-4528 (PNP) transistor; saturated operation, I_c/I_b, 25; input pulse, 2.0 volts; collector voltage, 1.0 volt.

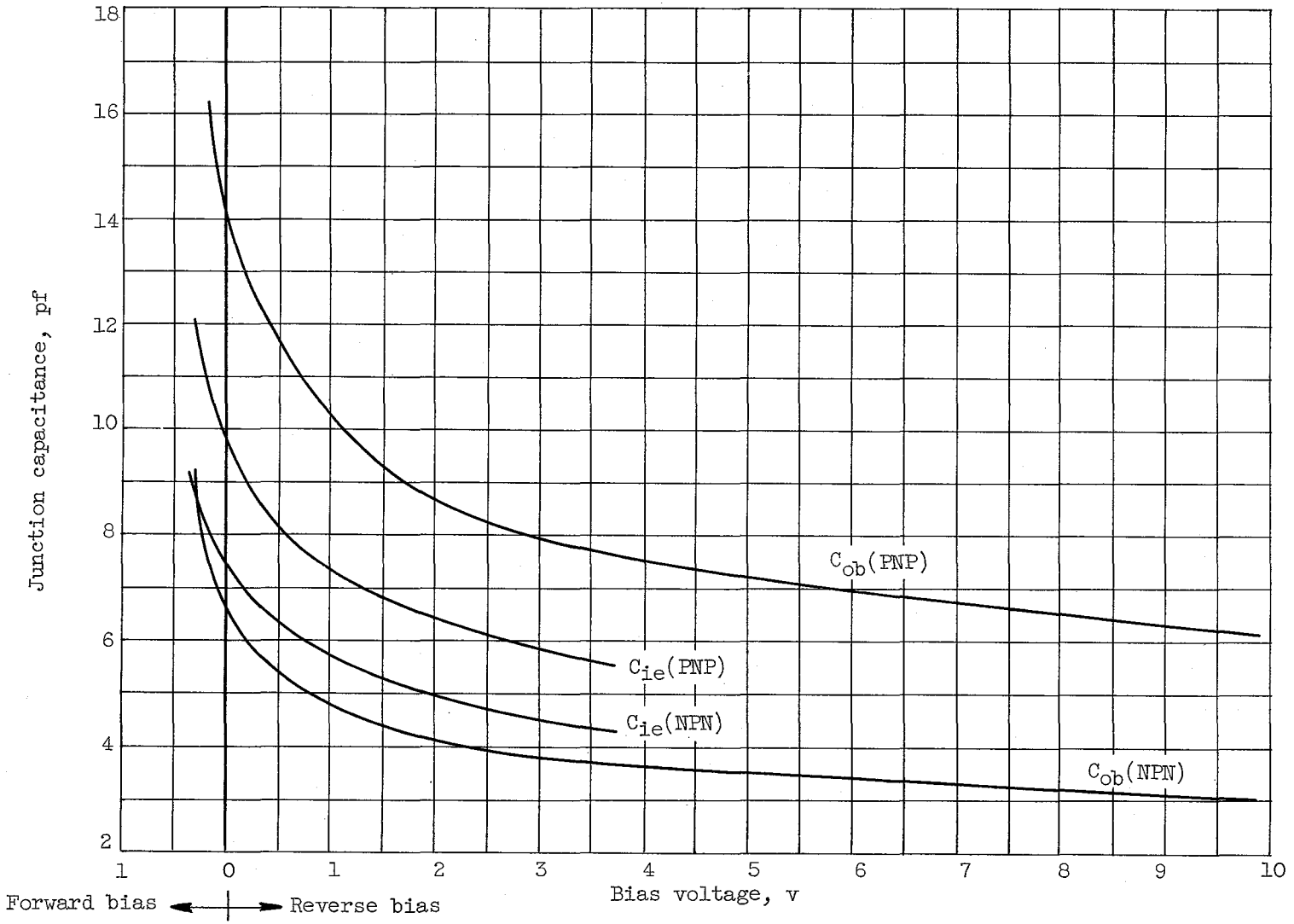


Figure 4. - Variation of junction capacitance with bias voltage. Type S-4528 (PNP) and S-4529 (NPN) transistors.

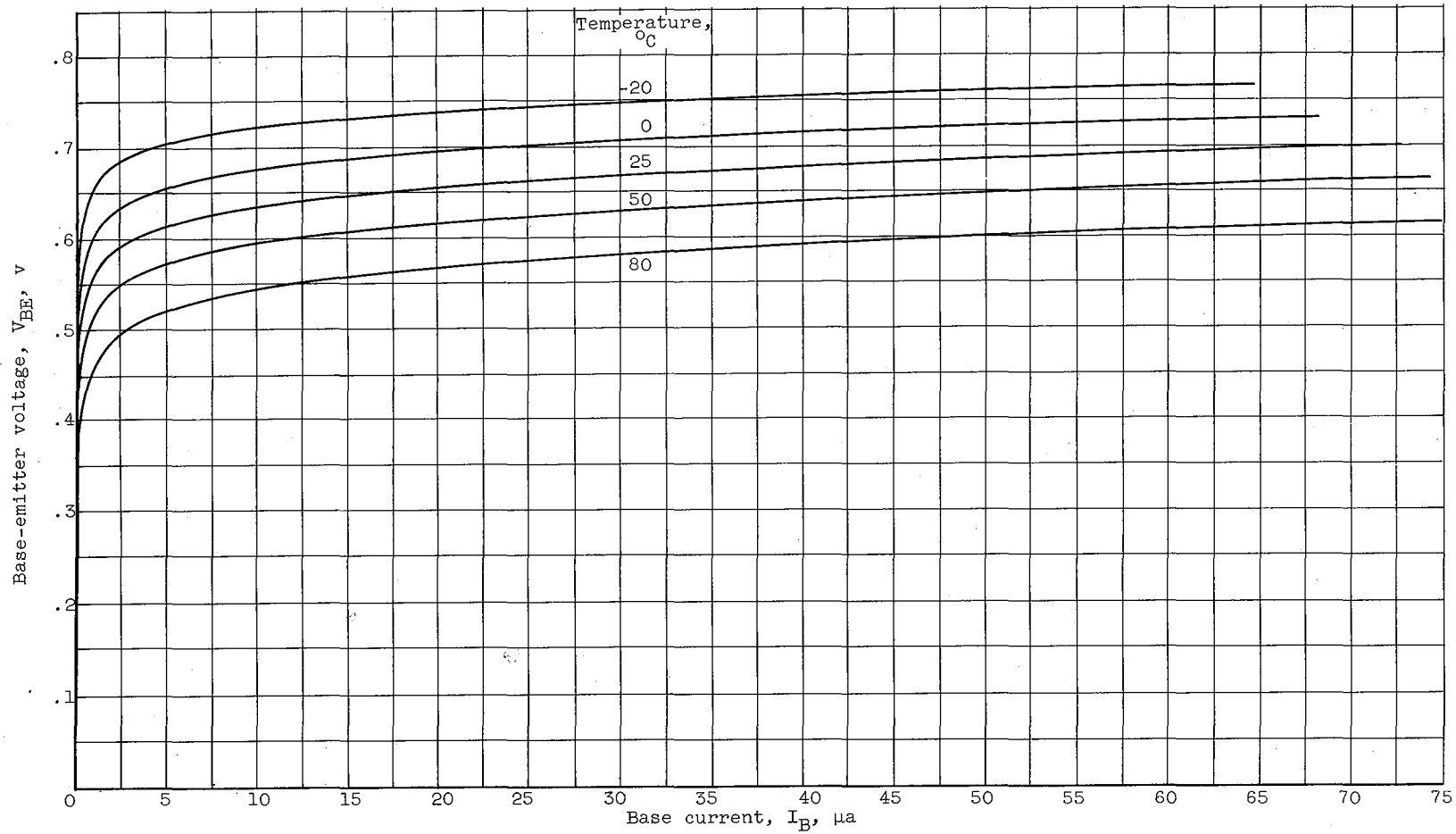


Figure 5. - Temperature dependence of V_{BE}. Type S-4529 transistor (NPN).

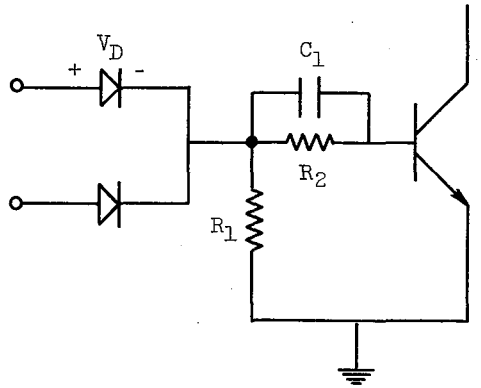


Figure 6. - Diode OR coupling network.

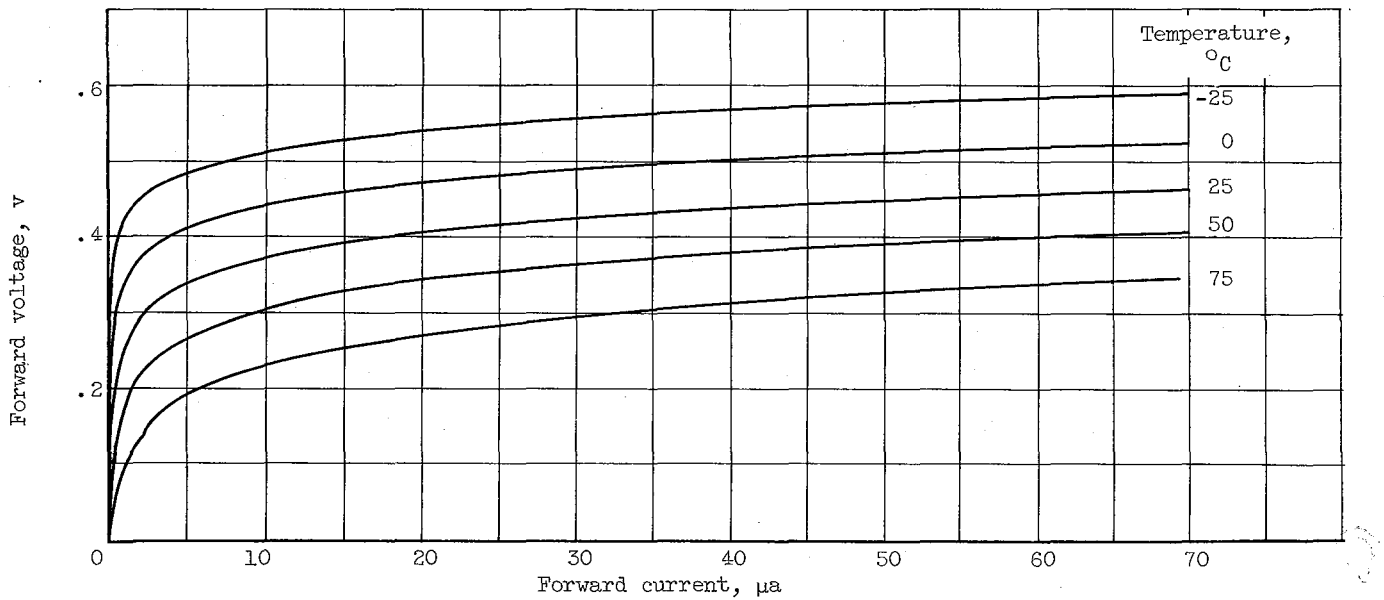


Figure 7. - Forward characteristic of silicon diode type FD-600.

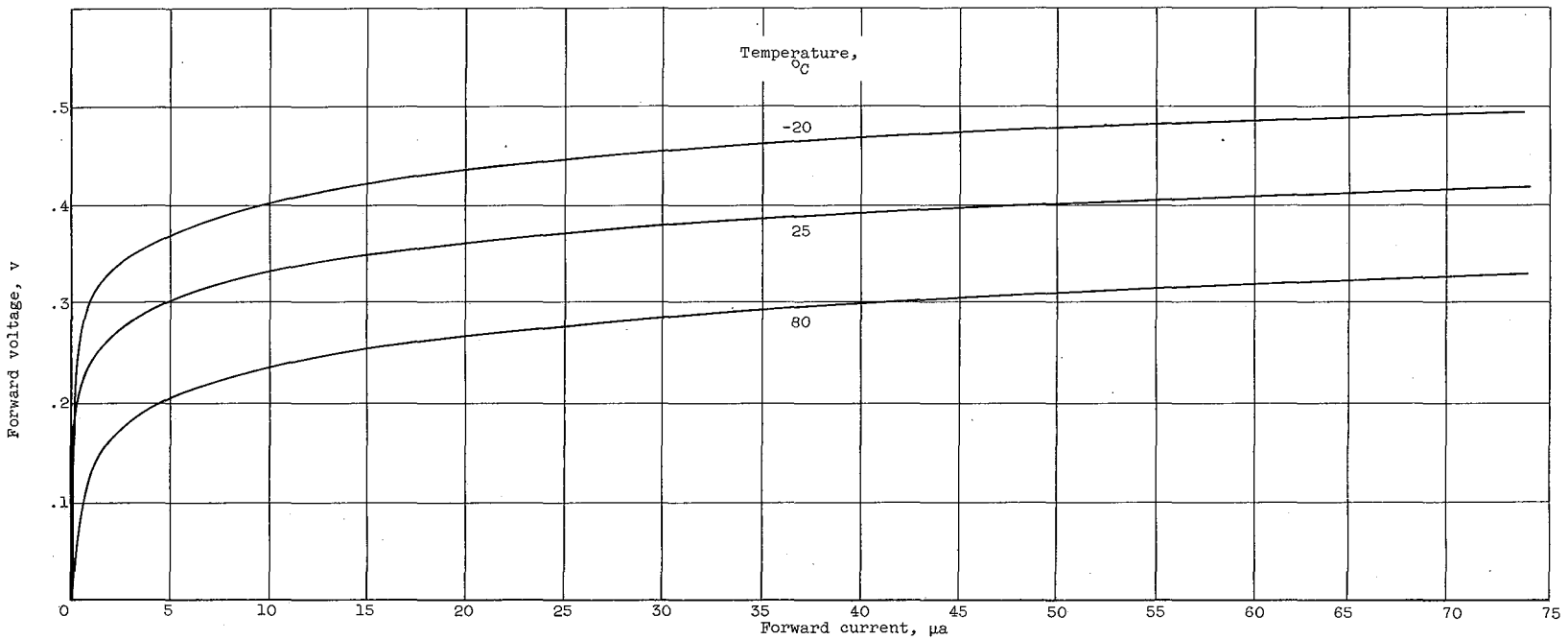


Figure 8. - Forward characteristics of gallium arsenide diode DGS-54.

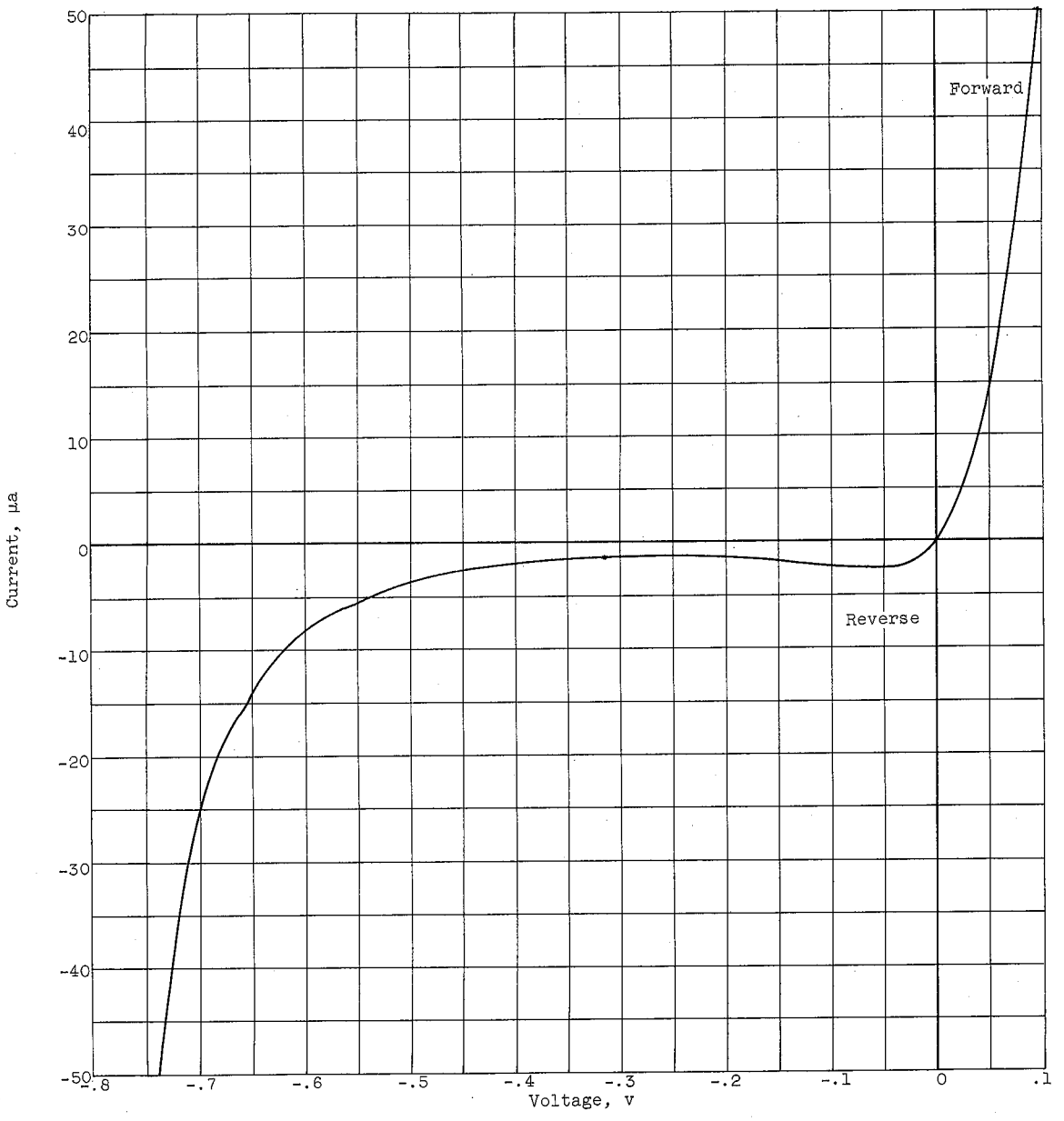


Figure 9. - Characteristics of type HU-5 silicon backward diode.

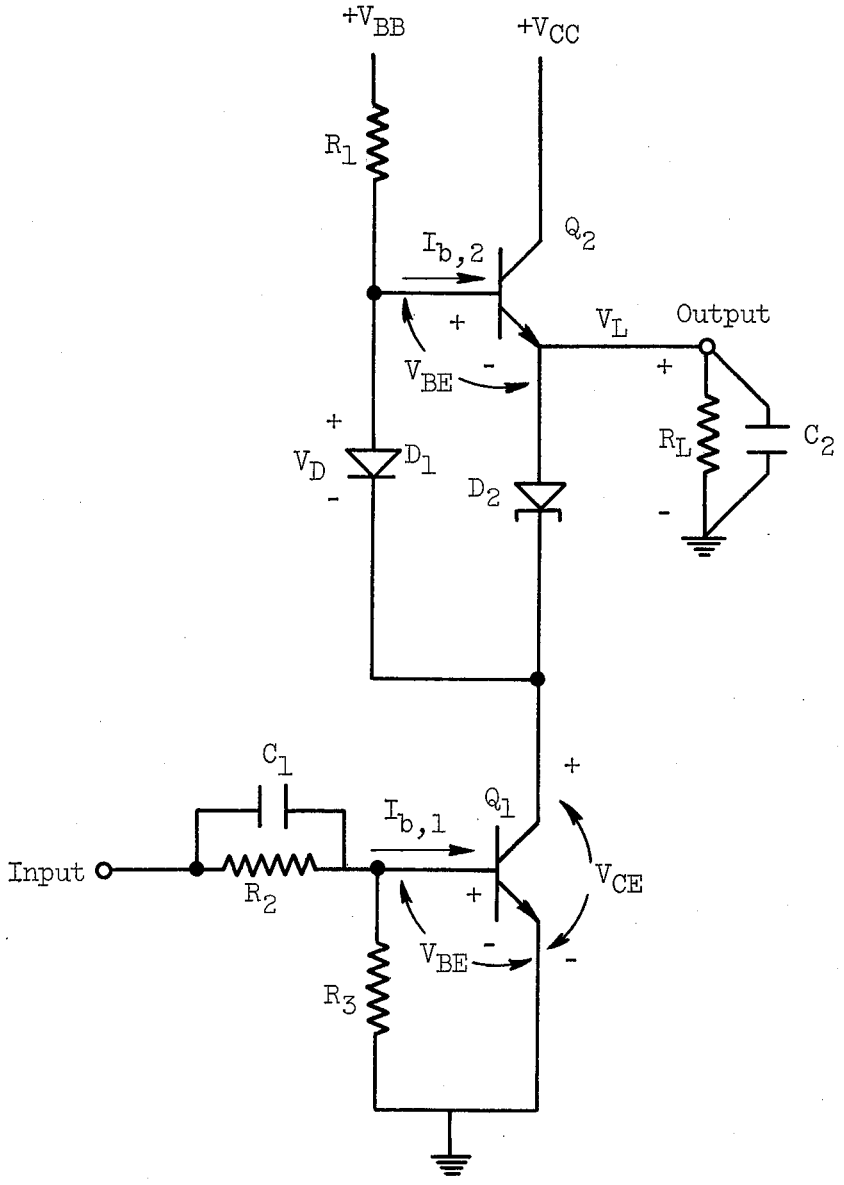


Figure 10. - Similar transistor inverter.

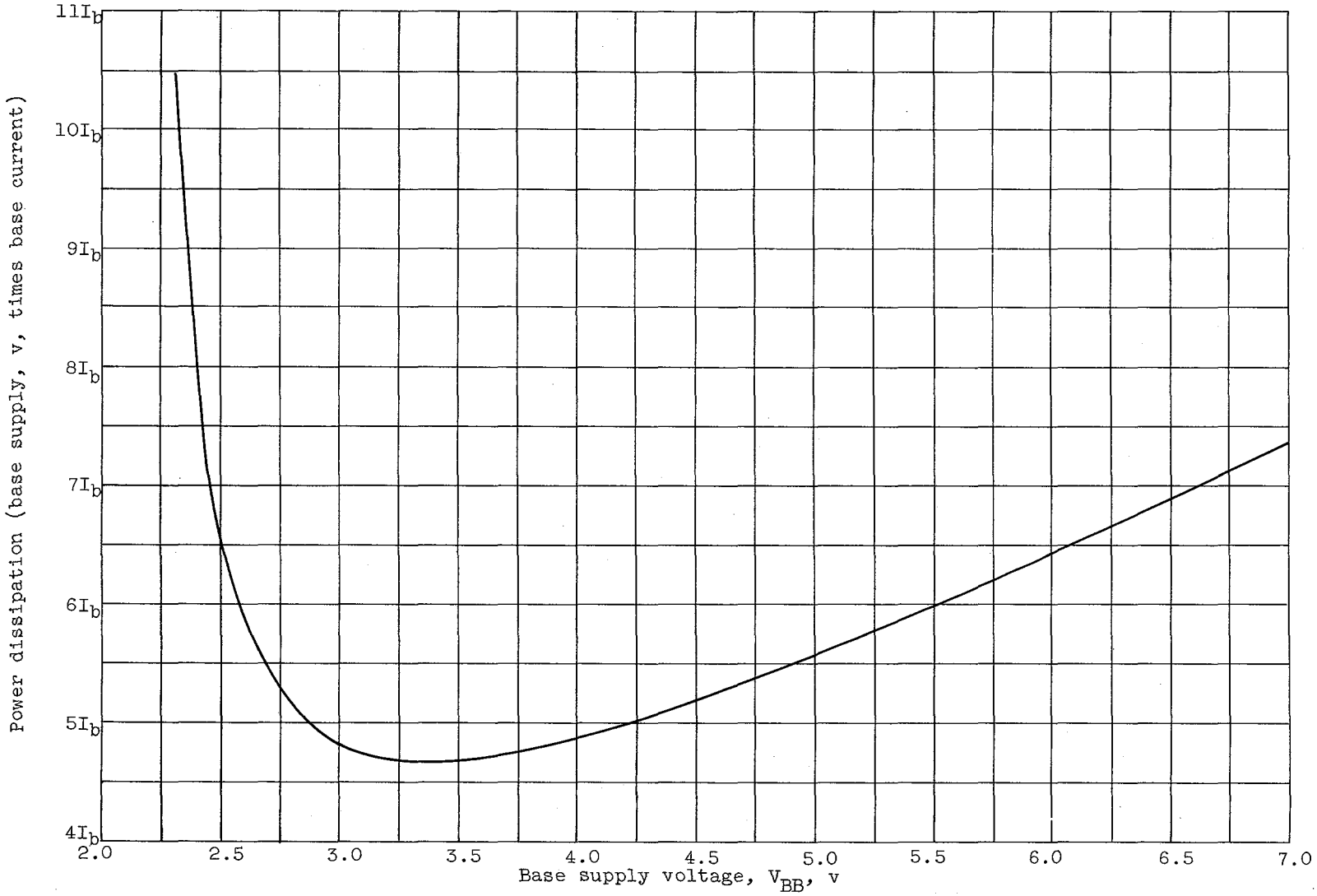


Figure 11. - Base circuit power dissipation. Similar transistor inverter circuit; V_{BE}, 0.60; V_{CE}, 0.15; V_D, 0.40; V_L, 1.50.

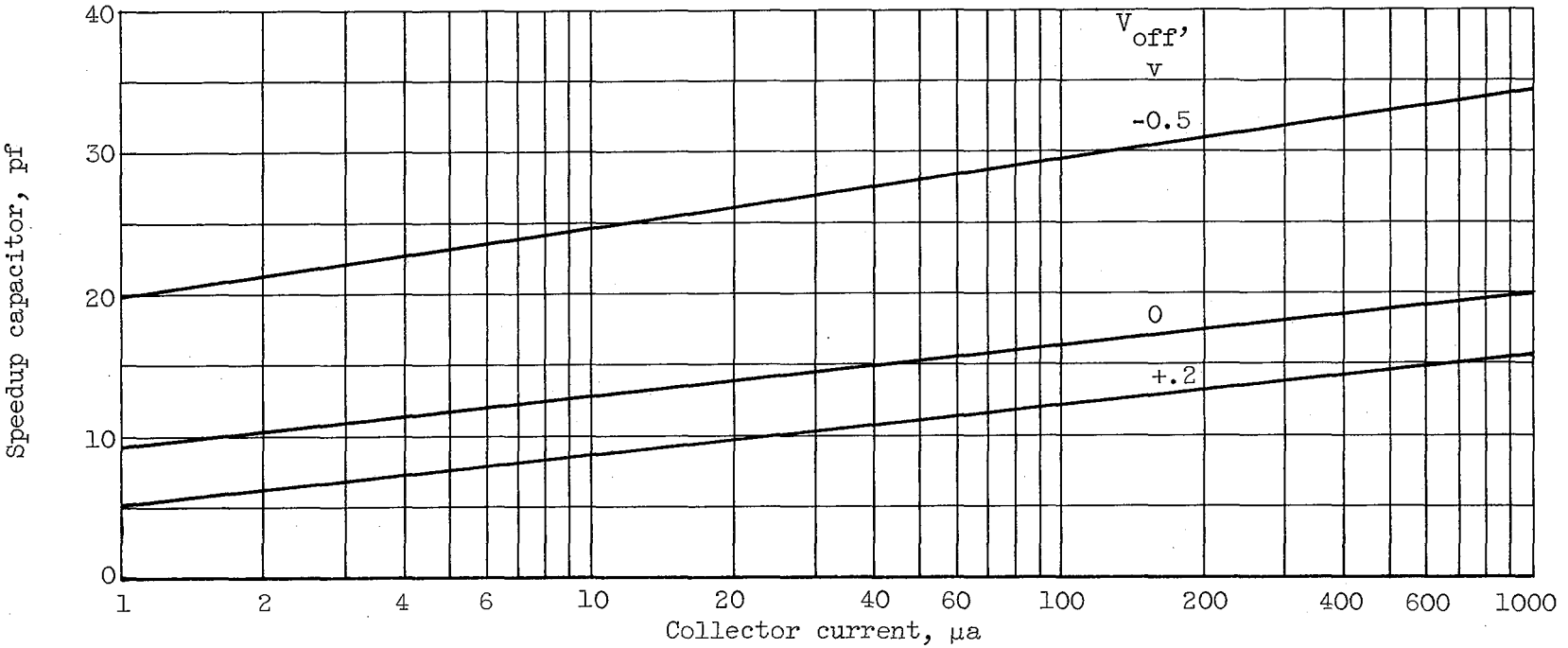


Figure 12. - Variation of required speedup capacitor with collector current. Type S-4529 (NPN); saturated operation; I_c/I_b, 50; input pulse, 2.0 volts; collector voltage, 1.0 volt.

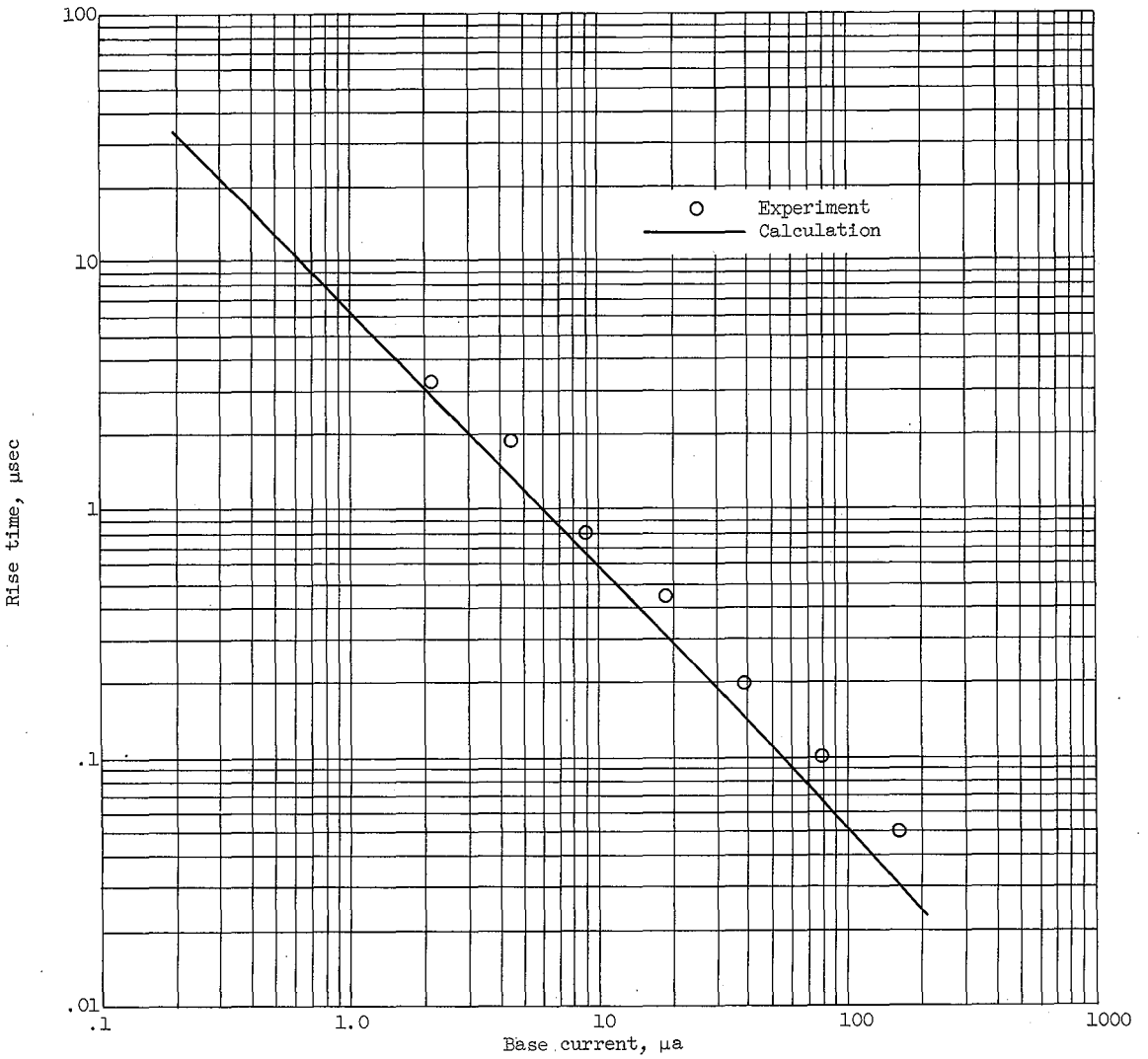
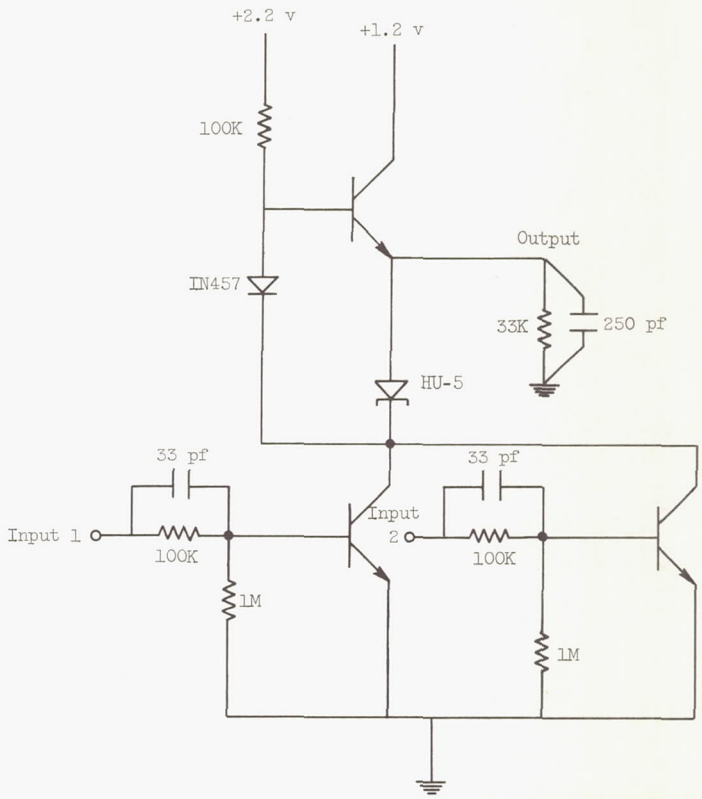
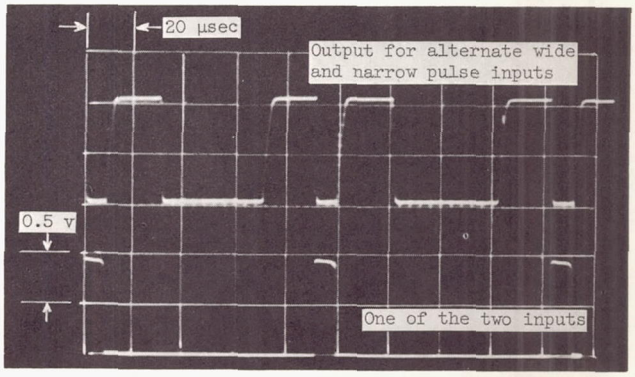


Figure 13. - Rise time for similar transistor inverter.





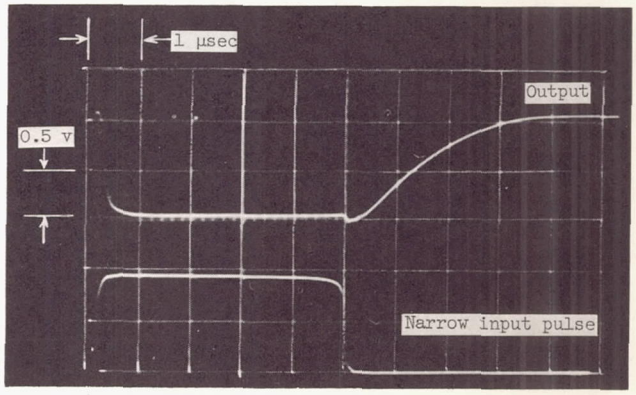


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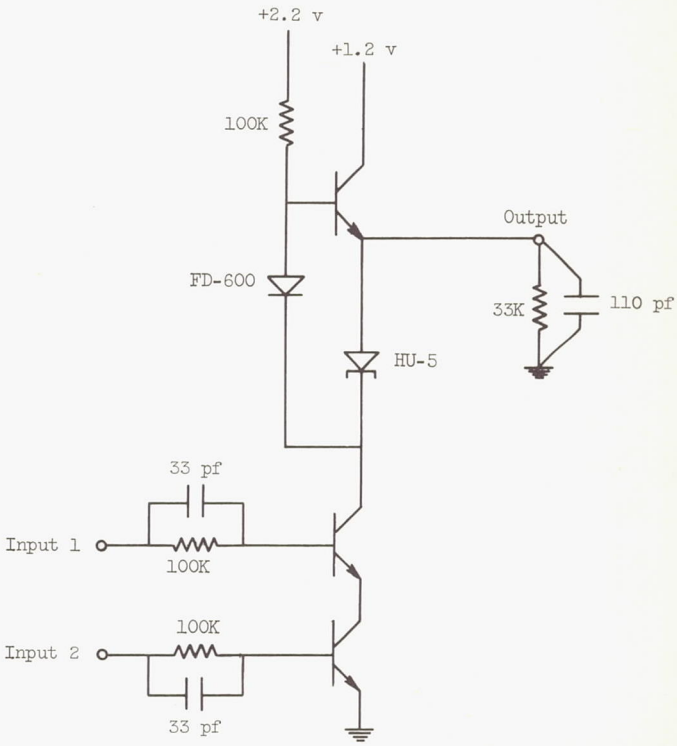
Figure 14. - Transistor input NOR.



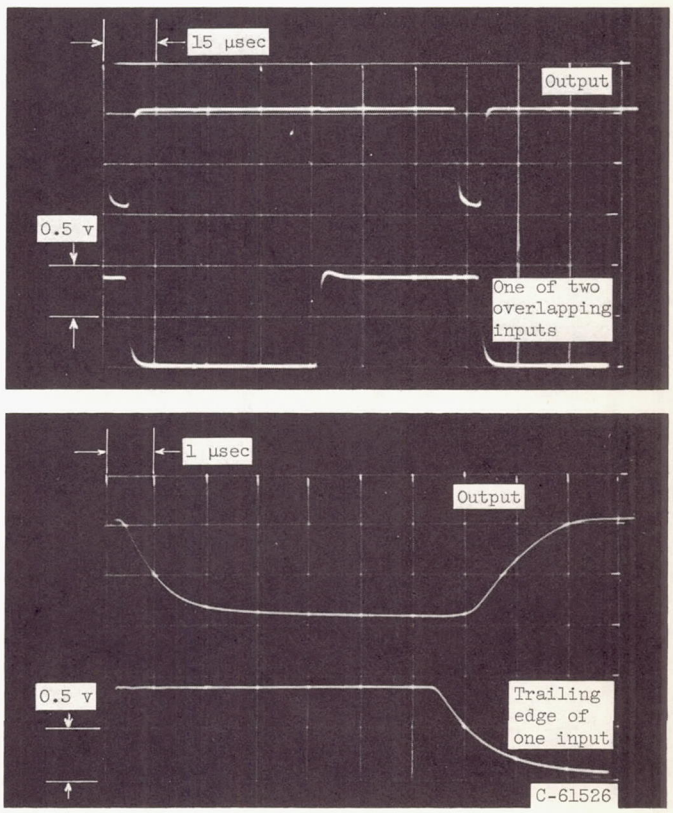
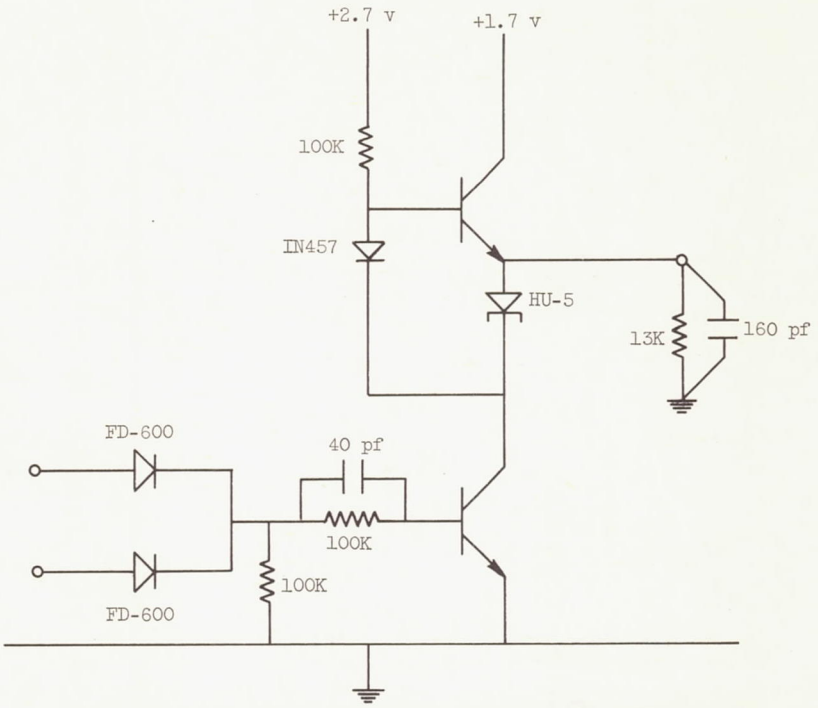
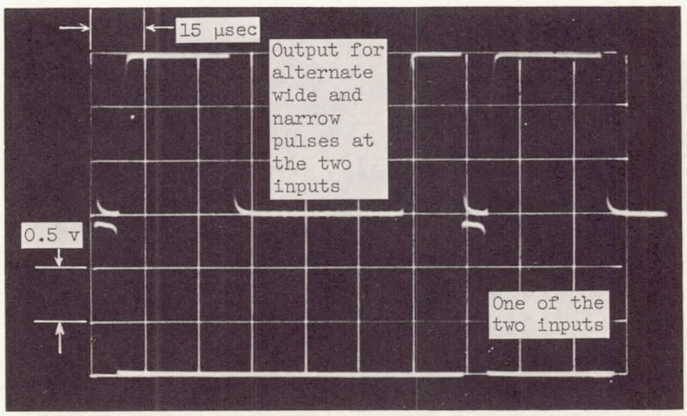


Figure 15. - Transistor input NAND.





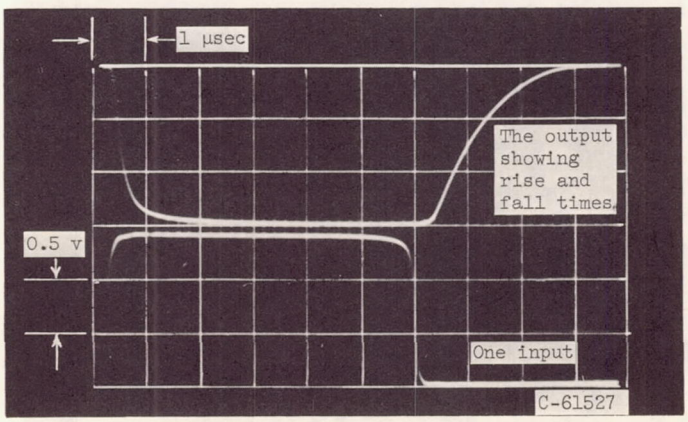
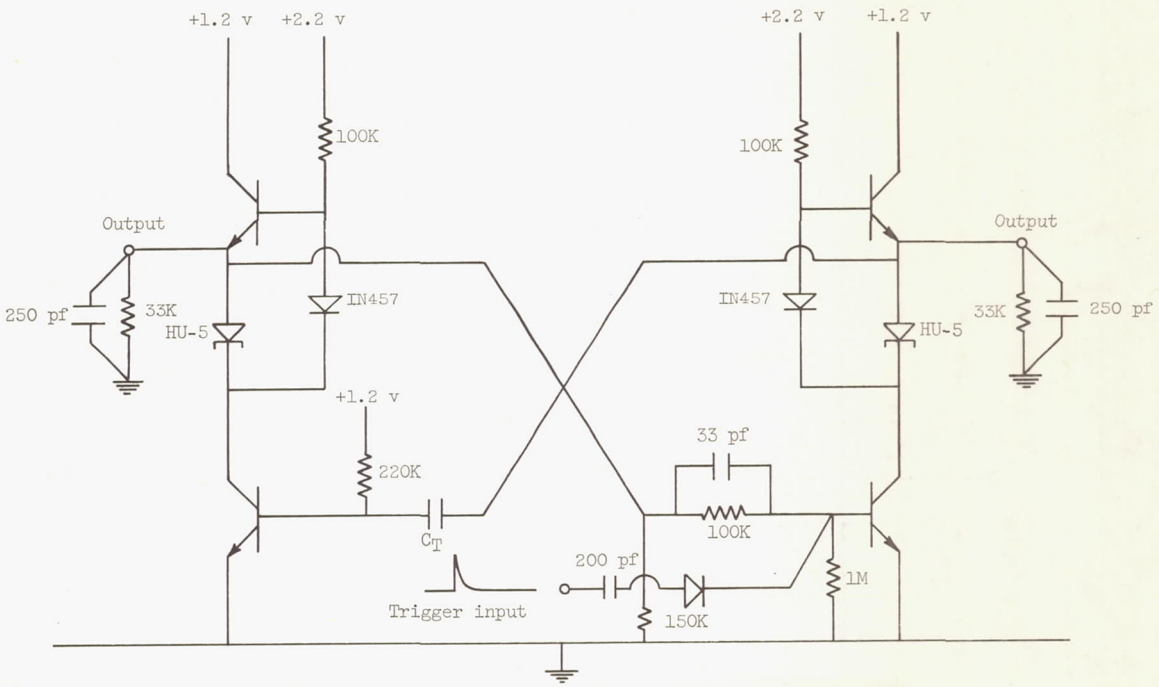
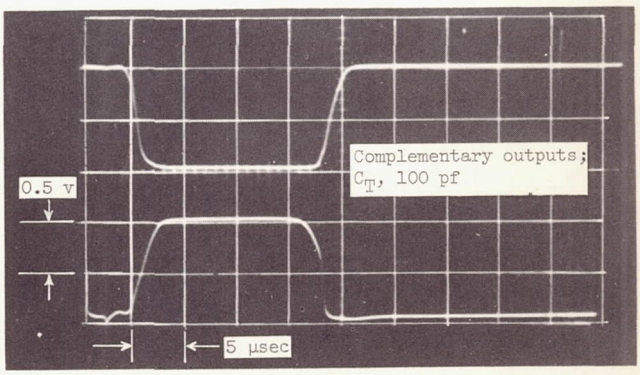
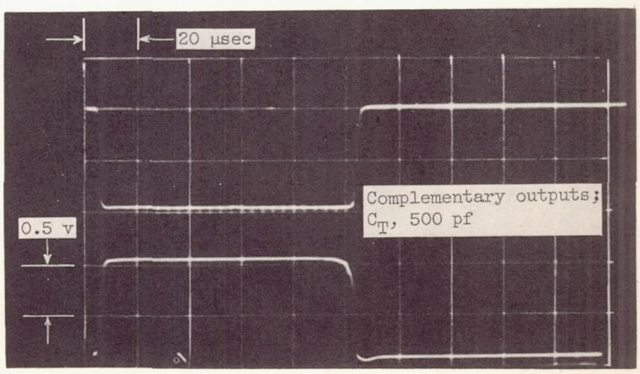


Figure 16. - Diode input NOR.







Timing capacitor	Output pulse width
0.02 µf	4.2 msec
500 pf	120 µsec
50 pf	12 µsec

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Figure 17. - Similar transistor monostable multivibrator.

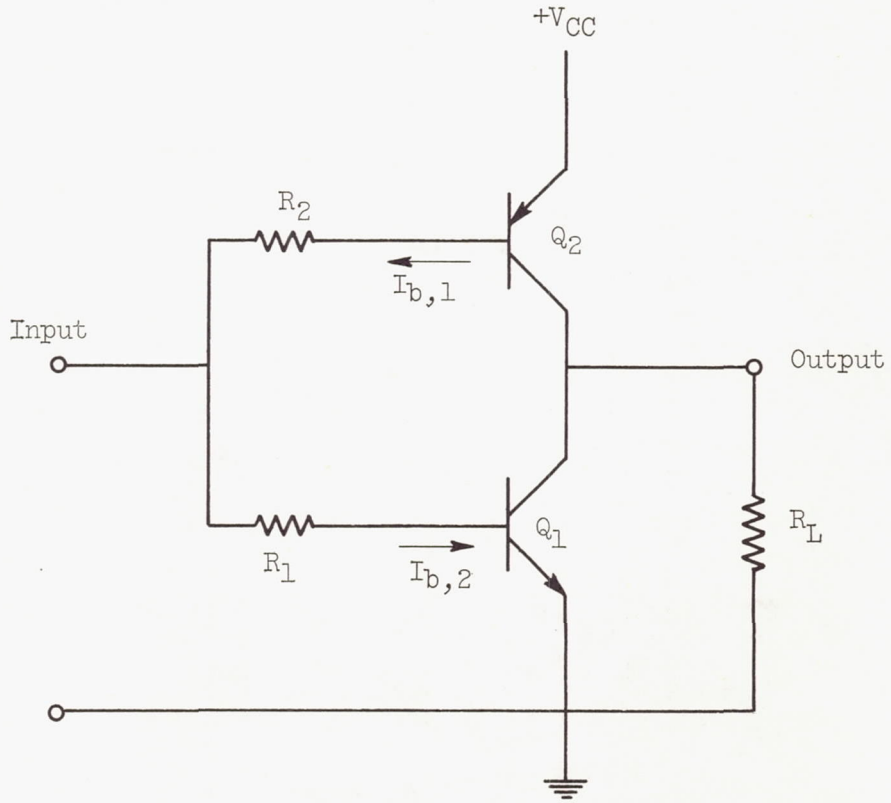
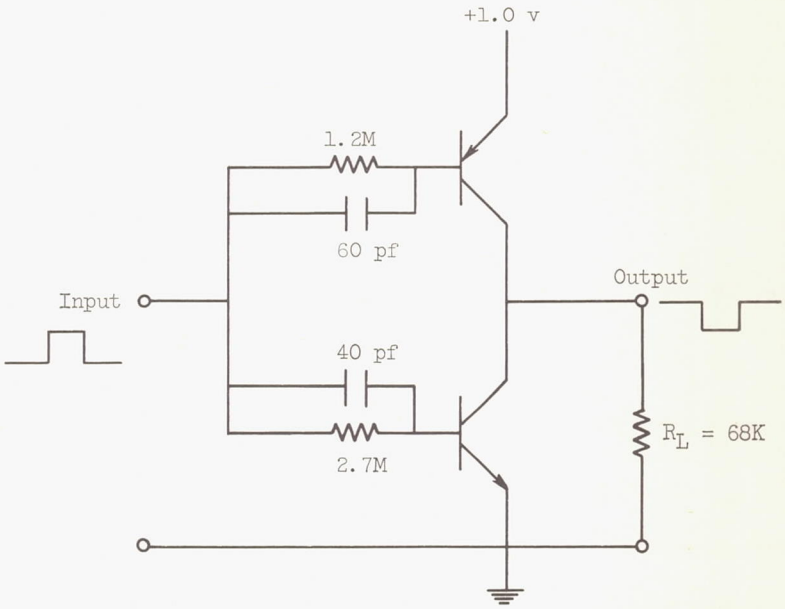
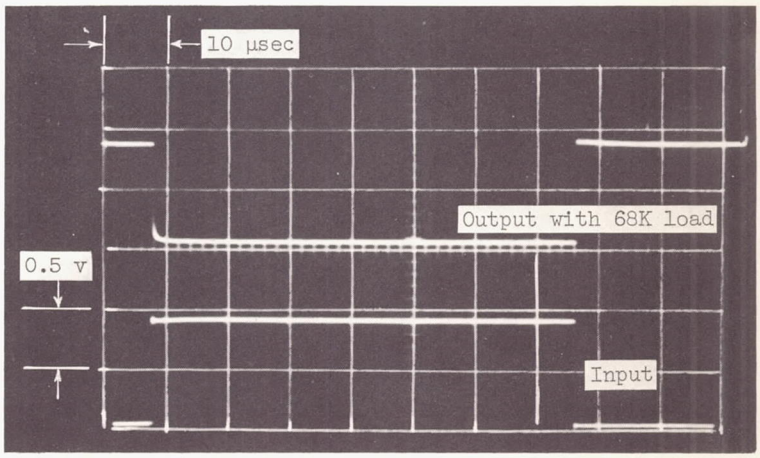


Figure 18. - Basic complementary inverter circuit.





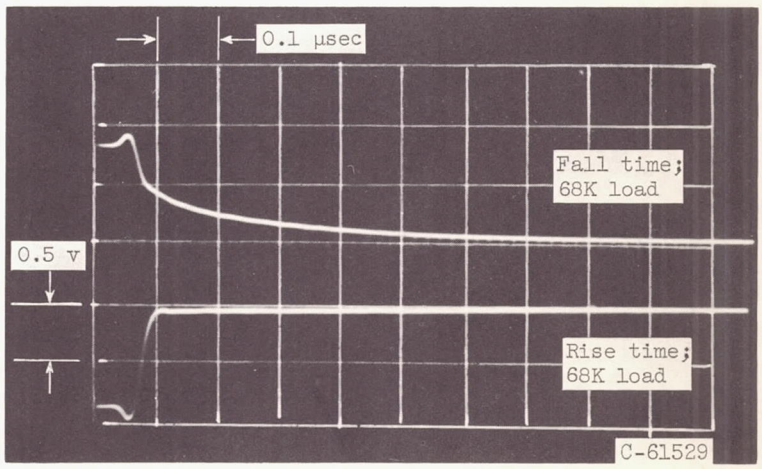


Figure 19. - Complementary inverter circuit.

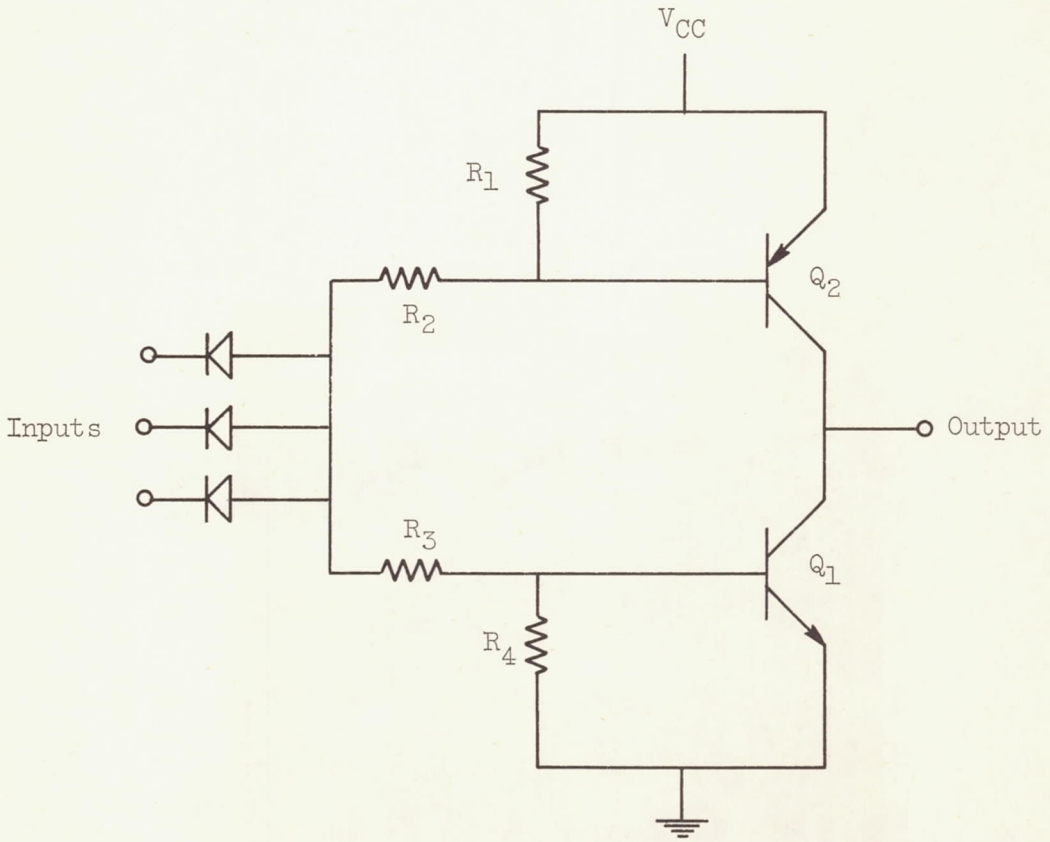
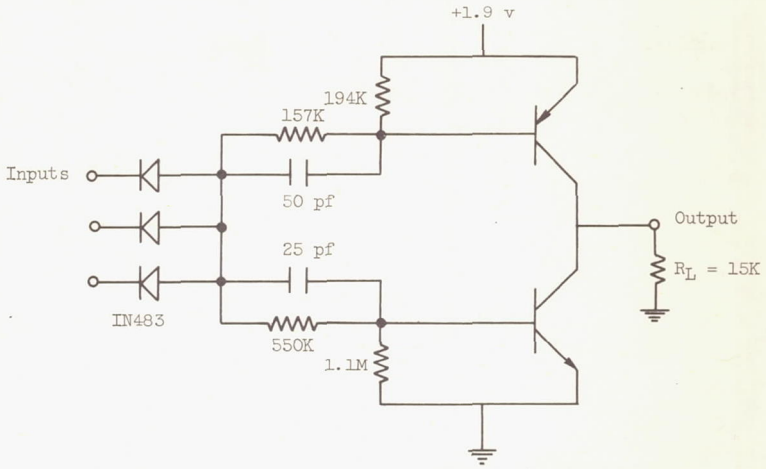


Figure 20. - Complementary inverter with diode gate input.



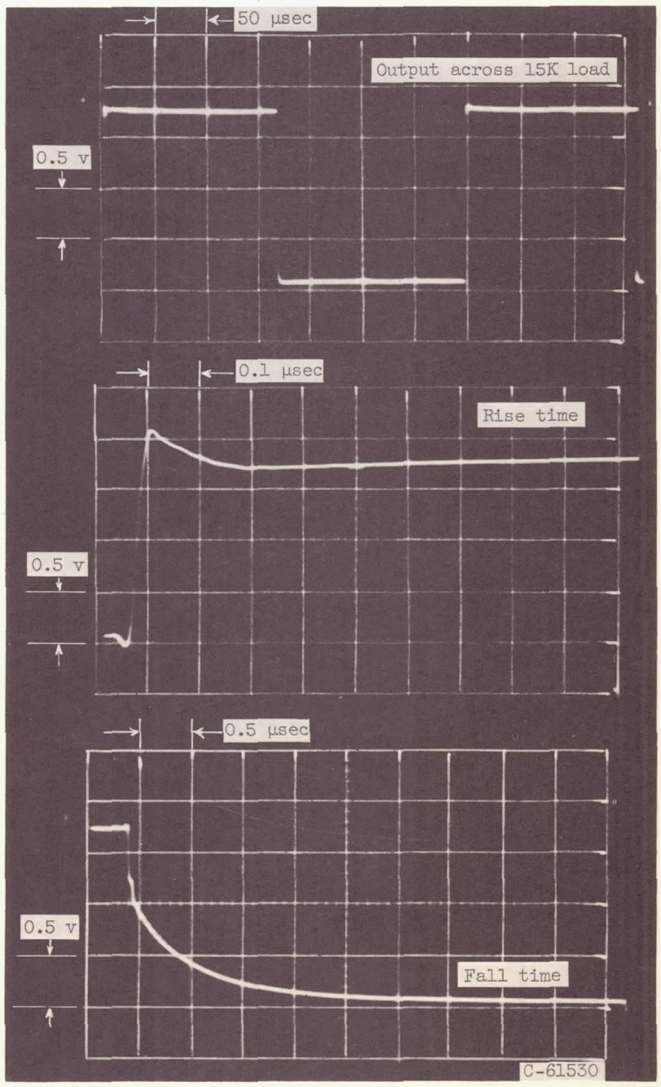


Figure 21. - Diode input complementary NAND.

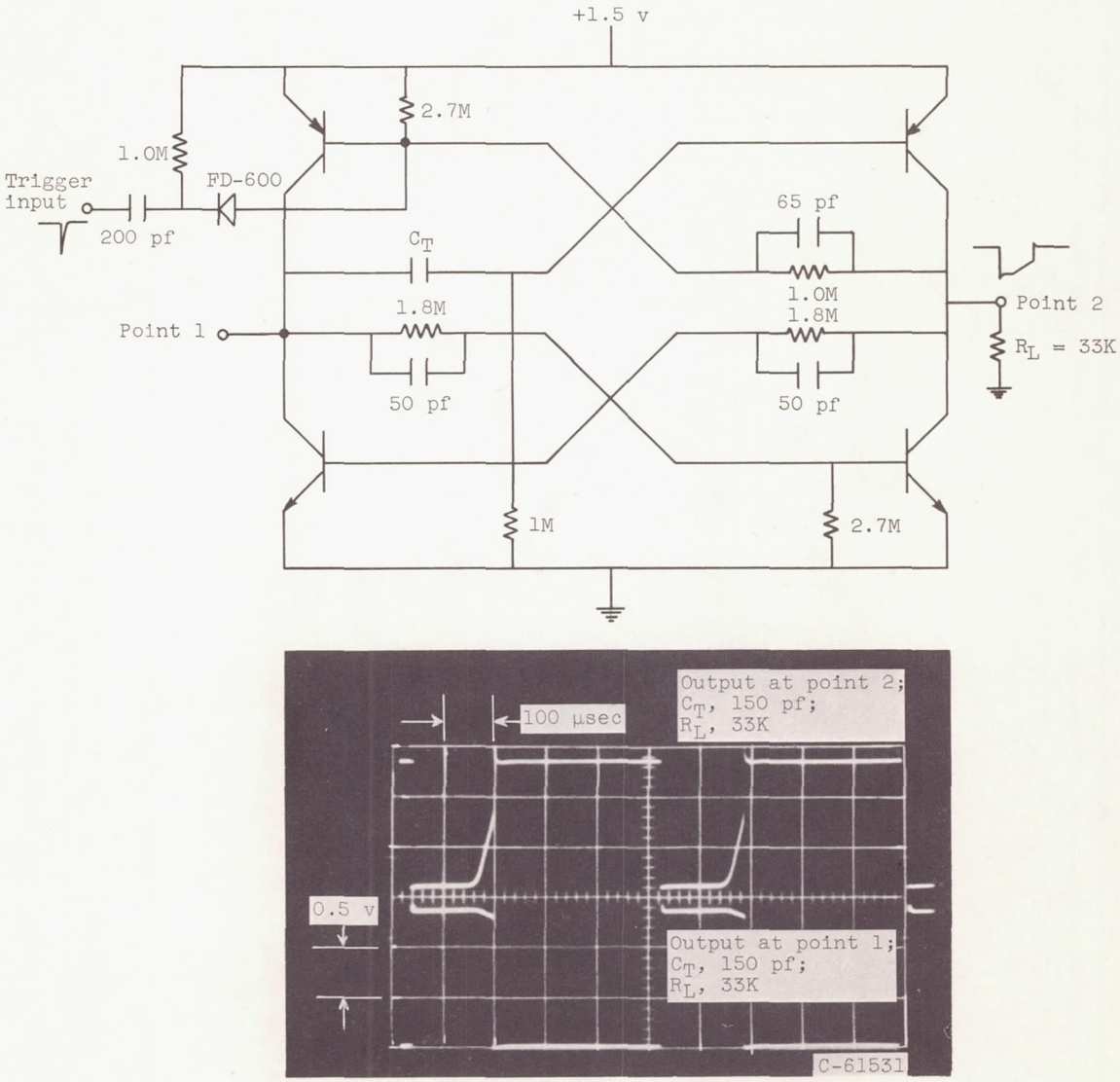
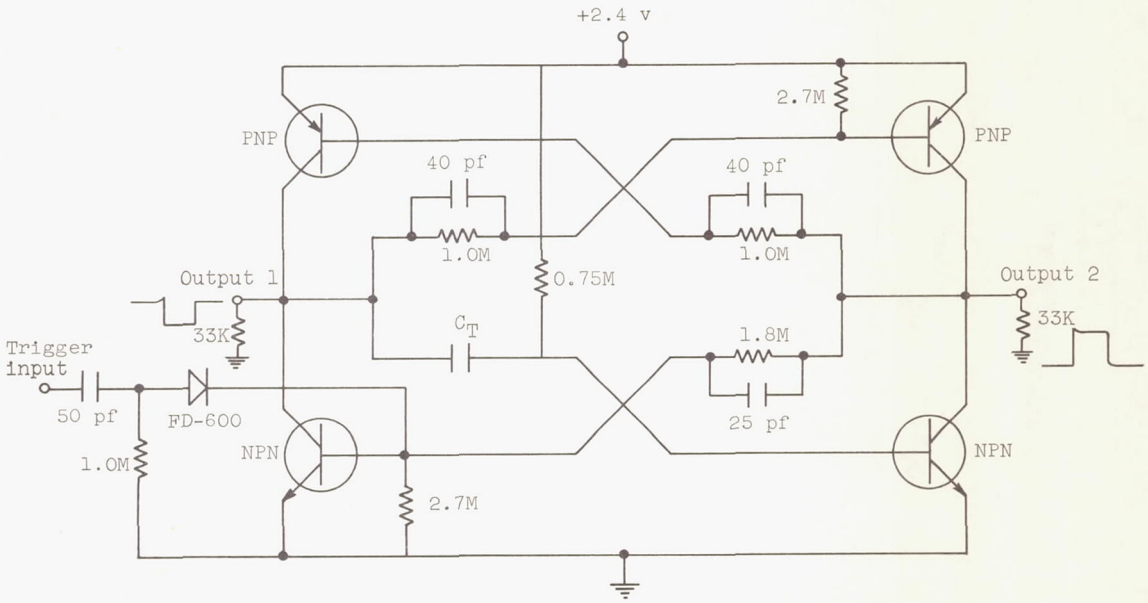


Figure 22. - Complementary monostable multivibrator.



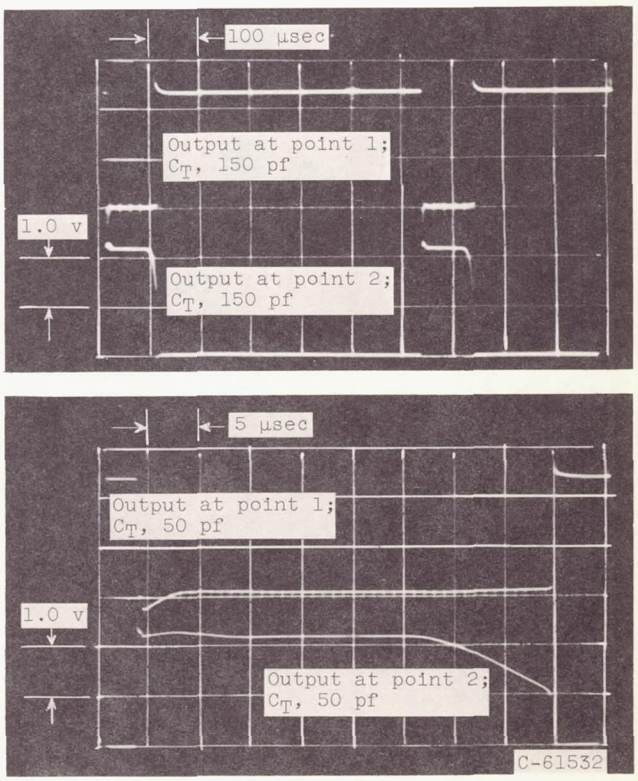
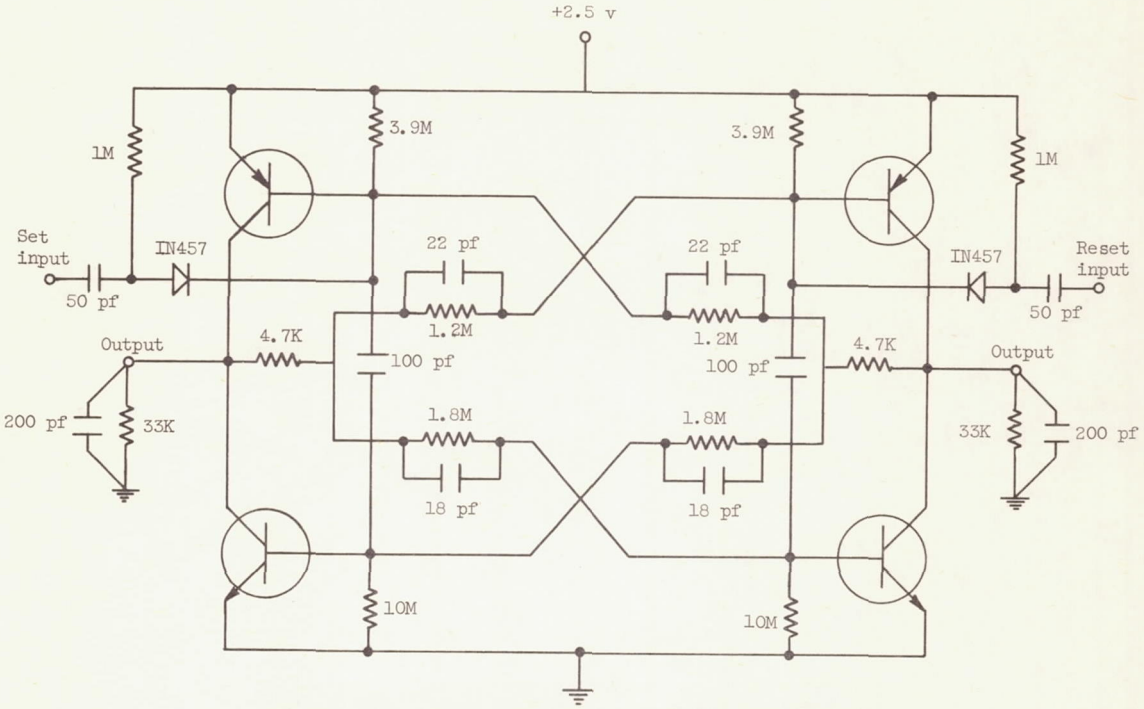
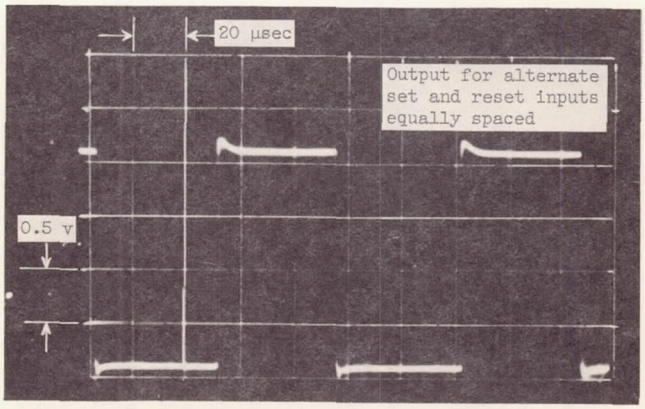


Figure 23. - Complementary monostable multivibrator for positive trigger.





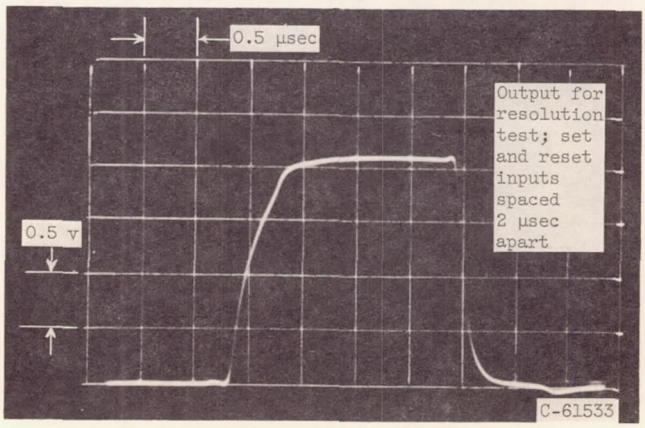
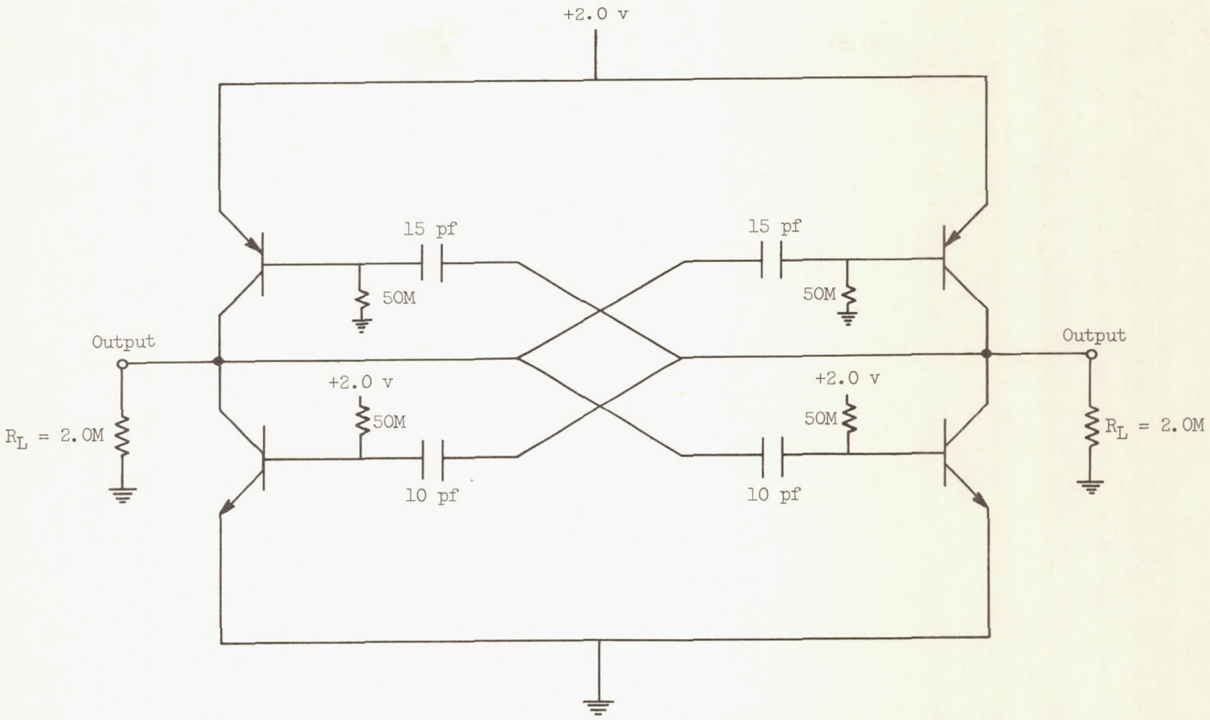


Figure 24. - Complementary transistor bistable.



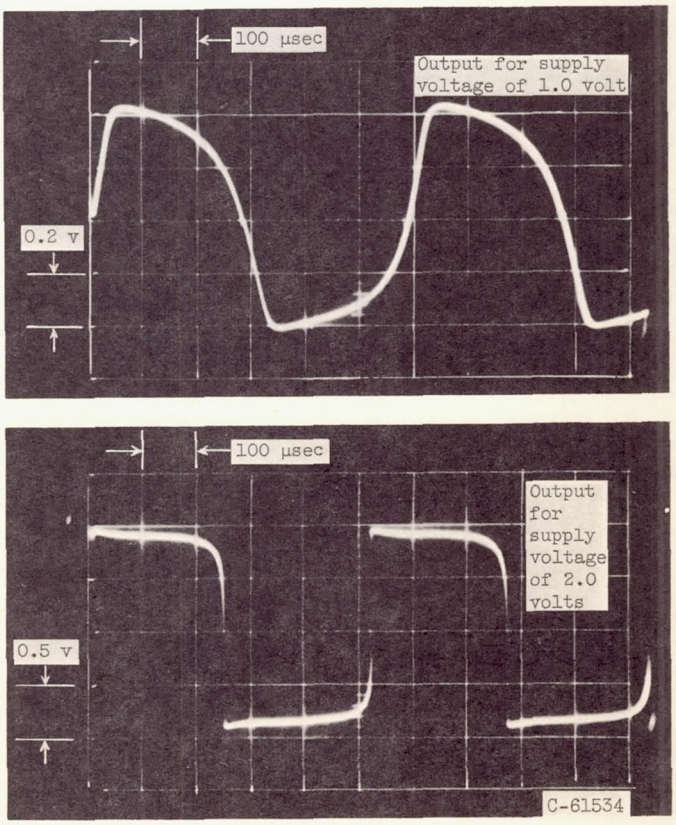


Figure 25. - Ultra-low-power free-running multivibrator.

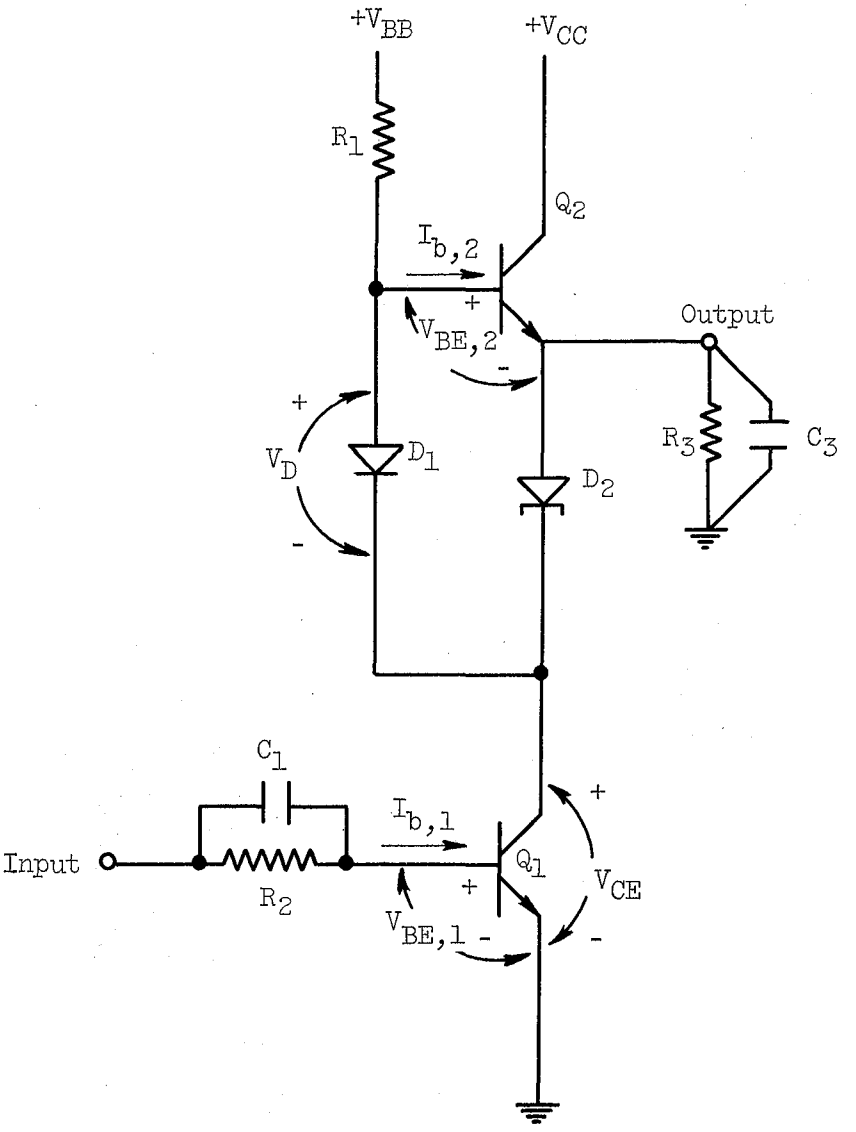
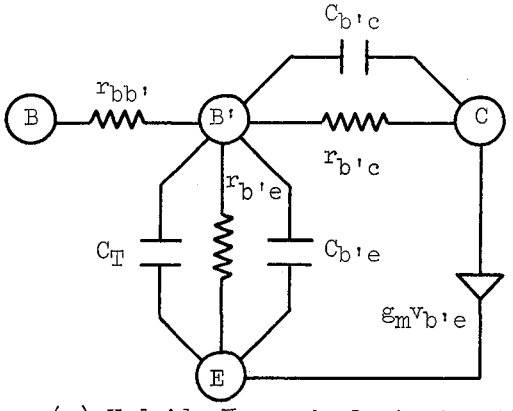
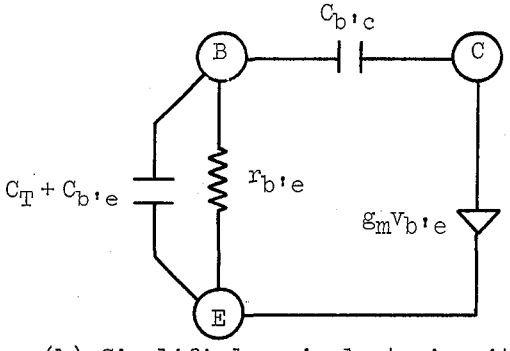


Figure 26. - Similar transistor inverter.



(a) Hydrid Π equivalent circuit.



(b) Simplified equivalent circuit.

$r_{bb'}$ = ohmic base resistance
$C_{b'e}$ = base-emitter diffusion capacitance
$C_{b'c}$ = C_{ob} = collector - base diode capacitance
C_T = base-emitter transition capacitance
$r_{b'e}$ = collector feedback resistance
$g_m v_{b'e}$ = $\beta i_{b'e}$
$g_m r_{b'e}$ = β

Figure 27. - Transistor equivalent circuits.

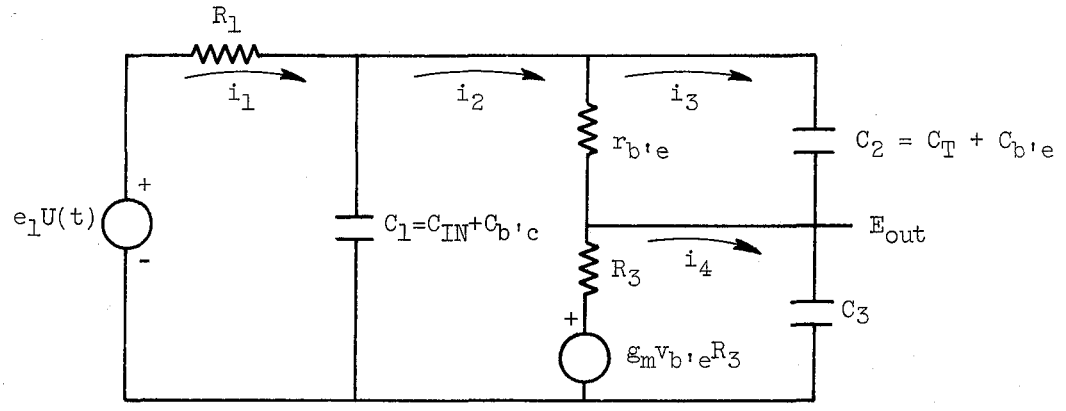


Figure 28. - Rise-time model for similar transistor inverter.

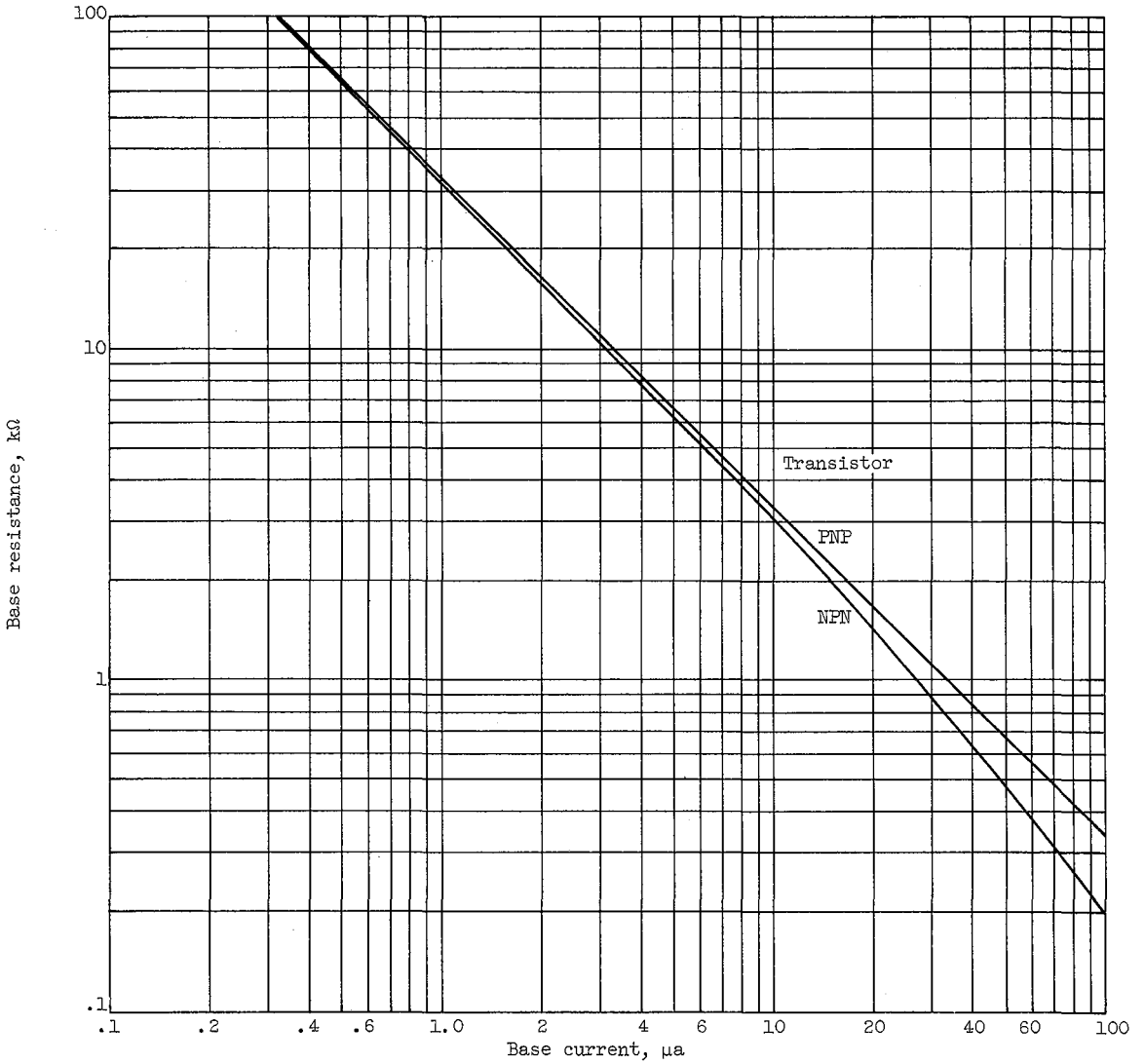


Figure 29. - Variation of small signal base resistance with base current for two representative transistors. Planar passivated transistors; S-4528 (PNP) and S-4529 (NPN).

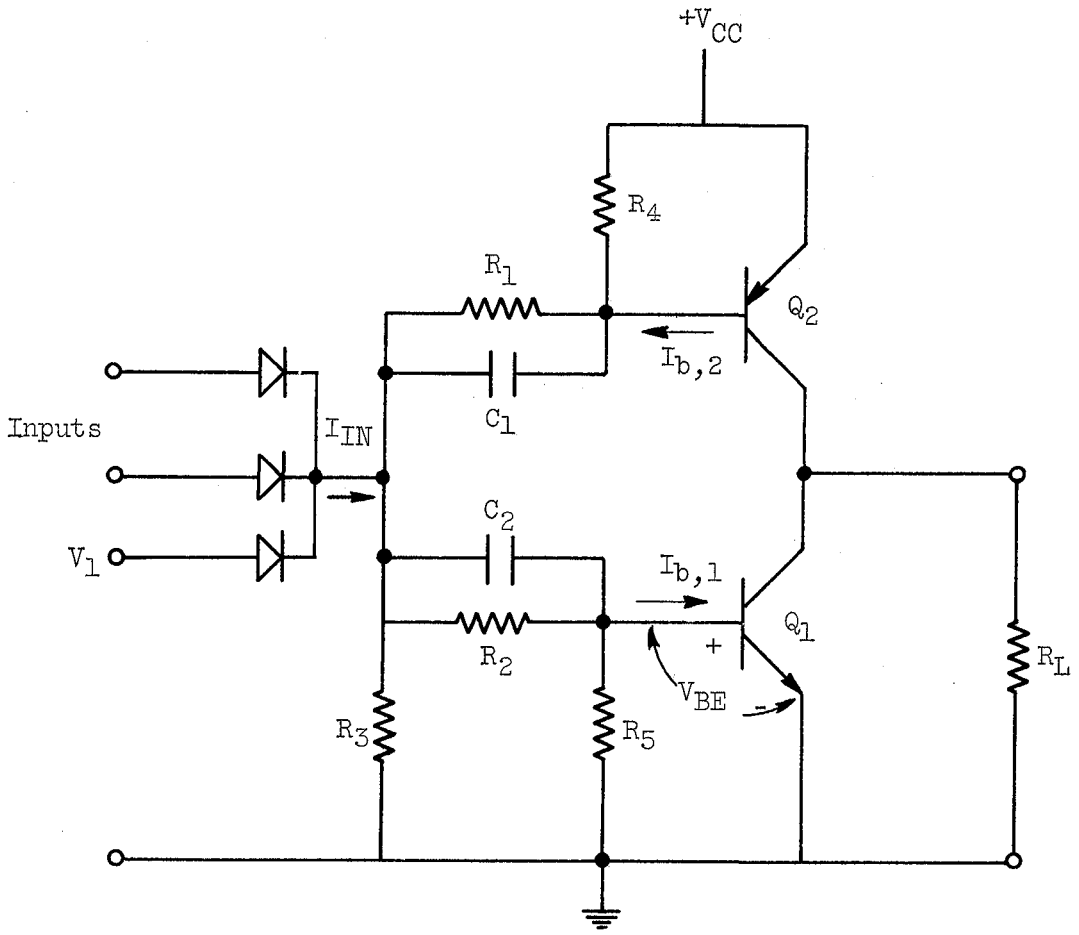


Figure 30. - Diode input complementary NOR.