X-561-63-199

41p.



# PFM SIMULATOR

SEPTEMBER 1963



NASA — GODDARD SPACE FLIGHT CENTER —
GREENBELT, MD.

# PFM SIMULATOR

Designers of the PFM Simulator:

Harold Levy,
Paul Heffner, and
Joseph Tinsley

Data Instrumentation Branch
Data Systems Division

September 1963 41p

NASA GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

CONTENTS


| | | Page |
|---|---|---|
| I | INTRODUCTION | 1 |
| II | SPECIFICATIONS | 2 |
| III | OPERATING INSTRUCTIONS | 5 |
| IV | DESCRIPTION AND THEORY OF OPERATION | 7 |
| V | CIRCUITS | 11 |
| | FREQUENCY BURST MIXER AND CLOCK CIRCUITS | 11 |
| | BISTABLE MULTIVIBRATOR (FLIP-FLOP) CIRCUIT | 17 |
| | MATRIX CIRCUIT | 17 |
| | RUNDOWN CIRCUIT | 20 |
| | ENVELOPE MULTIPLEXING AND OUTPUT BUFFERING CIRCUITS | 21 |
| | OSCILLATOR, AVC, AND OSCILLATOR GATE CIRCUITS | 21 |
| | POWER SUPPLY | 29 |
| VI | WIRING AND BOARD LOCATIONS | 33 |

## LIST OF ILLUSTRATIONS


| Figure | | Page |
|---|---|---|
| 1 | PFM Simulator (Mod C), Block Diagram. . . . . | 8 |
| 2 | Oscillator Gate External Control . . . . . | 9 |
| 3 | Flip-Flop – Run-Down External Control. . . . . | 10 |
| 4 | Frequency Burst Mixer and Clock . . . . . | 12 |
| 5 | Multiplexing the Separate Channel Bursts . . . . . | 13 |
| 6 | Diode Characteristic Curve . . . . . | 14 |
| 7 | Unijunction Clock Circuit. . . . . | 15 |
| 8 | Tunnel Diode and Unijunction Circuit Configuration . . . . . | 16 |
| 9 | Tunnel Diode and Family of Load Lines Corresponding to a Changing Source Voltage . . . . . | 16 |
| 10 | Flip-Flop Circuit . . . . . | 18 |
| 11 | Diode Matrix Board . . . . . | 19 |
| 12 | Rundown and Flip-Flop Operating Together as Monostable Multivibrator . . . . . | 20 |
| 13 | Run-Down Circuit . . . . . | 22 |
| 14 | Envelope Multiplexing and Output Buffering Circuits . . . . | 23 |
| 15 | Oscillator, AVC, and Oscillator Gate Circuits. . . . . | 24 |
| 16 | AVC Loop . . . . . | 27 |
| 17 | Complete L Pad. . . . . | 27 |
| 18 | AC Equivalent L Pad . . . . . | 27 |

LIST OF ILLUSTRATIONS (CONT.)


| Figure | | Page |
|---|---|---|
| 19 | Equivalent L Pad Seen by Input Signal . . . . . | 28 |
| 20 | Diode Characteristic Curve . . . . . | 28 |
| 21 | Power Supply, PFM Simulator (Mode II) . . . . . | 30 |
| 22 | Power Supply Parts Layout (Bottom View). . . . . | 31 |
| 23 | Board Location (Top View) . . . . . | 34 |
| 24 | Bucket No. I Wiring Diagram, PFM Simulator (Bottom View) . . . . . | 35 |
| 25 | Bucket No. II Wiring Diagram, PFM Simulator (Bottom View) . . . . . | 36 |

# PFM SIMULATOR

## I. INTRODUCTION

The pulse frequency modulation (PFM) simulator was designed in 1960 as a laboratory instrument to assist in the design and checkout of PFM equipment. The criteria for flexibility, data burst rates, data frequency ranges, etc., were based on previous PFM satellite ranges and expected future ranges. The unit was later modified to provide a frequency during the blank time to simulate the newer PFM signal formats.

The unit simulates the synchronous 16-channel frame pulse frequency-modulated signal with frame synchronization burst. Burst width, burst frequency, and burst amplitude for each channel are variable by front panel control. The frame synchronization burst can be positioned where desired at the beginning of the frame. The unit covers the broad data burst-rate range of two data bursts per second to 3000 data bursts per second, and is continuously variable over these limits in just two ranges. The frequency within each data burst may be internally or externally applied; noise may be linearly summed with the signal by application of a noise generator signal to the unit.

The unit, which is fully transistorized, employs functional printed circuit modules, including the power supply regulator. All circuits were designed by the Data Instrumentation and Development Branch. All outputs from the unit are protected against short circuits to ground.

## II. SPECIFICATIONS

| | |
|---|---|
| SIGNAL: | Synchronous pulse frequency modulated, 16-channel frame with synchronization burst and blank time reference frequency |
| CHANNELS: | |
| Number: | Sixteen |
| Individual controls for each channel: | |
| Burst frequency: | Internal or external. (Internal frequency continuously variable in two ranges covering 4.5 kc to 45 kc) |
| Burst duration: | Continuously variable, 0.33 ms to 500 msecs in two ranges |
| Burst amplitude: | Continuously variable, 0 to 4 vpp |
| Burst dc level: | ±0.5v continuously variable about 0vdc level of signal |
| SYNCHRONIZATION BURST: | Same controls as those for individual channels, plus control to position sync burst where desired between channel 16 and channel 2 (back panel controls) |
| REFERENCE FREQUENCY (BLANK TIME FREQUENCY): | |
| Frequency: | Internal or external. (Internal frequency continuously variable in two ranges covering 4.5 kc to 45 kc) |
| Amplitude: | Continuously variable to 0 to 4 vpp (back panel) |
| dc level: | ±0.5v continuously variable about PFM signal dc level (back panel) |

| | |
|---|---|
| Omission of signal: | Front panel control switch provides switching reference frequency in or out of PFM signal |
| REPETITION RATE (SIMULATED SAMPLING RATE): | 2 cycles/sec to 3 kilcycles/sec continuously variable, 2 ranges |
| CHANNEL BURST FREQUENCY AND REFERENCE FREQUENCY MONITOR: | Any one channel burst frequency or the reference frequency may be monitored from one BNC connector on back panel.<br><br>A 17-position switch on front panel provides for selection of desired signal frequency to be monitored. |
| TOTAL SIGNAL AMPLITUDE CONTROL (BURST OUTPUT AMPLITUDE): | Continuously variable, 0 to 4 vpp |

INPUTS AND INPUT IMPEDANCES:

| | |
|---|---|
| Noise input: | 13 kilo-ohms |
| Ext. Osc. input (back panel): | 15 kilo-ohms |

OUTPUTS AND OUTPUT IMPEDANCES:

| | |
|---|---|
| Frequency burst output: | 100 ohms |
| Burst envelope output: | 100 ohms |
| Comp. envelope output: | 100 ohms |
| Burst No. 1 Sync output: | 100 ohms |
| Burst No. 16 Sync output: | 100 ohms |
| Osc. output (back panel): | 10 kilo-ohms |

| | |
|---|---|
| POWER: | 105-120 volts rms<br>60 watts |

| | |
|---|---|
| ENVIRONMENTAL: | 60° F to 105° F |
| PHYSICAL: | Rack mountable (standard 19-inch rack) |
| Height: | 14 inches |
| Depth: | 17-1/2 inches |
| Controls: | Front and rear panels |

## III. OPERATING INSTRUCTIONS

1. Turn on power.
2. Synchronize scope at BURST NO. 16 OUT BNC.
3. Adjust burst-blank period:
   a. Turn each channel width delay to minimum.
   b. Monitor FREQ. BURST OUT and adjust BURST-BLANK PERIOD controls to obtain proper sample rate.
4. Adjust delay between the occurrence of channel 16 and channel 1 (sync burst) at the rear of the unit with SYNC POSITION CONTROLS.
5. Adjust individual channels for desired burst-duration using BURST-WIDTH CONTROLS.
6. Adjust individual channel frequencies using BURST FREQ. controls. The blank frequency is adjusted at the rear of the unit. Each channel frequency including the BLANK frequency may be monitored by a decimal counter from the rear of the unit at OSC. OUTPUT BNC. The selector switch on the front panel selects the desired channel or blank frequency to be monitored.

   (NOTE: If a channel frequency burst does not vary about ground, it may be balanced correctly with the BURST DC LEVEL screwdriver adjustment.)

   External sources for channel frequencies may be used by applying input sine waves at about 5 vpp. (The signal passes through an AGC circuit before being brought into the respective channel oscillator gate.) The signal is applied at the chosen channel BNC connection on the back panel of the unit and the switch associated with the BNC must be switched to EXT.
7. The blank frequency may be switched into or out of the signal by a switch located on the front panel of the unit and labeled BL.
8. The composite signal amplitude may be varied by the SIGNAL AMPLITUDE adjust on the front panel.
9. Noise may be applied at the NOISE INPUT BNC.
10. Individual circuit module adjustments:
    a. Adjusting the oscillators:

       The frequency range of the oscillator can be raised or lowered by adjustment of the trimpot located on the board. A change in

the trimpot will affect the high end of the oscillator range more than the low end.

b. Adjusting the power supply:

Both power supply voltages may be trimmed by adjustment of the two trimpots located on the power supply board.

## IV. DESCRIPTION AND THEORY OF OPERATION

The PFM simulator consists of 17 separate oscillator gates whose outputs can be gated on or off upon digital command. Control of the gating is made through a timing generator consisting of a clock, a four-stage binary counter, and a decoder as shown in Figure 1. The decoder is implemented by an AND matrix having 16 separate outputs, each providing a separate pulse sequentially with time. These outputs constitute the beginning of each channel burst, initiating a wide-range monostable multivibrator (MSMV) which constitutes the individual burst width. The outputs of these multivibrators are then the gating pulses to the oscillator gates. Exception to this is the synchronization burst which can be placed where desired between channel 16 and channel 2. This is implemented by placing in series with the synchronization burst width MSMV another wide-range MSMV which provides an adjustable delay time between the last channel of the succeeding frame and initiation of the sync. burst MSMV. One of the oscillator gates is digitally controlled by the resultant envelope of the combined gate control signals of the individual channels, so that when chosen (by switch) this oscillator gate will pass an oscillator signal during all times that no other gate is on. This will later constitute the blank frequency in the output signal.

An internal or external oscillator may be chosen as the oscillator signal into each oscillator gate. The chosen signal is first passed through an automatic gain control circuit and then through a variable L pad for amplitude control before being applied to the oscillator gate. The individual oscillator-gate input levels can then be set as desired; for each setting the signal amplitude into the oscillator gates will remain fixed even though the applied internal or external oscillator signal amplitudes may differ.

The output gated signals from all the oscillator gates are then linearly mixed, providing a time-division multiplexed simulated PFM signal. The signal is synchronous since all the channel bursts (except the synchronization burst) are initiated at a fixed period given by the clock. The mixed signal is amplified, buffered against output short circuits to ground, and applied to the FREQUENCY BURST OUT BNC. Noise, if applied, is added to the combined signal through linear resistive summing in the buffering stage following the amplifier.

The digital control pulses to the individual gates are brought into a separate circuit for summing and inverting for the ENV. OUT and

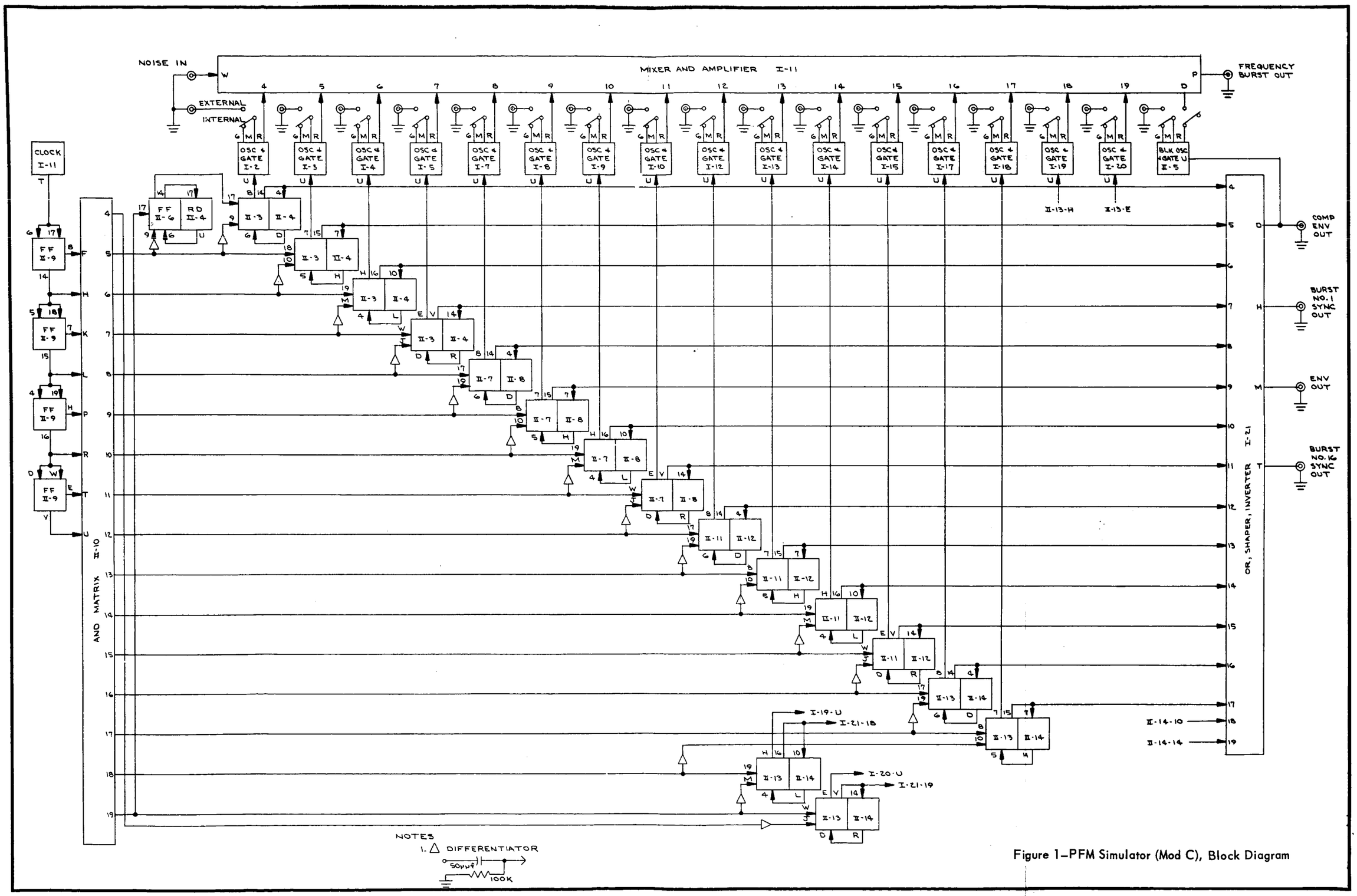



Figure 1–PFM Simulator (Mod C), Block Diagram

COMP ENV. OUT and to provide oscilloscope synchronization with BURST NO. 1 SYNC. OUT and BURST NO. 16 SYNC. OUT.

The facility to monitor each continuous-wave frequency being applied to the separate oscillator gates is made available by applying each gate oscillator input signal to a switch where selection of any one signal will apply that desired signal to the OSC. OUT BNC.

Figures 2 and 3 show the external control for the oscillator gate and the flip-flop – run-down circuits.

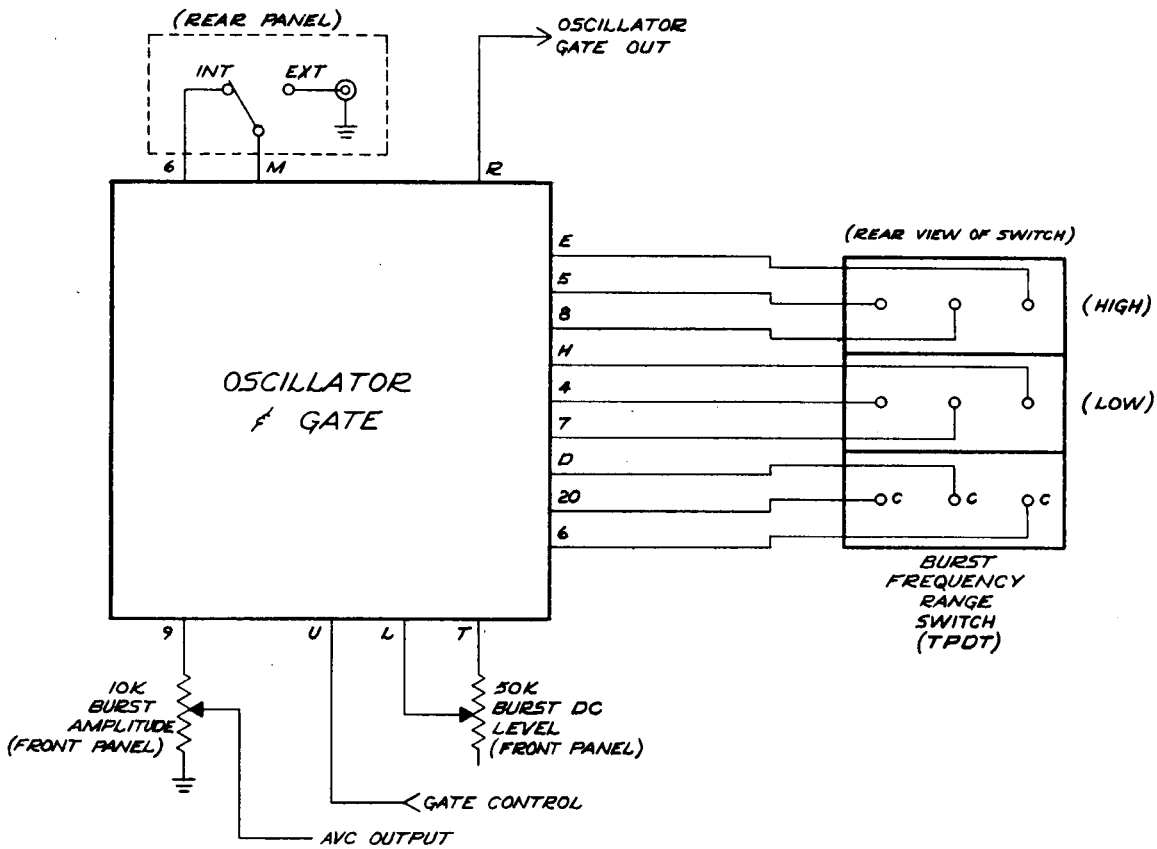
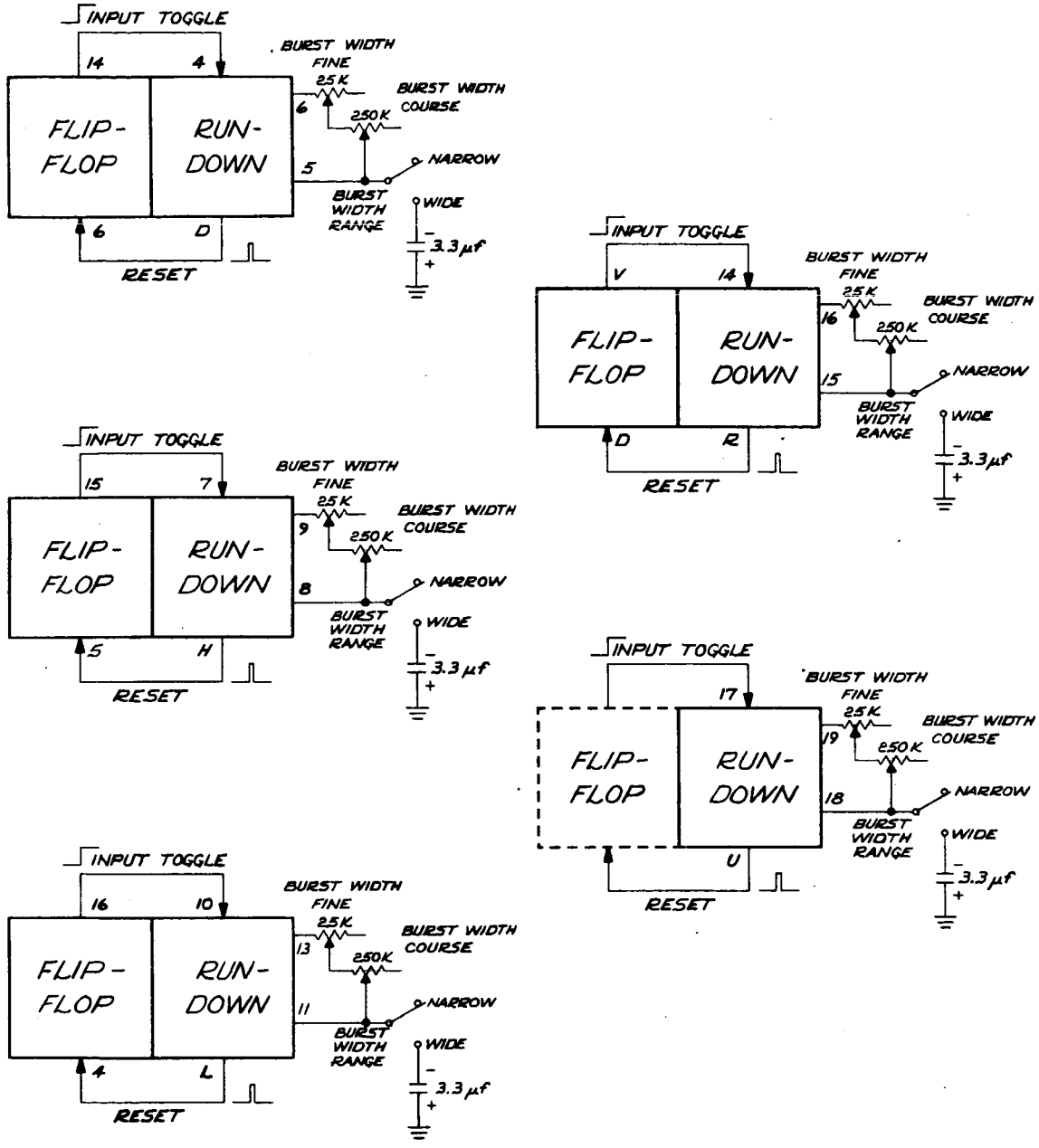



Figure 2-Oscillator Gate External Control




NOTE:

ALL POTENTIOMETERS / SWITCHES SHOWN ARE FRONT PANEL MOUNTED.

Figure 3-Flip-Flop - Run-Down External Control

# V. CIRCUITS

## FREQUENCY BURST MIXER AND CLOCK CIRCUITS

The frequency burst mixer and the simulator clock are both fabricated on one p.c. board. Each circuit will be discussed separately.

### Frequency Burst Mixer

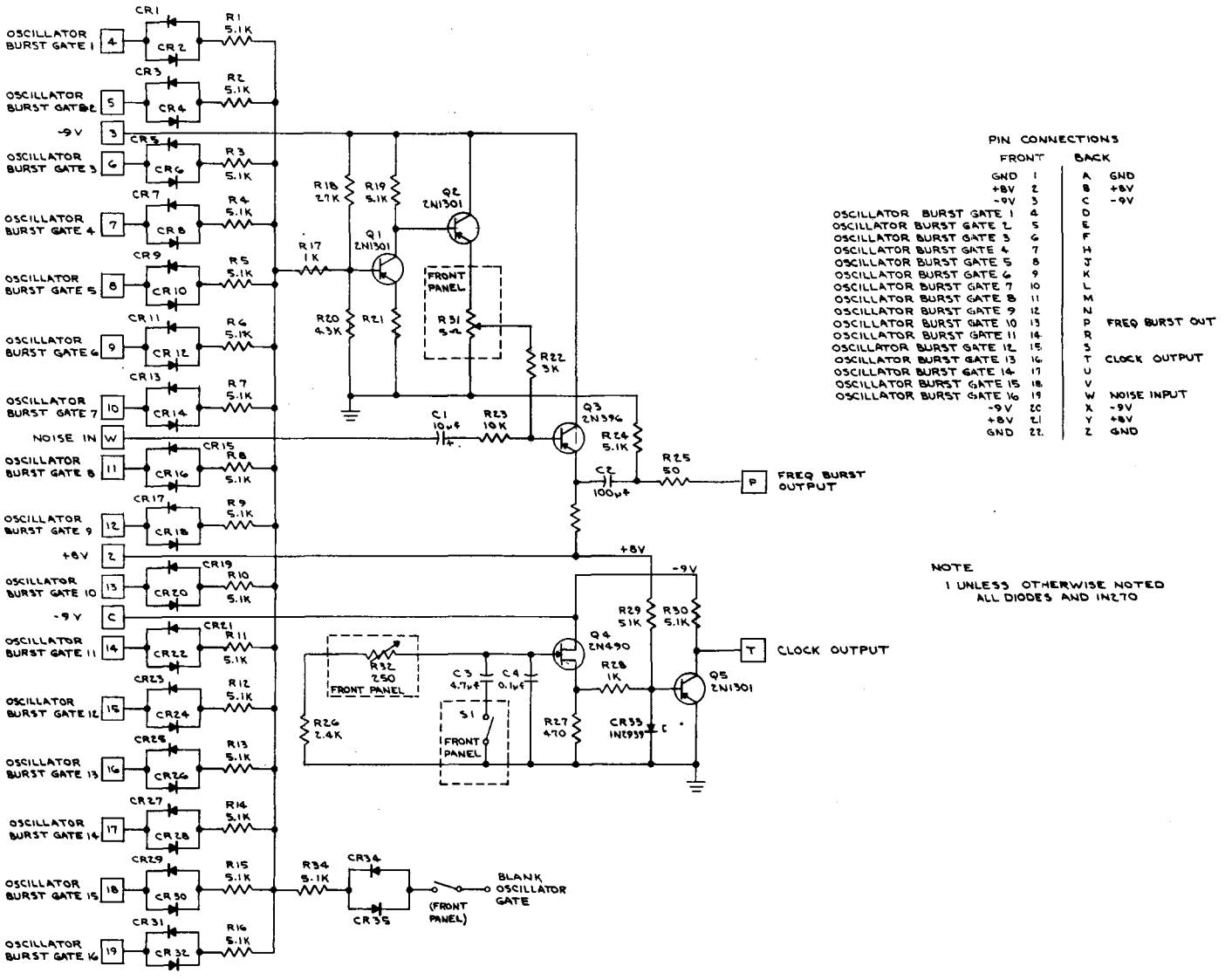
The frequency burst mixer (Figure 4) multiplexes the output from each of the 16 oscillator gates, each being activated at separate channel times, so that the output signal is then the time-division multiplexed PFM simulated signal. An additional input allows a gated blank frequency oscillator to be multiplexed with the other 16 channel input oscillator gates so that the output can then represent the PFM signal having a fixed reference frequency contained in each blank between the information bursts.

The technique for multiplexing the total 17-frequency burst inputs is that of summing all the signals at a common junction. The summed signal is then amplified to restore the input signal level from attenuation incurred during the summing.

Because each oscillator gate output, when a burst is not present, is the result of a fully saturated transistor clamping a continuous wave output signal to ground, there results on this clamped output a small continuous wave signal equivalent in dynamic level to the saturated voltage drop of the clamping transistor. A transistor having a very low saturating voltage drop ($V_{ce}$ SAT. = 0.05v) was chosen as the clamping transistor.

Therefore, if the signal degradation during blank times is about .05 volts for each input, for 17 inputs the summed signal in the worst case will be approximately 0.85 volts during blank times – a figure too large to be tolerated.

In order to avoid the summing of this signal degradation and other small noise which might be present within the system and still not to alter appreciably the frequency burst, two oppositely directed balanced diodes in parallel are employed at each input to the mixer (see Figure 5).




PIN CONNECTIONS

| | FRONT | BACK | |
|---|---|---|---|
| GND | 1 | A | GND |
| +8V | 2 | B | +8V |
| -9V | 3 | C | -9V |
| OSCILLATOR BURST GATE 1 | 4 | D | |
| OSCILLATOR BURST GATE 2 | 5 | E | |
| OSCILLATOR BURST GATE 3 | 6 | F | |
| OSCILLATOR BURST GATE 4 | 7 | H | |
| OSCILLATOR BURST GATE 5 | 8 | J | |
| OSCILLATOR BURST GATE 6 | 9 | K | |
| OSCILLATOR BURST GATE 7 | 10 | L | |
| OSCILLATOR BURST GATE 8 | 11 | M | |
| OSCILLATOR BURST GATE 9 | 12 | N | |
| OSCILLATOR BURST GATE 10 | 13 | P | FREQ BURST OUT |
| OSCILLATOR BURST GATE 11 | 14 | R | |
| OSCILLATOR BURST GATE 12 | 15 | S | |
| OSCILLATOR BURST GATE 13 | 16 | T | CLOCK OUTPUT |
| OSCILLATOR BURST GATE 14 | 17 | U | |
| OSCILLATOR BURST GATE 15 | 18 | V | |
| OSCILLATOR BURST GATE 16 | 19 | W | NOISE INPUT |
| -9V | 20 | X | -9V |
| +8V | 21 | Y | +8V |
| GND | 22 | Z | GND |

NOTE
1 UNLESS OTHERWISE NOTED ALL DIODES AND IN270

Figure 4-Frequency Burst Mixer and Clock

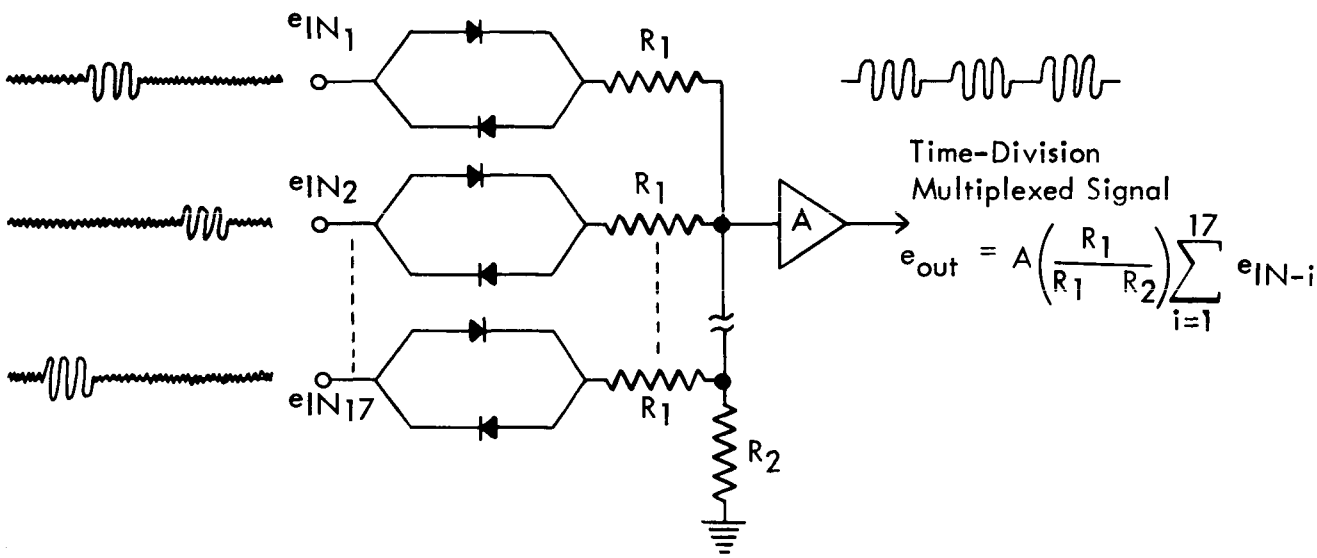



Figure 5-Multiplexing the Separate Channel Bursts

Considering the familiar Germanium diode characteristic (see Figure 6) it can be seen that the impedance seen looking into the diode for $e \leq .05$ volts is very high (in the order of 100 kilo-ohms) and that the impedance seen looking into the diode for $e \leq 0.3v$ is very low (in the order of 100 ohms).

By making $R_1$ and $R_2$ small in Figure 5, the degraded blank time ground level signals will all see very high impedances, whereas a 2vpp frequency burst will see a very low impedance to the summing junction. Passing a sine wave through such a network will produce crossover distortion, but this distortion is negligible.

The amplifier following the summing junction (Q1 on Figure 4) is a Class A amplifier having a voltage gain of 5. This amplifier works into an emitter follower (Q2) where the emitter resistor is center-tapped for control of the entire simulated signal level. This variable resistor is a front panel control. At Q3 the simulated signal is summed with the noise input. The output of Q3 is capacitively coupled to outside equipment at the FREQ BURST OUTPUT BNC.

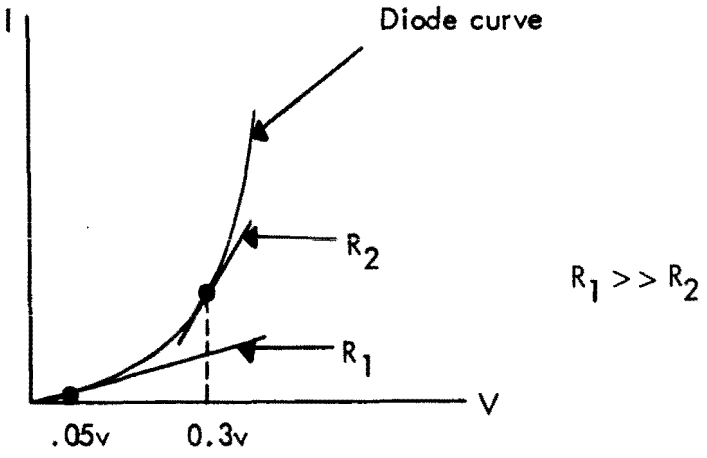



Figure 6-Diode Characteristic Curve

Clock

The frequency generator, or clock source, for the PFM simulator is a relaxation oscillator employing a unijunction transistor and a tunnel diode.

The unijunction serves as a threshold device having two thresholds: a threshold at which the device becomes appreciably resistanceless and a threshold at which it becomes a very high impedance. In shunt with the input to the unijunction is a capacitor (C) which is charged through resistor (R) as shown in Figure 7.

If C is at $V_{off}$, implying that C had discharged toward -V volts until the unijunction turned off (when $V_C = V_{off}$), C will charge toward ground according to the relation:

$$V_C = V_{off} (E^{-t/Rc}) \quad (1)$$

When

$$V_C = \eta V_{B_1B_2} \quad (2)$$

(where $\eta$ is the intrinsic stand-off ratio), the unijunction will fire and discharge C until $V_C = V_{off}$, at which time C begins again to charge.

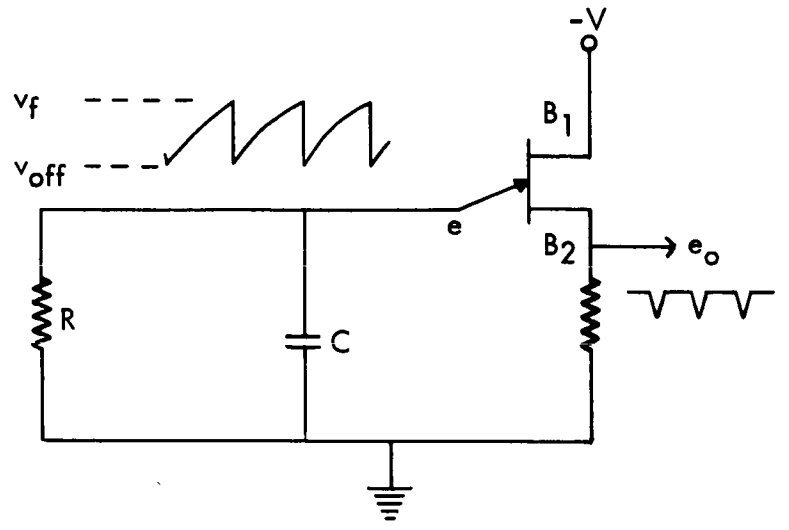



Figure 7-Unijunction Clock Circuit

Equating (1) and (2) then gives

$$V_{off}(e^{-t/RC}) = \eta V_{B_1 B_2}$$

from which

$$t = RC \ln \frac{V_{off}}{\eta B_1 B_2}$$

For the condition above to have been reached, t must be equal to one period. The period of the clock can be expressed as

$$P = \Delta t = RC \ln \frac{V_{off}}{\eta B_1 B_2}$$

or the frequency as

$$f = \frac{1}{RC \ln \frac{V_{off}}{\eta B_1 B_2}}$$

By varying R, the frequency of the clock can be varied. By changing C, the range of the clock is changed.

Since the output of the unijunction at $B_2$ is a negative pulse having a poor response time, a tunnel diode is used to threshold-detect this response and apply a step voltage to a transistor switch (Q5). Figures 8 and 9 show the characteristics of the tunnel diode (TD) seen at node A.

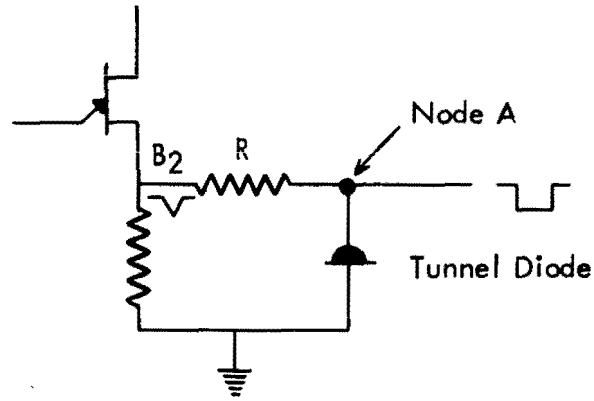



Figure 8-Tunnel Diode and Unijunction Circuit Configuration

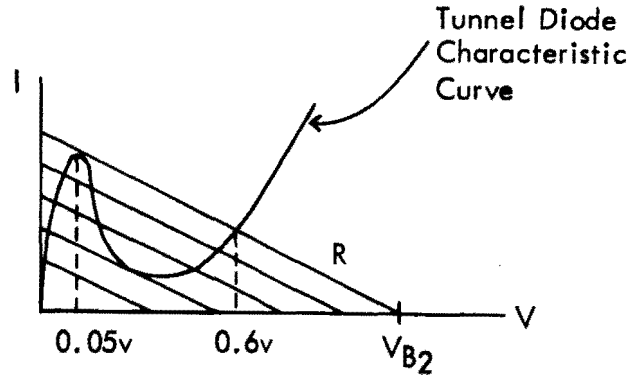


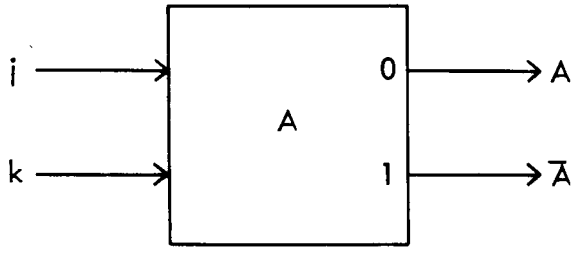

Figure 9-Tunnel Diode and Family of Load Lines Corresponding to a Changing Source Voltage

When the unijunction fires, the output at $B_2$ appears to the tunnel diode as a changing negative voltage source through R. The voltage across the diode correspondly varies from 0 to 0.05 volts, where the TD then exhibits its negatives resistance region and the diode switches along the load line, to about -0.6 volts. By applying this diode

voltage directly to a common emitter transistor ($Q_5$), the transistor will switch with a risetime of less than 0.2 $\mu$sec for any slow risetime presented at $V_{B_2}$. The output of $Q_5$ then is the clock pulse for the unit.

## BISTABLE MULTIVIBRATOR (FLIP-FLOP) CIRCUIT

The flip-flop circuit (Figure 10) is a JK Eccles-Jordan binary circuit. The reset (j) and set (k) inputs are ac coupled. By common connection of both the reset and set inputs, the circuit becomes a binary counter. A positive step voltage on the inputs constitute true inputs. The logical function performed by this circuit is shown below:




$$A(\tau) = \bar{k}A + j\bar{A}$$

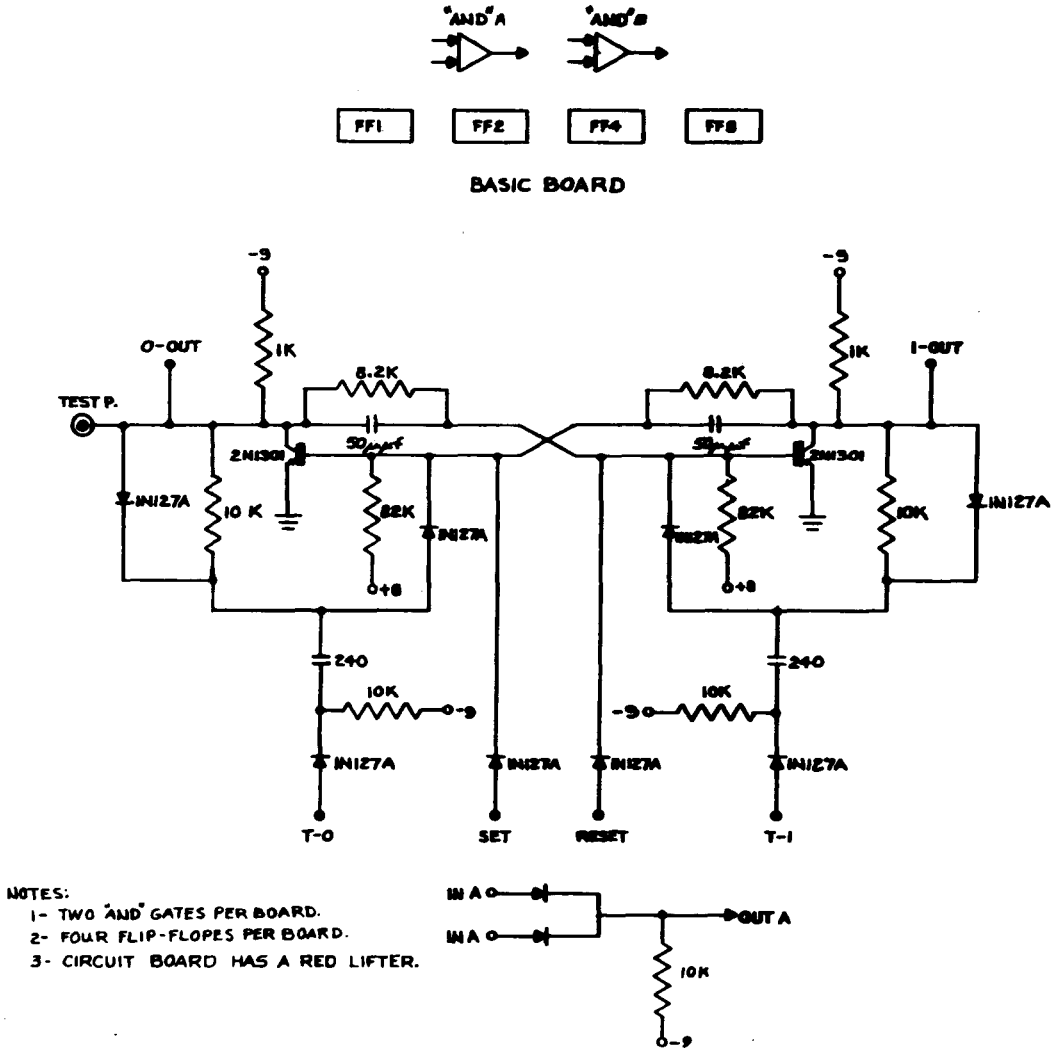
$$\bar{A}(\tau) = kA + \bar{j}\bar{A}$$

A set input and a reset input are included in the circuit. To employ these inputs a differentiated step voltage is applied.

Four flip-flop circuits and two passive AND gates are on each flip-flop board. The AND gates may be used to implement the four flip-flops as a decimal counter.

## MATRIX CIRCUIT

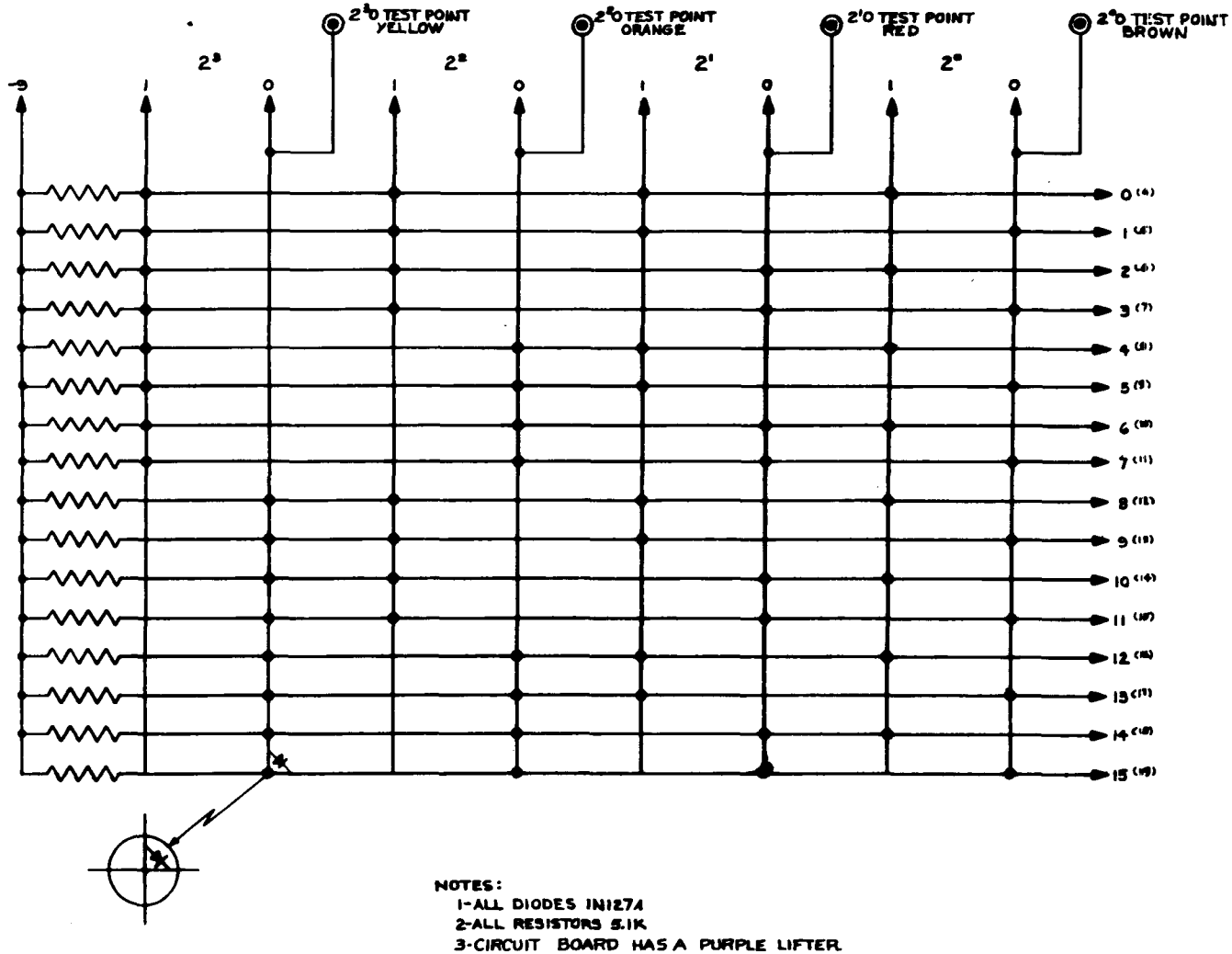
The diode matrix board (Figure 11) contains a binary to unitary switching AND matrix having as its inputs both states of a 4-bit binary counter and as it outputs 16 separate lines, each sequentially providing an output as the input binary counter monatonically increases through successive 16 counts.




PIN CONNECTIONS

| FRONT | | BACK | |
|---|---|---|---|
| GND | 1 | A | GND |
| +8 | 2 | B | +8 |
| -9 | 3 | C | -9 |
| T1-8 | 4 | D | T1-8 |
| T1-2 | 5 | E | OUT 1-4 |
| T1-1 | 6 | F | OUT AND A |
| OUT 1-2 | 7 | H | OUT 1-8 |
| OUT 1-1 | 8 | J | RESET-4 |
| RESET-1 | 9 | K | AND A |
| RESET-2 | 10 | L | AND A |
| SET-4 | 11 | M | RESET 8 |
| SET-8 | 12 | N | AND B |
| SET-2 | 13 | P | AND B |
| OUT 0-1 | 14 | R | SET 4 |
| OUT 0-2 | 15 | S | |
| OUT 0-3 | 16 | T | |
| T0-1 | 17 | U | OUT AND B |
| T0-2 | 18 | V | OUT-0-4 |
| T0-3 | 19 | W | T0-4 |
| -9 | 20 | X | -9 |
| +8 | 21 | Y | +8 |
| GND | 22 | Z | GND |

Figure 10-Flip-Flop Circuit




PIN CONNECTIONS

| BACK | | FRONT | |
|---|---|---|---|
| | A | 1 | -9 |
| | B | 2 | |
| | C | 3 | |
| | D | 4 | 0 |
| | E | 5 | 1 |
| $2^{-1}$ | F | 6 | 2 |
| $2^{-0}$ | H | 7 | 3 |
| | J | 8 | 4 |
| $2^{-1}$ | K | 9 | 5 |
| $2^{-0}$ | L | 10 | 6 |
| | M | 11 | 7 |
| | N | 12 | 8 |
| $2^{-1}$ | P | 13 | 9 |
| $2^{-0}$ | R | 14 | 10 |
| | S | 15 | 11 |
| $2^{-1}$ | T | 16 | 12 |
| $2^{-0}$ | U | 17 | 13 |
| | V | 18 | 14 |
| | W | 19 | 15 |
| | X | 20 | |
| | Y | 21 | |
| GND | Z | GND | |

OUTPUTS

OUTPUT

NOTES:
1-ALL DIODES IN1274
2-ALL RESISTORS 5.1K
3-CIRCUIT BOARD HAS A PURPLE LIFTER

Figure 11-Diode Matrix Board

## RUNDOWN CIRCUIT

The rundown circuit is a circuit which, when used with a flip-flop as shown below, constitutes a wide-range, continuously variable, high-duty cycle monostable multivibrator.

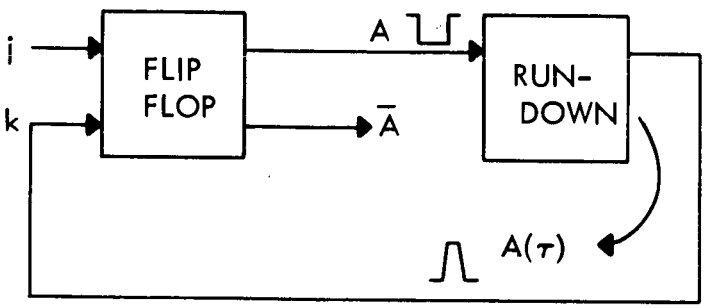



Figure 12 shows the timing relationship of the rundown and flip-flop

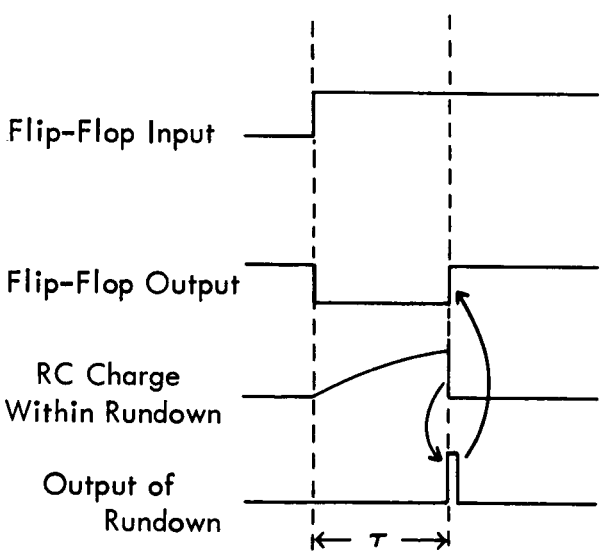



Figure 12–Rundown and Flip-Flop Operating Together as Monostable Multivibrator

When the input to the rundown circuit steps negatively from ground to -9v, $Q_1$ saturates and C begins to charge toward ground through the 2.4k resistor and the external front panel potentiometer. When the potential on C reaches the threshold* of the unijunction, it will break into conduction and discharge C to nearly -9v where the unijunction then presents an open circuit to C. The result of the fast discharge of C through the unijunction $Q_3$ is a negative pulse at $B_2$ of $Q_3$, which is coupled to $Q_4$. This input to $Q_4$ provides at its output a positive pulse which, as shown in Figure 12, is coupled back to the flip-flop, returning the flip-flop to its original state. This returns the input to the rundown to ground, and turns on $Q_2$, a clamping transistor, which clamps C to -9v until a new input arrives at $Q_1$. The delay time ($\tau$) of the circuit is a function of the setting of the front panel potentiometer and the choice of C. There are five rundown circuits on each board. (See Figure 13).

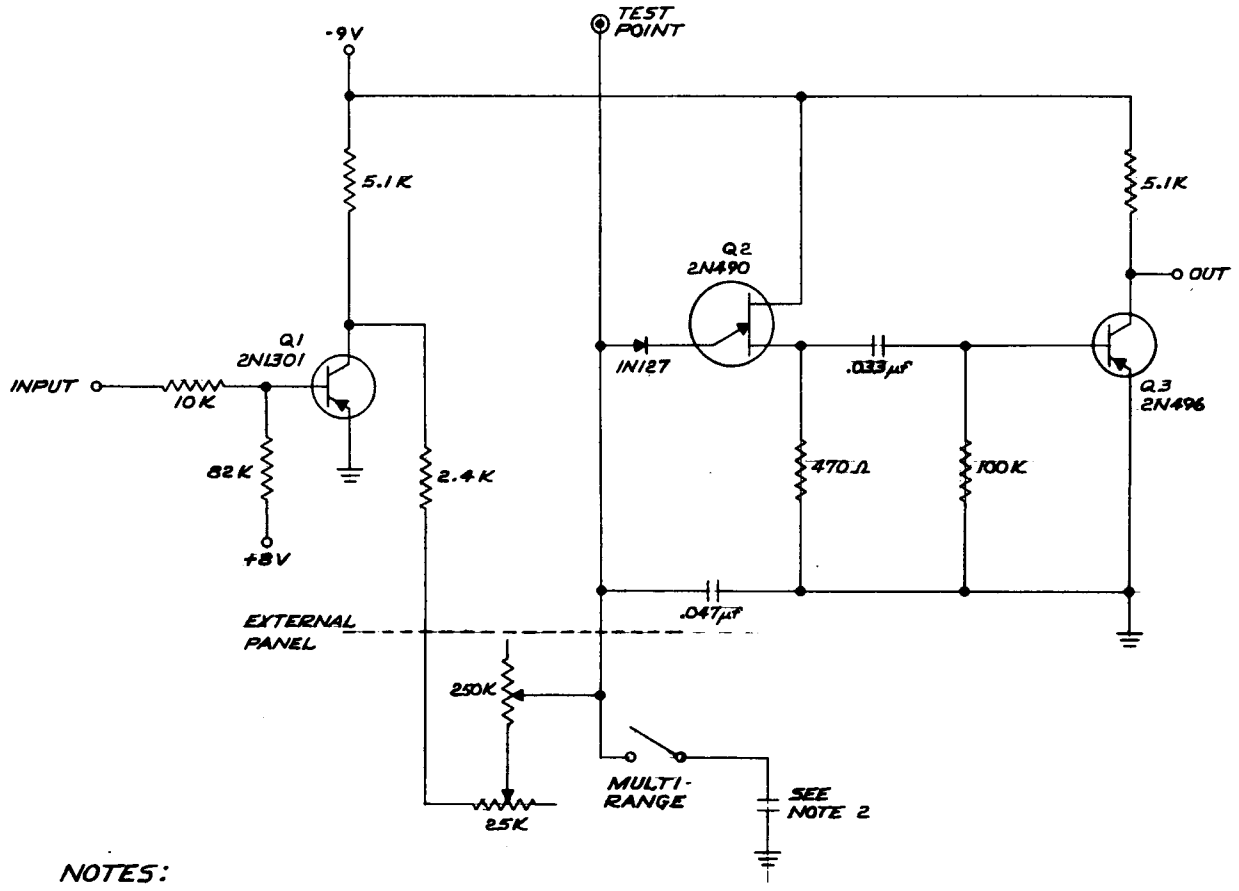
## ENVELOPE MULTIPLEXING AND OUTPUT BUFFERING CIRCUITS

The inputs to these circuits are the digital gating pulses for each channel burst time as generated by the individual flip-flop and rundown combination for each channel. The envelope circuit is in essence a 16-input diode-coupled transistor logic circuit (see Figure 14). The output of the circuit is then the equivalent ENVELOPE OUTPUT. This output is applied to an inverter to provide the COMP. ENV. OUTPUT. Channel No. 16 input is brought into two cascaded-emitter followers whose output then constitutes BURST NO. 16 SYNC OUTPUT. Likewise, Channel No. 1 is buffered and brought out as BURST NO. 1 SYNC OUTPUT. All outputs are buffered by emitter followers and are protected by 100-ohm series resistors.

## OSCILLATOR, AVC, AND OSCILLATOR GATE CIRCUITS

The oscillator gate board contains three principal circuits: a variable frequency oscillator, an automatic voltage controlled (AVC) circuit, and an oscillator gate circuit (Figure 15). Each circuit will be discussed separately.

*The threshold voltage of a unijunction is defined as $\eta V_{B_1B_2}$ where $\eta$ is the intrinsic stand-off ration ($\eta = 0.6$) and $V_{B_1B_2}$ is the voltage impressed across the unijunction.




PIN CONNECTIONS

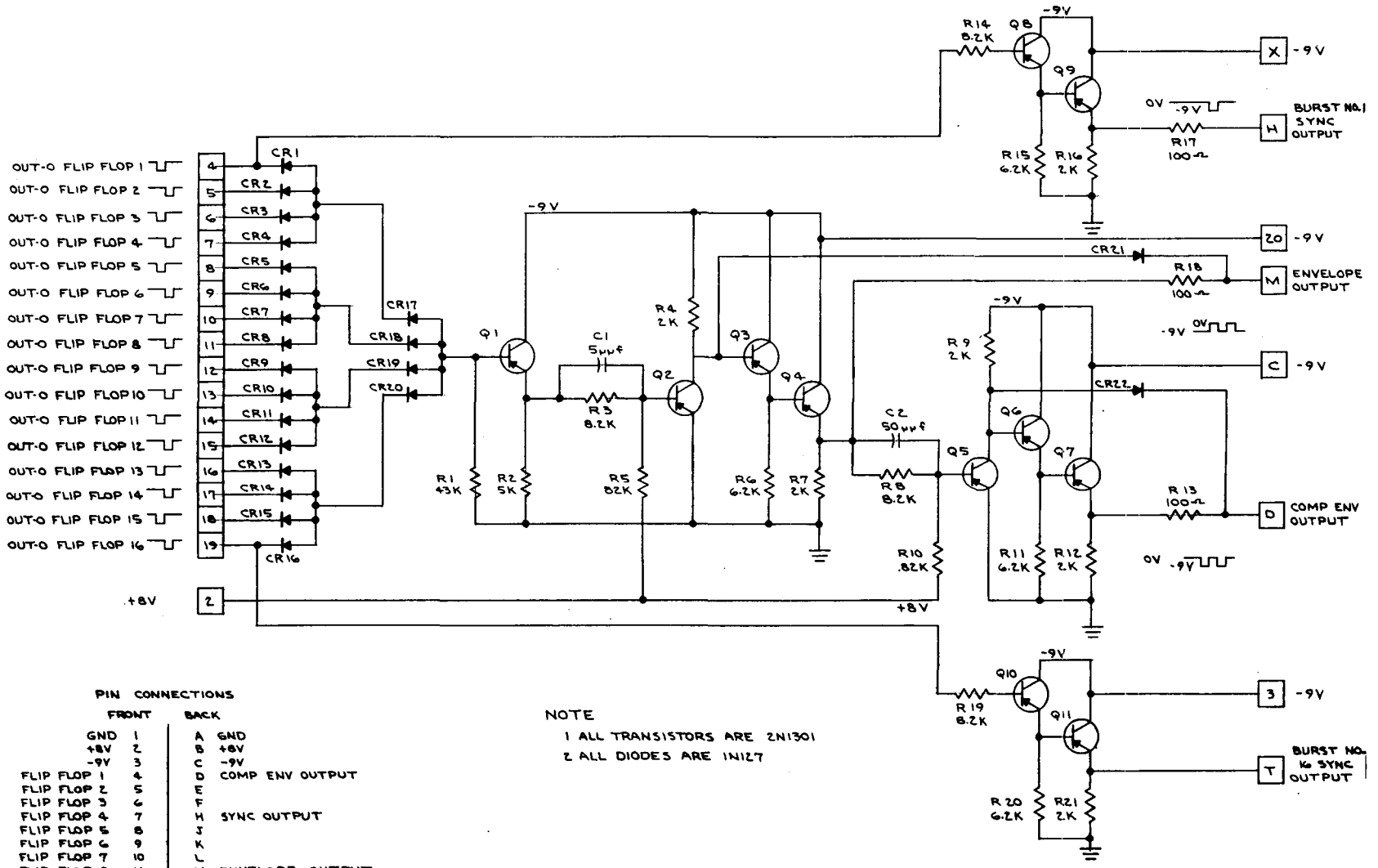
| | FRONT | BACK | |
|---|---|---|---|
| GND | 1 | A | GND |
| +8V | 2 | B | +8V |
| -9V | 3 | C | -9V |
| IN-1 | 4 | D | OUT-1 |
| B-1 (POT) | 5 | E | |
| A-1 (POT) | 6 | F | |
| IN-2 | 7 | H | OUT-2 |
| B-2 (POT) | 8 | J | |
| A-2 (POT) | 9 | K | |
| IN-3 | 10 | L | OUT-3 |
| B-3 (POT) | 11 | M | |
| A-3 (POT) | 12 | N | |
| | 13 | P | |
| IN-4 | 14 | R | OUT-4 |
| B-4 (POT) | 15 | S | |
| A-4 (POT) | 16 | T | |
| IN-5 | 17 | U | OUT-5 |
| B-5 (POT) | 18 | V | |
| A-5 (POT) | 19 | W | |
| -9V | 20 | X | -9V |
| +8V | 21 | Y | +8V |
| GND | 22 | Z | GND |

NOTES:

1. FIVE CIRCUITS PER BOARD.
2. DETERMINES RANGE.

| MULTI-RANGE | POT. | CAP. |
|---|---|---|
| .22MS - 19MS | 250K | .1μf |
| 7.8MS - 700MS | 250K | 4.7μf |

Figure 13-Run-Down Circuit




PIN CONNECTIONS

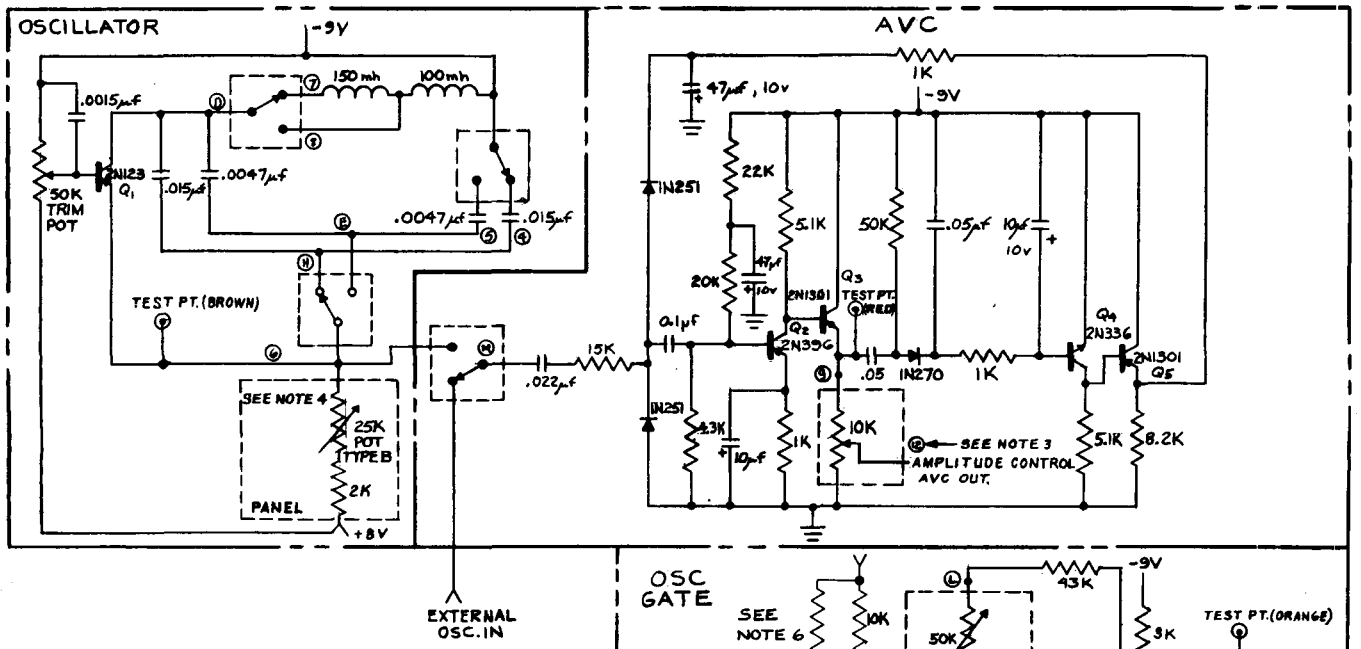
| FRONT | | BACK | |
|---|---|---|---|
| GND | 1 | A | GND |
| +8V | 2 | B | +8V |
| -9V | 3 | C | -9V |
| FLIP FLOP 1 | 4 | D | COMP ENV OUTPUT |
| FLIP FLOP 2 | 5 | E | |
| FLIP FLOP 3 | 6 | F | |
| FLIP FLOP 4 | 7 | H | SYNC OUTPUT |
| FLIP FLOP 5 | 8 | J | |
| FLIP FLOP 6 | 9 | K | |
| FLIP FLOP 7 | 10 | L | |
| FLIP FLOP 8 | 11 | M | ENVELOPE OUTPUT |
| FLIP FLOP 9 | 12 | N | |
| FLIP FLOP 10 | 13 | P | |
| FLIP FLOP 11 | 14 | R | |
| FLIP FLOP 12 | 15 | S | |
| FLIP FLOP 13 | 16 | T | #16 SYNC OUTPUT |
| FLIP FLOP 14 | 17 | U | |
| FLIP FLOP 15 | 18 | V | |
| FLIP FLOP 16 | 19 | W | |
| -9V | 20 | X | -9V |
| +8V | 21 | Y | +8V |
| GND | 22 | Z | GND |

NOTE

1 ALL TRANSISTORS ARE 2N1301

2 ALL DIODES ARE 1N127

Figure 14-Envelope Multiplexing and Output Buffering Circuits




NOTES:

1- EXTERNAL OUTLETS ARE BOXED WITH DOTTED LINES.

2- PIN CONNECTIONS ARE CIRCLED.

3- WHEN TRIM-POT IS MOUNTED ON BOARD AVC AMPLITUDE CONTROLLED OUTPUT IS PIN 12. WHEN EXTERNAL POT IS EMPLOYED AVC AMPLITUDE CONTROLLED OUTPUT IS CENTER TAP OF EXTERNAL 10K POT.

4- A 1K POT MAY BE ADDED IN SERIES WITH THE 25K POT TO PROVIDE FINE FREQUENCY ADJUSTMENT.

5- Q6: $10 < \beta < 30$

6- RESISTOR ADDED IN PARALLEL TO ATTENUATE OUTPUT SIGNAL SUCH THAT ALL OSCILLATOR GATES HAVE APPROX. SAME AMPLITUDE OUT.

(SEE NOTES 1 & 2)
PIN CONNECTIONS

| | FRONT | BACK |
|---|---|---|
| | GND 1 | A GND |
| | +8 2 | B +8 |
| | -9 3 | C -9 |
| | 4 | D |
| | 5 | E |
| | 6 | F |
| | 7 | H |
| | 8 | J |
| | 9 | K |
| | 10 | L |
| | 11 | M EXTERNAL OSC IN |
| SEE NOTE 3 | 12 | N |
| | 13 | P |
| | 14 | R |
| | 15 | S |
| | 16 | T |
| | 17 | U GATE INPUT |
| | 18 | V |
| CW IN | 19 | W |
| | -9 20 | X -9 |
| | +8 21 | Y +8 |
| | GND 22 | Z GND |

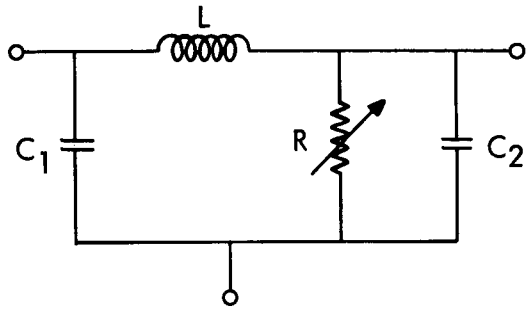
Figure 15-Oscillator, AVC, and Oscillator Gate Circuits

## The Oscillator Circuit

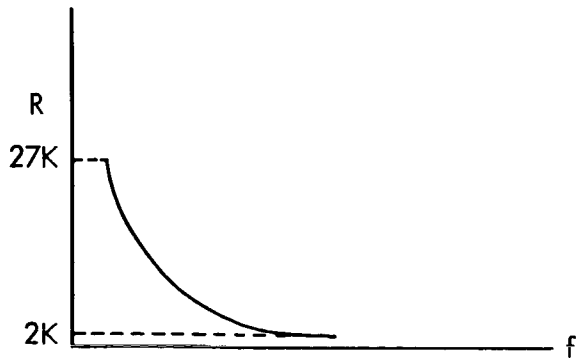
The first circuit is a continuously variable sinusoidal oscillator of the Colpitts type which, through external switch control, has the two frequency ranges of 4.5 to 15 kc and 15 to 45 kc. Each range is obtained by switching a separate LC network into the oscillator. The approximate center frequency of the oscillator for each tank is given by:

$$f = \frac{1}{2\pi\sqrt{LC_T}} \quad \text{where} \quad C_T = \frac{C_1 C_2}{C_1 + C_2}$$

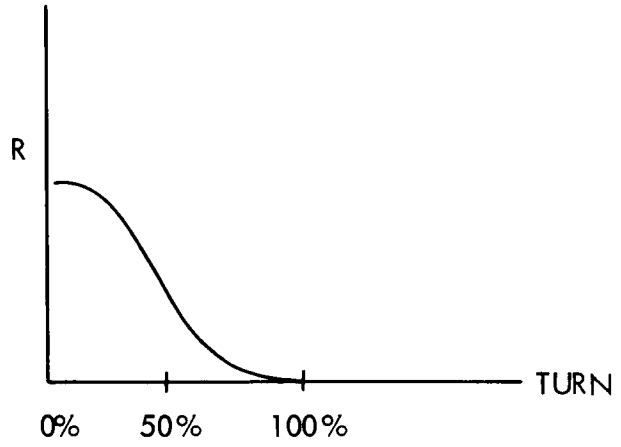
By adding a variable resistance (R) between the emitter and ac ground, the equivalent ac tank circuit appears as shown below:




By varying R, the equivalent reactance provided by $C_2$ is altered and the center frequency of the network is changed. In the Mode II simulator, R is the sum of a 25-kilo-ohm potentiometer and a fixed resistor of 2 kilo-ohms. The oscillator frequency variation with R is shown below.




Because the frequency varies nearly hyperbolically with R, a type-B logarithmic potentiometer having a curve as shown below is employed in such a manner to provide an approximately linear variation of frequency with the turning of the frequency control.




Automatic Voltage Controlled (AVC) Circuit

The function of the second circuit is to automatically voltage-control either the internally generated frequency signal or an externally applied frequency signal so that the input to the oscillator gate will always be a constant-level signal.

The principle employed is in essence that of controlling the gain of a Class A amplifier through interrogation of the output signal level as shown in Figure 16.

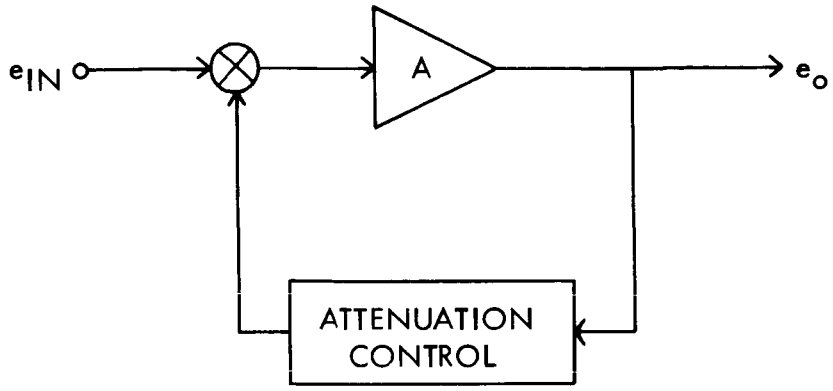



Figure 16-AVC Loop

This is done by equivalently varying the shunt resistance of an L pad preceding the input to the Class A amplifier with a dc current that is a function of the output signal level of the amplifier. The L pad consists of a series resistor and an equivalent ac shunt resistance of two diodes which are dc biased in a region where, for changes in the dc current through the diode, the small signal diode resistance can be varied. Figures 17, 18, and 19 show the complete L pad, the ac equivalent, and the equivalent configuration seen by the input signal.

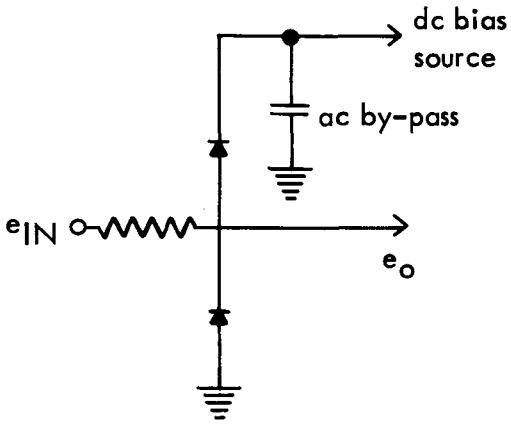



Figure 17-Complete L Pad

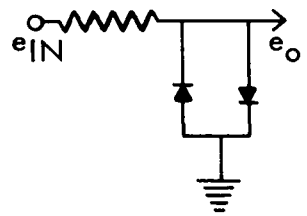



Figure 18– AC Equivalent L Pad

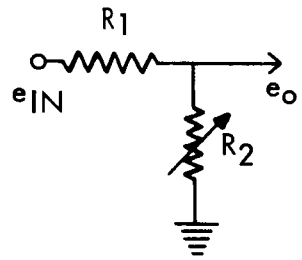



Figure 19–Equivalent L Pad Seen by Input Signal

The variation of the small signal resistance with the dc bias current can be seen by reviewing the characteristic curve of the diode as shown in Figure 20, where V is chosen to be the ordinate and I the abscissa.

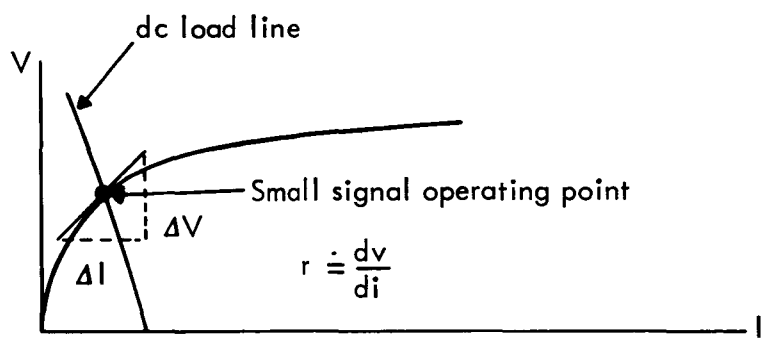



Figure 20–Diode Characteristic Curve

The resistance exhibited by the diode is the tangent to the curve at the intersection of the dc bias current and the characteristic curve. For very small time-varying signals, the ac resistance is appreciably linear for a fixed dc operating point. By changing the quiescent operating point, the ac resistance is changed as shown.

The small variation from linearity is improved by using two diodes in parallel, one in an ac forward biased direction and one in a negatively biased direction; the ac resistance is then the parallel resistance of the two small signal resistances given by the two operating points of both diodes.

The dc bias current to the L pad is supplied by detecting and low pass-filtering the output of the Class A amplifier ($Q_2$) amplifying this voltage, and then providing a current as a function of this voltage.

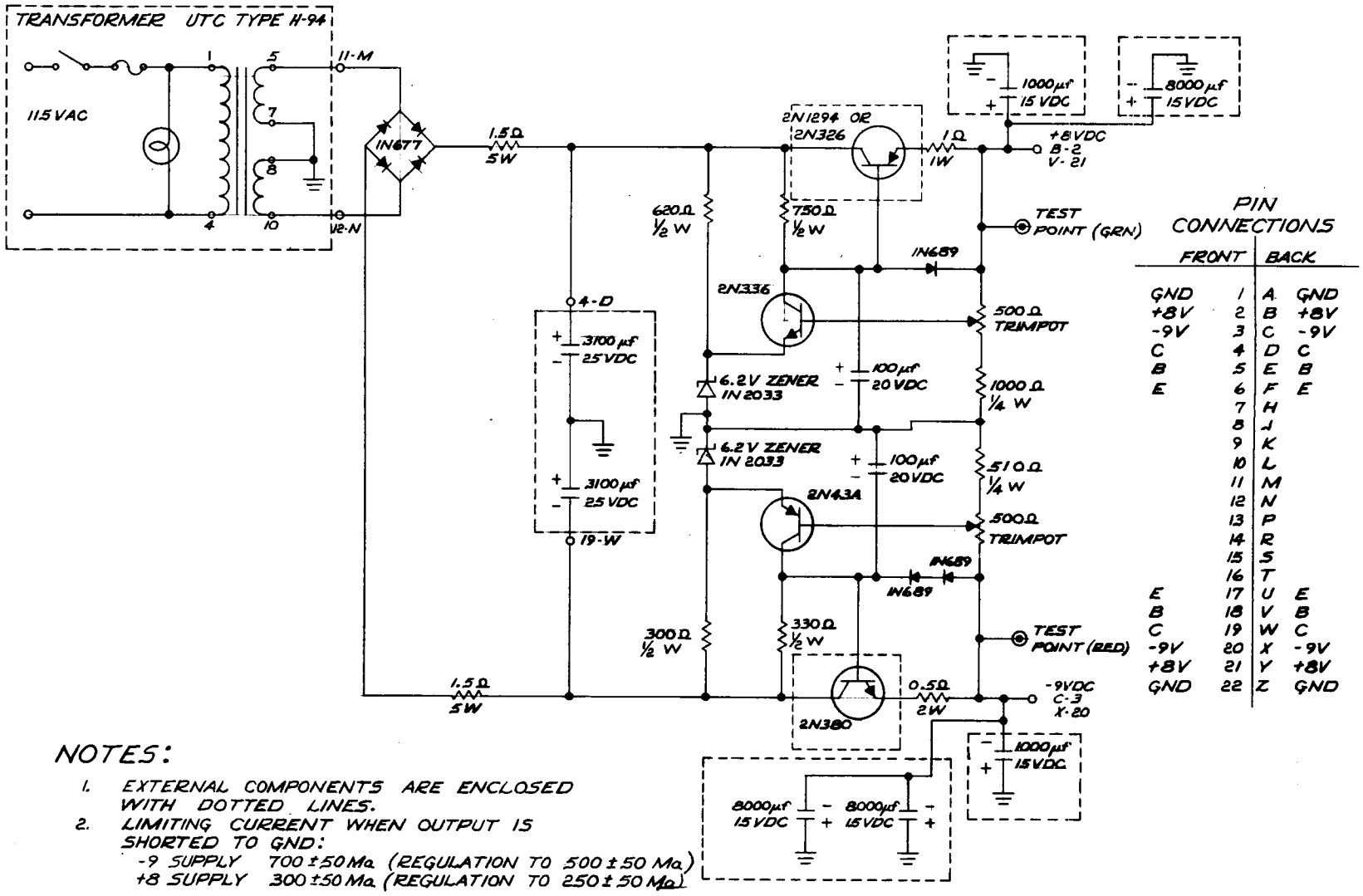
## Oscillator Gate

The oscillator gate (Figure 15) digitally controls passage or infinite attention of a time-varying signal such that the signal dc level during the time of infinite attention is the dc center of the peak-to-peak levels of the signal during passage. This is done by biasing a Class A amplifier ($Q_6$) such that the output quiescent operating level is ground. Application of a symmetrical input signal will then vary about ground at the output of the amplifier. A saturating transistor ($Q_7$) is digitally controlled (at pin U) to turn this transistor full-on or full-off which infinitely attenuates the output of the $Q_6$ or fully passes the output of $Q_6$, respectively. The 2N508 was chosen for $Q_7$ because it has an extremely low saturating voltage.

The dc level of the output of $Q_6$ is externally controlled by varying a 50-k potentiometer in the bias network as shown in Figure 15. For the particular application of this circuit in the Mode II simulator, the 10-k input resistance as seen at pin 19 was trimmed such that a group of 16 such oscillator gates would each provide equal maximum output levels.

## POWER SUPPLY

The power supply consists of two voltage regulators, one for +8vdc and one for -9vdc (Figures 21 and 22). The +8vdc power supply will deliver 300 ma and the -9vdc supply will deliver 400 ma. Both regulators are of the series type in which regulation is made through control of a series power transistor by referencing the output of each supply through a divider network to a constant voltage source provided by a Zener diode. Correction is made by varying the gain of the series power transistor through an amplifying stage with the infintesimal voltage differences




NOTES:

1. EXTERNAL COMPONENTS ARE ENCLOSED WITH DOTTED LINES.
2. LIMITING CURRENT WHEN OUTPUT IS SHORTED TO GND:
   -9 SUPPLY 700 ± 50 Ma (REGULATION TO 500 ± 50 Ma)
   +8 SUPPLY 300 ± 50 Ma (REGULATION TO 250 ± 50 Ma)

Figure 21-Power Supply, PFM Simulator (Mode II)

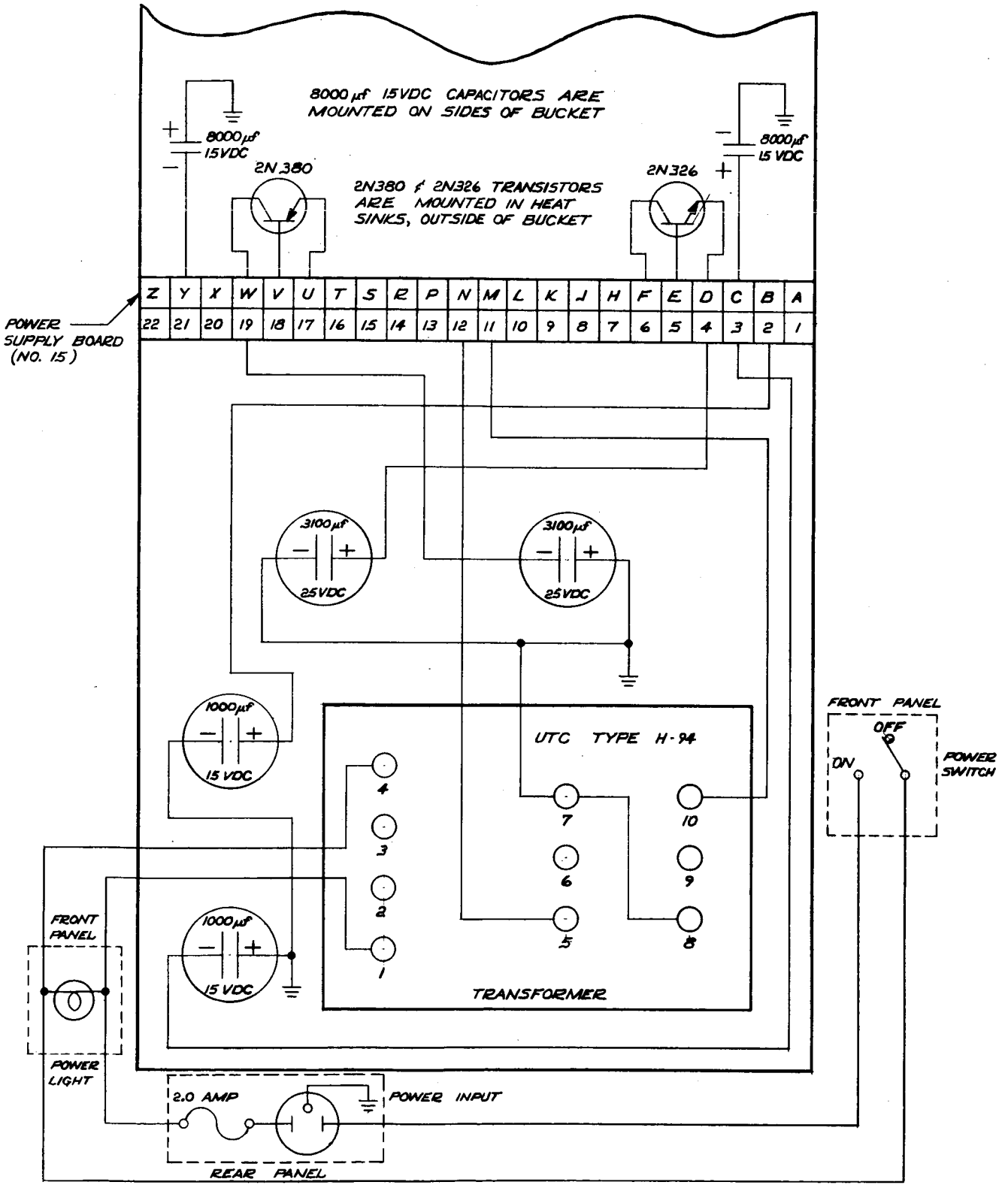



Figure 22-Power Supply Parts Layout (Bottom View)

seen between the Zener diode and the divider network. Both regulators share the same transformer input through a full wave rectifier; each supply is filtered separately.

Each supply is protected against short circuits or excessive loads through current limiting. The supply voltages may be finely varied by adjusting the trimpots incorporated in the divider network of each regulator. The power transistors are mounted on heat sinks external to the module board because of the power requirements of the simulator.

# VI. WIRING AND BOARD LOCATION

Figure 23 shows the board location of the PFM simulator. Figures 24 and 25 are the wiring diagrams for the unit.

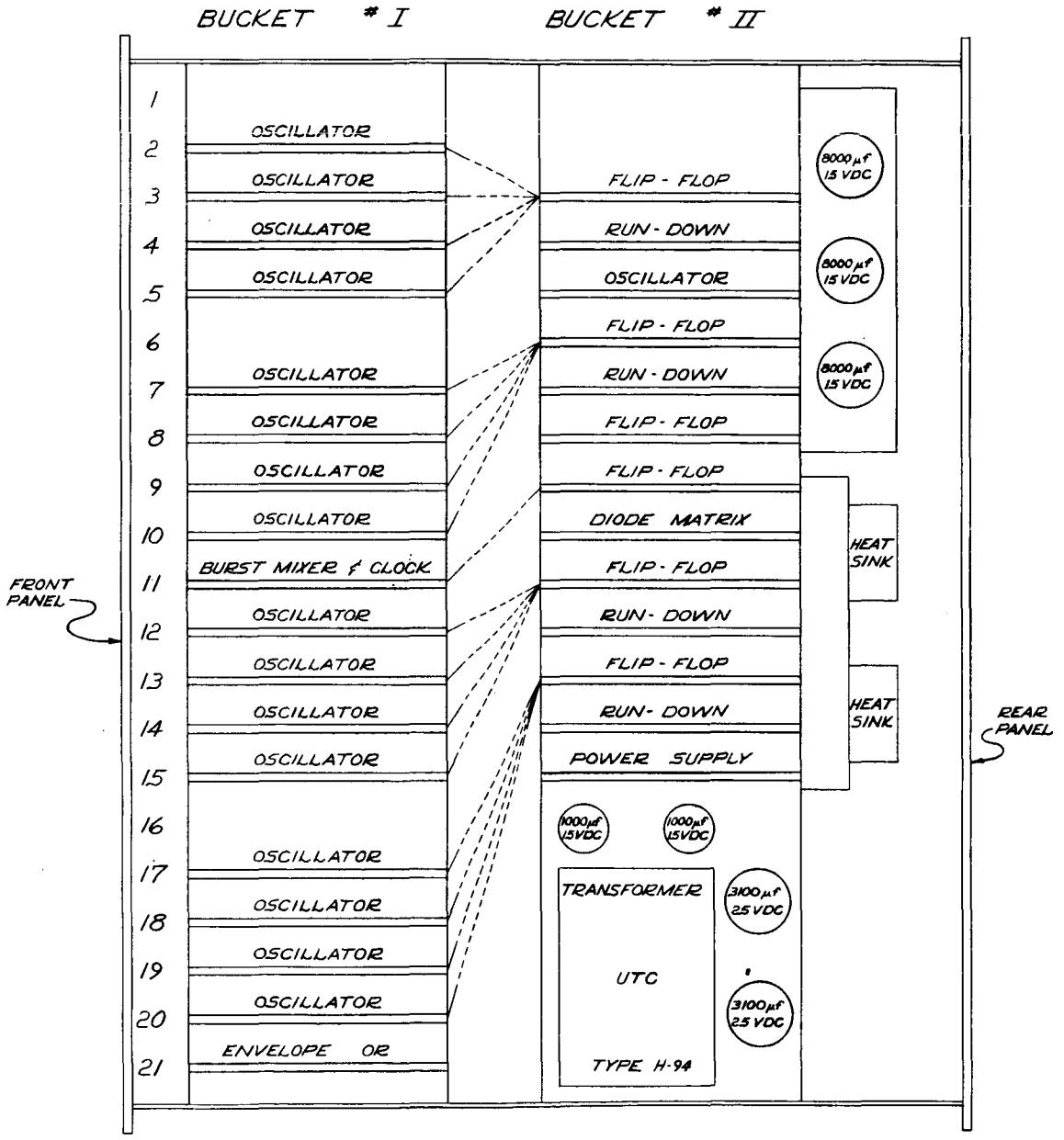



Figure 23-Board Location (Top View)

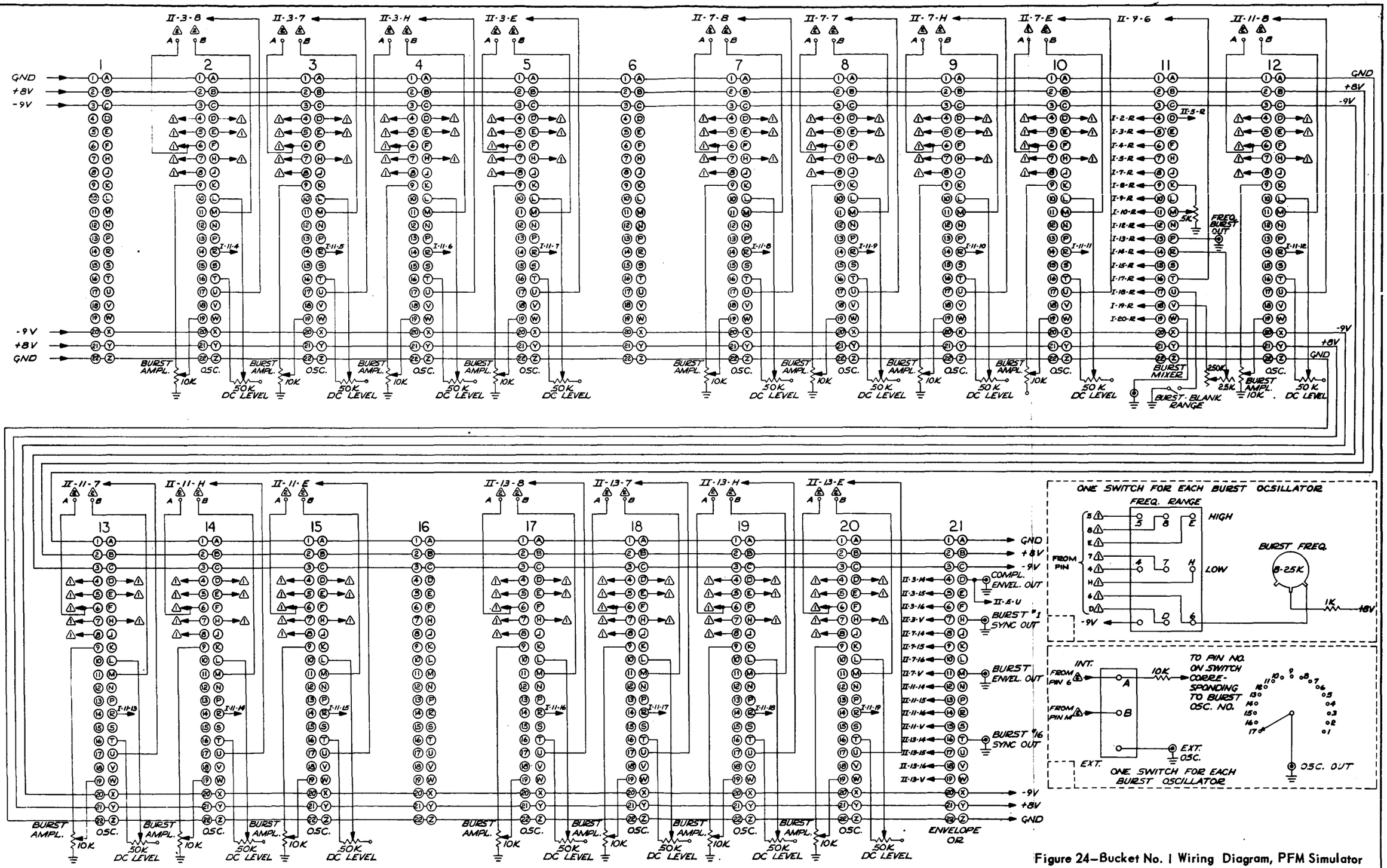
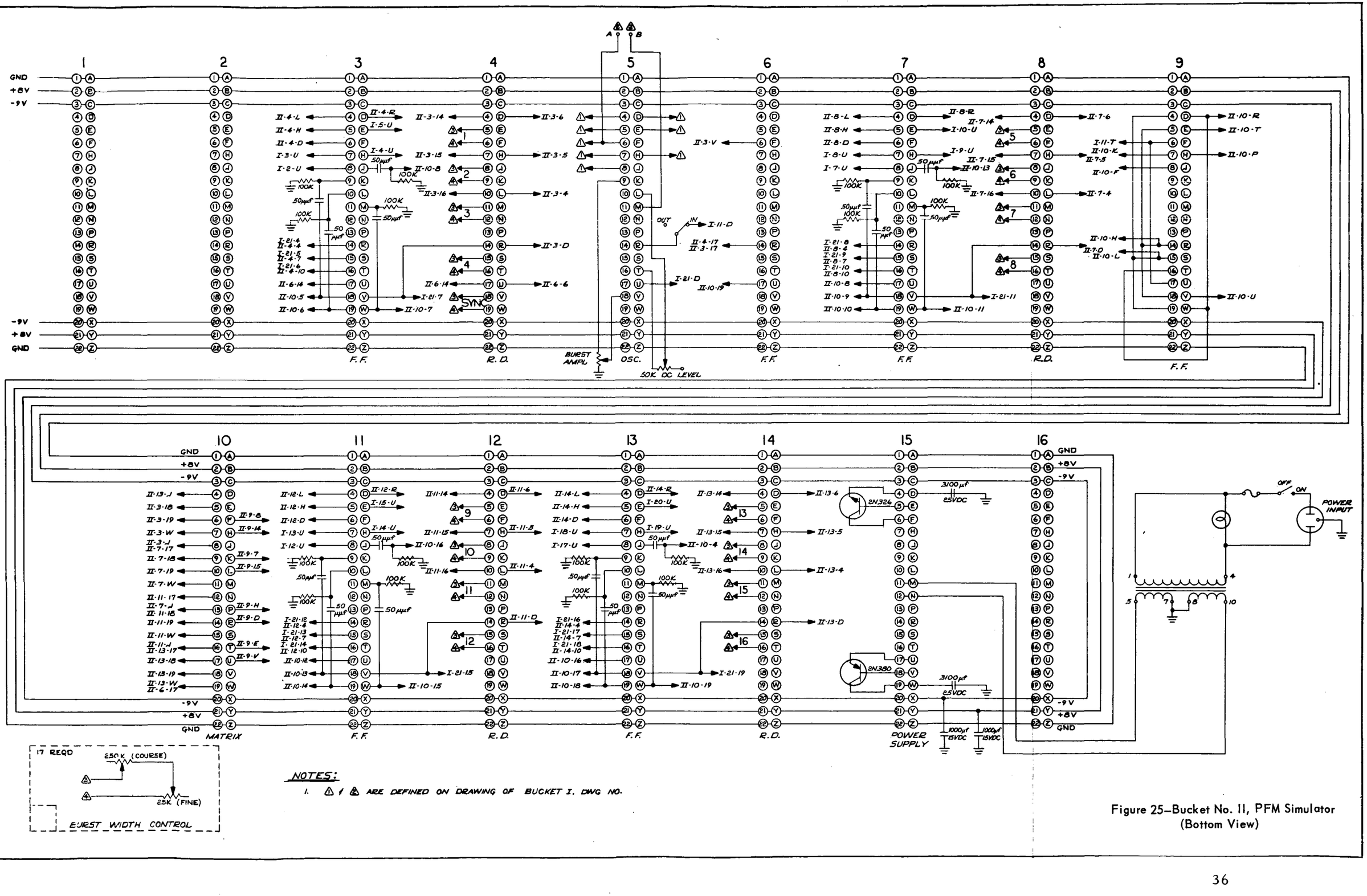



Figure 24—Bucket No. 1 Wiring Diagram, PFM Simulator (Bottom View)




NOTES:

1. ⚠1 & ⚠2 ARE DEFINED ON DRAWING OF BUCKET I, DWG NO.

Figure 25–Bucket No. 11, PFM Simulator (Bottom View)