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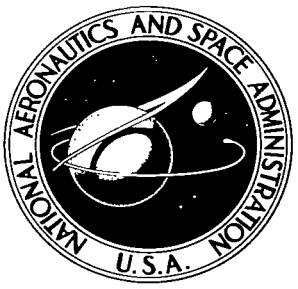

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WIDE RANGE PHASE DETECTOR

by George B. Robinson

Goddard Space Flight Center
Greenbelt, Maryland

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SUMMARY

A 4-diode bridge-type phase detector of constant cosine response from 20 cps to 100 kc, was developed as a part of an experimental phase-lock filter intended for operation in that range. A 6-transistor circuit drives the diode bridge. A wide-band resistive-T adder network, rather than the usual center-tapped transformer, supplies signal and reference inputs to the bridge. The output is balanced to ground; the internal resistance of the output circuit is 600,000 ohms. Total power consumption is 135 mw at 50 v. An analysis is made which shows that the cosine response at the output terminals to be: $E_{OUT} = -1.28\ E_s(\cos n\alpha)/\pi n$, for n odd; $E_{OUT} = 0$, for n even, where E_s = RMS signal input, α = phase angle of the input signal relative to the input reference voltage, and n = integer ratio of signal frequency to reference frequency. Typical maximum cosine response is 450 mv at 1 v signal level and 5 v reference level. The measured maximum translation between any two cosine curves does not exceed 20 mv throughout the operating range of 30 cps to 100 kc. The measured cosine curve translation at 50 kc does not exceed 20 mv in the temperature range of 0° to 50°C.

CONTENTS

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INTRODUCTION

The design requirements of a low frequency phase-lock filter system recently investigated required the operation of the phase detector over a wide frequency range. The following characteristics were considered paramount in the design of the phase detector:

1. Cosine response independent of frequency throughout a 20 cps to 100 kc range.
2. Reference and signal balance constant throughout the above frequency range.
3. Signal-reference balance stable in the 0 to 50°C range.
4. Cosine response independent of temperature in the above temperature range.
5. Freedom from spurious outputs.

This paper describes a four-diode phase detector of the double-balanced, bridge-circuit configuration whose salient feature is a push-pull reference source which does not use a transformer. The circuit design is described; the static cosine response is derived in a general form which includes the response when the signal frequency is an odd integer multiple of the reference frequency. The following characteristics are presented as measured data: cosine response in the 20 cps to 100 kc range; spurious response; reference and signal balance; temperature effects on the cosine response; effects of temperature on signal and reference balance.

CIRCUIT DESIGN

The circuit of the wide-range phase detector shown in Figure 1 is divided operationally into three sections: push-pull reference amplifier; signal amplifier; diode complex.

Reference Amplifier

The function of the reference amplifier is to supply a push-pull signal to the diode complex. The principle design criterion is equality of magnitude and constant 180-degree phase opposition of the individual outputs over the operating frequency range. This characteristic is required so that the phase detector will have a minimum or zero output when the reference is applied singly to the diode complex.

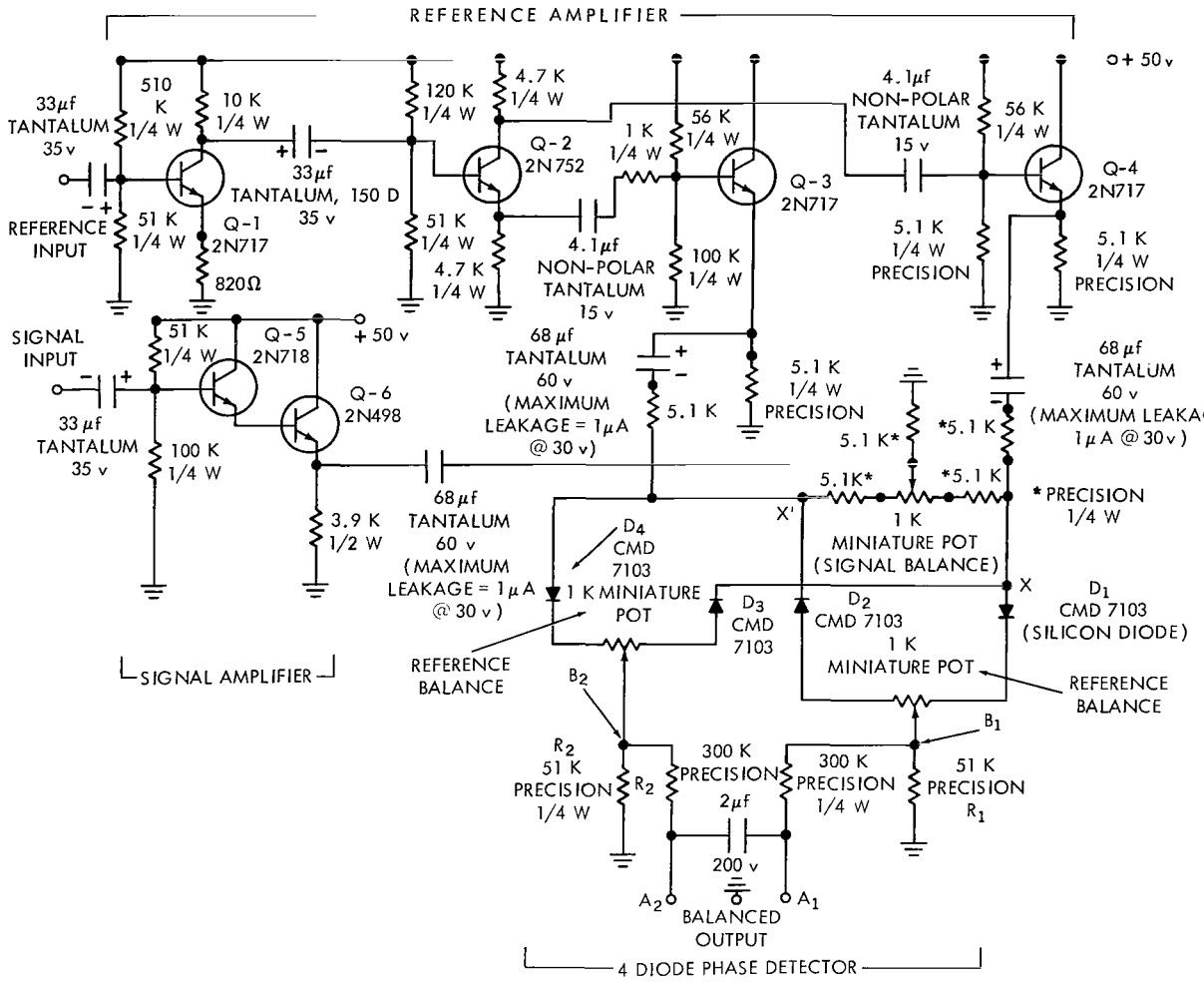


Figure 1—Phase detector circuit diagram.

The reference amplifier consists of a degenerative voltage amplifier stage with transistor Q-1 capacitively coupled to a paraphase transistor Q-2 whose collector is again capacitively coupled to the base of an emitter-follower Q-4; the emitter of Q-2 is coupled to the base of the emitter-follower Q-3. Wide frequency range is achieved by the use of tantalum capacitors and low over-all gain. The paraphase amplifier (Q-2) is the most critical stage in that the equality in magnitude of the individual push-pull output voltages and phase opposition are determined principally by this transistor. Collector impedance is considerably higher than the emitter impedance in this type of circuit; thus loading by the emitter follower stages tends to cause amplitude and phase differences. Phase error was reduced to no greater than 2 degrees by the insertion of a 1000-ohm resistor in the emitter output lead. Compensation was not complete in that a small difference in amplitude remained. Gain and phase characteristics of the reference amplifier are shown in Figure 2. Other pertinent measured data is shown in summary form in Table 1.

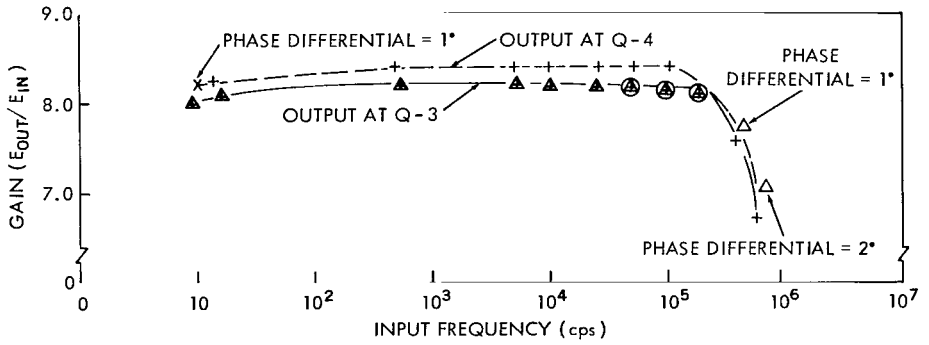


Figure 2—Reference channels—gain vs frequency.

Table 1

Reference-Signal Amplifier Chart.

Transistor and Function	Collector Current (Ma)	Maximum Undistorted Output Voltage (in circuit)	Magnitude of Impedance
Reference			Input:
Q-1, 2N717 Voltage Amplifier	3.7	22 v, p-p	7 k-ohms at 1 kc 2 k-ohms at 100 kc
Reference			
Q-2, 2N752 Phase-splitter	2.7	15 p-p { collector or emitter	-
Reference			Output:
Q-3, 2N717 Emitter-follower	5.5	30 p-p	53.6 ohms at 1 kc, 10 v, p-p
Reference			Output:
Q-4, 2N717 Emitter-follower	5.5	30 p-p	102 ohms at 1 kc, 10 v, p-p
Signal			Input:
Q-5, 2N718	.4	-	32 k ohms at 1 kc 30 k ohms at 100 kc
			Output:
Q-6, 2N498	8.2	12 p-p	13.7 ohms at 1 kc 13.7 ohms at 100 kc
Darlington emitter-follower			
Total Current (Power Supply Voltage = 50 v)	26.4		

Signal Amplifier

The signal amplifier consists of transistor Q-5 direct coupled to Q-6 in a Darlington configuration. This configuration increases the input impedance at the signal amplifier terminals which would otherwise be low because of the characteristics of the 2N498 power transistor employed as the output stage. The power transistor was found necessary to minimize signal suppression resulting from negative clipping when noise was present. The gain versus frequency response of this amplifier was not plotted; however, the gain is 0.975 at 600 kc and unity at 10 cps. Data pertaining to the signal amplifier is shown in Table 1.

Diode Complex

The diode portion of the phase detector is comprised of two independent sections; diodes D-1 and D-2 with output at A_1 and diodes D-3 and D-4 with output at A_2 (Figure 1). Each section synchronously rectifies a half-wave portion of the signal. The two sections are independent in operation and produce identical outputs of opposite polarity displaced by 180 degrees. Filtering is provided by a 2 μf capacitor across terminals A-1 and A-2. The dc output at these terminals is balanced with respect to ground. The particular diode configuration used here is known as a double balanced bridge.* The type of diode chosen for this circuit is a silicon mesa type with a maximum recovery time of 4 nanosec. The measured characteristics of this particular diode will be discussed in a later section.

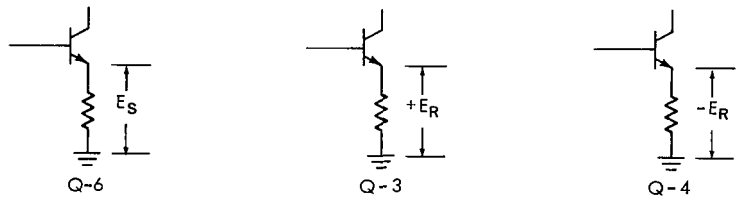
The diode complex also includes a resistive network which provides the signal-reference sum and difference to the diode pairs. This network consists of a T configuration (Figure 1) with 5100-ohm resistances as the arms. The signal is fed into the vertical arm of the 'T' from the output of transistor Q-6. A low-leakage 68-μf tantalum capacitor is used for dc isolation. This capacitor is rather critical in that the leakage must be very low. The type chosen showed a maximum leakage current of 1μamp at 30 v. The horizontal arms of the 'T' are fed through series isolating resistors (5100 ohms) from the push-pull reference outputs of Q-3 and Q-4. The isolating resistors prevent signal voltages from appearing across the emitter-follower (Q-3 and Q-4) load resistors. Low-leakage tantalum capacitors are also employed here as dc isolating elements. The network functions in the same manner as the transformer customarily used to form the signal-reference sum and difference.

CIRCUIT ANALYSIS

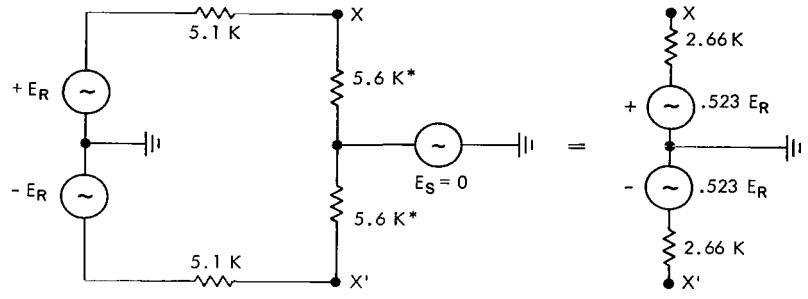
Phase Detector Equivalent Circuit

The equivalent circuit of the phase detector is shown in Figure 3d. Figures 3a, 3b, and 3c show a step by step derivation of the equivalent generator and equivalent source impedances which represent the T network and emitter-follower drivers. Figure 3a defines E_r and E_s (the reference

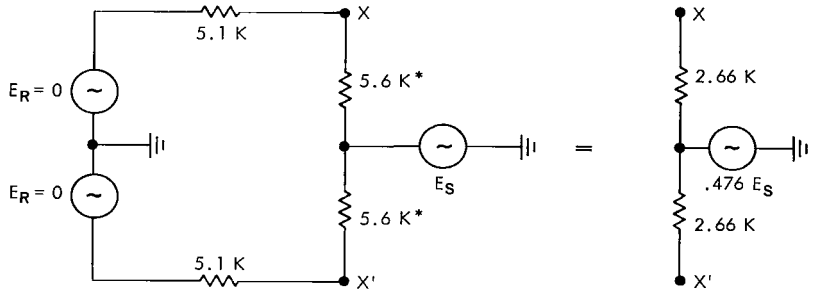
*Blickensderfer, J. A., "Diode Phase Detectors", Electronics Research Laboratory Technical Report No. 4, June 15, 1953.



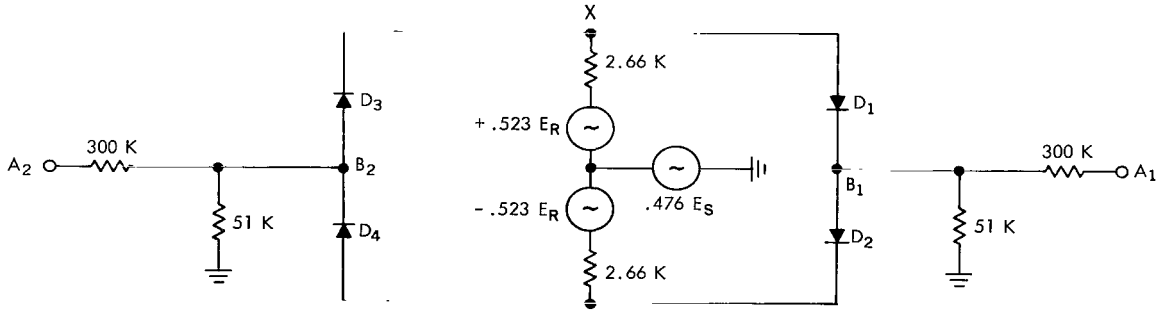
(a) Location of E_R and E_S in circuit



(b) Derivation of reference equivalent generators and source impedance



(c) Derivation of signal equivalent generator and source impedance



(d) Equivalent circuit of phase detector

* Includes balance potentiometer resistance-arm centered

Figure 3—Derivation of equivalent circuit of phase detector, 2μf filter capacitor omitted.

and signal outputs) and shows their location in the circuit diagram (Figure 1). In making the derivation shown in Figures 3b and 3c, it is first necessary to locate points X and X' in Figure 1. The open circuit voltage and source impedance at these points with the diodes disconnected are then determined by means of Thevenin's Theorem. For this derivation E_s is set equal to zero (Superposition Theorem). The final result is the diagram on the right (Figure 3b). In Figure 3c the process is repeated, but in this case E_r is set equal to zero. Thevenin's Theorem then gives the equivalent signal source shown on the right. Finally, in Figure 3d, Figures 3b and 3c are combined; the diode load and resistive filter network (without the filter capacitor) are also shown. For this derivation, the impedance of the reference and signal emitter followers, Q-3, Q-4, and Q-6, has been arbitrarily taken as zero to simplify the derivation. Actual values of these impedances taken from the chart shown in Table 1 and used in a more exact derivation show that the error in Figure 3b is about 1 percent, and in Figure 3c about .1 percent.

Phase Detector Operation with Reference Input Only

The equivalent circuit is helpful in formulating a qualitative description of the phase detector operation. First, consider operation with only the reference input with ideal diodes which are matched with respect to the following characteristics: forward and reverse resistance, and shunt capacitance. The configuration of the reference sources and diodes with respect to the ground point is that of a double bridge. Each section of the bridge will conduct during alternate half-wave portions of the reference source cycle. If E_r is positive with the diode polarity shown in Figure 3, D-1 and D-2 will conduct, but because of equal forward resistance, the instantaneous potential at B-1 will remain zero. During this portion of the cycle D-3 and D-4 are nonconducting and because of postulated equal reverse resistance the output at B-2 will also be zero. A similar argument can be made for the negative portion of the reference cycle during which time D-3—D-4 will conduct and D-1 and D-2 will be nonconducting. The conclusion is the same as formerly: B-1 and B-2 remain at zero potential. The output wave forms with reference input only are shown in Figure 4. The center trace shows the output wave forms of diodes D-1 and D-2 at point B-1, while the lower trace shows the output of diodes D-3 and D-4 at point B-2 (Figure 1). The upper trace is a 1 v signal for amplitude comparison. The output was taken after balancing inequalities in the diode characteristics by means of reference balance potentiometers (Figure 1). The function of these potentiometers will be discussed in greater detail.

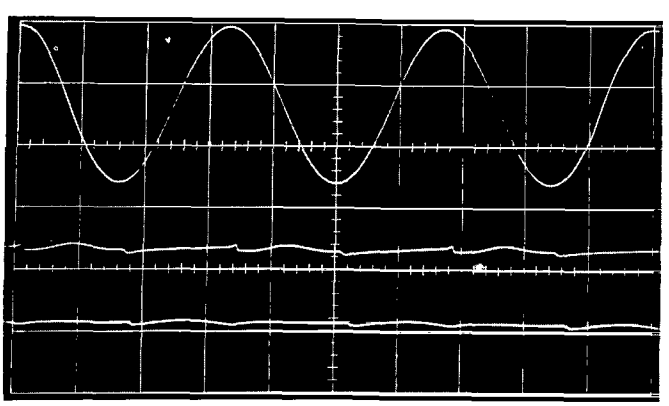


Figure 4—Phase detector reference balance: E_r = 5 v RMS; signal input = 0. Upper trace - 1 v RMS for amplitude comparison only; center trace - output at B_1, 1 v RMS = 1.8 cm. Lower trace - output at B_2, 1 v RMS = 1.8 cm.

Phase Detector Operation with Signal Input Only

Operation of the phase detector with signal input in the absence of the reference leads to

the direct transmission of the signal to the terminals, B-1 and B-2, preceding the integrator. This bi-directional conduction results from the polarity of the diodes in the circuit with respect to the signal source. An inspection of the equivalent circuit shows the positive portion of the signal would be expected to appear simultaneously at B-1 and B-2 because of the conduction of diodes D-1 and D-4. Similarly, the negative portion appears at these points because of conduction through D-2 and D-3. This can be seen from Figure 5. The wave forms at B-1 and B-2 are shown in the center and lower traces, while the upper trace shows the signal output at Q-6. These traces show that the signal is distorted and appears with diminished amplitude. This occurs because of the nature of the current-voltage characteristics of the diodes (Figure 6). The principal effect is a delay in conduction resulting from the knee of the diode conduction curve. It is to be noted that though the phase detector is bi-directional in signal conduction in the absence of reference, the dc potential difference is zero for balanced diodes.

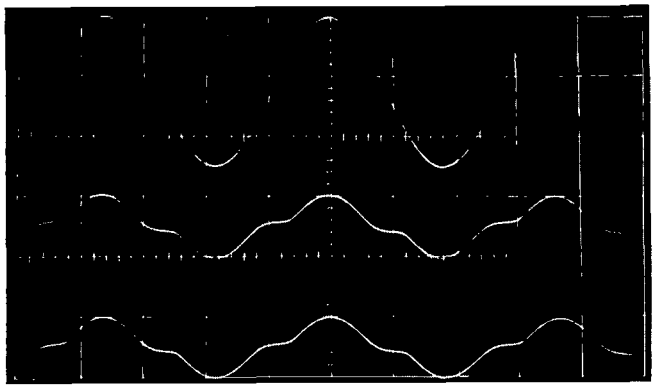


Figure 5—Phase detector bi-directional conduction in the absence of reference input. F = 50 kc. Upper trace - 1 v RMS signal at Q-6; 1 v p-p = .9 cm. Center trace - output at B_1, 1 v p-p = 1.8 cm. Lower trace - output at B_2, 1 v p-p = 1.8 cm.

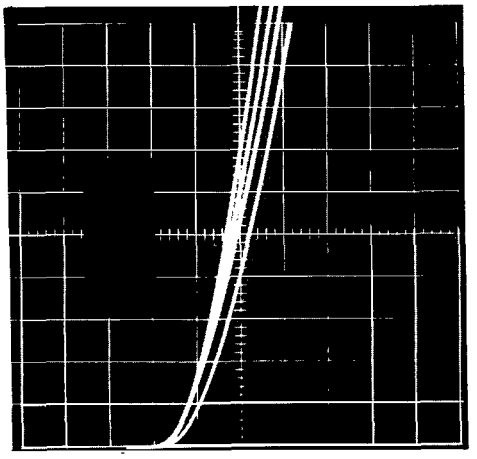


Figure 6—Forward conduction characteristics of diodes D-1, D-2, D-3, D-4 (left to right). Vertical: I = 50 ma/division; Horizontal: E = .5 v/division.

Phase Detector Transfer Function

Thus far the operation of the phase detector has been described with separate reference and signal inputs; the circuit was seen to be bi-directional with respect to signal conduction. Ideally with simultaneous inputs, the reference suppresses the bi-directional conduction and provides a transmission path for the signal over a time interval corresponding to half a cycle of the reference. This is due to the conduction of the diodes D-1 and D-2 during the positive portion of the reference. Hence the output at B-1 will be a 180 degree slice of the signal, the starting point being advanced or retarded depending on the signal-reference phase angle. The polarity of the diodes D-3 and D-4 is such that the transmission path is provided on the negative portion of the reference. Since conduction is retarded 180 degrees the signal output at B-2 will be the mirror image of the output at B-1. Ideally the balance of the system with respect to the reference is maintained so that the reference does not contribute to the output at B-1 and B-2. The output wave

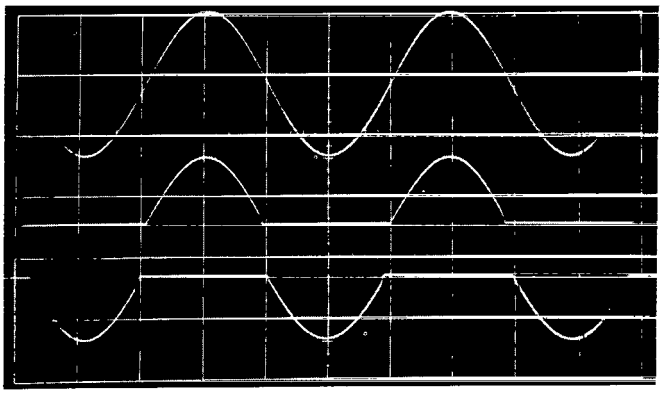


Figure 7—Phase detector output for $\theta = 0°$, $E_r = 5$ v, f = 1 kc. Upper trace - 1 v RMS signal at Q-6, 1 v = .85 cm. Center trace - output at B_1; 1 v = 1.7 cm. Lower trace output at B_2, 1 v = 1.7 cm.

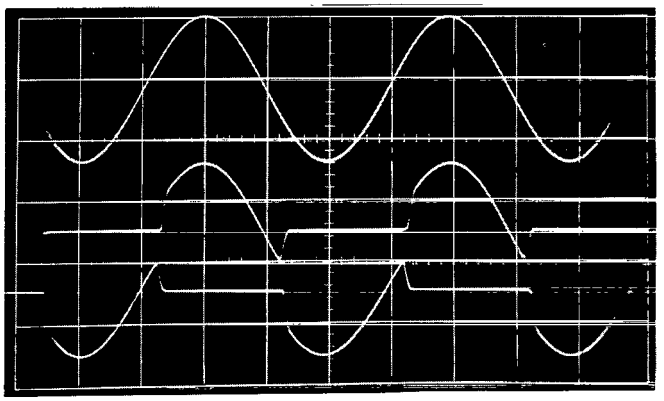


Figure 8—Phase detector output for $\theta = 45°$, $E_r = 5$ v, f = 1 kc. Upper trace - 1 v RMS signal at Q-6, 1 v = .85 cm. Center trace - output at B_1; 1 v = 1.7 cm. Lower trace output at B_2, 1 v = 1.7 cm.

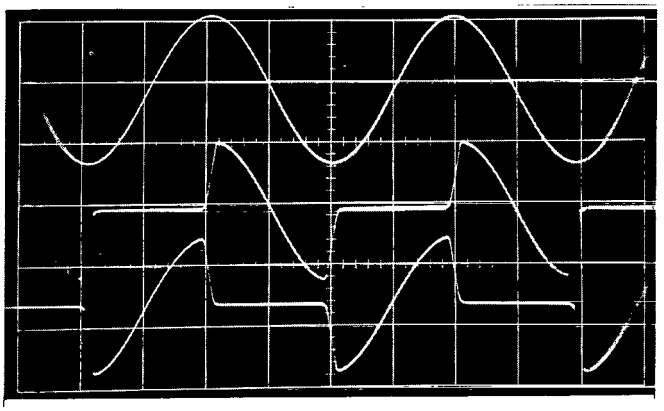


Figure 9—Phase detector output for $\theta = 90°$, $E_r = 5$ v, f = 1 kc. Upper trace - 1 v RMS signal at Q-6, 1 v = .85 cm. Center trace - output at B_1; 1 v = 1.7 cm. Lower trace output at B_2, 1 v = 1.7 cm.

forms for signal-reference phase angle of 0, 45, and 90 degrees are shown in Figures 7, 8, and 9. The central trace shows the output at point B-1 in Figure 3 (diodes D-1 and D-2) while the lower trace shows the output at B-2. The upper trace shows the signal-voltage output at transistor Q-6. Deflection sensitivity of the signal presentation (upper trace) is one half that of the lower traces so that the relative amplitude between the signal and the rectified portions of the signal is maintained. The lower sensitivity was required to maintain proportion because the signal output at transistor Q-6 is attenuated by approximately one-half by the T network (Figure 3c). Because the half-wave signal outputs are of opposite polarity relative to ground, the total potential difference available at the output terminals A-1 and A-2 is twice the individual potentials. Integration of the individual outputs is obtained by 300,000-ohm resistors feeding a 2-μf capacitor placed across A-1 and A-2.

Quantitatively the dc output at the A-1 terminal is the integral of the signal voltage, with the lower limit corresponding to the incidence of the on-time (diodes D-1 and D-2 conduct) and the upper limit corresponding to the incidence of the off-time (diodes D-1 and D-2 cease conducting). The resulting definite integral is then divided by a time corresponding to a complete reference cycle to obtain an average. In describing the dc output, quantitatively the following assumptions are made: (1) Diodes D-1 and D-2 conduct when $E_r > 0$ with a forward resistance of zero independently of the signal voltage; similarly diodes D-3 and D-4 conduct for $E_r < 0$ with zero forward resistance. (2) E_r does not appear in the output; i.e., the system is perfectly balanced with respect to the reference and balance is maintained when the signal is present.

The integral giving the dc output at A_1 is determined as follows: The instantaneous voltage output of the equivalent signal source (Figure 3) at angular frequency ω is $\sqrt{2}\,(.476)\,E_s \sin n(\omega t + \theta)$, where θ is the phase angle of the signal measured relative to the reference output E_r, E_s = RMS value at the output of transistor Q-6. The factor n is the ratio of the signal frequency to the reference frequency and is taken to represent an integer. The dc output at A_1 where D-1 and D-2 conduct during the positive half cycle of the reference, i.e. from 0 to π radians, is given by

$$E_{A_1} = \frac{K\,(\sqrt{2})(.476)E_s}{\frac{1}{f}} \int_{t_1=0}^{t_2=\pi/\omega} \sin n(\omega t + \theta)\, dt\,, \tag{1}$$

where $f \equiv \omega/2\pi$. The factor K in the above equation is the fraction of the signal voltage transferred to the 51,000-ohm load resistance through the source resistance of 2,660-ohms (Figure 3). This fraction is $51/(51 + 2.66)$ or 0.95. With this value of K Equation 1 integrates to (Appendix A)

$$E_{A_1} = \frac{(.95)\,(\sqrt{2})(.476)E_s}{\pi n} \cos n\,\theta, \text{ for n odd,} \tag{2}$$

$$E_{A_1} = 0, \text{ for n even.}$$

To determine the dc output appearing at terminal A-2, note that the polarity of diodes D-3 and D-4 is such that conduction occurs during the negative half cycle of the reference, i.e. from π to 2π radians:

$$E_{A_2} = \frac{(.95)\,\sqrt{2}(.476)E_s}{\frac{1}{f}} \int_{t_1=\pi/\omega}^{t_2=2\pi/\omega} \sin n(\omega t + \theta)\, dt\,. \tag{3}$$

Integrating, we have (Appendix I)

$$E_{A_2} = \frac{-(.95)\,(\sqrt{2})(.476)E_s}{\pi n} \cos n\theta, \text{ for n odd,} \tag{4}$$

$$E_{A_2} = 0, \text{ for n even.}$$

The total output voltage across the A-1—A-2 terminals is the potential difference $E_{A_1} - E_{A_2}$ (from Equations 2 and 4):

$$E_T = \frac{(.95)\,\sqrt{2}(.952)E_s}{\pi n} \cos n\theta, \text{ for n odd,} \tag{5}$$

$$E_T = 0, \text{ for n even.}$$

The response predicted mathematically by Equation 5 at odd multiples of n is evident intuitively: The switching interval occurs over a half period of the reference. This interval will contain n

alternate positve and negative half cycles of the signal. Each alternate pair cancels in the averaging process, thus a dc output will result only when the switching interval contains an odd number of half cycles of the signal. The attenuation factor $1/n$ appears in Equation 5 because the remaining odd half cycle is averaged over $2n$ half periods of the signal, whereas when n is unity the averaging occurs over 2 half cycles of the signal frequency since this is a half-wave rectification process.

In deriving Equation 5, the principal assumption made was that the diode pair conduction was determined solely by the reference source and independently of the signal. This assumption of independence is to a large measure satisfied if the reference voltage level is of sufficient magnitude relative to the signal level. However at low reference levels the above assumption is no longer valid and two effects occur which to lead to a reduction in dc output at the A-1—A-2 terminals: (1) The conduction angle becomes less than 180 degrees, (2) Bi-directional conduction occurs. The first effect can be seen in Figure 10 where the reference level has been reduced from 5 to 0.5 v (signal level is 1 v, as in Figures 7, 8, and 9). The upper trace at f = 1 kc is the signal output at transistor Q-6; The inner trace is the output of diodes D-1—D-2 at point B-1 (Figure 1) with the base line approximately coincident with the signal base line. The lower trace is the output of diodes D-2—D-3 at point B-2. Deflection sensitivity of the signal presentation is one half that of the lower traces so as to maintain amplitude proportion. It is evident that the reduction in the conduction angle is at least 30 degrees, although bi-directional conduction is not pronounced.

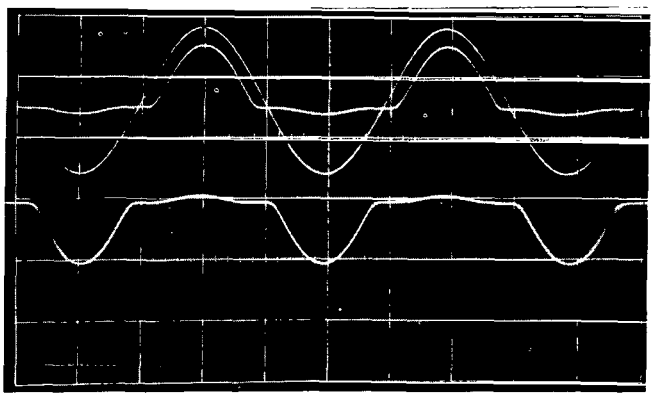


Figure 10—Phase detector output wave forms with reduced reference level: E_r = 0.5 v RMS, E_s = 1 v RMS, f = 1 kc, θ = 0: Upper trace - 1 v RMS signal at Q-6, 1 v p-p = .85 cm. Inner trace output at B_1, 1 v p-p = 1.7 cm. Lower trace - output at B_2, 1 v p-p = 1.7 cm.

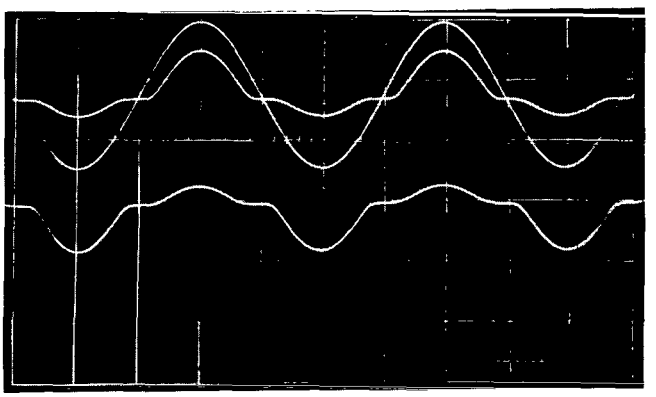


Figure 11—Phase detector output wave forms with reduced reference level: E_r = .25 v RMS, E_s = 1 v RMS, f = 1 kc, θ = 0. Upper trace output - 1 v RMS signal at Q-6, 1 v p-p = .85 cm. Inner trace output at B_1, 1 v p-p = 1.7 cm. Lower trace output at B_2, 1 v p-p = 1.7 cm.

The reduction in conduction angle reduces the interval of integration in Equations 1 and 3 with a corresponding reduction in the value of E_{A_1} and E_{A_2}.

Pronounced bi-directional conduction as well as further reduction in the conduction angle is evident in Figure 11, which is identical with Figure 10 except that the reference has been further reduced to a level of 0.25 v. Bi-directional conduction is evident in the lower trace (the output of diodes D-3 and D-4) below the interval of positive excursion of the

signal. Because the phase angle is zero, the reference is in phase with the signal and is therefore positive in this first interval; the polarity of D-3 and D-4 is such that the reference would ordinarily bias them off. Similarly, in the following interval where the signal and reference are negative, conduction is seen to take place in diodes D-1 and D-2, which with sufficient reference would ordinarily be biased off. Comparison of these traces with those shown in Figure 7 where the reference level is 5 v will make the above discussion clearer. A reduction in phase detector output results from bi-directional conduction in that rectification of the signal decreases since conduction takes place during both positive and negative excursions. In the limiting case where the reference is zero (as in Figure 5), rectification ceases entirely.

Quantitatively, both of these effects involve the forward resistance characteristics of the diodes in the region of greatest curvature (Figure 6). This resistance* is given by

$$rd = \frac{.052}{I_f} + R_s$$

where I_f = forward current, R_s = series resistance in ohms at T = 25 °C, r_d = forward resistance. Measured values of one diode show that this relationship is followed rather closely for currents greater than 10 μ-amp.

However, the inverse relationship between resistance and current exhibited by the solid state diodes precludes analysis by linear means; consequently no attempt was made to derive the phase detector transfer function at low reference levels. This aspect of phase detector operation has been considered by Blickensderfer† but his analysis appears to be adequate only for thermionic diodes. His analysis shows that at low reference-to-signal levels the output vs phase angle becomes more linear. However the data shown later in Figure 16 appear to be in conflict with Blickensderfer's analysis in that a cosine response, rather than a linear response was observed at low reference-to-signal levels.

MEASURED CHARACTERISTICS

Reference and Signal Balance

The development of Equation 5 postulated ideal diodes and a balanced push-pull reference source. Operationally these ideal conditions lead to zero output with reference input only, and zero dc output with signal input only. Individual signal and reference balances are desirable in actual operation of the phase detector as lack of balance results in dc offset of the zero point ($\theta = 90°$) of the phase detector cosine response as well as lack of symmetry in the positive and negative regions.

The principal cause of deviation from ideal balance probably arises from differences in individual diode characteristics. Although the diodes employed in this circuit were purchased as matched pairs there remains some disparity, particularly in the forward resistance characteristics

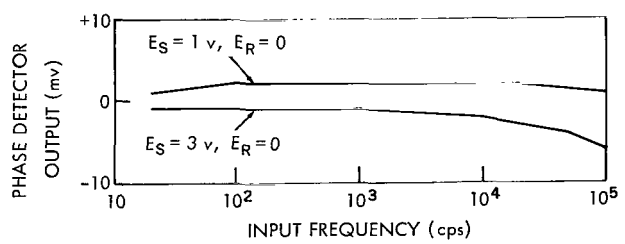
*"General Electric Transistor Manual", 6th Edition, 1962, pp 281-283.
†Blickenderfer, J. A., "Diode Phase Detectors", Electronics Research Laboratory Technical Report No. 4, June 15, 1953.

of D-4. This is evident from the voltage-current traces shown in Figure 6. A secondary cause of lack of balance is the small inequality in the amplitudes of the reference push-pull outputs at transistors Q-3 and Q-4 which is evident from the plot shown in Figure 2. To compensate for these deficiencies, at least partially, three balance potentiometers were included in the circuit. Balance with signal input only was obtained by a 1,000-ohm potentiometer placed in the center of the T network and is designated as "signal balance potentiometer" in the circuit diagram, Figure 1. For balance with reference input a 1,000-ohm potentiometer was inserted in series with diodes D-1 and D-2; An identical unit was placed in series with diodes D-3 and D-4. These two potentiometers are designated as "reference balance" in the circuit diagram.

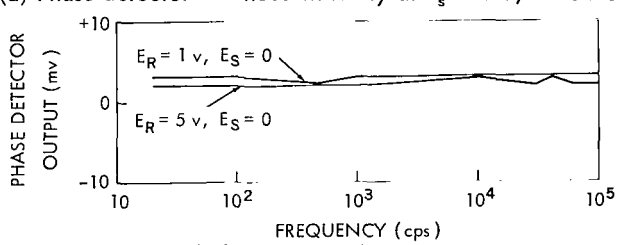
The designation of individual potentiometers as "signal" or "reference" is optimistic in that their effects on the signal or reference balance are to some extent mutually interacting. In practice, however, these adjustments were not found difficult to achieve, although the balances so obtained were functions of voltage level, temperature, and to a lesser extent, frequency.

Figure 12a illustrates the dependence of phase detector balance versus frequency on signal level. The phase detector output across A-1 and A-2 was minimized by adjusting the signal potentiometer with a 20 cps, 1 v signal input and zero reference input. The output was then plotted over a frequency range of 20 cps to 100 kc. To show the effect of a change in signal level, the signal was increased to 3 v and the output versus frequency again plotted. A similar procedure was followed in Figure 12b to show the effect of a change in reference level. In this case, initial balance was made at a 20 cps reference input of 5 v and zero signal input by adjusting the reference potentiometer.

The effects of ambient temperature variation on signal balance versus frequency are shown in Figure 13a. For this data, initial

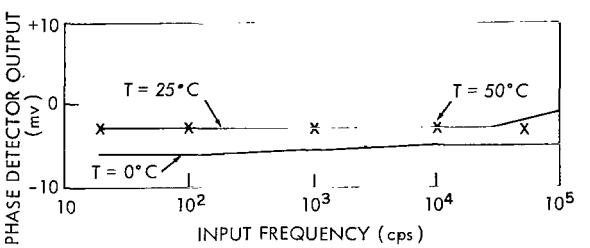


(a) Phase detector balanced initially at E_s = 1 v, f = 20 c

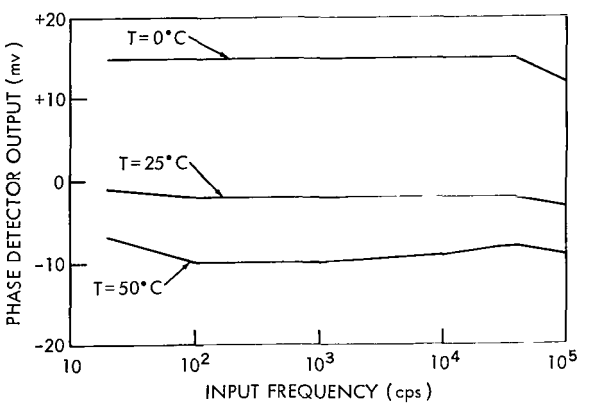


(b) Phase detector balanced initially at E_r = 5 v, f = 20 cps

Figure 12—Effect of change in signal or reference voltage on phase detector balance.



(a) Temperature effects on signal balance
E_s = 1 v, E_r = 0.



(b) Temperature effects on reference balance,
E_r = 5 v, E_s = 0

Figure 13—Temperature effects on signal or reference balance.

signal balance was made at T = 25 °C with a 20 cps, 1 v signal and zero reference input. The phase detector output versus frequency was then plotted for temperatures of 0 °C, 25 °C and 50 °C respectively. Reference balance versus frequency is shown for these temperatures in Figure 13b. Initial balance was established at 5 v reference input and zero signal input with T = 25 °C.

One final consideration with respect to balance has yet to be considered; that is, possible leakage through the 68 μf capacitors employed to couple the signal and reference to the diode circuitry. It might be expected that the capacitor leakage would produce an output at A-1 or A-2 in the absence of signal or reference inputs, particularly at higher temperatures. However at the highest temperature employed no output attributable to leakage was noted.

Phase Detector Response—Measured and Predicted Values

The solid line plotted in Figure 14 was computed from Equation 5 for a signal voltage of 1 v RMS, n = 1. The data points indicated by trangles are the measured dc output of the phase detector

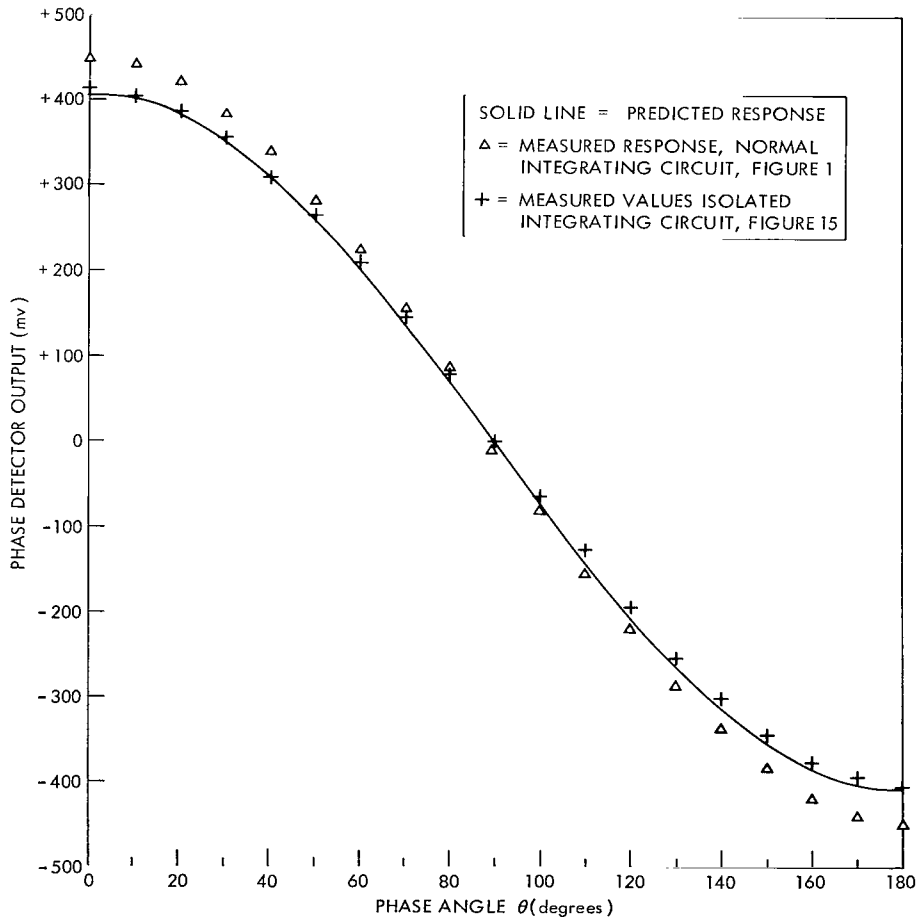


Figure 14—Measured and predicted response. E_r = 5 v RMS, E_s = 1 v RMS, f = 1 kc.

versus phase angle θ at a frequency of 1 kc for E_r = 5 v RMS. Data points indicated by crosses were obtained with the additional circuitry shown in Figure 15. With the use of this circuitry the integrating network was isolated with a high-input-impedance differential amplifier so that the potential normally developed across the integrating capacitor was prevented from affecting conduction in the diodes. Ordinarily a small dc potential does appear at the jucture of each pair of diodes because of transfer by means of the 300,000-ohm resistors to the upper terminals of the 51,000-ohm resistors at the diode junctions.

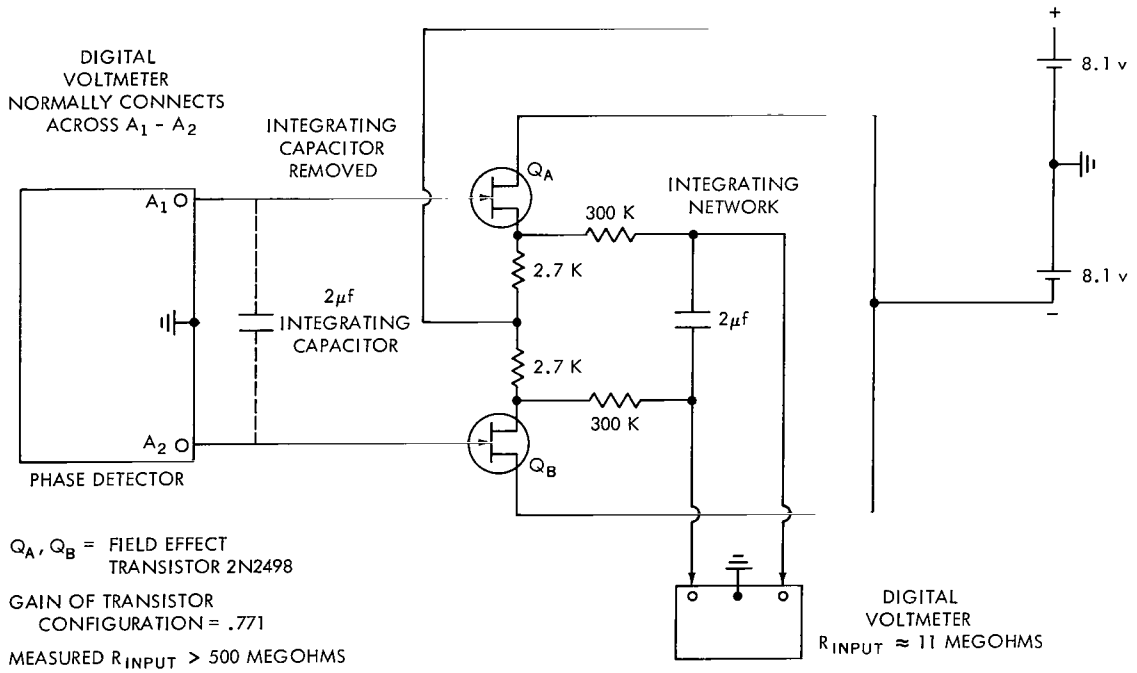


Figure 15—Isolating circuit employed taking data shown Figure 14.

Cosine Response at Lower Reference Inputs

The dc outputs at the A-1—A-2 terminals versus phase angle with the reference input decreased from 5 v (Figure 14) to 1 v, 0.5 v, and 0.25 v, respectively, are shown in Figure 16. Signal input is constant at E_s = 1 v RMS. Data points in Curve 1 are plotted as triangles while the values predicted by Equation 5, E_r = 1 v, n = 1 are shown as the solid line.

The second set, Curves 2 and 3, illustrate the response of the phase detector where bidirectional conduction and pronounced reduction in conduction angle occur because of insufficient reference voltage. The output wave forms at θ = 0 for reference voltages 0.5 and 0.25 v, have been shown in Figures 10 and 11. For these curves the solid lines of Figure 16 are best fit cosine functions rather than predicted values.

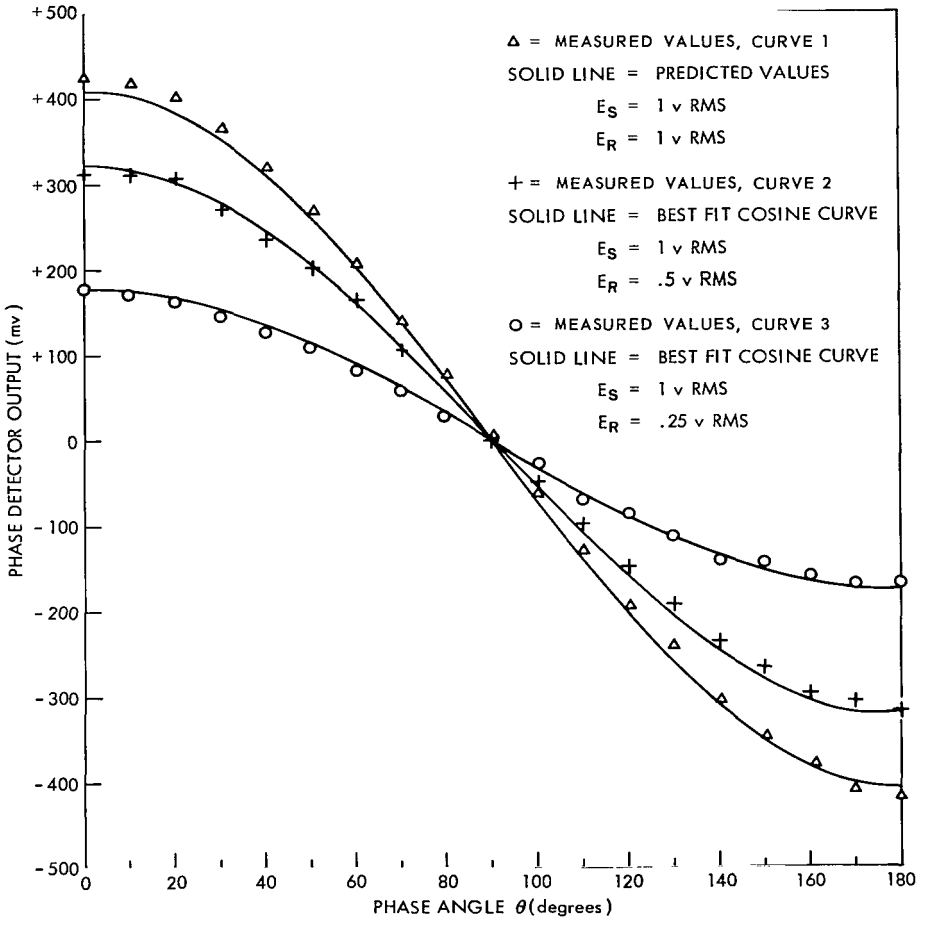


Figure 16—Phase detector output versus phase angle for E_r = 1 v, .5 v, .25 v RMS; E_s = 1 v RMS; f = 1 kc.

Wide Band Cosine Response

Wide band cosine response of the phase detector is illustrated by measurements presented in Figures 17 and 18. Previous to taking this data individual signal and reference balances were made at 30 cps at levels of 1 and 5 v respectively. With this fixed balance, cosine curve responses were measured at the following frequencies: 30, 400 cps, 10, 25, 50, and 100 kc with E_r = 5 v RMS, E_s = 1 v RMS. This presentation differs in one aspect from the previous cosine measurements—the phase angle plotted as the abcissa is the *input* phase angle rather than previously defined angle θ. Specifically, the phase angle of the signal at the base of Q-5 was measured relative to the reference input at the base of Q-1. This angle differs by 180° from θ as a result of the phase inversion which occurs in the voltage amplifier stage (Figure 1). Consequently, as a result of the identity $\cos(\theta \pm 180) \equiv -\cos\theta$, E_T in Equation 5 becomes negative for positive θ. Thus, this set of cosine curves is seen to be inverted in polarity when compared with the previous sets. Equation 5 is plotted with this alteration in sign as a solid line in Figures 17 and 18.

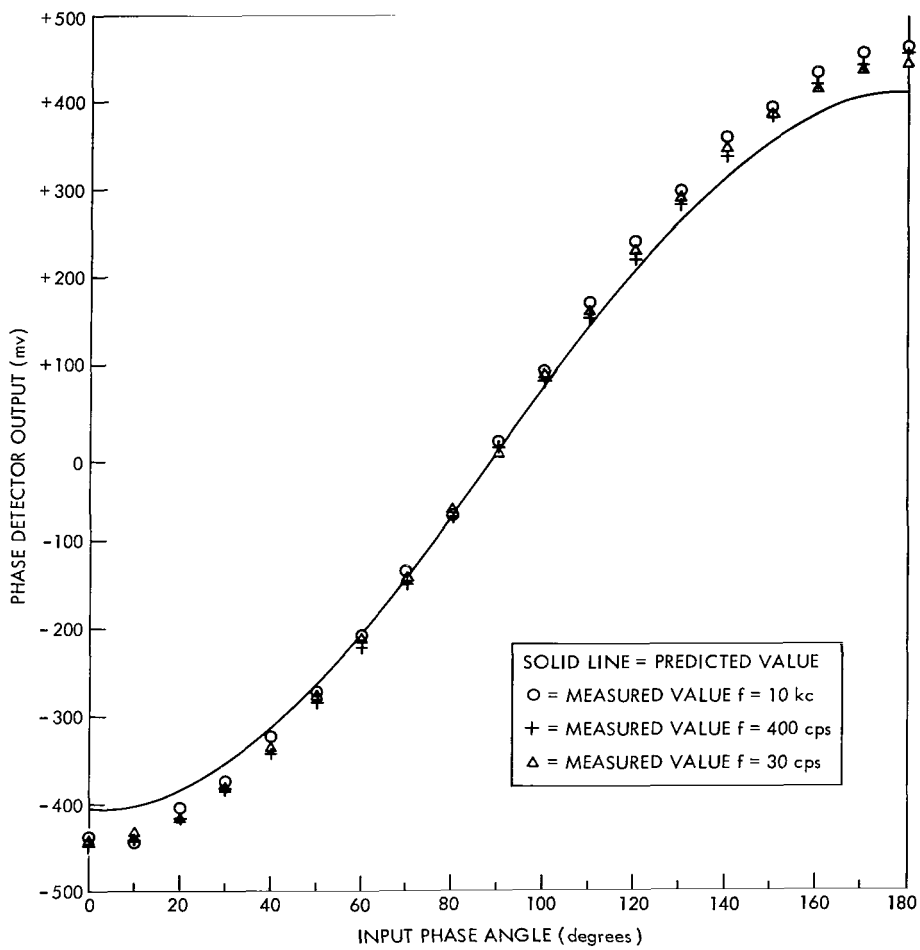


Figure 17—Phase detector output versus input phase angle for f = 30, 400 cps and 10 kc; input to signal amplifier = 1 v; input to reference amplifier = .61 v (E_r = 5 v RMS).

Effects of Ambient Temperature Variation on Cosine Response

Figure 19 shows the cosine response with the input phase angle as the abcissa, T = 0, 25, and 50 °C, and f = 50 kc. The initial balance was established at f = 30 cps, E_r = 5 v RMS, E_s = 1 v RMS. The lower solid line in Figure 20 is the measured response at T = 25 °C; Data taken at 50 °C are plotted as crosses; and the upper line is the response at T = 0 °C.

Cosine Response when Signal Frequency is an Odd Multiple of the Reference Frequency

Equation 5 predicts that although the maximum phase-detector cosine response occurs for equal signal and reference frequencies (n = 1), cosine responses attenuated by the factor 1/n will also occur if the signal frequency is an odd multiple of the reference frequency. Experimentally, the cosine response at odd multiples of n is difficult to determine. The type of system required to perform this measurement is shown in Figure 20a. In this system a single source feeds the

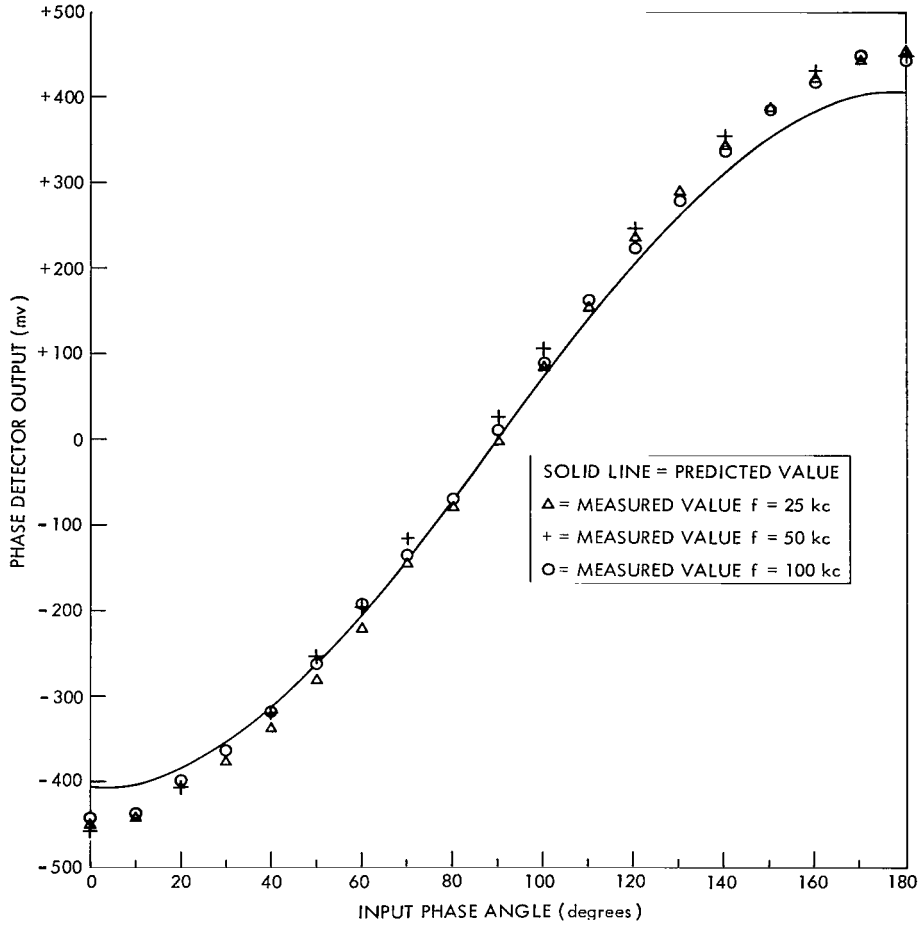


Figure 18—Phase detector output versus input phase angle for f = 25, 50, and 100 kc; input to signal amplifier = 1 v; input to reference amplifier = .61 volts RMS (E_r = 5 v RMS).

reference input and simultaneously a calibrated phase shifter. The output of the phase shifter drives an 'N' times frequency multiplier which is fed into the signal input of the phase detector. Coherence between signal and reference inputs is thus assured. Unfortunately most commonly available multipliers produce distorted outputs which would alter the cosine response of the phase detector. The method shown in Figure 20b is much simpler but does not permit actual cosine response measurement. The system does, however, permit the measurement of the 1/n factor predicted in Equation 5. The more simple method uses separate generators as reference and signal sources. The reference source is operated at a fixed frequency F_1; the signal source is adjusted to be *nearly* an odd multiple of F_1. The lack of periodicity between generator frequencies will then cause a cyclic variation in phase angle with a resultant fluctuation in phase detector output. (This fluctuation is, of course, the cosine response, but the phase angle is undetermined.) With this method, a pen recorder with stationary chart was used to record the output for different

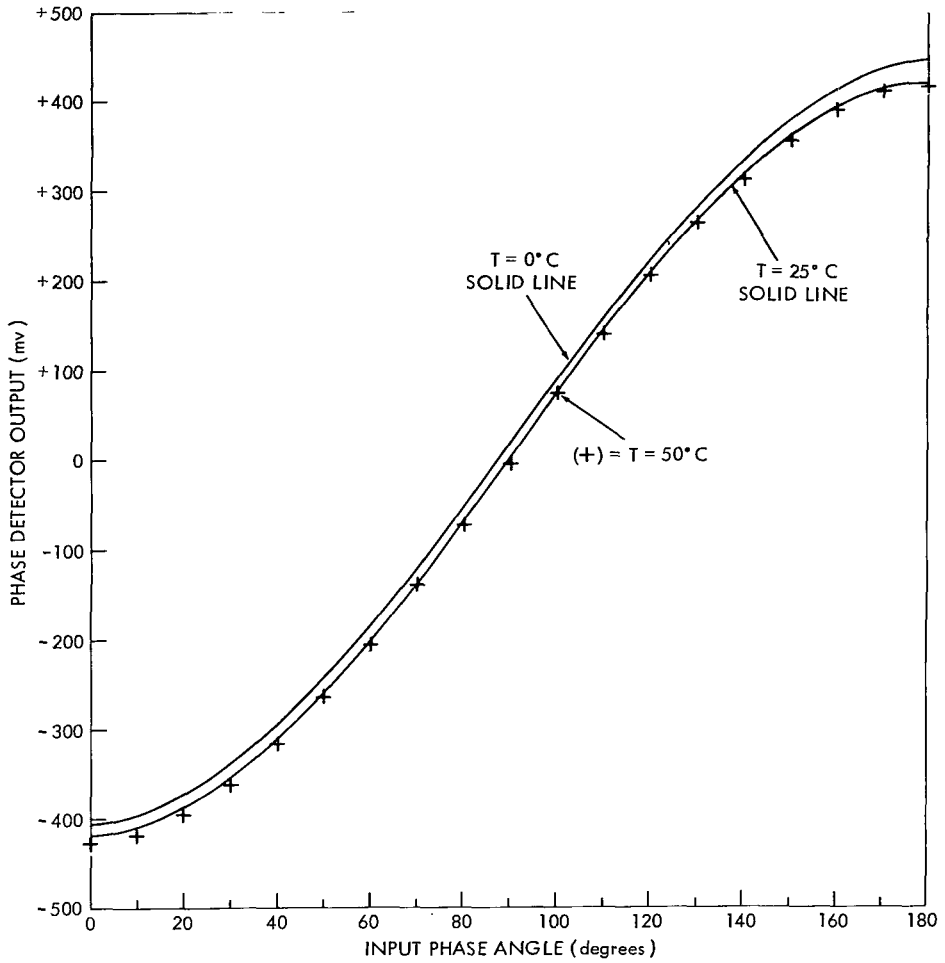
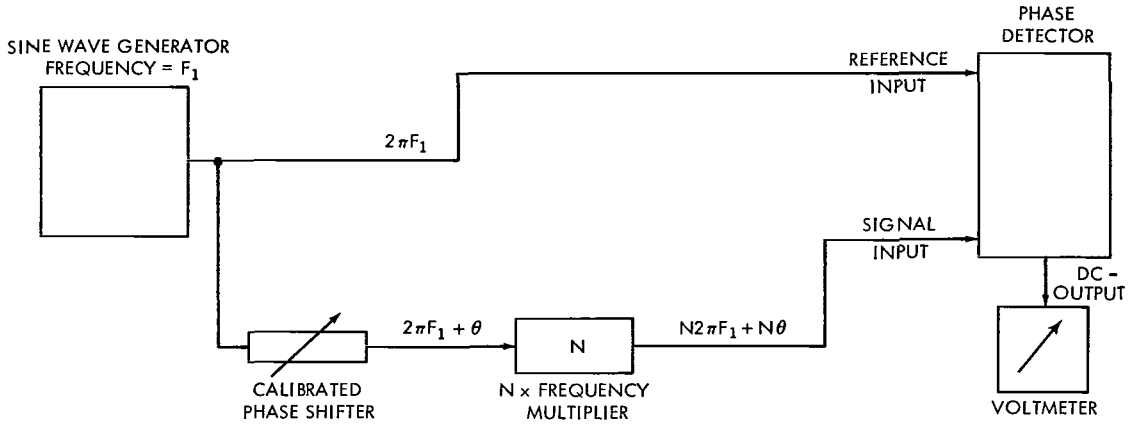


Figure 19—Measured phase detector output versus phase angle for T = 0, 25, and 50°C; E_r = 5 v RMS; E_s = 1 v RMS; F = 50 kc.

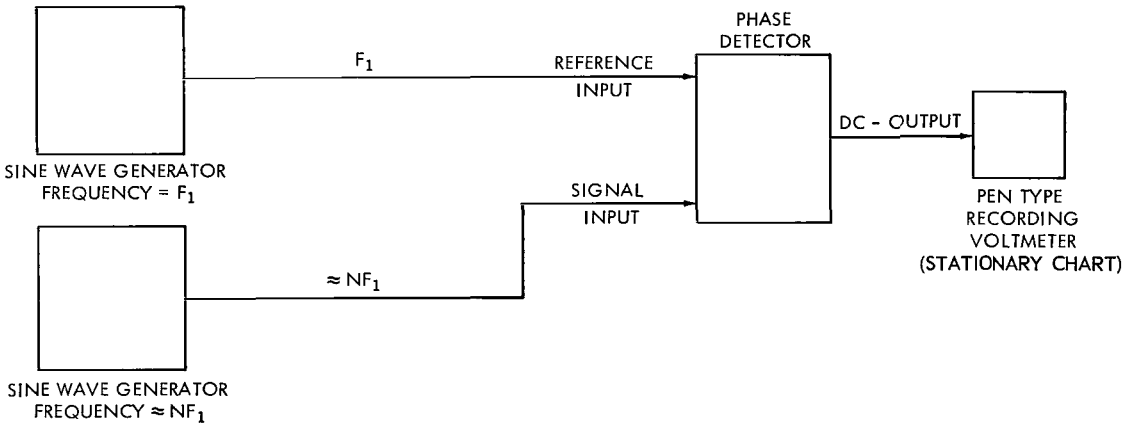
values of n. The length of the traces so obtained are proportional to the maximum to minimum excursion of each particular cosine response. The data obtained from the trace length measurement are shown in the last column of Table 2; the predicted values are shown in the center column.

The two generator system shown in Figure 20 was also used to determine whether cosine responses occurred at fractional values of n (a case not considered in the analysis) as well as noninteger values of n. No responses were observed at these values.

It might be remarked that the cosine response at odd multiples of n, though not measured directly by the two generator method has been observed in a phaselock system which included this type of phase detector.



(a) Ideal method for measuring odd-frequency multiple-response of phase detector



(b) Approximate method for determining maximum output only, at odd-frequency multiples.

Figure 20—Ideal and approximate methods for determining phase detector response at odd-frequency multiples.

Table 2

Predicted and Measured Values of Phase Detector Maximum Output Ratios at Odd Frequency Multiples.

Signal-reference frequency ratio N	Predicted maximum output for N = 1 divided by predicted maximum output for indicated N	Measured maximum output for N = 1 divided by measured maximum output for indicated N*
3	3	3.08
5	5	5.2
7	7	7.3
9	9	11.1

*Reference frequency =1 kc, E_R = 5 v RMS, E_S = 1 v RMS.

EXPERIMENTAL PROCEDURE

The two basic quantities which were measured were the A-1—A-2 voltage output and the signal-reference phase angle. The voltage output was measured with a digital voltmeter with an input resistance of 11-megohms; readings made with this instrument were corrected for loading. A value of 600,000 ohms at the A-1—A-2 terminals was employed in making this correction. Phase angle determination was made with a standard commercial instrument which had a coincident slicer preceded by cathode-coupled limiters. Claimed accuracy for this instrument was ±1 percent. Phase angle variation over a 180° range required three auxiliary phase shifters each covering a different band of frequency. At the upper frequencies a commercial delay line was found adequate. At frequencies below 30 kc and above 1 kc a capacitive rotating field type phase shifter was used. This device has two sets of stator plates mounted orthogonally and excited by quadrature voltages. A third set of plates is mounted so as to form a rotor which is capacitively coupled to the stator. A two-phase rotating field is produced by the stator plates and therefore the output of the rotor shows a phase variation proportional to its angular position. For frequencies below 1 kc a device similar in principle but magnetic in operation produced variable phase shift from a wound rotor.

CONCLUSION

The phase detector described here has proved to be very reliable in operation over a six-month period. However, the system reliability could probably be increased by the substitution of a type 2N719A transistor in all stages with the exception of Q-6; the 2N719A has an 80 v collector-to-emitter rating which should decrease the likelihood of transistor failure. The major design goal of constant cosine response in a 20 cps to 100 kc frequency range has been successfully achieved. Reference balance stability versus temperature, though adequate, could probably be improved by the selection of more carefully matched diodes. The use of a transistor push-pull wide-band amplifier as the reference source, rather than a transformer, appears to be a good choice, although there is a sacrifice in total power consumption.

The agreement between measured and predicted cosine responses appears to be very nearly perfect when the phase-detector integrating circuit is electrically isolated from the diodes. Where isolation is not employed the response is cosinusoidal as predicted, but the amplitude agreement shows a 10 percent error.

Extension of the present analysis to describe adequately the operation at low reference-to-signal-voltage ratios appears to be difficult with other than graphical means.

The predicted attenuation factor $1/n$ for odd-multiple signal-to-reference-frequency ratios shows good agreement with measured values up to and including 7, but shows an unexplained error at $n = 9$.

Measurements show the phase detector to be free from spurious responses throughout the operating frequency range.

(Manuscript received August 28, 1963)

Appendix I

Mathematical Analysis of the Phase Detector

Equation 1, page 9, with $K = .95$, is

$$E_{A_1} = \frac{.95(\sqrt{2})(.476)E_s}{\frac{1}{f}} \int_{t_1 = 0}^{t_2 = \pi/\omega} \sin n(\omega t + \theta)dt \qquad \text{(I-1)}$$

For convenience we let $A = (.95)\sqrt{2}(.476)$. Equation I-1, in integrable form, is

$$E_{A_1} = \frac{AE_s}{n\omega\frac{1}{f}} \int_{t_1 = 0}^{t_2 = \pi/\omega} \sin n(\omega t + \theta)\,(n\omega)dt \ , \qquad \text{(I-2)}$$

which yields

$$E_{A_1} = -\frac{AE_s}{2\pi n} \cos(n\omega t + n\theta) \Big|_{t_1 = 0}^{t_2 = \pi/\omega} \ . \qquad \text{(I-3)}$$

$$= -\frac{AE_s}{2\pi n} \left[\cos(n\pi + n\theta) - \cos n\theta\right] . \qquad \text{(I-4)}$$

But $\cos(\alpha \pm \beta) \equiv \cos\alpha\cos\beta \mp \sin\alpha\sin\beta$; with this identity, Equation I-4 is

$$E_{A_1} = -\frac{AE_s}{2\pi n} \left[\cos n\pi \cos n\theta - \sin n\pi \sin n\theta - \cos n\theta\right] . \qquad \text{(I-5)}$$

Let n be an *even* integer; then,

$$\cos n\pi \equiv +1 \ ,$$

$$\sin n\pi \equiv 0 \ .$$

With these relationships Equation I-5 gives

$$E_{A_1} = -\frac{AE_s}{2\pi n} \left[\cos n\theta - \cos n\theta\right] \equiv 0, \text{ for n even.} \qquad \text{(I-6)}$$

Let n be an *odd* integer, then

$$\cos n\pi \equiv -1 ,$$

$$\sin n\pi \equiv 0 .$$

Consequently Equation I-5 becomes

$$E_{A_1} = -\frac{AE_s}{2\pi n}\left[-\cos n\theta - \cos n\theta\right] = \frac{AE_s}{\pi n}\cos n\theta , \text{ for n odd.} \tag{I-7}$$

The integral giving E_{A_2} is obtained by a half-period shift of the limits of integration of Equation I-2:

$$E_{A_2} = \frac{AE_s}{2\pi n}\int_{t_1 = \pi/\omega}^{t_2 = 2\pi/\omega} \sin n(\omega t + \theta)\, n\omega dt . \tag{I-8}$$

The value of the above integral is

$$E_{A_2} = -\frac{AE_s}{2\pi n}\left[\cos(2\pi n + n\theta) - \cos(n\pi + n\theta)\right] . \tag{I-9}$$

With the previous cosine double angle identity this can be written as

$$E_{A_2} = -\frac{AE_s}{2\pi n}\left[\cos 2\pi n \cos n\theta - \sin 2\pi n \sin n\theta - \cos n\pi \cos n\theta + \sin n\pi \sin n\theta\right] , \tag{I-10}$$

but $\sin 2\pi n \equiv 0$, and $\sin \pi n \equiv 0$; where n is any integer. Thus these terms can be eliminated from Equation I-10.

$$E_{A_2} = -\frac{AE_s}{2\pi n}\left[\cos 2\pi n \cos n\theta - \cos \pi n \cos n\theta\right] . \tag{I-11}$$

For n *even*,

$$\cos 2\pi n \equiv \cos \pi n ;$$

thus,

$$E_{A_2} = -\frac{AE_s}{2\pi n}\left[\cos n\theta - \cos n\theta\right] \equiv 0 . \tag{I-12}$$

For n *odd;*

$$\cos 2\pi n \equiv +1$$

$$\cos \pi n \equiv -1 ;$$

hence, Equation I-11 gives

$$E_{A_2} = -\frac{AE_s}{2\pi n}\left[\cos n\theta + \cos n\theta\right] = -\frac{AE_s}{\pi n}\cos n\theta . \qquad \text{(I-13)}$$

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