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30p.

PULSE HEIGHT ANALYZER AND COMMUTATING CIRCUITS FOR IMP E vs dE/dx NUCLEAR ABUNDANCE EXPERIMENT

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AND COMMUTATING CIRCUITS FOR

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EXPERIMENT

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LIST OF ILLUSTRATIONS

PULSE HEIGHT ANALYZER AND COMMUTATING CIRCUITS FOR IMP E vs dE/dx NUCLEAR ABUNDANCE EXPERIMENT

INTRODUCTION

The E vs dE/dx experiment for the IMP spacecraft (S-74) is comprised of four cards containing instrumentation and electronics as shown in drawing 631.4-62-109. A cosmic ray scintillation telescope on card S-74/EE3 furnishes analog information on three output channels. Pulse height analyzer and coincidence logic circuits on the two electronics cards S-74/EE1 and S-74/EE2 change the analog information from two of the telescope output channels to digital form according to certain coincidence logic. A Geiger counter cosmic ray telescope on card S-74/EG1 furnishes digital information on three output channels to commutating circuits on electronics card S-74/EE2. Outputs from the pulse height analyzer and commutating circuits are fed in digital form from electronics card S-74/EE2 to the IMP spacecraft telemetry system.

This report describes the two parameter pulse height analyzer, the coincidence logic circuits and the commutating circuits located on the electronics cards S-74/EE1 and S-74/EE2.

PULSE HEIGHT ANALYZER

General Operation

The pulse height analyzer and coincidence logic circuitry is shown in a functional block diagram in drawing No. 631.4-62-84. Outputs from three photomultiplier tubes in the scintillation telescope are fed to circuits on card S-74/EE1 identified as channel A, Channel B, and channel C. These signals are positive-going pulses with 1 to 2 microseconds rise time and a fall time to 1/2 peak amplitude of approximately 7 microseconds. The channel A and channel B circuits on card S-74/EE1 are identical pulse height analyzers with a linear range of 1 to 256. The channel C circuits on card S-74/EE1 include amplifiers to feed a channel C signal to the logic circuits on card S-74/EE2.

The amplitude of an input pulse on channel A is a measure of the linear rate of energy loss, $\frac{dE}{dx}$, for a cosmic ray particle passing

through a thin CsI crystal in the cosmic ray telescope. The amplitude of an input pulse on channel B is a measure of the total energy, E, of a particle whenever it is stopped by a thick CsI crystal, also in the cosmic ray telescope. Coincidence of a channel A and channel B signal indicates that the same particle has given rise to both signals. An input on channel C arises from a particle striking a plastic crystal behind the channel B crystal. Coincidence of a C input with the A and B inputs indicates that the particle has passed through the B crystal and that the B signal is not a true measure of the total energy E. The pulse height analyzer circuits furnish a digital output count proportional to input pulse amplitude on each of the two energy channels (A and B) when and only when these inputs are coincident and no simultaneous input is present on the third channel C. This function is performed through the following operations:

(1) Coincidence-anticoincidence action
(2) Analog to Digital Conversion
(3) Input Disabling

Coincidence-anticoincidence action. Blocking oscillator and gating circuits located on S-74/EE2 furnish gating pulses whenever coincident inputs are received on channels A and B but not C. Linear gates in the channel A and channel B pulse height analyzers are normally blocked and become unblocked when gating pulses are furnished from the coincidence-anti-coincidence circuits.

Analog to Digital Conversion. Channel A and channel B signals which are coincident pass through their respective linear gates into an amplitude-to-time converter in each channel. A gate pulse is generated in channel A with a duration proportional to the A input signal amplitude. A similar gate pulse is generated in channel B with a duration proportional to the B input signal amplitude. Each gate pulse passes a burst of 500 kc oscillator pulses to the pulse height analyzer output. The resulting count of oscillator cycles in the output burst in each channel is proportional to the input signal amplitude in that channel.

Input Disabling. The pulse height analyzer is rendered insensitive to input signals whenever a coincident signal pair is being processed in order to prevent garbling of the analog-to-digital conversion, and also whenever the spacecraft encoder scalers are being read out to the telemetry circuits. Input disabling is accomplished by the BUSY BISTABLE and associated triggering circuits. In its normally RESET

condition this bistable blocks the channel A and channel B output gates and activates the coincidence-anticoincidence circuits. In this state the pulse-height-analyzer is ready to receive inputs from the scintillation telescope.

The BUSY BISTABLE is SET by either of the following:

(a) The first 500 kc oscillator pulse which occurs after the start of a channel A or channel B amplitude-to-time converter gate, or
(b) A SET signal ($\overline{B}$) received from the telemetry encoder.

In the SET condition this bistable performs the following functions:

(a) It starts the channel A and channel B timing action in the amplitude-to-time converters,
(b) It unblocks the channel A and channel B output gates, thus passing a burst of 500 kc oscillator pulses to the A and B outputs, and
(c) It disables the coincidence-anticoincidence circuits, thus rendering the pulse-height-analyzer insensitive to additional inputs while a coincident pulse pair is being processed.

The busy bistable is RESET by the trailing edge of telemetry encoder sync signal (2) F which occurs twice every telemetering sequence.

CIRCUIT DESIGN

The circuits on cards S-74/EE1 and S-74/EE2 are constructed in the form of welded modules and connected together by welded interconnecting matrices. For convenience in circuit description the modules in the pulse-height analyzers are grouped into the following functional sections:

(1) Preamplifier and Shaper Section
(2) Linear Gate Section
(3) Analog-to-Digital Converter Section
(4) Busy Bistable and 500 kc Clock
(5) Coincidence Amplifier and Threshold Detector Section
(6) Coincidence Logic Section
(7) Eight Position Matrix and Scalers
(8) Sync Shapers

Preamplifier and Shaper Section (drawing No. 631.4-62-101)

The preamplifier and shaper section (located on card S-74/EE1) consists of three welded circuit modules: One Amplifier type 1, one Shaper (2 microsecond), and one Amplifier type 2A. Input and output information and gain settings for channels A, B, and C are given in Table 1.

TABLE 1

PREAMPLIFIER AND SHAPER SECTION GAIN SETTINGS						
Channel	Minimum Input Sig.	Amp. Type 1 Gain	Shaper Gain	Amp. Type 2A Gain	Overall Gain	Preamp Output
A	2 mv	5.0	0.45	4.5	10	20 mv
B	10 mv	1.0	0.45	2.0	2	20 mv
C	5 mv	2.0	0.45	4.0	4	20 mv

The Amplifier type 1 is a two stage amplifier operating with positive-going input and output signals. Overall gain is approximately $\frac{R_1 + R_2}{R_2}$. Maximum gain is 10, and the shunting resistor across R_1 is used to adjust the gain to smaller values as needed.

The Shaper, 2 microsecond, is a two stage amplifier with delayed negative feedback. Positive-going input pulses with 2 microsecond rise time and greater than 7 microseconds fall time are shaped to give a very fast fall time. The beginning of the shaped fall time is determined by the delay line (2 microseconds), thus allowing pulses with rise times up to 2 microseconds to reach peak value before decaying. The shape of the output pulse decay is determined by adjusting a shunting resistor across R_3 and R_4. The shaper circuit furnishes negative-going output pulses.

The Amplifier type 2A operates on negative-going input signals and furnishes negative-going output signals. It is a two stage design similar to the type 1 amplifier except that the n-p-n and p-n-p transistors are interchanged and the d-c supply voltage polarities are reversed.

Lower circuit impedances have the effect of reducing phase shift from input to output.

Linear Gate Section (Drawing 631.4-62-103)

This section (located on card S-74/EE1) is divided into the following functional circuits:

Delay line, 3 microseconds
Compensating Amplifier, type 2A (first)
Linear Gate
Compensating Amplifier, type 2A, (second)

A signal from the preamplifier section is delayed 3 microseconds to allow time for the coincidence circuits to operate. The first compensating amplifier type 2A makes up for signal loss in the delay line. The negative-going output signal pulse from this amplifier is fed to the Q1 emitter in the linear gate. Transistors Q1 and Q2 are normally OFF, and conduct only when a gating pulse from the coincidence logice circuits is present on the secondary winding of the pulse transformer T1. Voltage drop from the Q1 emitter to the Q2 emitter is negligible compared to 10 mv. The parallel combination of diode, resistor, and capacitor in the transistor base circuits is necessary to minimize transients in the gated output due to the rise and fall of the gating pulse. The output compensating amplifier type 2A serves as an impedance matching device between the linear gate output and the input to the A to D Section. The signal amplitude corresponding to a pulse-height-analyzer output count of 1 at several reference points in the linear gate section is given as follows:

Reference Point	Min. Signal Amplitude
Input to Linear Gate Section	20 mv
Output of Delay Line	10 mv
First Compensating Amplifier Output	10 mv
Second Compensating Amplifier Output	10 mv

Analog-to-Digital Converter Section (Drawing 631.4-62-104)

This section consists of the following circuits:
Sweep circuit (located on S-74/EE1)

Shaper circuit (located on S-74/EE1)
Output gate (located on S-74/EE1)
Output driver (located on S-74/EE2)

Operation is illustrated in the waveform drawing 631.4-63-35. A negative-going input signal from the linear gate section is amplified by Q1 and Q4 and charges the capacitors C1 and C2 to a negative value proportional to signal peak amplitude. This potential remains at this level as long as Q5 is non-conducting. Emitter followers Q3 and Q2 transfer the capacitor voltage to Q1 emitter, thus the net drive on Q1 is the difference between input signal amplitude and negative emitter voltage. The positive-going portion of the input signal causes Q1 to conduct. This feeds a positive pulse through Q4 to the shaper and initiates a positive shaper output signal. After a 4 microsecond delay to insure that the capacitors charge to the full negative signal peak, coincidence between shaper output and a clock pulse places the busy bistable (not shown on drawing 62-104) in the SET condition. The busy bistable SET signal F causes Q5 to conduct, and the combination of Q5 and the 6.2 volt zener diode (T1653CO) acting as a constant current source discharges C1 and C2 at a constant rate. This discharge begins at the leading edge of the busy bistable signal F and ends when the capacitor voltage drops to its quiescent value. At this point Q1 stops conducting and a negative-going signal from Q1 through Q4 terminates the positive shaper output signal.

The output gate is normally blocked, and becomes unblocked only during coincidence of the positive shaper output and the busy bistable F signal. This coincidence endures as long as capacitors C_1 and C_2 are discharging, which depends on the voltage to which they are initially charged. Thus, the number of 500 kc oscillator pulses which pass through the output gate is proportional to the input signal amplitude. The circuit is designed to generate a 2 microsecond gate in response to a 10 millivolt signal applied to the sweep circuit input, and is linear for input signals up to 2.56 volts.

Output driver modules, one for channel A and one for channel B, are located on card S-74/EE2. These modules are dual emitter followers to provide two output terminals for channel A and two output terminals for channel B.

Busy Bistable and 500 kc Oscillator

These circuits, common to channels A and B, are shown on drawing 631.4-62-105. Busy bistable operation is summarized as follows:

Condition	Trigger	Output F, terminal 2	Output F, terminal 3
SET	+on 1	+6 volts	-3 volts
RESET	+on 4	-3 volts	+6 volts

The bistable is normally in the RESET condition to allow coincidence action to take place. It is placed in the SET condition by action of the "and-or" circuits upon coincidence of A shaper and clock or B shaper and clock.

The 500 kc clock is a crystal controlled oscillator with emitter follower output.

The busy bistable and 500 kc oscillator are both located on electronics card S-74/EE1.

Coincidence Amplifier and Threshold Detector Section

Each channel of the pulse-height-analyzer (channels A, B, and C) has a coincidence amplifier and threshold detector section (see drawing 631.4-62-84) to furnish signals to trigger the coincidence-anticoincidence blocking oscillators. Input to this section is obtained from the preamplifier and shaper section output.

Each coincidence amplifier and threshold detector section consists of the following welded circuit modules (see drawing 631.4-62-102).

Amplifier type 2A, input stage, gain of 10 (on card S-74/EE1)
Amplifier type 2A, driver stage, gain of 7 (on card S-74/EE1)

Threshold detector (on card S-74/EE2)
The threshold detector furnishes a positive 6 volt output pulse whenever a negative-going input pulse exceeds a threshold value determined by the "Threshold Level Adjust" resistor setting.

Coincidence Logic Section

The coincidence logic section, located on electronics card S-74/EE2, consists of six blocking oscillators and one delay line (1 microsecond) connected as shown in the block diagram drawing 631.4-62-106. The characteristics of the output pulses from the different blocking oscillators depends on the operating voltage and the transformer used. The arrangement shown in drawing 631.4-62-106 is summarized as follows:

Designation	Circuit	Transformer	Output Pulse
A	BO-1	T1-0.75-12	3/4 microsecond
B	BO-1	T1-0.75-12	3/4 microsecond
$A \cdot B$	BO-1	T1-1- 12	1 microsecond
C	BO-2	T2-2- 6	2 microseconds
$A \cdot B \cdot \overline{C}$	BO-1	T1-2- 12	2 microseconds
$A \cdot B \cdot \overline{C} \cdot \overline{F}$	BO-1	T1-1- 12	1 microsecond

Blocking oscillator pulse transformers are wound on Alladin Bobbin and Sleeve ferrite coil forms:

Bobbin No. 110-1097
Sleeve No. 110-1098

Winding information is as follows:

Transformer No.	Alladin No.	1-2	3-4	5-6	7-8
T1-.75-12	01-600	11	33	11	11
T1-1-12	01-601	13	39	13	13
T1-2-12	01-602	25	75	25	25
T1-4-6	01-616	28	84	28	28
T2-2-6	01-604	40	120		

The A and B blocking oscillators are triggered by signals from the A and B threshold detectors, respectively. Coincident A and B signals trigger the $A \cdot B$ blocking oscillator, and its output pulse is fed through 1.0 microsecond delay line to the $A \cdot B \cdot \overline{C}$ blocking oscillator. This blocking oscillator is disabled whenever the C blocking oscillator is

triggered. Thus, the $A \cdot B \cdot \overline{C}$ blocking oscillator fires whenever there is a signal on channel A coincident with one on channel B, but no signal on channel C.

The $A \cdot B \cdot \overline{C}$ signal triggers the $A \cdot B \cdot \overline{C} \cdot \overline{F}$ blocking oscillator only when the busy bistable is in the RESET condition. A "5" microsecond pulse output from this blocking oscillator is fed to the driving transformer in the linear gate section (see drawing 62-103) to unblock the linear gates in channels A and B.

ELECTRONICS PACKAGING AND INTERCONNECTIONS

Electronics Card S-74/EE1

Electronics card S-74/EE1 consists of 44 welded circuit modules mounted on six interconnecting sub-matrices which are themselves interconnected by means of a welded "mother matrix." An interconnection schematic of modules on this card is shown in drawing No. GD-S74-1008-263, "IMP E vs dE/dx (Nuclear Abundance Experiment) Electronic Card S-74/EE1, Schematic Diagram Sheet 1. Schematics of the separate modules are shown on sheet 2 and sheet 3 of the same drawing. Distribution of welded circuit modules on the interconnecting sub-matrices and drawing numbers for the sub-matrix interconnection diagrams are given in Table 2.

TABLE 2

Electronics Card S-74/EE1
Interconnecting Sub-Matrices

Sub Matrix Number	Welded Circuit Modules on Sub Matrix (See EE1 Schematic for Module Identification)	Sub Matrix Interconnection Diagram Code 672 Drawing No.
1	A_1, A_{2a}, A_{2b}, A_3 B_1, B_{2a}, B_{2b}, B_3 Power decoupler PD-1	01-114-1A7-D-02
2	C_1, C_{2a}, C_{2b}, C_3, C_4, C_5 Power decoupler PD-2 Driver Transformer 01-616	01-114-2A7-C-02
3	A_{4a}, A_{4b}, A_5, A_6, A_8, A_9, A_{10}, A_{11}, A_{12} B_{4a}, B_{4b}, B_5, B_6, B_8, B_9, B_{10}, B_{11}, B_{12} .01 mfd Sweep Control Capacitor, Channel A, .01 mfd Sweep Control Capacitor, Channel B	01-114-3A7-D-02
4	A_{14}, A_{15} B_{14}, B_{15} Power Decoupler PD-3	01-114-4A7-D-02
5	E_5, E_8 D_1, D_2, D_3 Power decoupler PD-4	01-114-5A7-C-02
6	Mother Matrix	0-114-6A7-D-02
7	Power Decoupler PD-5	
	Interconnection of Shielded Leads	01-114-7A7-D-02 01-114-6A7b-D-02

Electronics Card S-74/EE2

Electronics card S-74/EE2 has the power converter PS-8 and 29 other welded circuit modules mounted on three welded interconnecting sub-matrices. An interconnection schematic of modules on this card is shown in drawing No. GD-S74-1008-266, "IMP E vs dE/dx (Nuclear Abundance Experiment) Electronics Card S-74/EE2 Schematic Diagram," sheet 1. Schematics of the separate modules are shown on sheet 2 of the same drawing. Distribution of welded circuit modules on the interconnecting sub-matrices and drawing numbers for sub-matrix interconnection diagrams are given in Table 3.

TABLE 3

Electronics Card S-74/EE2
Interconnecting Sub-Matrices

Sub Matrix Number	Welded Circuit Modules on Sub Matrix (See EE2 Schematic for Module Identification)	Sub Matrix Interconnection Diagram Code 672 Drawing No.
1	Power Converter PS-8 Manufactured by Matrix Research and Development Corp.	Matrix Drawing D-1407
2	Power Decoupler Module PD-7 (Mounted on Mother-Matrix)	01-103-1C1-A-02
3	A_{13}, B_{13}	01-104-2A4-D-02
4	A_{16}, A_{17}, A_{18}, E_1, E_4 B_{16}, B_{17}, B_{18}, E_2, E_5 C_6, C_7, C_8, E_3, E_8 D_4, D_5, D_6, D_7, D_8, D_9 Power Decoupler PD-6	01-104-4A4-A-02
5	F_1 (Mounted on Mother Matrix)	01-121-PL-B-02 01-104-3A4-C-02
	Mother Matrix	01-104-1A4-C-02

Interconnecting Cabling

The instrumentation and electronics of the E vs dE/dx experiment are interconnected by a cable harness and Cannon connectors as shown in drawing No. GD-S74-1008-107 "IMP, E vs dE/dx (Nuclear Abundance Experiment) Interconnection wiring Diagram."

APPENDIX I.

WELDED MODULES

Table 4 gives the quantity of each different welded circuit module located on electronics card S-74/EE1 and the Code 631.4 drawing number for each module schematic. Table 5 gives the same information for welded modules located on electronics card S-74/EE2.

TABLE 4

Welded Circuit Modules

Located on S-74/EE1

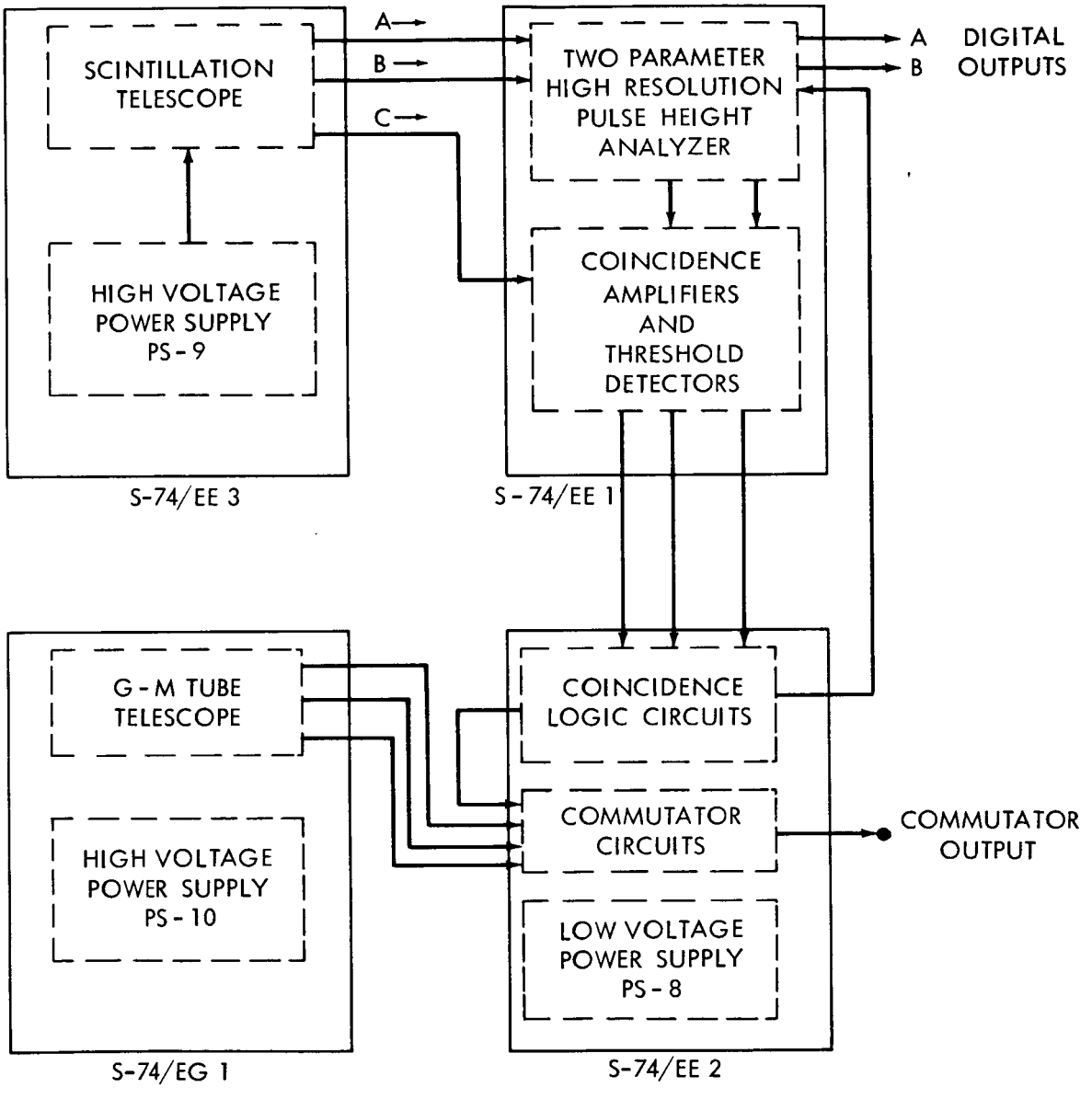
Welded Circuit Module	Quantity	Schematic Code 631.4 Drawing No.
Amplifier Type 1	3	62-45
Shaper, 2 Microsecond	3	62-42
Amplifier, Type 2A	13	62-6
Delay Line Coupler	2	62-89
Delay Lines, Artronic 26S		
2 Microseconds	3	
3 Microseconds	2	
Linear Gate	2	63-1
New Gate Driver (Transformer)	1	63-45
Sweep Circuit	2	62-61
Sweep Control	2	62-62
Shaper	2	62-63
Output Gate	2	62-64
Busy Bistable	1	62-58
By Pass Module	1	62-110
Trigger Delay	1	62-59
500 KC Oscillator	1	62-60
Power Decoupler PD-1	1	63-44
Power Decoupler PD-2	1	63-44
Power Decoupler PD-3	1	63-44
Power Decoupler PD-4	1	63-44
Power Decoupler PD-5	1	63-44

TABLE 5

Welded Circuit Modules

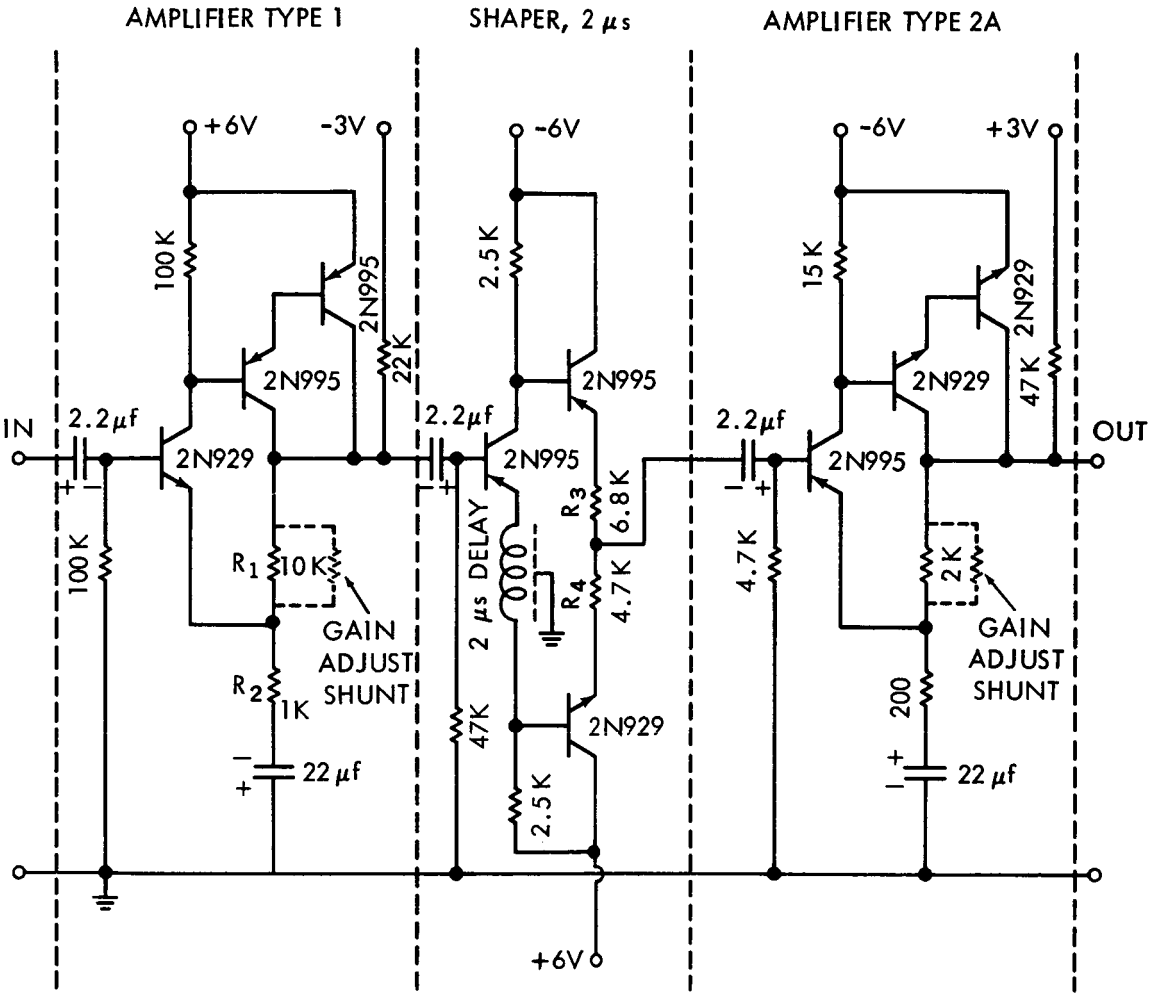
Located on S-74/EE2

Welded Circuit Module	Quantity	Schematic Code 631.4 Drawing No.	
Threshold Detector	3	62-7	
Emitter Follower	3	62-109	
Blocking Oscillator BO-1		62-19	
With Transformer T1-.75-12 (01-600)	2		
With Transformer T1-1-12 (01-601)	1		
With Transformer T1-2-12 (01-602)	1		
With Transformer T1-5-6 (01-603)			
Blocking Oscillator BO-2		62-20	
With Transformer T2-2-6 (01-604)	1		
Driver Type 1	2	62-77	
Driver Type 2	1	62-78	
Sync Shapers			
Type 1	1	62-79	(12-28-62)
Type 1A	1	62-79	(1-14-63)
Type 2	1	62-80	
Type 3	1	62-81	
Scaler, Single bit	3	62-82	
Matrix 8 position	1	62-83	
Delay Line, Artronic 26S, 1.0 Microsecond	1		
Modular Decoupler MD-1	6	62-18	
Power Decoupler PD-1	1	63-44	
Power Decoupler PD-2	1	63-44	

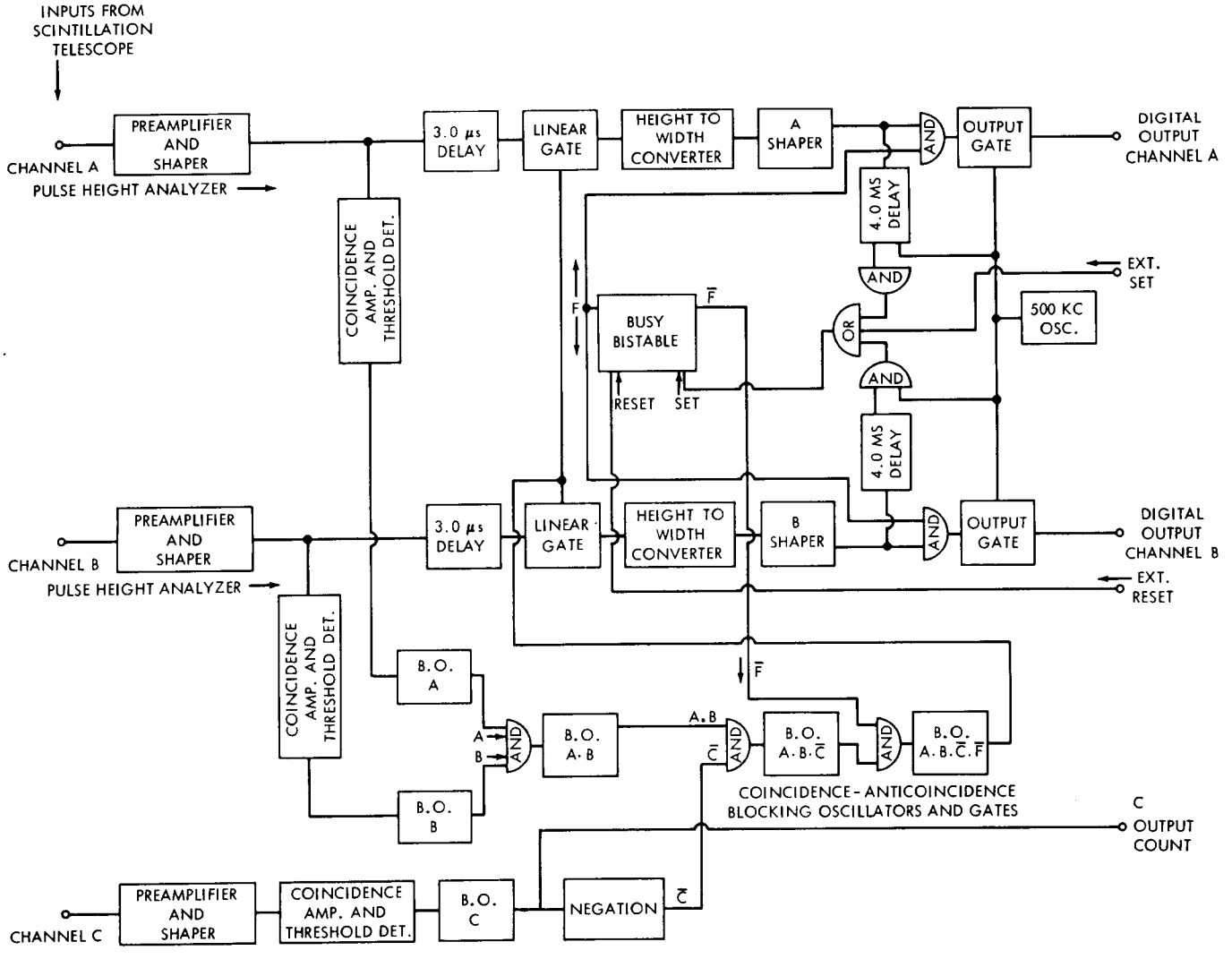


Signal Conditioning Electronics for the IMP E vs dE/dx Nuclear Abundance Experiment

631.4-62-109

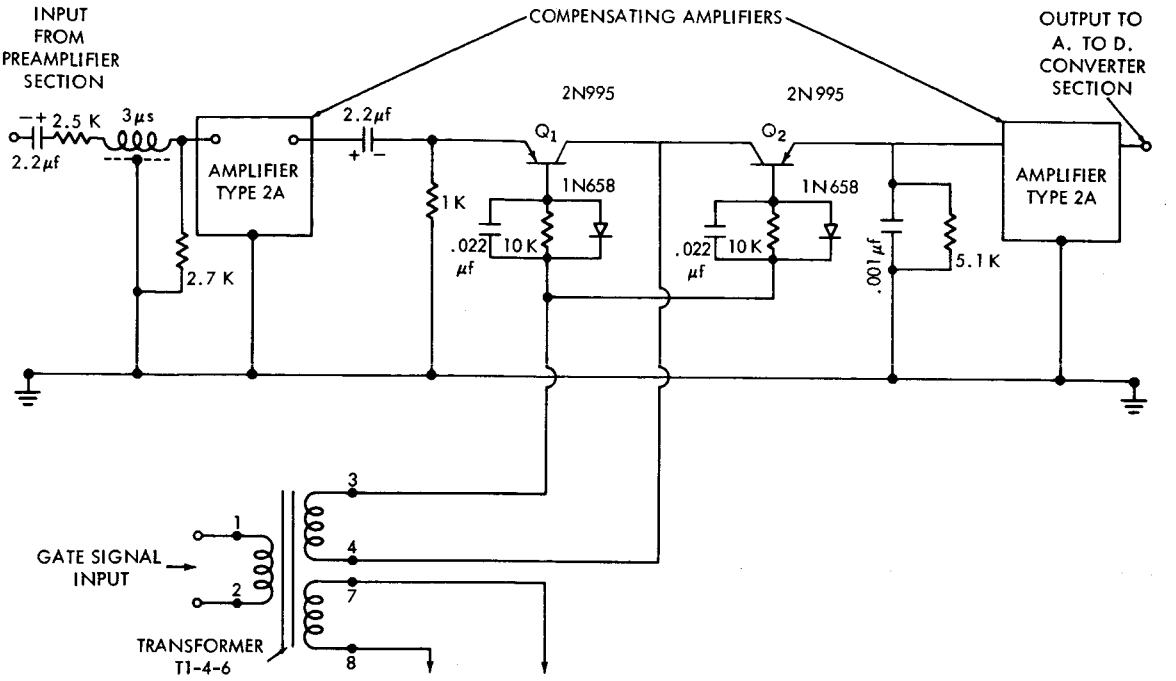


Preamplifier Section, Channels A, B, C
631.4-62-101



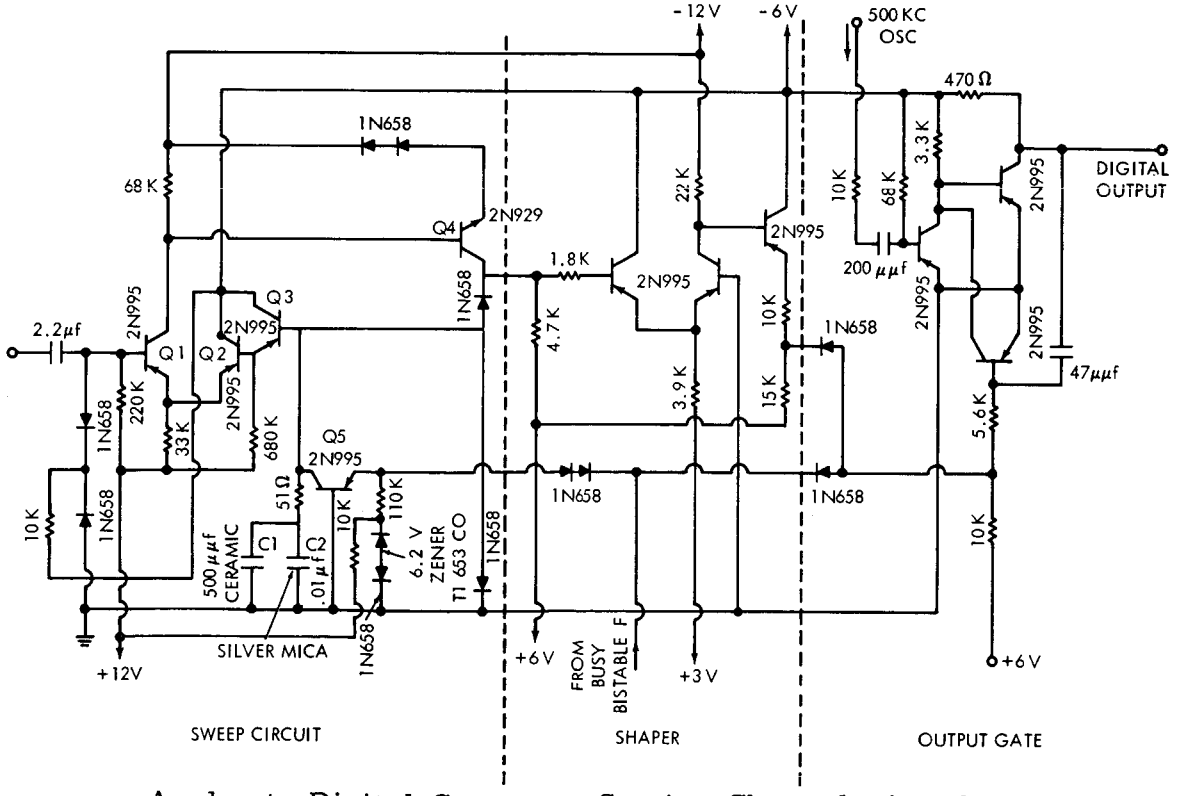
IMP Nuclear Abundance Experiment Pulse Height Analyzer Functional Block Diagram

631.4 - 62 - 84



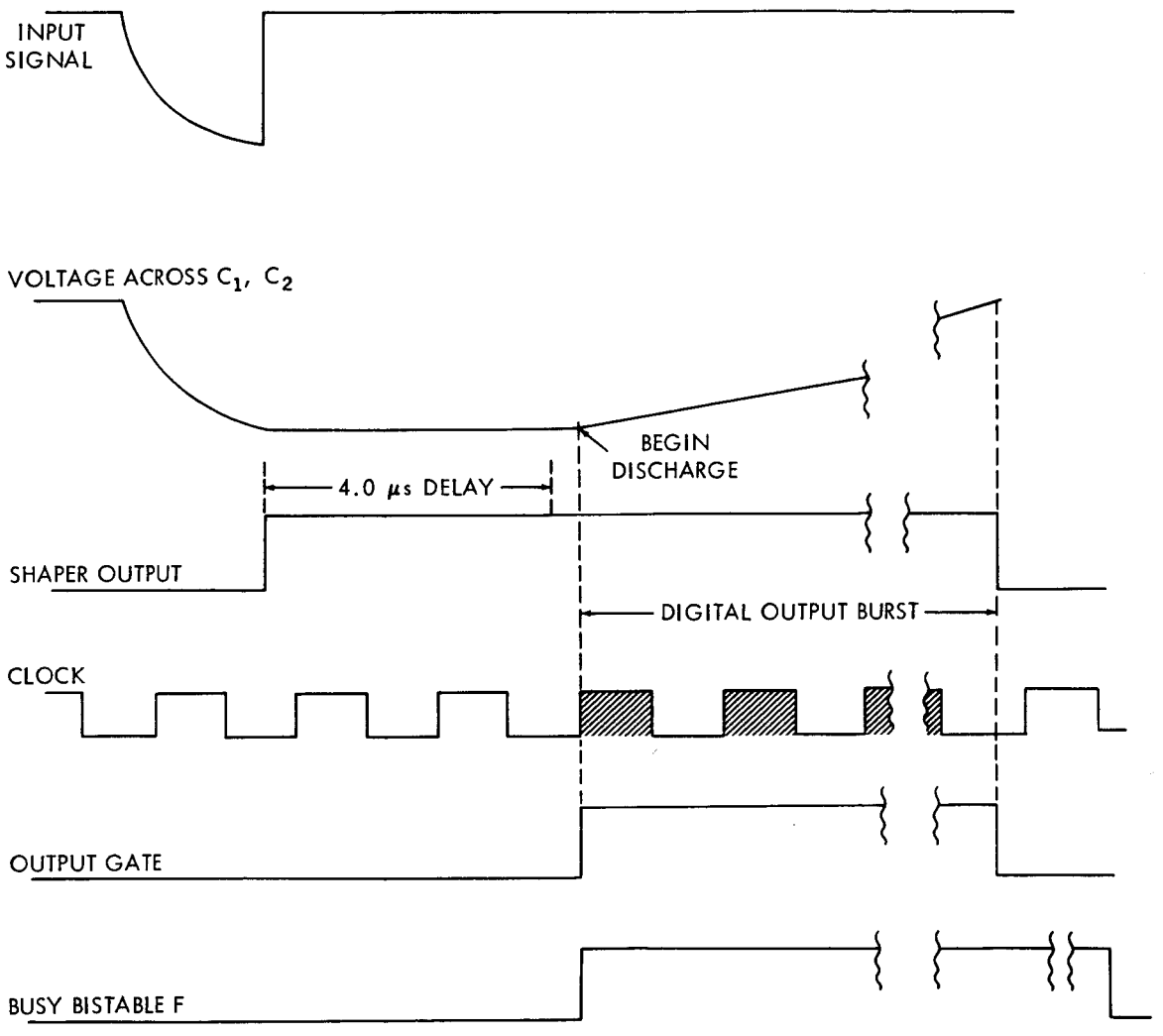
Linear Gate Section, Channels A and B

631.4-62-103

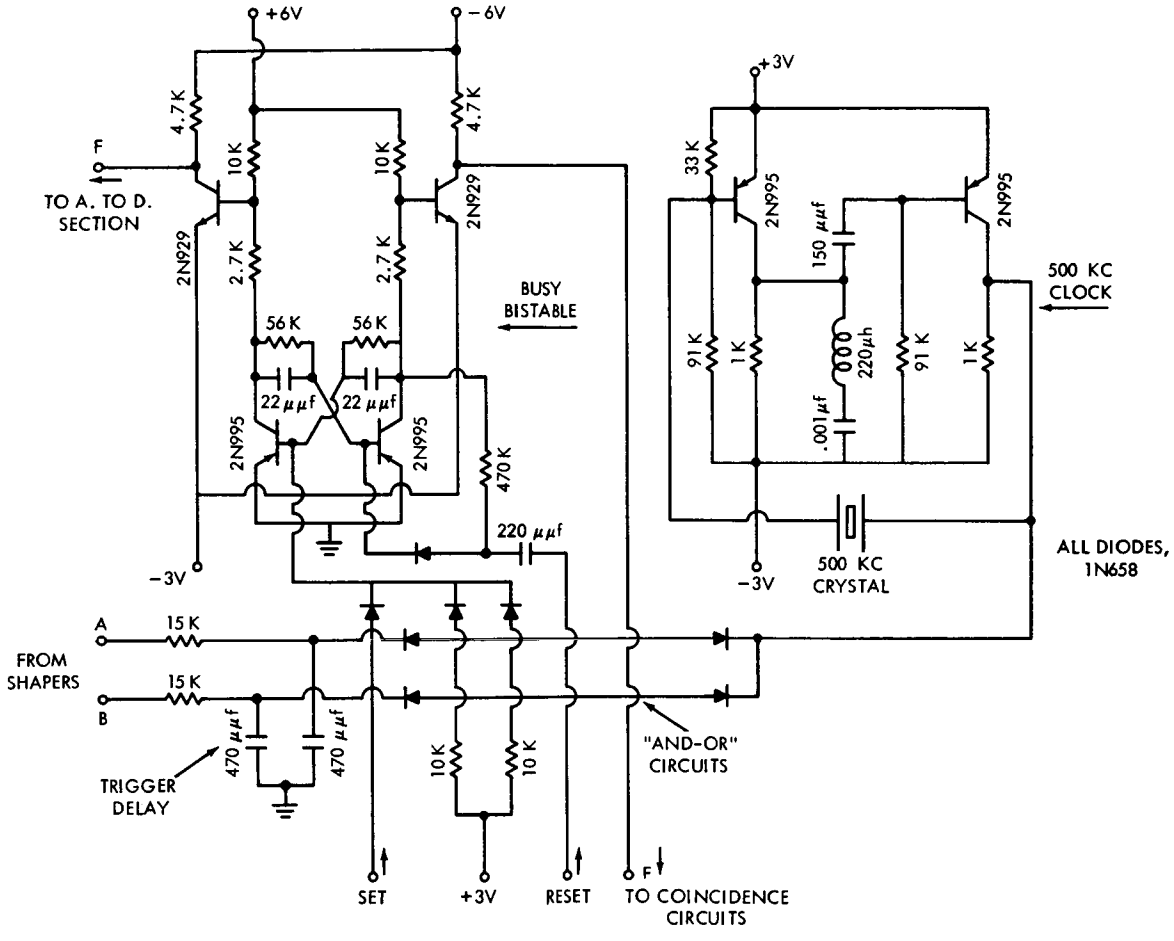


Analog to Digital Converter Section Channels A and B

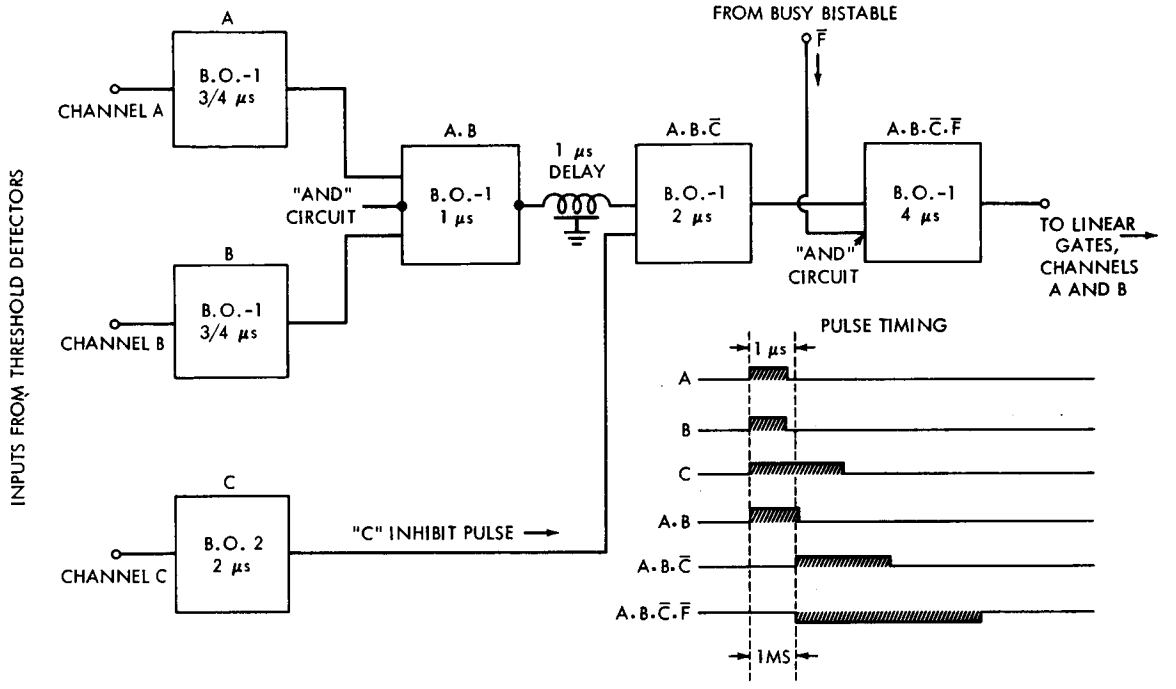
631.4-62-104



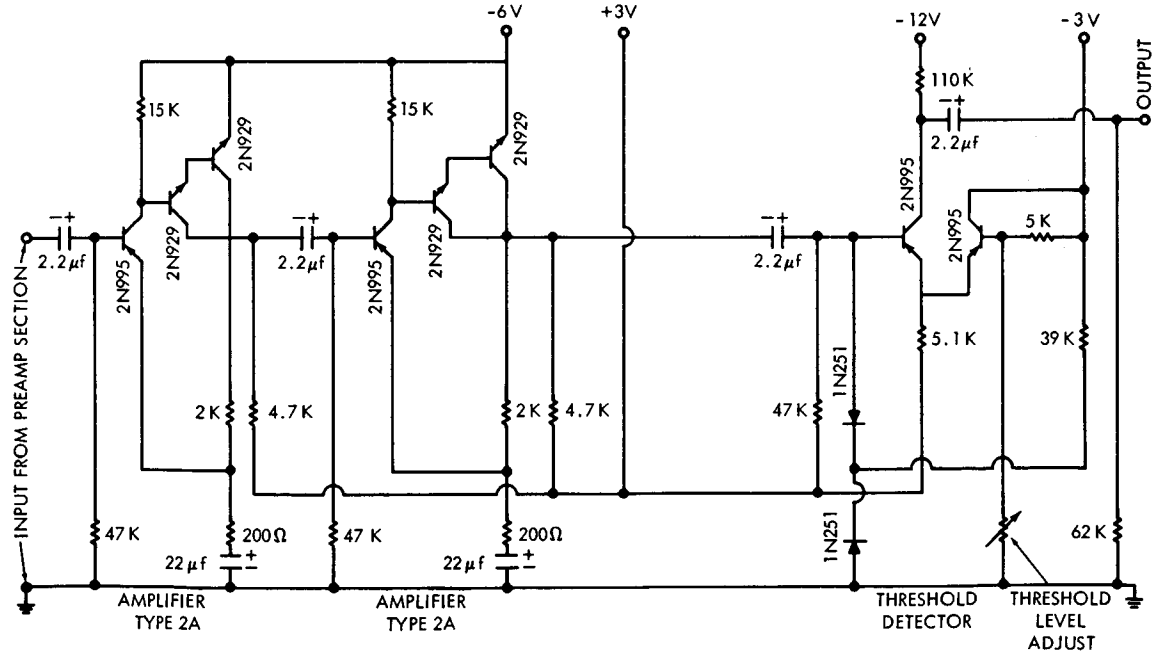
Analog To Digital Converter Operation
631.4-63-35



Busy Bistable and 500 KC Clock
631.4-62-105



Coincidence Circuit Logic E vs dE/dx Experiment, IMP
631.4-62-105



Coincidence Amplifiers and Threshold Detector Channels A, B, and C
631.4-62-102

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL

EE-1 NO.1 | EE-1 NO.2 | EE-1 NO.3 | EE-1 NO.4 | EE-1 NO.5 — POWER DECOUPLING MODULES

A1 AMP TYPE 1 — A IN FROM SCINT. TEL. — S2-8 — S2-7 A PREAMP OUT

A2b ARTRONIC 26S DELAY 2μs — A2a SHAPER 2μs

A3 AMP TYPE 2A

A4b ARTRONIC 26S DELAY 3μs — A4a DELAY LINE COUPLER

A5 AMP TYPE 2A

A6 TYPE 2 LINEAR GATE

A8 AMP TYPE 2A

A9 SWEEP CIRCUIT — A10 SWEEP CONTROL — SILVER MICA .01μf — S2-47 — S2-43

A11 SHAPER — A12 OUTPUT GATE — A OUT — P1-9 — S2-44 SET P1-30

D1 TRIG DELAY — D2 500KC. OSC — 500KC XTAL — 500KC — S2-49 — P1-10

S2-48

B1 AMP TYPE 1 — B IN FROM SCINT. TEL. — S2-6 — S2-5 B PREAMP OUT

B2b ARTRONIC 26S DELAY 2μs — B2a SHAPER 2μs

B3 AMP TYPE 2A

B4b ARTRONIC 26C DELAY 3μs — B4a DELAY LINE COUPLER

B5 AMP TYPE 2A

B6 TYPE 2 LINEAR GATE

B8 AMP TYPE 2A

B9 SWEEP CIRCUIT — B10 SWEEP CONTROL — SILVER MICA .01μf — S2-45

B11 SHAPER — B12 OUTPUT GATE — B OUT — P1-3

E8 BY PASS MODULE — E8 BUSY BISTABLE — P1-29 — P1-28

P1-26 A,B,C̄,F̄ IN

TRANSFORMER T1-4-6 ALADDIN 01-616 — OPEN WINDING — TP

P1-8 +12 — P1-6 +6 — P1-2 +3 — P1-4 +3 — P1-24 COMMON — P1-25 COMMON — P1-5 -3 — P1-1 -6 — P1-7 -12

COMMON

A14 AMP TYPE 2A — A15 AMP TYPE 2A

B14 AMP TYPE 2A — B15 AMP TYPE 2A

C1 AMP TYPE 1 — C IN FROM SCINT TEL — S2-4 — S2-3 C PREAMP OUT

C2b ARTRONIC 26S DELAY 2μs — C2a SHAPER 2μs

C3 AMP TYPE 2A

C4 AMP TYPE 2A

C5 AMP TYPE 2A

S2-40 COMMON — S2-38 — P1-27 RESET

A COIN OUT — P1-11 — P1-13

B COIN OUT — P1-12

C COIN OUT — P1-15

S2-13 COMMUTATOR POS. 1 — P1-22

S2-14 COMMUTATOR POS. 2 — P1-21

S2-15 ③ COMMUTATOR OUTPUT — P1-16

S2-16 1a — P1-17

S2-17 1b — P1-18

S2-35 2a — P1-19

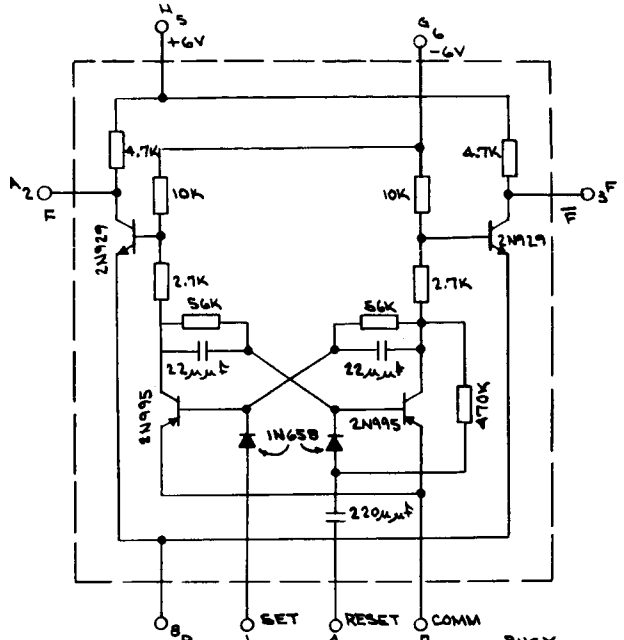
S2-37 2b — P1-20

CHASSIS GRD — P1-31

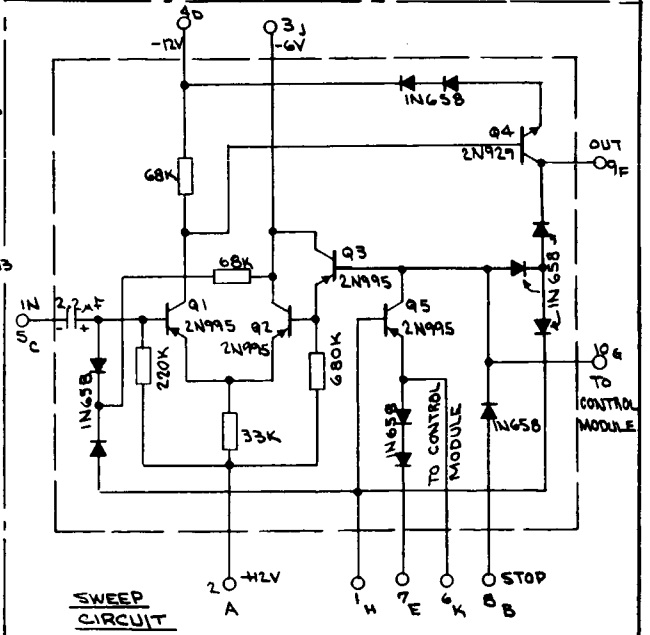
CHASSIS GRD — P1-32

CONNECTORS:
INTERCONNECTION: EE1-P1 DDM-36W-4P-NM(X)
TEST : EE1-S2 DDMF-50S-NM

BUSY BISTABLE



SWEEP CIRCUIT



EE1 REV. "B"

REQD	PART NO.	DESCRIPTION	MATL	MATL SPEC	UNIT WT.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS 1/64 DECIMALS ± .005 ANGLES ± 2°

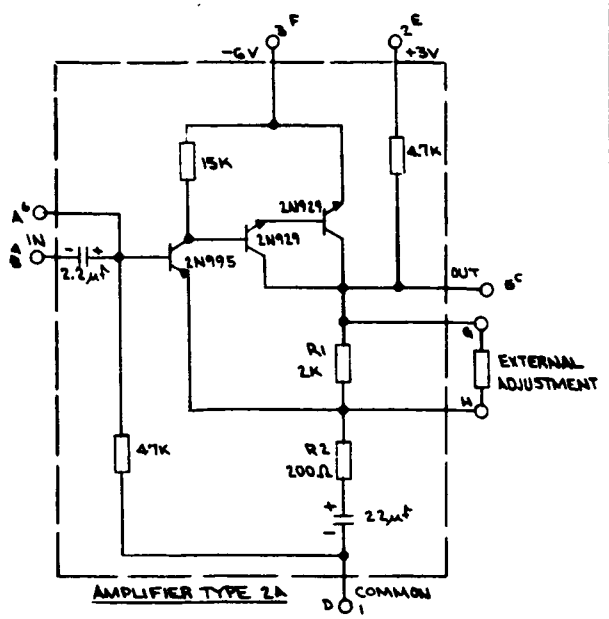
	NAME	INIT	DATE
DESIGNER			
DRAWN	WILLIAMS	JM	7-22-63
CHECKED			
APPROVED			
APPROVED			

1008-107
NEXT ASSY — USED ON

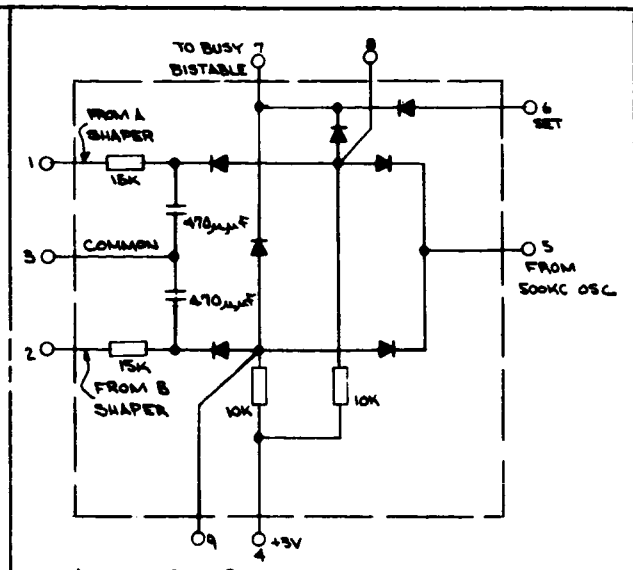
IMP
E vs dE/dx
NUCLEAR ABUNDANCE
ELECTRONICS CARD 1
S-74 EE1
SCHEMATIC DIAGRAM

SCALE — UNIT WT

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND
DRAWING NO.
GD-674-1008-263
CODE 672.2 SHEET 1 OF 3

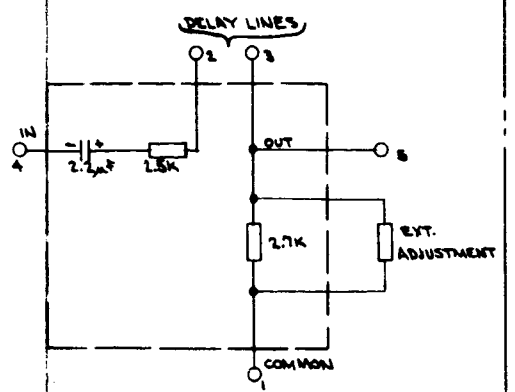


AMPLIFIER TYPE 2A

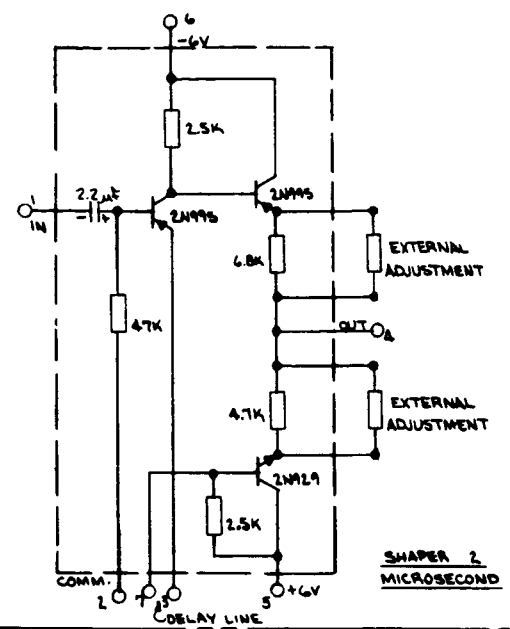


ALL DIODES 1N658

TRIGGER DELAY

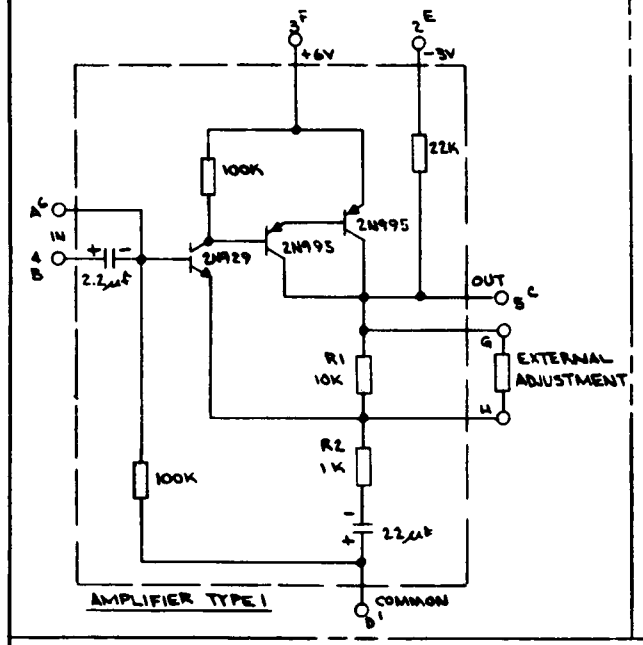


DELAY LINE COUPLER

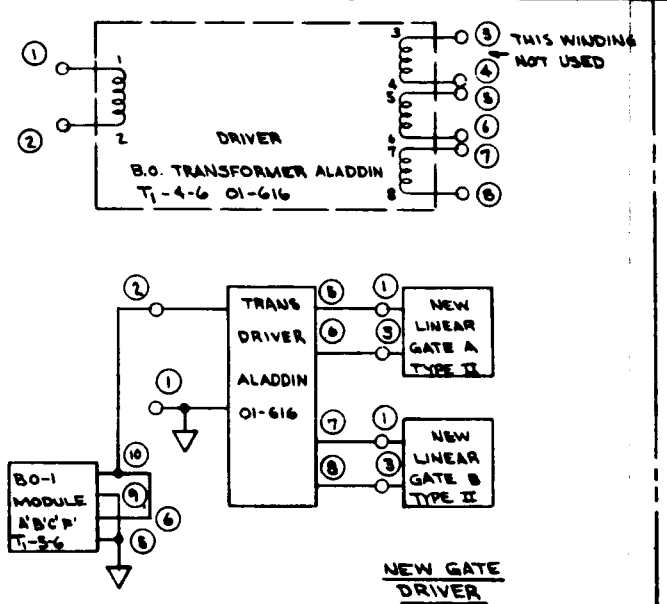


SHAPER 2 MICROSECOND

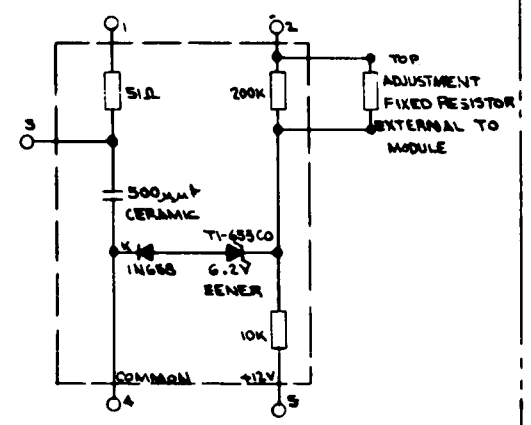
REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



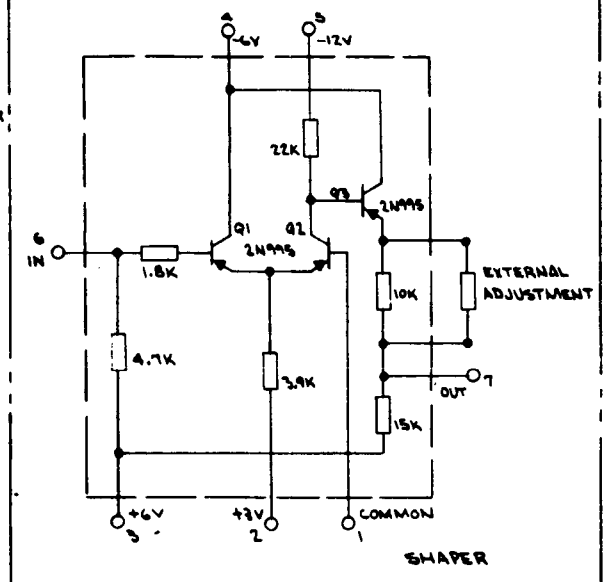
AMPLIFIER TYPE 1



NEW GATE DRIVER

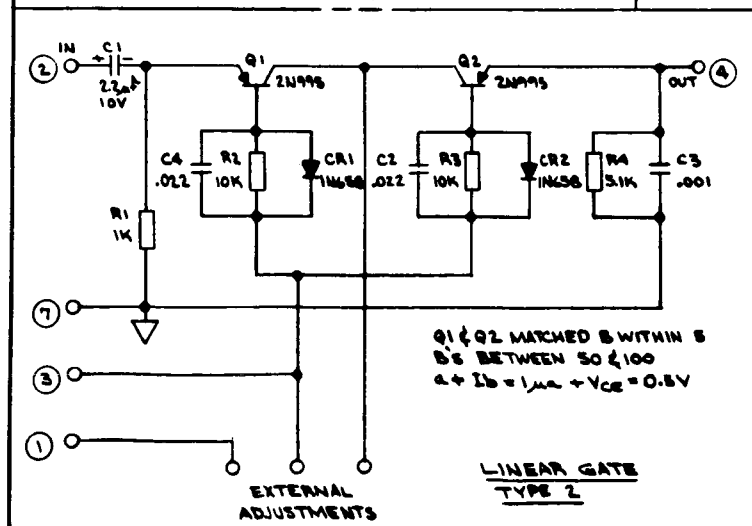


SWEEP CONTROL

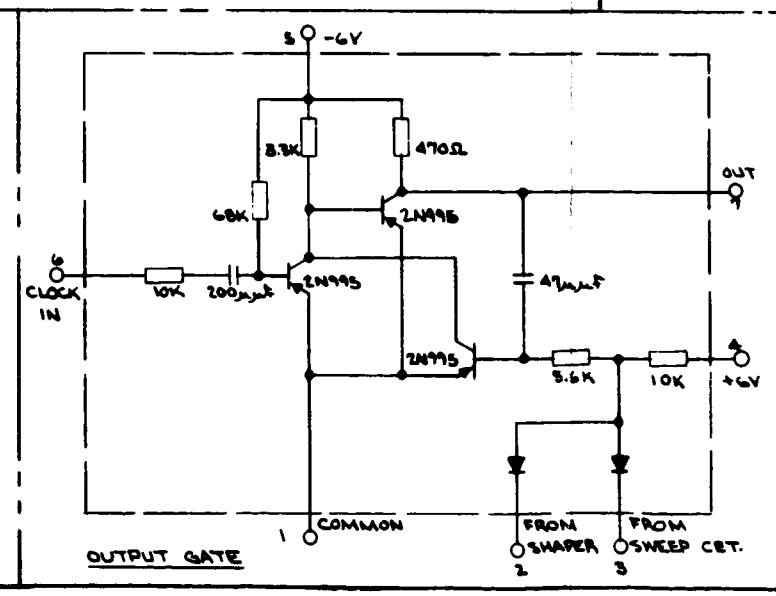


SHAPER

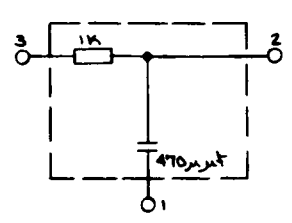
GD-574-1008-263
EE1 A



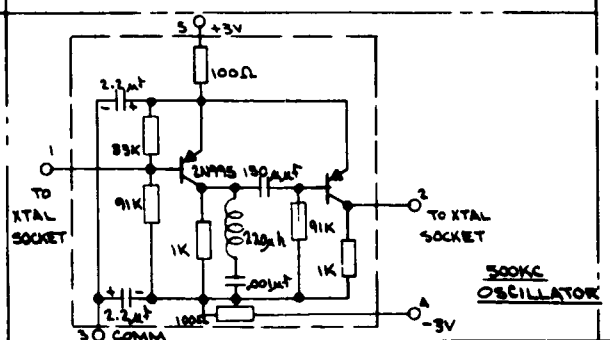
LINEAR GATE TYPE 2



OUTPUT GATE



BY-PASS MODULE



500KC OSCILLATOR

REQD	PART NO.	DESCRIPTION	MATL	MATL SPEC	UNIT WT.

LIST OF MATERIAL

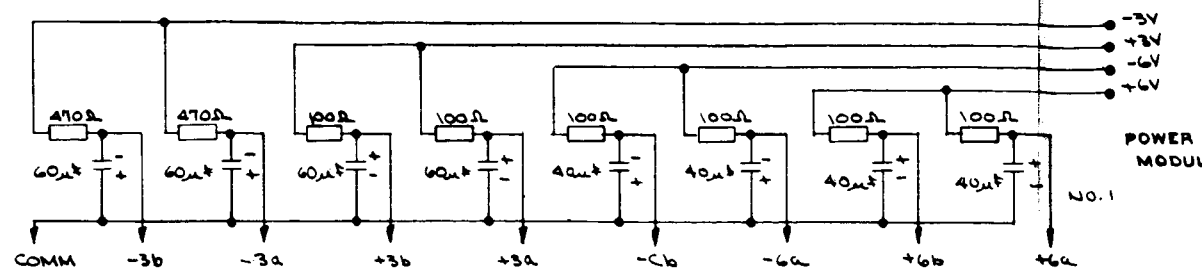
UNLESS OTHERWISE SPECIFIED	NAME	INIT	DATE
DIMENSIONS ARE IN INCHES	DESIGNER		
TOLERANCES ON:	DRAWN Mulvaney	J.L.M.	7-16-63
FRACTIONS 1/64 DECIMALS ± .005 ANGLES ± 2°	CHECKED		
	APPROVED		
1008-107	APPROVED		
NEXT ASSY	USED ON		

IMP
E vs dE/dx
(NUCLEAR ABUNDANCE)
S-74 EE1
ELECTRONICS CARD 1
SCHEMATIC DIAGRAM

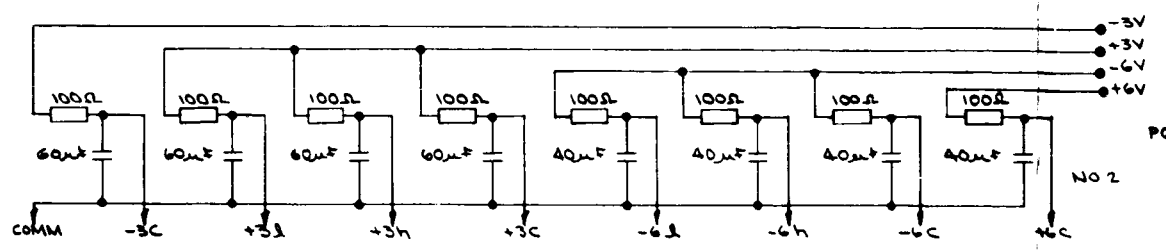
SCALE ~ UNIT WT

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND
DRAWING NO.
GD-574-1008-263
CODE 672.2 SHEET 2 OF 3

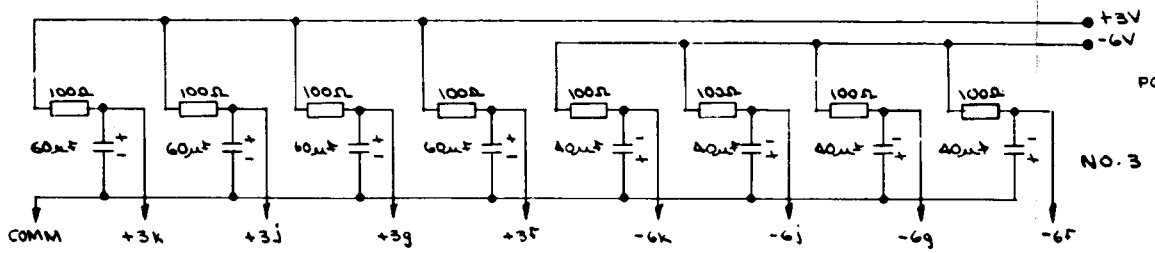
REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



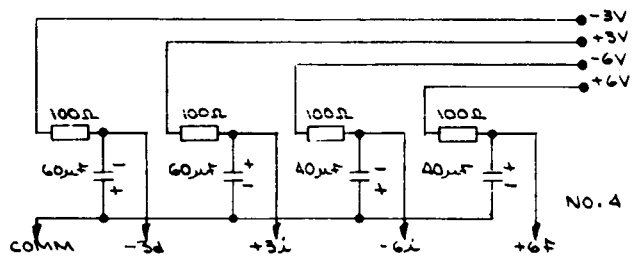
POWER DECOUPLING MODULE EE1



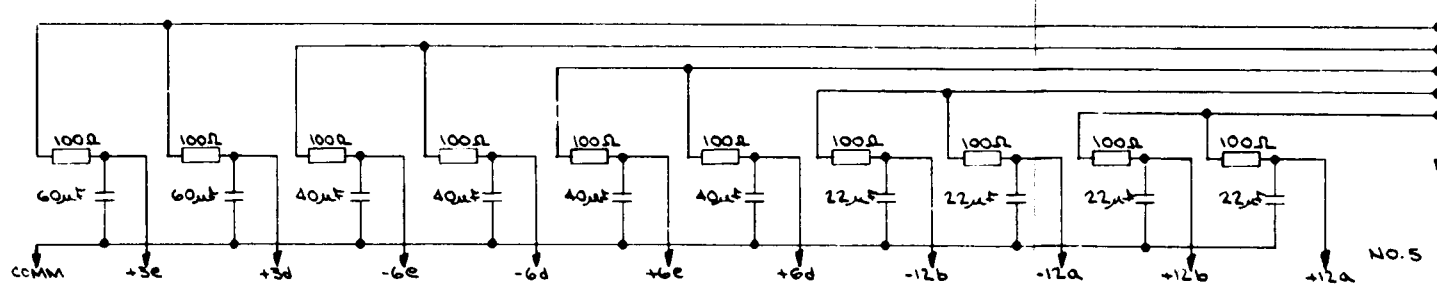
POWER DECOUPLING MODULE EE1



POWER DECOUPLING MODULE EE1



POWER DECOUPLING MODULE EE1



POWER DECOUPLING MODULE EE1

GDS74-1008-263
EE1 A

REQD	PART NO.	DESCRIPTION	MATL	MATL SPEC	UNIT WT.
		LIST OF MATERIAL			

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS 1/64 DECIMALS ± .005 ANGLES ± 2°

NAME	INIT	DATE
DESIGNER		
DRAWN MILLMAN	HM	8-7-63
CHECKED		
APPROVED		
APPROVED		

1008-107
NEXT ASSY | USED ON

IMP
E vs dE/dx
(NUCLEAR ABUNDANCE)
S-74 EE1
ELECTRONICS CARD 1
SCHEMATIC DIAGRAM
SCALE ~ | UNIT WT

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND
DRAWING NO.
GD-S74-1008-263
CODE 672 | SHEET 3 OF 3

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL

ARTRONIC 26S DELAY LINE 0.5 μs

A16 THRESH DET

A17 EMITTER FOLLOWER

A18 A BO-1 T1-.75-12

E1 A B BO-1-A T1-1-12

E2 IN OUT

CR1

10K

A·B RELAY

Z RELAY

A·B·C

F5 MATRIX 8 POSITION

F6 DRIVER TYPE 2

COMMUTATOR OUT

CHASSIS

COMMUTATOR POS 3

COMMUTATOR POS 1

COMMUTATOR POS 2

F TEST

1M

CR2

E4 A·B·C·F BO-1 T1-5-6

B16 THRESH DET

B17 EMITTER FOLLOWER

B B18 BO-1 T1-.75-12

MD-1 D4 D5 D6 D7 D8 D9

C6 THRESH DET.

C7 EMITTER FOLLOWER

C8 BO-2 T2-2-6

E3 BO-1 T1-2-12

F2 SCALER SINGLE BIT

F3 SCALER SINGLE BIT

F4 SCALER SIN BI

SCALER RESET

B13 DRIVER TYPE 1

A13 DRIVER TYPE 1

F1 TYPE 1A / TYPE 3 / TYPE 2 / TYPE 1

RESET

SET

POWER DECOUPLER EE2 No. 1

POWER DECOUPLER EE2 No. 2

PS-8

COMM

+12 IN

-12 IN

COMMON

+12V IN

-12V IN

ADVANCE

RESE TEST

RESET

P2	S1
P2-41	
P2-40	
P2-19	
P2-21	
P2-46	
P2-47	
P2-48	
P2-43	
P2-42	S
P2-44	A·B·C
	S1-5 X
	S1-3 Z
	S1-1 SUM
P2-45	A·B·C·F
	S1-28 A·B·C·F
	S1-7 F
	S1-11 B
	S1-9 C
	S1-17 A
	S1-15 B
	S1-30 RESET
	S1-32 SET
	S1-47
	S1-48
	S1-49
	S1-31
	S1-27
	S1-29
	S1-26
	S1-25
	S1-24
	S1-23
	S1-22
	S1-21
	S1-20
	S1-19
	S1-18
	S1-50
	S1-44
P2-9	
P2-39	
	S1-35
	S1-34
P2-23	
	S1-46
	S1-45
P2-27	
P2-38	
	S1-43 1a
P2-1	
P2-3	
	S1-42 1b
P2-16	$\bar{A}_2$
P2-25	ADVANCE F
P2-11	
P2-29	RESE TEST 2 F
P2-13	RESET
P2-15	$\bar{B}$ SET
	S1-41 2a
P2-5	
P2-7	
	S1-40 2b
P2-17	COMMON
P2-35	+12V IN
P2-34	
P2-37	-12V IN
P2-36	

GD-S74-1008-266
EE2 B

NOTES:
1. INTERCONNECTION CONN. EE2-S1 DDM-50S-NM(R)
   SPACECRAFT CONN. EE2-P1 DDM-50P-NM(R)
2. ALL CAPACITORS IN POWER DECOUPLERS ARE SPRAGUE TYPE 1500, CASE SIZE B.

REQD	PART NO.	DESCRIPTION	MATL	MATL SPEC	UNIT WT.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ±1/64 DECIMALS ± .005 ANGLES ± 2°

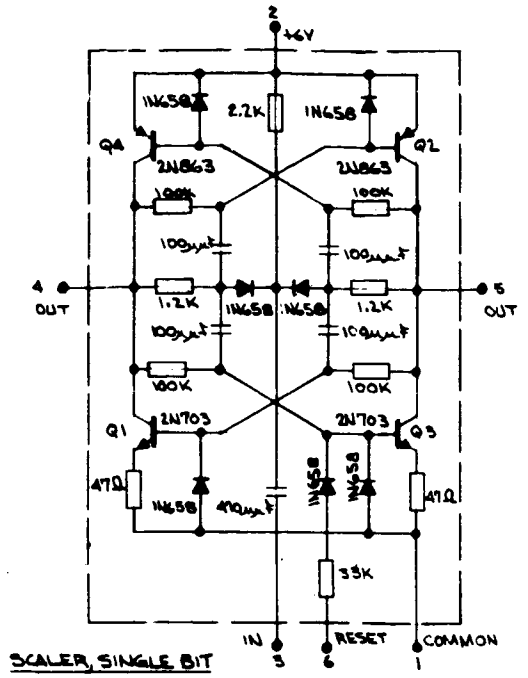
NAME	INIT	DATE
DESIGNER		
DRAWN MILLMAN		
CHECKED		
APPROVED		
APPROVED		

1008-107
NEXT ASSY | USED ON

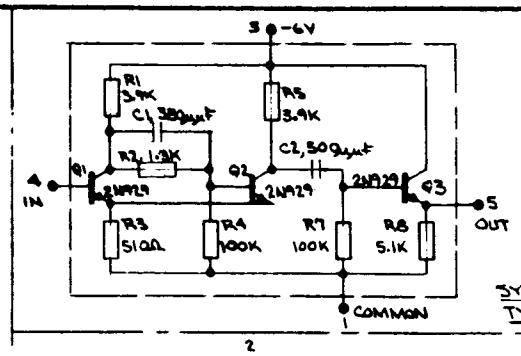
IMP
E vs dE/dx EXPERIMENT
(NUCLEAR ABUNDANCE)
ELECTRONICS CARD 2
5-74 EE2
SCHEMATIC DAGRAM

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND
DRAWING NO.
GD-S74-1008-266

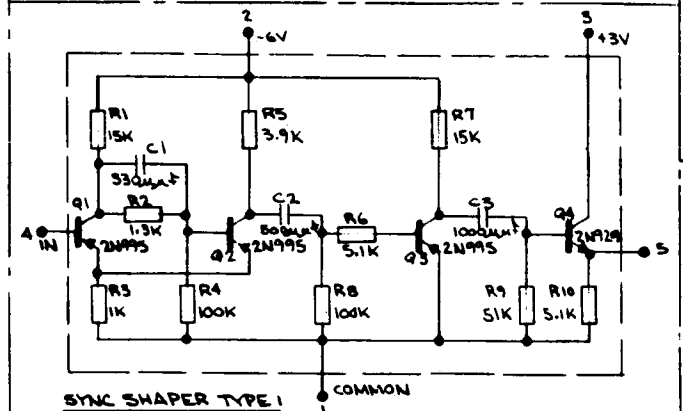
SCALE ~ | UNIT WT | CODE 612 | SHEET 1 OF 2



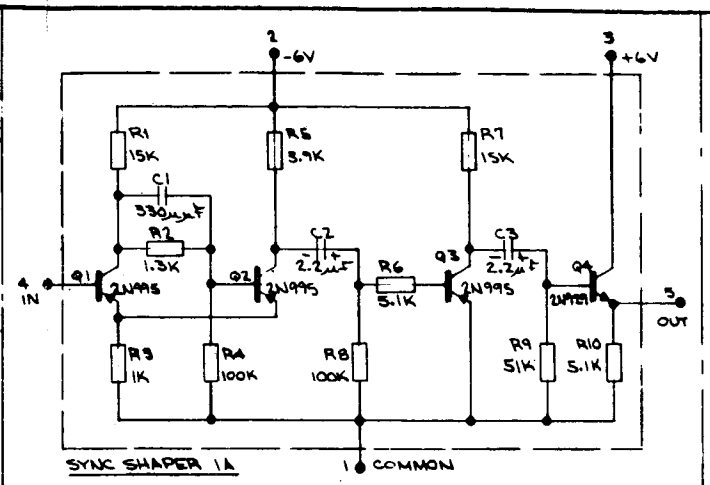
SCALER, SINGLE BIT



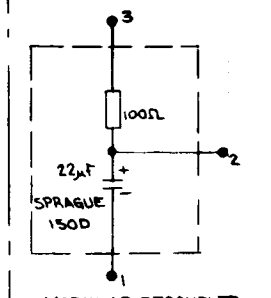
SYNC SHAPER TYPE 2



SYNC SHAPER TYPE 1

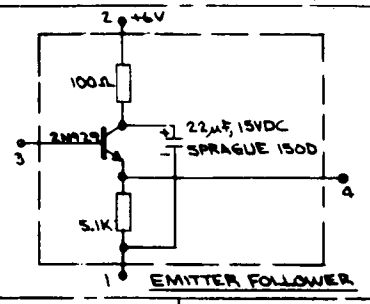


SYNC SHAPER 1A

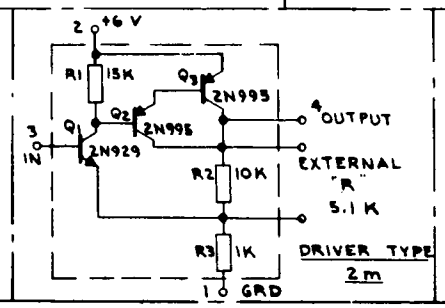


MODULAR DECOUPLER MD-1

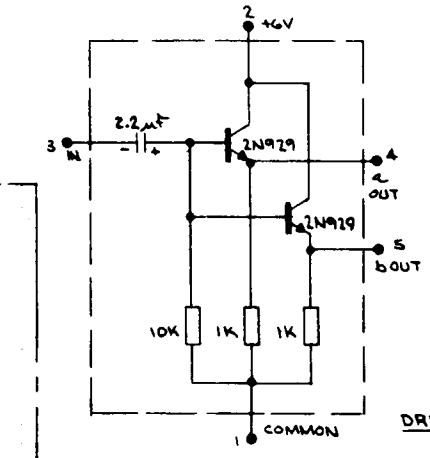
REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



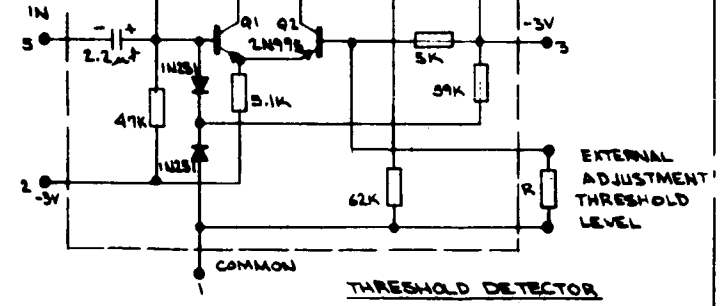
EMITTER FOLLOWER



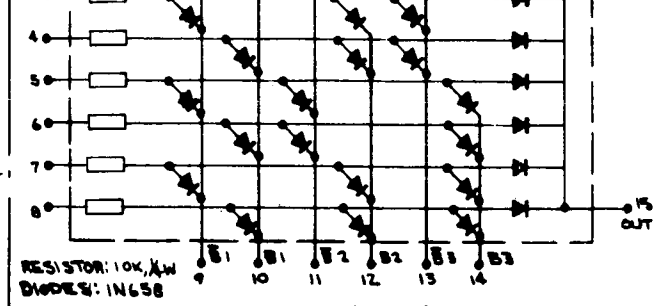
DRIVER TYPE 2m



DRIVER TYPE 1

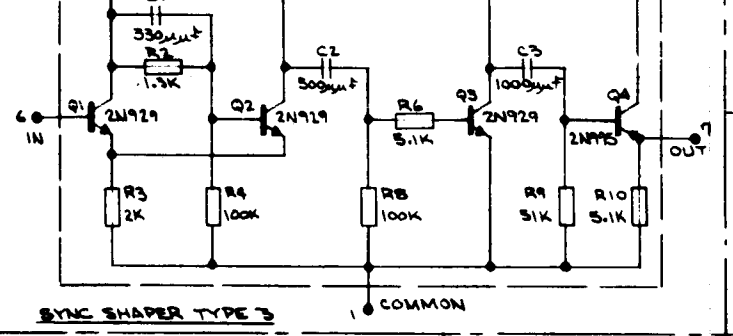


THRESHOLD DETECTOR



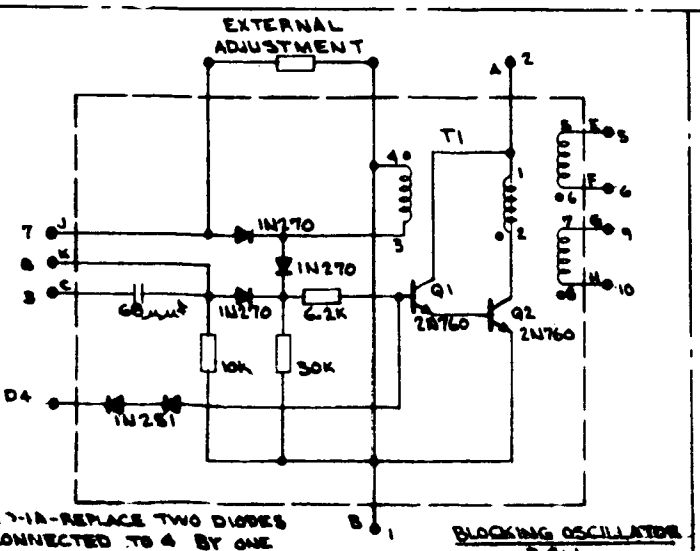
RESISTOR: 10K, ¼W
DIODES: IN658

MATRIX, 8 POSITION



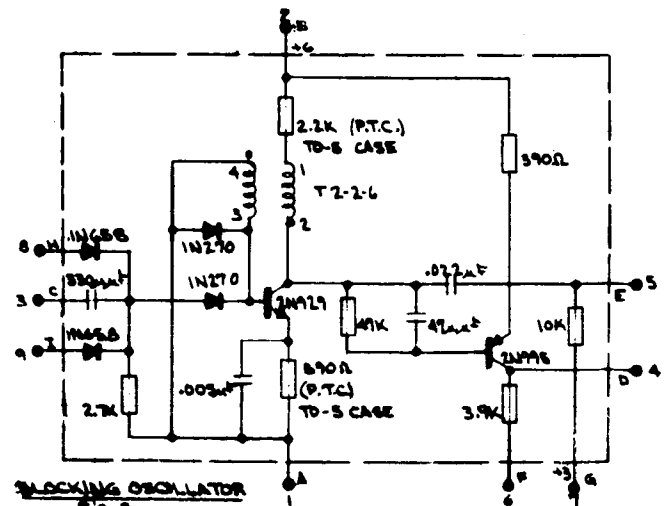
SYNC SHAPER TYPE 3

GD-S74-1008-266
EE 2 B



E7-1A-REPLACE TWO DIODES CONNECTED TO 4 BY ONE IN270

BLOCKING OSCILLATOR BO-1



BLOCKING OSCILLATOR BO-2

MODEL	PART NO.	DESCRIPTION	MATL	MATL SPEC	UNIT QT.

LIST OF MATERIAL

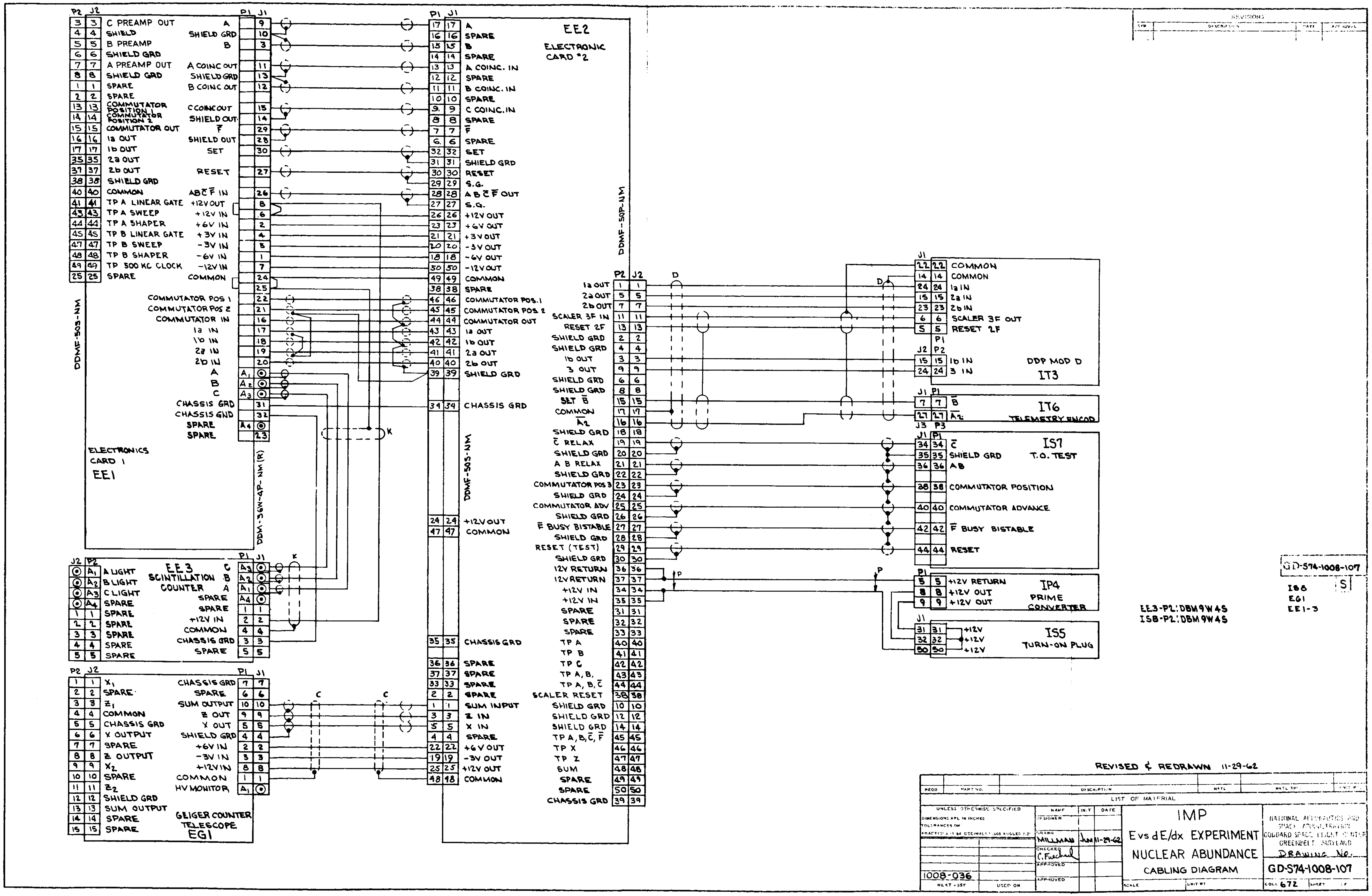
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS ±1/64 DECIMALS ± .005 ANGLES ± 1°

1008-107
NEXT ASSY | USED ON

NAME	INIT	DATE
DESIGNED		
DRAWN	MILLMAN	4-18-63
CHECKED		
APPROVED		
APPROVED		

IMP
E vs dE/dx EXPERIMENT
(NUCLEAR ABUNDANCE)
ELECTRONICS CARD 2
S-74 EE2
SCHEMATIC DIAGRAM
SCALE ~ | SHEET SIZE

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND
Drawing No
GD-S74-1008-266
MODEL 472 | SHEET 2 OF 2


ELECTRONICS CARD 1
EE1
DDMF-50S-NM
DDM-36W-4P-NM (R)
EE2
ELECTRONIC CARD #2
DDMF-50P-NM
DDMF-50S-NM
EE3
SCINTILLATION COUNTER
GEIGER COUNTER TELESCOPE
EG1
DDP MOD D
IT3
IT6
TELEMETRY ENCOD
IS7
T.O. TEST
IP4
PRIME CONVERTER
IS5
TURN-ON PLUG
EE3-P2: DBM9W4S
IS8-P2: DBM9W4S
GD-S74-1008-107
IS8
EG1
EE1-3
REVISED & REDRAWN 11-29-62
REVISIONS
LIST OF MATERIAL
IMP
E vs dE/dx EXPERIMENT
NUCLEAR ABUNDANCE
CABLING DIAGRAM
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND
DRAWING No.
GD-S74-1008-107
1008-036
MILLMAN
11-29-62
C. Fuechsel
672

G.S.F.C. 207