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THE EPE-D TWO YEAR TIMER

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NASA — GODDARD SPACE FLIGHT CENTER

GREENBELT, MARYLAND

THE EPE-D
TWO YEAR TIMER

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TABLE OF CONTENTS

FOREWORD

This document is intended for general descriptive purposes only. It is a guide for those who need or wish to know the general circuitry and the specific functional operation of the Two Year Timer in relation to the spacecraft during testing and flight. No attempt has been made to present detailed theoretical or circuit analysis.

SUMMARY

A solid state timing system used to disconnect the solar cells from the batteries after an interval of two years is described. The basic timing principle is discussed, as well as the circuits used to provide telemetry monitoring of the timing system performance. The circuitry for providing blockhouse testing and monitoring of the system is shown, along with an explanation of the precautions taken to isolate the test circuitry from the actual timing system after testing. Examples and the interpretation of the information received during testing are given. Finally, expected telemetry monitor readout during the complete two year period is tabulated.

AUTHOR

GENERAL FUNCTION AND DESCRIPTION

The mission of the EPE-D Two Year Timer is to disable the payload so that transmissions will cease after a period of approximately 2 years from launch. This is accomplished by opening normally-closed magnetic latch-relay contacts which connect the solar cell panel and the battery. The timer consists of two identical, parallel, timing circuits which independently operate two latch relays. Connections are made to the relays such that both relays are required to operate before the solar cells are disconnected from the battery.

BASIC TIMING CIRCUIT OPERATION

A block diagram of the basic timing circuitry is shown in Figure 1. The power for the circuitry is obtained through a voltage regulator operating directly from the spacecraft +19.6 volts battery line. The timing pulses are derived from a unijunction transistor acting as a relaxation oscillator. The pulse output of the unijunction is amplified before entering the magnetic core divider. An output from the divider occurs after 20×10^6 inputs. This output pulse then fires a silicon controlled rectifier, used as a power pulse-former, which in turn energizes a magnetic latch relay. Figure 2 shows this basic timing circuitry in a schematic diagram.

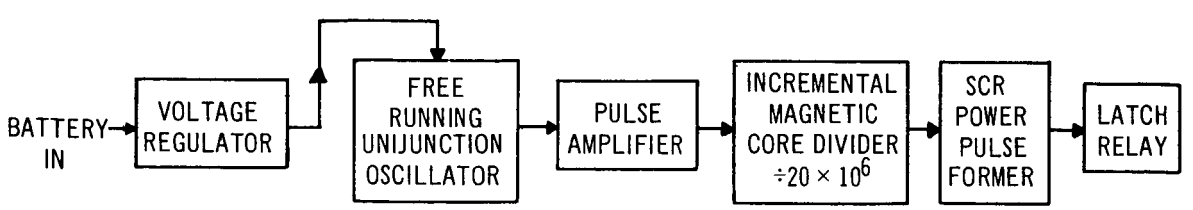

Figure 1-Block Diagram of Basic Timing Circuit EPE-D

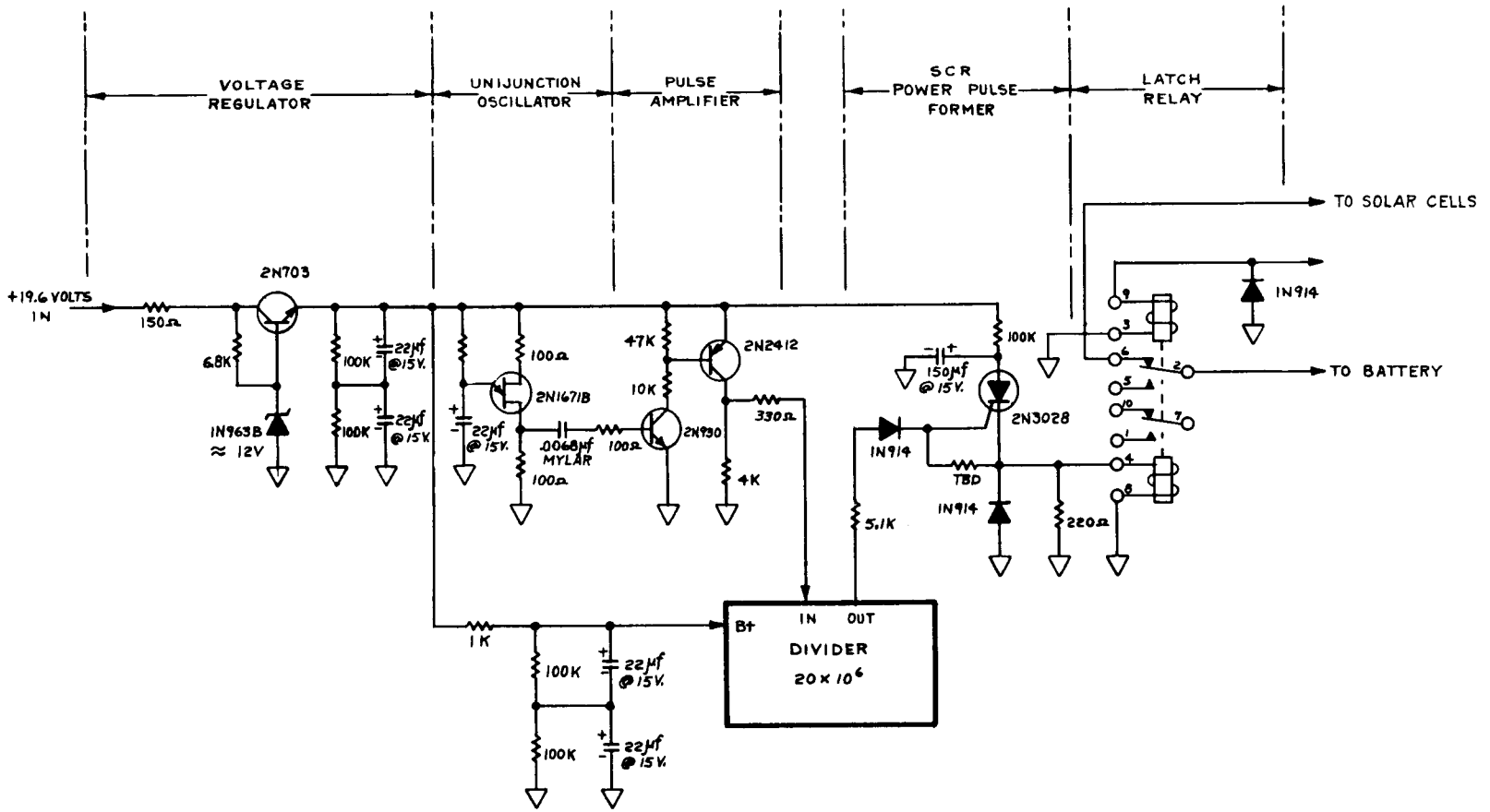

Figure 2-Schematic Diagram Basic Timing Circuit EPE-D

Figure 3 shows two basic timing circuits connected to form the Two Year Timer. The two timing circuits are completely independent except at the battery power input.

TELEMETRY MONITOR

Figure 4 is a block diagram showing the operation of the telemetry monitor incorporated into the timer units as well as the relay wiring. The monitor is a flip-flop which operates from certain intermediate outputs of the core dividers and which acts to provide a shunt to ground to a section of a voltage divider network in the encoder. This divider network then furnishes voltage to a voltage controlled oscillator whose frequency is sampled and transmitted in the telemetry information.

Figure 5 depicts the operation of the telemetry monitor flip-flop upon the voltage divider network in the encoder. Either the 36 day pulses from timer A or the 39 day pulses from Timer B will operate the flip-flop of Q7 and Q9. Q8 of this flip-flop in turn causes Q10 to be on or off and hence short the 10K encoder resistor to ground or leave it open. This operation persists for 720 days. At this time, Relay A is actuated and the resistor R_A is connected in series with the 10K encoder resistor. The operation of Q10 and the flip-flop remain the same. The other contact of Relay A, acting as one of the parallel Solar Cell-Battery Connect switches, is also opened at this time.

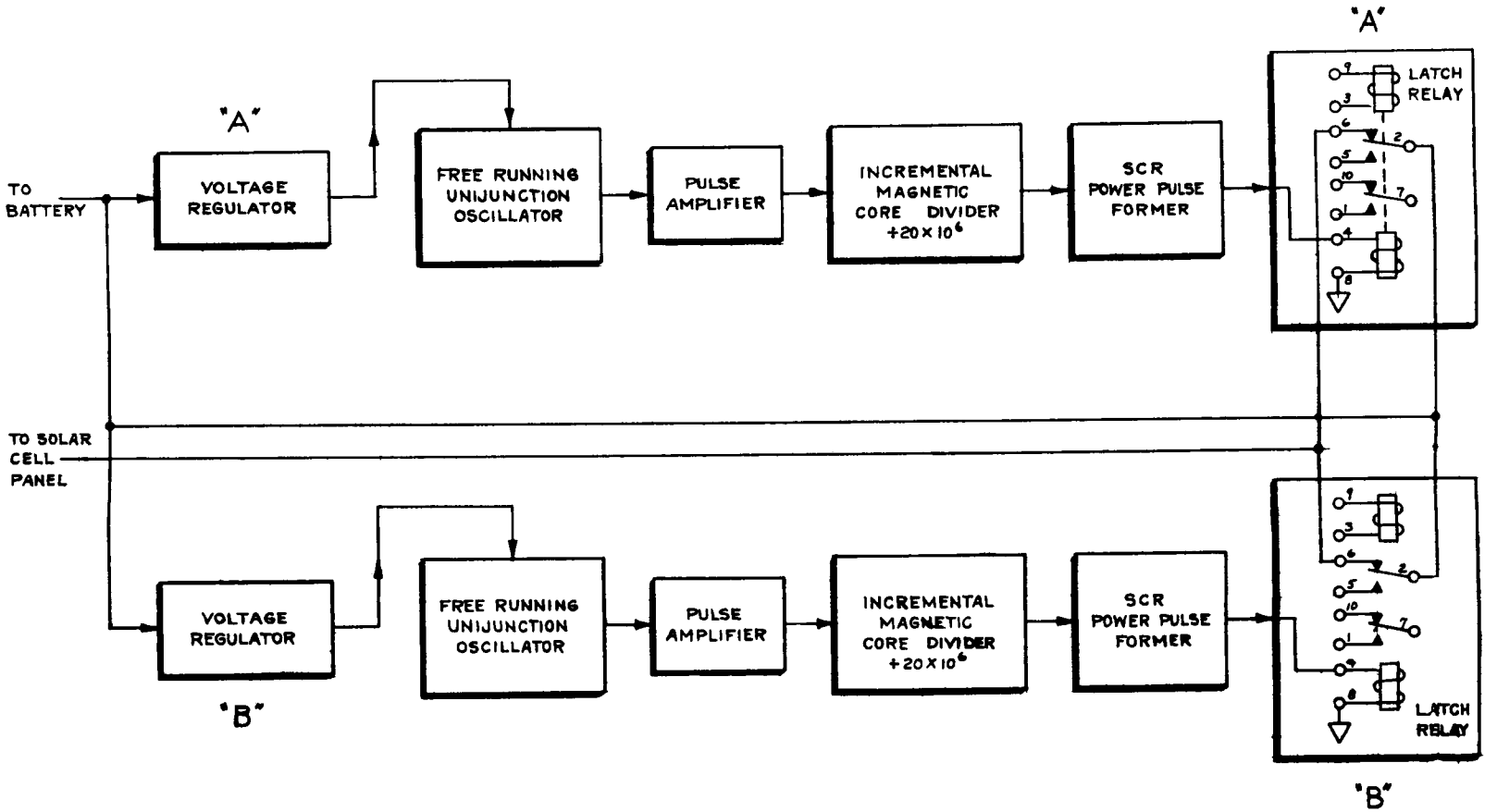

Figure 3-Block Diagram Basic Parallel Timers Showing Redundant Relay Circuit EPE-D

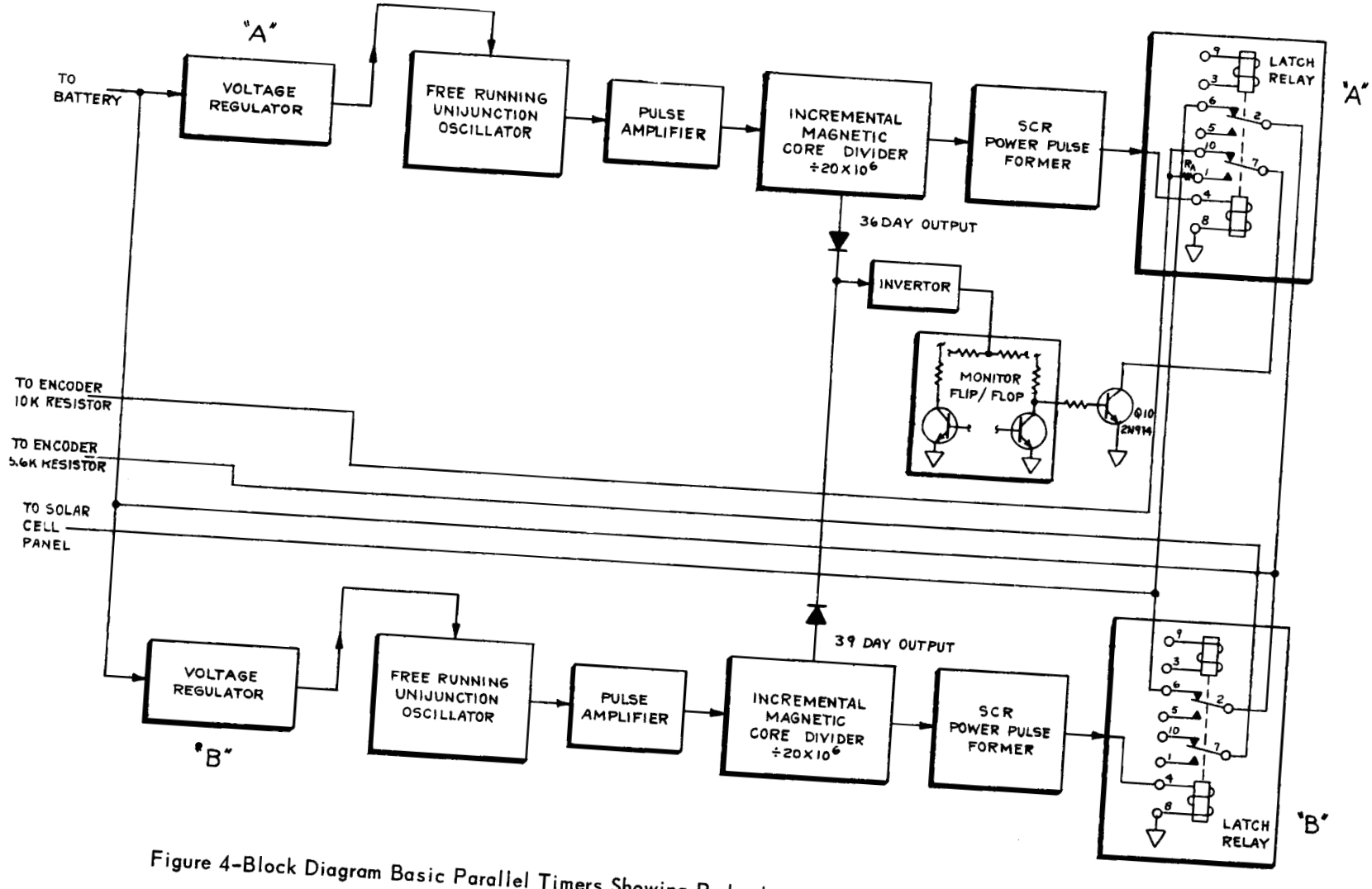

Figure 4-Block Diagram Basic Parallel Timers Showing Redundant & Telementry Monitor Circuits EPE-D

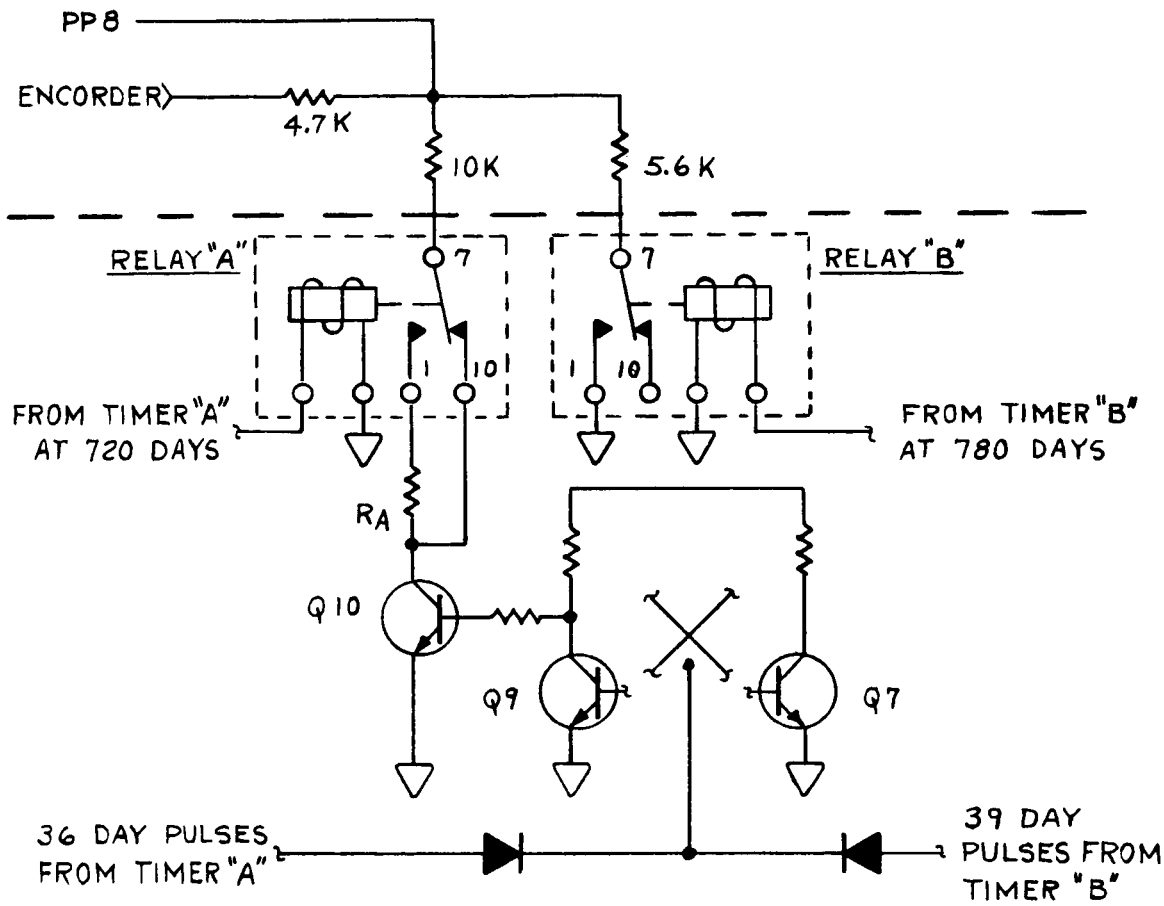

Figure 5-Two Year Timer Switching Sequence EPE-D

At T=780 days, Relay B is actuated. With this, the 5.6K encoder resistor is connected to ground through one set of the relay contacts. The other set opens the remaining Solar Cell-Battery Connect switch and completes the disconnect of the Solar Cells and Battery. When this occurs, the life of the spacecraft depends solely upon the remaining capacity of the battery.

Table I summarizes the switching sequence of the Timer. The column labeled Resistance Switching is merely a list of the switching sequence of the resistors in the encoder voltage level network. The column labeled Voltage Level Switching refers to the curves shown in Figure 6. The reference voltage of the divider network in the encoder is derived from the -17.8 volt bus. Therefore, monitoring performance parameter 8 of the encoder sequence and comparing it to a calibration curve will give information concerning the -17.8 volt has as well as the condition and operation of the Two Year Timer Unit.

TABLE 1

Time	Resistance Switching Figure 5	Voltage Level Switching Figure 6	Relay "A"	Relay "B"
T = 0 to T = 720 days	Open to 10K	1 to 3	Closed	Closed
T = 720 days to T = 780 days	Open to $10K + R_A$	1 to 2	Open	Closed
T = 780 days to batt. death ($\approx$ 2 – 3 hours)	5.6K to $\frac{5.6K\,(10K + R_A)}{5.6K + 10K + R_A}$	4 to 5	Closed	Closed

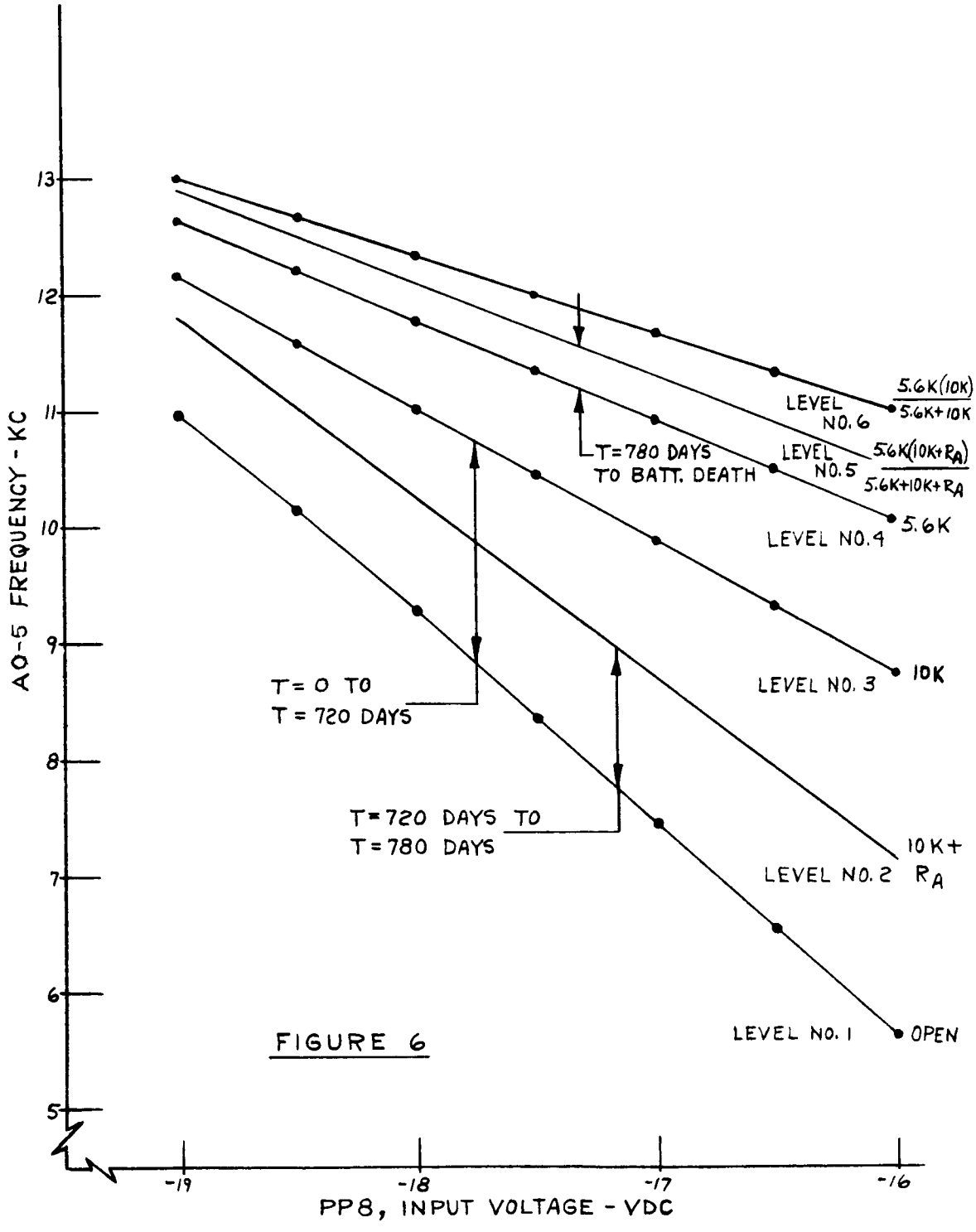

FIGURE 6

Figure 6-Encoder Divider Resistance

SPEED-UP AND CABLE DRIVER OPERATION

Figure 7 is a block diagram of the auxiliary speed-up and cable driver circuitry provided for testing. This auxiliary circuitry is isolated from the timing circuit by diodes and resistors and uses separate power from the blockhouse. Therefore the timing circuitry is protected from any possible failures due to the auxiliary circuitry. The cable driver is a pulse stretcher and amplifier for monitoring the normal rate of the oscillator and the functioning of the pulseformer section of the magnetic core divider. The pulse outputs from the cable driver from both timing circuits are diode coupled and fed through the Normal Rate line to the blockhouse. The speed up rate for the timer is derived from a separate oscillator whose output is coupled into the pulse amplifier preceding the divider. Upon completion of the timing cycle at speed-up rate, the output of the SCR operating the relay fires a SCR which shunts the speed-up oscillator power to ground. The shunt SCR will stay on until the speed-up power is released. This operation insures that the timer does not pass the T_0 position of the timing cycle at the accelerated rate.

DATA INTERPRETATION

Figure 8 shows the telemetry indication of the operation of the timer for the full two year interval. The indications are based on idealized timing oscillator function, that is, no error in accuracy or stability. Figure 8 also assumes that the telemetry monitor flip-flop is in such a position that the telemetry indication is at Level 1 at time T_0. (See

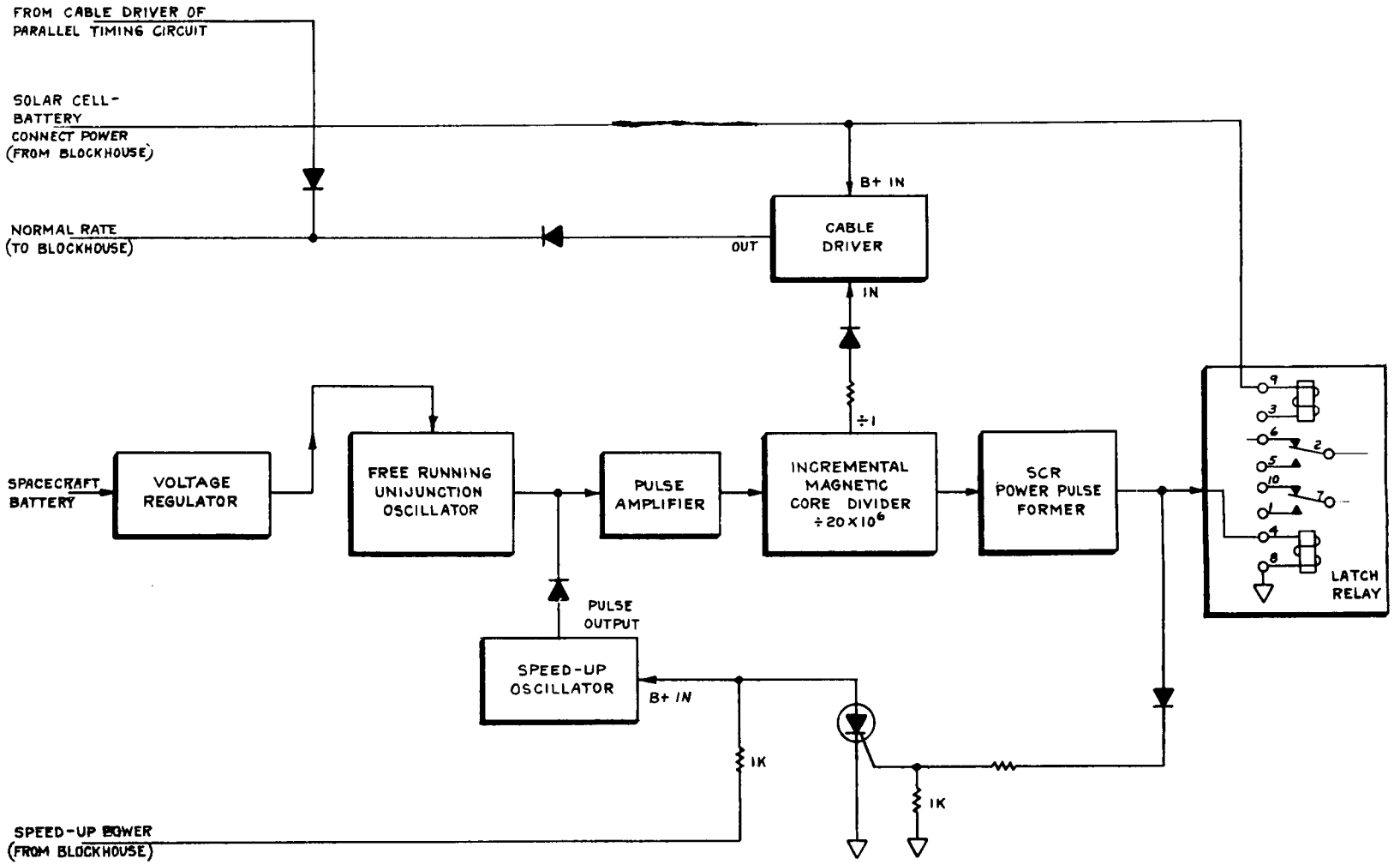

Figure 7-Block Diagram Basic Timing Circuit Showing Speed-Up & Cable Driver Circuit EPE-D

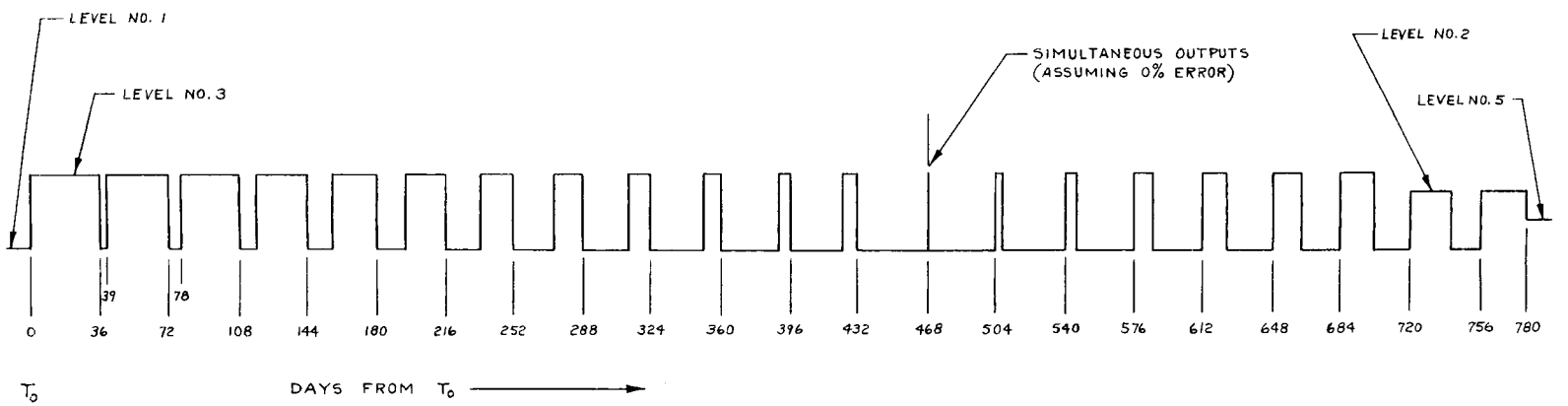

Figure 8–Graph Real Time Telemetry Monitor Readout EPE-D

Figure 6) However, since the speed-up oscillators of the timer are not synchronized with the normal rate oscillators the telemetry indication may be at either Line 1 or line 3 at time T_0. Variations in normal oscillator rate that may be expected from normal variations in temperature, stability, and accuracy will be measured and estimated for each flight unit. This data will then be available to aid in telemetry data interpretation.

POWER REQUIREMENTS

The two year timer will operate normally with battery voltage input range from +10.0 volts to +25 volts. At the normal spacecraft voltage of +19.6 volts, the unit draws 8 to 10 milliamperes.

ACCURACY AND STABILITY

The maximum components of error in the total accuracy of the Two Year Timer over the flight lifetime of two years are tabularized below:

Component	Maximum Percentage of the Timing Error
Accuracy in initial oscillator rate	±1%
Stability at a given temperature	±3%
Stability over the temperature range of -20°C to +70°C	±6%
Battery voltage variations	<±1%

Therefore, the total error of the two year interval will be ±10% or less.

COMPONENT RELIABILITY CONTROL AND UNIT TESTING

The basic circuitry is relatively simple and has been flown successfully in several spacecraft. Therefore, extensive additional circuit analysis has not been necessary. However, considerable effort has been extended toward ensuring maximum component reliability. Filter and timing capacitors are high reliability solid tantalum types. Coupling capacitors are low temperature coefficient mylar. The capacitors are individually checked electrically and given burn-in tests in the lab before use. The unijunction transistors are selected and lab tested, primarily to ascertain low and stable peak point emitter current. The silicon controlled rectifiers are selected and given extensive tests for holding and firing current variations. The remaining transistors are high reliability versions which have passed 200 hour burn-in tests.

The fabricated flight units will be given operating temperature tests in the lab to ensure overall stability. These tests will include a minimum of 20 temperature cycles between -30°C and ±75°C in addition to a minimum of 100 hours of operation at +75°C.

PRELAUNCH TESTS AND MONITOR

Since the timing cycle of the Two Year Timer is continuous, it is important that the prelaunch tests and monitoring of the unit be performed with care and thought to ensure that the timer is at the beginning of its two-year cycle. These tests should be performed at any convenient time prior to launch. The tests will consist of running the timer through its cycle twice at the speed up rate.

The tests will include the following:

1. Timing of the interval length at speed-up rate.
2. Recording the flip flop monitor output and observing the number and interval of the cross over points (See Figure 8).
3. Noting speed up power line current to ensure that the speed-up oscillators are turned off at the end of the timing cycle.
4. Ensuring operation of both relays in the timer at the end of the timing cycle.
5. Correlating the above information with decommutated telemetry readout.
6. Ensuring that the lines between the batteries and the solar cells are reconnected after the speed-up cycle.
7. Checking the normal oscillator rates.
8. Ensuring that speed-up current is not inadvertently applied before launch.
9. Recording position of telemetry monitor through telemetry readout.

All of this information will be available with proper monitoring of the Blockhouse lines from the Timer in the spacecraft. The complete test sequence and performance monitoring will be performed with the test panel provided with the Timer. This panel will also include test circuitry for the Program Switch and the Despin timer. The schematic of the test circuitry is shown in Figure 9. The prelaunch tests will be performed by Programmers Section personnel. The time required to perform the tests will be 2 hours or less.

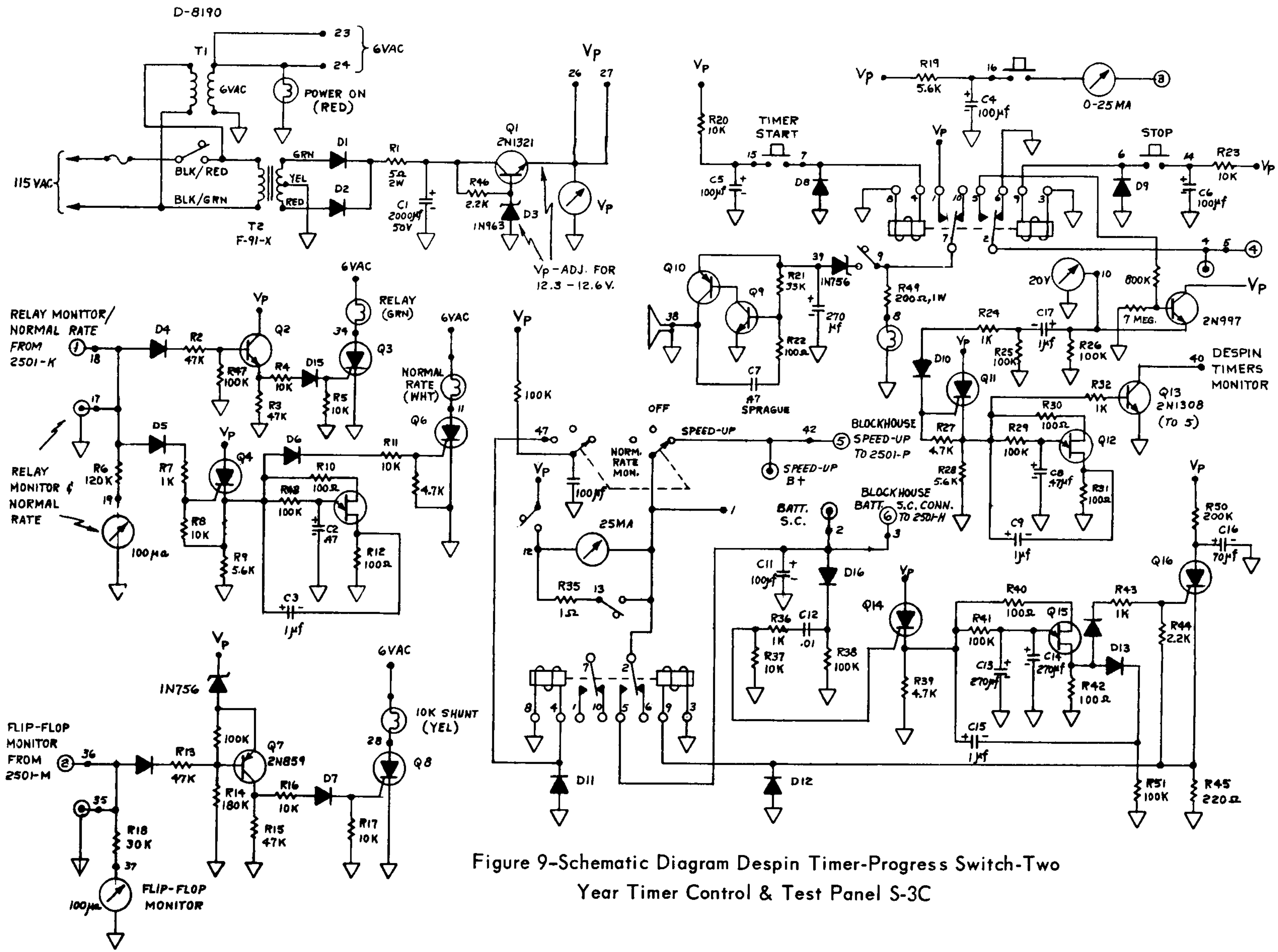

Figure 9-Schematic Diagram Despin Timer-Progress Switch-Two Year Timer Control & Test Panel S-3C

The schematic of the complete Two Year Timer with Monitor is shown in Figure 10.

NOTES:

1. ALL DIODES IN914

BLOCKHOUSE SPEED-UP P

FROM 5.6 K ENCODER RESISTOR R

TO BATTERY J N L

BLOCKHOUSE "CELL/BATT. ON" INPUT E H

BLOCKHOUSE FLIP-FLOP MONITOR TO SOLAR CELLS M D

BLOCKHOUSE RELAY MONITOR & NORMAL OSC. RATES F K B A

FROM 10 K ENCODER RESISTOR C

2501 (BOTTOM)

VA T.P. P

7PB M

VB T.P. R

GND. C

TP A A

2502 (TOP)

"B" SPEED-UP

"A" SPEED-UP

MONITOR FLIP/FLOP

RELAY "B" P & B SL11

RELAY "A" P & B SL11

Figure 10–Schematic Diagram Two Year Timer With Monitor EPE-D