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OPERATION AND MAINTENANCE MANUAL FOR UNIVERSAL PFM REAL-TIME DATA-REDUCTION SYSTEM

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Volume 1 of 2

OPERATION AND MAINTENANCE MANUAL FOR UNIVERSAL PFM REAL-TIME DATA-REDUCTION SYSTEM

Data Instrumentation Development Branch
Data System Division

Goddard Space Flight Center
Greenbelt, Maryland

LIST OF EFFECTIVE PAGES

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NOTE: The portion of the text affected by the current revision is indicated by a vertical line in the outer margins of the page.

Title	Original
i through v	Original
I-1 through I-9	Original
II-1 through II-25	Original
III-1 through III-45	Original
IV-1 through IV-23	Original
V-1 through V-3	Original
A-1 through A-9	Original

*The asterisk indicates pages revised, added or deleted by the current revision.

TABLE OF CONTENTS

Paragraph		Page
	SECTION I. GENERAL DESCRIPTION	
1.1	Approach	1-1
1.2	Scope	1-1
1.3	Physical Characteristics	1-2
1.4	Functional Description	1-4
1.4.1	Signal Processing	1-5
1.4.2	Recording Facilities	1-8
1.4.3	Special Box	1-8
1.5	Summary of System Characteristics	1-8
	SECTION II. OPERATION	
2.1	Approach	2-1
2.2	Controls and Indicators	2-1
2.3	Patching Arrangements	2-18
2.3.1	Digital Comb Filter	2-18
2.3.2	Program Boards No. 1 and No. 2	2-19
2.4	Normal Operating Conditions	2-21
2.4.1	Set-Up Procedure	2-21
2.4.2	Operating Procedure	2-23
2.5	Normal and Emergency Shutdown Procedures	2-25
	SECTION III. THEORY OF OPERATION	
3.1	Approach	3-1
3.2	System Functional Description	3-1
3.2.1	System Timing Section	3-2
3.2.2	Digital Data-Processing Section	3-3
3.2.3	Analog Signal-Processing Section	3-4
3.2.4	Special Box	3-4
3.3	Unit Functional Descriptions	3-4
3.3.1	Bit Synchronizer	3-4
3.3.2	Frame and Channel Control	3-8
3.3.3	Digital Comb Filter Unit	3-15
3.3.4	Digital Memory Unit	3-18
3.3.5	Digital Readout Control Unit	3-19
3.3.6	Hold Register Unit	3-21
3.3.7	BCD Converter Unit	3-22
3.3.8	Printer Code Converter	3-28
3.3.9	Period Readout and Display	3-32
3.3.10	Special Box	3-34

TABLE OF CONTENTS (Continued)

Paragraph — Page

SECTION III. THEORY OF OPERATION (Continued)

3.3.11 Control Panel No. 1 3-35
3.3.12 Control Panel No. 2 3-36
3.3.13 Control Panel No. 3 3-36
3.3.14 Special Circuits 3-37

SECTION IV. MAINTENANCE

4.1 Approach 4-1
4.2 Preventive Maintenance 4-1
4.2.1 Inspection Schedule 4-1
4.2.2 Lubrication Schedule 4-1
4.2.3 Minor Repair and Adjustment 4-2
4.3 Corrective Maintenance 4-2

SECTION V. PARTS LIST

Parts List 5-1

SECTION VI. DIAGRAMS — Volume 2

APPENDIX I

A-1.1 Approach A1-1
A-1.2 IMP Telemetry Format A1-1
A-1.3 Filter/Detector/Clamp A1-1
A-1.4 Special Lockout Circuits A1-3
A-1.5 Sequence Identifier A1-3
A-1.6 University of Chicago Readout Control A1-5
A-1.6.1 Performance Characteristics A1-5
A-1.6.2 Timing Considerations A1-6
A-1.6.3 Sequence of Operation A1-6
A-1.7 Simulator A1-7
A-1.7.1 Data Train A1-7
A-1.7.2 Marker Pulses A1-8

LIST OF ILLUSTRATIONS

Figure — Page

SECTION I. GENERAL DESCRIPTION

1-1 Universal PFM Real-Time Data-Reduction System No. 1 1-3
1-2 Universal PFM Real-Time Data-Reduction System No. 1, Location of Units 1-4
1-3 Universal PFM Real-Time Data-Reduction System No. 1, Simplified Functional Block Diagram 1-5

SECTION II. OPERATION

2-1 Bit Synchronizer Unit, Controls and Indicators 2-2
2-2 Frame and Channel Control Unit, Upper Panel, Indicators 2-3
2-3 Frame and Channel Control Unit, Lower Panel, Controls and Indicators 2-4
2-4 Digital Comb Filter Unit, Rear Panel, Controls and Indicators 2-5
2-5 Printer Code Converter Unit, Printer Programming Panel, Controls and Indicators 2-6
2-6 Period Readout Control Unit, Controls and Indicators 2-7
2-7 Control Panel No. 1, Controls and Indicators 2-9
2-8 Control Panel No. 2, Controls and Indicators 2-11
2-9 Control Panel No. 3, Controls and Indicators 2-13
2-10 Rejection Filter Unit, Controls and Indicators 2-15
2-11 Bit Rate Filter Unit, Controls and Indicators 2-16
2-12 Special Box Unit, Controls and Indicators 2-17
2-13 Digital Comb Filter 2-18
2-14 Program Boards No. 1 and No. 2 2-20

SECTION III. THEORY OF OPERATION

3-1 Universal PFM Real-Time Data-Reduction System No. 1, Functional Block Diagram 3-1
3-2 Bit Synchronizer, Functional Block Diagram 3-5
3-3 Frame and Channel Control, Functional Block Diagram 3-9
3-4 Digital Comb Filter, Functional Block Diagram 3-16
3-5 Typical Memory Cell 3-18
3-6 Digital Readout Control, Functional Block Diagram 3-20
3-7 Hold Register, Functional Block Diagram 3-22
3-8 BCD Converter, Functional Block Diagram 3-25
3-9 Printer Code Converter, Functional Block Diagram 3-29
3-10 Period Readout and Display Logic, Functional Block Diagram 3-33
3-11 Simple Ladder Network 3-37
3-12 Rundown Circuit, Simplified Schematics 3-43

SECTION IV. MAINTENANCE

4-1 D to A Converter and VCO, Component Locations 4-3
4-2 Detector, Integration and Sync Recognition, Component Locations 4-4
4-3 Schmitt Trigger, Component Locations 4-5

LIST OF ILLUSTRATIONS (Continued)

Figure — Page

SECTION IV. (Continued)

4-4 Signal Conditioner Board No. 1, Component Locations 4-6
4-5 Filter and 2X Amplifier, Component Locations 4-7
4-6 AGC Circuit, Component Locations 4-8
4-7 Detector Circuit, Component Locations 4-9
4-8 Discriminator, Component Locations 4-10
4-9 Rundown Circuit, Component Locations 4-11
4-10 Flipflop, Component Locations 4-12
4-11 NAND Circuit, Component Locations 4-13
4-12 Power Supply, Component Locations 4-14
4-13 Resistor Termination Board, Component Locations 4-15
4-14 Bit Synchronizer, Timing Diagram 4-16
4-15 Frame and Channel Control, Timing Diagram 4-17
4-16 Digital Comb Filter, Timing Diagram 4-18
4-17 Hold Register, Timing Diagram 4-19
4-18 Binary-to-BCD Converter, Timing Diagram 4-20
4-19 Digital Readout Control, Timing Diagram 4-21
4-20 Printer Code Converter, Timing Diagram 4-22
4-21 Simulator (Special Box), Timing Diagram 4-23

APPENDIX I

A-1 IMP Telemetry Format A1-2
A-2 Special Box, Functional Block Diagram A1-4

LIST OF TABLES

Table — Page

SECTION I. GENERAL DESCRIPTION

1-1 Standard Commercial Equipment Used in Universal PFM Real-Time Data-Reduction System No. 1 1-2
1-2 Summary of System Characteristics 1-9

SECTION II. OPERATION

2-1 Bit Synchronizer Unit, Controls and Indicators 2-2
2-2 Frame and Channel Control Unit, Upper Panel, Controls and Indicators 2-3
2-3 Frame and Channel Control Unit, Lower Panel, Controls and Indicators. 2-4
2-4 Digital Comb Filter Unit, Rear Panel, Controls and Indicators 2-5
2-5 Printer Code Converter Unit, Printer Programming Panel, Controls and Indicators 2-6

LIST OF TABLES (Continued)

Table		Page
	SECTION II. OPERATION (Continued)	
2-6	Period Readout Control Unit, Controls and Indicators	2-7
2-7	Control Panel No. 1, Controls and Indicators	2-8
2-8	Control Panel No. 2, Controls and Indicators	2-10
2-9	Control Panel No. 3, Controls and Indicators	2-13
2-10	Rejection Filter Unit, Controls and Indicators	2-14
2-11	Bit Rate Filter Unit, Controls and Indicators	2-16
2-12	Special Box Unit, Controls and Indicators	2-17
	SECTION III. THEORY OF OPERATION	
3-1	Contents of BCD Register Stages During Binary-to-BCD Conversion Process	3-27

SECTION I.
GENERAL DESCRIPTION

1.1 APPROACH

The Universal PFM Real-Time Data-Reduction System No. 1 was designed and constructed by the Data Instrumentation Development Branch of the Data Systems Division at Goddard Space Flight Center, Greenbelt, Maryland, to be readily adaptable to the characteristics of all present and anticipated PFM telemetry signals. This manual describes the applications and the capabilities of the system. It contains the instructions and information necessary to indoctrinate thoroughly an experienced technician regarding the operating technique required, the intricacies of programming the equipment, and the performance characteristics to be expected from it. The major portion of the text is devoted to operating instructions and to a detailed functional description of the overall system and the individual units of which it consists.

1.2 SCOPE

The text of this manual and the supporting tables, diagrams, and photographs provide the information necessary to enable an experienced technician to set up and operate the equipment, to adapt it to the unique data train of a specific PFM telemetry signal, and to perform the preventive and corrective maintenance procedures which may be required from time to time. This section contains a discussion of the physical characteristics of the equipment, a functional description of the overall system, a table summarizing the capabilities and limitations of the system, and a list of reference manuals pertinent to the standard commercial equipment incorporated in the design of the system. Section II contains complete operating instructions for the equipment and an explanation of the programmable patch panels essential to the universality of the system. Section III contains a theory of operation discussion at the functional block diagram level for the individual units of the equipment, and circuit descriptions keyed to the schematic diagrams of unique circuits. Section IV contains instructions for the performance of preventive and corrective maintenance procedures, including the tests and adjustments necessary for compliance with minimum performance standards. Section V consists of a parts list. Section VI, Volume II, consists of a complete set of logic and schematic diagrams. The appendix to this manual contains a functional description of the special circuits and modifications used to adapt the universal data-processing system to the unique format of a specific telemeter. The appendix includes a brief introduction to the general PFM telemetry signal format, an explanation of the way in which the specific telemeter deviates from this general format, and a complete programming schedule for processing the data from the specific telemeter. Since it is assumed that anyone attempting to familiarize himself with the equipment has a basic

knowledge of logic circuits, their symbols and their performance characteristics, it is not within the scope of this manual to discuss individual circuits, except for the special cases previously noted. However, a more detailed explanation of each of the circuits used in this equipment which are not analyzed in this document will be found in the Computer Control Company's (3C) manual listed in Table 1-1.

Table 1-1. Standard Commercial Equipment Used in Universal PFM Real-Time Data-Reduction System No. 1

FUNCTION (Figure 1-2)	COMMERCIAL NAME	MANUFACTURED BY	APPLICABLE REFERENCE MANUALS
Digital printer	Digital recorder: Model 562A Model H24-562A	Hewlett-Packard Company, Palo Alto, California	Operating and Service Manual 01331-1, for Model 562A, with Supplement 01381-1 Service Manual for Printer Mechanism Type 130
Galvanometer amplifiers (2 units)	Model T6GA galvanometer amplifiers	Minneapolis-Honeywell Regulator Co. Denver, Colorado	Operation and Maintenance Manual for Model T6GA, Series 500 and 600
Rejection filter	Model 722 filter	Dytronics Company Columbus, Ohio	Operating and Instruction Manual for Model 722 Filter
Bit rate filter	Model 720 bandpass filter		Operating and Instruction Manual for Model 720 Bandpass Filter
Oscillograph CEC (2 units)	Type 5-124 recording oscillograph	Consolidated Electro-dynamics Corp., Pasadena, Calif.	Operating and Maintenance Manual for Type 5-124 Recording Oscillograph. Galvanometer Users' Handbook
Logic modules	S-PAC digital modules	Computer Control Company, Inc. Framingham, Mass.	Instruction Manual for S-PAC Digital Modules Publication No. 71-100A

1.3 PHYSICAL CHARACTERISTICS

Figure 1-1 is a photograph of the Universal PFM Real-Time Data-Reduction System completely contained by relay racks of standard height and width, with a depth of 19-1/2 inches. The location of the individual units of the system is shown in Figure 1-2. If remote control is desired, the control panels can be mounted in a console and linked by prefabricated cables to the units remaining in the relay racks. The physical design of the equipment is such that it also can be adapted to installation within a trailer. Printed circuit cards of the 3C S-PAC digital-module type manufactured by the Computer Control Company are used throughout the system. Standard items of commercially available electronic equipment which have been purchased as complete units, and incorporated in the design of the system as such, are listed in Table 1 with applicable manufacturers' instruction manuals.

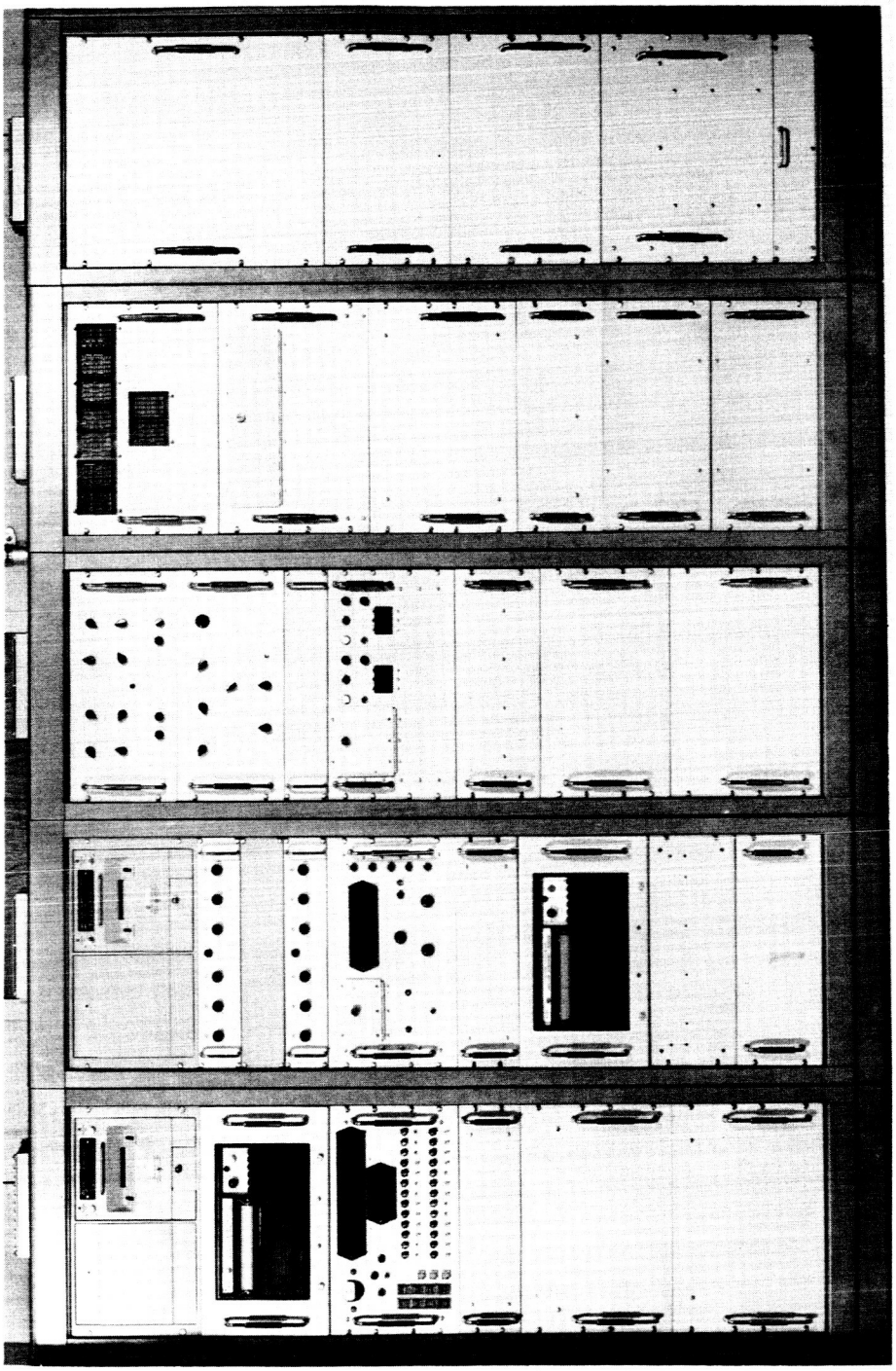


Figure 1-1. Universal PFM Real-Time Data-Reduction System No. 1

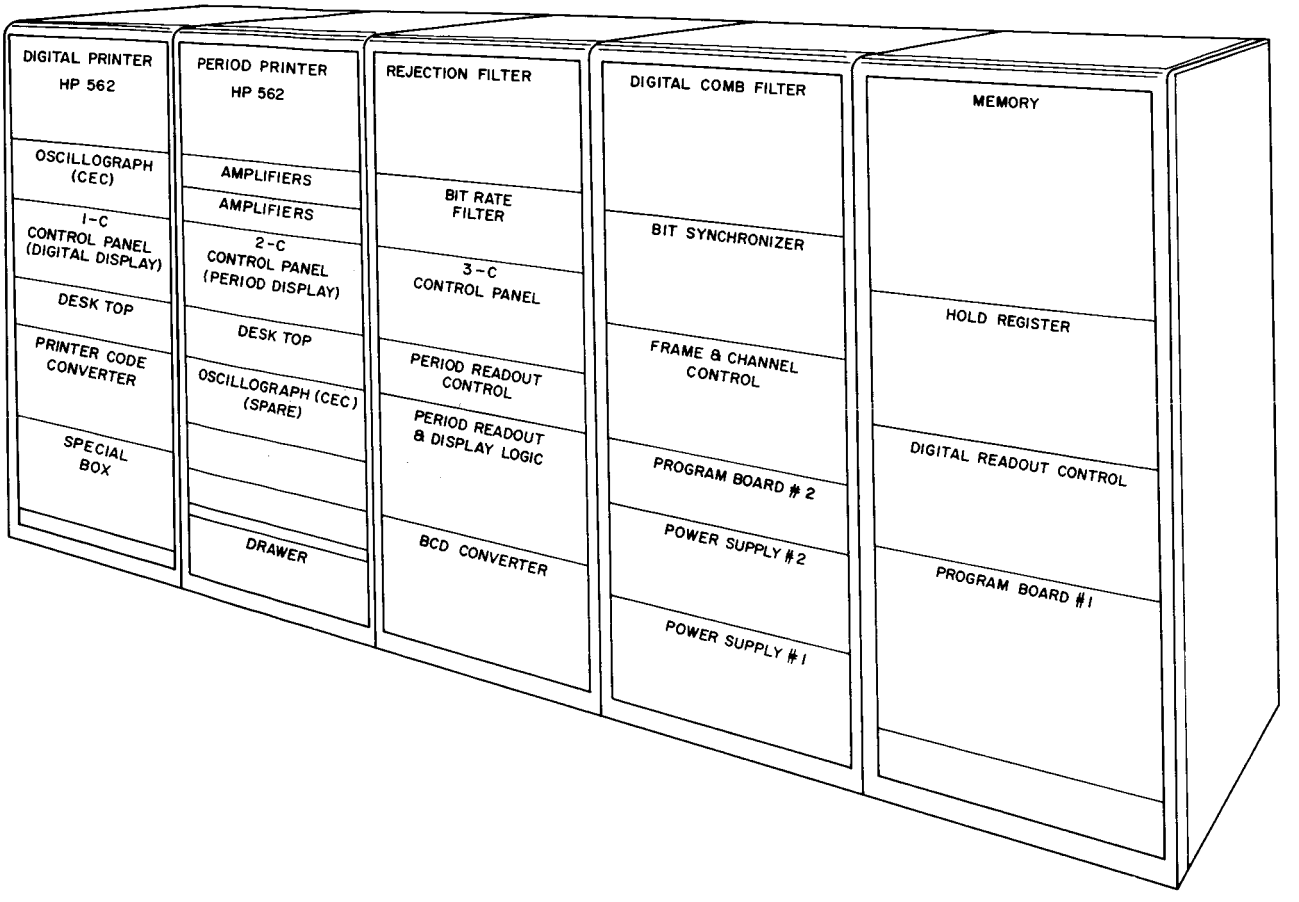


Figure 1-2. Universal PFM Real-Time Data-Reduction System No. 1, Location of Units

1.4 FUNCTIONAL DESCRIPTION

The equipment has been designed to process the digital and analog data contained in all known, and anticipated, PFM telemetry signal formats. The universality of the system is a result of its complete flexibility of programming. This is made possible by such distinguishing features as the digital demodulation technique, the programmable patchboards used for signal coupling, the versatility of the operating controls provided, and a functional unit, the special circuits of which are contained in a drawer referred to as the "special box." The system is capable of processing any PFM signal which has a bit rate between the limits of 3 and 200 cps, and any ratio of channels per frame, and frames per sequence, between the limits of one and sixteen. The system also provides the operator with a choice of frame sync recognition methods, and is readily adaptable to the application of special circuits to detect subcommutation signals and to lock out unwanted CW transmissions. The digital data-processing section can be programmed to accommodate words consisting of as many as 21 information bits each.

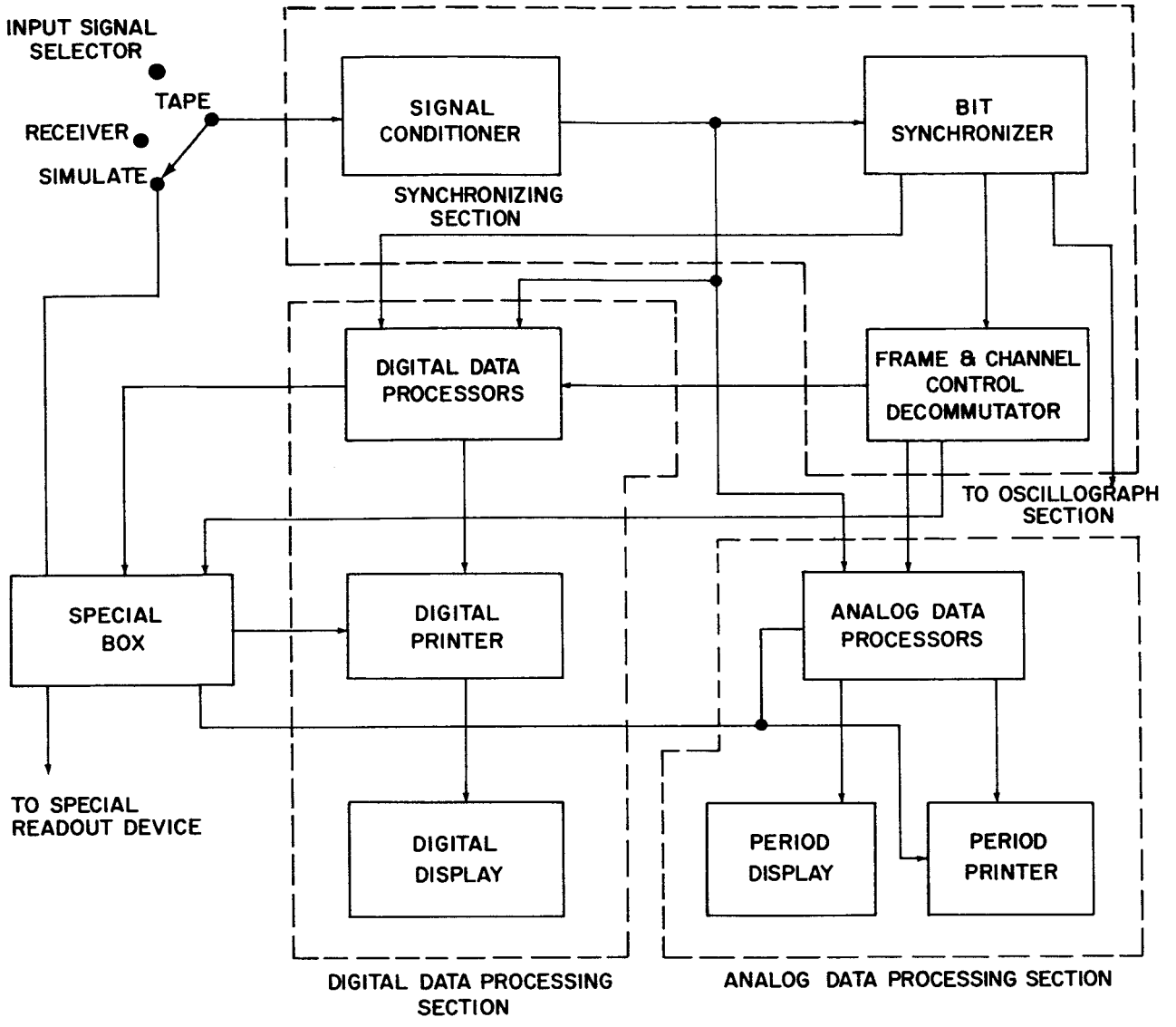


Figure 1-3. Universal PFM Real-Time Data-Reduction System No. 1, Simplified Functional Block Diagram

1.4.1 SIGNAL PROCESSING

Figure 1-3 is a simplified block diagram of the data-reduction system. The equipment is discussed here, and shown in the block diagram, as a system consisting of a synchronizing section, a digital data-processing section, an analog data-processing section, and a special box. It decommutates and demodulates incoming PFM telemetry signals from a receiver, tape recorder, or signal simulator, sorts the digital and analog information channels received, and prints out the extracted data in the form of decimal numbers on two separate paper tapes. At the same time, the decimal values of the digital and analog channel information are displayed separately by two groups of nixie tubes, and analog values representative of the modulation frequency present in each PFM data burst can be recorded on a rack-mounted oscillograph. Synchronous timing signals for the digital and analog

data-processing sections are developed from the incoming telemetry signal data train by the synchronizing section. These timing signals are used to sort the data bursts of the incoming signal by digital and analog information channels in the process of decommutating them, and as gating signals which control the demodulation processes. The data bursts are demodulated in the digital and analog data-processing sections, where the printout and display of the extracted data is also accomplished.

1.4.1.1 Synchronizing Section

Basically the synchronizing section consists of a signal conditioner, a bit synchronizer, and a frame and channel decommutator.

1.4.1.1.1 The input PFM-telemetry data train is fed into the signal conditioner. This subsection performs amplitude limiting and pulse shaping operations which make the synchronizing and data-processing functions independent of variations in the input signal-to-noise ratio. After passing through the signal conditioner, the data train is sent to the digital and analog data-processing sections and to the bit synchronizer. A low pass rejection filter of commercial design (table 1-1) is used to couple the signal from the INPUT SIGNAL SELECTOR switch to the remainder of the signal conditioning circuits. This filter, which is broadly tuned to span the range of anticipated subcarrier oscillator frequencies, is used to improve the input signal-to-noise ratio.

1.4.1.1.2 Timing signals for system synchronization are developed by the bit synchronizer from the reconstituted telemetry clock. The data burst/blank envelope is extracted from the input signal by a detector, peaked and refined by a bit-rate filter, and reshaped to serve as a frequency and phase-locked reference source which makes burst-by-burst signal synchronization possible. This signal is used in conjunction with a digital memory and comparison circuit to continuously control a voltage-controlled oscillator (VCO) by employing a servotechnique. The electronic flywheel action of the synchronizer is used to maintain synchronization during periods of signal fading and CW transmissions. A strobe generator, located in the bit synchronizer unit and controlled by a counter coupled to the VCO, provides the timing pulses used for system synchronization.

1.4.1.1.3 Decommutation of the telemetry signal is accomplished by the frame and channel control section. This function is coordinated by timing signals from the bit synchronizer. These two functional sections work together to assure the synchronization of system output data. Frame synchronization is established by recognition of the extrawide frame-sync burst through the integrate-and-dump technique. The electronic flywheel of the bit synchronizer acquires synchronism with the incoming telemetry signal. The frame-synchronizer circuits and the sync search and lock circuits of the frame and channel control section are then used to establish a system search and lock mode; this mode inhibits data processing until a satisfactory confidence ratio occurs between frame-synchronization recognitions which occur in synchronism and out of synchronism with the channel decommutator. This ratio is variable and can be programmed by the operator. When the system is in synchronism, the lock mode is established and processing begins. When synchronism is lost, the system shifts to the search mode and digital data processing is discontinued until synchronism is reacquired. Frame and channel sorting and frame correction are accomplished by the frame

and channel control section, which includes a frame and channel matrix. The outputs of this matrix are the 256 individual channel marks. This matrix is coupled to the digital data-processing section through a patch board known as program board No. 2 and to the analog data-processing section by 256 of the 289 toggle switches located on the period readout control switching panel.

1.4.1.2 Digital Data-Processing Section

Telemetry channels modulated by digital data are processed first by the digital comb filter which resolves the subcarrier modulation frequency of each data burst it receives into an octal number. This number is then transferred in binary form to the memory unit, three memory cells being associated with each channel demodulated. When all of the channels associated with a word have been processed, the word is transferred in parallel to the hold register; from the hold register, the word is shifted out serially as a pure binary number and converted to a binary coded decimal (bcd) number. The bcd number is again converted and printed out as a pure decimal number on the printer tape, together with its register and sequence identification number. At the same time, this number is visually displayed at control panel No. 1 by a group of nixie tubes. The output of the comb filter is coupled to the memory unit and the output of the memory unit is coupled to the hold register by a patch panel known as program board No. 1. Program changes can be accomplished for various telemetry formats by preparing program board No. 1 and No. 2 patch panels in advance and plugging them into their respective receptacles as required. The center frequency and bandwidth of each of the comb-filter teeth is readily changed by manipulating the placement of pins in a program board located on the front panel of the filter unit.

1.4.1.3 Analog Data-Processing Section

The information extracted from analog channel is printed out, and simultaneously displayed by nixie tubes at control panel No. 2, as a decimal number equivalent to the average period computed from the value of ten successive cycles of the subcarrier modulation frequency. The average period is computed for each channel by the printer code converter unit, which makes the information available in bcd form for use by a digital printer. These bcd numbers are also coupled to the period display control circuits of the period readout and display logic unit. In each case, the bcd numbers are converted to decimal numbers which are printed out on a paper tape together with sequence, frame, and channel identification numbers, and are also sequentially displayed by five in-line nixie tubes. The decimal numbers are the ten-period average values in microseconds of the individual channel subcarrier modulation frequencies transmitted.

1.4.1.3.1 A bank of 289 toggle switches provides a means of conditioning the period readout and display logic circuits so that the inclusion or exclusion of information to the data readout circuits of the analog data-processing section can be selectively controlled with respect to all channels, frames, and sequences. By manipulating these switches the operator can select any, or all, of the experimental data being received to be read out at any chosen time.

1.4.2 RECORDING FACILITIES

The data-processing speed of the system is limited by the mechanical response rate of the digital-recording equipment used. The digital and period printers currently in use with the equipment (table 1-1), which are capable of five printouts per second, are adequate in this respect for use with the telemeter described in Appendix I of this volume, since a low data-burst rate of 3-per-second is involved. However, the system has been designed with the capabilities to drive a high-speed printer which can respond to data bursts as frequent as 55-per second. Such a printer may be acquired and used as peripheral equipment when the need for it arises.

1.4.2.1 A second means of recording output data is provided by an oscillographic recorder (table 1-1). A discriminator located in the bit synchronizer unit is coupled to the oscillograph by a bank of galvanometer amplifiers. The discriminator, which develops output signal voltages with peak amplitudes linearly related to the subcarrier oscillator frequencies of the input signal, has been designed with an internal calibration system for use over a wide range of data-burst rates. Twelve channels of amplification are available by using two galvanometer amplifier units (table 1-1) of standard commercial design. Each amplifier channel is equipped with an individual gain control which enables the operator to regulate manually the resolution of the oscillographic record for each experiment processed.

1.4.3 SPECIAL BOX

The universality of the equipment as a data-reduction system easily adapted to any PFM telemetry format is implemented by a plug-in unit referred to generally as the special box. This unit contains unique circuits individually designed to accommodate the features of the signal to be processed. A separate special box is used for each telemeter concerned to change over from the processing of data from one satellite to that from another. The circuits incorporated in the individual special boxes may be designed to perform several functions. However, one of the prime functions of this unit is to generate for test purposes a simulated signal which closely conforms to the characteristics of the telemetry signal with which it is to be used. Each special box, therefore, will invariably contain a signal simulator circuit of unique design. The special box designed to implement this system for use with a specific telemeter is described in Appendix I of this volume.

1.5 SUMMARY OF SYSTEMS CHARACTERISTICS

Table 1-2 summarizes significant physical and functional characteristics of the system.

Table 1-2. Summary of System Characteristics

Primary Power	
Source	110 V.A.C., 60 cps, single phase
Line 1 capacity	30 amps
Line 2 capacity	30 amps
Line 3 capacity	30 amps
Operating Temperature	25 C° ambient
Input Signal Characteristics	
Source	Telemetry receiver, magnetic tape deck, or simulator (special box)
Type	Any PFM signal
Operating range	
Channel rate	3-55 cps
Channels per frame	1-16
Frames per sequence	1-16
Operating Modes	Search and lock, automatic synchronization indicators on control panel No. 2 and on frame and channel control unit panel
Lock	Frame sync acquired, digital and analog data processed
Search	Loss of frame sync, analog data only processed
Output Signal Characteristics	
Digital data-processing section	Functions in lock mode only
Data recording	Eleven-wheel digital printer provides 7-place decimal value printout per word, plus word and sequence number identification, on paper tape
Data display	Nixie tube readouts on control panel No. 1 provide 7-place decimal value display per word plus 3-place digital register number identification
Analog data-processing section	Functions continuously at flywheel rate
Data recording	Twelve-wheel digital printer provides, per channel, a 5-place decimal value printout of the burst period in microseconds to nearest tenth, plus channel frame and sequence number identification on paper tape
	Oscillograph provides continuous trace on photo-sensitive paper. Twelve galvanometer amplifier channels selectable from control panel No. 2
Data display	Nixie tube readout on control panel No. 2 provides, per channel, a 5-place decimal value display of the burst period in microseconds to nearest tenth
Programming	
Synchronizing section	Accomplished with operating controls of rejection filter, bit-rate filter, bit synchronizer, frame and channel control units, and sync oscillator section of digital comb filter unit patch panel
Digital data-processing section	
Demodulation	Controlled at digital comb filter unit patch panel
Decommutation	Controlled by program boards No. 1 and No. 2
Analog data-processing section	
Demodulation	Controlled at printer code converter unit programming panel
Decommutation	Regulated at period readout control unit switching panel
Special box	Provides simulated signal for tests and troubleshooting. (Refer to paragraphs 4.5 and A-1.7.)

SECTION II.
OPERATION

2.1 APPROACH

This section contains procedures for turning on the Universal PFM Real-Time Data Reduction System No. 1, for operating it under normal conditions, and for shutting it down under normal and emergency conditions. Patching arrangements are described, as are checks, calibrations, and adjustments which are part of the normal sequence of operation. However, before operating the equipment, the operator must become familiar with the controls, indicators, and adjustments on the equipment, and the functions of each.

2.2 CONTROLS AND INDICATORS

The following tables list all controls, indicators, and adjustments on each panel by panel nomenclature, as well as the function of each component. Each table is supported by a photograph of the associated panel.

Table 2-1. Bit Synchronizer Unit, Controls and Indicators

FIGURE 2-1 REF. NO.	NOMENCLATURE	FUNCTION
1	BIT RANGE SELECTOR rotary switch	Positioning this switch roughly selects desired bit range
2	PHASE ADJUSTMENT potentiometer	Adjusts phase between flywheel and data to be processed
3	EXT. METER toggle switch	Controls bit-rate indicator on control panel No. 1
4	VCO LOW indicator (amber)	Lights to indicate that VCO frequency, at last comparison, was low
5	BIT RATE INDICATOR meter	Measures comparison between data and flywheel; best adjustment is made at center scale
6	VCO HIGH indicator (amber)	Lights to indicate that VCO frequency, at last comparison, was high
7	OPERATE/SET toggle switch	In SET position locks UP-DOWN counter to center of its range
8	BIT RATE ADJUSTMENT multideck potentiometer	Used to adjust bit synchronizer to data bit rate when OPERATE/SET switch is in SET position

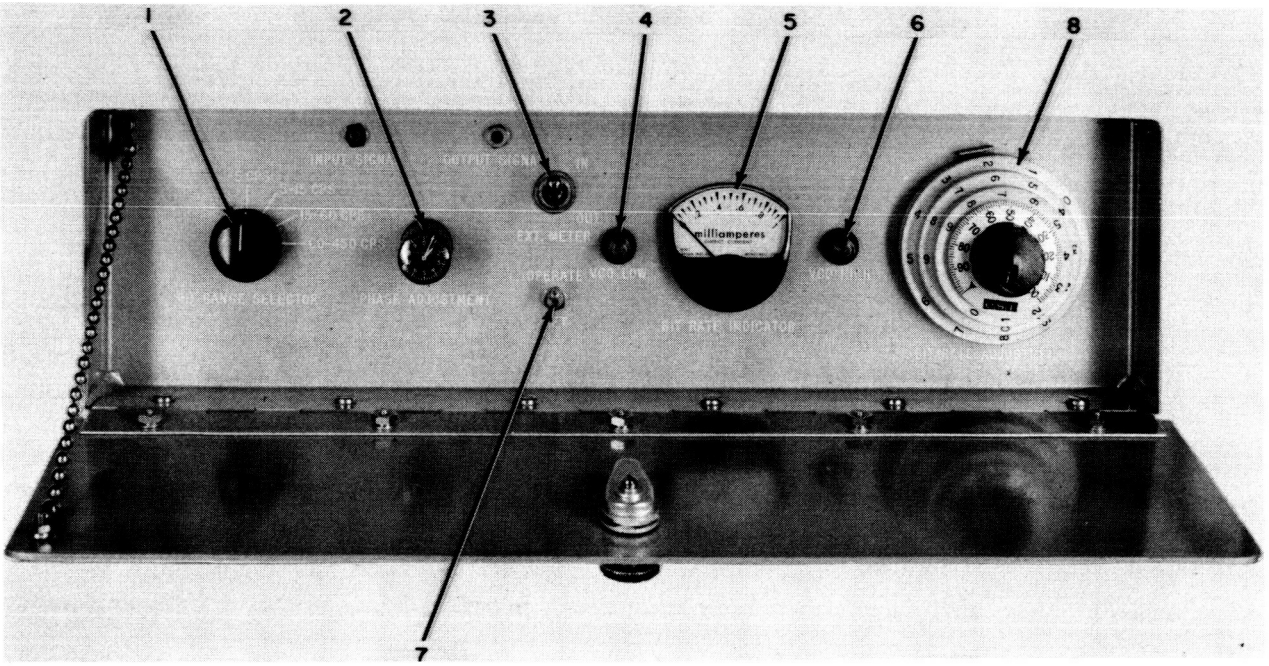


Figure 2-1. Bit Synchronizer Unit, Controls and Indicators

Table 2-2. Frame and Channel Control Unit, Upper Panel, Controls and Indicators

FIGURE 2-2 REF. NO.	NOMENCLATURE	FUNCTION
1	FRAME SYNC RECOG rotary switch	Allows operator to make appropriate selection of any frame sync mode of recognition for given satellite format
2	BIT RATE rotary switch	Selects time constants for integration circuit and detector
3	INTEGRATION SYNC ADJ. potentiometer	Adjusts waveform of integrator circuit for wide burst recognition
4	SEARCH indicator (amber)	Lights to indicate that equipment is searching for frame sync
5	RESET pushbutton	Initiates search mode for frame sync
6	LOCK indicator (amber)	Lights to indicate that frame sync is locked on
7	CHANNEL SELECTOR rotary switch	Used for troubleshooting in conjunction with OUT test point, by selecting any of 16-channel pulses for oscilloscope display

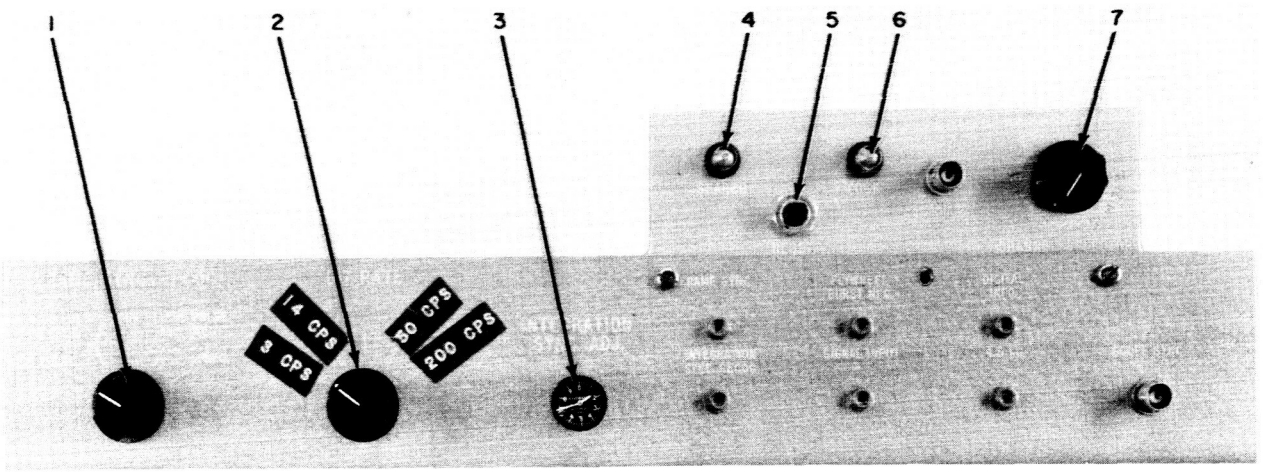


Figure 2-2. Frame and Channel Control Unit, Upper Panel, Controls and Indicators

Table 2-3. Frame and Channel Control Unit, Lower Panel, Controls and Indicators

FIGURE 2-3 REF. NO.	NOMENCLATURE	FUNCTION
1	IN PHASE COUNTER toggle switches (4)	A binary setting which represents the number of in-phase frame sync recognition pulses required to initiate a locked condition
2	OUT OF PHASE COUNTER toggle switches (4)	A binary setting which represents the number of out-of-phase frame sync recognition pulses required to initiate a search condition
3	CHANNEL PROGRAMMING toggle switches (4)	These switches are set according to satellite format and determine the number of channels, in agreement with data format
4	FRAME PROGRAMMING toggle switches (4)	The switches are set according to satellite format and determine the number of frames, in agreement with data format

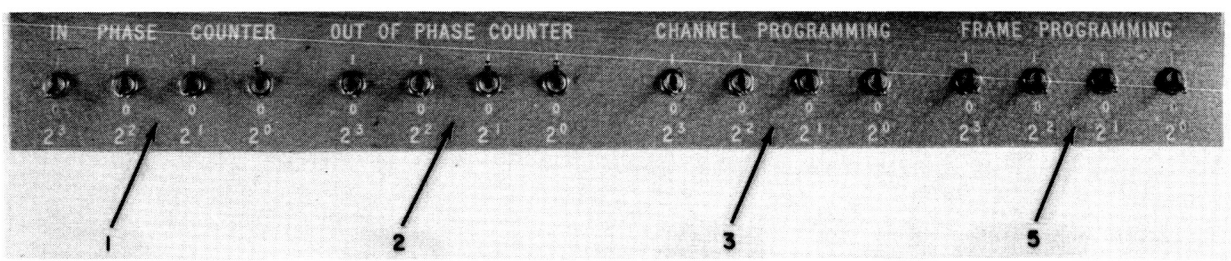


Figure 2-3. Frame and Channel Control Unit, Lower Panel, Controls and Indicators

Table 2-4. Digital Comb Filter Unit, Rear Panel, Controls and Indicators

FIGURE 2-4 REF. NO.	NOMENCLATURE	FUNCTION
1	CH0 thru CH7 indicators (8, amber)	Light to indicate what octal number is being processed
2	ERROR indicator (amber)	Lights to indicate that sample being processed is outside any of eight frequency ranges
3	FREQ. ADJ. potentiometer	Used in testing to vary frequency of input over all eight channels
4	TEST/OPERATE rotary switch	In TEST position, allows internal circuitry to test digital comb filter
5	INITIAL CLEAR pushbutton switch	Depressed to initially clear digital comb filter circuitry in test mode

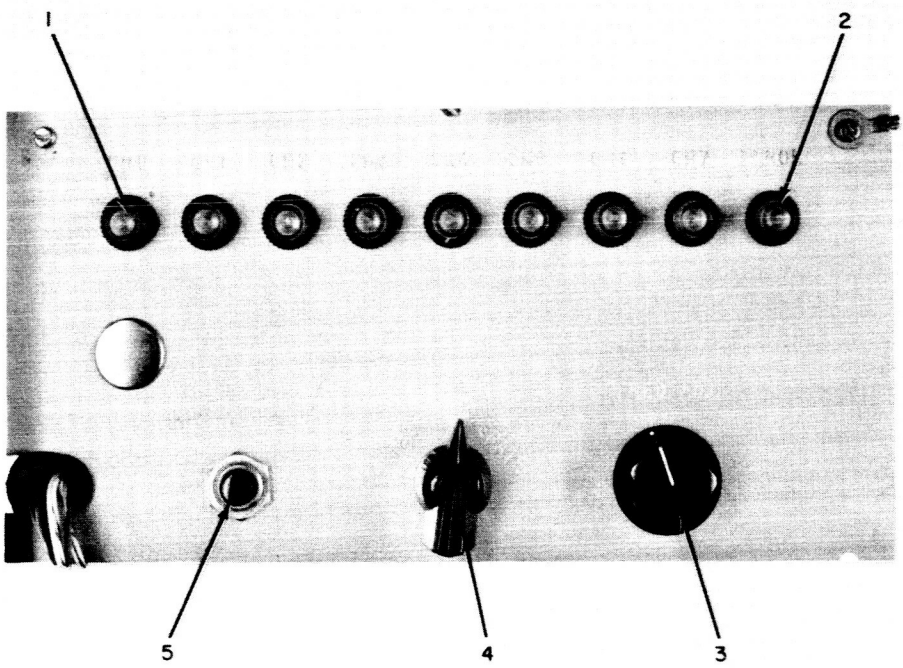


Figure 2-4. Digital Comb Filter Unit, Rear Panel, Controls and Indicators

Table 2-5. Printer Code Converter Unit, Printer Programming Panel, Controls and Indicators

FIGURE 2-5 REF. NO.	NOMENCLATURE	FUNCTION
1	INPUT rotary switch	External positions allow for either serial or parallel loading of the decade counter; internal position utilizes internal period measurement facilities
2	BURST/BLANK toggle switch	Positioned to measure frequencies during either burst or blank periods
3	WORD LENGTH toggle switches	Positioned to correspond to number of decimal places in a readout plus one for a command pulse
4	DECADES/SEQUENCE patches (18)	Allows printing, in a selectable sequence, of up to eight decades and a command
5	PERIOD MEASUREMENT PULSE DELETE toggle switches (5)	Positioned to allow operator to delete up to 31 periods of each burst or blank of incoming signal
6	H. S. PRINTER CONTROL toggle switch	In IDLE position, printing operation is disabled
7	READOUT CONTROL toggle switch	Positioned to allow for external control of printer; i.e., print command, start, stop, etc.

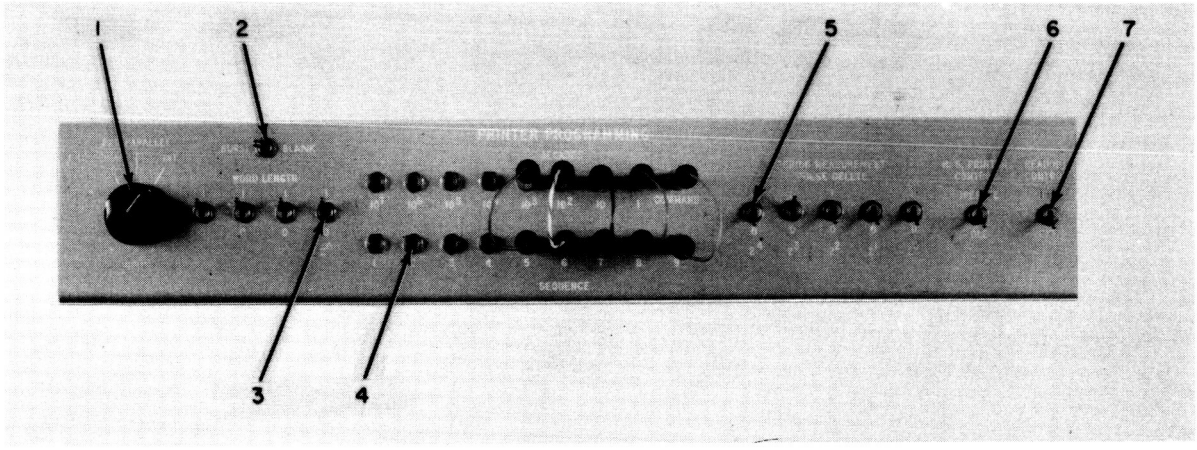


Figure 2-5. Printer Code Converter Unit, Printer Programming Panel, Controls and Indicators

Table 2-6. Period Readout Control Unit, Controls and Indicators

FIGURE 2-6 REF. NO.	NOMENCLATURE	FUNCTION
1	SEQUENCE toggle switches (16)	Positioned to select any or all sequences of analog readout
2	FRAME toggle switches (16)	Positioned to select any or all frames of analog readout
3	CHANNEL toggle switches (256)	Positioned to select any or all channels of analog readout
4	MASTER toggle switch	In downward position, disables sequence switches in event that sequence information is not available

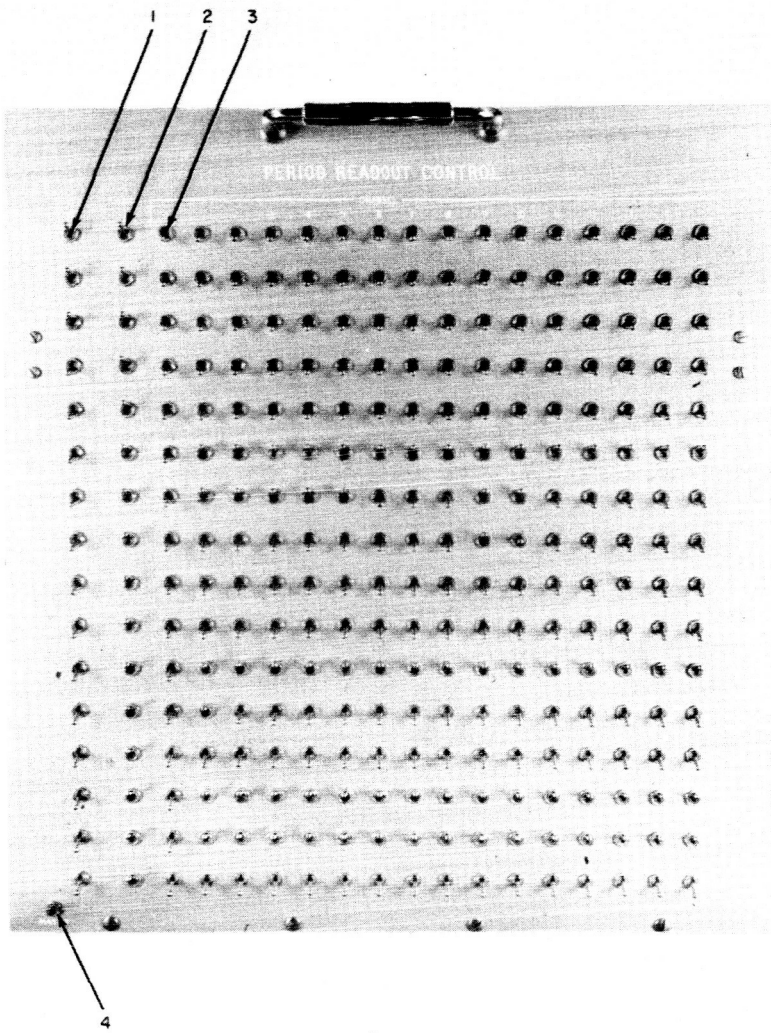


Figure 2-6. Period Readout Control Unit, Controls and Indicators

Table 2-7. Control Panel No. 1, Controls and Indicators

FIGURE 2-7 REF. NO.	NOMENCLATURE	FUNCTION
1	VCO LOW indicator (amber)	Lights to indicate that VCO frequency, at last comparison, was low
2	BIT RATE INDICATOR meter	Measures comparison between data and flywheel
3	VCO HIGH indicator (amber)	Lights to indicate that VCO frequency, at last comparison, was high
4	DECIMAL VALUE nixies (7)	Indicate decimal value of digital word from the BCD converter
5	DIGITAL REGISTER NUMBER nixies (2)	Indicates what portion of the memory is being read out
6	DIGITAL DISPLAY SELECTION indicators (25, amber)	Lights to indicate that respective ON/OFF toggle switch is in ON position
7	ON/OFF toggle switches (25)	Positioning to ON selects a particular word for processing and readout
8	ALL indicator (amber)	Lights to indicate that respective ON/OFF toggle switch is in ON position
9	ALL ON/OFF toggle switch	Positioning to ON selects all 25 words for processing and readout, regardless of position of other switches
10	LINE 1 indicator (amber)	Lights to indicate that number one line cable is connected
11	LINE 2 indicator (amber)	Lights to indicate that number two line cable is connected
12	LINE 3 indicator (amber)	Lights to indicate that number three line cable is connected
13	POWER ON/RECORD pushbutton indicators (3, red/green)	a. POWER ON positions light to indicate that ac power is available for either oscillograph, digital data printer, or period measure low-speed printer b. RECORD position lights to indicate that record mode of applicable printer has been selected
14	OSCILLOGRAPH pushbutton indicator (red)	Lights when ac power has been applied to the oscillograph by depressing the switch
15	DIGITAL DATA PRINTER pushbutton indicator (red)	Lights when ac power has been applied to the printer by depressing the switch
16	PERIOD MEAS. L. S. PRINTER pushbutton indicator (red)	Lights when ac power has been applied to the printer by depressing the switch
17	PRINT ALL/PRINT SELECTED pushbutton indicator (red/green)	a. PRINT ALL lights to indicate that all 25 words, regardless of selection, are being processed and read out b. PRINT SELECTED lights green to indicate that only selected words of the possible 25 are being processed and read out
18	DIGITAL DISPLAY pushbutton indicator (red)	Not presently used in the system
19	POWER ON/OFF toggle switch	When positioned ON, applies power to control panel No. 1
20	INTERLOCK BYPASS indicator (red)	Lights to indicate that INTERLOCK switch is in BYPASS position
21	INTERLOCK OPEN	Lights to indicate that INTERLOCK switch is in OPEN position
22	POWER ON indicator (red)	Lights to indicate that panel power is available

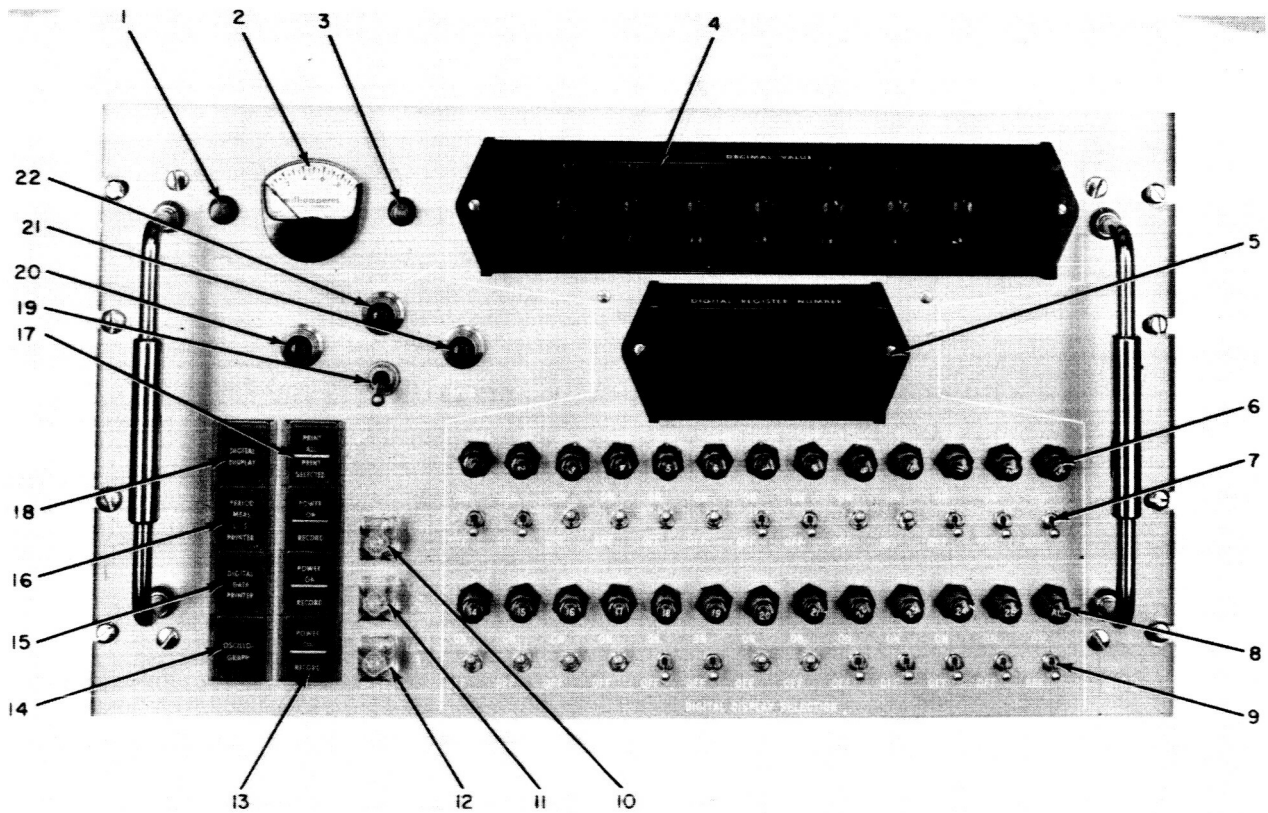


Figure 2-7. Control Panel No. 1, Controls and Indicators

Table 2-8. Control Panel No. 2, Controls and Indicators

FIGURE 2-8 REF. NO.	NOMENCLATURE	FUNCTION
1	DISCRIMINATOR ADJUSTMENTS CAPACITANCE rotary switch	Allows for selection of appropriate range for bit rate used in the discriminator
2	DISCRIMINATOR ADJUSTMENTS OPERATE/TEST toggle switch	TEST position allows use of an external oscillator for calibration of the discriminator
3	DISCRIMINATOR ADJUSTMENTS RESISTANCE potentiometer	Used in initial set-up of discriminator output amplitude
4	CHANNEL BURST PERIOD nixies (5)	Displays the 10-period average, in μsecs, of frequency within the burst being processed
5	HIGH SPEED PRINTER POWER ON/OFF toggle switch	Positioning the switch ON applies ac power to the highspeed printer
6	HIGH SPEED PRINTER POWER ON/OFF indicator (red)	Lights to indicate that ac power has been applied to the highspeed printer
7	OSCILLOGRAPH INPUT SELECTION FRAME rotary switch	Selected frame of data is processed on oscillograph, in conjunction with channel selected
8	SYSTEM INPUT SELECTOR rotary switch	Selects main data input signal
9	OSCILLOGRAPH INPUT SELECTION CHANNEL rotary switch	Selected channel of data is processed on oscillograph, in conjunction with frame selected
10	LOCK indicator (amber)	Lights to indicate that frame sync is locked on
11	FRAME SYNC SEARCH LOCK RESET pushbutton	Initiates the search mode for frame sync when pressed
12	SEARCH indicator (amber)	Lights to indicate that equipment is searching for frame sync

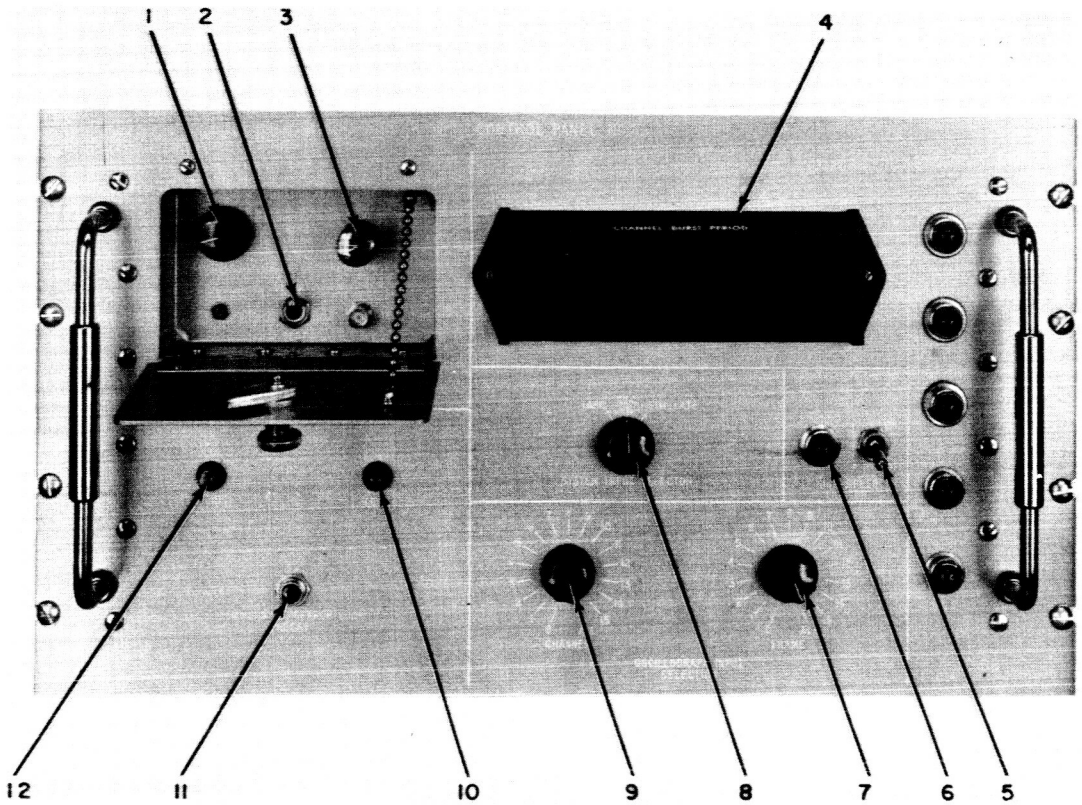


Figure 2-8. Control Panel No. 2, Controls and Indicators

Table 2-9. Control Panel No. 3, Controls and Indicators

FIGURE 2-9 REF. NO.	NOMENCLATURE	FUNCTION
1	ELAPSED TIME INDICATOR meter	Measures the equipment running time
2	AC indicators (2, green)	Lights to indicate that POWER ON/OFF switch is in ON position
3	DC FAIL indicators (2, red)	Lights when dc power supply fails
4	INPUT 7 AMP fuses (2)	Protects each of the dc power supplies
5	SPARE fuses (2)	Spare fuses available, if needed
6	POWER SUPPLY 2 circuit breakers (3)	Circuit protection for power supply along outputs of supplied voltage
7	POWER SUPPLY 1 circuit breakers (3)	Circuit protection for power supply along outputs of supplied voltage
8	POWER ON/OFF toggle switches (2)	Controls the energization of each power supply; in ON position, supplies dc voltage to the system

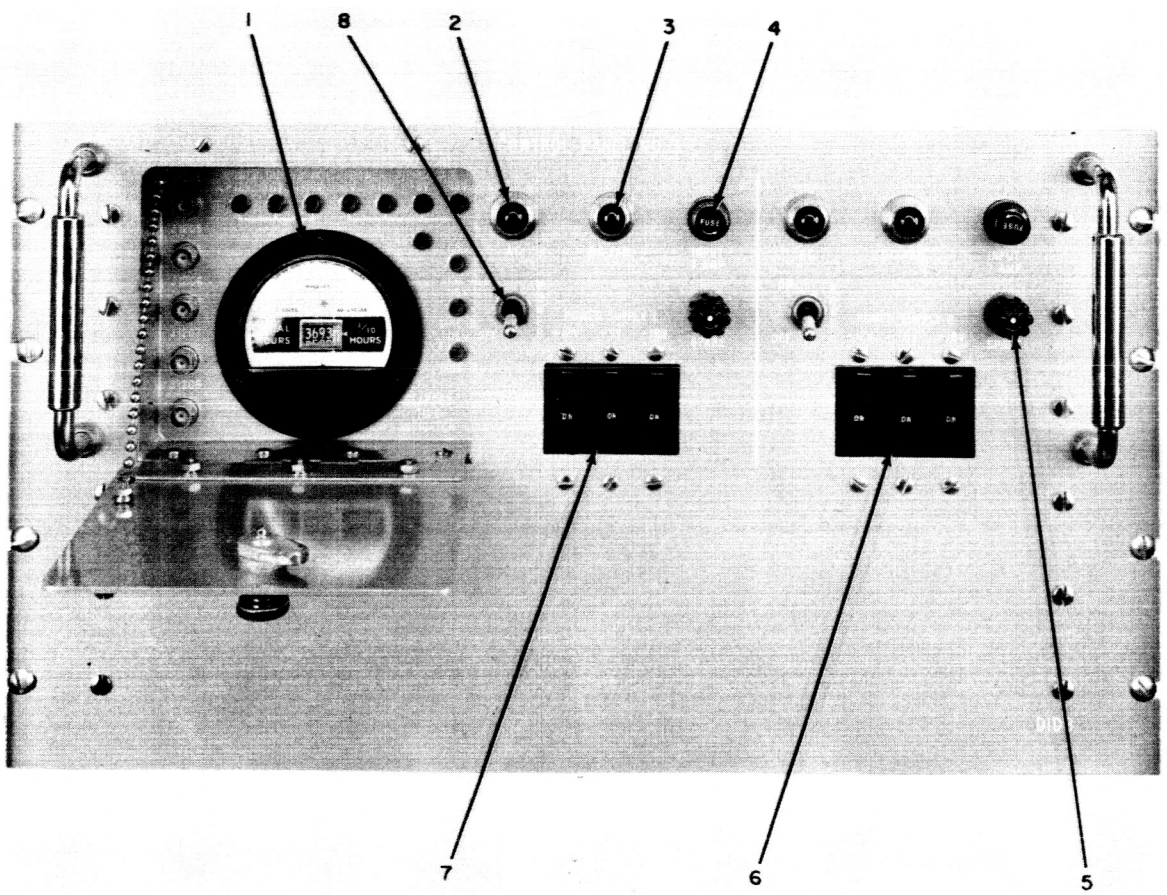


Figure 2-9. Control Panel No. 3, Controls and Indicators

Table 2-10. Rejection Filter Unit, Controls and Indicators

FIGURE 2-10 REF. NO.	NOMENCLATURE	FUNCTION
1	FREQUENCY-CPS rotary switches (4)	Used in pairs to select filter cutoff frequency in digital form for high-pass and low-pass sections of the filter
2	FREQUENCY MULTIPLIER rotary switches (2)	Positioned to determine the factor by which the indicated filter cutoff frequency must be multiplied to determine actual cutoff frequency
3	LOW PASS/HIGH PASS rotary switches (2)	Selection determines whether the applicable filter section is used as high-pass or low-pass filter unit
4	Indicator (red)	Lights to indicate that both power supplies are functioning
5	HIGH PASS DC BALANCE potentiometers (2)	This control balances dc voltages at output terminals to zero volts when filter is operating as a high-pass unit
6	LOW PASS DC BALANCE potentiometers (2)	This control balances dc voltage at output terminals to zero volts when filter is operating as a low-pass unit

NOTE

The rejection filter has high- and low-pass sections and is used as a noise-rejection device. Noise occurring below the low-pass frequency and above the high-pass frequency is rejected. The desired waveforms are tailored to the specific system and should be examined with an oscilloscope when troubleshooting.

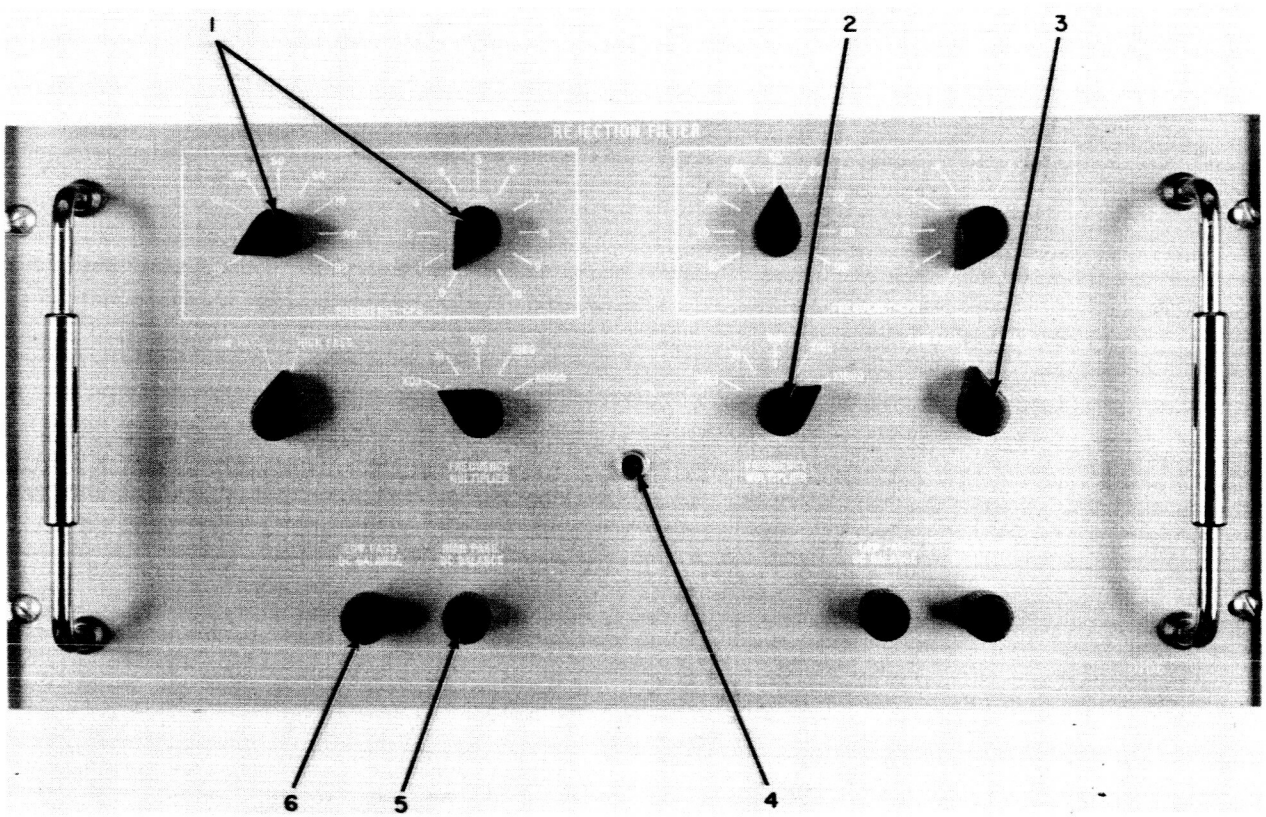


Figure 2-10. Rejection Filter Unit, Controls and Indicators

Table 2-11. Bit Rate Filter Unit, Controls and Indicators

FIGURE 2-11 REF. NO.	NOMENCLATURE	FUNCTION
1	FREQUENCY selector rotary switches (4)	These four switches (together with FREQUENCY multiplier switch) are used for setting filter center frequency
2	FREQUENCY multiplier rotary switch	Multiplies frequency set into FREQUENCY selector switches by factors of 10, in order to cover the frequency range from 1.0 cps to 10,000 cps
3	Indicator (red)	Lights to indicate that power has been applied to the unit
4	SELECTIVITY rotary switch	Used to set the filter bandwidth to one of three selectable values
5	GAIN rotary switch	Used to set the filter gain to selectable db values

NOTE

All controls on this panel function in conjunction with each other to select a specific bit rate. In troubleshooting this unit, the operator must set up the unit using an oscilloscope.

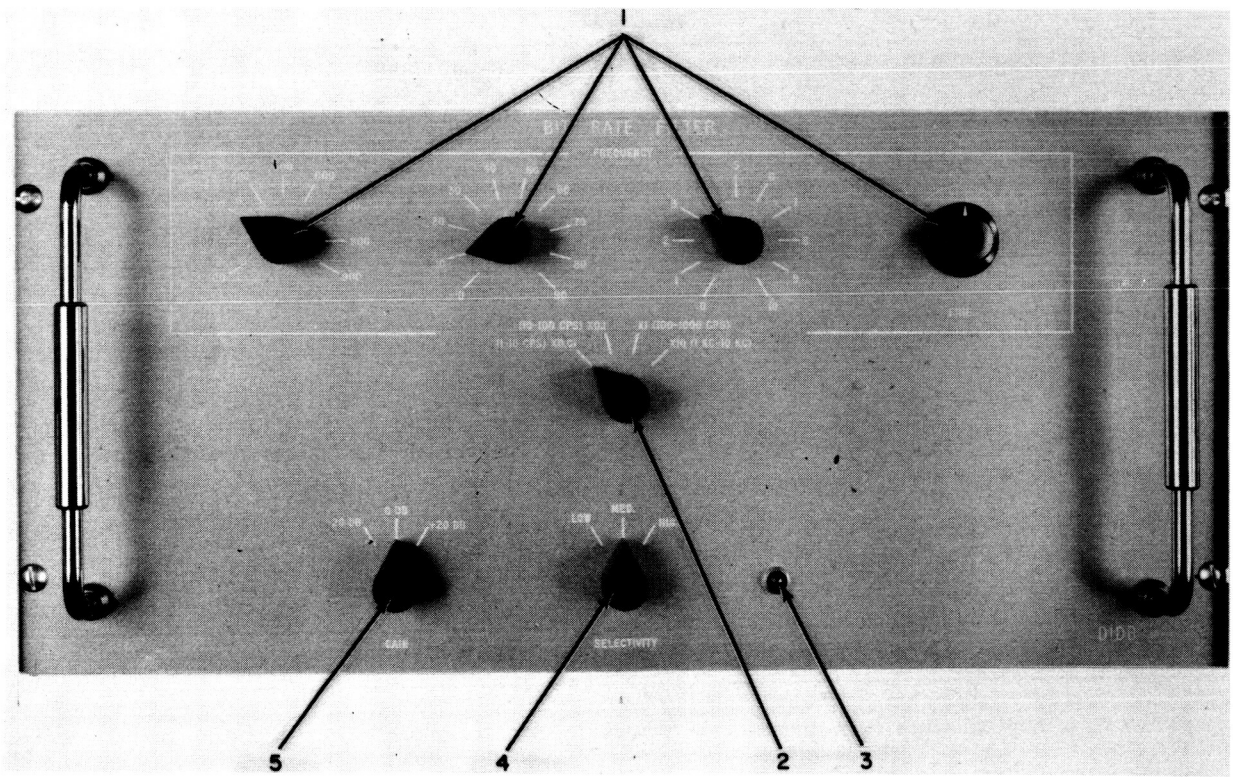


Figure 2-11. Bit Rate Filter Unit, Controls and Indicators

Table 2-12. Special Box Unit, Controls and Indicators

FIGURE 2-12 REF. NO.	NOMENCLATURE	FUNCTION
1	FREQUENCY ADJUST potentiometer	Adjusts frequency that appears during the burst period of a simulated signal
2	SIMULATOR BIT RATE rotary switch	Three selections available providing capability of simulating various bit rates for troubleshooting purposes

NOTE

Each special box will contain a signal simulator and the controls shown here. If a special box is encountered having controls not listed in this table, a complete explanation of them will be found in the appropriate appendix to this volume.

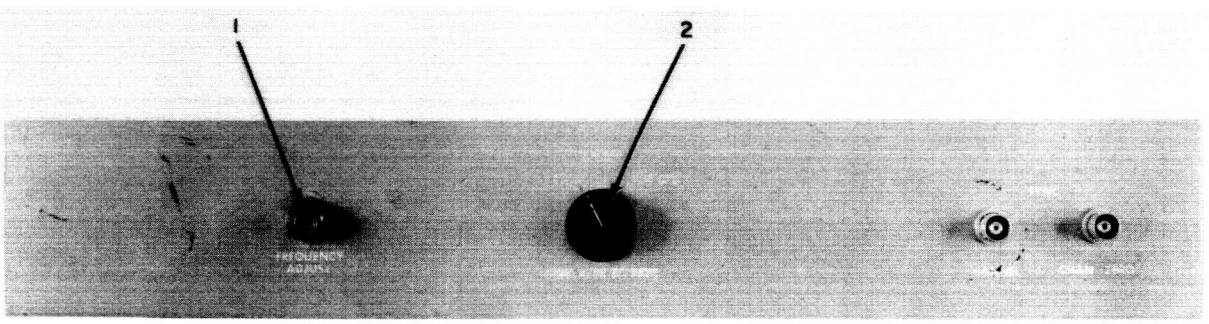


Figure 2-12. Special Box Unit, Controls and Indicators

2.3 PATCHING ARRANGEMENTS

Three patch panels, each with individual patching arrangements, are provided in the equipment. These patchboards are the digital comb filter, and two fixed, pre-wired patchboards, program board No. 1 and program board No. 2. In all cases, program boards No. 1 and No. 2 are utilized in pairs. Each pair is wired and connected for specific data within the satellite format. When one patchboard is replaced, the other patchboard of the pair is also replaced.

2.3.1 DIGITAL COMB FILTER

The digital comb filter, shown in figure 2-13, detects and indicates the presence of a set of discrete frequencies, octally coded, at its input. Specific frequencies are detected by proper insertion of the comb filter pins. The format used in patching the digital comb filter is predetermined by the programmer in accordance with preselected frequencies and should never be altered except when processing data with a different format from a new satellite.

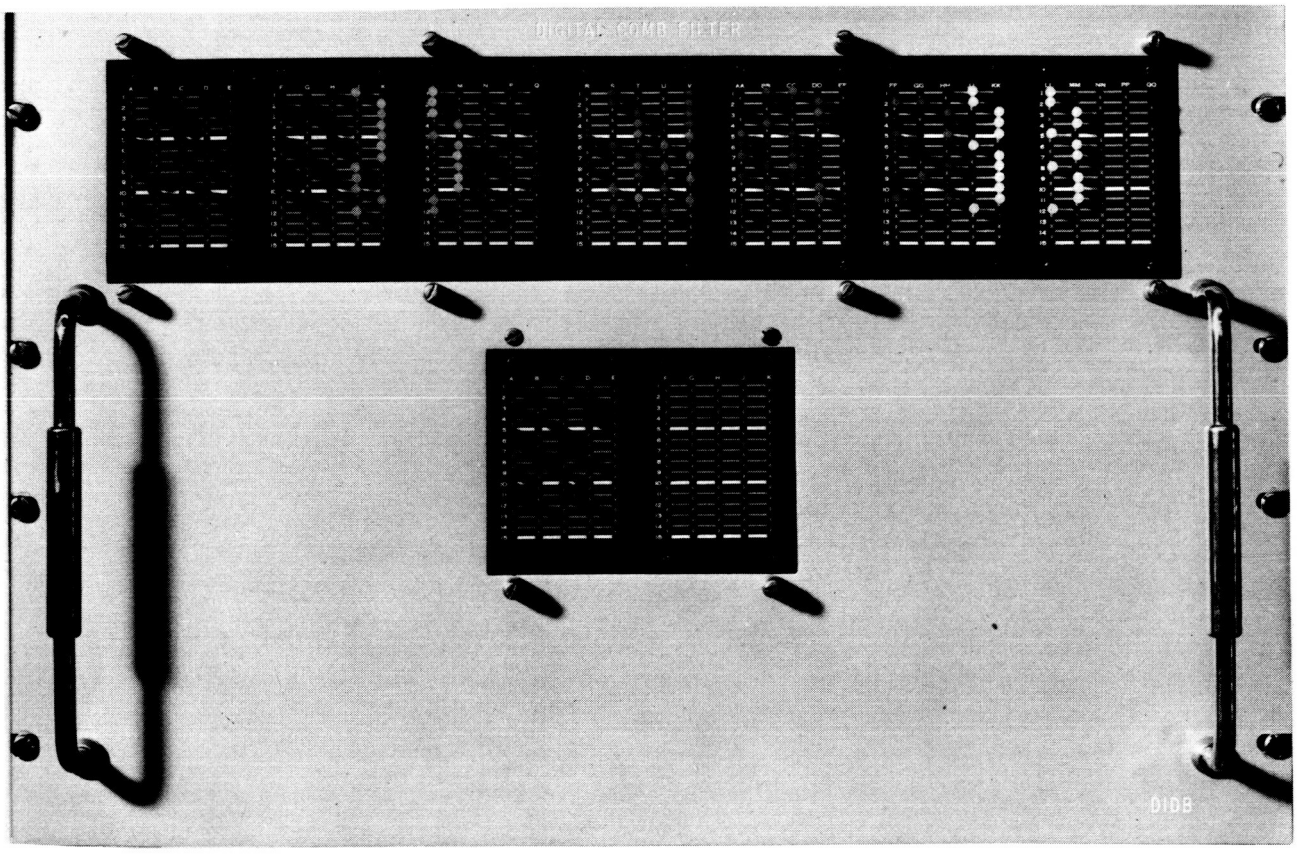


Figure 2-13. Digital Comb Filter

2.3.1.1 The digital comb filter patch panel contains seven panels along the top face of the drawer, and two panels directly below them. Each panel is subdivided into five columns, each column being interlaced by 15 rows, the intersections of which are known as bit-positions. Of the 35 columns available in the top row of patch panels, only 32 are utilized for octal number patching purposes. The 32 utilized columns are divided into eight sections, each section being allotted one octal number. Therefore, columns A, B, C, and D comprise an octal number, which is designated as octal zero. Likewise, columns E, F, G, and H comprise an octal number which is designated as octal one. This coding continues through columns JJ, KK, LL, and MM, which are designated as octal seven. For all eight octal numbers in the aforementioned columns, only 13 rows are used. Each row constitutes one bit of information for that column. The use of 13 bits is specified because the digital comb filter uses a 13-stage counter.

2.3.1.2 Each octally-coded number is assigned upper and lower limits. In the case of octal zero, column A and B represent a binary number equivalent to the upper limit assigned to octal zero. Similarly, columns C and D represent a binary number equivalent to the lower limit assigned to octal zero. The upper and lower limits for each octal number are further subdivided into columns of binary 1's and 0's; i.e., columns A and C represent binary 0 and columns B and D represent binary 1's. Thus, the 13-bit upper limit for octal zero is represented as 001100000111 (reading from 2^{11} to 2^{0}), and the lower limit for octal zero is represented as 001010100011. Translated, the upper limit for octal zero becomes 775 and the lower limit for octal zero becomes 675, for periods of 1.240 ms and 1.080 ms respectively. These numbers are dimensionless and are arrived at by taking the reciprocal of the frequency and multiplying it by the number of periods sampled, which is 10. This product is then multiplied by the selected clock-rate ratio. The result is a ratio of two periods and is, therefore, dimensionless.

2.3.1.3 The bit positions of rows 14 and 15 in columns A through E are patched to select the desired clock-rate ratio. The options are 1/16 of the 1-mc clock rate, 1/8 of the 1-mc clock rate, 1/4, 1/2, or the full 1-mc clock rate.

2.3.1.4 A patching arrangement is also available to control the number of cycles over which an average is taken. This is accomplished by patches QQ1 through QQ6.

2.3.1.5 During each odd frame, and only appearing during channel 0, a signal within the upper and lower limits of the sync oscillator period is sensed. These limits are patched into the left-hand patch panel in the second row of panels in the same manner described for the octal numbers. The sync oscillator can only occur in channel zero and occurs in every odd frame.

2.3.2 PROGRAM BOARDS NO. 1 AND NO. 2

Two program patchboards (figure 2-14) are used in the digital portion of the system only. The program boards are prewired in matched pairs. They allow random location of digital information in a format, and variable word length.

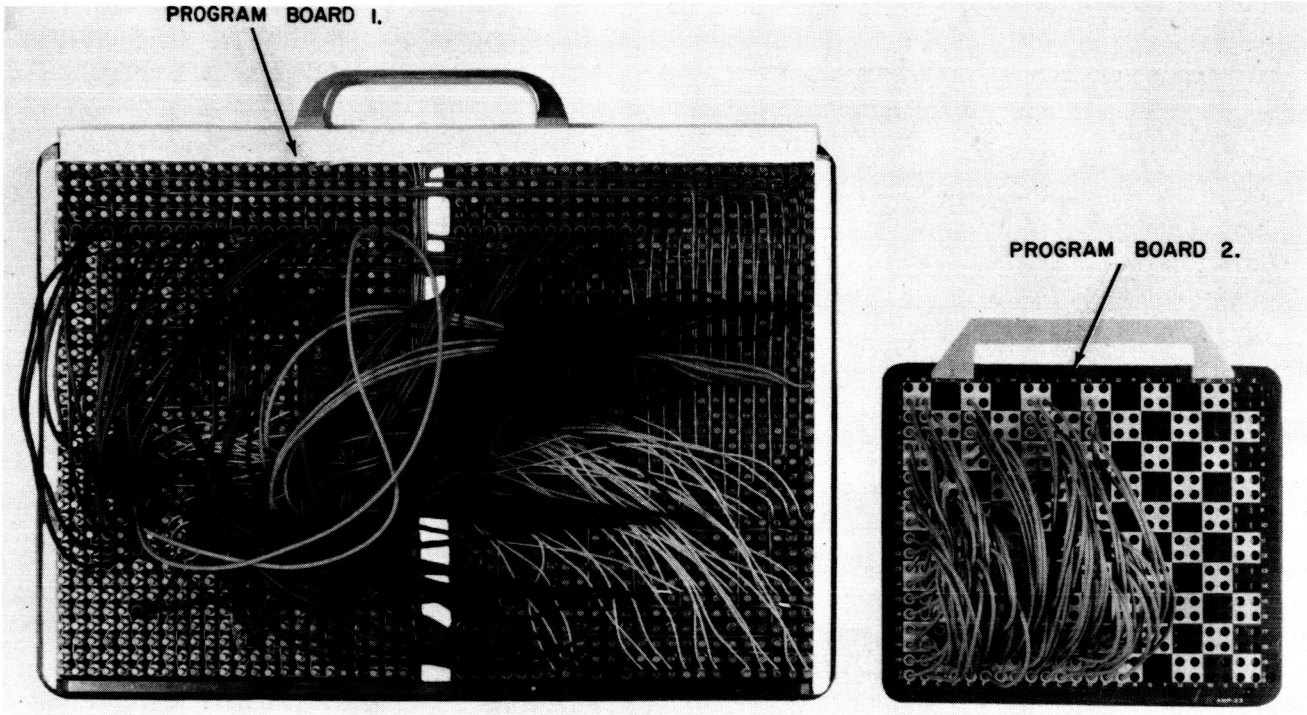


Figure 2-14. Program Boards No. 1 and No. 2

2.3.2.1 Program board No. 2 is the physically smaller of the two, containing 480 holes arranged in 20 rows of 24 holes each. The prime function of this program board is to select those channels in a format which contain digital information and make them available to the larger patchboard. The frame and channel control unit matrix supplies the necessary inputs to program board No. 2 in the form of 256 individual channel pulses. The channel pulses are arranged in an array of 16 x 16 on the patchboard. This array corresponds to 16 channels by 16 frames of the PFM format. Program board No. 2 selects up to 96 possible outputs of the 256 channel pulses for application to program board No. 1, via the inverters in the hold register.

2.3.2.2 Program board No. 1 (figure 6-15 of Volume II), the larger of the two, is a fixed, prewired patch panel which receives up to 96 inverted channel marks from program board No. 2. The larger patchboard selects the proper inputs for each of the individual memory cells being used. The output of each memory cell is hard-wired to the appropriate hold register input, and the full indicator input is selected.

2.3.2.3 The required inputs to any memory cell are as follows: a channel mark, an information bit, a transfer pulse, and a clear pulse. The channel marks are located (on the patchboard) in rows 16 through 19, columns ZZ through AA. The information bits are located on row 16, columns Z through A (2^0 on pins Z-16 through S-16, 2^1 on pins R-16 through J-16, and 2^2 on pins H-16 through A-16). The transfer pulses are found in rows 11 through 15 in columns R through K. Hold register inputs are found in rows 19 through 34 in columns Z through A. The full indicator inputs are located

in row 18, columns Z through A and row 17, column A. The remainder of the patchboard contains the inputs and outputs of the memory cells.

2.3.2.4 To properly patch a digital word, the operator determines which channels of the telemetry are carrying the data for the word. The channels are then selected on program board No. 2, making them available to program board No. 1. Each of the channels selected is patched to three memory cells at the input designated for the channel mark. Three cells per channel are required since each channel contains three bits of digital information. Each of the three cells is associated with a particular channel and must receive a different information bit (2^0 is patched to one cell, 2^1 is patched to another, and 2^2 is patched to a third). The operator now selects a word-number designation; usually the first word to receive all of its information is designated word 1, etc. Having made this designation, the operator patches the proper transfer pulse to the proper input of all memory cells associated with that word (transfer pulse 1 is patched to word 1, etc.). The proper clear pulse is also patched to the proper input of all cells associated with that word in a similar manner. The last channel mark associated with the word is used to indicate that all of the data for that word has been received and the word is ready to be read out. This is accomplished by patching the last channel mark to the proper full indicator input, in addition to patching it to three memory cells. The outputs of the memory cells must be patched to the inputs of the hold register (the least significant bit of the word in memory is patched to the least significant bit of the hold register, etc.).

2.4 NORMAL OPERATING CONDITIONS

The normal operating conditions for the data-reduction system are established when the equipment is set up, operated, and shut down in compliance with the procedural steps which follow.

2.4.1 SET-UP PROCEDURE

To set up the equipment prior to a mission, proceed as follows:

a. Insert the pair of program boards No. 1 and No. 2.

b. Set up digital comb filter for applicable channels and sync oscillator frequency.

c. On control panel No. 2, set SIMULATE position onto SYSTEM INPUT SELECTOR rotary switch.

d. Set appropriate bit rate into simulator on SIMULATOR BIT RATE rotary switch.

e. On rejection filter panel, set FREQUENCY-CPS switches (1, table 2-10), to desired cutoff frequency.

f. On rejection filter panel, set FREQUENCY MULTIPLIER switch (on left-hand side of panel), to appropriate multiplication factor to achieve high-pass filter action.

g. On rejection filter panel, set LOW PASS HIGH PASS switch (on left-hand side of panel), to HIGH PASS.

h. On rejection filter panel, set HIGH PASS DC BALANCE potentiometer (5, table 2-10), to balance output terminals.

i. On rejection filter panel, repeat steps e. and f. for second frequency on appropriate switches on right-hand side of panel.

j. Set LOW PASS HIGH PASS switch (3, table 2-10), to LOW PASS.

k. Set LOW PASS DC BALANCE potentiometer (6, table 2-10) to balance output terminals.

l. On bit-rate filter panel, set up desired bit rate frequency on three FREQUENCY rotary switches.

m. On bit-rate filter panel, set frequency multiplier rotary switch to appropriate multiplication factor.

n. Adjust frequency with FINE potentiometer.

o. On bit-rate filter panel, set SELECTIVITY rotary switch to MED.

p. On bit-rate filter panel, set GAIN rotary switch to 0 DB.

q. On bit synchronizer panel, set BIT RANGE switch such that the selected bit rate is within the range of the switch setting.

r. On bit synchronizer panel, set EXT. METER toggle switch to IN.

s. On frame and channel control upper panel, select desired position of FRAME SYNC RECOG rotary switch.

t. On upper frame and channel control upper panel, select desired position of FRAME SYNC RECOG rotary switch.

u. On lower frame and channel control panel, set CHANNEL PROGRAMMING toggle switches to binary number equivalent to number of channels per frame.

v. On lower frame and channel control panel, set FRAME PROGRAMMING toggle switches to binary number equivalent to number of frames per sequence.

w. On lower frame and channel control panel, set IN PHASE COUNTER toggle switches to appropriate positions for locked indication.

x. On lower frame and channel control panel, set OUT OF PHASE COUNTER toggle switches to appropriate positions for searched condition.

y. On printer programming panel of printer code converter, set BURST/BLANK toggle switch to position desired.

z. On printer programming panel of printer code converter, make the following adjustments:

1. Set INPUT rotary switch to INT position.

2. Select number of incoming data periods to be deleted by manipulating PERIOD MEASUREMENT PULSE DELETE toggle switches.

Following steps are required only if high-speed printer is used.

3. Set desired word length with WORD LENGTH toggle switches.

4. Connect selected DECADES jacks to selected SEQUENCE jacks with patching cords provided as necessary to comply with program (see 3.3.8.2.1).

5. Set H. S. PRINTER CONTROL switch to OPERATE position.

6. Set READOUT CONTROL switch to INT position.

2.4.2 OPERATING PROCEDURE

To energize the system and to operate the equipment in preparation for and during a mission, proceed as follows:

a. On control panel No. 3, ensure that DC POWER switches are in OFF position.

b. On control panel No. 1, set ac POWER switch ON.

c. On control panel No. 3, set six circuit breakers ON.

d. On control panel No. 3, set dc POWER switches ON.

e. On bit synchronizer panel, set OPERATE/SET toggle switch to SET.

f. Using oscilloscope, adjust PHASE ADJUSTMENT potentiometer until flywheel is in phase with incoming telemetry signal.

g. Disconnect oscilloscope.

h. Adjust BIT RATE ADJUSTMENT potentiometer to correspond to selected bit rate, related to meter.

i. On upper frame and channel control panel, using an oscilloscope adjust INTEGRATION SYNC ADJ potentiometer to trigger at channel 0, without other channels causing triggering.

j. On bit synchronizer panel, set OPERATE/SET toggle switch to OPERATE.

k. On control panel No. 1, depress DATA PRINTER pushbutton.

l. On control panel No. 1, depress PERIOD MEAS. PRINTER pushbutton.

m. On period readout control panel, select channels to be printed out by selecting desired sequences, frames, and channels.

n. On control panel No. 1, depress period measurement printer RECORD switch.

o. On control panel No. 1, select digital words to be read out.

p. On control panel No. 1, depress digital data printer RECORD pushbutton.

q. On control panel No. 1, depress OSCILLOGRAPH pushbutton.

r. On oscillograph, depress desired speed pushbutton.

s. On control panel No. 2, set OPERATE/TEST toggle switch to TEST.

t. With oscillator connected to DISCRIMINATOR portion of control panel No. 2, adjust width of oscillograph trace using settings of CAPACITANCE switch and by rotating RESISTANCE potentiometer.

u. On upper galvanometer amplifier, vary oscillograph trace using channel 1 potentiometer.

v. On control panel No. 2, set OPERATE/TEST toggle switch to OPERATE.

w. Remove oscillator from DISCRIMINATOR portion of control panel No. 2.

x. Depress PRINT SELECTED/PRINT ALL pushbutton on control panel No. 1 to desired position.

NOTE

After POWER pushbutton is ON on control panel No. 1, manually control oscillograph.

y. On control panel No. 2, select desired FRAME and CHANNEL positions.

z. On control panel No. 2, set SYSTEM INPUT SELECTOR rotary switch to either REC or TAPE, as desired.

aa. Adjust indicator potentiometers and BIT RATE ADJUSTMENT, on bit synchronizer and frame and channel control panels, after selected mode is reached.

ab. Change experiments on period readout control panel as desired during operation.

ac. Change digital words on control panel No. 1 as desired during operation.

2.5 NORMAL AND EMERGENCY SHUTDOWN PROCEDURES

To cease operation of the equipment either under normal conditions or under emergency conditions, the following procedures apply:

a. On control panel No. 3, position dc POWER switch to OFF.

b. On control panel No. 1, position ac POWER switch to OFF.

SECTION III.
THEORY OF OPERATION

3.1 APPROACH

This section discusses the theory of operation of the Universal PFM Real-Time Data Reduction System at the block diagram level. First, there is a functional description of the entire system, followed by a detailed discussion of each unit of the system. Nonstandard circuits designed and built by Goddard Space Flight Center are also described in detail.

3.2 SYSTEM FUNCTIONAL DESCRIPTION

Figure 3-1 is a functional block diagram of the entire data-reduction system. It is divided into three major sections: system timing, digital signal processing, and analog signal processing. Each section is discussed below.

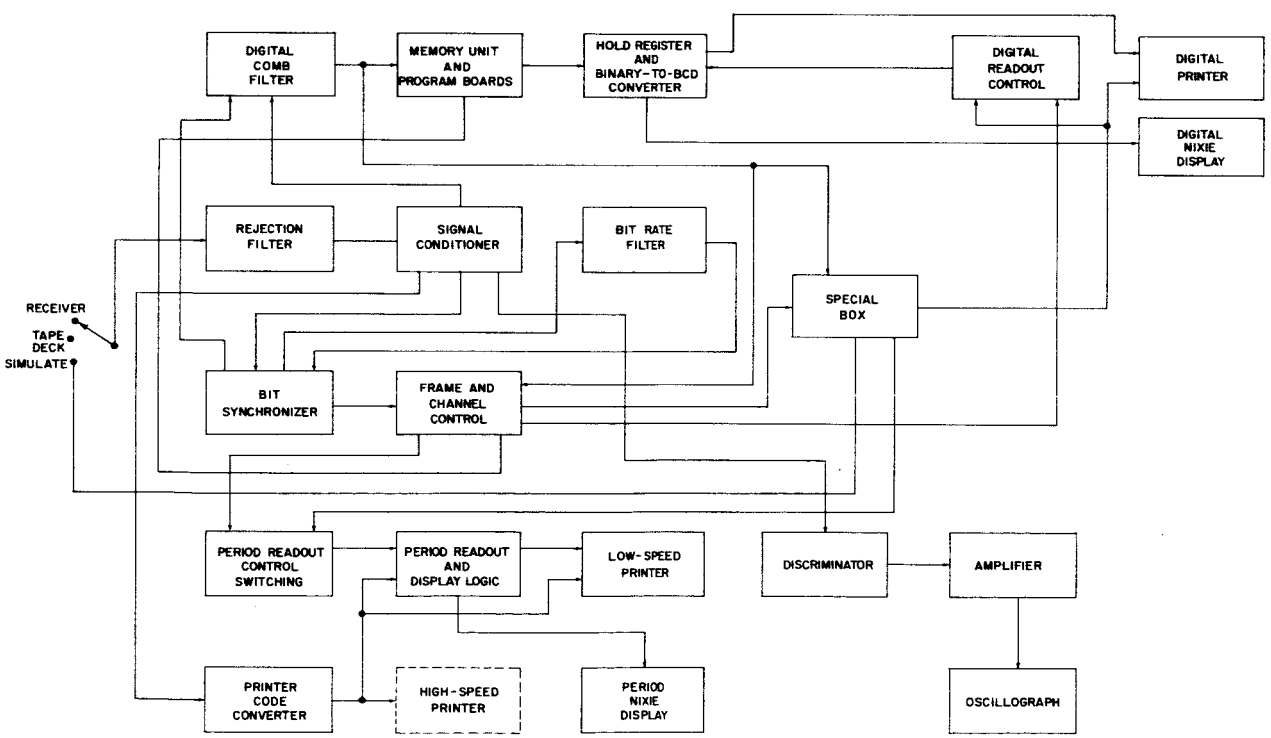


Figure 3-1—Universal PFM Real-Time Data-Reduction System No. 1, Functional Block Diagram

3.2.1 SYSTEM TIMING SECTION

3.2.1.1 The PFM input signal may be from a receiver, a tape deck, or from a signal simulator located in the special box. The signal is first fed into the rejection filter for noise reduction, and then into the signal-conditioning circuits. The rejection filter is of standard commercial design. It may be operated as a high-pass or low-pass filter depending on the requirements of the particular situation. The signal conditioning circuits further improve the signal-to-noise ratio by providing limiting and AGC action. After power amplification, the AGC response signal is fed to a burst-blank detector (part of the bit synchronizer), the digital comb filter unit, the printer code converter unit, and to the discriminator which develops an analog signal proportional to the burst frequency to drive the oscillograph.

3.2.1.2 To decommutate the incoming telemetry signal, it is necessary to reconstitute the satellite clock. This process is initiated by detecting the burst-blank envelope in the burst-blank detector. The detected envelope is fed into the bit-rate filter (a bandpass filter of commercial design with its center frequency set to the data burst rate) used for noise reduction. The output from the filter is a sine wave at the telemetry bit rate which is relatively immune to noise. This sine wave is then fed back into the bit synchronizer and serves as the basis for the timing pulses used for system synchronization.

3.2.1.3 By rephasing and shaping, the sine wave is converted to a square wave with a pulse every burst-blank time at the telemetry bit rate. The square wave is used to compensate a voltage-controlled oscillator (VCO) whose output is the reconstituted satellite clock. In the event of signal fading or loss of sync pulse recognition due to CW transmissions, the VCO and its associated circuits function as an electronic flywheel providing a continuous square wave output, as well as the usual strobe pulses. The reconstituted clock signal (called the flywheel signal) is used by the frame and channel control unit and the printer code converter unit. Strobe pulses generated in the bit synchronizer are used by the frame and channel control unit and the digital comb filter.

3.2.1.4 The frame and channel control unit decommutates the incoming PFM data train into frames and channels. To do this it operates in conjunction with the bit synchronizer and digital comb filter. The first step in decommutation is to acquire frame sync. This may be done in one of four ways by the frame and channel control unit, depending on the format of the satellite PFM telemetry signal: (1) The unit can recognize a wide frame sync burst; (2) It can lock on a discrete sync recognition frequency appearing in the frame sync channel (Recognition of the frequency is done in the digital comb filter.); (3) When both types of frame sync information are transmitted by a satellite, it can acquire sync by recognition of the wide burst or the frame sync frequency; or, (4) It can require the coincident occurrence of the wide burst and the frame sync frequency.

3.2.1.5 The frame and channel control unit contains a search and lock section which determines the acquisition of frame sync with a programmable degree of confidence. It evaluates a predetermined ratio of valid-to-false frame sync recognition signals detected to assure that frame sync has been acquired. Until this ratio is attained, the system remains in the search condition and operation of the digital-processing section is inhibited. Once the programmed number of

valid sync pulses have been counted, the system goes into the lock mode and processing of digital data begins. If, after the system is in synchronization, a programmed number of false frame sync recognition pulses are recognized, the system reverts to the search mode and digital data processing is again inhibited. Reacquisition of frame sync is done automatically.

3.2.1.6 The actual decommutation of the PFM signal is accomplished in the digital and analog-signal processing sections of the systems using channel and frame marker pulses derived in the frame and channel control unit by counting down the flywheel signal. The flywheel signal is first counted down by a channel sorter circuit to derive channel marker pulses, and further counted down by a frame sorter to derive frame marker pulses. The pulses from the channel and frame sorters are combined in a frame and channel matrix which provides sequentially a marker pulse for every channel of every frame. The sorter and matrix circuits are designed for a standard 16 channel by 16 frame PFM format; however, they are programmable so that nonstandard formats may be accommodated.

3.2.1.7 The frame sorter is updated by a frame corrector circuit every even-number frame to assure sync with the telemetry signal. An octally-coded frame identification frequency is decoded in the digital comb filter every even-number frame, and used to force the frame sorter to the proper frame count if it is not already in step with the incoming signal.

3.2.2 DIGITAL DATA-PROCESSING SECTION

3.2.2.1 The conditioned PFM telemetry signal is fed to the digital comb filter which quantizes the data bursts containing digital information. Since there are eight subcarrier oscillator frequencies assigned for the transmission of digital data, and a ninth for frame sync, the comb filter is programmed to determine the average period in microseconds of each digital burst, and to generate an appropriate signal in one of nine output channels corresponding to the frequency of the burst. The three information bits for each digital burst are transferred through a program board to appropriate cells of the memory unit, and the frame sync recognition signal is fed back to the frame and channel control unit for use by the frame sync and frame corrector circuits.

3.2.2.2 The memory unit consists of 200 cells. Each cell accepts one bit; therefore, three cells are needed to receive the octal number from each digital data burst. For cells to accept the bits from a particular burst, the bits must appear in coincidence with the proper channel marker. When the number of cells equivalent to a word have been filled, a transfer pulse is received from the digital readout control which transfers the word in parallel from the memory to a 21-bit hold register. Word length is variable, and is determined by programming.

3.2.2.3 Following the transfer of the word from the memory unit to the hold register, the digital readout control generates a clear pulse which clears the memory cells associated with the word, and begins the shifting of the word from the hold register into the bcd converter. Following 21 shift pulses, the binary-to-bcd conversion is completed, and a print command is generated by the digital readout unit. At this time the decimal equivalent of the word is printed out by the digital printer and displayed by nixie tubes on the digital display.

3.2.3 ANALOG SIGNAL-PROCESSING SECTION

3.2.3.1 The processing of analog data is controlled by the period readout control switching section. This section consists of 289 toggle switches which function with the readout and display logic circuit to include or exclude any sequence, frame, or channel of information in the analog data readout. The 289 switches are divided into 256 channel switches, 16 frame switches, 16 sequence switches, and one master sequence switch, which are connected to the frame and channel matrix of the frame and channel control. Placing a switch in the OUT position prevents a print command from being generated in the period readout and display logic section so that the data in the channel, frame, or sequence associated with the switch cannot be printed out.

3.2.3.2 The conditioned PFM signal is fed to the printer code converter along with the flywheel signal. In the printer code converter, the 10-period average of the modulation frequency of each burst (or blank) is determined and made available in bcd form for the period printer and period display. A "start readout" command is sent to the period readout and display logic section by the printer code converter at the proper time. Those channels, frames, and sequences whose readout control toggle switches are in the IN position are then printed out and displayed by the period nixie display. The bcd-to-decimal conversion for the printer is done in the printer, and the conversion for the nixie display is done by the period readout and display logic section. Provision is made in the printer code converter to accommodate a high-speed printer if one is required.

3.2.4 SPECIAL BOX

The special box contains circuits necessary to adapt the data-reduction system to a particular PFM telemetry format. In addition, it provides a simulated signal for test purposes which closely conforms to the characteristics of the PFM signal being processed.

3.3 UNIT FUNCTIONAL DESCRIPTIONS

3.3.1 BIT SYNCHRONIZER

3.3.1.1 The bit synchronizer has three purposes:

- It improves the signal-to-noise ratio of the raw incoming telemetry signal.
- It detects, demodulates, and reconstructs the satellite encoder clock waveform, providing a square wave output which has approximately the same period and phase as the satellite encoder clock. The signal will persist with the same period and phase during times when the encoder clock is not available for comparison, as during telemetry fading and CW transmissions.
- It provides strobing pulses which are used to prevent spikes caused by transition and propagation delays from introducing errors into the system.

A functional block diagram of the bit synchronizer appears in figure 3-2. Logic block diagrams of the bit synchronizer appear as sheets 1, 2, and 3 of figure 6-2 of Volume II. Schematic diagrams of special circuit cards used in the unit appear on sheets 2 and 3 of figure 6-17, Volume II. Functional descriptions of the special circuits are given in paragraph 3.3.14 of this volume.

3.3.1.2 To improve the signal-to-noise ratio, the incoming signal is first processed by a group of signal-conditioning circuits which includes a protective limiter and AGC detector circuit. The burst-blank envelope is then extracted from the AGC response signal, peaked and refined to a sine wave by the bit rate filter (a bandpass filter tuned to the bit-rate frequency), and then is reshaped. The AGC response signal is also used at the digital comb filter, the printer code converter, and the discriminator of the oscillographic recorder. The digital comb filter and the discriminator are coupled to this signal by the TEST/OPERATE switch on control panel No. 2, and by gating circuits within the bit synchronizer which are controlled by the OSCILLOGRAPH INPUT SELECTION (FRAME and CHANNEL) switches of control panel No. 2.

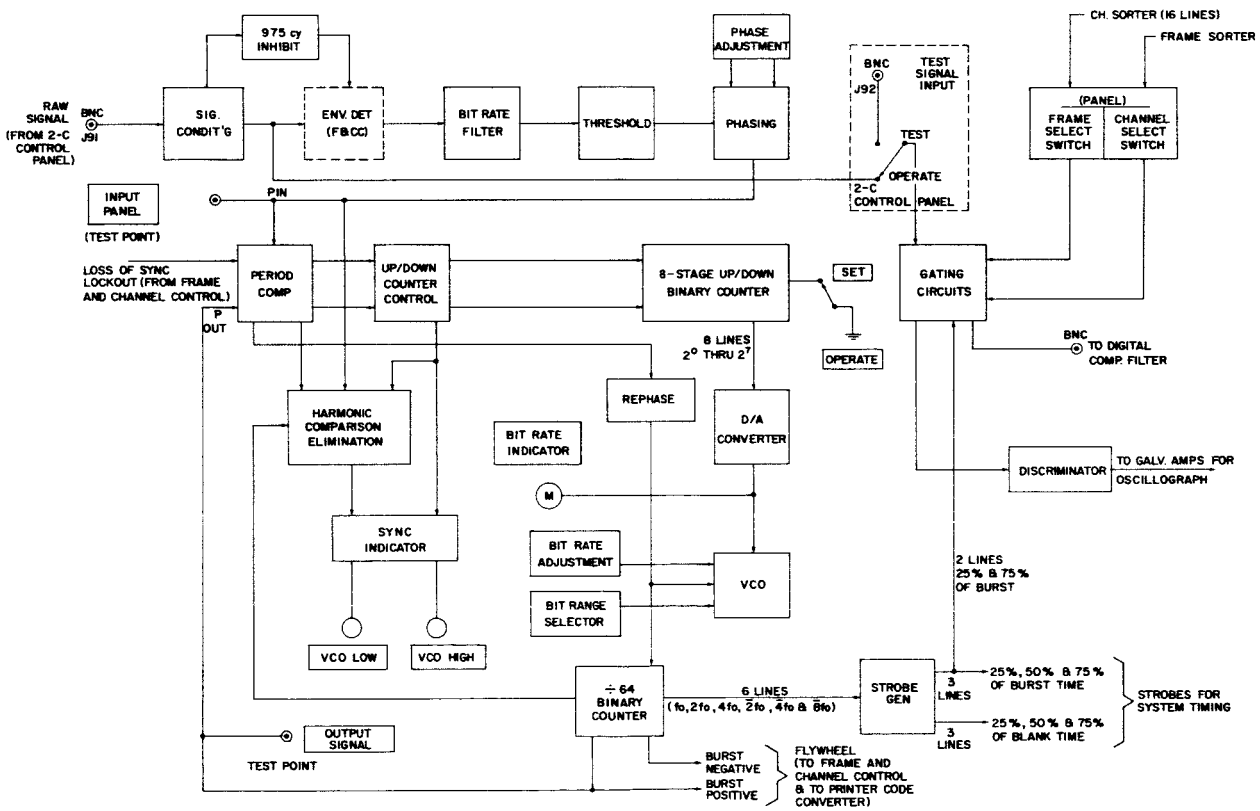


Figure 3-2—Bit Synchronizer, Functional Block Diagram

3.3.1.3 To reconstruct the satellite encoder clock, the burst-blank envelope is extracted from the AGC response signal by the data-burst detector portion of the integrate-and-dump envelope detector, the voltage response of which is coupled to the input of a programmable bit-rate filter. This filter,

which is tunable by the operator over a wide range of frequencies, is the commercially available model 720 bandpass filter manufactured by the Dytronics Company of Columbus, Ohio. Passing the signal through this filter with its center frequency tuned to match the data burst rate minimizes width modulation and provides immunity to noise in the form of randomly occurring input pulses. The filter is designed to have a Q of between 10 and 15; consequently, signal build-up and decay time within the filter takes place during a period approximately equal to 10 to 15 cycles of the input signal.

3.3.1.4 The output signal of the bit-rate filter is a sine wave, which must be phase-compensated and reshaped before being coupled to the period comparator, where it is then used to regulate the electronic clock. It is therefore coupled by a threshold detector circuit to a shaper which can be programmed by the operator with a BIT RANGE SELECTOR switch and PHASE ADJUSTMENT potentiometer. The output of the shaper is a square wave, the period of which is immune to amplitude changes in the input sine wave. To inhibit any response from the filter which does not dependably represent the signal data-burst rate, the threshold detector is biased to recognize when the filter output response has reached a voltage equal to two-thirds that of its peak voltage. The output of this detector controls a gate which passes or inhibits the square wave output signal from the shaper. In this way, the period comparator will be presented with either a dependably good representation of the data-burst rate or no signal at all.

3.3.1.5 Because the bit-rate filter introduces a phase lag between the leading edge of the data-burst detector output signal and that of the output signal from the shaper, rephasing is necessary when the square wave signal from the shaper is coupled to the period comparator. This is accomplished by using a special rundown circuit card to control the timing of the flip flop generating the shaper output signal. When the BIT RANGE SELECTOR switch and PHASE ADJUSTMENT controls are properly set, the negative-going-edge of the square wave output signal from the shaper is exactly in phase with the leading edge of the detected burst-blank envelope of the telemetry signal. The input signal to the period comparator, therefore, is a pulse every burst-blank time at the real-time signal bit rate, the negative-going edge of which coincides with the beginning of the frequency burst of the received telemetry signal.

3.3.1.6 At the period comparator, the input signal (the square wave signal representative of the telemetry signal burst-blank envelope) serves as the standard of comparison for regulating the output signal (the square wave flywheel signal) which is controlled by the VCO. A servoloop is formed by the period comparator, an up/down counter control circuit, an eight-stage up/down binary counter, a digital-to-analog converter, the VCO, and the divide-by-64 binary counter which generates the flywheel burst signals from the output signal of the VCO. The frequency of the VCO is regulated by the voltage applied to its input terminals. When the period of the output signal is larger or smaller than the period of the input signal, the up/down counter control flip flop is set or reset by the period comparator so that the digital number stored by the up/down counter will change accordingly. Since the regulating voltage applied to the VCO is proportional to this digital number, any such change is converted to a change in the operating frequency of the VCO. This conversion is accomplished by the digital-to-analog converter, which has a resolution of 1/256 with respect to

the number stored by the up/down counter. A full-scale change in the VCO regulating voltage, from zero volts to -4 volts, produces a 4-percent change in the frequency of the VCO output signal. Consequently, a change in the least significant bit of the up/down counter results in a change of 0.016 percent (0.04/256) in the frequency of the VCO output signal.

3.3.1.7 When, for example, the period of the output signal is larger than that of the input signal, a correction must be made to reduce the period of the output signal, in order to establish equilibrium between the telemetry signal bit rate and the output bit rate of the bit-synchronizer flywheel burst. Since the output bit rate is proportional to the voltage-controlled oscillator frequency, the correction must decrease the period of the VCO. To accomplish this, the comparison circuit, finding the output period longer than the input period for two consecutive comparisons, commands the up/down counter to count up (that is, to store a new number which is greater than the previous number by one bit). In turn, the digital-to-analog voltage converter correspondingly provides an increased voltage at its output which shortens the period of the VCO output and, consequently, the output of the bit synchronizer. This newly established period will then be compared with the input period at the next data burst time. If the output period is still too long, the bit synchronizer repeats the same procedure and shortens the period again. Comparisons at each data burst time are made until the output period becomes one incremental period step shorter than the input period, at which time the reverse situation takes place; that is, a correction is made to lengthen the output period. The procedure by which this correction is made is analagous to that already described, except that all commands are opposite to those for shortening the output period. The correction, requiring two burst-blank periods, makes the output period either prefect or one incremental period step too long. A settled condition then occurs where the up/down counter continually corrects first one count up and then one count down, in which case the output-bit rate will be varying within ±0.016 percent of the true bit rate.

3.3.1.8 For the synchronizer output signal to maintain proper phasing with respect to the input signal, rephasing is effected at the beginning of the input signal period each data burst time. The six-stage binary counter is reset at this rephasing time to ensure that the divide-by-64 function will always begin at the start of a new full period. When signal dropout occurs, or sync recognition is impaired by continuous-wave transmissions, the period comparator is temporarily disabled by the loss-of-sync lockout signal from the frame and channel control unit. No comparisons are made when this condition exists, and the digital number stored by the up/down counter cannot change. This locks the period of the output signal from the VCO and an electronic-flywheel effect results as the bit synchronizer provides a continuous square-wave output signal, and strobing pulses, at the bit rate established during the most recent comparison time.

3.3.1.9 The bit-synchronizer functional section includes sync indicator circuits and front panel controls which enable the operator to initially adjust the VCO output signal frequency, at 64 times the bit rate, until it is within the range of control of the servo loop. VCO HIGH and VCO LOW indicator lights serve as a visual tuning aid. Each light is connected to the up/down counter control flip flop so that a prediction as to whether the VCO frequency is too high or too low can be made by watching which light is on. Using the lights as a guide, the operator can adjust the VCO frequency

with the BIT RATE ADJUSTMENT control until a quasistable state is reached in which both lights flicker on and off evenly due to the control flipflop continually changing state with each data burst input signal. A SET/OPERATE switch is provided which further assists in adjustment of the VCO by clamping the up/down counter to a half count (SET position). This operation drives the VCO to center frequency of its range, thereby inhibiting the VCO from being continually swept through its frequency range by the up/down counter. When the operator sees from the indicating lights that he has adjusted the VCO to a frequency at the threshold of being neither too high nor too low, he puts the switch in the OPERATE position, thereby releasing the clamp and allowing the synchronizer to servo. To prevent the lights from falsely indicating that bit-rate synchronization has been established when the output-signal frequency is a harmonic of the input-signal frequency, harmonic comparison elimination logic circuits are used which force the VCO HIGH indicator light to remain energized when the period of the output signal is less than two-thirds the period of the input signal. When this condition is corrected, normal control of the indicator lights by the up/down counter control flipflop is resumed.

3.3.1.10 The strobe generator section of the bit synchronizer consists of an input matrix formed by NAND gates, six delay multivibrators which generate 200-microsecond wide strobe pulses, and 12 output inverter amplifiers. Six lines from the set and reset outputs of four stages of the divide-by-64 binary counter driven by the VCO are coupled to the matrix of the strobe generator section. Inverter amplifiers coupled to the assertions and negation outputs of each of the six strobe pulse generators make positive and negative strobes for 25 percent, 50 percent, and 75 percent of the burst (and of the blank) period available at the output terminals of the strobe generator section.

3.3.2 FRAME AND CHANNEL CONTROL

The frame and channel control unit, working in combination with the bit synchronizer and digital comb filter, decommutates the PFM signal by frames and channels. For purposes of discussion the frame and channel control functional section is divided into subsections (as shown in figure 3-3) consisting of frame sync recognition, sync search and lock, channel sorter, frame sorter, frame and channel matrix, and frame corrector. A logic diagram of the frame and channel control section appears as sheets 1 through 6 of figure 6-3 in Volume II. A schematic diagram of the integrate-and-dump detector is shown in figure 6-17, sheet 1, of Volume II.

3.3.2.1 General Discussion

The frame sync recognition section provides the operator with a choice of sync recognition modes. It includes the special circuit card which extracts the burst-blank envelope from the AGC response signal and generates positive frame sync recognition pulses. It also provides special lockout gating circuits for decoupling the detected burst-blank envelope signal from the input of the bit-rate filter, and logic to implement the mode of sync recognition chosen by the operator. The sync search and lock section contains (a) time-coincidence logic and programmable counters for evaluating the ratio of valid-to-false sync recognition signals detected, (b) a loss of frame sync recognition signal detector and delayed reset circuit, (c) the logic which provides the operator with a visual

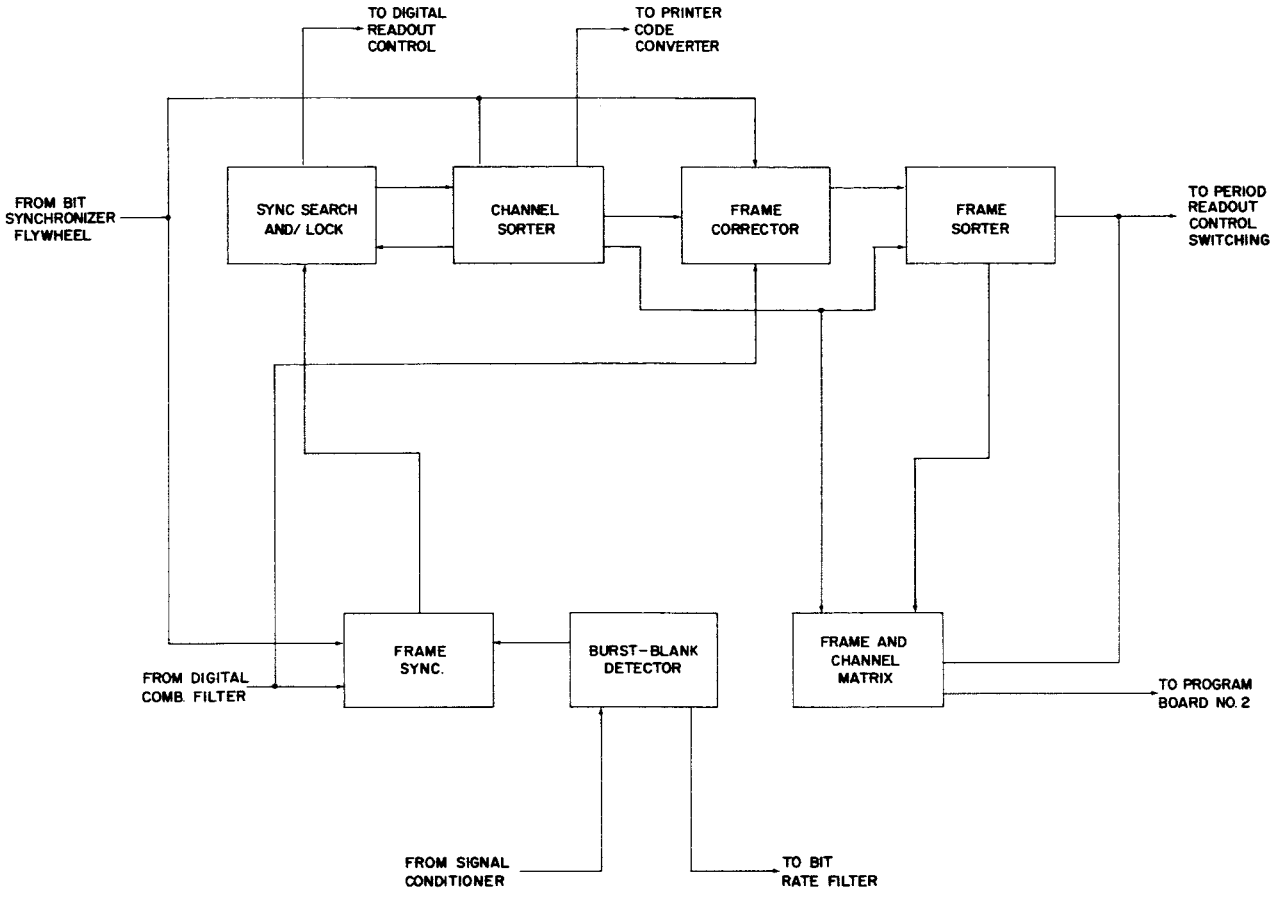


Figure 3-3—Frame and Channel Control, Functional Block Diagram

indication of whether the system is searching for sync or has acquired sync with the telemetry signal, and (d) a reset gate which controls the binary counter of the channel sorter. The channel sorter and frame sorter sections each consist of a four-stage binary counter with a programmable count selector and NAND gated output matrix. The outputs of these matrices are combined in the frame and channel matrix section to obtain 256 sequential pulses for decommutating the telemetry signal. The frame corrector section consists of a diode matrix which converts octal number frame identification signals, detected by the digital comb filter, into control signals which keep the frame sorter updated.

3.3.2.2 Frame Sync Recognition

Two distinct types of frame sync recognition information are usually included in the PFM telemetry format, so that (A) the frequency burst time of each channel zero transmission is 50 percent greater (wide burst) than that of all other channels, and, (B) a discrete sync recognition frequency (the sync oscillator frequency) appears in the wide burst of alternate channel zero transmissions. However, the presence of type (B) information should not always be expected, since a PFM format may be

encountered occasionally which does not include a sync oscillator frequency. When both types of information are present, the operator has a choice of the following sync recognition modes: (1) recognition of type (A) information only; (2) recognition of type (B) information only; (3) recognition of either type (A) or type (B) information; and, (4) recognition of each time coincident occurrence of type (A) and type (B) information. The sync recognition mode employed is selected by the setting of the FRAME SYNC RECOG switch, the four functional positions of which are: mode 1, WIDE PULSE; mode 2, FREQ; mode 3, WIDE PULSE OR FREQ; and mode 4, WIDE PULSE AND FREQ. Mode 1 is normally selected when operating this system. The manner in which frame sync recognition is functionally accomplished for each mode is explained in the following paragraphs.

a. Mode 1 – The PFM telemetry signal burst-blank envelope is a symmetrical square wave, with the exception of channel zero, which has a blank period equal to 25 percent of the channel period and a burst period equal to 75 percent of the channel period. (All other channels are 50 percent blank and 50 percent burst.) This signal is extracted by the envelope detector portion, and used to control the integrator portion of a special circuit (paragraph 3.3.14.3) in such a manner that the wide burst of each channel zero transmission results in an output pulse which indicates to the system that frame sync recognition has been accomplished. The output pulse is produced when the charge on a capacitor has leaked off sufficiently to trip a threshold detector circuit. The time constant of the capacitor discharge circuit is regulated by the INTEGRATION SYNC. ADJ. control. When this control is properly set, the time constant of the capacitor discharge circuit prevents the threshold from tripping for a burst period of normal duration (50 percent of the burst-blank envelope period); however, the prolonged burst period of each channel zero transmission (75 percent of the envelope) is sufficient to cause a response from the threshold circuit. The threshold response signal is shaped and coupled through the wiper of the FRAME SYNC RECOG switch to the time coincidence logic circuits, and to the loss of frame sync recognition signal detector of the sync search and lock section.

CW Lockout Gate – Since the integrate-and-dump circuit capacitor is charged at the beginning of each cycle of the flywheel signal from the bit synchronizer, and is discharged in response to the output signal from the envelope detector portion of this circuit, output signal gating is necessary to inhibit false frame-sync recognition pulses which would otherwise be coupled to the recognition mode logic circuits when CW transmissions are received. The CW lockout gate used for this purpose consists of a NAND gate controlled by the set output signal from a flipflop. When the flipflop is set, the NAND gate couples the frame sync recognition pulse to the recognition mode logic circuits. The reset input to the flipflop is controlled by the flywheel signal, which causes it to be reset at the beginning of each cycle. The envelope detector output signal, which excites the bit-rate filter, is also used to set this flipflop in response to each data burst detected, and to control the discharge period of the integrate-and-dump circuit capacitor. The envelope detector response to a CW transmission is a steady output signal which results in continuous output pulses from the integrate-and-dump circuit, but which is capable of setting the flipflop only once. Since the flipflop is reset by the flywheel signal, it remains reset for the duration of the CW transmission period, Consequently, the NAND gate is inhibited, decoupling the integrate-and-dump output signal from the recognition mode logic circuits.

b. Mode 2 – When the sync oscillator frequency appears in alternate channel zero transmissions (odd numbered frames), the digital comb filter unit is programmed to detect its presence, and a sync oscillator recognition signal is consequently generated in a discrete output channel of the filter at appropriate times. This signal is then coupled to the sync search and lock section circuits by the FRAME SYNC RECOG switch.

c. Mode 3 – The threshold response signal from the wide burst detector circuit is NOR gated with the sync oscillator recognition signal from the digital comb filter unit, and the output of this gate is coupled to the sync search and lock section circuits by the FRAME SYNC RECOG switch.

d. Mode 4 – The threshold response signal and the sync oscillator recognition signal are NAND gated, and the output of that gate is coupled to the sync-search-and-lock section circuits by the FRAME SYNC RECOG switch.

e. Specific Adaptations – An example of the manner in which the sync recognition section may be easily adapted to special telemetry formats is the addition of special lockout circuits and a filter/detector/clamp circuit. These adaptations affect the output signal from the envelope-detector special circuit card in different ways to make the system compatible with a specific satellite telemetry format. The adaptations are constructed on printed circuit card modules which can be inserted or removed as desired without the need for making changes in the existing wiring. When the modules are removed, the equipment functions normally as a data-reduction system for the standard PFM telemetry format signal. (Special circuits for the IMP telemetry format are discussed in Appendix I of this volume.)

3.3.2.3 Sync Search and Lock

The sync-search-and-lock section, through programmable logic circuits, decides whether the system is or is not in synchronism, and as a result of this decision either enables or inhibits the digital information printout process, and indicates whether the lock or search mode of operation prevails. The channel sorter is reset through the sync-search-and-lock section when the frame sync recognition signal is lost for the duration of 32 or more successive frames, or by the first frame sync recognition pulse when the unit is in the search mode. The unit then evaluates the synchronism of the channel sorter with respect to the frame sync recognition burst over a programmed number of frames, and decides whether the system should go into lock or should remain in the search mode. If the system is not ready for lock, the channel sorter is again reset, as above, and another evaluation of synchronism is made. This process continues until the system is in synchronism, at which time the sync search and lock unit places the system in the lock mode and enables the digital information printer.

a. Time Coincidence Logic – The time coincidence of each frame sync recognition pulse and channel zero bracket pulse is compared logically to arrive at in-sync and out-of-sync decisions.

This is accomplished by a coincidence circuit consisting of two NAND gates, one of which generates an output signal when the sync pulse and bracket pulse occur simultaneously. The other NAND gates provide an output pulse if the sync pulse occurs at any time which does not coincide with the occurrence of the channel zero bracket pulse. Since the channel zero bracket pulse is derived in the channel sorter section from the bit synchronizer flywheel signal, coincidence of the bracket pulse and the sync pulse indicates that the decommutator is in sync with the telemetry signal, while a phase shift between these two signals indicates a synchronization error.

b. Programmable Counters – Two 4-stage binary counters are included in the sync-search-and-lock section to store the in-sync and out-of-sync decisions from the time coincidence logic circuits. Each of these counters is programmable by the manipulation of four IN PHASE COUNTER and four OUT OF PHASE COUNTER toggle switches, respectively. These switches, located behind the front panel on the lower part of the frame and channel control bucket, are used to select the set or reset output signals from the individual counter stages and couple them to the NAND gates controlling the sync-search- and lock-reset functions and the system operating mode. The counters can be programmed with these switches to select the desired ratio of in-sync to out-of-sync decisions which must continually recur for the lock mode of operation to prevail. Any desired ratio, the value of which is defined by integers between 1 and 16, may be selected by the switches. When the count accumulated in either counter reaches the value for which that counter has been programmed, the NAND gate associated with the counter generates an output signal to initiate appropriate reset functions and to control the search/lock indicator circuits accordingly.

c. Reset Functions – When the ratio of in-sync to out-of-sync decisions made by the time coincidence logic circuits is equal to or greater than the ratio selected by programming the in-phase and out-of-phase counters, the system is considered to be satisfactorily in synchronism and the lock mode of operation automatically prevails. Under these conditions, the in-phase counter is first to reach its programmed limit and the output pulse generated by the NAND gate to which it is coupled resets both counters and sets the search/lock control circuit flipflop. When the ratio of in-sync to out-of-sync decisions does not compare favorably to the programmed ratio, the out-of-phase counter is first to reach its programmed limit. The pulse generated by the NAND gate associated with the out-of-phase counter occurs at this time. This pulse resets both counters, in addition to resetting the flipflop in the search/lock control circuit and setting a flipflop which opens the channel sorter reset gate. The search mode is normally initiated in this manner if the incoming sync recognition pulse is not interrupted by a circuit malfunction. However, the time coincidence logic gates are inhibited when such a condition occurs and the counters become inactive. If this condition continues to exist long enough for 32 or more frames to be missed, the search mode is initiated by the delayed reset circuits.

d. Delayed Reset – A five-stage binary counter which controls a flipflop, NAND gate, and delay multivibrator capable of initiating the reset function which puts the system in the search mode, functions as a loss-of-frame-sync recognition signal detector and delayed reset circuit. This counter, which performs a divide-by-32 function, responds once per frame to a pulse originating

in the channel sorter each time channel 15 is expected. However, the counter is reset by each frame sync recognition pulse, and the count cannot accumulate as long as this pulse is present. When loss of this pulse does occur for 32 or more consecutive frames, the count accumulates and a delayed reset function occurs when it exceeds the capacity of the counter. The counter then sets a flipflop which enables a NAND gate coupled to the input of a 200-μsec delay multivibrator which generates the pulse necessary to initiate the search mode.

e. Search/Lock Control Circuits – Whenever the search mode is initiated, the search/lock control circuits generate a signal which: (1) interrupts the processing of digital data, (2) resets the divide-by-64 counter in the bit synchronizer, and (3) opens the special lockout circuit gate which couples the output signal from the envelope detector to the input of the bit-rate filter. This signal originates at the reset output of the search/lock control flipflop which stores commands from both the in-phase counter and the delayed reset circuits previously described. The search/lock control also provides visual indication of the system's operating mode by energizing the appropriate LOCK or SEARCH indicator light coupled to the set or reset output, respectively, of the search/lock control flipflop. The flipflop is set by a gated signal from the programmed output of the in-phase counter, and is reset by a similar signal from the out-of-phase counter or from the delayed reset circuits. Consequently, once the search mode is initiated, the system remains in search until the ratio of in-sync to out-of-sync decisions made through the time coincidence logic circuits equals, or exceeds, the acceptable ratio programmed by means of the IN PHASE COUNTER and the OUT OF PHASE COUNTER toggle switches discussed in paragraph 3.3.2.3.b.

f. Channel Sorter Reset Gate – Synchronization of the decommutator is accomplished by resetting the channel sorter coincident with the occurrence of a frame sync recognition pulse, and updating the frame sorter with the frame corrector in response to signals from the digital comb filter. The channel sorter reset gate is implemented by a delay multivibrator which generates a reset pulse for the channel sorter in response to the first recognition pulse occurring after the search mode is initiated. The gating of the recognition pulse to trigger the multivibrator is controlled by a flipflop which stores commands from the out-of-phase counter, the delayed reset circuits, and a feedback signal. Consequently, the channel sorter reset gate is opened when the search mode is initiated and is closed by the pulse generated to reset the channel sorter. This pulse also resets the in-phase and out-of-phase counters.

g. Manual Reset – The search mode may also be initiated manually with the push-button RESET switch located adjacent to the SEARCH and LOCK indicator lights on a subpanel at the top of the frame and channel control bucket.

3.3.2.4 Channel Sorter

One count is accumulated in the four-stage programmable binary counter of the channel sorter at the end of each cycle of the burst negative flywheel signal from the bit synchronizer. The binary output of the channel sorter counter is coupled to the frame and channel matrix by a matrix of NAND

gates. An output signal for each count is also taken directly from the NAND matrix outputs to the printer code converter, and to the OSCILLOGRAPH INPUT SELECTION CHANNEL switch. The signals may also be paralleled from these points to other parts of the system, as required. For a standard PFM telemetry format of 16 channels per frame, the four-stage binary counter resets itself when it reaches its capacity at the end of each frame. The positive-going pulse which occurs at the set output of its final stage is coupled at this time to the input of the frame sorter where it is counted by a second four-stage counter. The counter output also controls a reset function which has been made programmable by the addition of four-CHANNEL PROGRAMMING toggle switches. These switches are located behind the front panel at the bottom of the frame and channel control bucket; they are used to select the set or reset outputs of each counter stage and to couple them, through a delay multivibrator which serves as a pulse generator, to a reset input common to all four counter stages. Consequently, the channel sorter may be programmed to reset itself when any desired count corresponding to the number of channels per frame of the incoming telemetry signal has been reached. The counter should not be programmed for a count of less than eight, since to do so prevents the set output of the final stage from changing state. The counter is also reset when the search mode has been initiated by a signal from the channel sorter reset gate of the sync search and lock section (paragraph 3.3.2.3.f.) which serves to resynchronize the decommutator. A positive-going pulse for the duration of one channel time is available at the SCOPE SYNC output connector each time a count of 15 is reached. A similar signal is available for any channel count from zero through 15 at the OUT connector. The count selected depends on the setting of the CHANNEL SELECTOR switch. A negative-going pulse for the duration of the channel count each time channels 1, 3, 5, 7, 9, 11, and 13 are counted appears at the output of an NOR gate which is coupled to the printer code converter. This signal is used by the printer code converter when a high-speed printer is used, and is discussed at greater length in paragraph 3.3.8.

3.3.2.5 Frame Sorter

One count is accumulated in the four-stage binary counter of the frame sorter each time the channel sorter is reset. Like the binary counter of the channel sorter, the counter of the frame sorter resets itself on the count of 16 to conform to the standard PFM telemetry format, or it may be programmed to reset after any desired count has been reached by manipulating the four FRAME PROGRAMMING toggle switches located behind the front panel at the bottom of the frame and channel control bucket. Functionally, the frame sorter performs in a manner identical to that of the channel sorter, except that it counts frames instead of channels and is capable of being updated by signals from the frame corrector matrix when alternate frames of the incoming telemetry signal are received. The frame sorter provides a marker pulse for each frame counted to: the frame and channel matrix, the printer code converter unit, and the OSCILLOGRAPH INPUT SELECTION FRAME switch. From these points the signals may also be paralleled to other points of the system, as required. The frame sorter is coupled to the frame corrector by eight lines which convey the necessary information to keep it in sync with the telemetry signal being received.

3.3.2.6 Frame Corrector

The diode gating matrix of the frame corrector is enabled by the channel zero bracket pulse from the channel sorter whenever the SYSTEM INPUT SELECTOR switch on control panel No. 2 is placed in the TAPE or REC. position. The matrix is then used to couple frame-identification signals from the digital comb filter unit to selected set and reset inputs of the frame sorter counter stages. Consequently, the frame sorter counter is updated, if necessary, in response to the octally coded frame identification frequency during the burst period of channel zero of even numbered frames. When, for example, the digital comb filter detects a digital 3 in the channel zero burst frequency (the code which identifies channel 8), a signal occurs on one of the eight input lines to the frame corrector and is coupled by the matrix to the dc reset inputs of the 2^0, 2^1, 2^2 stages, and the dc set of the 2^3 stage of the frame sorter counter. Consequently, the counter is forced to a count of 8 if it is not already in step with the incoming signal. When a digital 7 (the code which identified channel zero) is detected, the frame corrector couples this signal through a gate controlled by the channel zero bracket pulse directly to the common reset input of all four stages of the frame sorter counter. The frame sorter then is reset to coincide with the beginning of frame zero of each sequence of the incoming telemetry signal. When the SYSTEM INPUT SELECTOR is in the SIMULATE position, the frame corrector matrix is inhibited, except for the common reset line to the frame sorter.

3.3.2.7 Frame and Channel Matrix

The frame and channel matrix consists of 256 NAND gates, each of which generates a positive-going output signal pulse once every 16 frames. Two hundred fifty-six discrete marker pulses are generated sequentially by the individual gates during each 16-frame period as a result of the coincidence of signals from the frame counter and channel counter at their input terminals. The marker pulses are employed for data control throughout the system.

3.3.3 DIGITAL COMB FILTER UNIT

To make it universally adaptable to the format of any PFM telemeter, the digital comb filter unit has been made programmable. The unit's response to incoming telemetry signals can be changed readily by the insertion of pins in its front panel patchboards, as explained in paragraphs 2.3.1 through 2.3.1.3. It is used to quantize the subcarrier oscillator frequencies of selected channel bursts. For this purpose, digital circuits are used to detect and indicate the presence of discrete input frequencies, a function previously performed by tuned circuit filters. The digital circuits are programmed to determine the average period in microseconds of each channel burst analyzed, and to generate an appropriate octal recognition signal in one of eight output channels, or a sync recognition signal in a ninth output channel. A functional block diagram of the digital comb filter unit appears in figure 3-4, and the logic diagram of its digital circuitry is contained in sheets 1 through 8 of figure 6-4, Volume II.

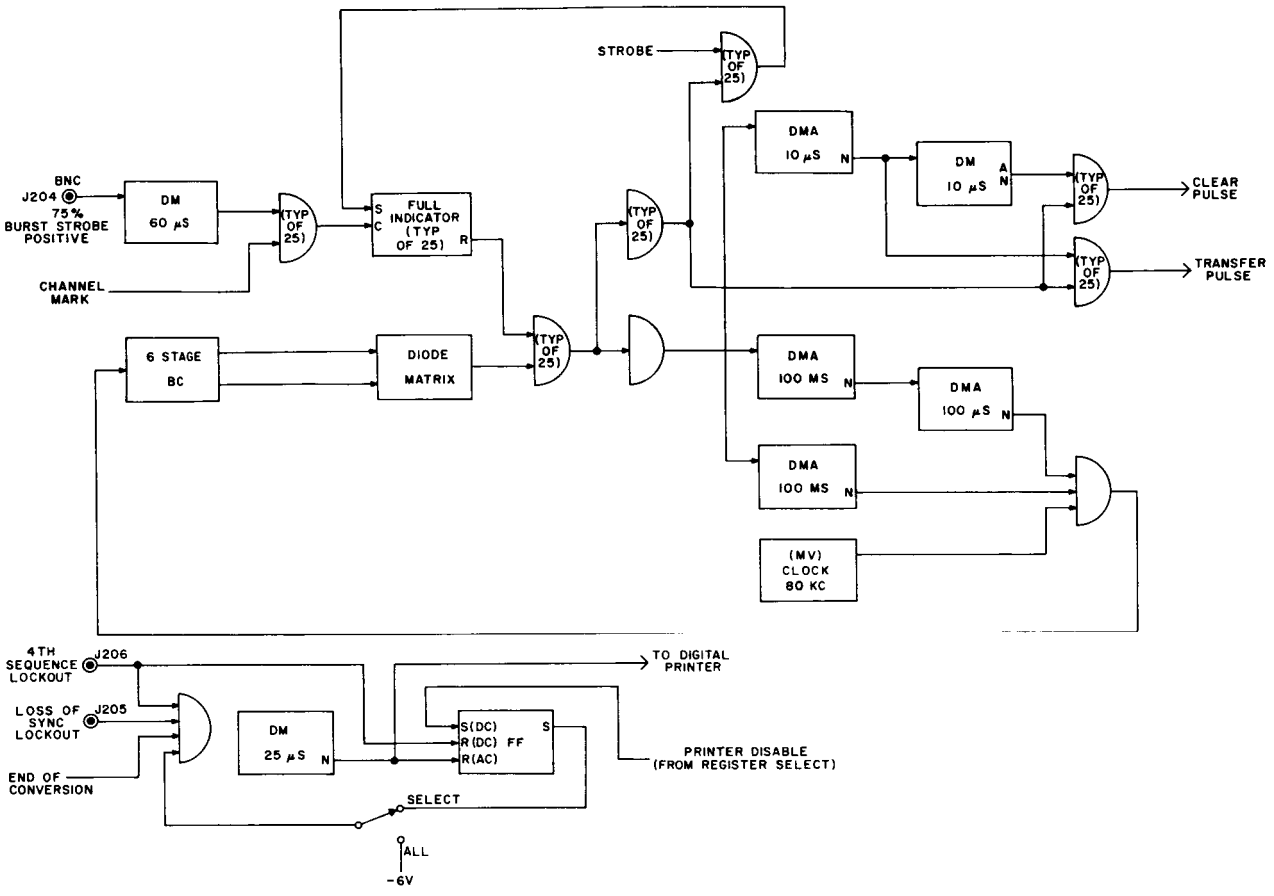


Figure 3-4—Digital Comb Filter, Functional Block Diagram

3.3.3.1 Since eight discrete subcarrier oscillator (sco) frequencies are assigned for the transmission of digital information in a PFM format, and a ninth frequency is reserved for frame synchronization, a corresponding number of output channels has been incorporated in the design of the digital comb filter unit. Output channels zero through seven are supplemented with indicator lights which are energized individually by the presence of recognition signals in the respective channels. In line with the octal number recognition lights is an ERROR indicator light which is energized whenever the sco frequency of the channel burst signal is not within the range of frequencies for which the unit is programmed.

3.3.3.2 Each output channel recognition signal represents an octal number and, as such, is coupled permanently to the appropriate inputs of the frame and channel control unit's frame-corrector circuits. It is also converted to a three-bit binary number, the bits of which are coupled to program board No. 1, and in parallel to other points in the system, as needed. The binary bits are then

patched at program board No. 1 as information bits to the cells of the memory unit. This process is described in paragraphs 2.3.2.2 and 2.3.2.3.

3.3.3.3 A gated oscillator and a time delay circuit for generating a test signal and reset strobe pulse are included in the digital comb filter unit as a convenient tool for bench testing. To use this feature, the TEST/OPERATE switch is placed in the TEST position. However, it is customary to test the digital comb filter as part of the complete data reduction system. This is accomplished with the SYSTEM INPUT SELECTOR switch (control panel No. 2) in the SIMULATE position, while the digital comb filter unit TEST/OPERATE switch remains in the OPERATE position.

3.3.3.4 Included in the signal-conditioning circuits of the comb filter are several NAND gates, a Schmitt trigger, a delay multivibrator, and a two-stage binary counter. Signals containing the frequencies to be quantized by the filter are coupled to the input of the Schmitt trigger circuit. Each positive-going transition from the output of the Schmitt trigger excites the delay multivibrator which generates a 0.6 μsec pulse for each cycle of the comb-filter input signal. The elapsed time between these pulses consequently corresponds to the period of the input signal. This period is measured by counting the cycles (which occur between pulses) of the output signal from a one-megacycle clock. The NAND gates of the signal-conditioning circuits are used by the two-stage binary counter to discard the first two pulses generated by the delay multivibrator for each input signal to be analyzed, since they may not exactly correspond to the period of the signal. A selected number of subsequent pulses is then coupled to the input of the cycle counter, which controls the one-megacycle clock on-off time via a programmable binary count selector at its output. The number of output pulses generated by the clock during a predetermined number of cycles of the input signal, divided by the selected output of the cycle counter, is the true period of the input signal in microseconds.

3.3.3.5 The output signal from the one-megacycle clock is digitally resolved by a 13-stage binary counter, the output of which is controlled by a second programmable binary count selector to represent the period of a single cycle of the comb-filter input signal. Eighteen NAND gates, each of which is coupled to programmed outputs of this binary count selector, form a matrix which controls 18 individual flipflops. Each of the flipflops functions to define the upper or lower period limit of one of the nine comb-filter output channels, and each of these channels represents a discrete band of frequencies, the center frequency of which corresponds either to the sync recognition frequency, or to one of the eight subcarrier oscillator frequencies used to transmit digital information from the satellite. As the count progresses in the 13-stage binary counter, one after the other of these flipflops is set by the gating action of the matrix as a lower or upper limit of the count defining each filter output channel is exceeded. When the counting stops, the upper- and lower-limit flipflops are sampled. If both upper and lower limits of a channel have been exceeded, or if neither has been exceeded, no action is taken. If, however, the lower limit of a channel has been exceeded and the upper limit has not, then the input signal must fall within this band of frequencies, and the sample pulse causes an output flipflop to take the set state. An output flipflop is the source of each output channel recognition signal.

3.3.3.6 A programmable clock divider coupled to the output of the one-megacycle clock may be used for coupling the clock signal to the 13-stage binary counter to avoid exceeding the limits of the counter when low-frequency signals are being processed. The clock divider is a four-stage binary counter with a programmable count selector at its output, by means of which the operator may select the set output of any one of its stages to obtain a divide by 2, 4, 8, or 16 function. The choice of coupling the one-megacycle clock output to the 13-stage binary counter either directly or through the clock divider, the programming of the binary pins representing upper and lower limits, and the selection of the number of cycles over which a count is made, is accomplished at the program board located on the front panel of the digital comb filter unit. Instructions for programming it are contained in paragraphs 2.3.1 through 2.3.1.4.

3.3.4 DIGITAL MEMORY UNIT

3.3.4.1 The memory unit contains 200 discrete memory cells. Each cell consists of a flipflop with individual 2-input NAND gates connected in the set input and set output lines. In operation, the memory unit accepts, stores, and transfers into a hold register on command, the binary bits of octal numbers.

3.3.4.2 A typical memory cell is shown in figure 3-5. Logic diagrams of the memory unit are found in Volume II, figure 6-4, sheets 1 through 4. The input circuit (a 2-input NAND gate) functions at coincidence of a negative information bit and an inverted (negative) channel mark. The information bit can be any one of the three significant bits of an octal number furnished by the comb filter. The inverted channel mark is a timing pulse which occurs only once for a selected channel every 256 channels. At coincidence, therefore, the output of the NAND gate becomes and remains positive for the duration of the information bit, provided the information bit is not a zero. This positive pulse is connected to the set input of the flipflop. The resultant change of state sets the flipflop at a negative-output level which remains after the inputs are removed. In this manner, information is stored in the memory.

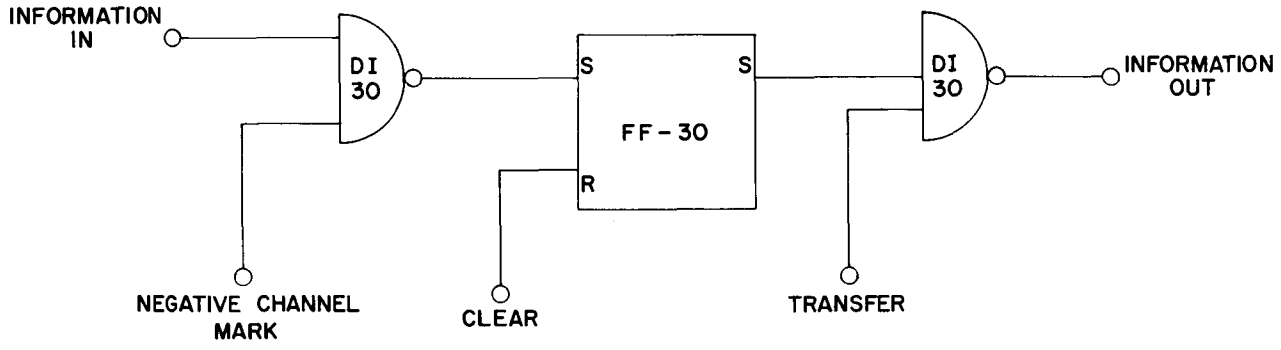


Figure 3-5—Typical Memory Cell

3.3.4.3 The output circuit of the memory cell is also a 2-input NAND gate. One input is the FF-30 negative set-output level, and the other is a negative transfer pulse. The transfer pulse appears whenever information is to be read out of the memory. At coincidence of these two signals, the output of the NAND gate becomes positive. This positive pulse is then directed to the hold register. It must be noted that information is stored in the memory unit in the form of words. A word contains at least one and not more than 21 bits of information. Since one memory cell is required for each bit contained in a word, there are as many memory cells per word as there are bits for that word. At readout, each of the memory cells associated with a particular word receives a transfer pulse.

3.3.4.4 The clear pulse, which occurs after the transfer pulse, conditions the memory cell for accepting a new information bit. This positive pulse is inserted at the dc reset input of the flip-flop. Each cell receiving a transfer pulse also receives a clear pulse. Since there are 25 transfer and clear pulses in this system, 25 words may be stored in the memory unit. Both the transfer and the clear pulses are programmable so that a particular cell can be part of a given word at one time, and part of a different word at another time. The information input and output circuits are also programmable. A programmable information input gives each memory cell the capability of accepting different bits from different channels. Similarly, a programmable information output permits placing the stored bit, at different times, in different stages of the hold register. A discussion of programming is presented in paragraph 2.3.2.2.

3.3.5 DIGITAL READOUT CONTROL UNIT

The digital readout control unit contains the circuits necessary for controlling word transfer from memory to the hold register, for clearing the memory, for initiating bcd conversion and for generating a print command pulse for the digital printer. Figure 3-6 shows a functional block diagram of the digital readout control unit. The logic diagram appears in Volume II, figure 6-6, sheets 1 through 4.

3.3.5.1 The digital readout process begins whenever a word in the memory is completed. At this time, the channel mark representing the channel which contains the last information bits of a given word is gated to the complement input of a full indicator. A full indicator is one of the flipflop stages of a BC-30 module. There are 25 such full indicators, one for each word which may be stored in memory. Complementing resets the full indicator, and the resultant reset output becomes one input to a 2-input NAND gate.

3.3.5.2 There are also 25 of these 2-input NAND gates, one gate being associated with each full indicator. The other NAND gate input is the output from a group of diode clusters which receives inputs from a six-stage binary coded decimal (bcd) counter. The diode cluster forms a matrix for decoding the six-bit bcd number and coupling it to one line of a 25-line output. Each output

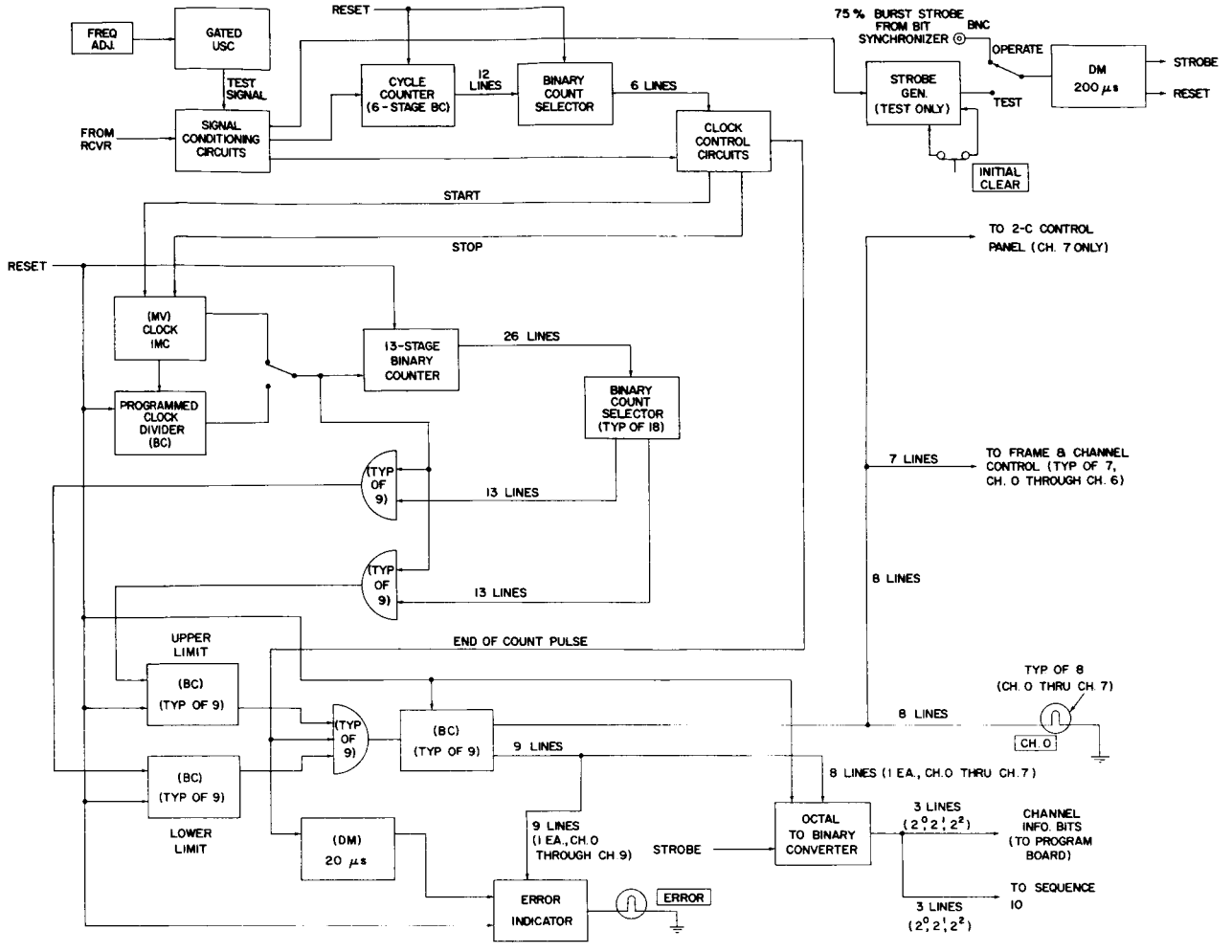


Figure 3-6—Digital Readout Control, Functional Block Diagram

line from the matrix is associated with the output signal from one of the 25 full indicators. The bcd counter, which is driven by a free-running multivibrator (MV) at an 80-kc rate, continuously and sequentially samples each full indicator at the 2-input NAND gate.

3.3.5.3 When coincidence of a signal from the matrix and from the full indicator occurs at its input, a NAND gate output becomes positive and this change of signal level is coupled through a 25-input OR gate to initiate a series of pulses. The first in this series is referred to as the transfer pulse and is generated on the leading edge of each positive-going NAND gate output signal by a 10-μsec delay multivibrator. The resultant 10-μsec transfer pulse is then connected to the proper pins (rows 11 through 15; columns J through C) of program board No. 1. The second pulse is the clear pulse and is generated on the trailing edge of the transfer pulse by another 10-μsec delay multivibrator. The clear pulse is also routed to the proper pins (rows 11 through 15; columns R through K) of program board No. 1. Also generated is a third pulse referred to as the inhibit pulse, the leading edge of which is coincident with the leading edge of the transfer pulse. This pulse interrupts the signals from the 80-kc MV to the input of the bcd counter for the time required to print out a word. When the signal to the counter is inhibited by this pulse, sampling of the full

indicators is interrupted and the next sequence cannot be initiated until the current one has been completed. The inhibit pulse, which is approximately 200 milliseconds long, is generated by three 100-millisecond delay multivibrators.

3.3.5.4 The print pulse is generated by a 25-μsec delay multivibrator (DM). At the conclusion of the binary-to-bcd conversion, an end of conversion trigger is routed from the bcd converter to an input of the NAND gate which excites the DM. If all the other NAND gate inputs are correct, a print command pulse is generated by the DM and sent to both the digital printer and the ac reset of a control flipflop. When the PRINT ALL/PRINT SELECTED switch on control panel No. 1 is the PRINT SELECTED position, this flipflop (UF) inhibits the NAND gate to the DM after each print command pulse has been generated. The UF must then be set by an enable pulse from the register select circuits before the DM can again be triggered by the end-of-conversion signal. The UF has no effect on the NAND gate to the DM when the PRINT ALL/PRINT SELECTED switch is in the PRINT ALL position. However, this gate is always inhibited by the presence of a fourth sequence lockout or loss-of-sync lockout signal.

3.3.5.5 The bcd counter (paragraph 3.3.5.2) is also the source of signals which convey word identification information to control panel No. 1. Here this information is converted to a decimal value by nixie circuits, and displayed as the DIGITAL REGISTER NUMBER by nixie readout tubes.

3.3.6 HOLD REGISTER UNIT

The hold register unit basically consists of a 21-stage shift register with appropriate parallel input circuits. In operation, the hold register receives data in parallel from the memory unit and serially shifts this data to the bcd converter. The hold register unit also contains 96 inverter circuits which provide negative channel marks for the memory unit.

3.3.6.1 A functional block diagram of the hold register unit is shown in figure 3-7. The logic diagram is shown in Volume II, figure 6-7. Each register stage is formed from one of the flipflops located on the 3C S-PAC SR-30 modules. Parallel transfer of data from the memory to the register set input terminals is via a multi-input OR gate. The reason for the large number of OR gate inputs is that each word formed in the memory must transfer its bits into the corresponding bit stage of the register. Thus, the least significant bit (2^0) of all words in memory must transfer into the least significant bit stage (2^0) of the hold register, and so on.

3.3.6.2 Those bits in memory which are to be transferred to the hold register are selected at program board No. 1. When a memory cell is strobed by a transfer pulse, the resultant zero-volt output sets the hold register stage to which it is connected. At shift-pulse time, all bits are moved from the stage in which they are stored into the next more significant bit stage of the register (the most significant bit stage (2^{20}) shifts into the bcd converter). After 21 shift pulses,

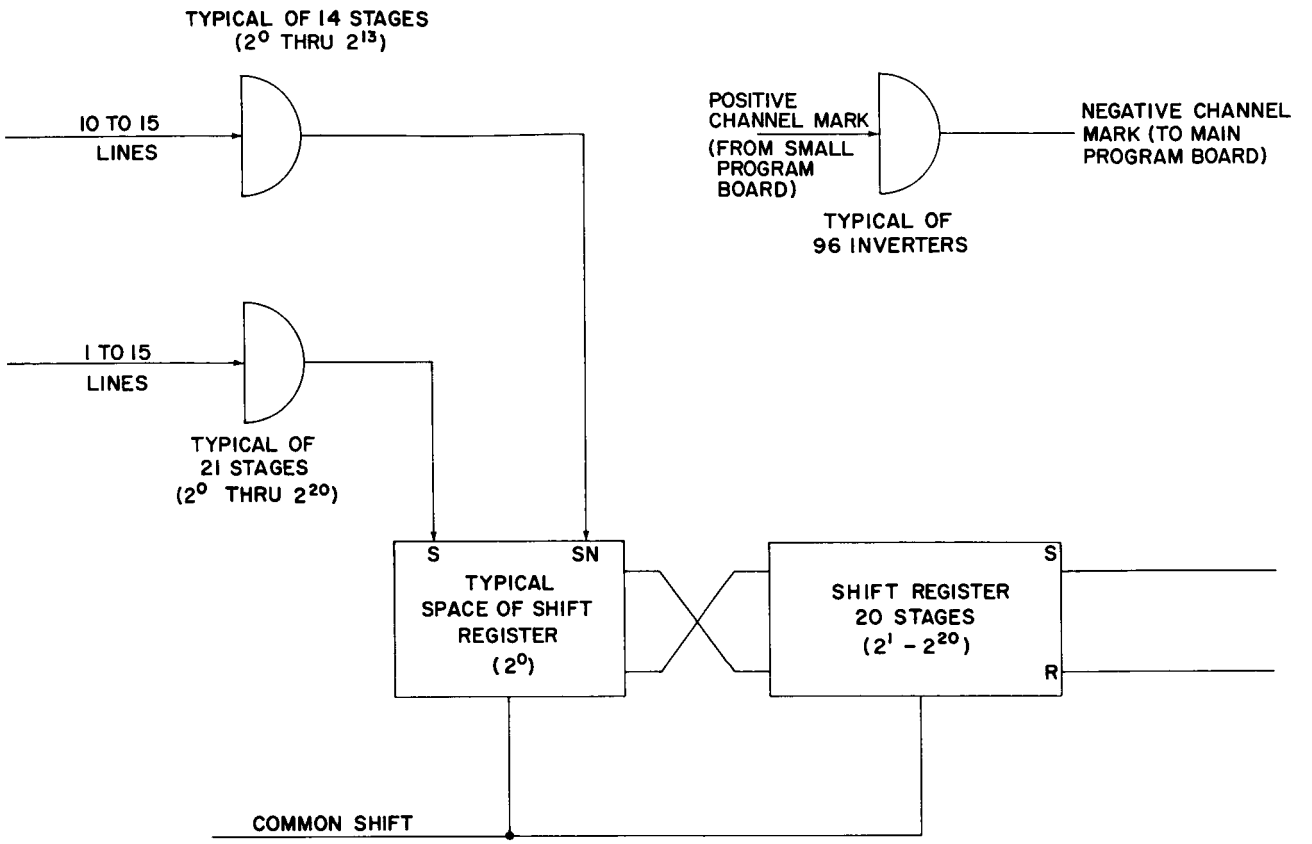


Figure 3-7–Hold Register, Functional Block Diagram

the bit initially found in the least significant register stage (2^0) will have shifted through all 21 stages into the bcd converter. The hold register will then be clear of all information.

3.3.6.3 Inputs to the 96 inverter circuits located in the hold register unit are connected to program board No. 2. The 256 positive channel marks are also connected to this program board. For use in the memory unit, 96 of these positive channel marks are selected on program board No. 2, inverted by the 96 inverters in the hold register unit, and then connected to program board No. 1.

3.3.7 BCD CONVERTER UNIT

The binary coded decimal (bcd) converter unit contains the circuits necessary for converting a binary number to a binary coded decimal number. This unit accepts binary numbers serially from the hold register, transforms these numbers to binary coded decimal representations, routes the encoded numbers to a digital printer for decimal printout, and stores the value for nixie display.

3.3.7.1 Certain mathematical principles underlie the bcd conversion process. A discussion of these principles is essential to an understanding of the bcd converter circuits. In general, a true binary number of any length can be expressed as:

(1) $N = A_n \cdot 2^n + A_{n-1} \cdot 2^{n-1} + A_{n-2} \cdot 2^{n-2} + A_{n-3} \cdot 2^{n-3} + \ldots + A_{n-n} \cdot 2^{n-n}$

where A is either 0 or 1, and n is the binary power 0, 1, 2, 3, etc. A numerical example of this expression will appear less formidable. Consider the binary number 1101 (decimal 13):

(2) $N = 1_3 \cdot 2^3 + 1_{3-1} \cdot 2^{3-1} + 0_{3-2} \cdot 2^{3-2} + 1_{3-3} \cdot 2^{3-3}$

or:

(3) $N = 1_3 \cdot 2^3 + 1_2 \cdot 2^2 + 0_1 \cdot 2^1 + 1_0 \cdot 2^0$

A continued reduction of this expression will produce:

(4) $N = 8 + 4 + 0 + 1$

The result is a decimal 13. The given value, therefore, has been converted from a binary number to a decimal number.

Now by rewriting (3):

(5) $N = \left[(1_3 \cdot 2 + 1_2)\, 2 + 0_1\right]\, 2 + 1_0$

a pattern of multiplication by 2 (doubling) and adding appears. By working out several examples it is proved that this pattern can be stated as a general rule for converting from binary to decimal numbers. The rule, which is called the Double-Dabble Method of conversion, says that given a true binary number of any length, the equivalent decimal number can be found by:

(a) Doubling the most significant bit.

(b) Adding the next most significant bit (either 0 or 1).

(c) Doubling the accumulated sum.

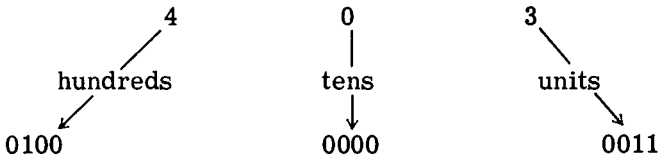
(d) Repeating from (b) until the least significant bit has been added.

Here is the Double-Dabble Method of conversion for the binary number 1101.

Most Significant Bit			Least Significant Bit
1	1	0	1
1	3	6	13

3.3.7.2 The Double-Dabble Method is basically the conversion method used in the bcd converter unit. This conversion process is easily implemented in the binary number system because the doubling operation is merely the shift of all digits one position towards the most significant bit. Since, however, the actual conversion process begins with a binary number and ends with a binary coded decimal number, the binary coded decimal number must now be considered.

3.3.7.3 A binary coded decimal number is one in which a group of four binary bits is associated with each of the several positions of a decimal number. As an example, the decimal number 403 is represented in this manner:



Similarly, the decimal number 10 is represented in bcd as 0001 0000. It is obvious that a bcd number less than 10 cannot be distinguished from a true binary number. This fact presents no problem when doubling or shifting as long as the result is also less than 10. In advancing, however, from 9 to 10, the bcd number is distinguished from the true binary number by a carry function into the next higher decimal position. Consider the true binary number 9 (1001). If a binary 1 (0001) is added, the result is a binary 10 (1010). Suppose that the binary 9 was actually a bcd 9. The addition of 1 still results in 1010. This latter number should now be a bcd 10, but it attempts to represent the sum of 10 in one decimal digit without providing a carry. In other words, the bcd number is confined to the units groups, thereby representing nothing.

3.3.7.4 To make this bcd number a true representation of the number 10, an additional 6 counts must be added to the binary 10 (1010). The desired result is 0001 0000. Here are the changes from 9 to 10 in the decimal, binary, and bcd systems:

Decimal		Binary		BCD
9	=	1001	=	1001
+1	=	0001	=	0001
				0110 Add 6
10		1010		10000
carry				carry

From this it follows that a count of 6 is always added to a bcd number when an operation is performed on the number, the result of which has a decimal value of 10 or greater. Since shifting effectively doubles a number, it also follows that bcd numbers less than 10 and greater than or equal to 5 which are shifted require an additional 6 counts. The 6 counts may be realized by

adding 3 counts prior to shifting because, by shifting, the 3 counts are effectively doubled and become the required 6 counts. It should be noted that a count of 6 is employed whenever the bcd number shifts into the next decimal position, i.e., from units to tens, tens to hundreds, etc.

3.3.7.5 A functional block diagram of the bcd converter is shown in figure 3-8. The logic diagram is found in Volume II, figure 6-8. The converter essentially consists of a 28-bit serial register which accumulates bcd numbers, and the control circuits for operating the register. The basic elements of the serial register are the circuits contained on the 3C S-PAC UF-30 module. These circuits are arranged in groups of four, with each group representing one of the several positions of a decimal number. The serial shift is accomplished both within each group and between succeeding groups. Associated with each group of four UF-30 circuits are gating circuits which perform the add 3 operation. Separate bcd storage flipflops, one for each register stage, store the output bcd digits for both the digital printer and the nixie display units.

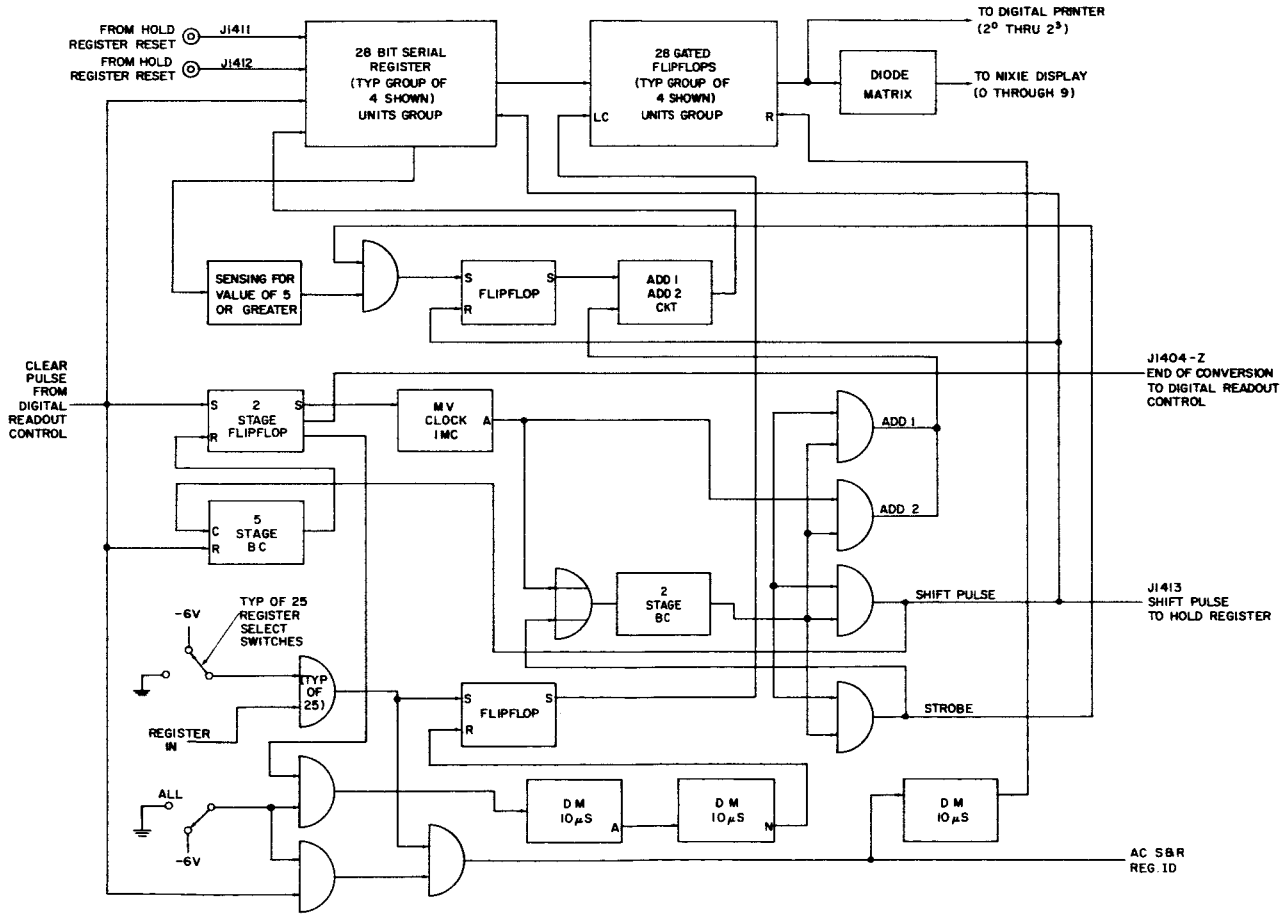


Figure 3-8—BCD Converter, Functional Block Diagram

3.3.7.6 The control circuits provide conditioning pulses for the print operation, and four special pulses in a recurring sequence for the actual bcd conversion process. The circuits also permit selection of any or all words in the register for printout. The sequence of four special pulses begins following the appearance of a clear pulse. This clear pulse, which occurs after a word has been transferred from the memory to the hold register, turns on a 1-megacycle clock (MV-30). The output clock pulses are connected to one input of four 2-input NAND gates, and to one input of a NOR gate. The other input to each NAND gate is supplied by a 2-stage counter which causes a sequencing of the four different conversion pulses. Consider an initial condition of 00 in the counter. At the first clock pulse, a strobe pulse is generated. One function of this strobe pulse is to step the counter to the 01 state. The other function of the strobe pulse is to sample the contents of each register stage, and, when the proper condition exists, to trigger a flipflop in the adder circuits. The proper condition is the presence of a number which is 5 or greater in any group of four register stages. This value of 5 or greater can exist as follows: (a) fourth register stage (2^3) contains a 1; (b) third stage (2^2) and second stage (2^1) contain a 1; (c) third stage (2^2) and first stage (2^0) contain a 1. If none of these possibilities are present, the strobe pulse does not trigger the adder flipflop.

3.3.7.7 At the second clock pulse an add 1 pulse is generated. Simultaneously, the counter is stepped to the 10 state. The add 1 pulse is routed to the adder circuits. At the third clock pulse an add 2 pulse is generated and the counter moves to the 11 state. The add 2 pulse is also routed to the adder circuits. The last clock pulse generates a shift pulse and the counter returns to the initial 00 state.

3.3.7.8 Table 3-1 shows the contents of each bcd register stage in the units and tens group for selected steps in the conversion of a binary 10 to a bcd 10. Assume that a binary 10 is stored in the hold register as follows:

2^{20} through 2^4	2^3	2^2	2^1	2^0
0	1	0	1	0

The initial conditions of the bcd converter at this time are 0's in the units and tens group. As each shift pulse occurs, the bits in the hold register advance serially towards the most significant stage. Between shift pulses the contents of each bcd converter group are sampled simultaneously for a value of 5 or greater. When the 18th shift pulse occurs, the first information bit from the hold register enters the 2^0 stage of the bcd converter units group. The contents of this group consequently have a value of one when the next sampling pulse occurs. The 19th shift pulse moves the binary one into the 2^1 stage of the units group, the contents of which now have a value of 2 (still less than 5) when sampled. The 20th shift pulse causes binary 1's to appear in the 2^0 and 2^2 stages, resulting in a sample with a value of 5, and the adder circuit flipflop is triggered when sampling occurs. Consequently three counts are added, increasing the value of the contents of the

units group to 8. Therefore there is a binary 1 present in the 2^3 stage of this group, which is shifted into the 2^0 stage of the tens group when the final (21st) shift pulse occurs. During this process the binary 5 was increased to 8 and then doubled to become a binary 16 in the first five stages of the bcd converter register. When the register stages are considered sequentially, in groups of four, this number is a bcd 10.

Table 3-1. Contents of BCD Register Stages During Binary-to-BCD Conversion Process

BCD CONVERTER								
CONDITIONS	TENS GROUP				UNITS GROUP			
	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
Initial	0	0	0	0	0	0	0	0
After 18th shift pulse: sample < 5 No add	0	0	0	0	0	0	0	1
After 19th shift pulse: sample < 5 No add	0	0	0	0	0	0	1	0
After 20th shift pulse: sample = 5 Add 1 Add 2	0 0 0	0 0 0	0 0 0	0 0 0	0 0 1	1 1 0	0 1 0	1 0 0
After 21st shift pulse: carry of 1 into TENS GROUP	0	0	0	1	0	0	0	0

3.3.7.9 The 21st shift pulse terminates the conversion process and initiates the print command pulse. A five-stage binary counter records the shift pulses and, after 21 counts, turns off the 1-megacycle clock. If, prior to the arrival of the 21st shift pulse, the DIGITAL DISPLAY SELECTION toggle switch labeled ALL ON/OFF (control panel No. 1) is in the OFF position, an enabling signal may be present at one input of a 2-input NAND gate. The 21st-shift pulse, connected to the other input of this NAND gate, thus resets the flipflop which controls the storage flipflop. This operation results in printout and readout of the most recent data to be accumulated in the bcd converter stages.

3.3.7.10 Initially, all those words to be printed out are selected by means of the 25 DIGITAL DISPLAY SELECTION switches on control panel No. 1. (Figure 3-6 shows one switch as typical of all 25.) The output from each switch is connected to one of 25 NAND gates when the switch is

placed in the ON position. The other NAND gate inputs are controlled by pulses from the proper full indicator in the hold register. The resultant output is a pulse which performs the following functions: (1) enables the print pulse circuits; (2) triggers a flipflop which enables transfer of bcd information from the bcd register stages (UF's) to the storage flipflops (FA's) during the conversion process; and (3) provides a common reset for the bcd storage flipflops.

3.3.8 PRINTER CODE CONVERTER

The printer code converter extracts information from each channel and sends it in bcd form to a digital printer and the nixie display on control panel No. 2. This information is the average period computed from ten successive cycles of each data burst, which is printed out and displayed as its decimal equivalent. Thus, the decimal numbers are the ten-period average values, in microseconds, of the individual channel subcarrier modulation frequencies. The printer code converter determines this value with a resolution of $\pm 1\ \mu$sec. Figure 3-9 is a functional block diagram of the unit; the logic diagrams are figure 6-9, sheets 1 through 5, of Volume II.

3.3.8.1 Period Measurement

3.3.8.1.1 Action is initiated with the arrival of a flywheel burst positive signal at the input control DM (see sheet 1 of figure 6-9, Volume II) from the bit synchronizer unit. This results in the clearing of the eight decades of the clock counter and the enabling of the input gate so that the input signal can enter the period measurement circuits. Either the period of the burst or the blank portion of a channel may be measured depending on the position of the BURST/BLANK toggle switch. With the switch in the BURST position, the input control DM triggers on the leading edge of the flywheel burst positive signal and enables the input gate so the burst portion of the channel is gated in for measurement. Placing the switch in the BLANK position triggers the DM on the trailing edge of the flywheel signal so that the blank portion of the channel is gated into the period measurement circuits.

3.3.8.1.2 The input signal is taken from the bit synchronizer unit after passing through a limiter and AGC circuit. It then is fed to a Schmitt trigger at the input of the printer code converter where the burst (or blank) portion of each channel is converted to a square-wave train. When the input gate is enabled, the wave train then enters the five-stage variable input trigger delete counter. The purpose of this counter is to eliminate a selected number of the initial pulses of each burst to eliminate the effects of a phasing error between the flywheel and burst pulses, and thus reduce the possibility of an erroneous count in the period counter. The first one to 31 pulses of each burst may be eliminated by setting the five PERIOD MEASUREMENT PULSE DELETE toggle switches. When the selected number of pulses have been counted the decoder gate at the output of the counter is enabled. The positive output pulse from the gate triggers a sliver eliminator circuit which, in turn, sets a UF. With the UF in the set condition, the period counter input gate is enabled so that burst pulses can now enter the period counter. The sliver eliminator circuit

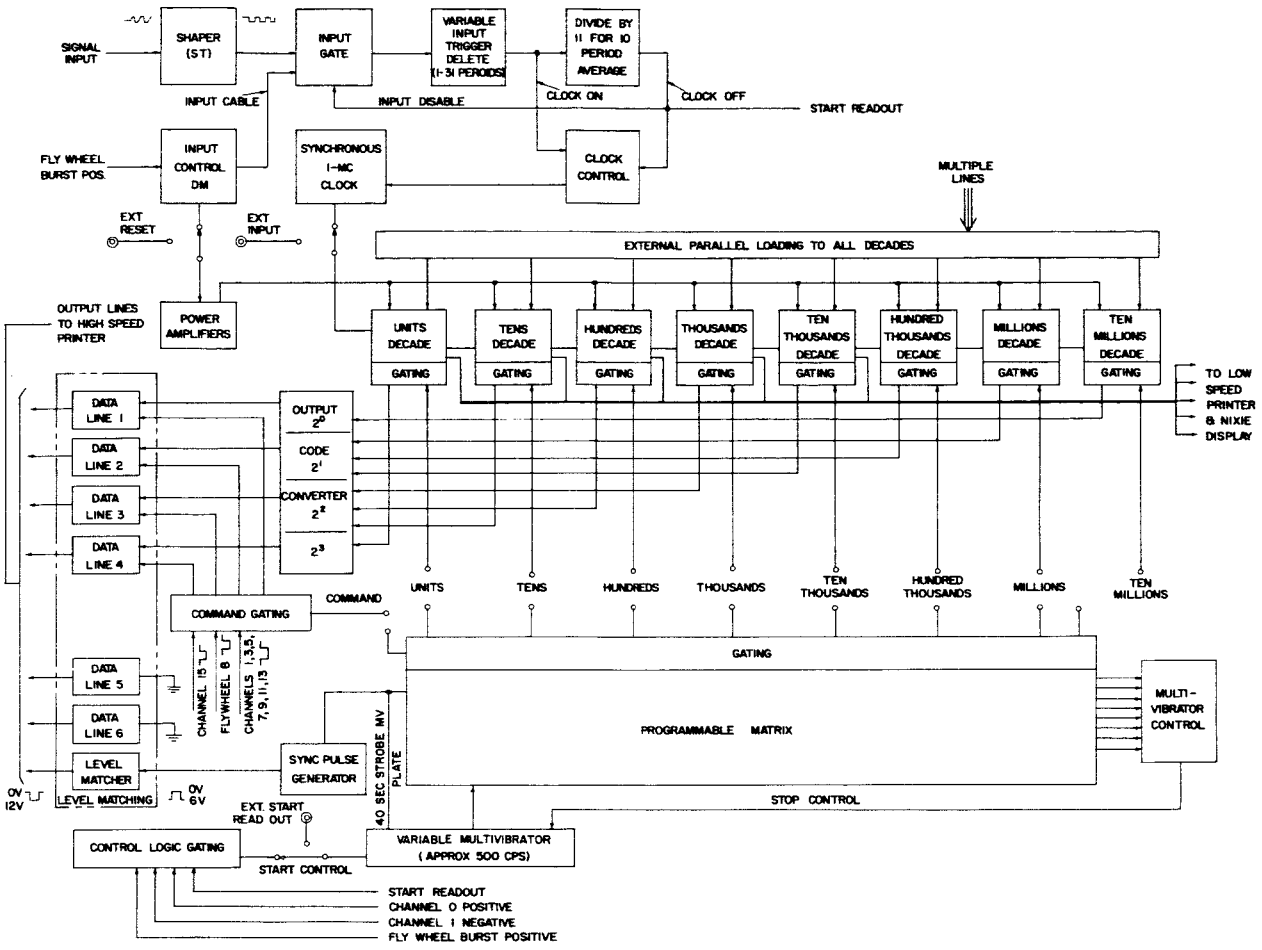


Figure 3-9—Printer Code Converter, Functional Block Diagram

ensures that the period counter input gate is not erroneously opened and the period counter started before the proper number of burst pulses have been eliminated. Once the period counter input gate is enabled, the next burst pulse enters the period counter, and, simultaneously, the 1-Mc clock is started.

3.3.8.1.3 The period counter is a four-stage counter connected in the bcd configuration. In order to count ten complete periods of the burst frequency, it is necessary to gate eleven burst pulses into the period counter before inhibiting the counter input gate and cutting off the 1-Mc clock. To perform the divide-by-eleven function, the set output of the last stage of the counter is connected to the ac set input of a UF, and the reset output of the first stage of the counter is connected to the ac reset input of the UF. On the tenth count, the positive transition at the set input of the UF puts it in the set condition.

All four stages of the counter are now set at "zero." The positive-going edge of the eleventh pulse entering the counter causes a positive transition at the reset output of the first counter

stage. This results in the UF going to the reset condition with a positive transition at the set output. The set output of the UF is connected to a DM. When the positive transition occurs, the DM is triggered. The output pulse from the DM has five functions:

1. To stop the 1-Mc clock
2. To inhibit the input to the period and trigger delete counters
3. To serve as the "start readout" command for the printer
4. To reset the period and trigger delete counters
5. It is connected to the dc reset input of the UF to ensure that the UF is in the reset condition when the next burst (or blank) arrives.

At this time the count from the clock is read out from the eight decade counters. The cycle described above is repeated for the next burst (or blank) with the arrival of the positive flywheel burst pulse.

3.3.8.1.4 The MC-30 1-Mc clock has a continuous output from its sync output pin. This is necessary to control the UF which cuts the clock's negation output on and off. The negation output is fed serially into the eight decade counters when the period counter starts operation, and is cut off when 11 pulses of the burst (or blank) frequency have been counted. The count in the decade counters at this time is the 10-period average of the burst frequency in microseconds. Sheet 2 of figure 6-9, Volume II, shows the counter decades (units to ten millions) in detail. In addition to loading by the self-contained clock, the decade counters may also be loaded serially or in parallel from an external source by placing the INPUT switch in the proper position. The gating for parallel drop-in is shown on sheet 5 of figure 6-9, Volume II. These gates are inhibited when the INPUT switch is in the INT. or EXT. SERIAL positions. When the printer code converter is used with the Hewlett-Packard Model 562A low-speed printer, the output from the decade counters is taken from the reset outputs of the units through the ten-thousands decades, passed through inverters, and sent to the printer in bcd form. The same output is also sent to the period readout and display logic unit to drive the nixie display on control panel No. 2. The hundred thousands and higher decades of the decade counter are not used with the low-speed printer or nixie display. All decades, and the gating at the output of the decades, are required only when the unit is used to drive a high-speed printer.

3.3.8.2 Control Logic

This section of the printer code converter is required only when the unit is used with the Burroughs high-speed printer. It controls the readout of the count in the eight decade counters, so that each decade is read out in proper sequence. The section consists of a multivibrator, multivibrator control, control logic gating, a sync pulse generator, and a programmable matrix which controls the sequence of readout of the decade counters. Sheet 3 of figure 6-9, Volume II, is the logic diagram for the section.

3.3.8.2.1 The multivibrator (MV) provides pulses which strobe the output gates of the eight decade counters in sequence from the most significant decade to the least significant decade. It also provides a command pulse which follows the least significant digit readout. The command pulse is required by the high-speed printer for such operations as line feed and carriage return, and must always follow the least significant digit readout pulse. Patch points are provided on the printer programming panel to determine the sequence of reading out the count in the decade counters. Four WORD LENGTH toggle switches are set to cut off the MV after the required number of readout pulses and the command pulse have been generated. If, for example, a four-digit character is to be strobed from the decade counters, the WORD LENGTH switches must be set for a binary five. This allows the strobing of four decades and a command pulse before the MV is cut off. The printer programming panel is patched as follows: 10^3 decade to sequence point No. 1, 10^2 decade to sequence point No. 2, 10's decade to sequence point No. 3, units decade (1) to sequence point No. 4, and COMMAND to sequence point No. 5. When the "start readout" pulse is received, the count in the 10^3 decade will be strobed out first, the units decade next to last, and finally the command pulse.

3.3.8.2.2 The "start readout" pulse is fed to the control logic gating circuit. This circuit gates "start readout" with channel 0 positive, channel 1 negative, and flywheel burst positive so that the readout of the channel 0 count is inhibited until channel 1 blank time. This is done to allow ample time for the printer to perform the carriage return and line feed function. The output pulse from the control logic gating starts the MV and strobing of the decade counter gates begins.

3.3.8.2.3 The multivibrator is adjusted to put out a 40-μsec pulse at a rate of approximately 500 cps. Its output is fed into a four-stage binary counter, to the sync pulse generator, and used to strobe the gates at the output of the binary counter. The output from the binary counter gates provides the strobe pulses to readout the content of the eight decade counters. Also connected to the output of the binary counter are the four WORD LENGTH toggle switches. The SEQUENCE patch points receive negative strobe pulses in ascending order beginning with point No. 1 when the MV is started. After the number of MV pulses equivalent to the setting of the WORD LENGTH switches have been counted, the NAND gate at the input to the multivibrator control is enabled. As a result, the MV is cut off before another pulse can be generated, and the four binary counter stages are reset. This cycle is repeated for each telemetry burst (or blank).

3.3.8.2.4 The sync pulse generator provides a 20-μsec negative pulse which serves as a print command for the high-speed printer. It must be in coincidence with each strobe pulse generated by the MV. This is done by triggering the sync pulse generator by each output pulse from the MV. Thus, when the MV is cut off, the sync pulse generator is also inoperative. The sync pulse is connected to the OPERATE/IDLE toggle switch so that the pulse is shorted to ground when the switch is in the IDLE position. This prevents a printout until the switch is returned to the OPERATE position.

3.3.8.3 Code Converter

The code converter receives the content of the eight decade counters and passes it to the high-speed printer over four data lines. It also receives the pulses for the printer to perform idle, space, carriage-return, and line-feed operations. The logic diagram for the code converter is sheet 4 of figure 6-9, Volume II.

3.3.8.3.1 Inputs to the code converter are four 8-input NOR gates. Each gate drives a data line. In addition, there are two data lines (lines No. 5 and No. 6) which are always at the mark level (-12v). Each of the eight inputs to each NOR gate is connected to the 2^0, 2^1, 2^2, or 2^3 position of each decade of the eight decade counters. As each decade is strobed, its count is passed through the NOR gates and on to the data lines. The printer command gates are wired so that there is a carriage return and line feed following channel 15, a space between all odd channels except 15 and 1 (carriage return and line feed occurs during this time), and so that the printer idles between all even channels. Note that the command pulse is required for all these printer operations.

3.3.8.3.2 The logic levels for the high-speed printer are 0v for a space and -12v for a mark. This level also applies to the printer sync pulses. All data line outputs and the sync pulse output are on the same DI board, II-22. To match the printer logic levels, the -6v clamp voltage at pin 3 of the board is removed and the pin is connected to a -12v source.

3.3.9 PERIOD READOUT AND DISPLAY

The period readout and display encompasses the following functional sections:

a. Period Readout Control Switching – This section consists of a bank of 289 toggle switches. The switches function, along with control logic, to include or exclude any sequence, frame, or channel of information in the data readout.

b. Period Readout and Display Logic – This section consists of the following circuits:

   (1) Two 5-stage bcd counters and a diode matrix to identify the frame and channel being processed during printout – Output information from each counter is presented as a bcd number (0 through 15) to the period printer (Hewlett Packard Digital Recorder, Model H24-562A).

   (2) Gating circuits to control the print command pulse – These circuits are fed by the bank of 289 switches.

   (3) Period display control circuits – These are five groups of identical logic, each containing four flipflop with separate input and output NAND circuits feeding a bcd-to-decimal decoder.

The circuits first convert a 10-period average count from a bcd number to a decimal number, and then control the readout of this number through five nixie display units. Five nixie tubes display the period readout (channel burst) in microseconds to the nearest tenth.

3.3.9.1 Figure 3-10 shows a functional block diagram of the period readout and display logic unit. The logic diagram is found in Volume II, figure 6-10. Circuit description begins with the period readout control switching. This bank of 289 toggle switches is divided into 256 channel switches, 16 frame switches, 16 sequence switches, and one master sequence switch. The channel switches are in groups of 16, each group representing one frame of a 16-frame sequence. Input signals to the channel switches are channel marker pulses from the frame and channel matrix. Since each channel switch feeds a NOR gate, there are also 16 groups of NOR gates. The output of a NOR gate group is one input to one of 16 two-input NAND gates. The other input of each NAND gate is fed a selected frame bracket pulse, via a control switch, from the frame sorter. At signal coincidence, a NAND gate supplies an output pulse representing each selected channel during any selected frame. The 16 NAND gate outputs are OR gated and become one input to a 3-input NAND gate. The other inputs to this gate are a sequence bracket pulse from the sequence identification logic circuits, and a print command pulse from the printer code converter unit. The resultant output is a command pulse to the printer occurring only during the selected sequence, frame, and channel period. This pulse also triggers a 50-μsec delay multivibrator which, in conjunction with two 10-μsec delay multivibrators, generates an assertion and a negation pulse spaced 50 microseconds apart. The two pulses are then applied to the period display control circuits.

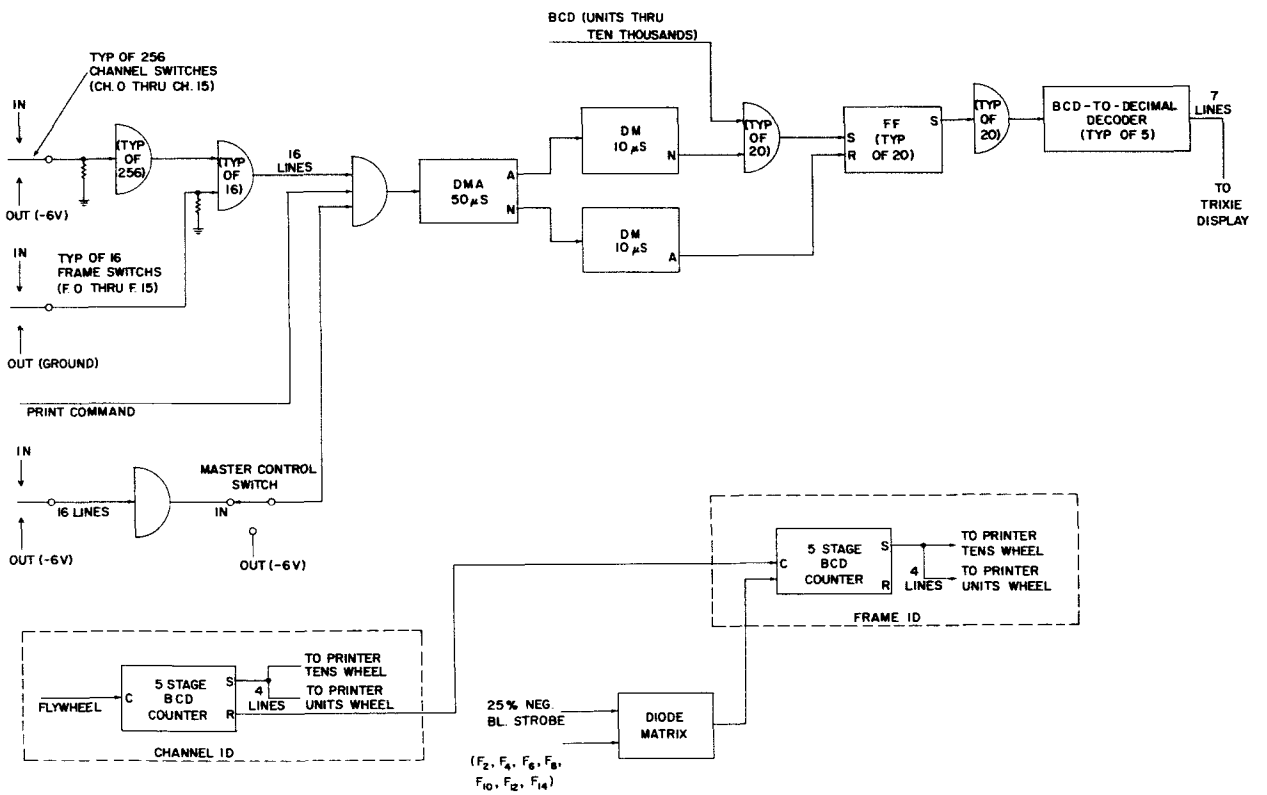


Figure 3-10—Period Readout and Display Logic, Functional Block Diagram

3.3.9.2 The function of the assertion pulse (which occurs first) is to reset all flipflops in the period display control. This operation insures that the bcd-to-decimal decoder has reached its final state before the arrival of new data from the printer code converter. The negation pulse (which lags the assertion pulse by 50-μsec) is connected to one terminal of each input NAND gate. Its function is to gate in bcd numbers (at the other NAND gate terminals) representing the 10-period average count. A logic 1 at both inputs of any NAND gate sets the associated flipflop, thereby supplying a bcd digit directly to the proper bcd-to-decimal decoder. Since both the bcd digit and its negation are required to drive the decimal decoder, each flipflop output is also inverted by a single input NAND circuit. The bcd-to-decimal decoders are 3C OD-30 S-PAC modules. Decoded output signals from each OD-30 are routed to their respective nixie units.

3.3.9.3 Frame and channel identification are effected by two five-stage counters operated in tandem. Each of these counters (consisting of four BC stages and one UF stage) is wired for the 8421 bcd mode of operation. Four stages of each counter control a wheel of the period printer, one counter being used to control the units wheel (column 7 of the printer record) for channel identification, and the other counter being used to control the units wheel (column 9 of the printer record) for frame identification. In like manner, the fifth stage of each counter controls a printer wheel (columns 8 and 10 of the printer record) which prints out the tens digit for channel and frame identification, respectively. The channel counter is stepped by the flywheel signal from the frame and channel control unit. After nine counts, a positive-going pulse is shifted into the fifth stage (UF) of the channel counter. This operation sets the UF stage and thus produces a negative level (logic 1) at its set output to activate the tens wheel of the printer. The negative level remains at the set output until the end of 16 counts, at which time all five stages of the counter are reset by a zero-state input from the frame and channel control unit. The zero-state reset coincides with the start of channel 0 for all frames, thereby insuring synchronization between period read-out and frame- and channel-control counters.

3.3.9.4 Resetting the channel-identification counter after 16 counts forces the reset output of the UF stage of that counter to the negative state. The reset output is then inverted and applied to the input stage of the frame-identification counter. The frame-identification counter, which steps in a manner similar to the channel-identification counter, produces data to control the frame-identification wheels of the period printer. Frame correction during even-numbered frames is supplied by a matrix feeding the reset inputs and/or set node inputs of the frame-identification counter. The frame-identification inputs to the matrix force the frame counter to be in step with the main frame sorter. The same channel-0 reset from the frame sorter is also used to reset the frame-identification counter.

3.3.10 SPECIAL BOX

The circuits contained in the special box adapt the broadly programmable, universal features of this data-reduction system to the unique characteristics of a specific PFM telemeter. Since the

format of each satellite telemetry signal to be processed is tailored to meet the requirements of the experiments it serves, no two formats are entirely alike, and a special box is needed for each satellite. The circuits of each special box are therefore designed for use with a particular satellite, after the distinguishing characteristics of its telemetry signal have been thoroughly evaluated. Each special box consists of three S-Blocks to accommodate the necessary circuits, which will always include a satellite signal simulator. The signal simulator is designed to generate a test signal comparable to the signal expected from the satellite with which it will be used. The simulator makes it possible for the operator to test the accuracy and dependability of the data-reduction system prior to a mission, when the programming for that particular mission has been accomplished. In addition to the signal simulator (which must be designed and built separately for each special box), it may be necessary to include other circuits in the special box to perform such special functions as sequence identification or modification of the digital output signals for certain experiments. A functional description of the first special box designed for use with this system appears in Appendix I. As the system is adapted to the formats of additional telemeters, additional special boxes and circuits will have to be designed, and patching instructions for additional program boards will be needed. Collectively, the special boxes contribute to the versatility of the universal data-reduction system. Individually, each box is the key element in making the system completely compatible with a specific telemeter.

3.3.11 CONTROL PANEL NO. 1

The schematic diagram for control panel No. 1 is figure 6-11 of Volume II, sheets 1, 2, and 3. When the three primary power cables in the rear of the test stand are connected to the power source, the appropriate indicators on control panel No. 1 (LINE 1, LINE 2, LINE 3) light. When the POWER toggle switch is in the ON position, relay K1 energizes. In so doing, primary power is applied directly to the coil of relay K2, also lighting the POWER ON indicator. The normal condition for energizing relay K2 is that switch S4 is normally open and indicator DS2 has a very high impedance. Connected to the same point are several series interlocks (not shown on schematic), which are normally closed, providing a direct path to ground. When any of these series interlocks open, indicator DS2 lights; the operator then closes switch S4, bypassing the interlocks and extinguishing indicator DS2.

3.3.11.1 When -18 vdc is available to control panel No. 1, the VCO LOW/HIGH indicator automatically lights. When pushbutton switches S5 through S10 and S31 are depressed, the appropriate indicator lights. Switches S5, S6, and S7 remotely control the application of primary power to the digital and period printers as well as to the oscillograph.

3.3.11.2 A sealed power-supply unit within control panel No. 1 receives 115 vac and steps it up to 170 vdc. This dc voltage is used as the anode voltage for the DECIMAL VALUE and DIGITAL REGISTER NUMBER nixies.

3.3.12 CONTROL PANEL NO. 2

Figure 6-12 of Volume II is the schematic diagram for control panel No. 2. This panel contains four rotary switches, five CHANNEL BURST PERIOD nixies, five RACK TEMPERATURE indicators, LOCK and SEARCH indicator lights, a FRAME SYNC. SEARCH LOCK RESET pushbutton switch, a H. S. PRINTER POWER ON/OFF switch, a TEST/OPERATE toggle switch, and discriminator controls.

3.3.12.1 The SYSTEM INPUT SELECTOR rotary switch has input positions available for an analog tape recorder, a telemetry receiver, and the simulator. Signals received from the selected instrument are sent to the rejection filter.

3.3.12.2 The CHANNEL BURST PERIOD nixies receive inputs from the period readout control logic. These nixies display the 10-period average in μ secs of the frequency within the burst being processed.

3.3.12.3 The discriminator selection switches, FRAME and CHANNEL, select the frame and channel number of data to be processed by the discriminator for display on the oscillograph.

3.3.12.4 The discriminator controls consist of a rotary switch and a potentiometer. The rotary switch (DISCRIMINATOR ADJUSTMENT CAPACITANCE) selects the appropriate range for the bit rate used in the discriminator. The potentiometer (DISCRIMINATOR ADJUSTMENT RESISTANCE) controls the amplitude of the discriminator output.

3.3.12.5 In the TEST position, the DISCRIMINATOR ADJUSTMENTS OPERATE/TEST toggle switch provides a means of calibrating the discriminator with an external oscillator connected to the bnc connector.

3.3.12.6 The H. S. PRINTER POWER ON/OFF toggle switch and indicator are connected in the ac line to the high-speed printer. When the toggle switch is positioned ON, the indicator lights.

3.3.12.7 SEARCH and LOCK indicators, in addition to the FRAME SYNC. SEARCH LOCK RESET pushbutton, are all connected between the power supply and the frame and channel control unit. The pushbutton is depressed to initiate the search mode. The indicators light to indicate the respective mode.

3.3.13 CONTROL PANEL NO.3

Control panel No. 3 contains six circuit breakers, three each for power supplies 1 and 2; two AC and DC FAIL indicators, one pair for each power supply; two POWER ON/OFF toggle switches; and an elapsed time meter. Its schematic diagram is figure 6-13 of Volume II.

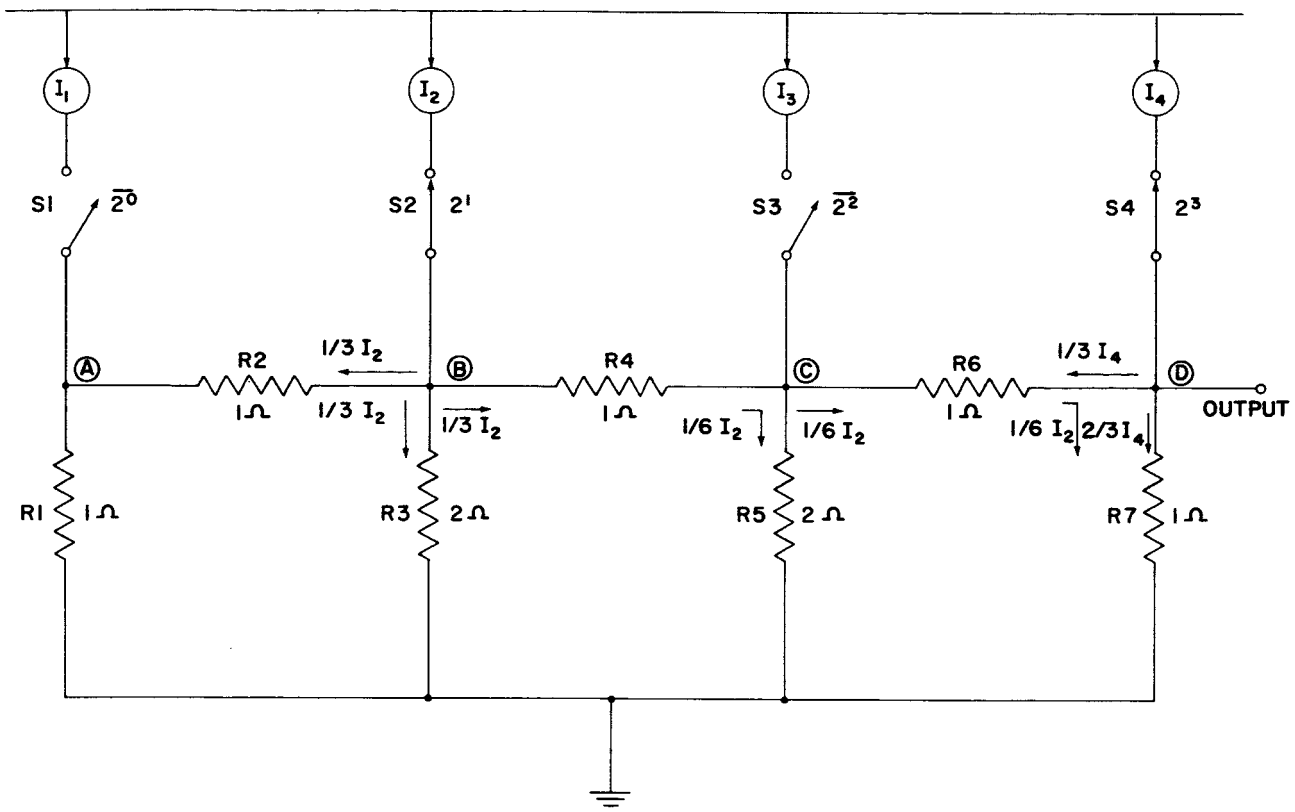


Figure 3-11—Simple Ladder Network

3.3.13.1 The power-supply circuit breakers protect the power-supply output voltage from overloading.

3.3.13.2 The DC FAIL indicators light when dc power fails.

3.3.13.3 The ELAPSED TIME INDICATOR meter measures the equipment running time.

3.3.13.4 The POWER ON/OFF toggle switches control the application of primary power to each power supply. When the toggle switch(es) are ON, the applicable AC indicator(s) light. Two INPUT 7-AMP fuses, one for each power supply, are used in series with the primary power windings; two SPARE fuse holders are provided adjacent to the INPUT 7-AMP fuse holders.

3.3.14 SPECIAL CIRCUITS

3.3.14.1 Digital-To-Analog Converter

The digital-to-analog converter circuit board is designed for use with an eight-stage binary register or counter. The output from the converter is a voltage level representative of the digital number connected to the inputs. Since there are 256 possible combinations of the eight digital inputs, the

converter circuit can provide 256 discrete voltage levels between ground and -4 volts. A schematic diagram of the digital-to-anglog converter circuit is found in Volume II, figure 6-17, sheet 3 of 3. The conversion process employed in the digital-to-analog converter circuit is that of summing currents in a balanced ladder network. For the purpose of explanation, a simple ladder network is shown in figure 3-11. In this network, four switches (S1 through S4) individually select the output from one of four constant-current generators (I1 through I4). Each switch has an open and a closed position corresponding to the true and false inputs, respectively, of binary digits 2^0 through 2^3. Only the closed (or true) position supplies current to the network. Therefore, since switches S2 and S4 are shown as closed, binary digits 2^1 and 2^3 are true, and generators I2 and I4 supply current. This current is added algebraically at the right-hand rung of the ladder in proportion to the binary weight assigned to the inputs.

Consider the junction of resistors R2, R3, and R4 at node B of the simple ladder network. By the use of superposition it is verified that I2 sees two ohms in each direction from node B. I2 thus contributes 1/3 I2 to node C. At node C, the 1/3 I2 sees two ohms in the direction of R5, and two ohms in the direction of R6. The 1/3 I2 thus contributes (1/2) (1/3 I2) through R6 and R7 to ground. At node D, I4 sees two ohms in the direction of R6, and one ohm in the direction of R7. I4 therefore contributes 2/3 I4 through R7 to ground. The voltage across R7 with the I2 and I4 currents is: $[(1/2)\ (1/3\ I2) + (2/3\ I4)]\ R7 = (1/6 + 2/3)\ 1 = 5/6$ volt. In general, the output voltage for this simple ladder network can be expressed as: $[(1/3)\ (1/2)\ (1/2)\ I1 + (1/3)\ (1/2)\ I2 + (1/3)\ I3 + (2/3)\ I4]\ R7$. From this expression it is seen that R7 receives the following currents: 1/12 amp from I1, 1/6 amp from I2, 1/3 amp from I3, and 2/3 amp from I4. The resultant current is a binary-weighted current proportional to the binary weighting at the digital inputs.

The digital-to-analog converter circuit (Volume II, figure 6-17, sheet 3) is basically similar in operation to the simple ladder network. Each constant-current generator consists of a common-base transistor circuit in which the base is supplied by a fixed voltage source regulated by a zener diode. The constant current is generated by returning the emitter of each transistor, via a resistor, to the cathode side of the zener diode. The combination of a single zener-diode voltage regulator and equal-value emitter resistors ensures that all current sources are equal. A 1-kilohm potentiometer permits adjusting the zener voltage by a few hundredths of a volt.

Transistors Q1 through Q8 are used to open and close the current sources (transistors Q9 through Q16) to the ladder network. For example, a logic zero (false input) connected to the emitter of Q1 forward biases Q1. The resultant positive-going collector voltage of Q1 turns off constant-current generator Q9. Similarly, a logic one (true input) turns off Q1, thereby permitting Q9 to supply current to the network.

The output of the ladder network (collector of Q16) is buffered by emitter followers Q17 and Q18. Voltage drops between the base-to-emitter junctions of these emitter followers are nullified by using one PNP and one NPN transistor. A 0-volt adjust potentiometer permits compensating for any small difference between the absolute value of these voltage drops.

3.3.14.2 Voltage-Controlled Oscillator

The voltage-controlled oscillator (VCO) circuit board uses a unijunction transistor as a threshold and discharge device to produce a positive-going 10-microsecond output pulse. Any center frequency between 50 cps and 28 kc can be selected by external resistance and capacitance adjustments. With a center frequency thus selected, the excursion will be ±2 percent for a minimum-to-maximum input voltage change. Selection of a second input terminal extends the variation to ±4 percent. A schematic diagram of the VCO is found in Volume II, figure 6-17, sheet 3.

The VCO circuit produces a ramp voltage by continually integrating a dc voltage (0 to -4 volts) applied at the base input terminals of constant-current generator Q20. Capacitors C2 and C3 in the collector circuit of Q20 are the integrating capacitors. These capacitors are discharged through unijunction transistor Q21 when the threshold level is reached. A resultant 3-volt negative spike thus appears at B2 of Q21. This spike triggers Q22, thereby producing the 10-microsecond output pulse. The transition time for the output pulse from -6 volts to ground is completed in less than 0.2 microsecond.

The VCO can be held off by applying a negative reset voltage at the base input terminal of Q24. This operation permits starting the VCO at the beginning of a period.

The center frequency can be controlled by applying a -2 volt input and adjusting the control potentiometers R49 and R50. Frequency stability is ensured by a sensistor (R47) for temperature compensation, and by a zener diode (CR4) for voltage regulation. A high or low frequency range can be selected by changing the integrating capacitors.

3.3.14.3 Detector, Integration, and Sync Recognition

The detector, integration, and sync recognition circuit board contains the following circuits: (a) an integrate-and-dump circuit consisting of an R-C integrator and a unijunction transistor; (b) a full-wave rectifier, filter, and saturating amplifier. A schematic diagram of the detector, integration, and sync recognition board is found in Volume II, figure 6-17, sheet 1.

The integrator portion of the integrate-and-dump circuit consists of resistor R1 and switch-selectable capacitors C1 through C4. The time constant of this charging network is changed for various repetition rates by selecting these different capacitors. Fine adjustment is made by potentiometer R1 connected as a rheostat. A ground-level signal at the input to the integrator causes the capacitor to charge. If the input level is of sufficient duration, the voltage across the capacitor (which is also impressed across the emitter and base 2 of unijunction transistor Q2) reaches the threshold level of Q2. At this time, Q2 becomes forward-biased and the base 1 resistance drops from 5 kilohms to approximately 20 ohms. A negative output pulse is then developed at base 2 of Q2 by a current surge through R18. This negative pulse drives tunnel diode CR1 to its high-voltage region, thereby providing a fast turn-on of inverter stage Q3. The resultant sync output pulse appears at the collector of Q3.

The emitter of unijunction transistor Q2 is clamped to -6 volts at the end of each channel time. This operation is effected by a 1.5-millisecond pulse which turns on Q1 and thus drops its emitter (common to emitter of Q2) to -6 volts. Any charge present on the integrating capacitor is thereby dumped so that, with each new channel, the capacitor will be fully discharged.

The detector portion of the detector, integration, and sync recognition board is driven by an emitter-follower stage Q4. Clipper-diode network CR5-CR6 provides peak-amplitude clipping for input signals of 18 volts or greater, peak-to-peak. Transformer-coupling is used in the emitter circuit of Q4. Signals appearing at the secondary of T1 are rectified by full-wave rectifier CR5 and CR6. Filtering in the emitter circuit of Q5 produces the desired signal envelope. This signal envelope is amplified by Q6 and appears in the collector citcuit.

Envelope detection of a signal which is a burst followed by a blank is effected by the detector. However, if the signal is a burst followed by a fill-in frequency during the blank time, additional inputs are required by the detector. In this case, the fill-in frequency must be filtered out and detected externally. The resultant signal is then used to clamp the base of Q5 to ground during the time of the fill-in frequency.

3.3.14.4 Schmitt Trigger

The Schmitt trigger circuit board contains two Schmitt circuits and two negative-logic saturating amplifier stages. A schematic diagram of the Schmitt trigger is found in Volume II, figure 6-17, sheet 3 of 3. The Schmitt circuit has two PNP and two NPN transistors in a push-pull arrangement, all with a common emitter resistor. A potentiometer is provided for threshold adjustment. Both positive and negative voltage levels are available at the outputs. Test points are also provided at the input and output of each Schmitt circuit.

The negative-logic saturating amplifier stages each contains a single PNP-transistor amplifier circuit. These circuits are used to improve the rise and fall time of the negative level output of the Schmitt trigger, and to restore the dc level. The resultant saturated output complements the input level.

3.3.14.5 Signal Conditioner Board No. 1

The signal conditioner board No. 1 contains the following circuits: (a) two cascaded emitter followers; (b) a single emitter-follower stage; and (c) a peak amplitude clipper-diode network. A schematic diagram of the signal conditioner board No. 1 is found in Volume II, figure 6-17, sheet 2 of 3.

Two basic Darlington circuits comprise the cascaded emitter-follower stages. A single input terminal (pin M) is common to both circuits. The Q2 output circuit contains diode clippers which provide a clipped output for signals of 0.6 volt peak-to-peak or greater. The Q4 output circuit does not provide any clipping action.

The single emitter-follower stage Q5 is a standard circuit which can be used for isolation.

The peak amplitude clipper-diode network provides a clipped output for signals of 17-volts peak-to-peak.

3.3.14.6 Filter and 2X Amplifier

The filter circuit is basically an adjustable bandwidth twin-tee network. This circuit is designed to pass a very narrow band of frequencies, the center of the band being determined by circuit parameters. A separate class-A amplifier is also included on the filter board for use with weak input signals.

3.3.14.6.1 A schematic diagram of the filter circuit is shown on sheet 2 of figure 6-17, Volume II. Input signals of 0.5 volt or less are coupled through capacitor C3 to the base of Q1. The signals are amplified by class-A amplifiers Q1 and Q4, and then applied to the filter network proper. Since the network is an RC notch filter, presenting a high impedance at only the center frequency, the side frequencies easily pass through the filter to the base of Q3. Notice that Q3 is in parallel with the collector load R12 of Q1. The increased conduction of Q3, therefore, effectively short circuits the side frequency signals at the collector of Q3 (degenerative feedback), and results in no output from the filter circuit at this time.

3.3.14.6.2 During the time when the center frequency is being received, the filter network proper offers maximum signal rejection. Since Q3 receives no input signal at this time, there is no short circuit at the collector of Q1, and normal signal amplification occurs. The center frequency, now amplified approximately 10 times by Q1 and Q4, appears at the base of Q5. A high input impedance with a low output impedance is provided by Q5 and Q6. R17, in the emitter circuit of output stage Q6, is the bandwidth adjustment potentiometer. A portion of the output signal at Q6 is fed back via C6 and R16 to the emitter of Q4. Since this feedback is positive, the resultant regeneration emphasizes the center frequency in accordance with the settings of R17. As more regeneration is produced, the bandwidth becomes narrower. Conversely, as less regeneration is produced, the bandwidth becomes wider. Maximum bandwidth is -6 db per octave. Minimum bandwidth depends on the center frequency. A typical minimum bandwidth is -6 db at a center frequency of 50 cps, ±3 cps. It should be noted that the filter circuit lends itself to universal application, since the center frequency of operation can be changed through application of the formula shown in Figure 6-17. This formula determines the filter resistance and capacitance values needed for different center frequencies.

3.3.14.6.3 Amplifier Q2 is a class-A amplifier for use with signals of insufficient amplitude (0.1 volt peak-to-peak) to drive the filter. The amplifier has a voltage gain of two.

3.3.14.7 AGC Circuit

The AGC circuit basically consists of a variable attenuation network in which the output voltage is held constant by feedback control of a current generator. A schematic diagram of the AGC circuit is found in Volume II, figure 6-17, sheet 2 of 3.

Input signals at pin E of the AGC circuit board are clipped at the 17-volt peak-to-peak level by diodes CR1 and CR2. The signals are then routed through amplifier Q1 and connected to the bases of both PNP transistor Q2, and NPN transistor Q3. These two transistors function as clippers, with the clip level being determined by the respective collector circuit-divider networks. The emitter output from Q2 and Q3 is coupled through capacitor C5 to the AGC circuit proper. C5 isolates the variable attenuator diodes CR3 and CR4 from direct currents originating at the input circuit.

The variable attenuation network consists of forward-biased diodes CR3 and CR4, resistor R15, and transistor circuit Q5. The output of this network is held constant, regardless of the input, by changing the resistance ratio (Rd + R15)/Rd, where Rd is the diode resistance. This ratio, in turn, is changed by controlling the diode current through a current generator.

Transistor circuit Q5 functions as the current generator for the variable attenuation network. Along with feedback diode detector CR7, Q5 supplies more or less current to CR3 and CR4. In operation, detector CR7 utilizes a long time constant to determine the long-term average of the peak input-signal voltage. When CR7 detects a large peak signal, it tends to increase the current output of Q5, thereby lowering resistance Rd. Under these conditions the output voltage of the variable attenaution network tends to decrease. Conversely, a small peak signal decreases the output of Q5, thereby increasing resistance Rd. The output voltage of the attenuation network then tends to increase. In effect, the output of the variable attenuation network remains constant despite long-term changes in the peak voltage of the input signals.

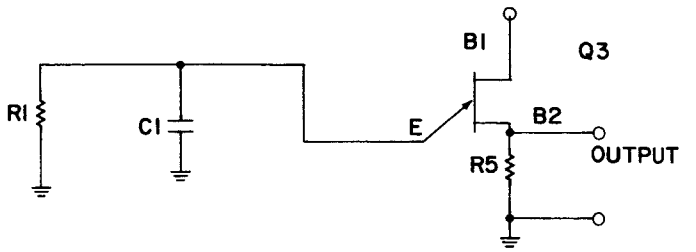
Output signals from the variable attenuation network are coupled through isolation stage Q4 to linear amplifier circuit Q6 and Q7. The amplified collector output at Q7 is then connected simultaneously to the bases of emitter followers Q8 and Q9. The emitter output of Q8 is used to derive the feedback signal for the variable attenuation network. The emitter output of Q9 constitutes the AGC output signal.

3.3.14.8 Detector Circuit

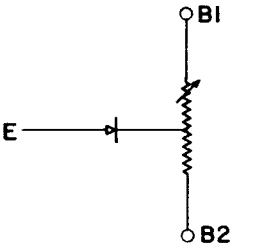
The detector circuit board contains a full-wave rectifier and filter driven by an emitter-follower stage. Reverse-connected diodes at the input provide peak positive and negative signal limiting for noise-rejection purposes. The detector board also contains a saturated amplifier stage.

3.3.14.9 Discriminator Circuit

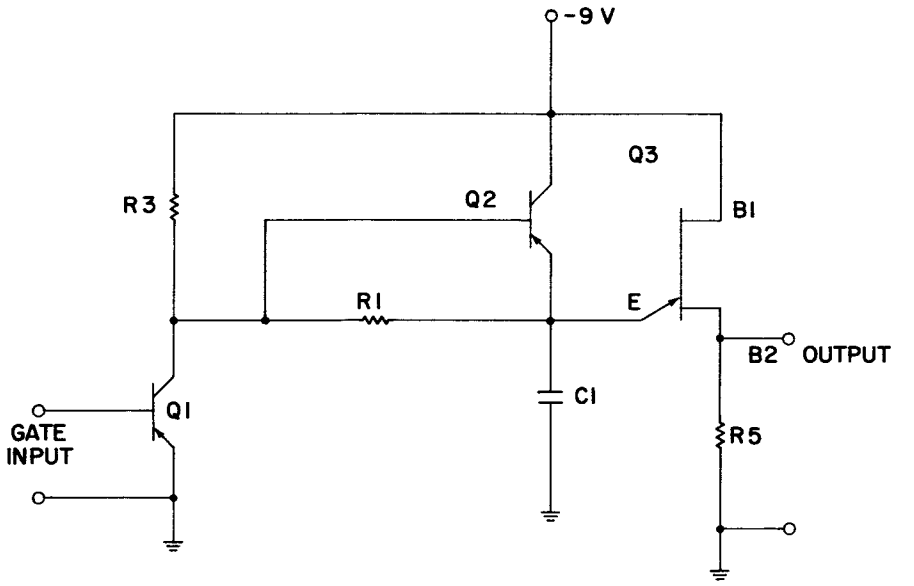
The discriminator circuit board contains a cascaded emitter-follower circuit (Darlington Circuit) which can be used with an external R-C integrator to drive, for example, a galvanometer amplifier.



(a)



(b)



(c)

Figure 3-12—Rundown Circuit, Simplified Schematics

The board also contains an amplifier stage which can be controlled to discharge or dump the integrator voltage, thereby interrupting the emitter-follower output. A schematic diagram of the discriminator circuit is found in Volume II, figure 6-17, sheet 3.

In operation, input signals at pin H of the discriminator board are differentiated by C1-R2. The negative portion of the differentiated signals are then passed through CR1 to pin F. An external R-C integrator is connected at F in this manner: The resistance part is connected between F and E, and the capacitance part is connected between E and ground. The integrated voltage at E is coupled through Q2 and Q3 to output pin D for connection to the external galvanometer amplifier. The integrated voltage is directly proportional to the frequency of the input signal. The collector of normally off transistor Q1 is also connected to the integrated voltage at E. When Q1 is turned on by a negative input at pin 4, the collector is returned to ground, thus providing a discharge path for the integrator capacitor. This operation drives the emitter of Q3 to ground, thereby interrupting the output at D for the period of the dump.

3.3.14.10 Rundown Circuit

The rundown circuit board contains five functionally identical gated relaxation oscillators utilizing the unijunction transistor. A schematic diagram of the Rundown Circuit is found in Volume II, figure 6-17, sheet 3.

Figure 3-12(a) is a simplified circuit of a unijunction-transistor relaxation oscillator. Figure 3-12(b) is the equivalent circuit of the unijunction transistor. In figure 3-12(b), base 1 and base 2 form a resistance-dividing network. The diode represents the emitter diode. The resistance of base 1 is shown as variable since this resistance varies with the emitter current. In operation, the unijunction transistor functions as an oscillator because of its highly stable negative-resistance characteristics. With power connected at B1 (figure 3-12(a)), the emitter-base junction E-B1 of Q3 becomes forward biased. Capacitor C1 thus charges to approximately the B1 supply voltage. Simultaneously, B2 approaches its most negative voltage level. When a certain minimum potential difference between E and B1 is reached, the emitter E presents a high impedance to C1, and C1 begins to discharge through R1. Since emitter current is now cut off, B1 and B2 form a fixed voltage divider with a more positive voltage at B2. Capacitor C1 continues to discharge through R1 until the emitter-base 1 junction E-B1 again becomes forward biased. The sequence is then repeated.

A simplified diagram of the rundown circuit is shown in figure 3-12(c). Capacitor C1 is charged to approximately -9 volts when power is initially applied. The rundown sequence begins when a negative voltage level is connected at the gate input of Q1. This operation causes the collector of Q1 to go to ground, thereby reverse-biasing Q2 and providing a discharge path for C1 through R1. The oscillator or rundown continues until a ground level is connected at the gate input of Q1. At this time, Q1 is reverse biased, Q2 is forward biased, and C1 again charges to approximately -9 volts. Q2 holds C1 in a charged state until the next gate level is applied. The base-2 output of unijunction transistor Q3 is ac-coupled to the base of saturating amplifier Q4. This saturating stage converts the base-2 level charge to a saturated pulse suitable for logic functions.

3.3.14.11 Flipflop

The flipflop circuit board contains four Eccles-Jordan flipflops and two passive AND gates. A schematic diagram of the flipflop is shown in Figure 1-17, sheet 3, of Volume II. The flipflop set and reset inputs are ac-coupled. By connecting these two inputs together, the circuit operates as a binary counter. Positive step voltages at the inputs constitute true signals. DC set and reset inputs are also included in the circuit. The AND gates can be used to implement the four flipflops as a decimal counter.

3.3.14.12 NAND Circuit

The NAND circuit board contains (a) six two-input NAND gates with inverter transistor outputs, (b) two expandable input NAND gates with inverter transistor output, and (c) two two-input diode clusters. A schematic diagram of the NAND circuit is shown in figure 6-17, sheet 3, of Volume II. The circuit performs the NAND function for negative true signals. The two expandable input NAND gates have anode inputs to which extra diodes (such as the two-diode clusters) can be connected.

3.3.14.13 Power Supply

The power supply board contains two series-regulated power supplies with respective dc outputs of +8 volts at 300 milliamperes, and -9 volts at 400 milliamperes. Both power supplies operate from a common input transformer and full-wave recitfier to change an unregulated input voltage to a regulated output voltage.

3.3.14.13.1 A schematic diagram of the power supply board is shown in figure 6-17, sheet 2, of Volume II. Voltage regulation is achieved by controlling the gain of a series power transistor in accordance with output voltage variations. In operation, the output of each supply is referenced to a constant voltage source provided by a zener diode. Voltage differences sensed between the output divider network and the reference source are coupled through an amplifier stage to vary the gain of the series regulator. Any increase in output voltage reduces the gain of the series regulator, thereby lowering the output voltage. Similarly, any decrease in output voltage increases the gain of the series regulator, thereby raising the output voltage. Each power supply is protected against excessive load currents by current limiting resistors. The supply voltages can be varied finely by adjusting separate trim potentiometers in the divider network of each regulator.

SECTION IV.
MAINTENANCE

4.1 APPROACH

This section contains information on the performance of preventive and corrective maintenance for the Universal Real-Time Data Reduction System No. 1. To assist in troubleshooting, photographs showing the location of components on all special circuit boards designed by Goddard Space Flight Center are included, as well as timing diagrams for various units of the system.

4.2 PREVENTIVE MAINTENANCE

To minimize the incidence of mechanical failures, it is essential to comply with the referenced operation and maintenance instructions for data-recording equipment listed in table 1-1.

4.2.1 INSPECTION SCHEDULE

Except for the mechanical components of the standard commercial units listed in table 1-1, and the forced air cooling-system components of each cabinet, inspection of the equipment consists of the periodic visual examinations of wiring, controls, etc., which are a part of the basic routine practiced by every well-trained electronics technician. Refer to the equipment manuals listed in table 1-1 for inspection schedules applicable to equipment requiring special attention because of the moving parts involved. Check the fan motors in each equipment cabinet daily to be sure they are operational, and clean the air filter associated with each fan at least once a week. When severely dusty environmental conditions are encountered the air filters should be cleaned more frequently. A vacuum cleaner or source of dry compressed air is satisfactory for cleaning the filters. Dry compressed air should also be used to remove accumulated dust from the wiring and other electrical components at least once a month, and more often if made necessary by severe environmental conditions.

4.2.2 LUBRICATION SCHEDULE

The motor-drive components of the digital recorders and recording oscillographs require lubrication at regular intervals. Refer to the applicable manuals for this equipment (table 1-1) for lubrication instructions. The fan motors located in the equipment cabinets are self-lubricating, sealed-bearing devices, and should be replaced if subject to overheating and/or rotational failure.

4.2.3 MINOR REPAIR AND ADJUSTMENT

Modular construction is employed throughout the system for all functional units designed by the Data Instrumentation Development Branch of Goddard Space Flight Center. Standard 3CS-BLOCS, which serve as multiple receptacles for standard S-PAC digital modules and their equivalents, are used for this purpose. The S-BLOCS and S-PAC modules are thoroughly described by the "Instruction Manual for S-PAC Digital Modules," Publication No. 71-100A. Refer to this book, which is issued by the Computer Control Company, Inc., Framingham, Mass. as a guide to the minor repair and adjustment of the digital module circuits and circuit boards. Defective modules should be replaced with counterparts which are known to be good.

CAUTION

Turn off all secondary power to avoid damage to semiconductor elements when making or breaking connections between the printed-circuit card modules and the S-BLOC receptacles.

Refer to the equipment manuals listed in table 1-1 for the minor repair and adjustment procedures applicable to the standard commercial units used in this system.

4.3 CORRECTIVE MAINTENANCE

As an aid to troubleshooting and maintenance, figures 4-1 through 4-13 show the locations of components on all the special circuit boards designed by Goddard Space Flight Center. Figures 4-14 through 4-21 are timing diagrams for various units of the system. The wiring diagram for the inter-rack ac power connections is figure 6-16 of Volume II. Figure 6-18 of Volume II shows the wiring connections between the rejection and bit-rate filters and the remainder of the system.

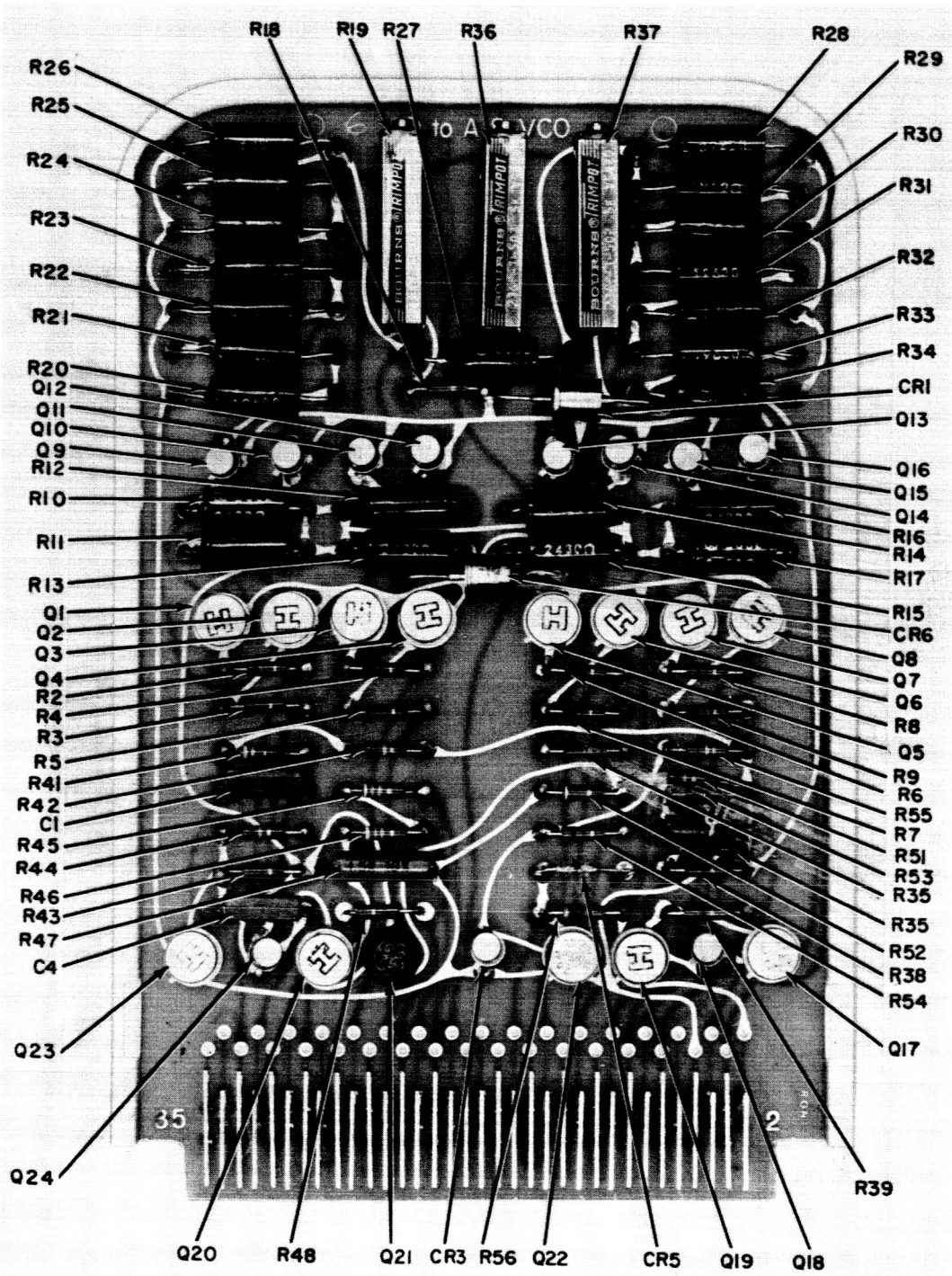


Figure 4-1. D to A Converter and VCO, Component Locations

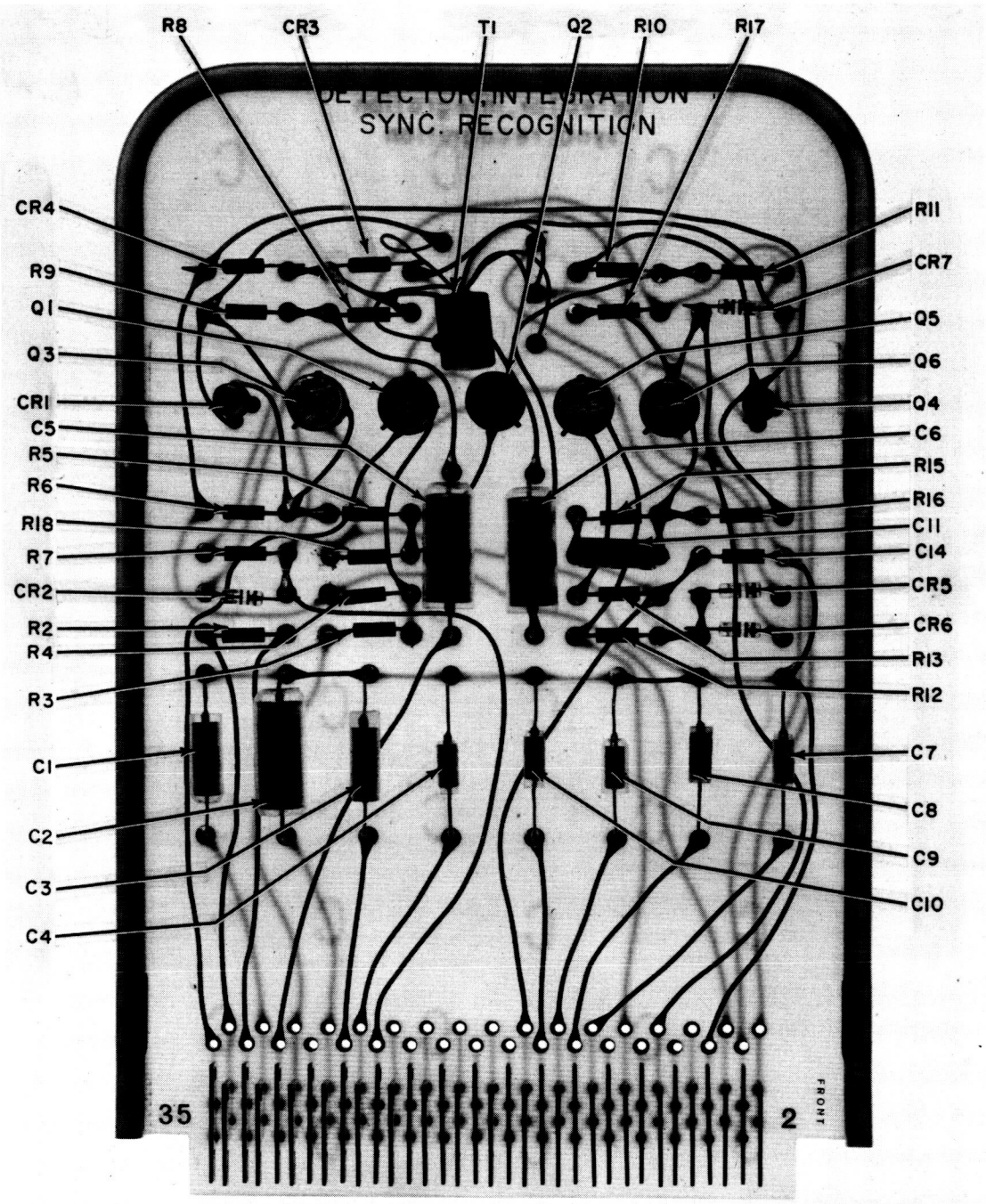


Figure 4-2. Detector, Integration, and Sync Recognition, Component Locations

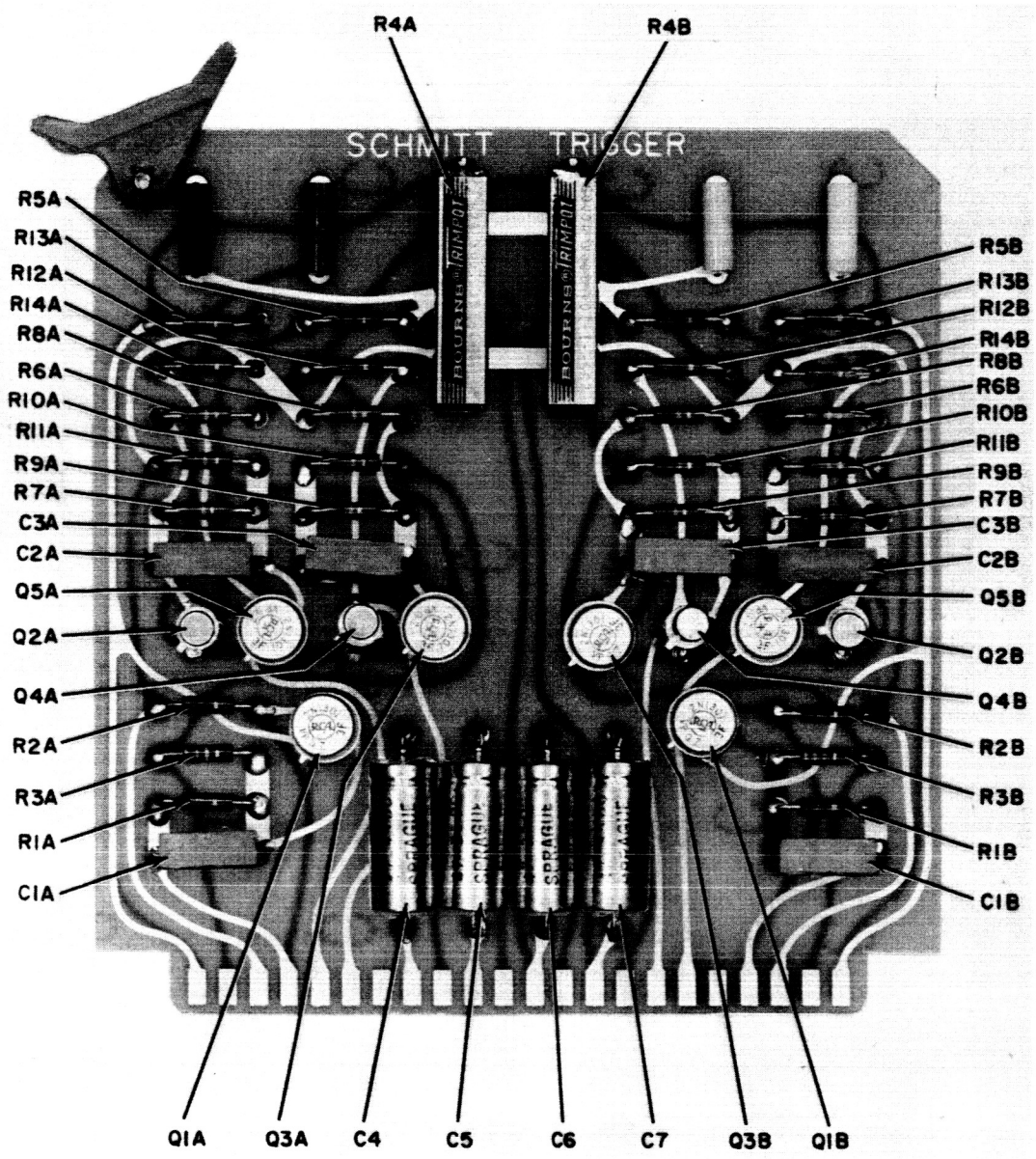


Figure 4-3. Schmitt Trigger, Component Locations

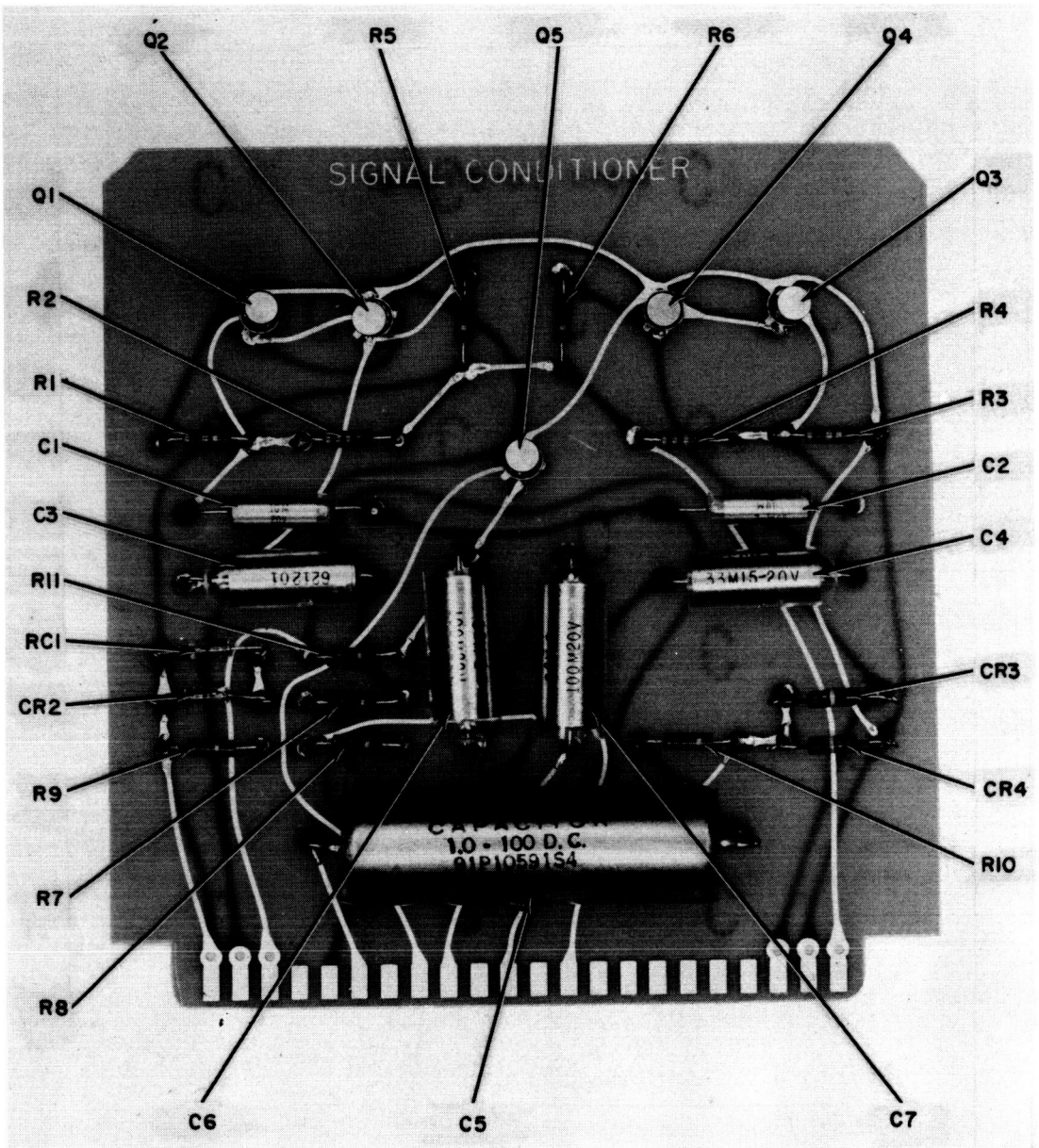


Figure 4-4. Signal Conditioner Board No. 1, Component Locations

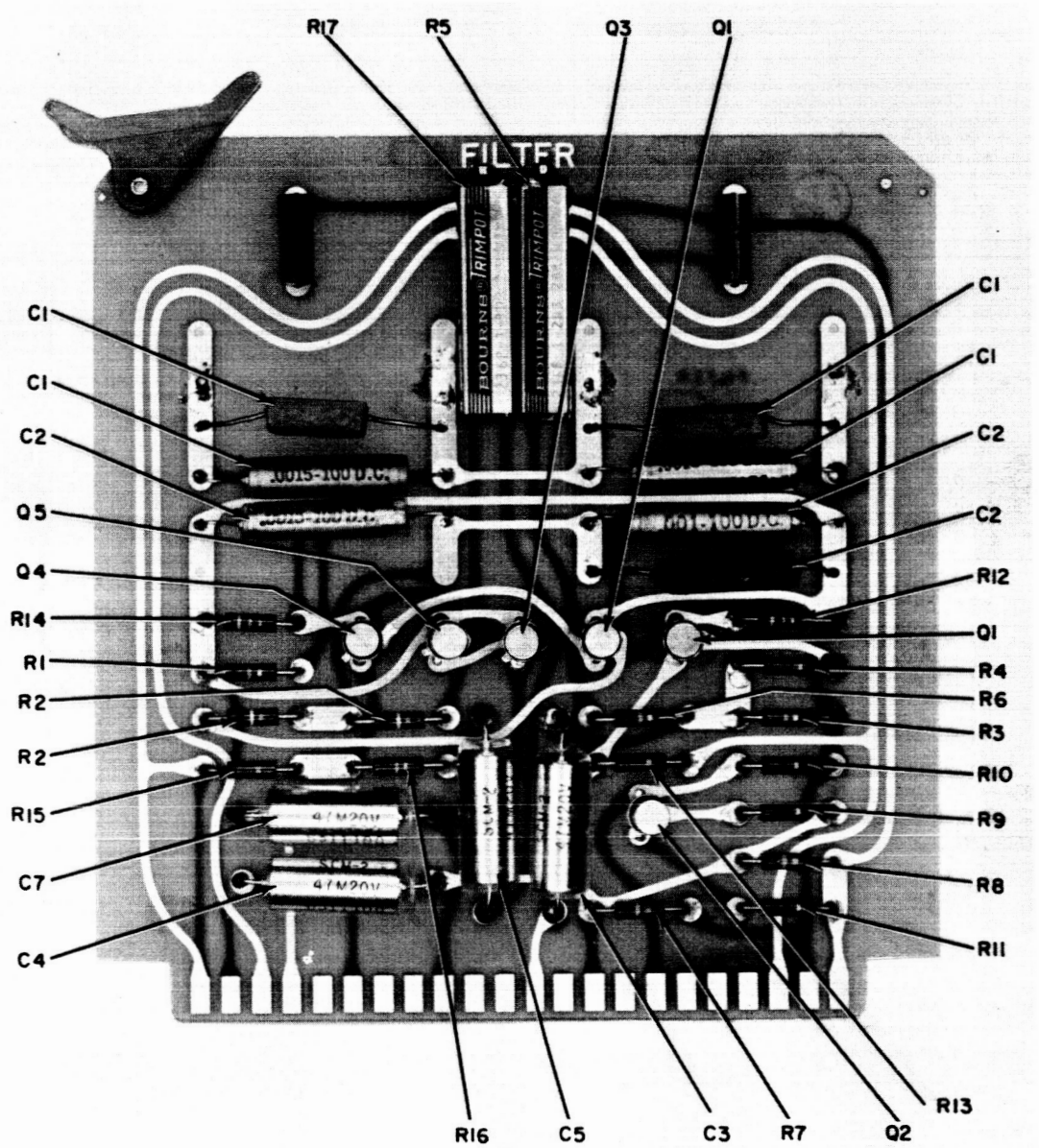


Figure 4-5. Filter and 2X Amplifier, Component Locations

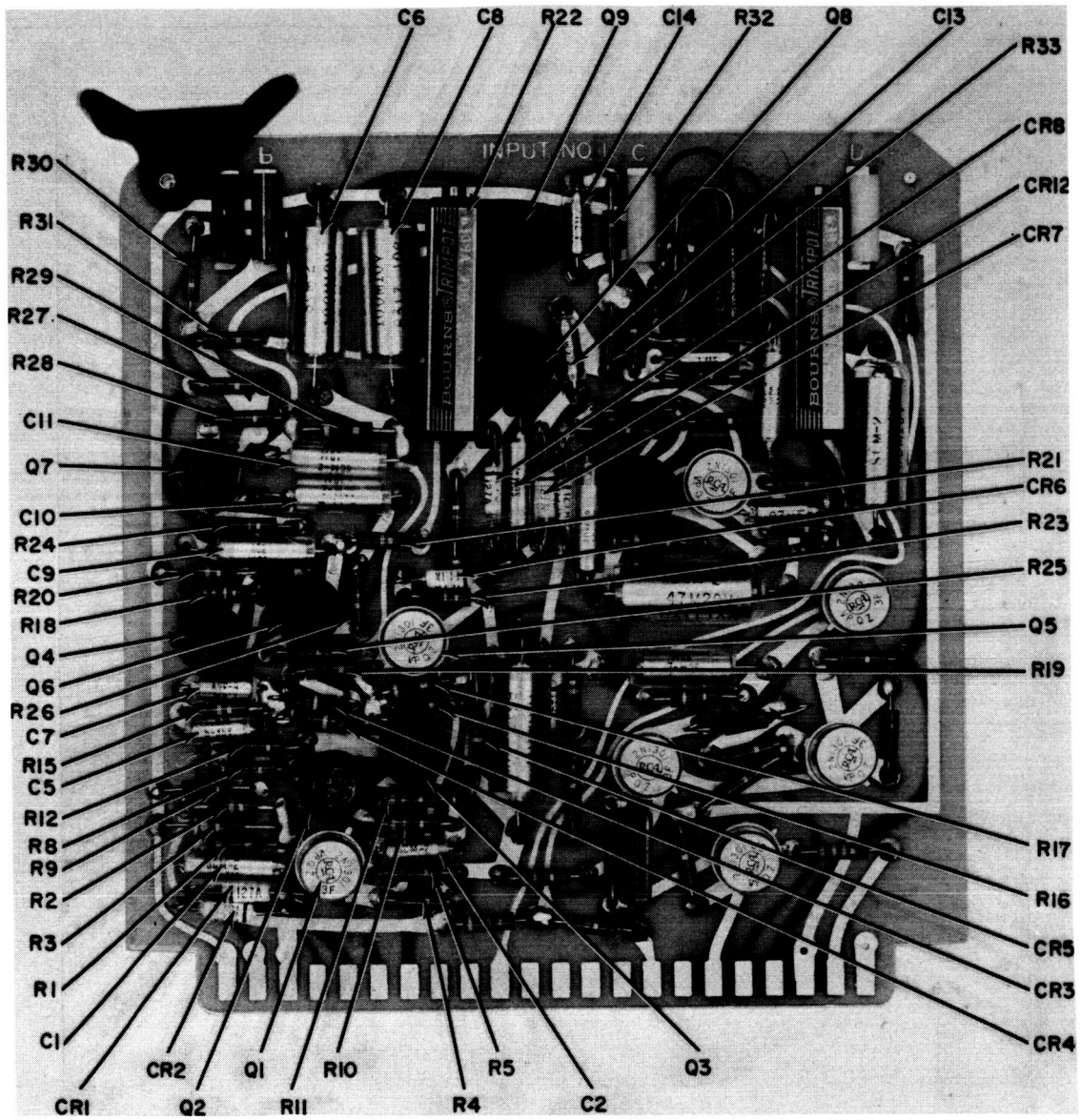


Figure 4-6. AGC Circuit, Component Locations

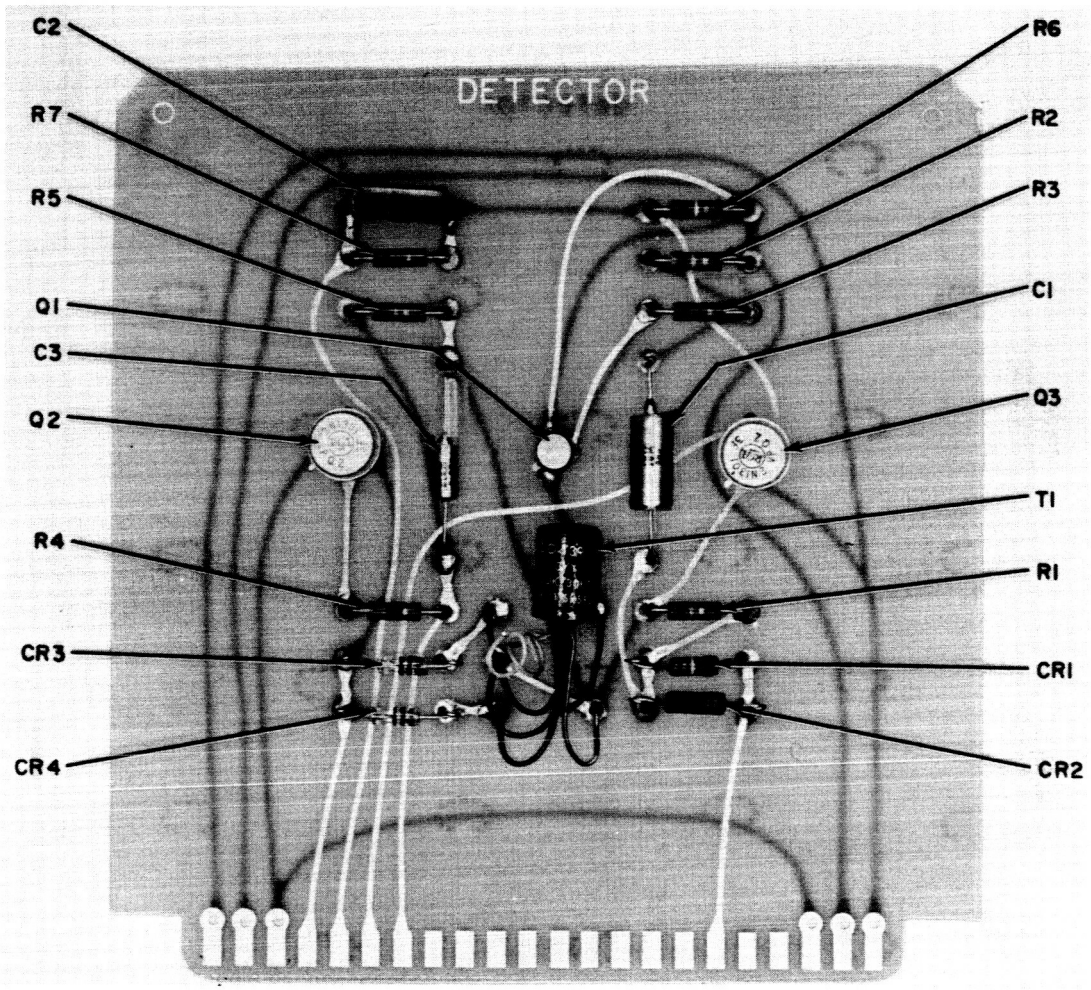


Figure 4-7. Detector Circuit, Component Locations

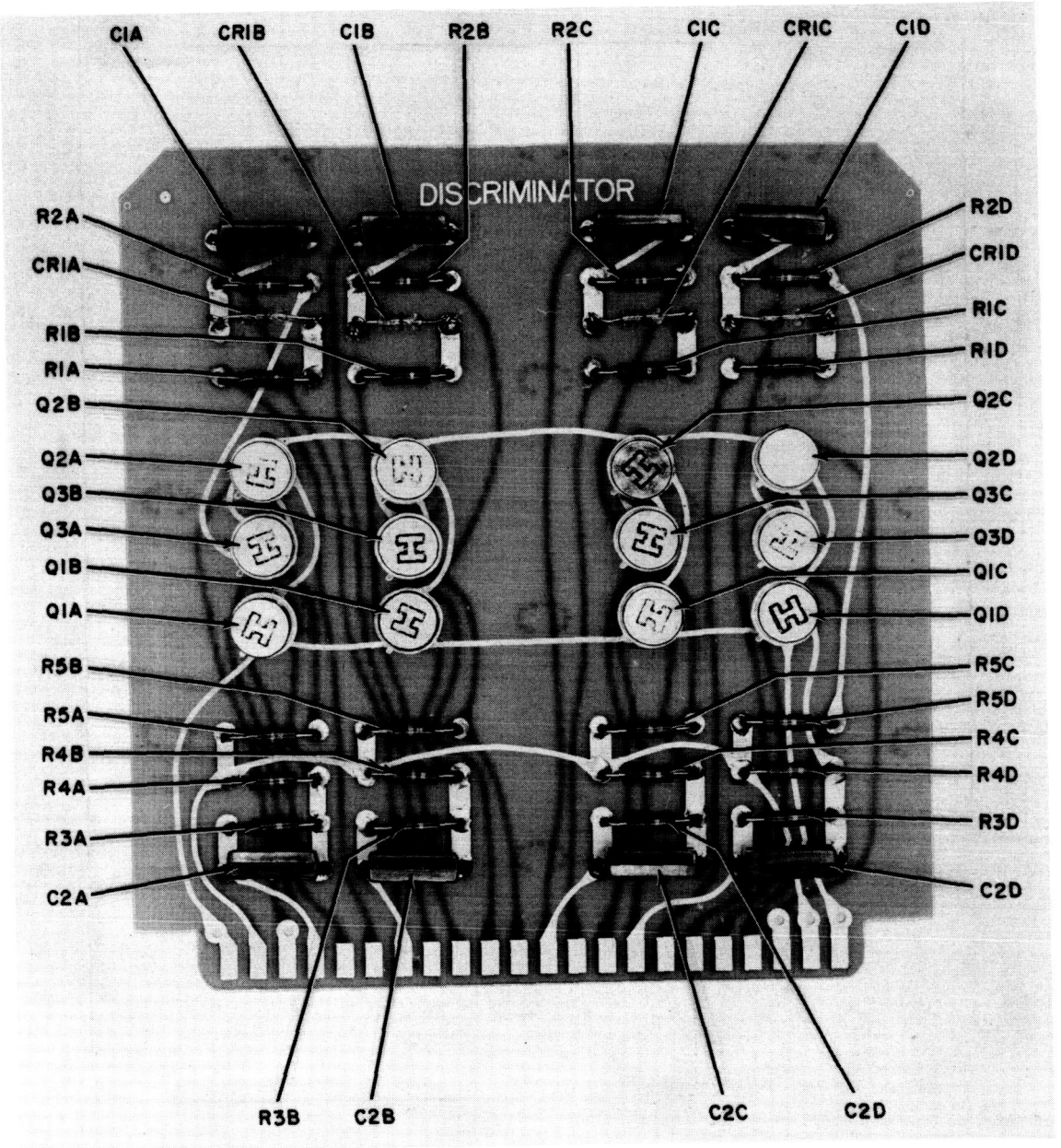


Figure 4-8. Discriminator, Component Locations

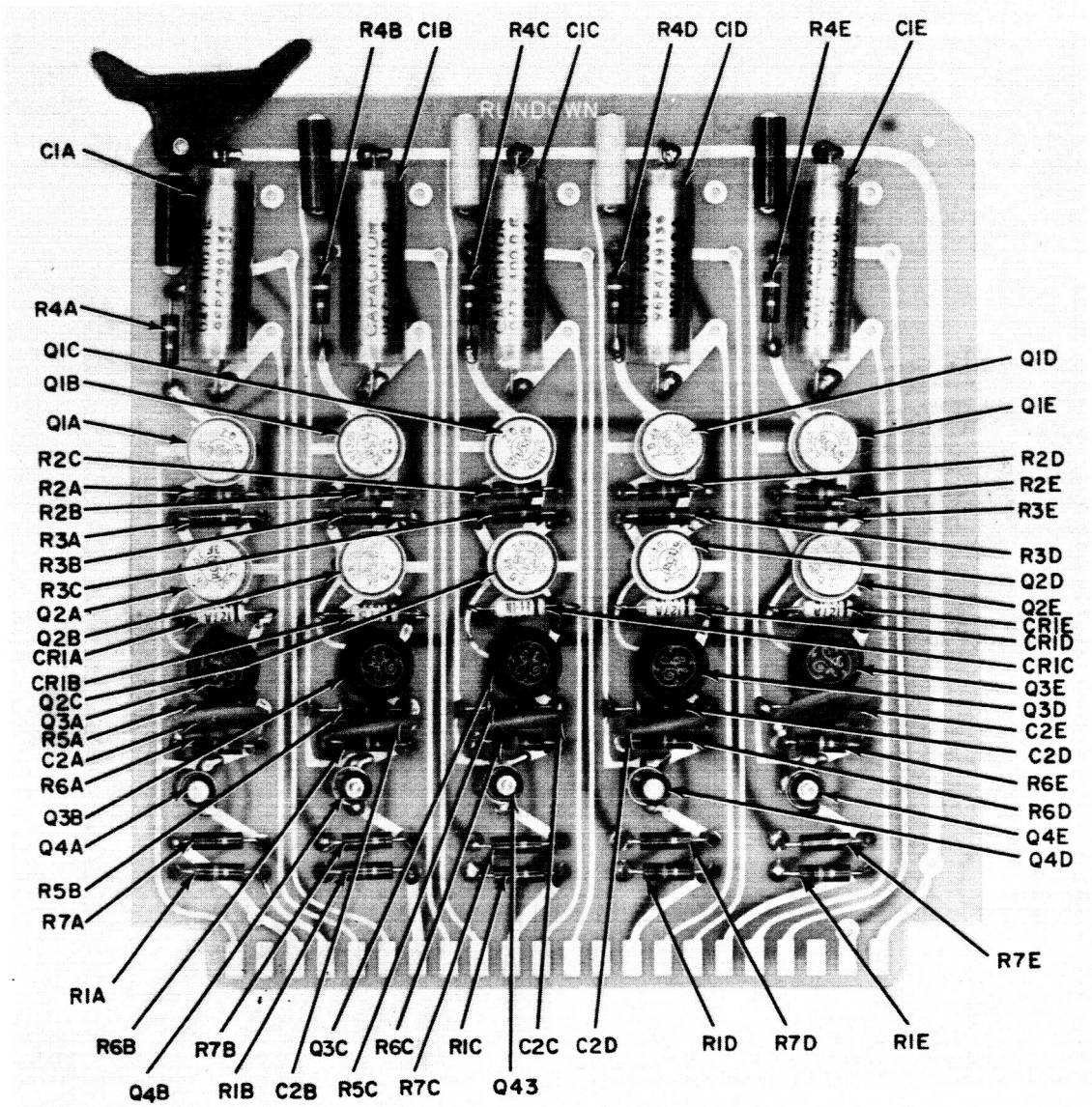


Figure 4-9. Rundown Circuit, Component Locations

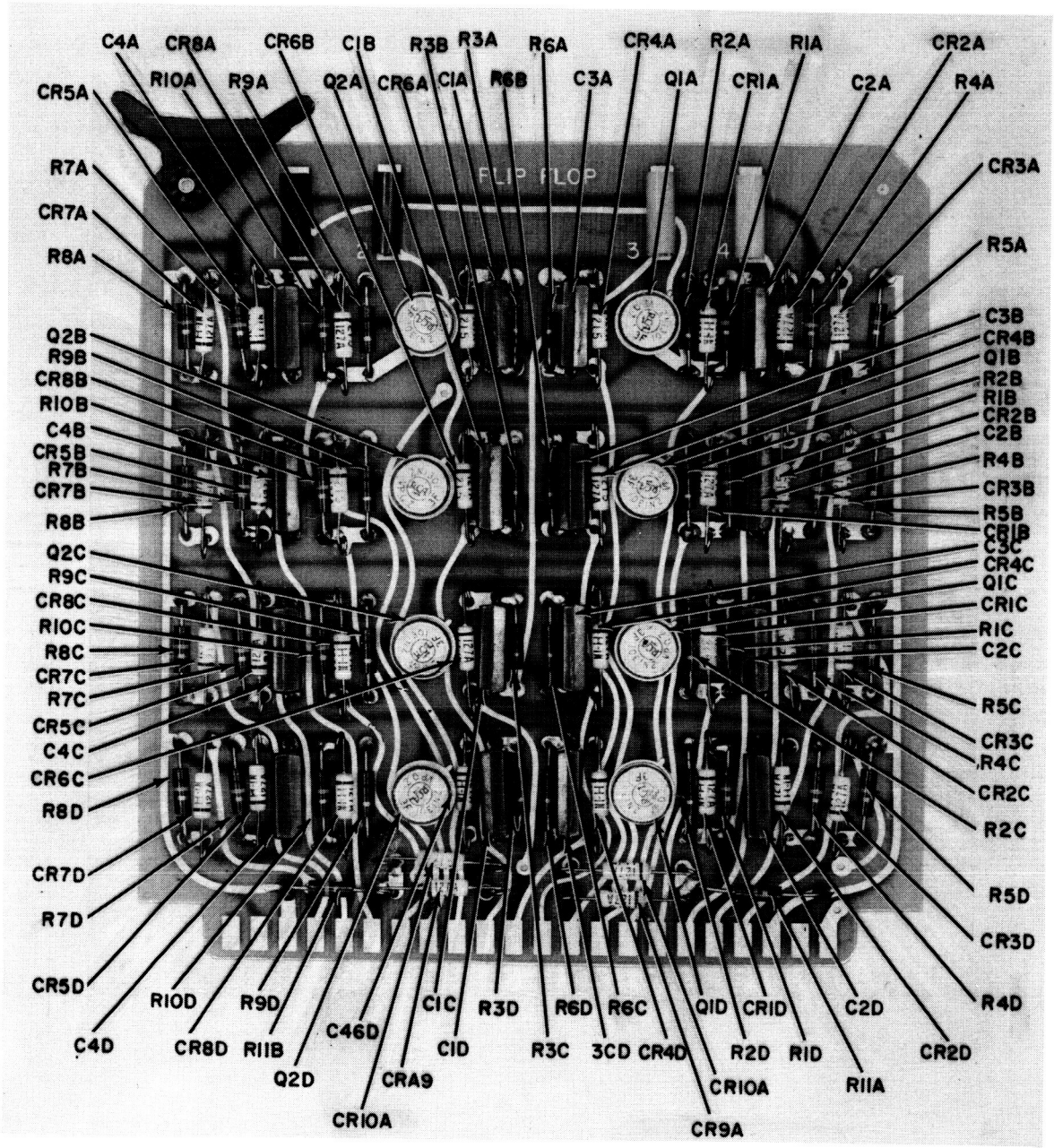


Figure 4-10. Flipflop, Component Locations

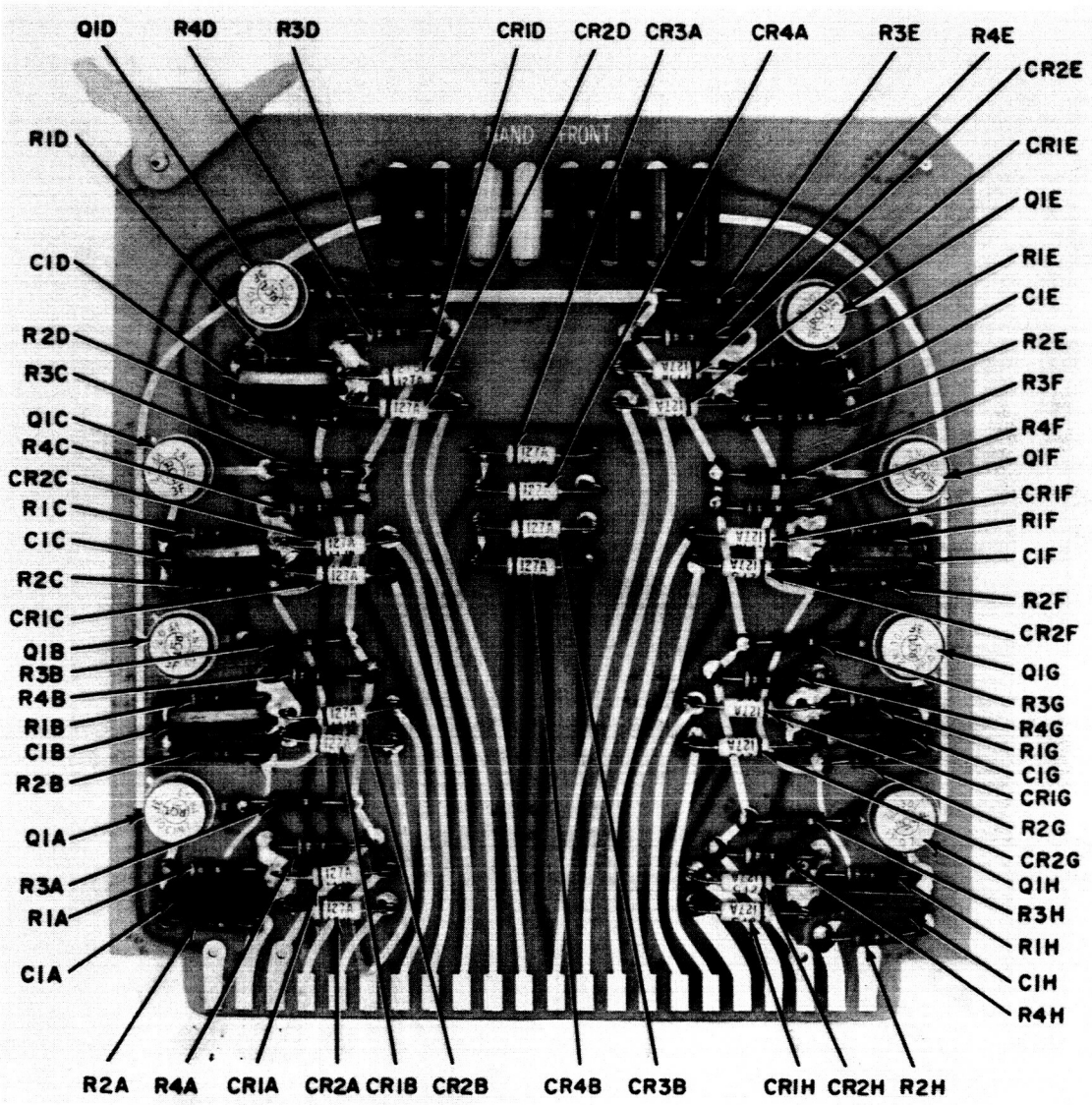


Figure 4-11. NAND Circuit, Component Locations

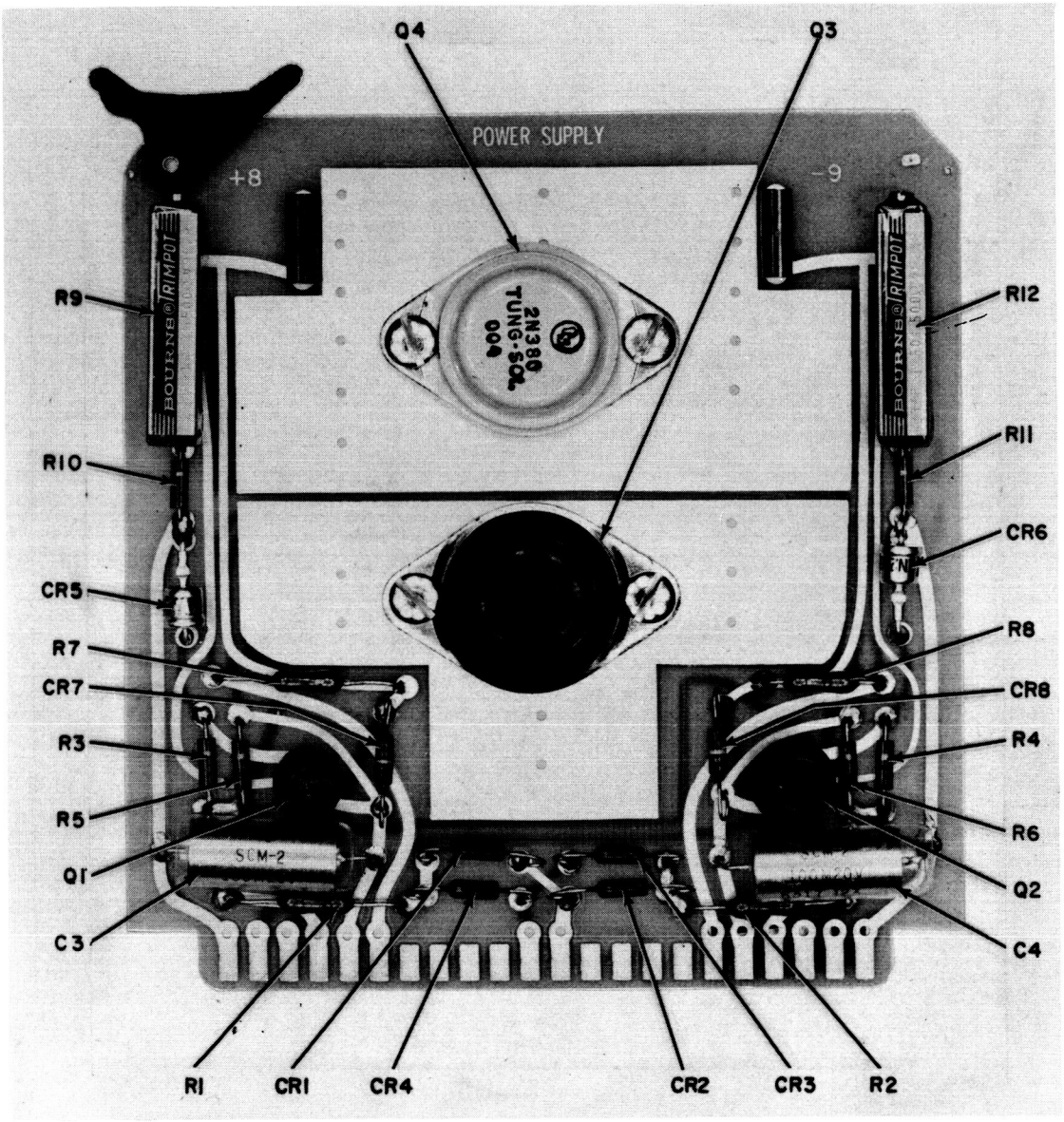


Figure 4-12. Power Supply, Component Locations

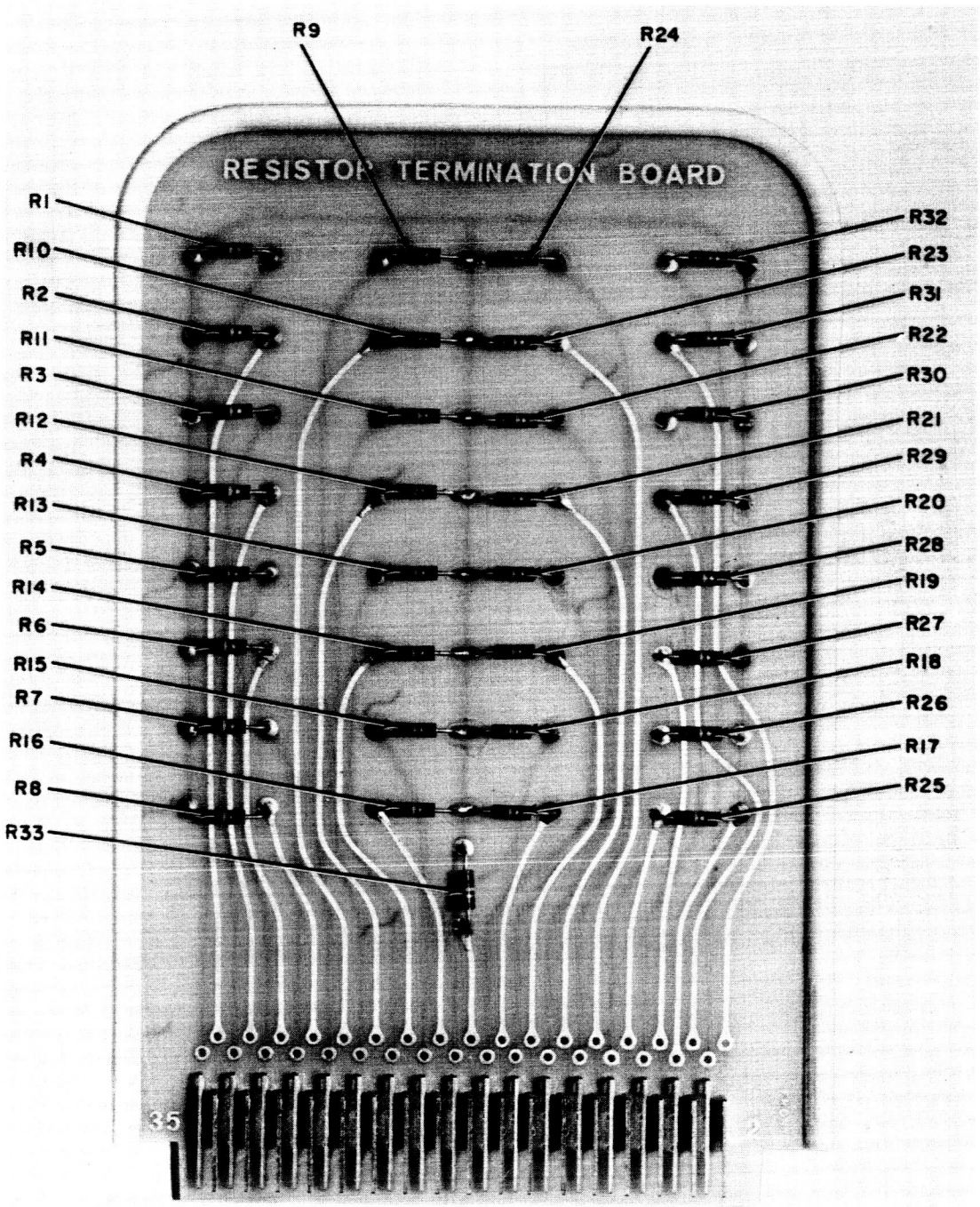


Figure 4-13. Resistor Termination Board, Component Locations

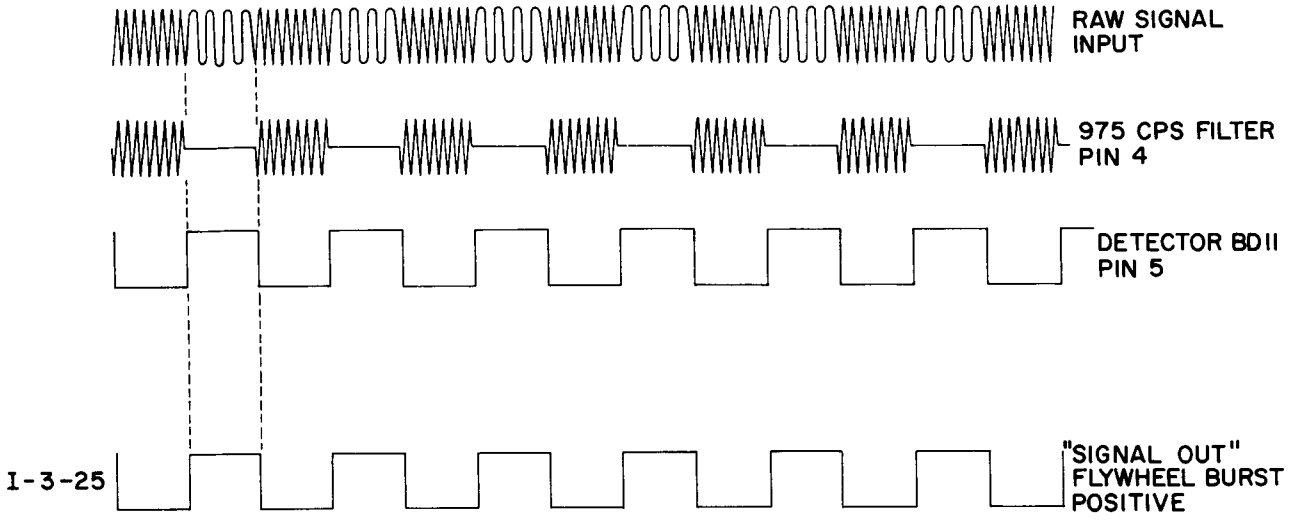


Figure 4-14. Bit Synchronizer, Timing Diagram

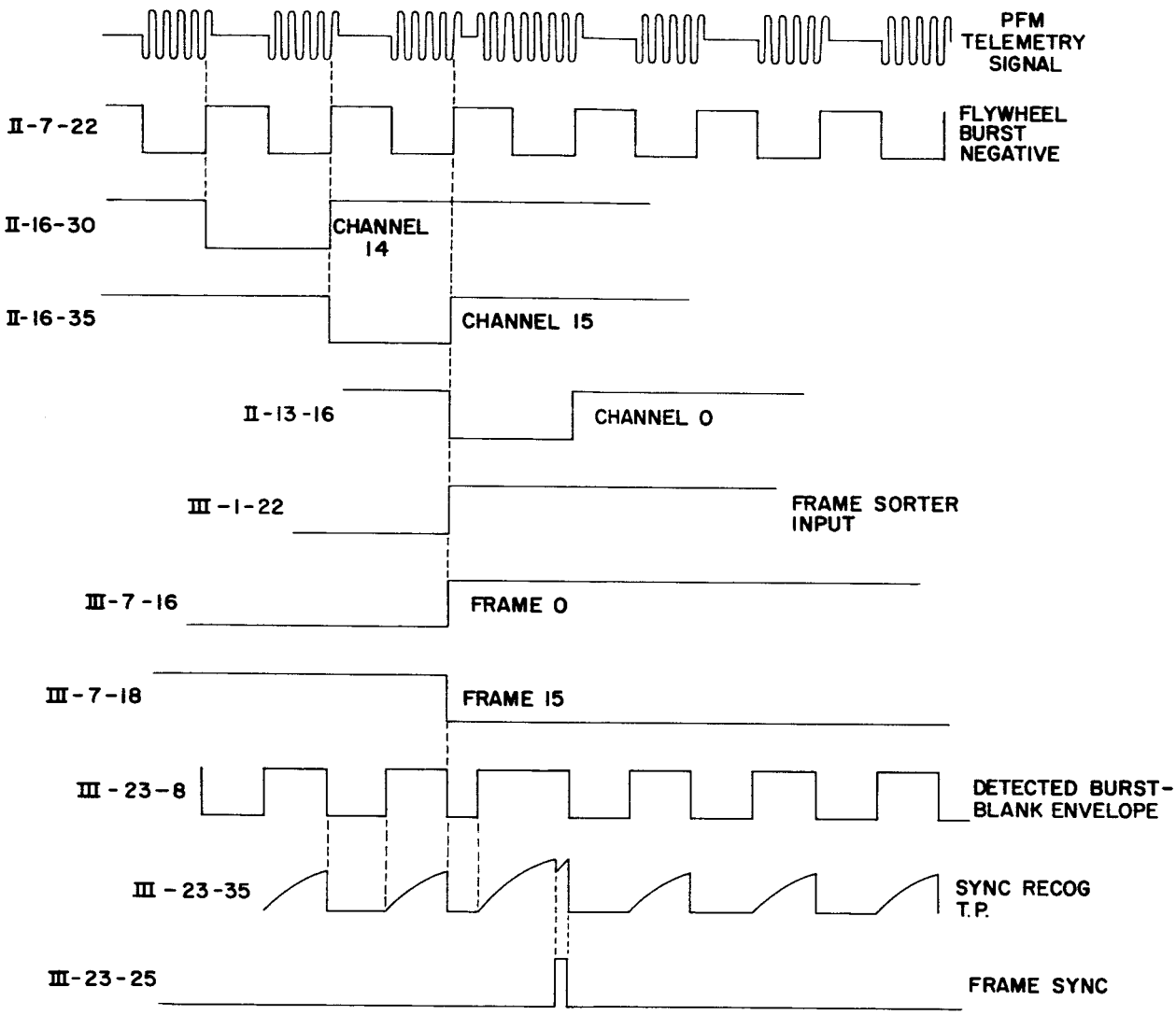


Figure 4-15. Frame and Channel Control, Timing Diagram

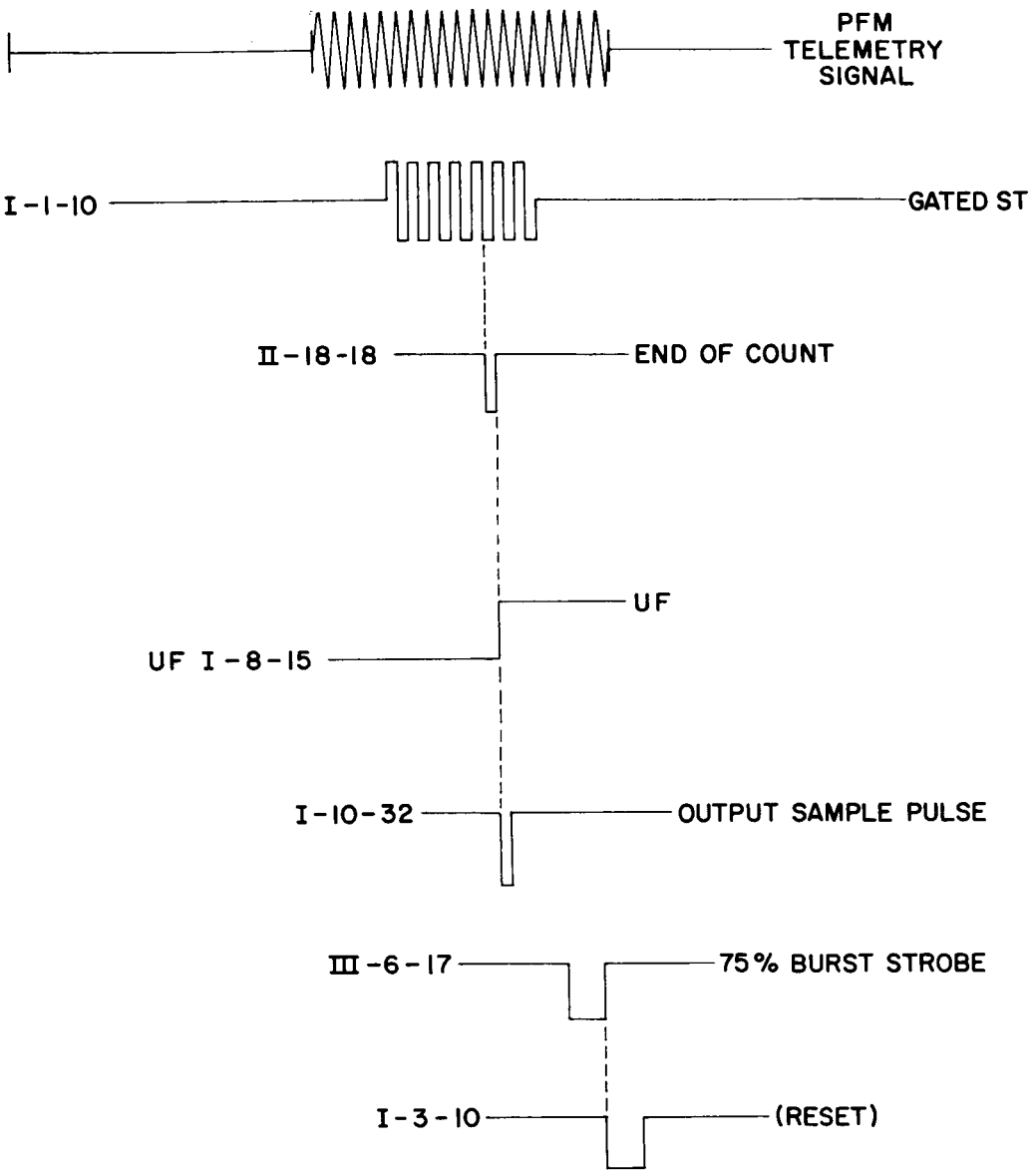


Figure 4-16. Digital Comb Filter, Timing Diagram

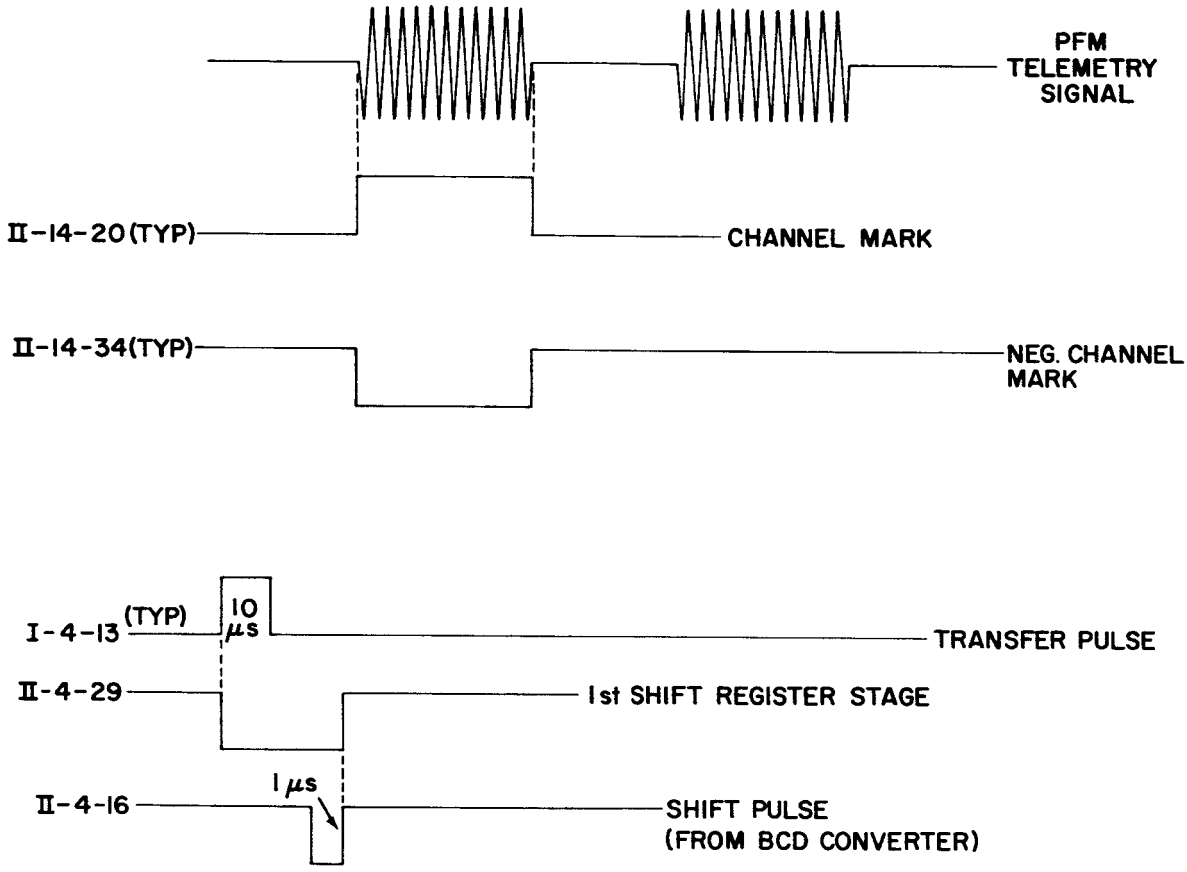


Figure 4-17. Hold Register, Timing Diagram

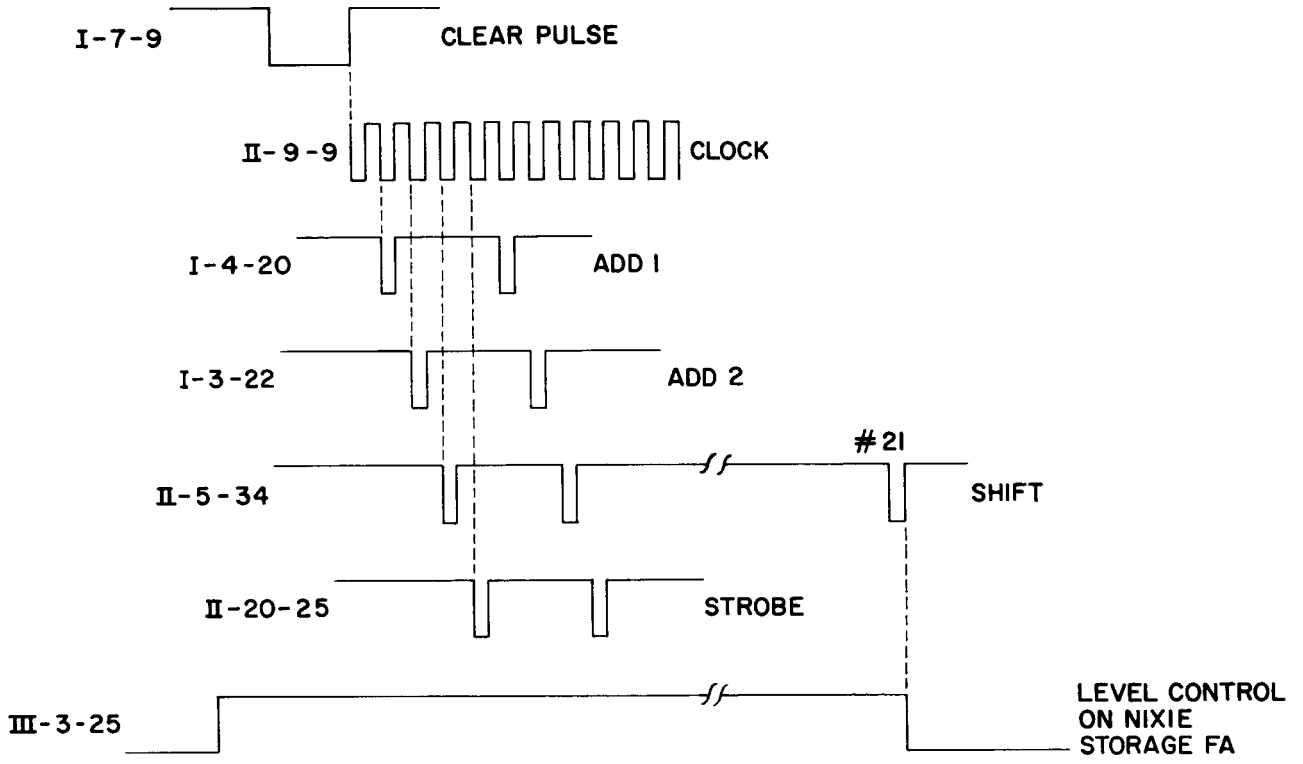


Figure 4-18. Binary-to-BCD Converter, Timing Diagram

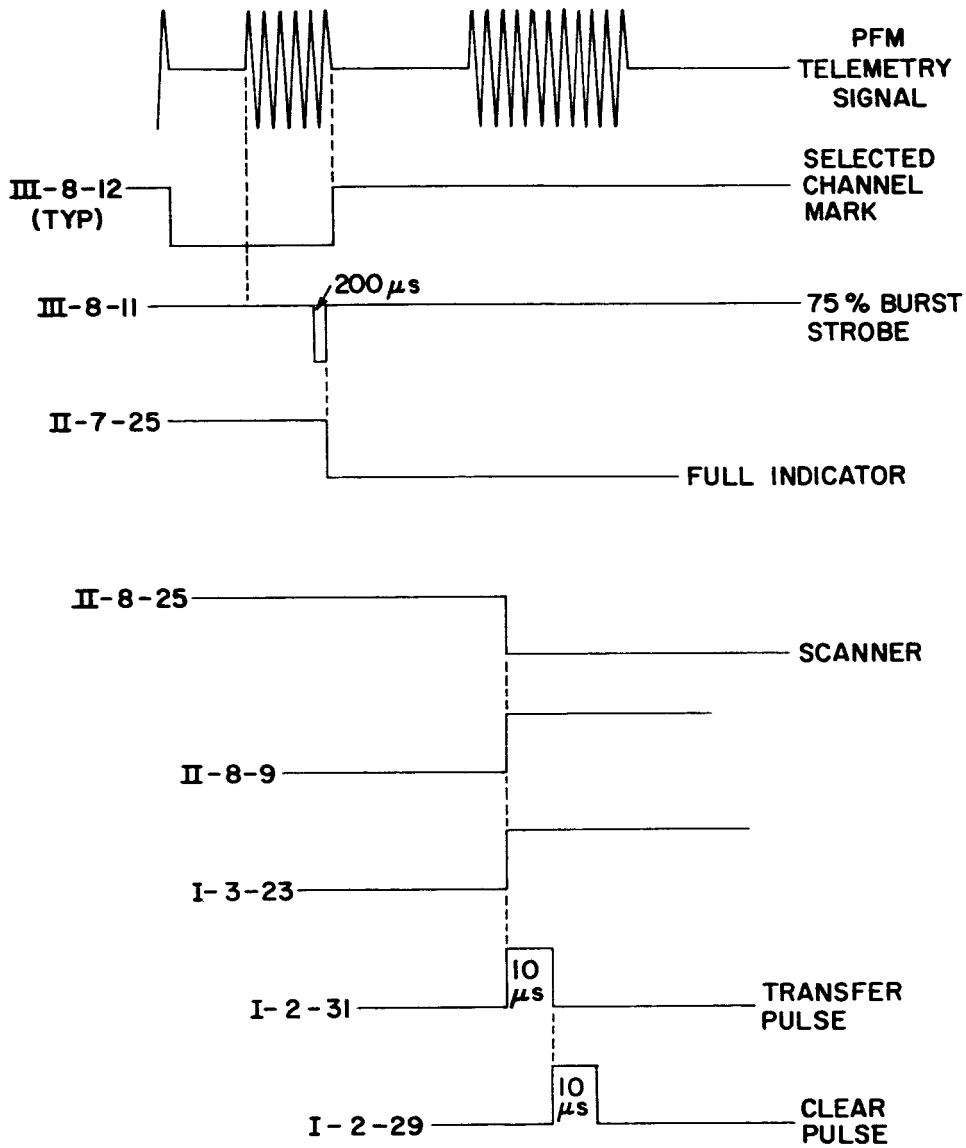


Figure 4-19. Digital Readout Control, Timing Diagram

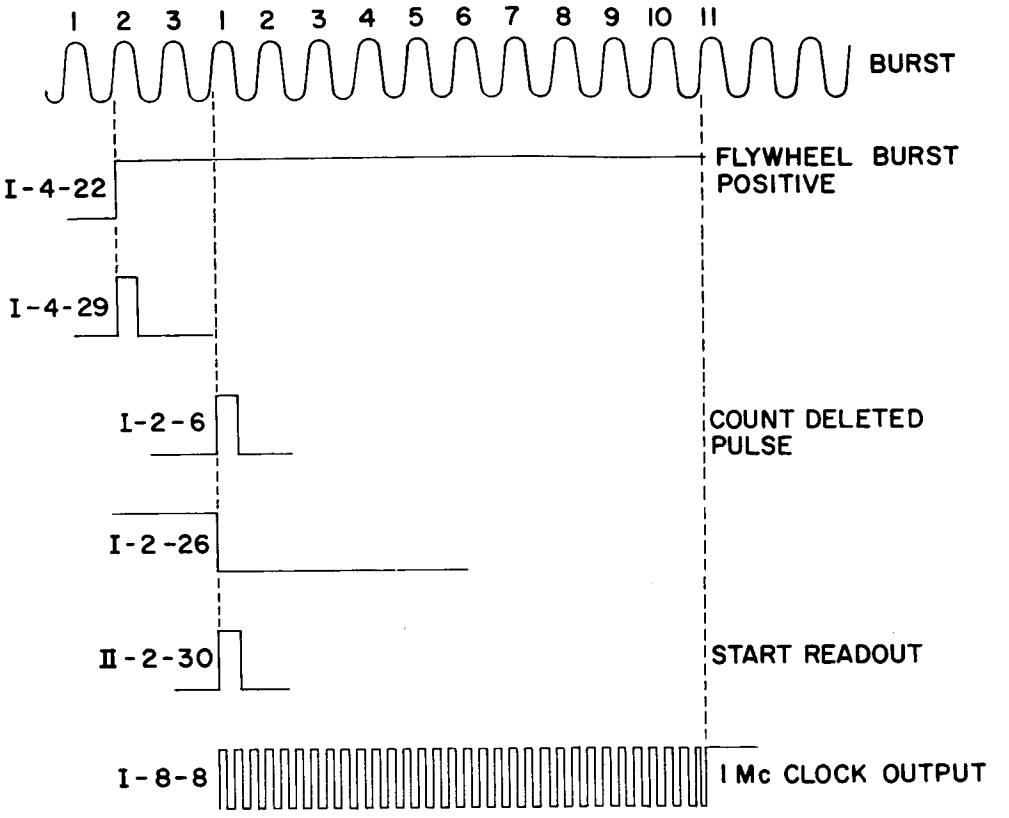


Figure 4-20. Printer Code Converter, Timing Diagram

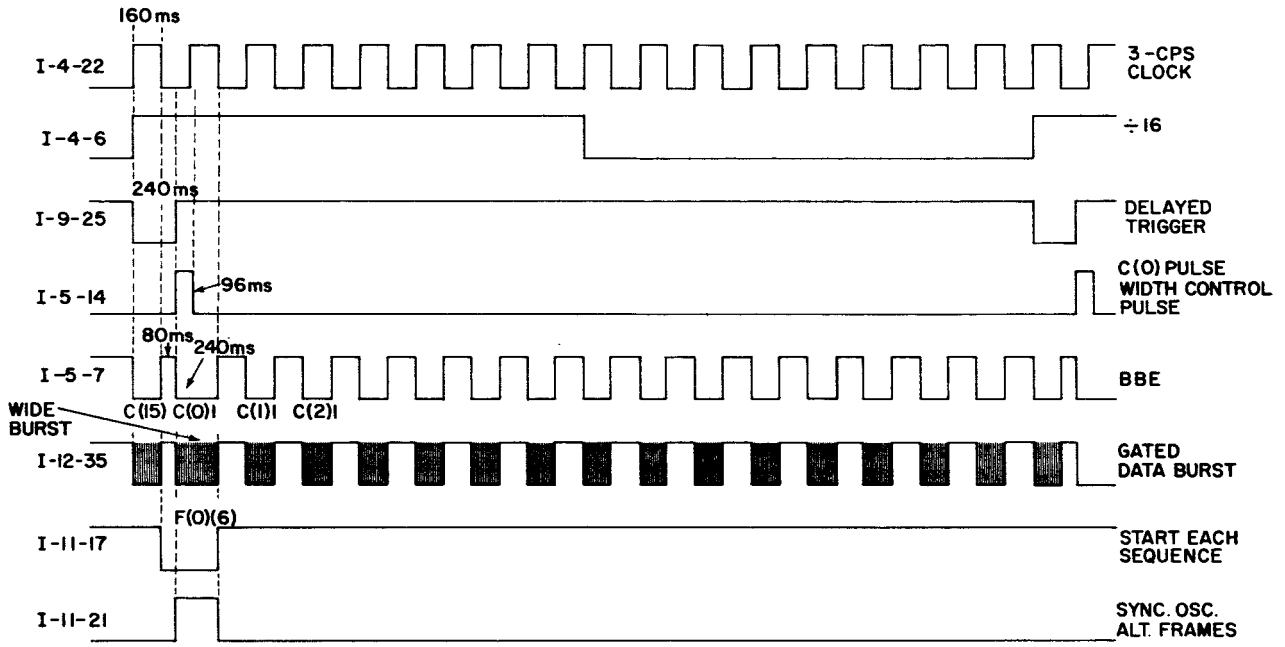


Figure 4-21. Simulator (Special Box), Timing Diagram

SECTION V.
PARTS LIST

Reference Designation	Figure Number	Description	Manufacturer	Mfg. Part Number	Qty.
		Digital Comb Filter			
	6-4, sheet 4	Pin Board, 525 hole	Amp, Inc.	397540-3	1
	6-4, sheet 8	Pin Board, 75 hole	Amp, Inc.	397540-9	2
		Pins	Amp, Inc.	495831	-
	6-4, sheet 4	Indicator lights	Computer Control	UI-30	9
Sw1	6-4, sheet 1	Switch, test-operate	Central Lab	PA67	1
	6-4, sheet 1	Switch, pushbutton	Grayhill	2201	1
		Bit Synchronizer			
Sw702	6-2, sheet 2	Switch, bit-rate selection 5 position, 2 wafers	Central Lab	PA73	1
		Switch, ext. meter, SPDT	Arrow	CHH-24213	1
	6-2, sheet 2	Switch, operate-set, DPDT	Torbal	DP-6	1
	6-2, sheet 1	Potentiometer, phase adj., knobpot	Bournes	3600S-1-104	1
	6-2, sheet 2	Potentiometer, VCO frequency	Dekapot	DP311	1
	6-2, sheet 2	Meter, VCO	Honeywell	MM1	1
	6-2, sheet 2	Indicator lights, VCO	Computer Control	UI-30	2
		Frame and Channel Control			
Sw1	6-3, sheet 1	Switch, frame-sync recognition	Central Lab	PA63	1
Sw2	6-3, sheet 1	Switch, bit rate	Central Lab	PA63	1
Sw3	6-3, sheet 2	Switch, sync search and lock reset pushbutton	Grayhill	2201	1
	6-3, sheet 3	Switch, channel selector	Central Lab	JU9001	1
R101	6-3, sheet 1	Potentiometer, sync integrator adj., knobpot	Bournes	3600S-1-503	1
	6-3, sheet 2	Indicator lights, search-lock	Computer Control	UI-30	2

Reference Designation	Figure Number	Description	Manufacturer	Mfg. Part Number	Qty.
		Program Board No. 2			
		Removable patchboard, 480 holes	Amp, Inc.	595534-2	1
		Frame and spring assembly	Amp, Inc.	695305-3	1
		Power Supply	Computer Control	RP-32	2
		Rejection Filter	Dytronics	Mod. 722	
		Bit Rate Filter	Dytronics	Mod. 720	
		Control Panel No. 3			
M300	6-13	Elapsed time meter	Marion	HM3-ET	1
		Circuit breakers	Heineman		3
		Period Readout Control			
	6-10, sheet 3	Switches, SPDT miniature	Torbal	TS-3	288
		Control Panel No. 2			
S85	6-12	Switch, discriminator test	Electro Snap	A3-33-103	1
S81	6-12	Switch, pushbutton, frame sync search and lock reset	Grayhill	2201	1
S86	6-12	Switch, system input selection	Central Lab	PA73	1
S82	6-12	Switch, channel selector	Central Lab	JU9001	1
S83	6-12	Switch, frame selector	Central Lab	JU9001	1
R89	6-12	Potentiometer, disc. adj. knobpot	Bournes	3600S-1-104	1
S84	6-12	Switch, disc. adj.			1
		Indicator, period readout, nixie	Burroughs	Mod. 56	5
		Control Panel No. 1			
M1	6-11, sheet 1	Meter, bit-rate indicator, 1 ma	Honeywell	#MM1	1
DS53-54		Indicator lights, VCO high/low	Computer Control	UI-30	2
DS27-DS52		Indicator lights, digital word selected	Marco	VM300M	26
S2-S27		Switches, digital word select, DPDT	Torbal	DP6	26
S5-S10, S30, S31		Switches, remote-control indicator	Honeywell	2D5	8
DS81, 82, 83		Indicator light power	Drake	105	3
S1		Switch, power, TPST			1
DS55-DS63		Indicators, digital readout nixie	Burroughs	B5031	9
A1		Power Supply, 170v dc	Technipower, Inc.	M168	1

Reference Designation	Figure Number	Description	Manufacturer	Mfg. Part Number	Qty.
		Printer Code Converter			
S1	6-9, sheet 1	Switch, input	Central Lab	PA73	1
		Switch, miniature	Torbal	SP1	11
		Switch, burst-blank	Electro Snap	A3-33-103	1
		Program Board No. 1			
	6-15	Program patchboard, 1632 hole	Amp, Inc.	695316-2	1
		Frame and spring assembly 1632 contacts	Amp, Inc.	695010-4	1
		Terminal, solder lug	Amp, Inc.		
		System			
		Connector, 50 pin	USC	50M2SL 50F2SL	28
		Connector, 50 pin	CEC	500C-50P1-J-HS	10
		Connector	Cannon		40
		Connector, BNC	Amphenol	UG-58	21
		Connector, twistlock	Hubbell		4
		Connector, Blue Ribbon	Amphenol	30500-40500	2

APPENDIX I

A-1.1 APPROACH

This section deals with the programming necessary, and the special circuits which have been designed, to make the Universal PFM Real-Time Data-Reduction System compatible specifically with the IMP satellite telemetry format. It includes complete programming information for use with the IMP format, a diagram of the IMP format, a functional description of the special circuits referred to above, and a functional block diagram of the special box.

A-1.2 IMP TELEMETRY FORMAT

Figure A-1 is a graphic representation of the IMP telemetry format, which is described in detail by the document titled "IMP PFM Encoder (S-74)."* Of the six main modifications to the standard PFM telemetry format incorporated in the IMP format, those described in chapter I, paragraphs I(d) and I(e) are the most significant with respect to the special circuits referred to in this appendix. These circuits consist of the sequence identifier and the simulator, both of which are contained in the special box; the special lockout circuits located in the frame and channel control unit (figure 3-2); and the 975-cps filter/detector/clamp circuit of the bit synchronizer (figure 3-1). Chapter IV, paragraphs G.1 through G.4 of "IMP PFM Encoder" also contains information pertinent to the sequence identifier; information pertinent to the University of Chicago readout control circuits (also a part of the special box) will be found in chapter III, paragraph III-G of that document.

A-1.3 FILTER/DETECTOR/CLAMP

During the normally blank period of each digital information channel transmitted by the IMP telemeter, the carrier signal is modulated by a 975-cps fill-in frequency signal from the subcarrier oscillator. Whenever this condition exists, it is necessary to force the envelope-detector output signal (which excites the bit-rate filter) to -6v for the duration of each fill-in frequency transmission in order to extract the true burst/blank envelope from the incoming signal. This is accomplished with the output signal from a detector which senses the energy from a special filter designed to respond only to the 975-cps fill-in frequency. The filter/detector/clamp circuit is located between the output of the bit synchronizer signal-conditioning circuits and an input to the envelope detector of the frame and channel control integrate-and-dump special-circuit card, where the output from

*IMP PFM ENCODER (S-74) (Preliminary); Prepared by Code 631.1, GSFC, NASA; Revision A: August 6, 1962.

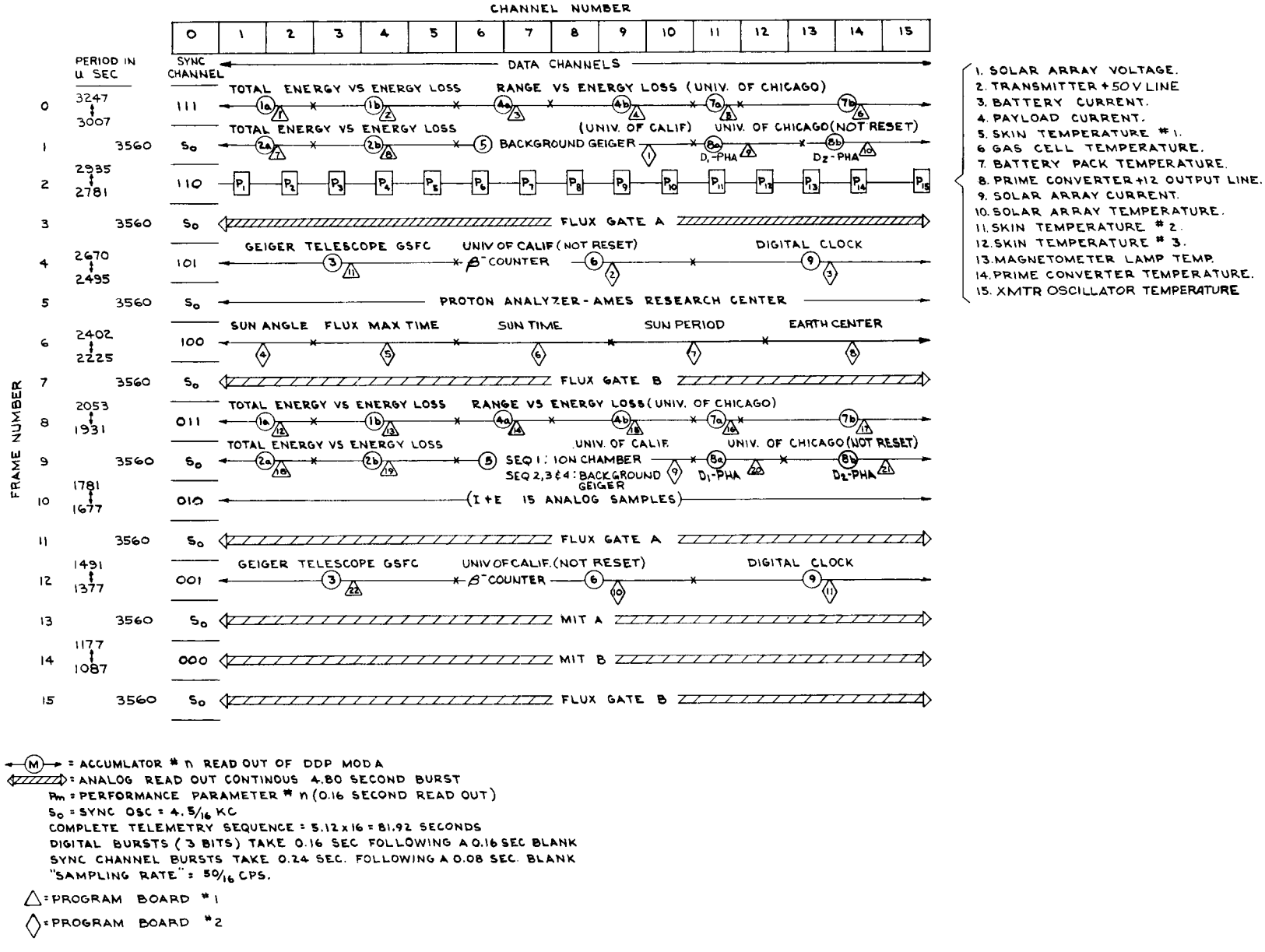


Figure A-1. IMP Telemetry Format

the detector is used to bias-off the amplifier stage of the burst-blank envelope-detector circuit. Physically, the filter/detector/clamp circuit is located in the bit synchronizer unit. The discrete frequency of the fill-in signal developed for any specific format is a function of encoder design parameters and may vary widely (if used at all) in the formats of other telemetry signals. It is necessary only to design a filter tuned to this frequency to make the filter/detector/clamp circuit compatible with the signal being received. The filter and detector circuits involved are described in detail in paragraphs 3.3.14.3, 3.3.14.6, and 3.3.14.8.

A-1.4 SPECIAL LOCKOUT CIRCUITS

The special lockout circuits consist of logic designed to inhibit signal flow between the envelope-detector portion of the integrate-and-dump circuit and the input to the bit-rate filter when selected frames and channels are received. In the IMP satellite telemetry format, for example, the envelope-detector output signal is locked out at the input to the bit-rate filter for all channels, except channel zero, of frames 3, 7, 10, 11, 13, 14, and 15 during sequences 1, 2, and 3, and for all of the fourth sequence. This is done to avoid false excitation of the bit-rate filter which might otherwise result from transmission of continuous data. The signal flow at channel zero time does not trip the threshold detector following the bit-rate filter output, since the signal does not occur frequently enough to cause a signal build-up of significant amplitude in the resonant circuits of the filter. However, this signal at each channel zero time does serve to open the CW lockout gate which couples the output signal of the integrate-and-dump circuit to the recognition mode logic (paragraph 3.3.2.2.a.) so that frame sync recognition pulses from this source to the sync search and lock section are not interrupted. This is accomplished by OR gating the desired outputs from the frame sorter with a channel zero output signal from the channel sorter, a fourth sequence lockout signal from the special box, and a search signal from the sync search and lock section. The output of this OR gate is used to control the NAND gate which couples the envelope-detector output signal to the bit-rate filter, and to the set input of the CW lockout gate flipflop. The search signal from the sync search and lock section of the frame and channel control unit reopens the gate normally controlled by the special lockout circuits and holds it open for as long as the search mode prevails. Initiating the search mode with the manual RESET pushbutton (paragraph 3.3.2.3.g.), therefore, can considerably expedite re-acquisition of the lock mode when the system is adapted to the IMP telemetry format, particularly towards the end of the third sequence or anytime during reception of the fourth sequence. For similar reasons, it is always advisable to press the RESET button when initial acquisition of the lock mode is not accomplished within a few seconds of signal acquisition.

A-1.5 SEQUENCE IDENTIFIER

The IMP telemetry format consists of four sequences of 16 frames each. The first three sequences are repetitive; the fourth sequence is used for the transmission of 16 frames of continuous analog samples. During the fourth sequence the digital-processing section is inhibited, and only the analog-processing section of the data-reduction system remains active to generate analog readouts at the

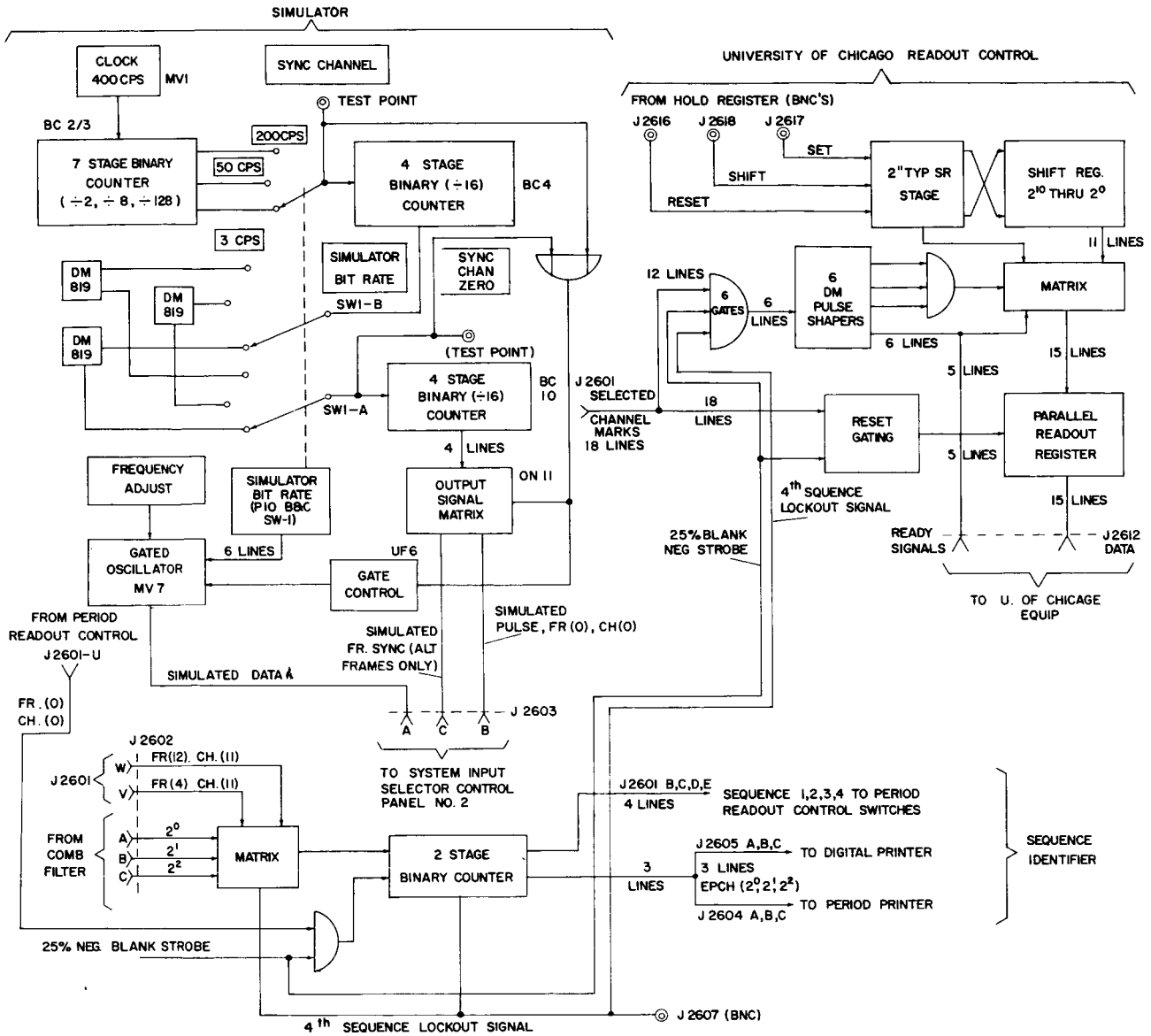


Figure A-2. Special Box, Functional Block Diagram

flywheel rate. The sequence identifier located in the special box (figure A-2 and figure 6-14, sheet 1, Volume II) generates the required fourth-sequence lockout signal. It also supplies binary information to the sequence identification wheel of the period printer and the digital printer, in addition to providing sequence marker signals (one on each of four lines) to PERIOD READOUT CONTROL SEQUENCE switches for readout selection purposes. The sequence identifier consists of a matrix of NAND gates and a two-stage binary counter. The NAND gating configuration is arranged so that it converts the binary output of the digital comb filter into the proper signals at the proper times to appropriately update the counter in step with the telemetry signal sequence. Sequence-identification information is transmitted by the satellite during the channel 11 burst period of frames 4 and 12; consequently, frame 4, channel 11 and frame 12, channel 11 marker pulses selected from

the frame and channel matrix output are used to gate the converted comb filter signals to the proper set and reset inputs of the counter. For example, when the output of the digital comb filter is either a binary one or a binary five (both of which are indicative of the third sequence), the matrix output signal is gated to the set inputs of both counter stages, forcing the output of the counter to a binary three, if it is not already in step with the incoming signal. The counter is stepped at the beginning of each sequence by the frame zero, channel zero marker. The fourth sequence lockout signal, binary data for the period and digital printers, and marker signals for the PERIOD READ-OUT CONTROL SEQUENCE switches are obtained from the gated output signals of the counter. The fourth-sequence lockout signal is fed back to inhibit the gates which couple the converted comb-filter output signals to the sequence counter set and reset inputs, since dependable sequence-identification information from the telemeter is not available during the fourth sequence.

A-1.6 UNIVERSITY OF CHICAGO READOUT CONTROL

The 15-bit parallel readout of pure binary data required for the University of Chicago experiment is provided for by the University of Chicago readout control circuits, located in the special box (figure A-2 and figure 6-14, sheet 2, Volume II). These circuits consist of a 12-stage shift register which is coupled to a 15-bit hold register having parallel readout capabilities, and circuits to signal the experimenter when data is ready for readout, and to reset the hold register after each readout is accomplished. Matrix control and ready signal pulses are developed by delay multivibrators and inverter amplifiers which are driven by selected timing pulses from the frame and channel matrix. These pulses are coupled to the inputs of the multivibrators by NAND gates which are inhibited when the fourth-sequence lockout signal occurs. Selected timing pulses to reset the hold register are processed by an inverter amplifier to which they are coupled through NOR gates. The possibility of falsely exciting the delay multivibrators and inverter amplifiers as a result of unwanted gating transients is minimized by the use of the 25-percent blank negative strobe pulse from the bit synchronizer as the final enabling signal to each of the input signal coupling gates.

A-1.6.1 PERFORMANCE CHARACTERISTICS

An examination of figure A-1 reveals that the University of Chicago experiment results in the transmission of three 15-bit words during each of the first three sequences. Each word is processed in two parts (4a and 4b, 7a and 7b, 8a and 8b) and reappears in updated form a second time during each of these sequences, first in frame zero or frame one, and again in frame eight or frame nine. Since the objective is to accomplish a 15-bit parallel readout of the complete word in each case, both parts of each word are separately loaded into the shift register and transferred to their respective positions in the hold register. A ready signal pulse is then generated for each word, and the hold register is cleared after each parallel readout of a complete word takes place. The readout command pulse is generated by the University of Chicago unit in response to the ready signal pulse.

A-1.6.2 TIMING CONSIDERATIONS

When the digital-processing section of the data-reduction system is operating, digital information is transferred from the comb filter to the memory unit and strobed into the hold register at the rate of three bits per channel. When a predetermined amount of information has been stored in the hold register, the bits of that information are shifted into the bcd converter during the blank period of the next channel time. At the same time, this information is serially transferred to the University of Chicago readout-control shift register (the least significant bit of the information present being the last bit to enter the register in each case). During the blank period of the following channel time, the parallel transfer of this information, from the shift register to the hold register of the University of Chicago readout-control circuits, takes place. One of the two parts of a 15-bit digital word is stored in the appropriate stages of the hold register when this transfer function is accomplished. The entire process is then repeated to store the second part of that word in the hold register. A reset pulse is generated to clear the hold register, in preparation for storage of the two parts of the next 15-bit word, when sufficient time has elapsed to permit the parallel transfer of the present word to the University of Chicago unit. The necessary timing to control these functions is provided by the selected timing marks which are coupled to the readout-control circuits by 18 lines from connector J2601. Each line carries a marker signal which is coincident with one of the following times: F(0) C(9) (frame zero, channel 9), F(0) C(11), F(0) C(12), F(0) C(13), F(1) C(1), F(1) C(2), F(1) C(14), F(2) C(2), F(8) C(11), F(8) C(12), F(8) C(13), F(9) C(1), F(9) C(2), F(9) C(14), F(10) C(1), and F(10) C(2). The sequence of operation of the readout-control circuits is described in the following paragraph as an example of the functional application of these timing marks.

A-1.6.3 SEQUENCE OF OPERATION

Channels 6 through 15 of frames zero and eight, and channels 11 through 15 of frames one and nine are used to transmit the three words associated with the University of Chicago experiment. Each of these words contains 15 information bits and is processed in two parts. This is explained in paragraph A-1.6.1 and shown graphically in figure A-1. Unless otherwise indicated in the following discussion, all of the channels referred to are a part of frame zero. Word 4a occurs in channels 6 and 7 and consequently consists of six information bits (three per channel) which are transferred to the University of Chicago readout-control shift register at the beginning of channel 8. This information is then gated through the matrix to the appropriate stages of the parallel readout hold register by a transfer pulse which is generated when the 25-percent blank negative strobe coincides in time with the F(0) C(9) marker signal. At the same time, 6 of the 9 information bits of word 4b (from channels 8 and 9) are being stored in the memory unit of the data-reduction system circuits. The remaining 3 bits of this word (from channel 10) are similarly stored, and all 9 bits are then transferred to the data-reduction system hold register during the burst period of channel 10. At the beginning of channel 11, the 6 bits of word 4a are shifted out of the University of Chicago readout-control shift register and replaced by the 9 bits of word 4b in time to be gated through the matrix to the appropriate unoccupied stages of the readout-control hold register when the 25-percent blank

strobe coincides with the F(0) C(11) marker signal. This transfer pulse generated at this time also serves as the ready signal which initiates a readout command pulse from the University of Chicago unit. The 15-bit word (4a + 4b) is then read out of the hold register and the register is cleared by the reset pulse generated when the 25-percent blank negative strobe coincides with the F(0) C(12) marker signal. Meanwhile, the 3 information bits of word 7a (from C(11)) have replaced the 9 bits of word 4b in the shift register and are ready to be transferred to the appropriate stages of the hold register while the F(0) C(13) marker signal is present. The 3 bits of word 7a are replaced in the shift register at the start of F(1) C(0) by the 12 bits of word 7b (from channels 12 through 15), which are gated through the matrix and transferred to the appropriate unoccupied stages of the hold register while the F(1) C(1) marker signal is present. The transfer pulse generated at this time also provides a ready signal to the University of Chicago unit. Consequently, the 15-bit word (7a + 7b) is read out and the hold register is cleared by the reset pulse generated while the F(1) C(2) marker signal is present. The third word (8a + 8b, from frame one, channels 11 through 15) is processed in the same manner as the first word (4a + 4b), except that the timing is governed by marker signals F(1) C(14), F(2) C(1), and F(2) C(2). The entire function for all three words is repeated when the words reappear in the format of frames 8 and 9, the timing then being governed by the remainder of the marker signals listed in paragraph A-1.6.2. For each of the first three sequences, the entire process described in this paragraph is repeated. During the fourth transmission sequence, clear pulses may be generated at the reset gating network; however, the remainder of the input-timing gates are inhibited by the fourth sequence lockout signal so that the transfer pulses, which would otherwise drive the gating matrix and provide ready signals, cannot occur.

A-1.7 SIMULATOR

A frequency-regulated square-wave signal which simulates the clock rate of the IMP telemetry-signal data train is generated by the simulator circuits located in the special box. These circuits also generate alternate frame-sync markers and sequence-marker pulses which are compatible with the format of the IMP telemeter. Collectively, the signals from the simulator may be used to conduct pre-mission operational tests and to troubleshoot the data-reduction system at normal or accelerated bit rates when the equipment has been programmed to process signals from the IMP satellite. A functional block diagram and a logic diagram of the simulator circuits are shown in figure A-1, and figure 6-14, sheet 3, of Volume II, respectively.

A-1.7.1 DATA TRAIN

The simulated data train is contained in the output pulses of a gated oscillator, the duty cycle of which simulates the burst-blank envelope of the normal telemetry signal, and the frequency of which simulates the satellite subcarrier oscillator frequency modulation normally present during a channel burst period. A pulse repetition frequency corresponding to the normal IMP telemetry bit rate, or to one of two accelerated bit rates (3.125, 50, or 200 cps, respectively), is selectable

from the gated oscillator as a function of the SIMULATOR BIT RATE switch position. This switch also regulates the control range of the gated oscillator FREQUENCY ADJUST potentiometer to maintain an oscillator signal frequency which is compatible with the bit rate selected. The gating signal which controls the oscillator pulse repetition frequency is derived from the clock signal generated by a 400-cps astable multivibrator in the following manner. The clock signal is coupled to the input of a seven-stage binary counter. The set output from the 2^0, 2^2, or 2^6 stage of this counter is selected by the SIMULATOR BIT RATE switch position and coupled to a flipflop which controls the oscillator gate. The result is a selectable pulse repetition frequency with a 50-percent duty cycle which simulates the symmetrical burst-blank envelope of the normal telemetry signal. To simulate the asymmetrical envelope of the wide-burst frame-sync recognition pattern, the duty cycle of the gated oscillator is increased to 75-percent for the duration of every 16th pulse by modifying the length of the gating signal. The fundamental gating signal from the SIMULATOR BIT RATE switch is consequently coupled in parallel to one input (the SYNC CHANNEL test point) of a two-input OR gate and to the input of a four-stage binary counter which performs a divide-by-16 function. The output signal from this counter is coupled through a multivibrator delay circuit to the second input (the SYNC CHAN ZERO test point) of the OR gate, and the output signal from the OR gate is the gating signal to the flipflop which controls the oscillator gate. The delay time introduced by the multivibrator circuit causes the duration of every 16th gating signal from the OR gate to be half again that of the fundamental gating signal. Three multivibrator coupling circuits with discrete preset time delays are provided, and the correct circuit is selected automatically through the SIMULATOR BIT RATE switch. The flipflop used to control the oscillator gate is synchronized with the output signal of the gated oscillator to avoid pulse splitting. The FREQUENCY ADJUST control may be set to simulate any desired frequency from the subcarrier oscillator of the IMP telemeter. When an accelerated bit rate is selected, this frequency is increased proportionately, making it possible to test the performance of the control and timing circuits in a small fraction of the time required to process the real-time signal.

A-1.7.2 MARKER PULSES

Simulated frame-sync and sequence marker pulses are generated in an output-signal matrix of NAND gates by combining the SYNC CHANNEL test-point signal with the SYNC CHAN ZERO test-point signal, and gating the resultant marker-pulse signal with the output signals from a four-stage binary counter. The SYNC CHAN ZERO test-point signal is coupled to the input of the counter, and the set output of the 2^0 counter stage is NAND gated with the marker pulse signal to generate a simulated frame-sync marker pulse which occurs for alternate frames only, at an output of the matrix. Signals from the reset outputs of all four stages of the counter are also NAND gated with the marker-pulse signal to generate the simulated F(0) C(0) sequence marker pulse which occurs for each frame zero, channel zero time at a second output of the matrix. The simulated frame-sync marker pulse takes the place of the frame-sync recognition signal normally developed by the digital comb filter of the data-reduction system (paragraph 3.3.2.2.b.) from the real-time IMP telemetry signal, making it unnecessary for the simulator to develop a sync oscillator frequency signal as part of the simulated data train. The simulated F(0) C(0) sequence marker pulse is used to reset

the frame sorter at the end of each 16-frame sequence, when the SYSTEM INPUT SELECTOR switch is in the SIMULATE position. This assures synchronization of the frame sorter with the simulated data train and eliminates the necessity of developing octally coded frame identification signals as part of the data train (paragraph 3.3.2.6); consequently, the frame-corrector matrix is inhibited when the SIMULATE mode is selected.