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Volume 2 of

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OPERATION AND MAINTENANCE MANUAL FOR UNIVERSAL PFM REAL-TIME DATA-REDUCTION SYSTEM

MAY 1964

GODDARD SPACE FLIGHT CENTER
GREENBELT, MD.

Volume 2 of 2

OPERATION AND MAINTENANCE MANUAL FOR UNIVERSAL PFM REAL-TIME DATA-REDUCTION SYSTEM

Data Instrumentation Development Branch
Data System Division

Goddard Space Flight Center
Greenbelt, Maryland

LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGED PAGES. DESTROY SUPERSEDED PAGES

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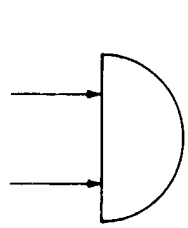

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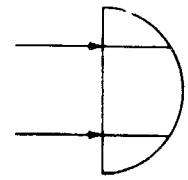

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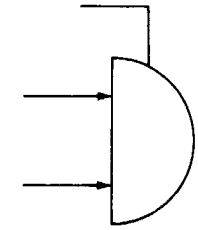

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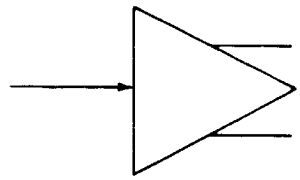

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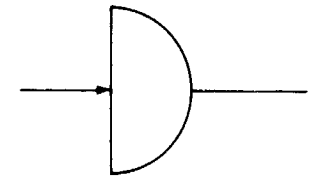

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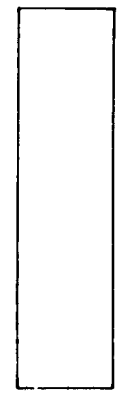


FLIPFLOP (FF)
BINARY COUNTER STAGE (BC)
SHIFT REGISTER STAGE (SR)
SCHMITT TRIGGER (ST)
MULTIVIBRATOR (MV)
DELAY MULTIVIBRATOR (DM) OR
ADJUSTABLE DELAY MULTIVIBRATOR (DMA)
SPECIAL CIRCUIT (SC)

Figure 6-1—Logic Symbols

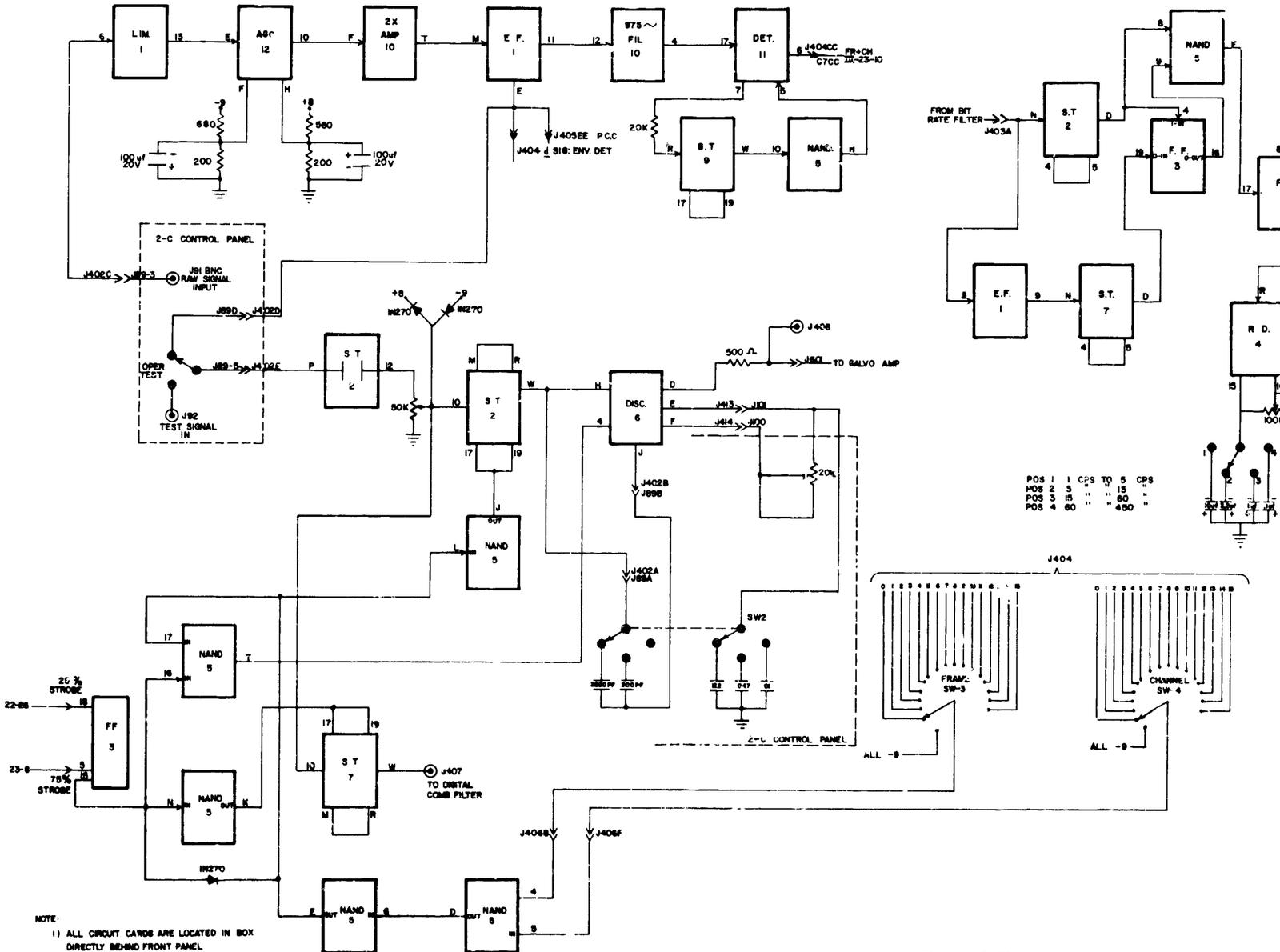
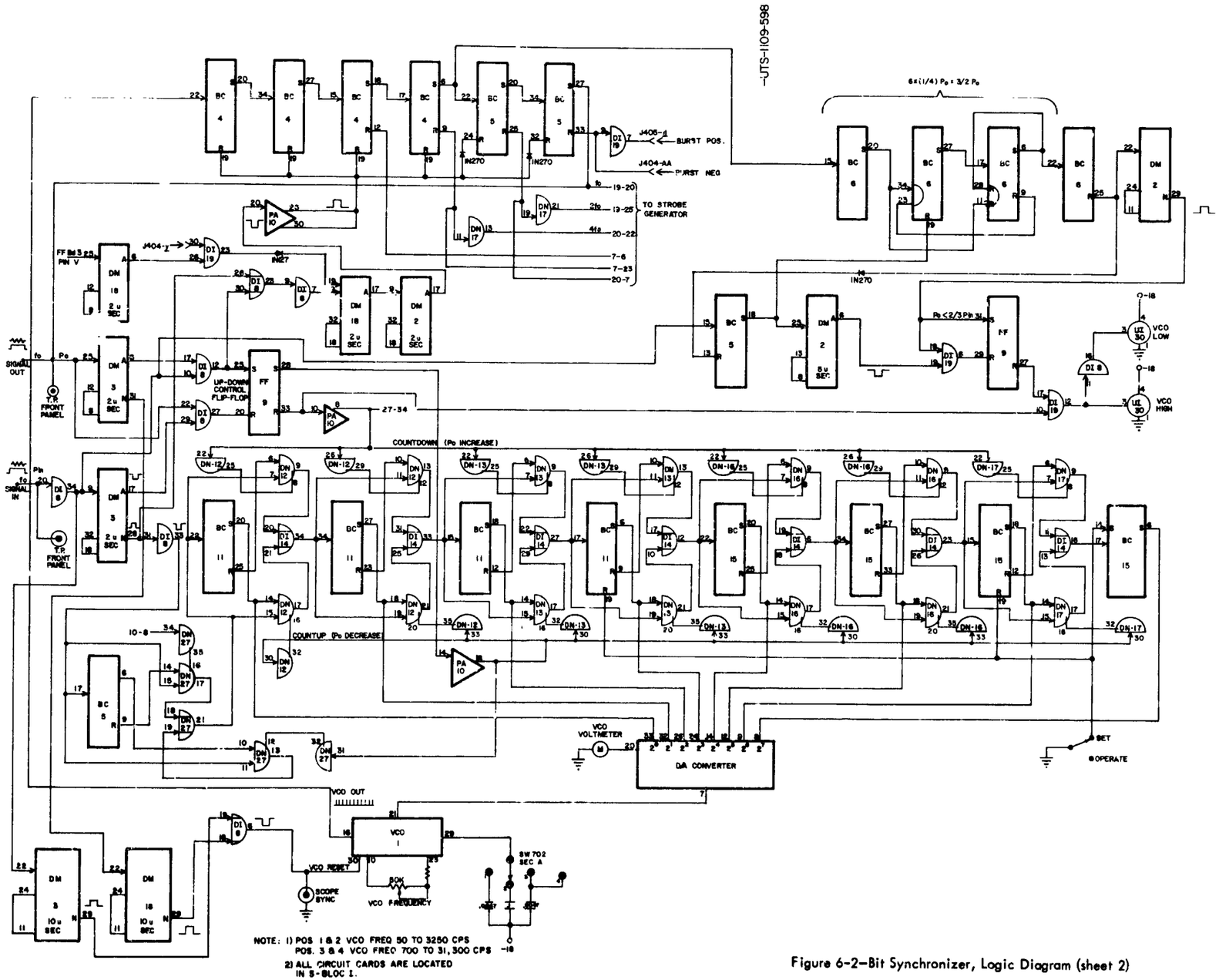


Figure 6-2–Bit Synchronizer, Logic Diagram (sheet 1)



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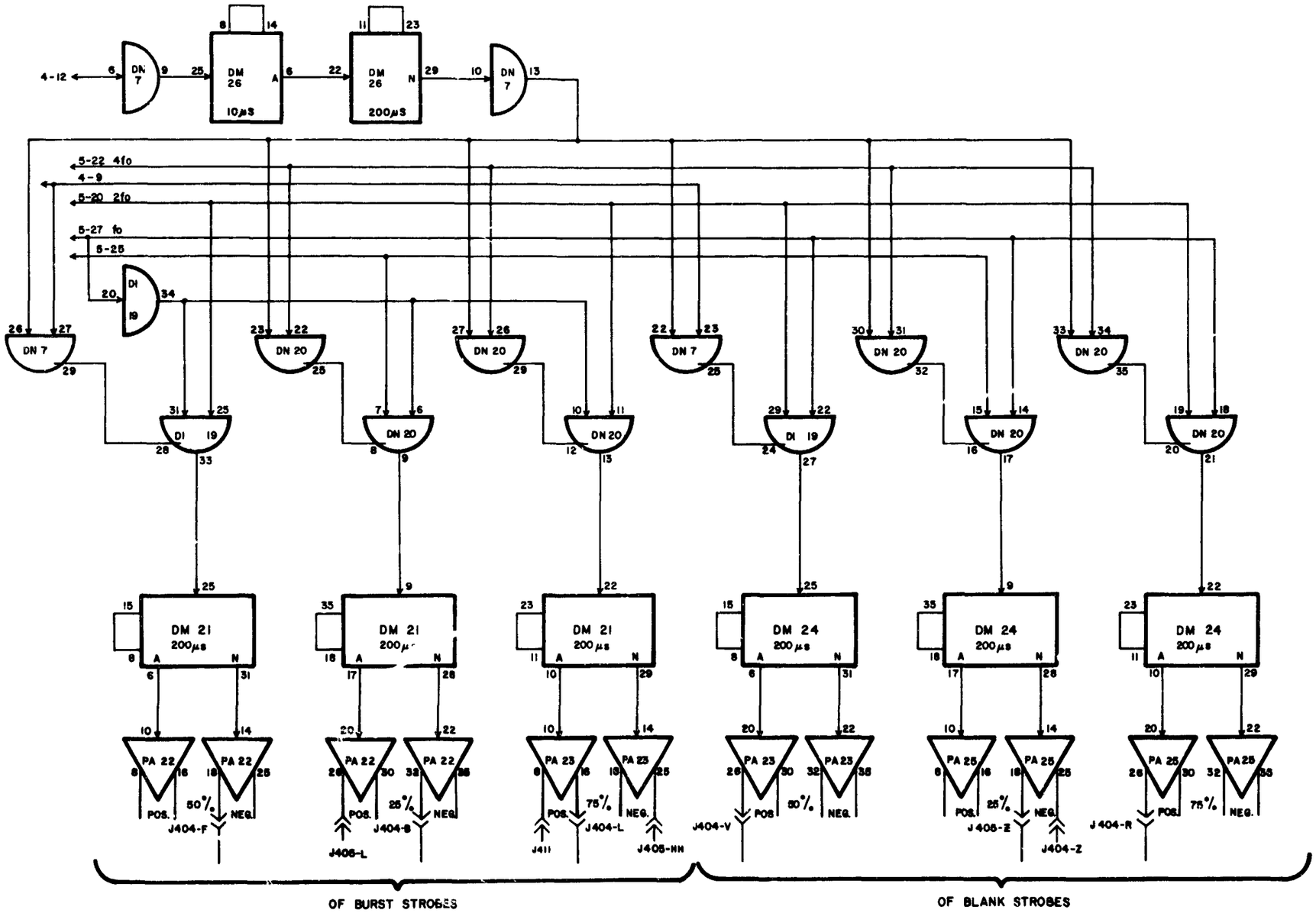


NOTE
1) ALL CIRCUIT CARDS ARE LOCATED IN S-BLOC I.

Figure 6-2—Bit Synchronizer, Logic Diagram (sheet 3)

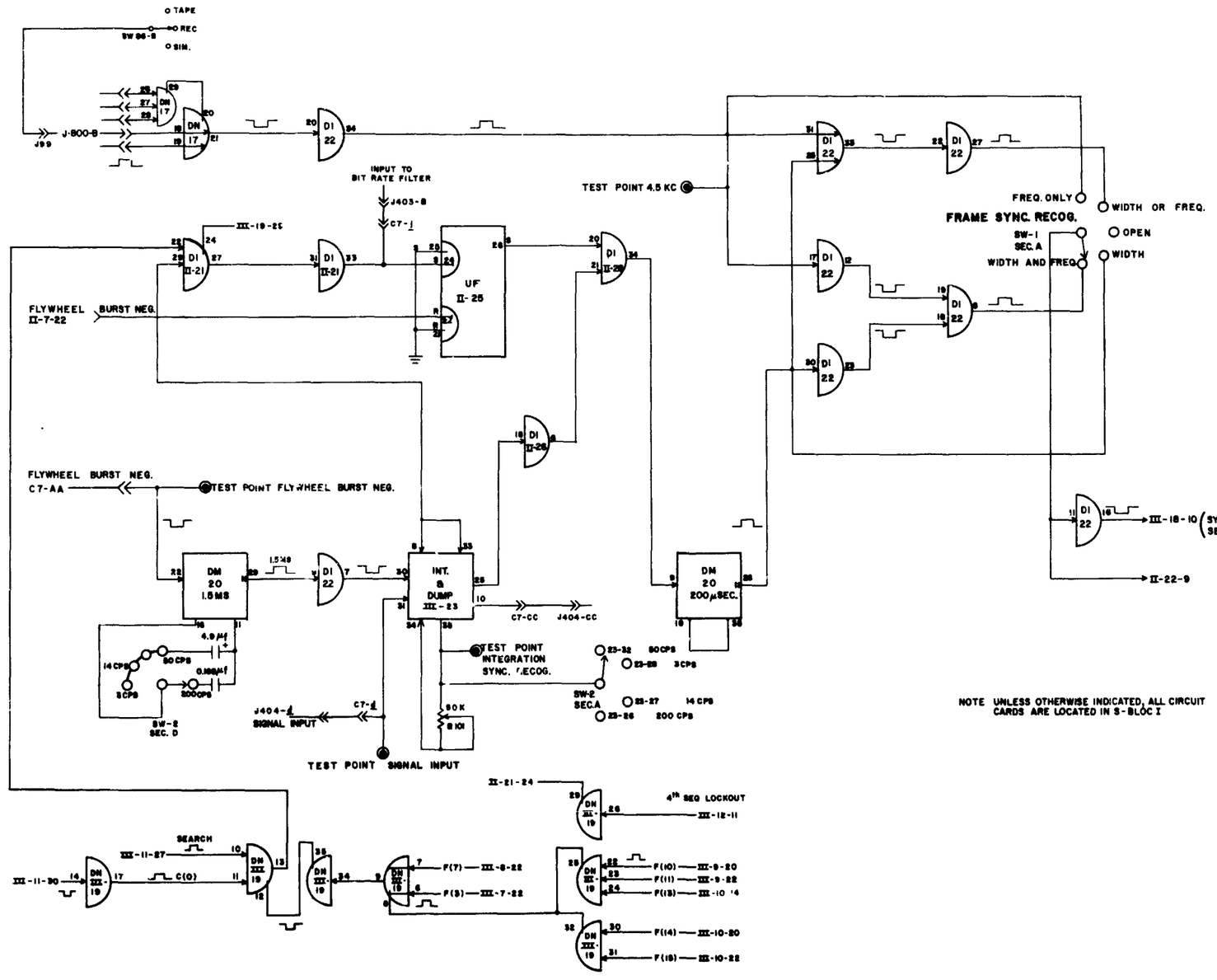


Figure 6-3–Frame and Channel Control, Logic Diagram (sheet 1)

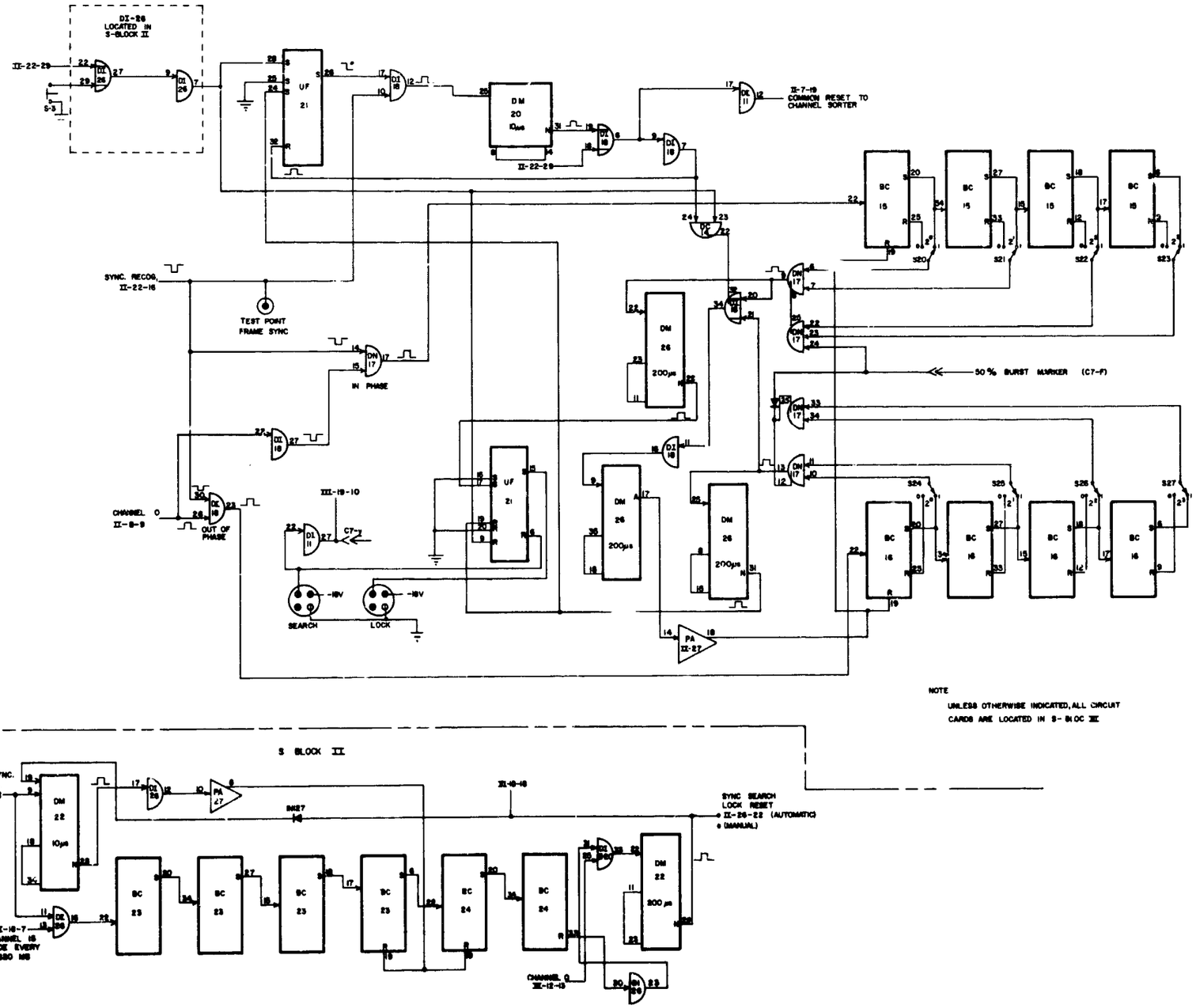


Figure 6-3–Frame and Channel Control, Logic Diagram (sheet 2)

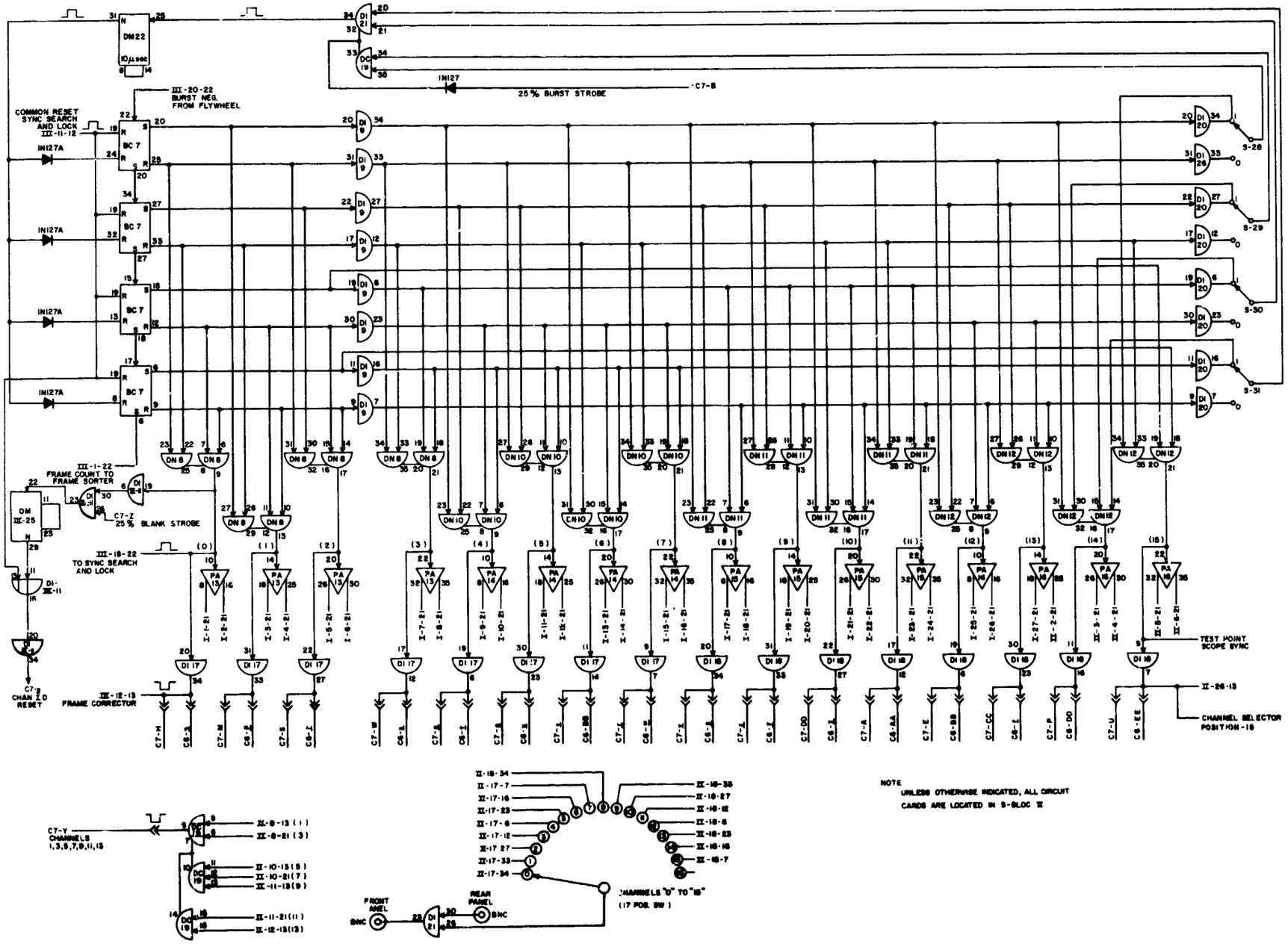


Figure 6-3—Frame and Channel Control, Logic Diagram (sheet 3)

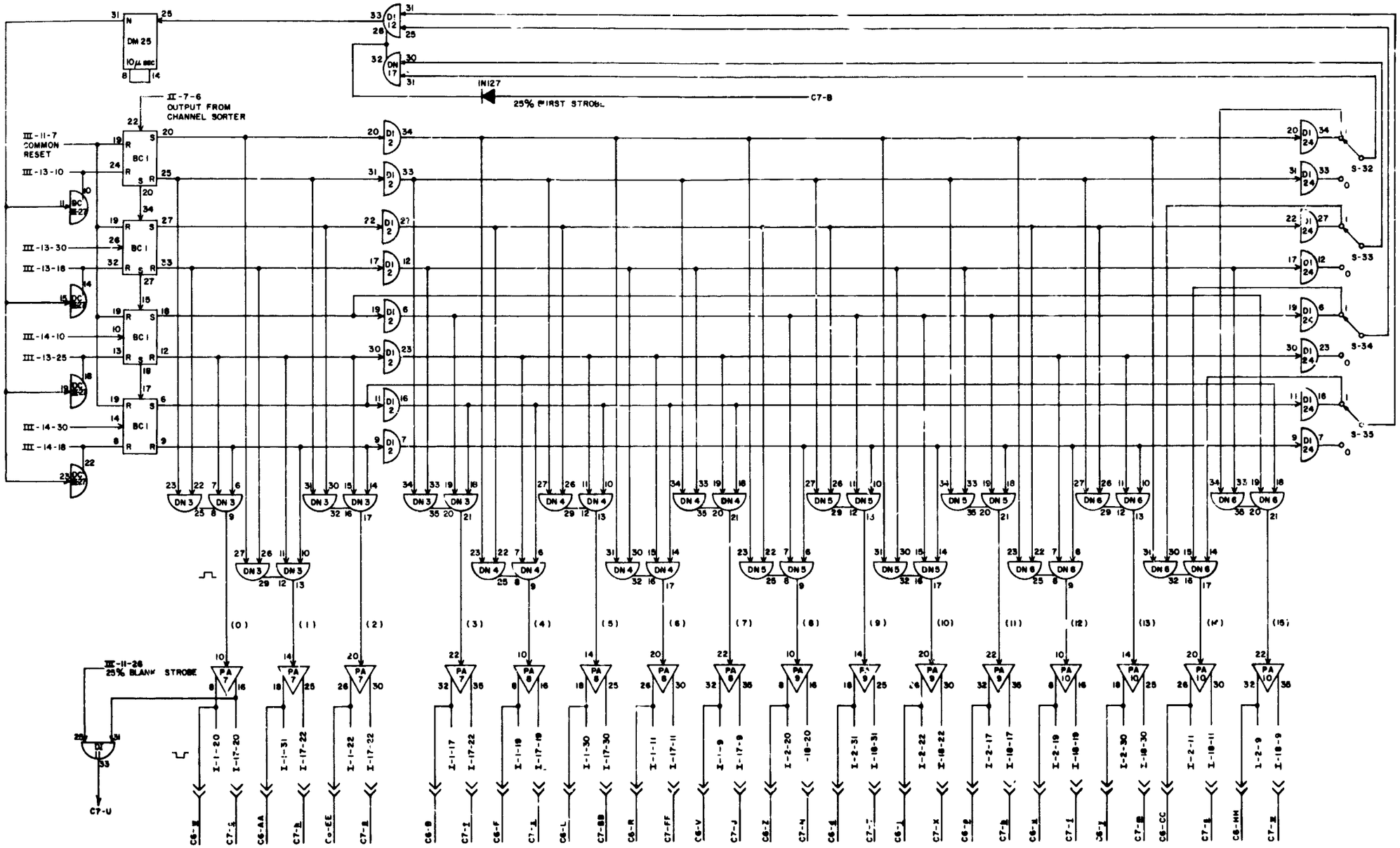


Figure 6-3—Frame and Channel Control, Logic Diagram (sheet 4)

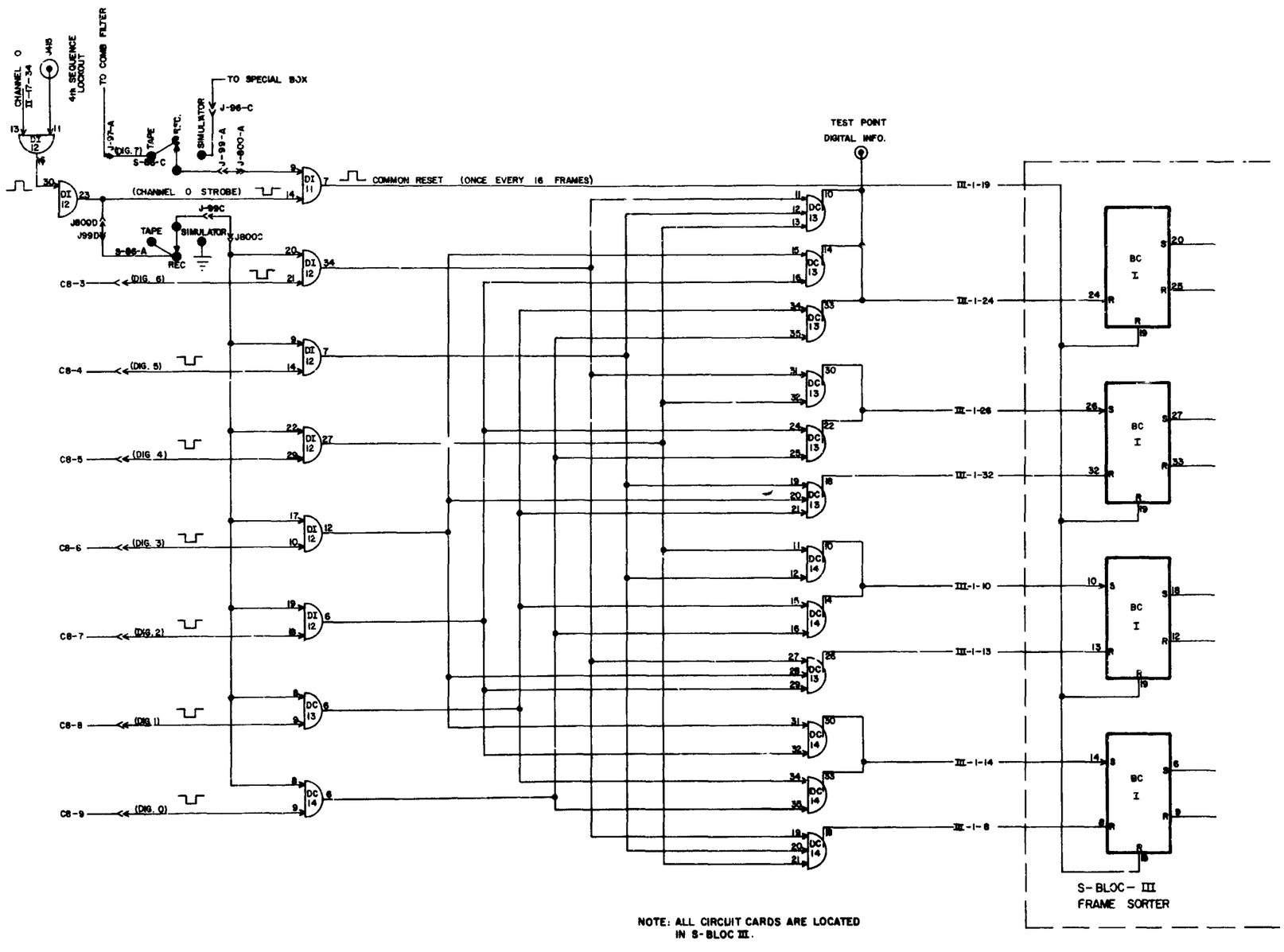


Figure 6-3—Frame and Channel Control, Logic Diagram (sheet 5)

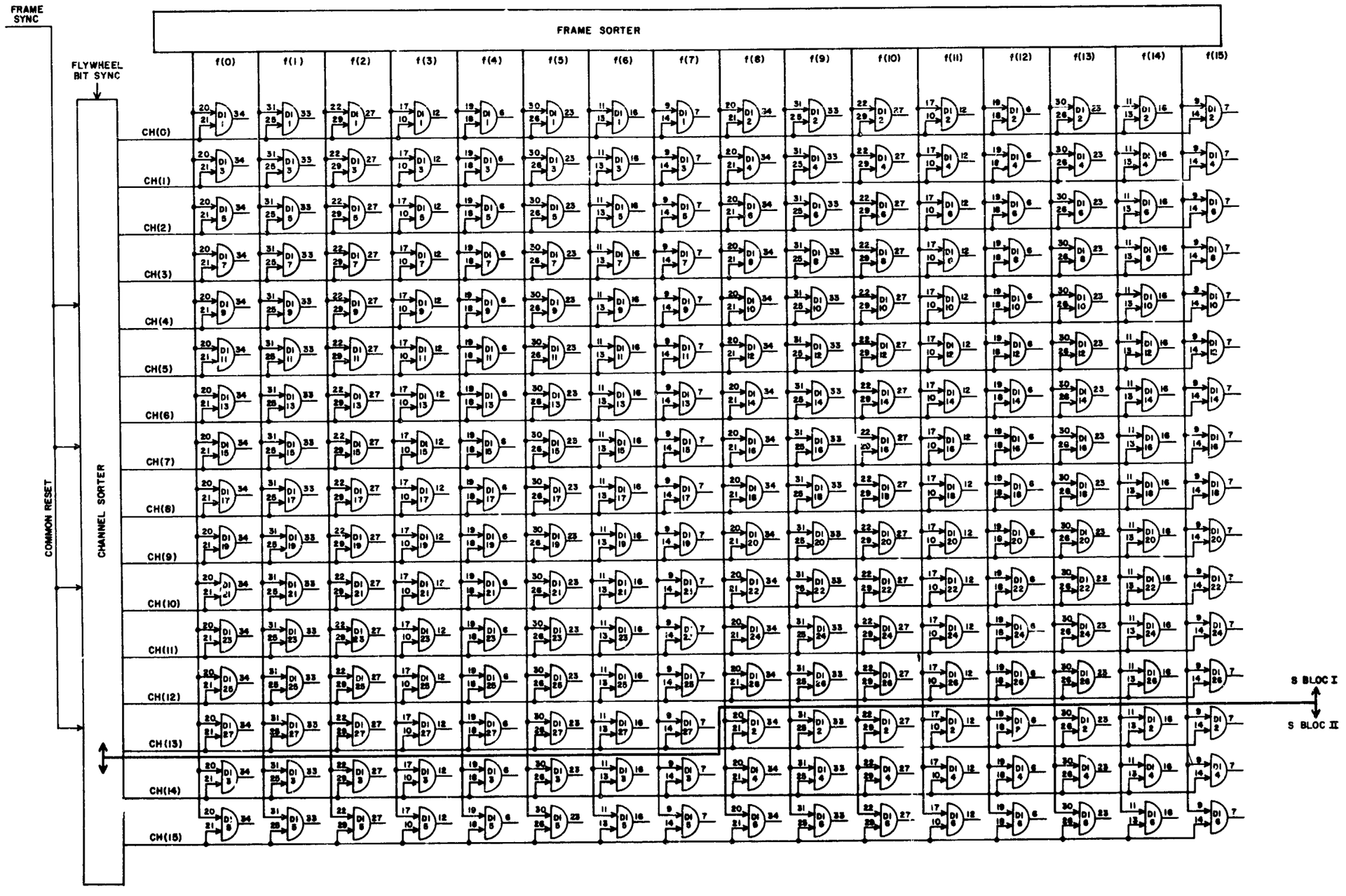
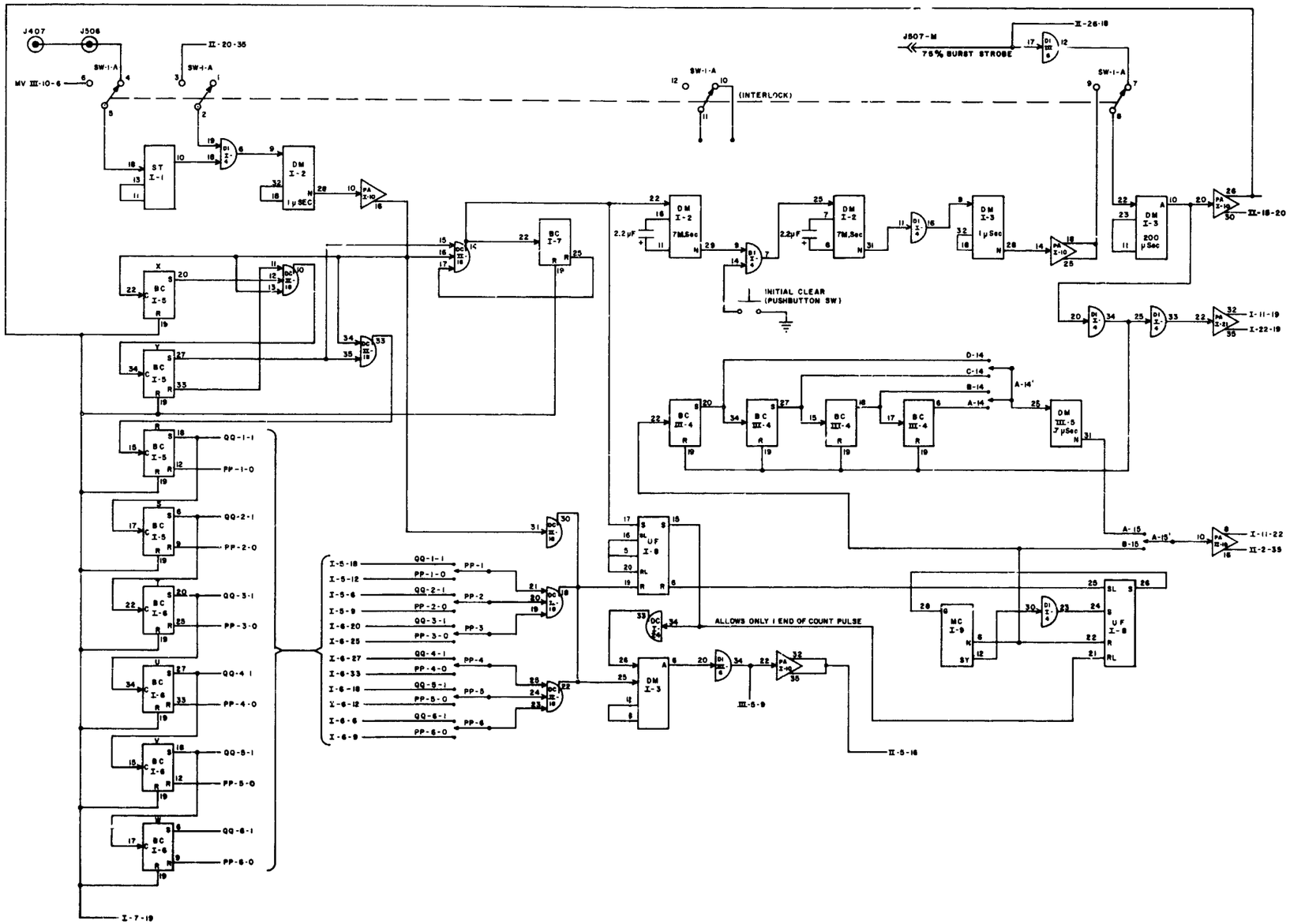


Figure 6-3–Frame and Channel Control, Logic Diagram (sheet 6)



NOTE: ALL SWITCHES SHOWN IN OPERATE POSITION

Figure 6-4—Digital Comb Filter, Logic Diagram (sheet 1)

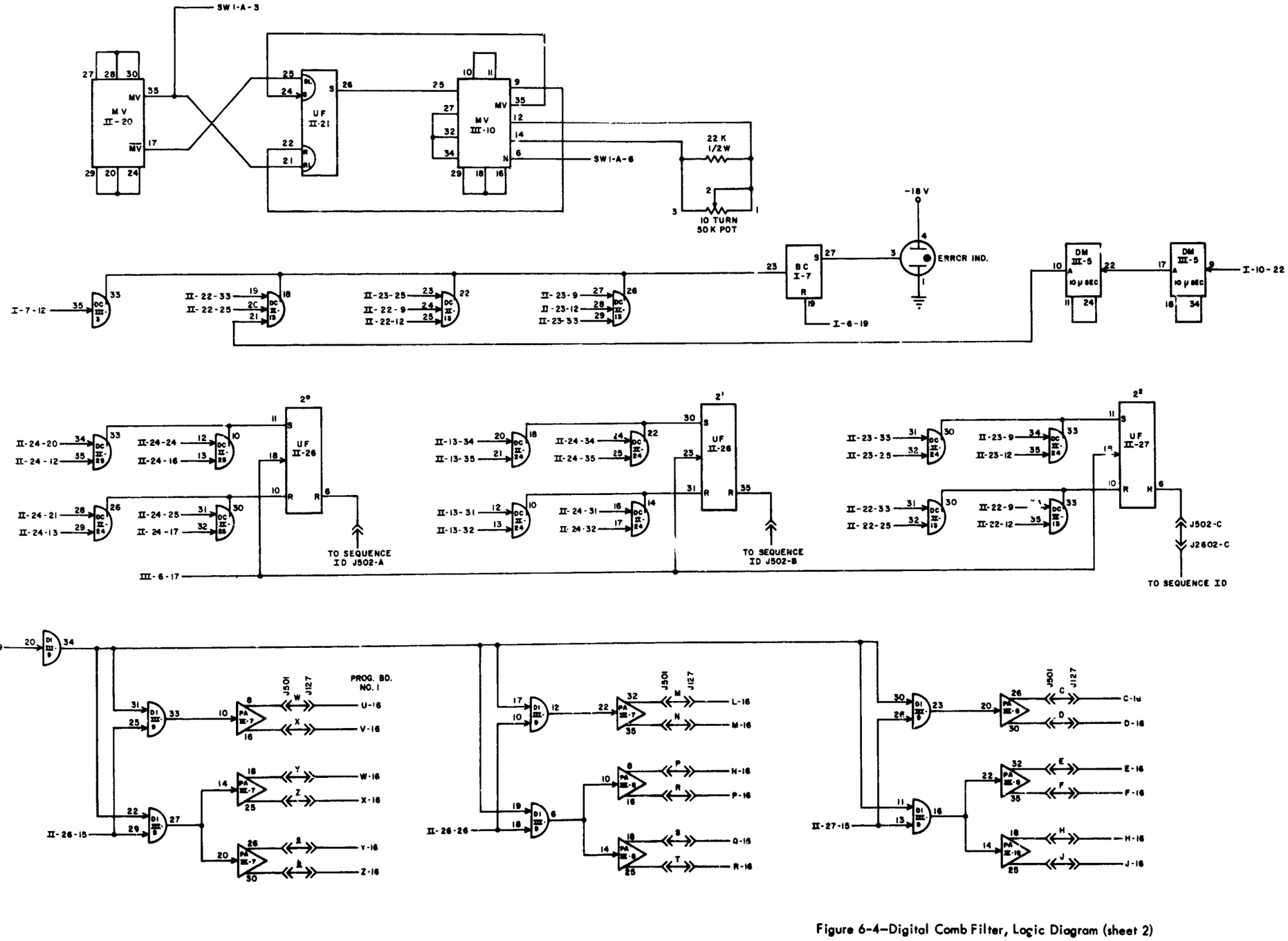


Figure 6-4—Digital Comb Filter, Logic Diagram (sheet 2)

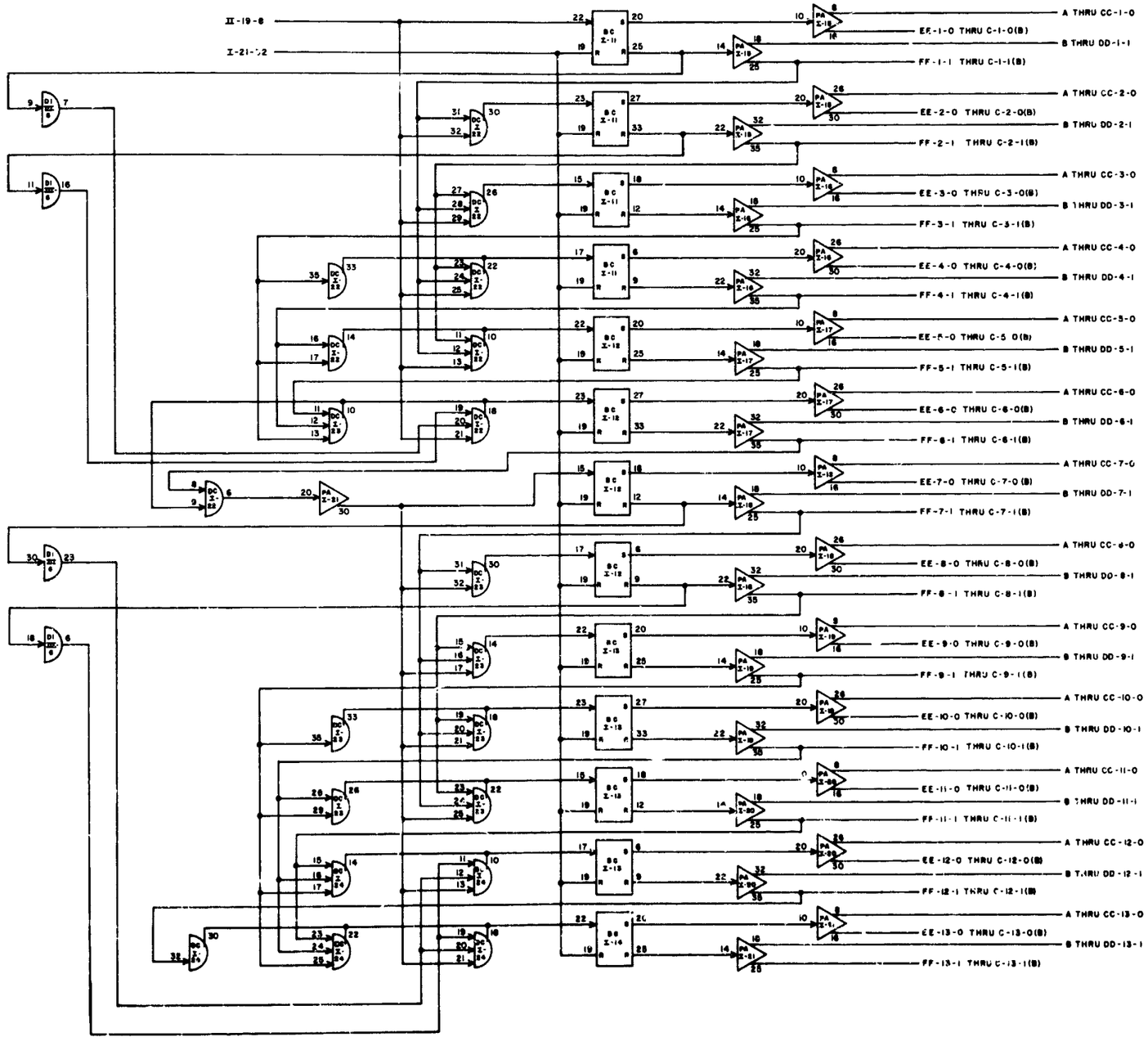


Figure 6-4–Digital Comb Filter, Logic Diagram (sheet 3)

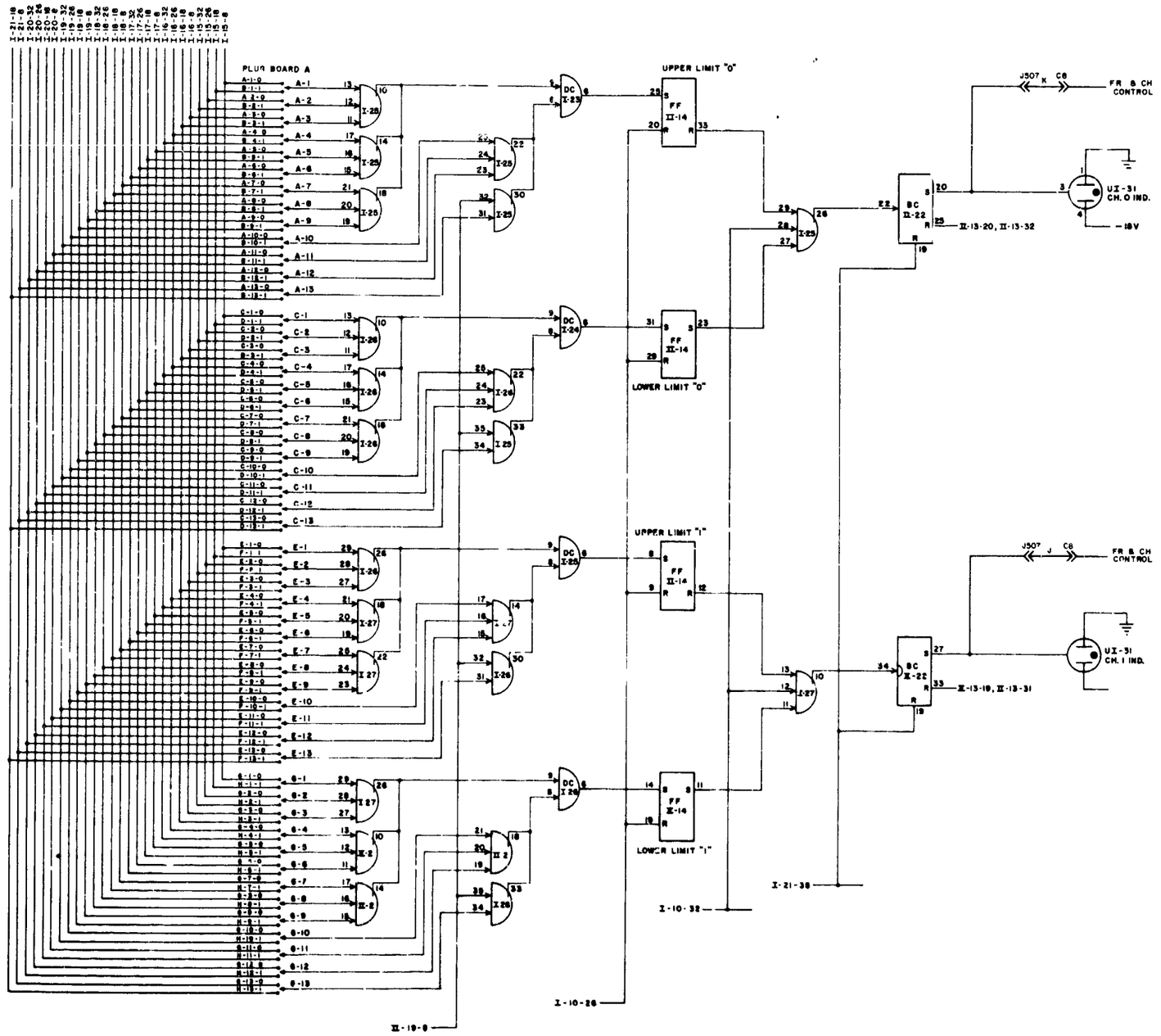


Figure 6-4-Digital Comb Filter, Logic Diagram (sheet 4)

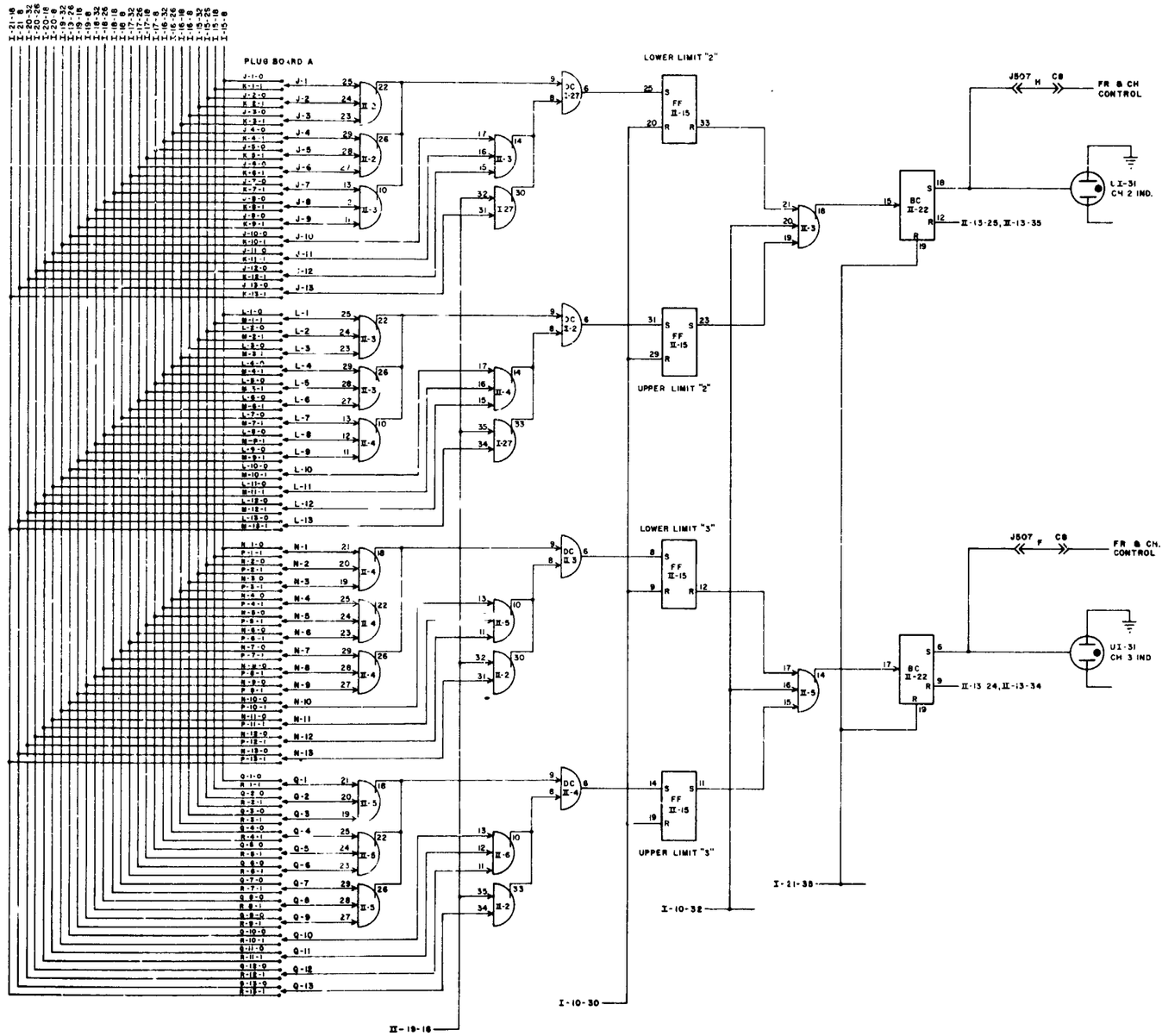


Figure 6-4—Digital Comb Filter, Logic Diagram (sheet 5)

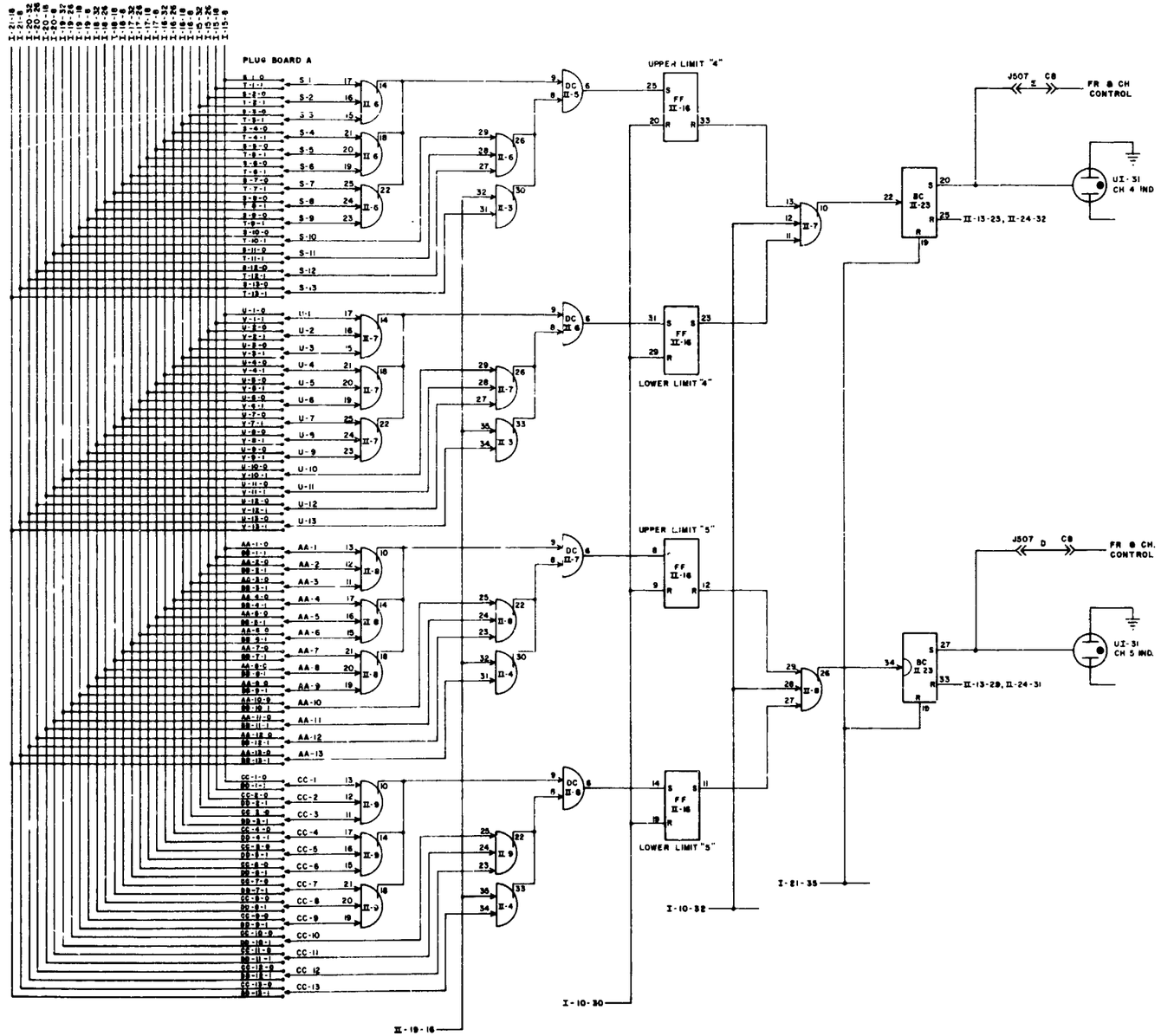


Figure 6-4—Digital Comb Filter, Logic Diagram (sheet 6)

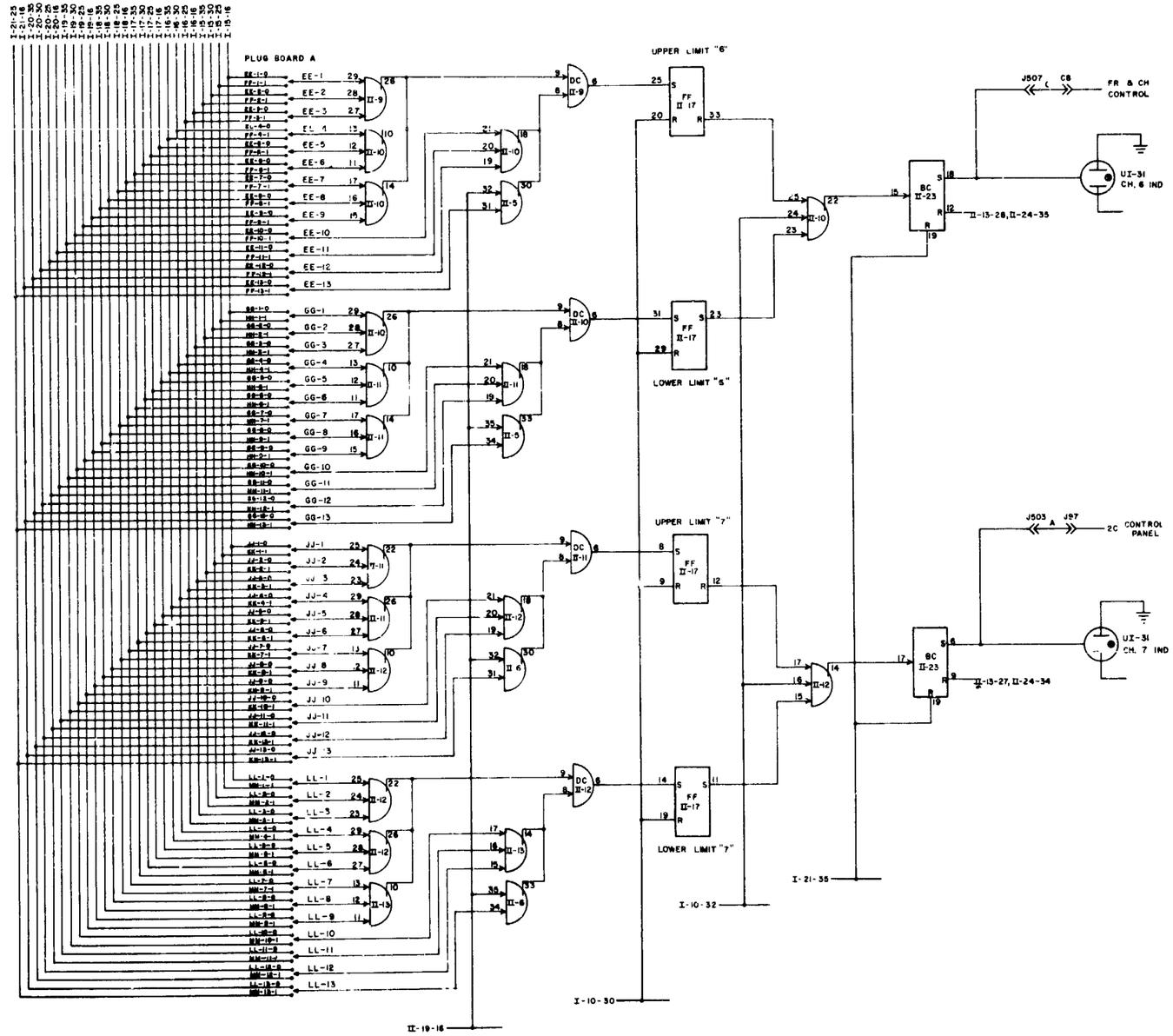
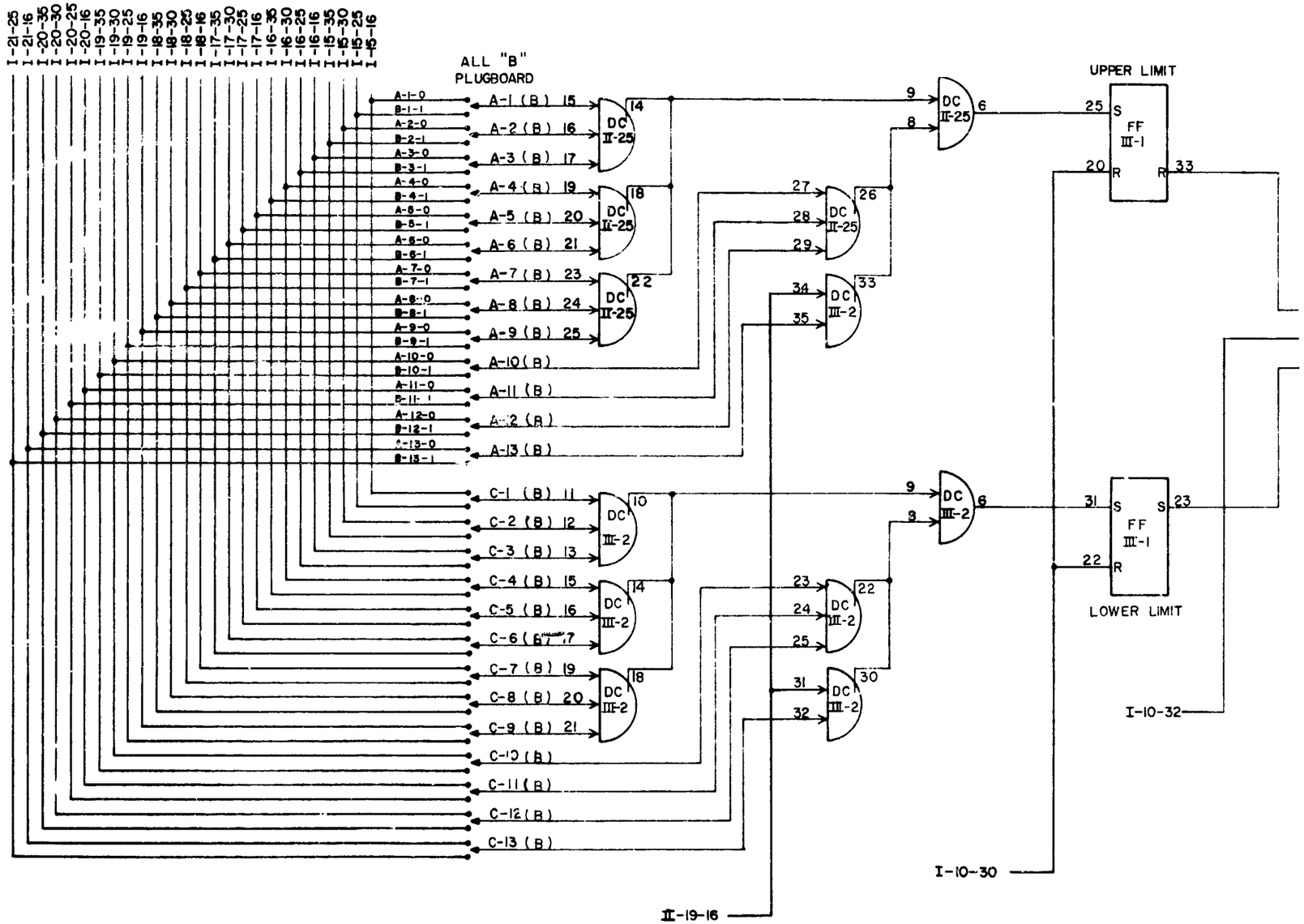


Figure 6-4—Digital Comb Filter, Logic Diagram (sheet 7)


I-21-25
I-21-16
I-20-35
I-20-30
I-20-25
I-20-16
I-19-35
I-19-30
I-19-25
I-19-16
I-18-35
I-18-30
I-18-25
I-18-16
I-17-35
I-17-30
I-17-25
I-17-16
I-16-35
I-16-30
I-16-25
I-16-16
I-15-35
I-15-30
I-15-25
I-15-16
ALL "B" PLUGBOARD
A-1-0
B-1-1
A-2-0
B-2-1
A-3-0
B-3-1
A-4-0
B-4-1
A-5-0
B-5-1
A-6-0
B-6-1
A-7-0
B-7-1
A-8-0
B-8-1
A-9-0
B-9-1
A-10-0
B-10-1
A-11-0
B-11-1
A-12-0
B-12-1
A-13-0
B-13-1
A-1 (B) 15
A-2 (B) 16
A-3 (B) 17
A-4 (B) 19
A-5 (B) 20
A-6 (B) 21
A-7 (B) 23
A-8 (B) 24
A-9 (B) 25
A-10 (B)
A-11 (B)
A-12 (B)
A-13 (B)
C-1 (B) 11
C-2 (B) 12
C-3 (B) 13
C-4 (B) 15
C-5 (B) 16
C-6 (B) 17
C-7 (B) 19
C-8 (B) 20
C-9 (B) 21
C-10 (B)
C-11 (B)
C-12 (B)
C-13 (B)
DC II-25
DC III-2
DC III-1
FF III-1
UPPER LIMIT
LOWER LIMIT
I-10-32
I-10-30
II-19-16

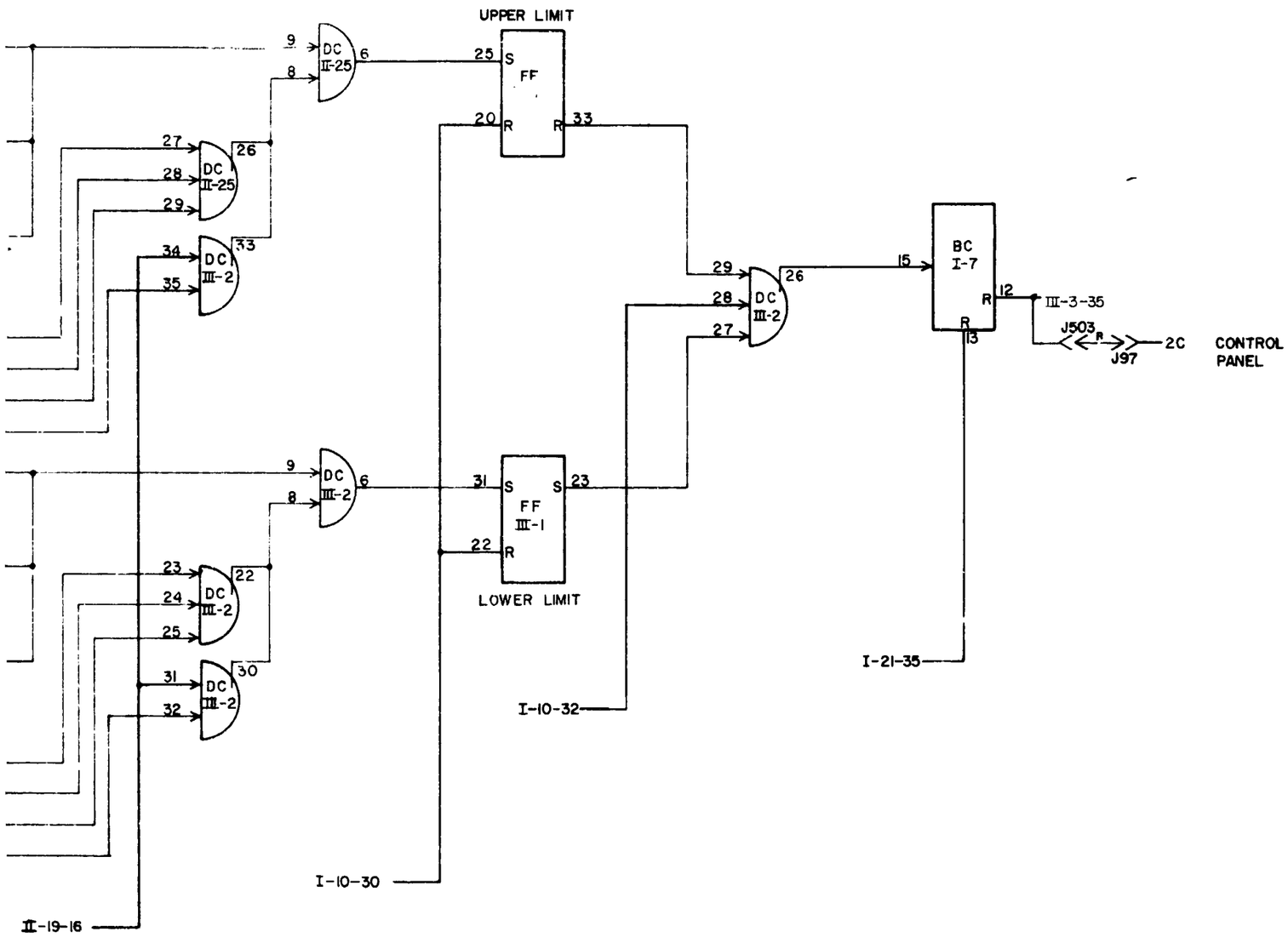


Figure 6-4—Digital Comb Filter, Logic Diagram (sheet 9)

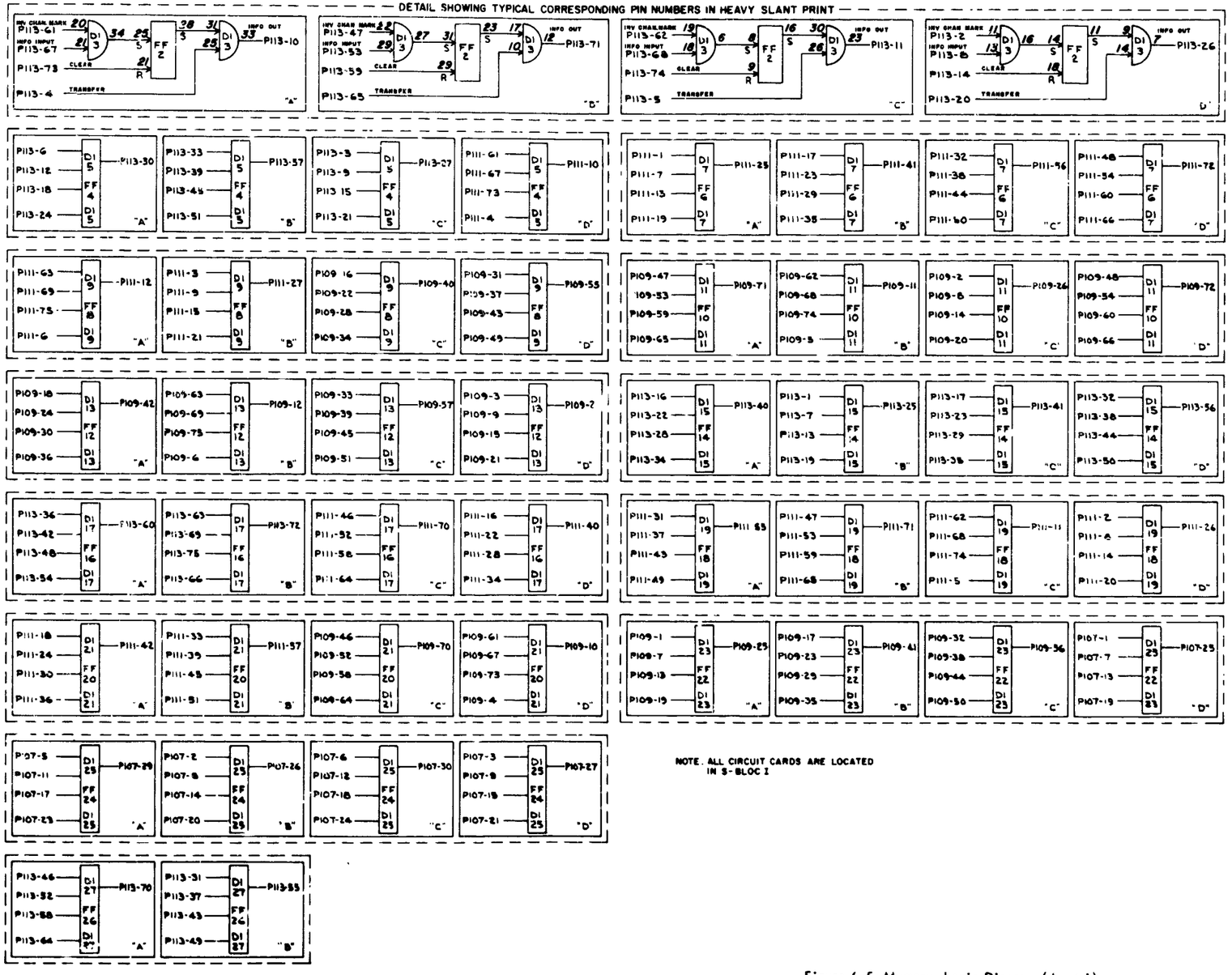


Figure 6-5–Memory, Logic Diagram (sheet 1)

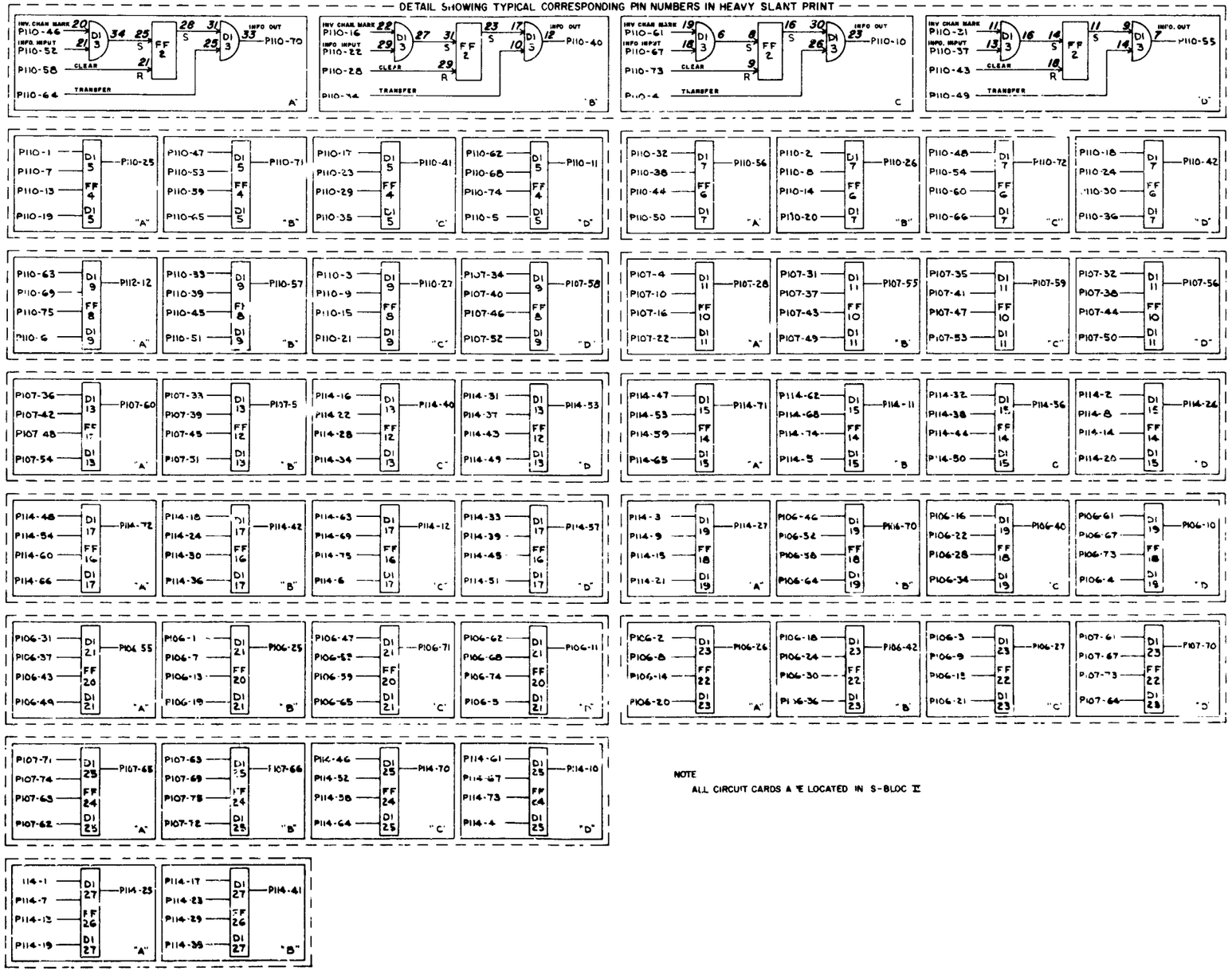


Figure 6-5–Memory, Logic Diagram (sheet 2)

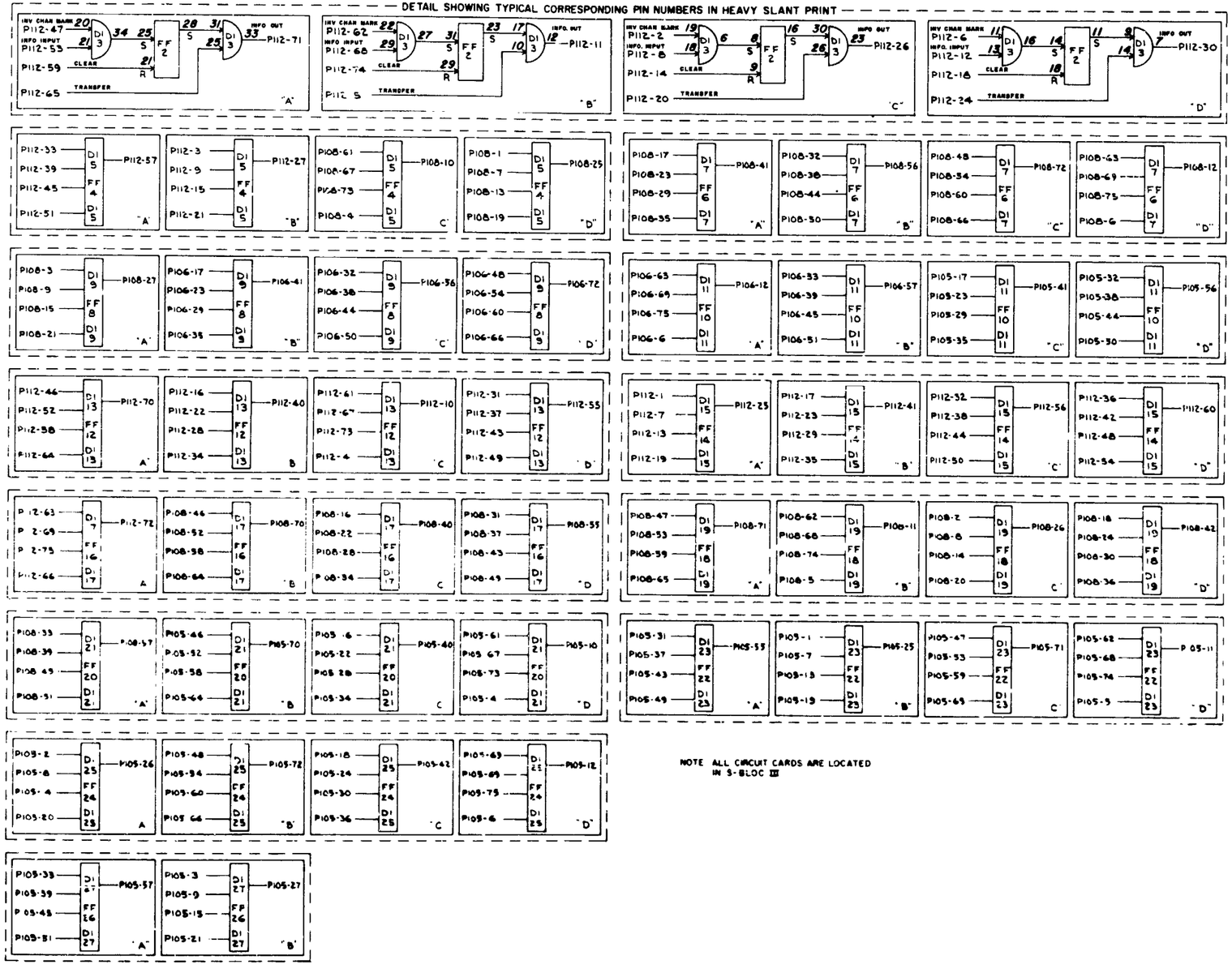


Figure 6-5—Memory, Logic Diagram (sheet 3)

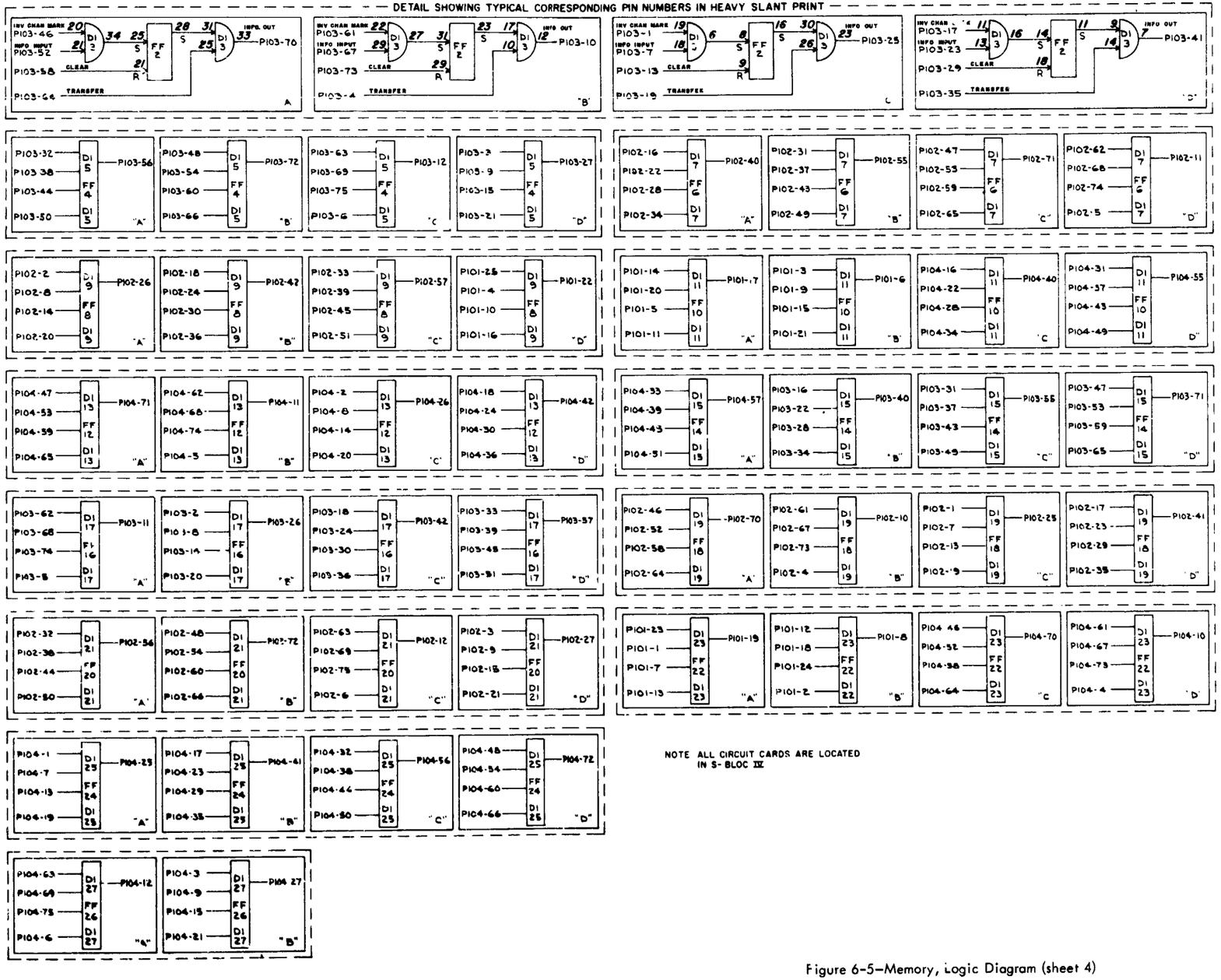


Figure 6-5–Memory, Logic Diagram (sheet 4)

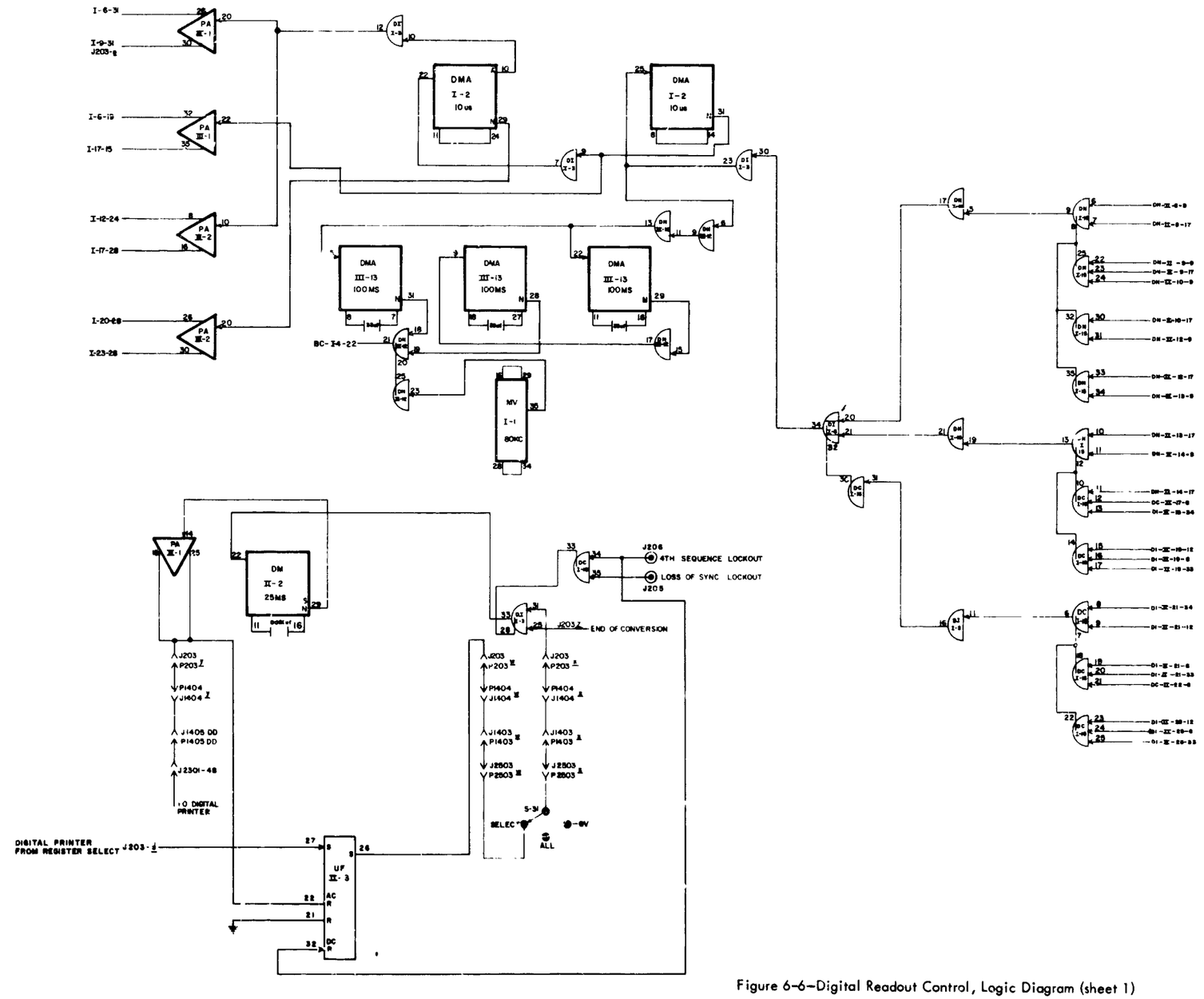


Figure 6-6–Digital Readout Control, Logic Diagram (sheet 1)

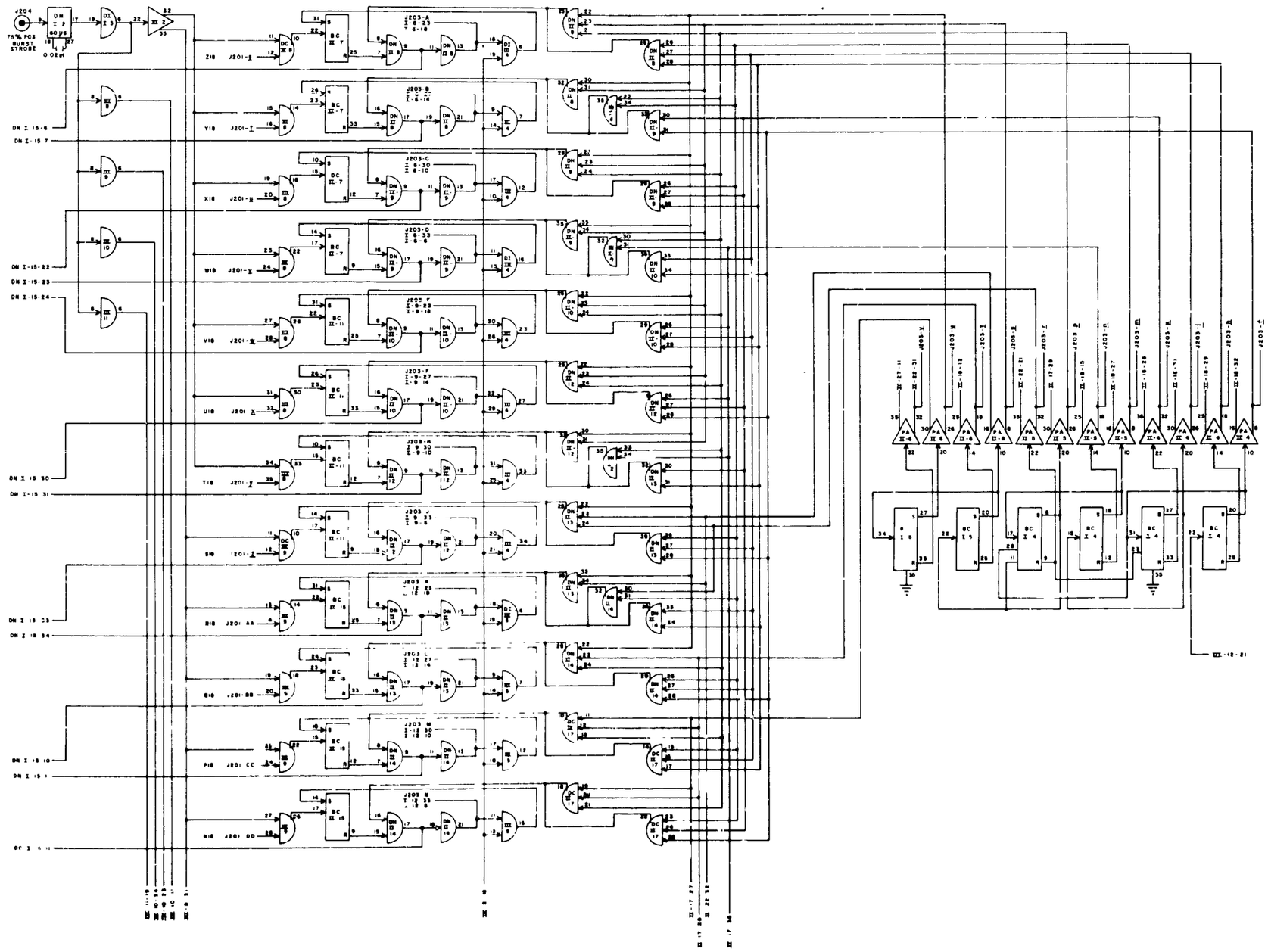


Figure 6-6—Digital Readout Control, Logic Diagram (sheet 2)

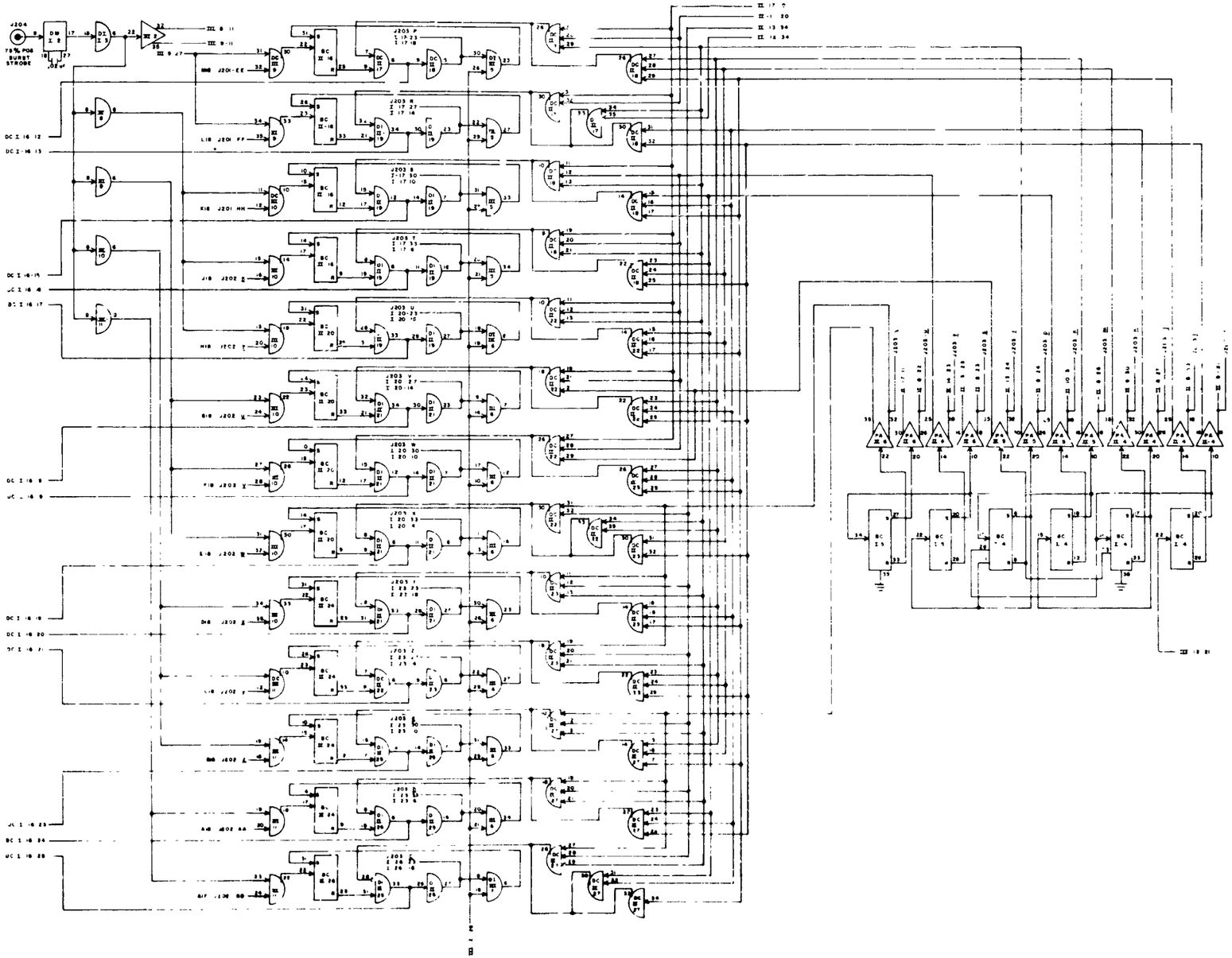


Figure 6-6–Digital Readout Control, Logic Diagram (sheet 3)

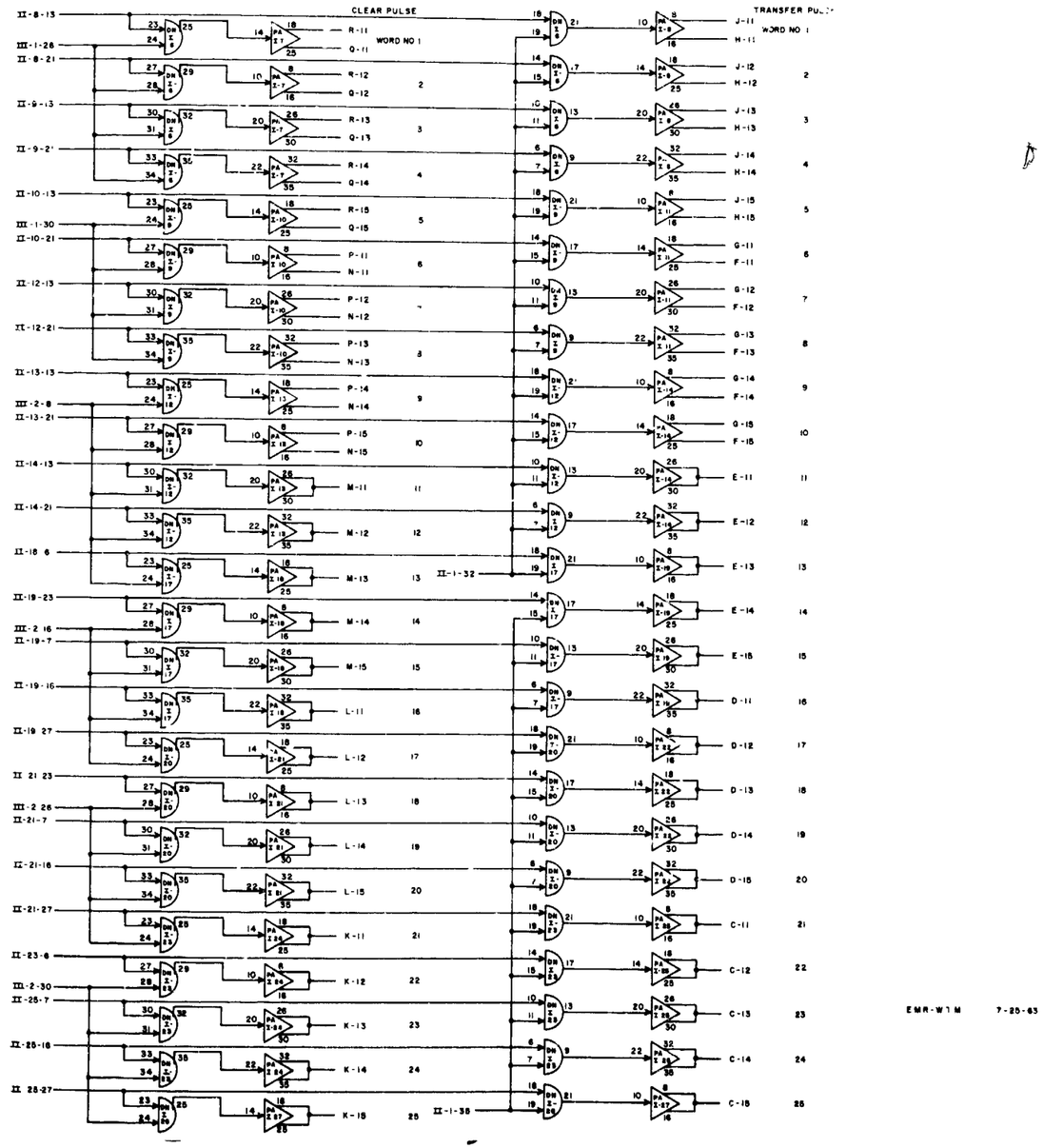


Figure 6-6-Digital Readout Control, Logic Diagram (sheet 4)

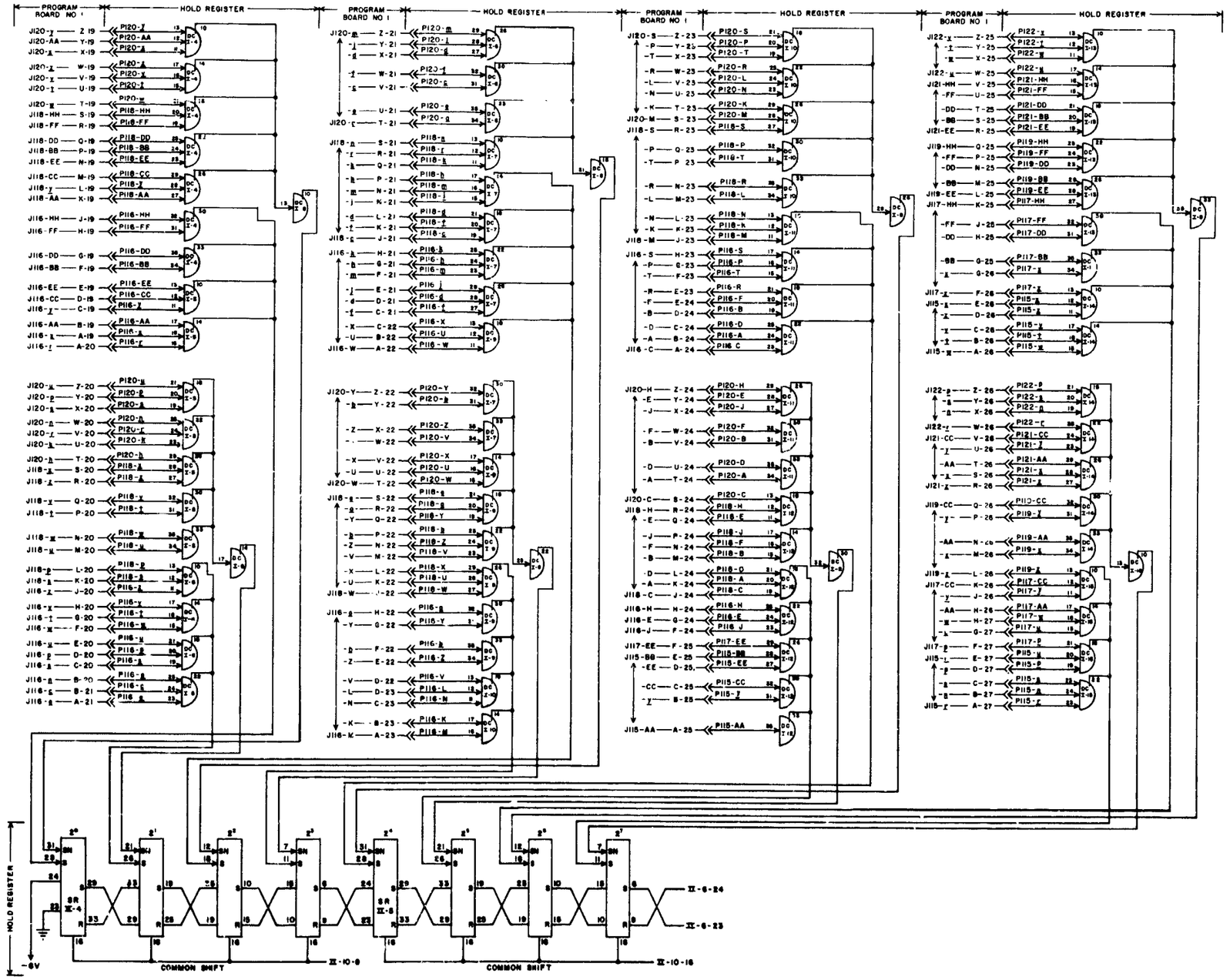


Figure 6-7–Hold Register, Logic Diagram (sheet 1)

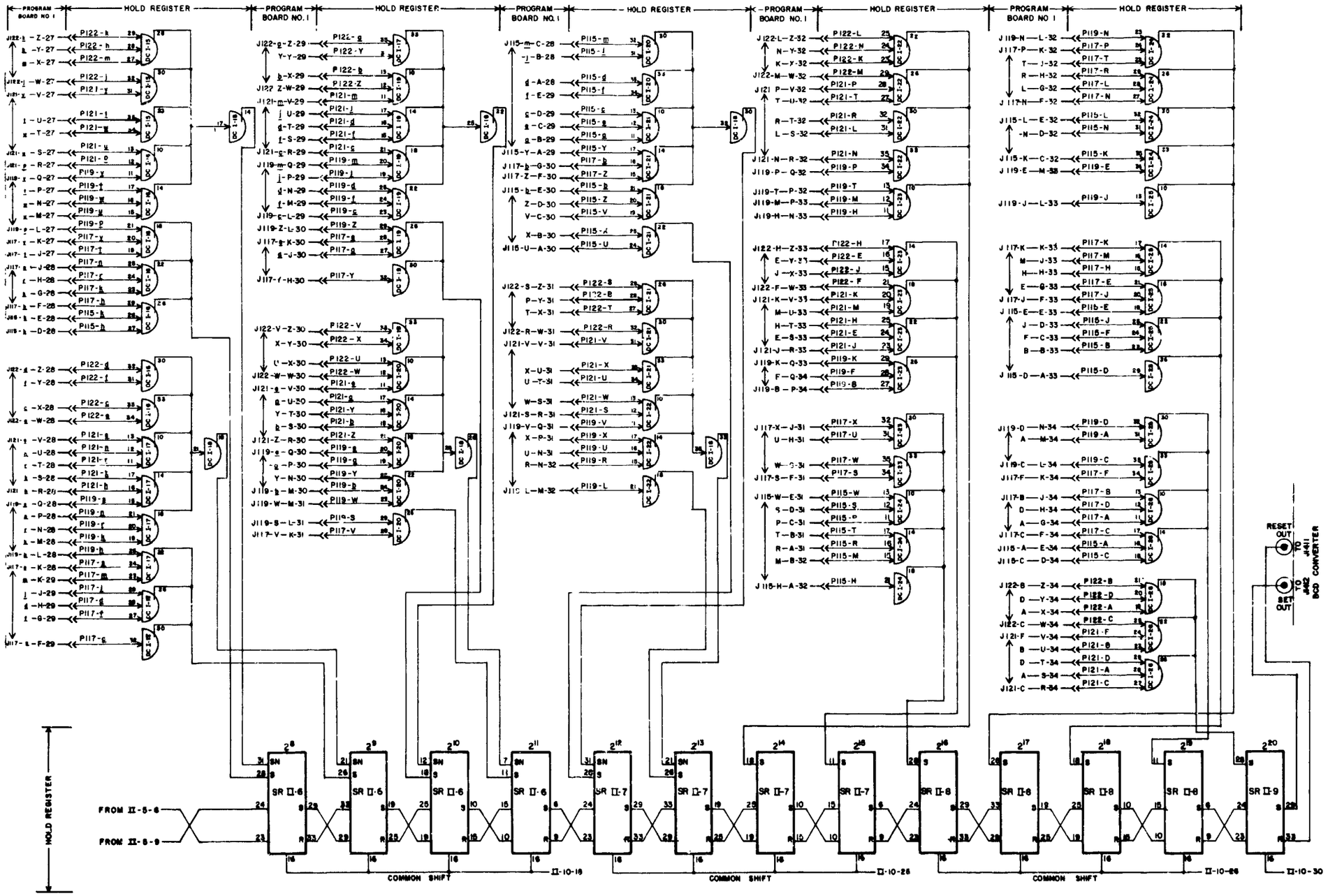
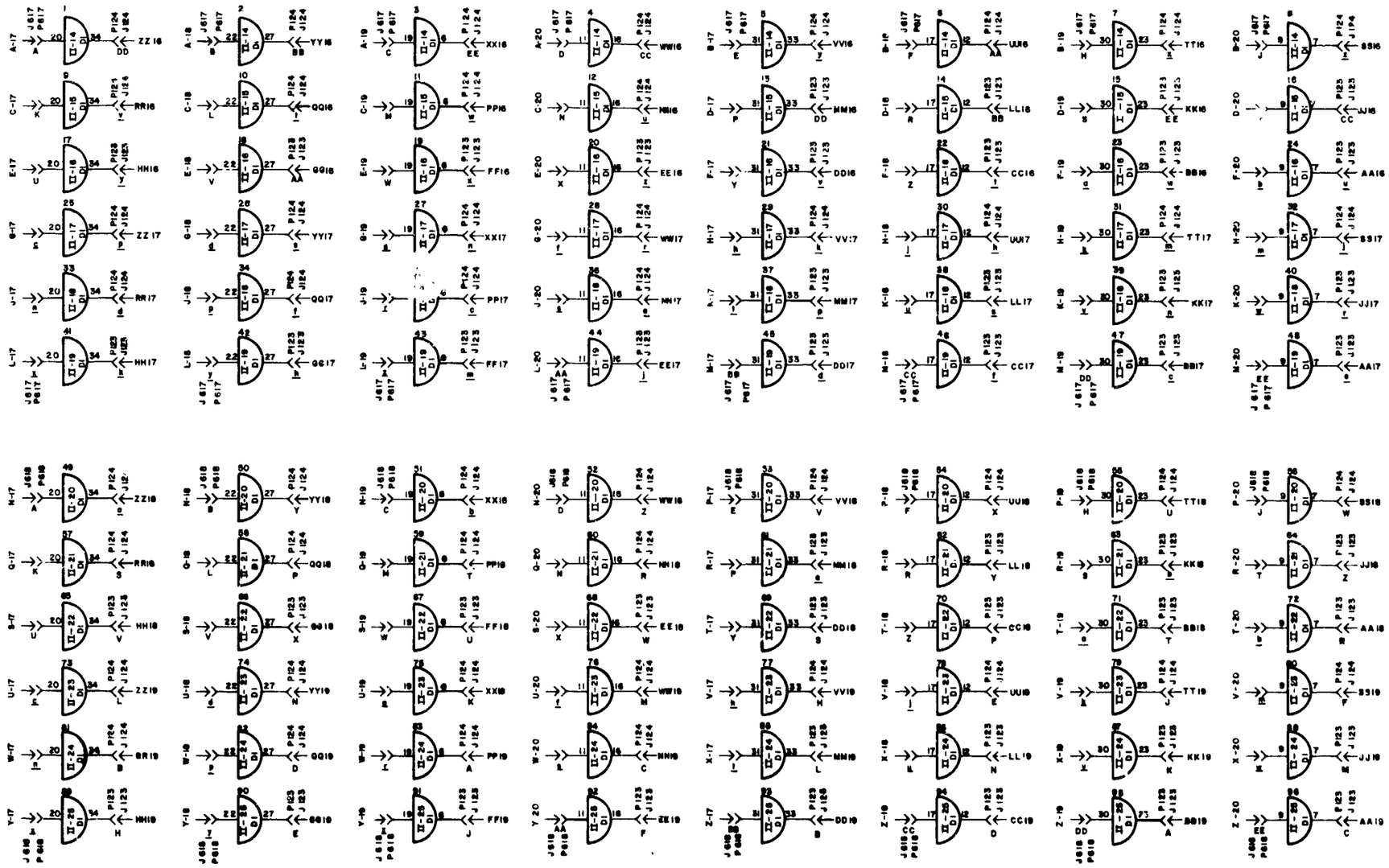


Figure 6-7—Hold Register, Logic Diagram (sheet 2)



NOTE:

A. ZZ16 THRU AA19 ARE LOCATED ON PROGRAM BOARD NO. 1
B. A-17 THRU Z-20 ARE LOCATED ON PROGRAM BOARD NO. 2

Figure 6-7–Hold Register, Logic Diagram (sheet 3)

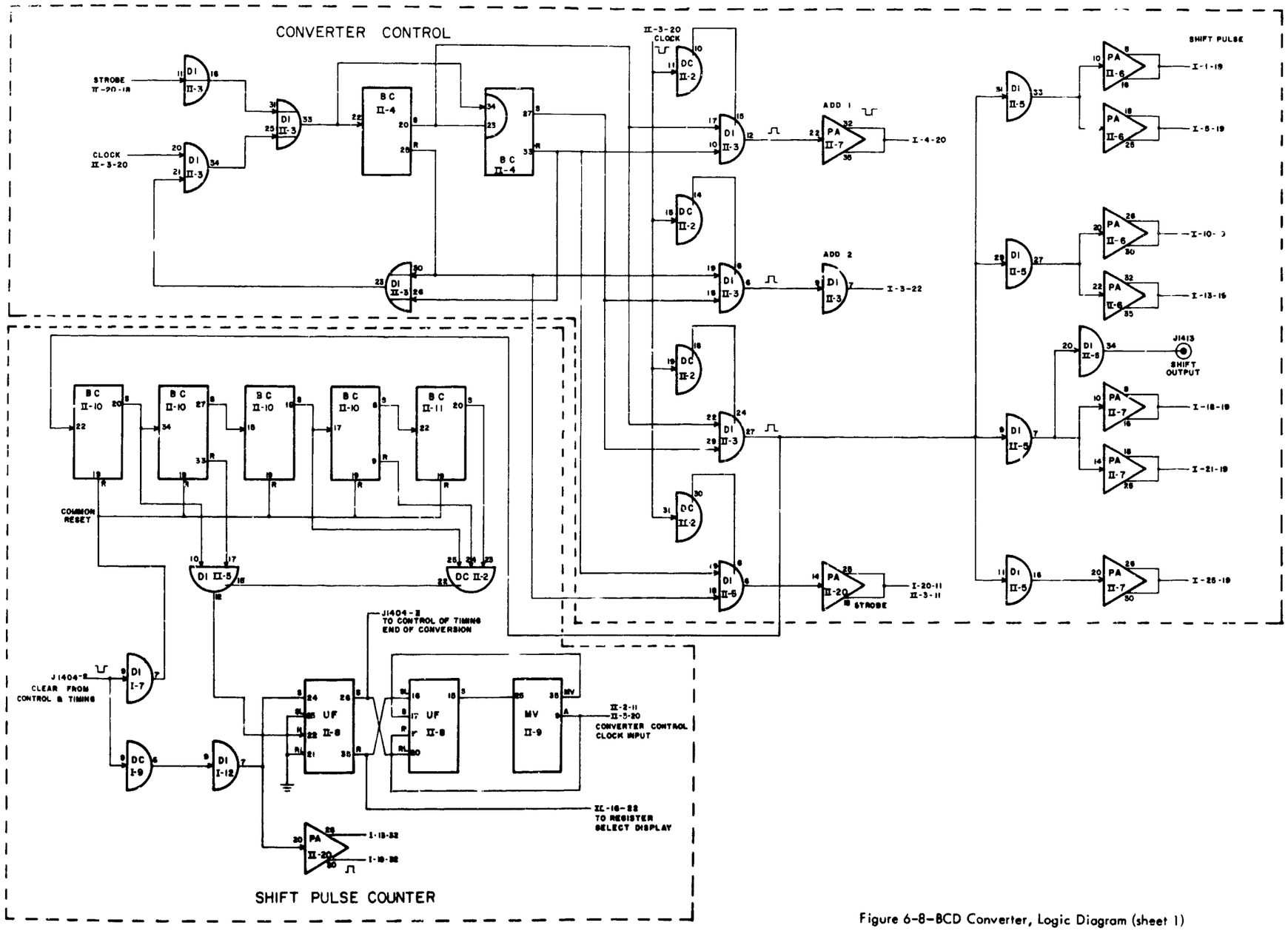
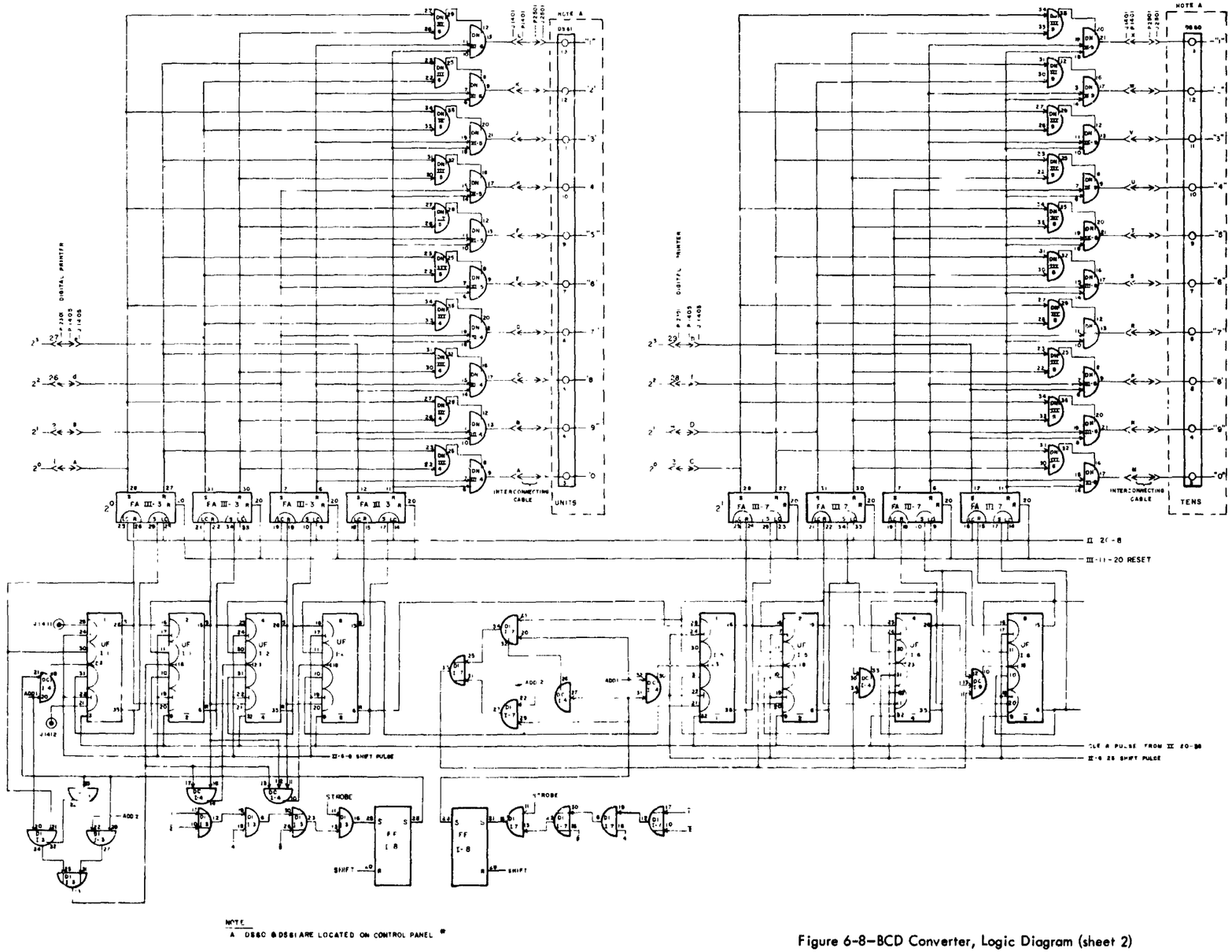


Figure 6-8-BCD Converter, Logic Diagram (sheet 1)



NOTE
A DS&C & DS81 ARE LOCATED ON CONTROL PANEL *

Figure 6-8—BCD Converter, Logic Diagram (sheet 2)

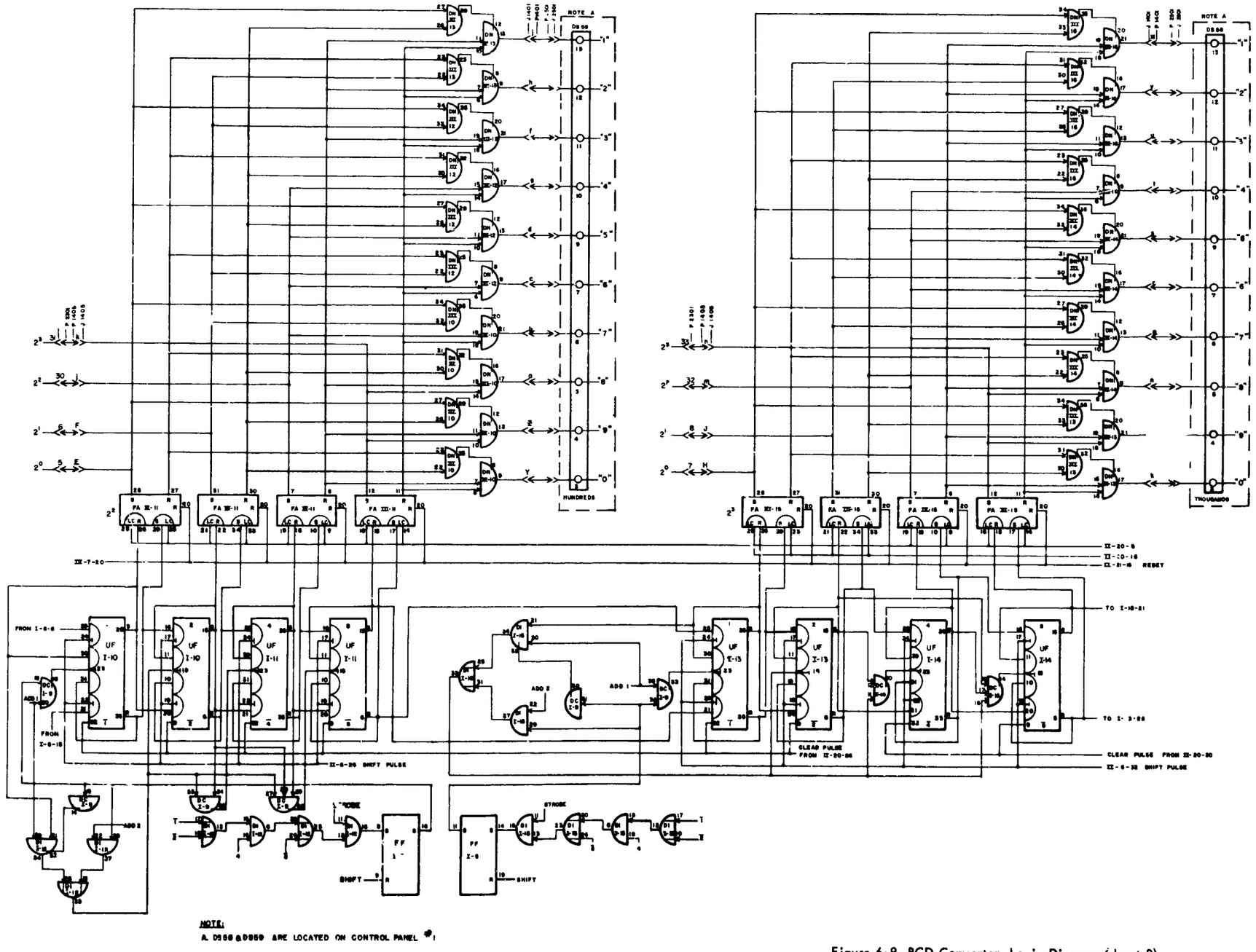
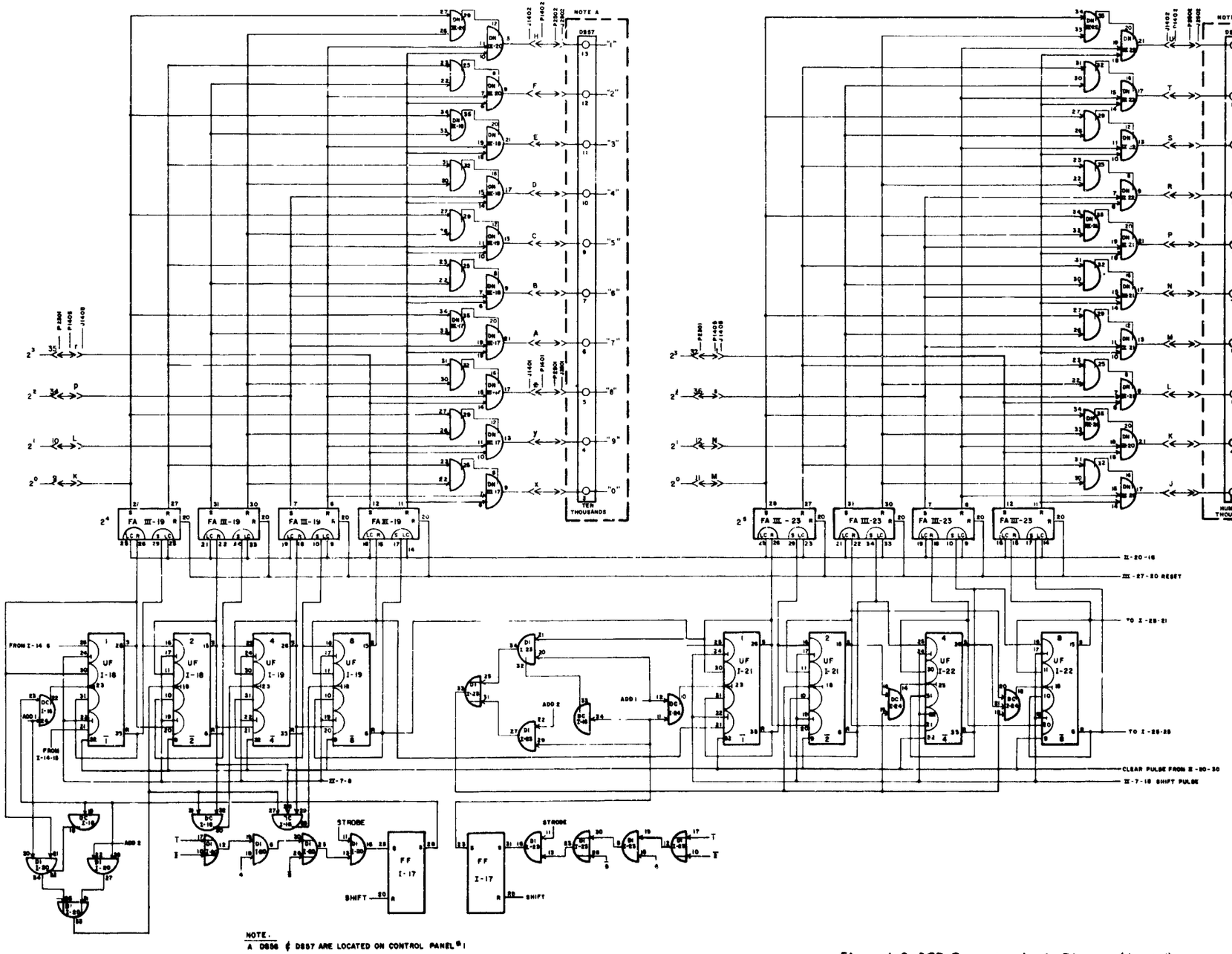


Figure 6-8–BCD Converter, Logic Diagram (sheet 3)



NOTE.
A D856 & D857 ARE LOCATED ON CONTROL PANEL #1

Figure 6-8-BCD Converter, Logic Diagram (sheet 4)

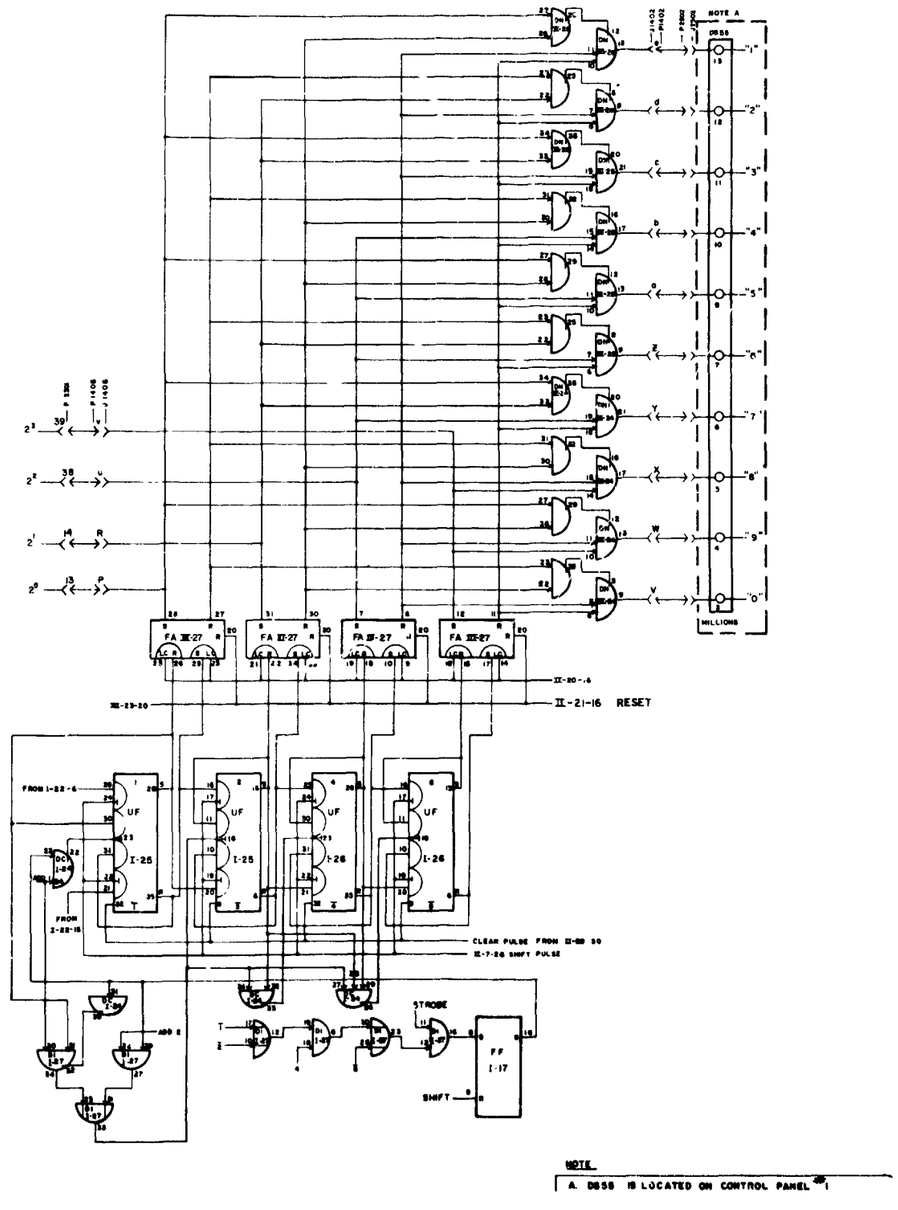


Figure 6-8–BCD Converter, Logic Diagram (sheet 5)

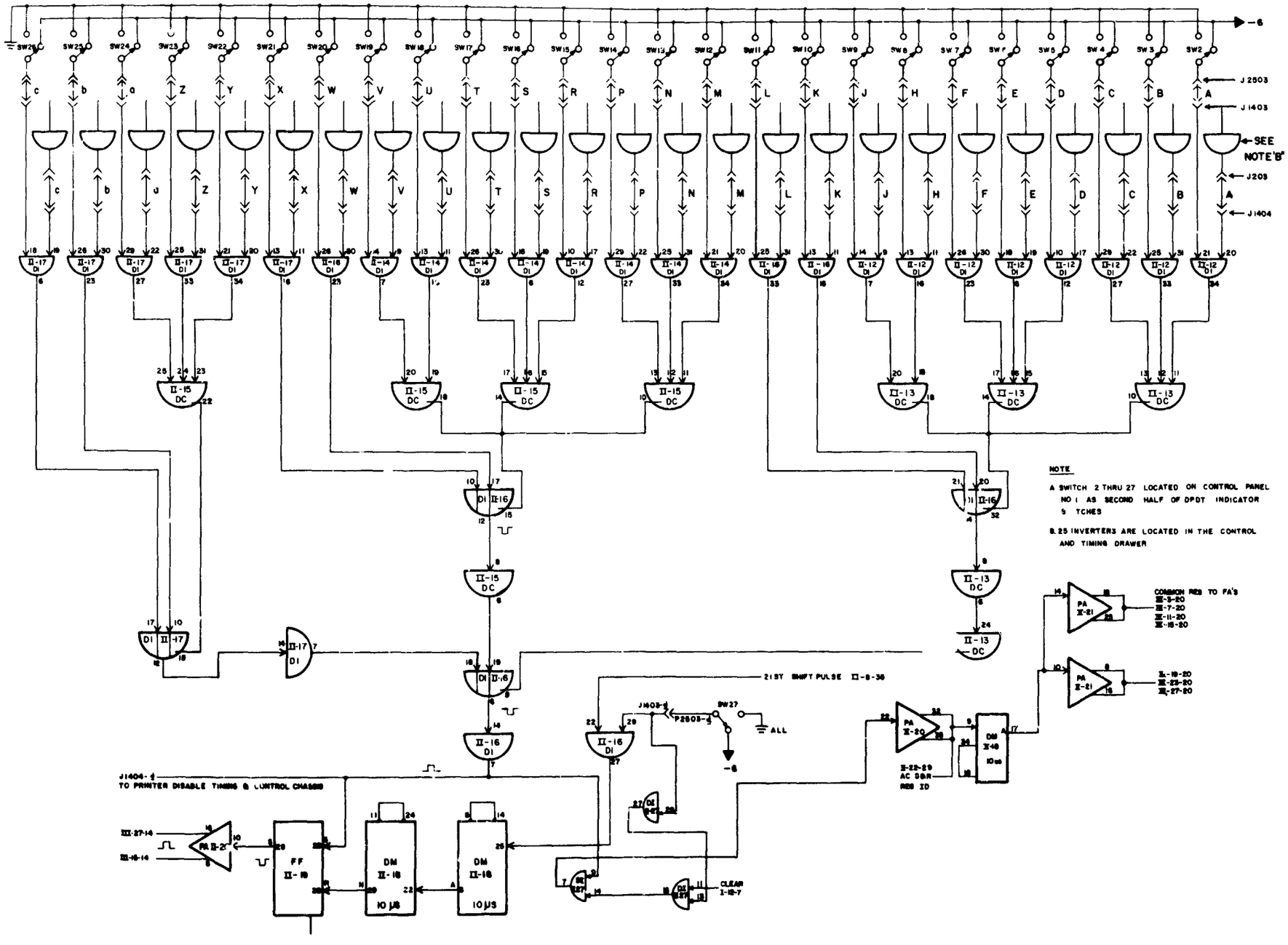


Figure 6-8-BCD Converter, Logic Diagram (sheet 6)

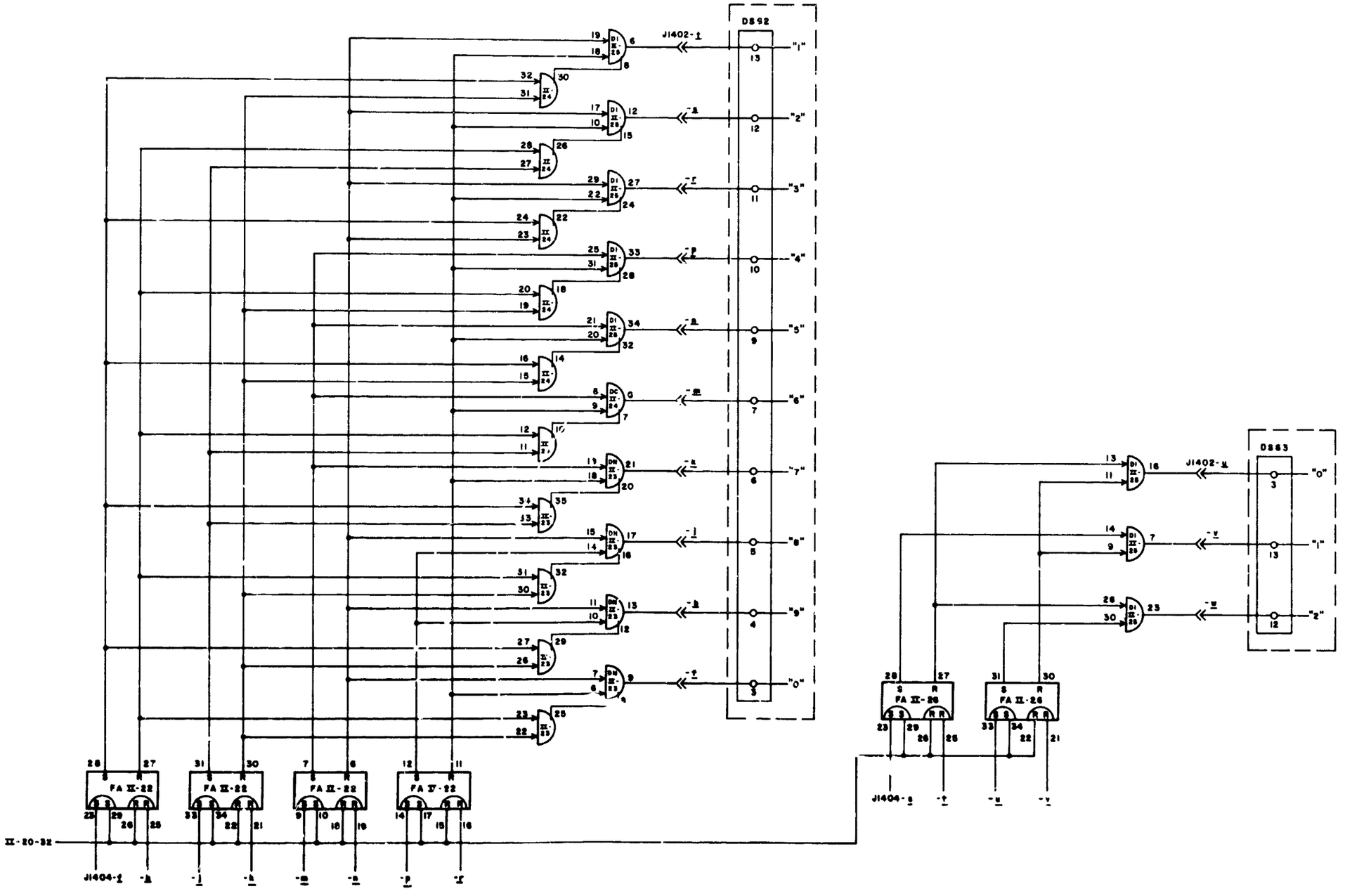


Figure 6-8-BCD Converter, Logic Diagram (sheet 7)

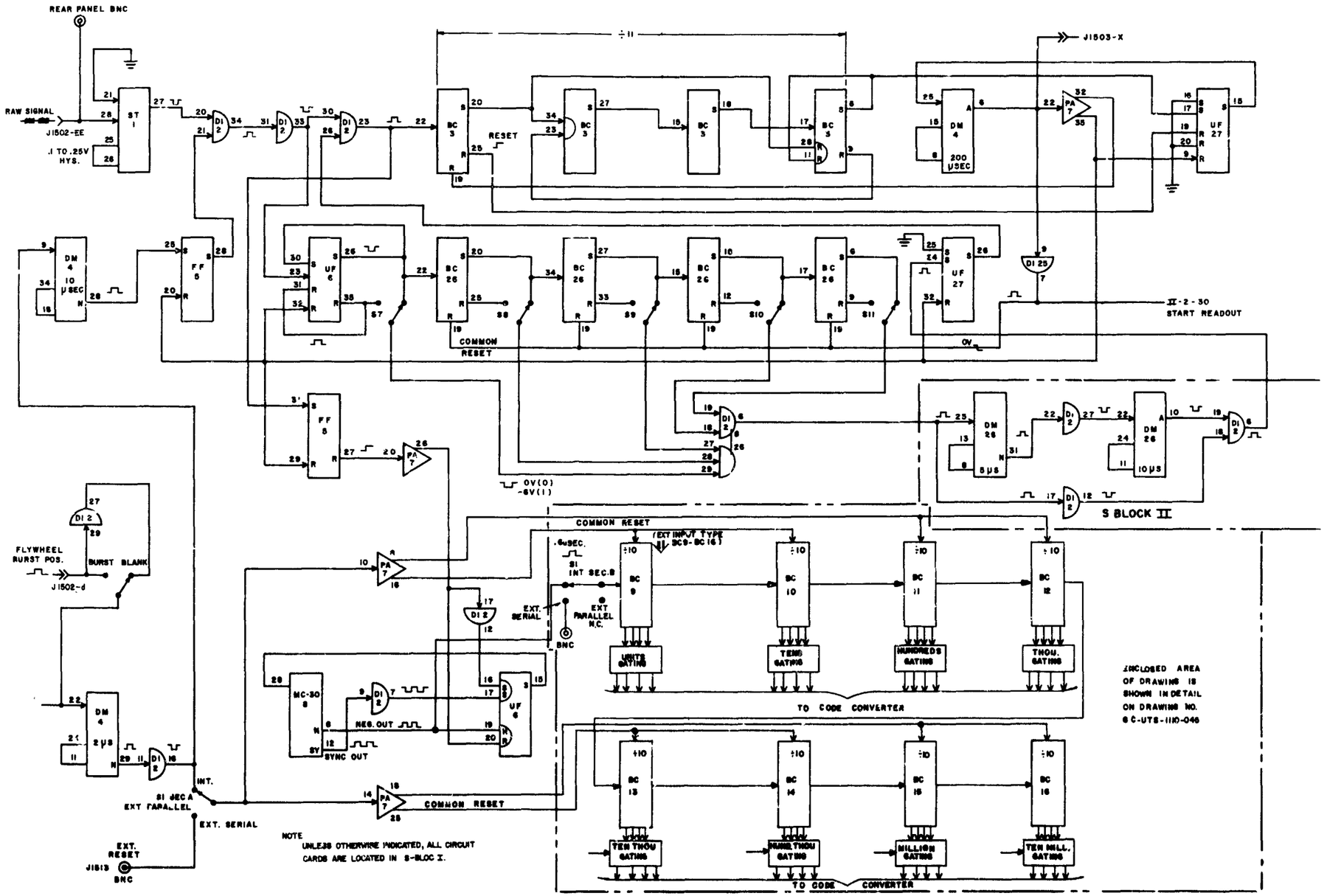
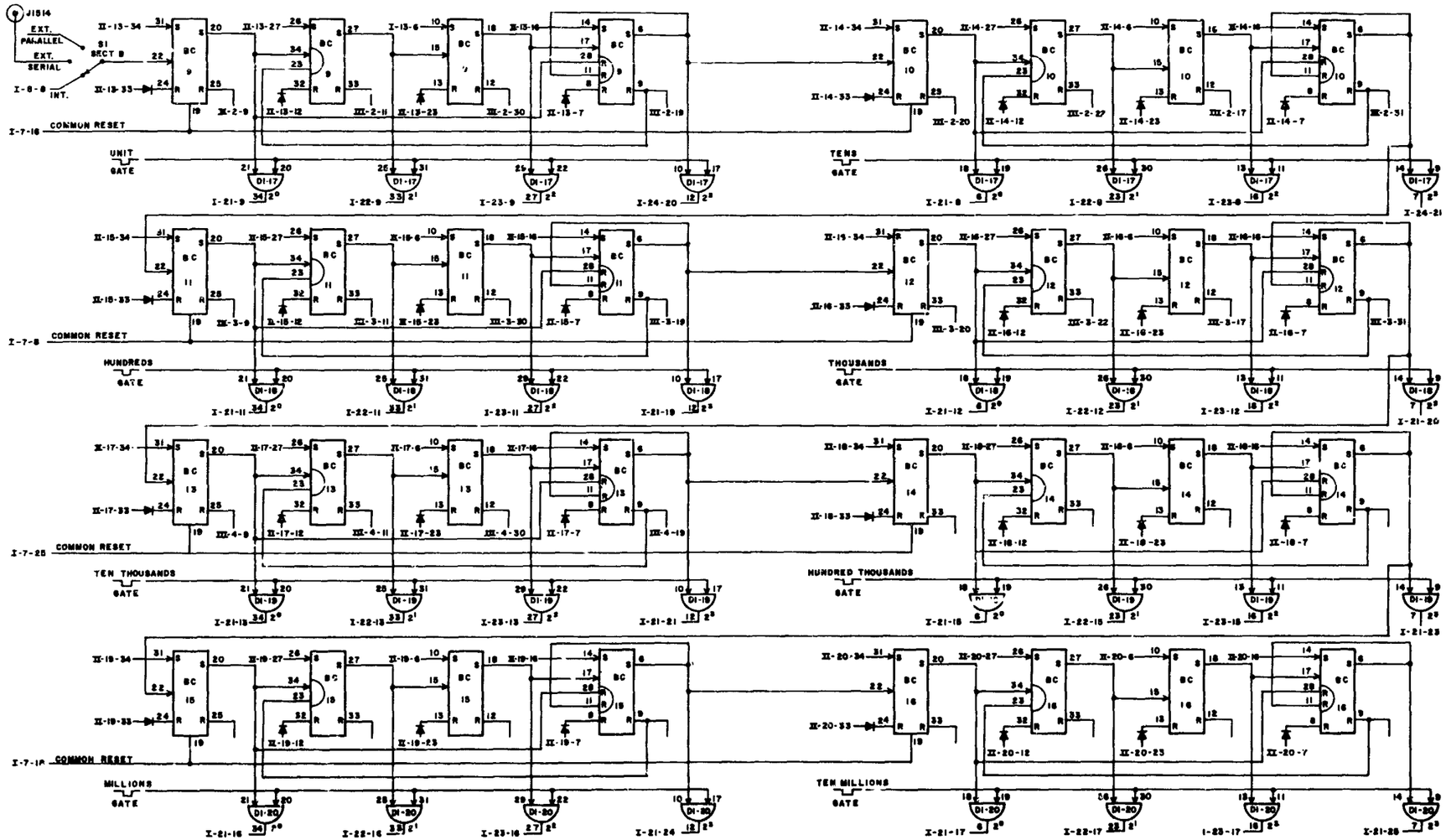
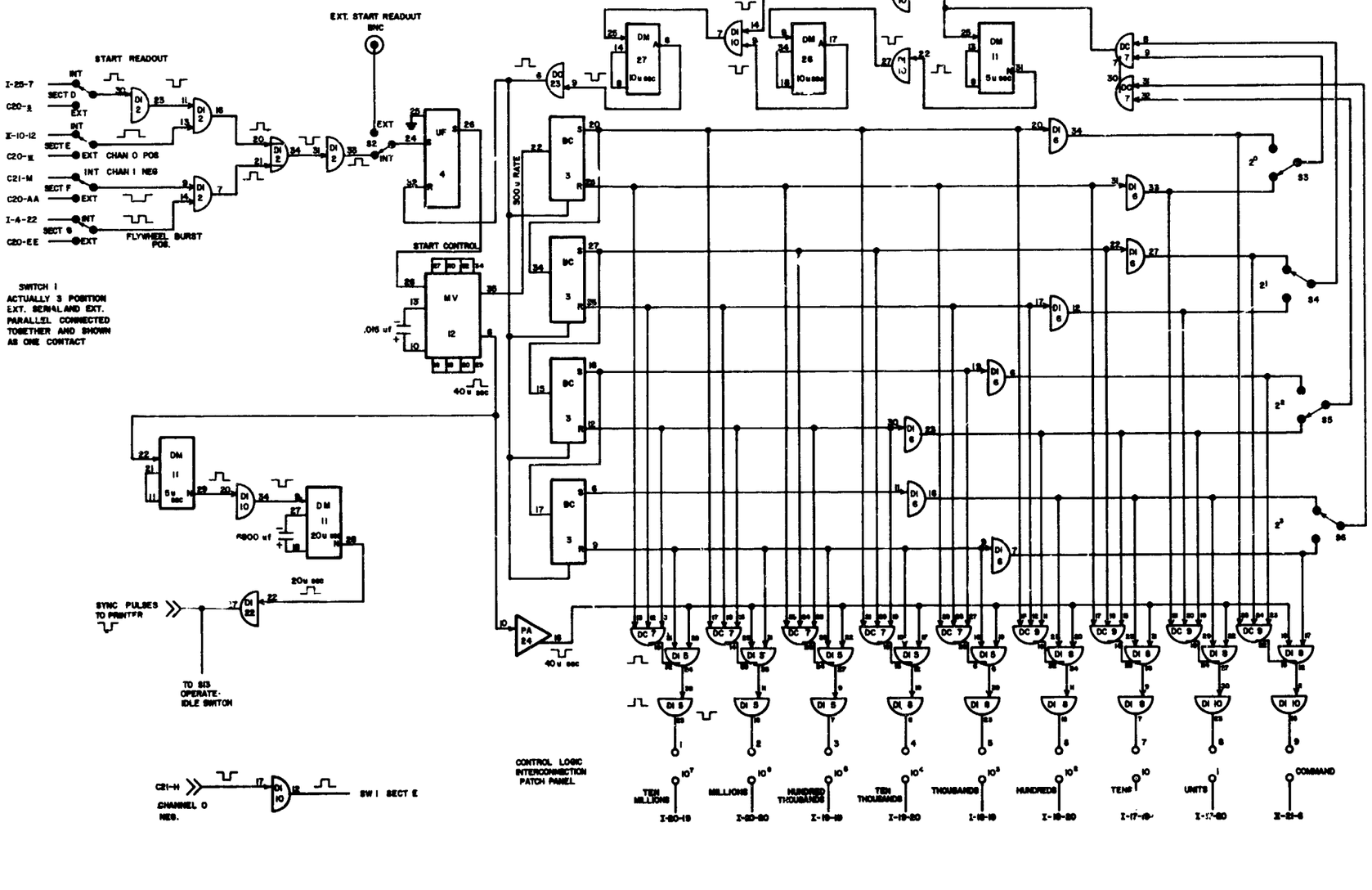


Figure 6-9—Printer Code Converter, Logic Diagram (sheet 1)



NOTE: UNLESS OTHERWISE INDICATED, CIRCUIT CARDS ARE LOCATED IN 9-BLOC I.

Figure 6-9—Printer Code Converter, Logic Diagram (sheet 2)



NOTE: ALL CIRCUIT CARDS ARE LOCATED IN S- BLOC II.

Figure 6-9—Printer Code Converter, Logic Diagram (sheet 3)

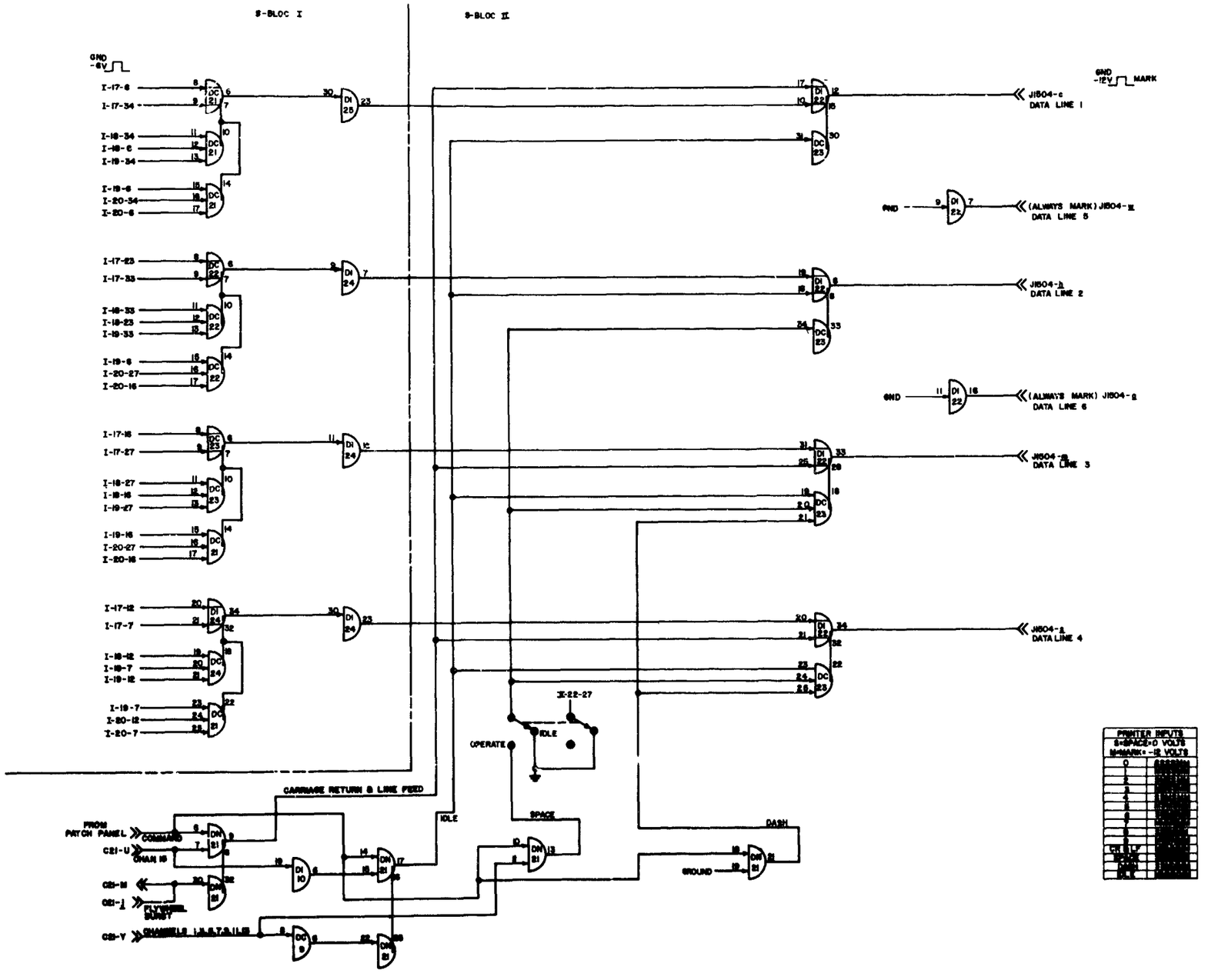
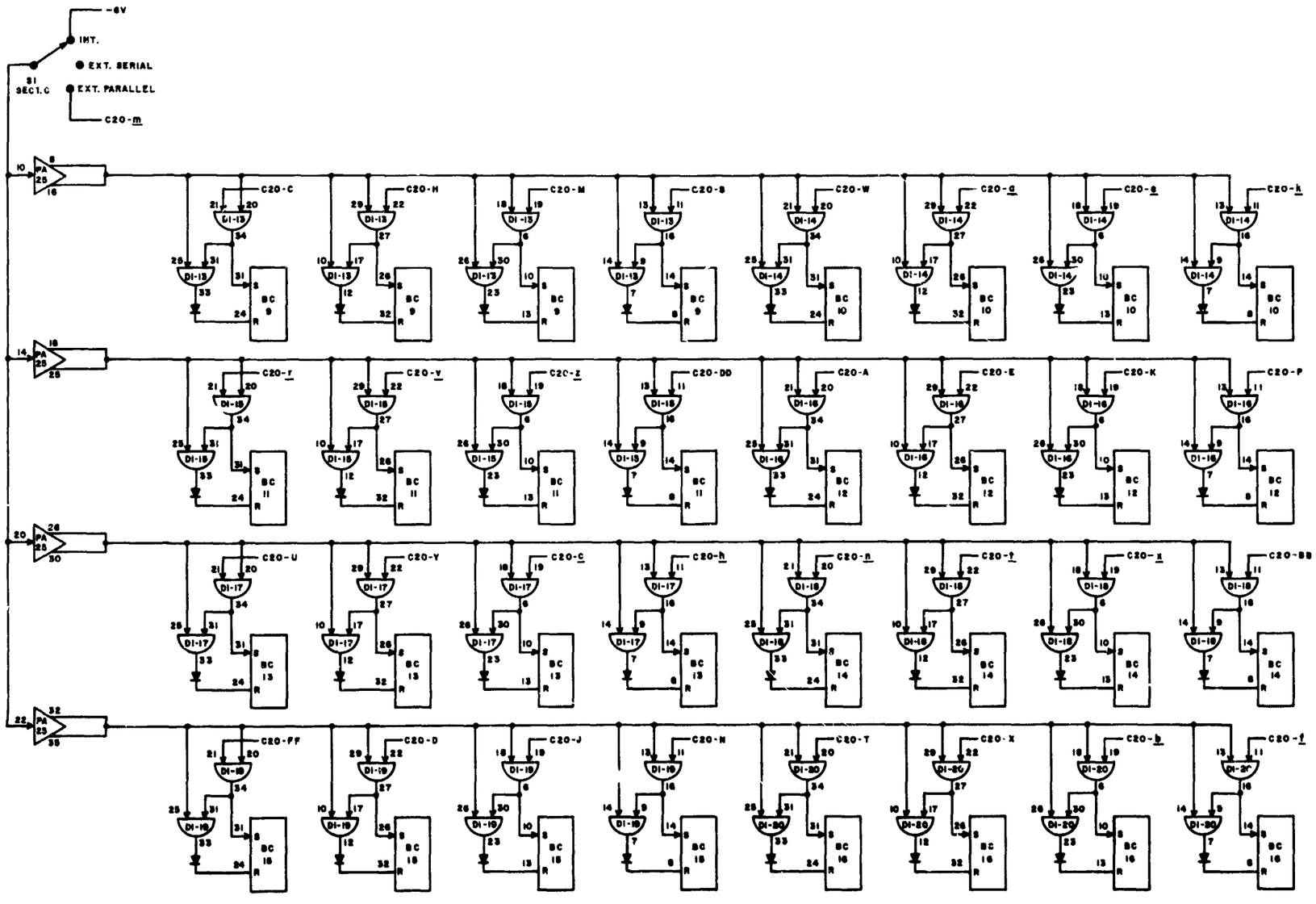


Figure 6-9—Printer Code Converter, Logic Diagram (sheet 4)



NOTES:

1. ALL DIODES IN127A
2. ALL BC BOARDS ARE LOCATED IN 8 BLOC Σ
3. ALL DI AND PA BOARDS ARE LOCATED IN 8 BLOC Σ

Figure 6-9–Printer Code Converter, Logic Diagram (sheet 5)

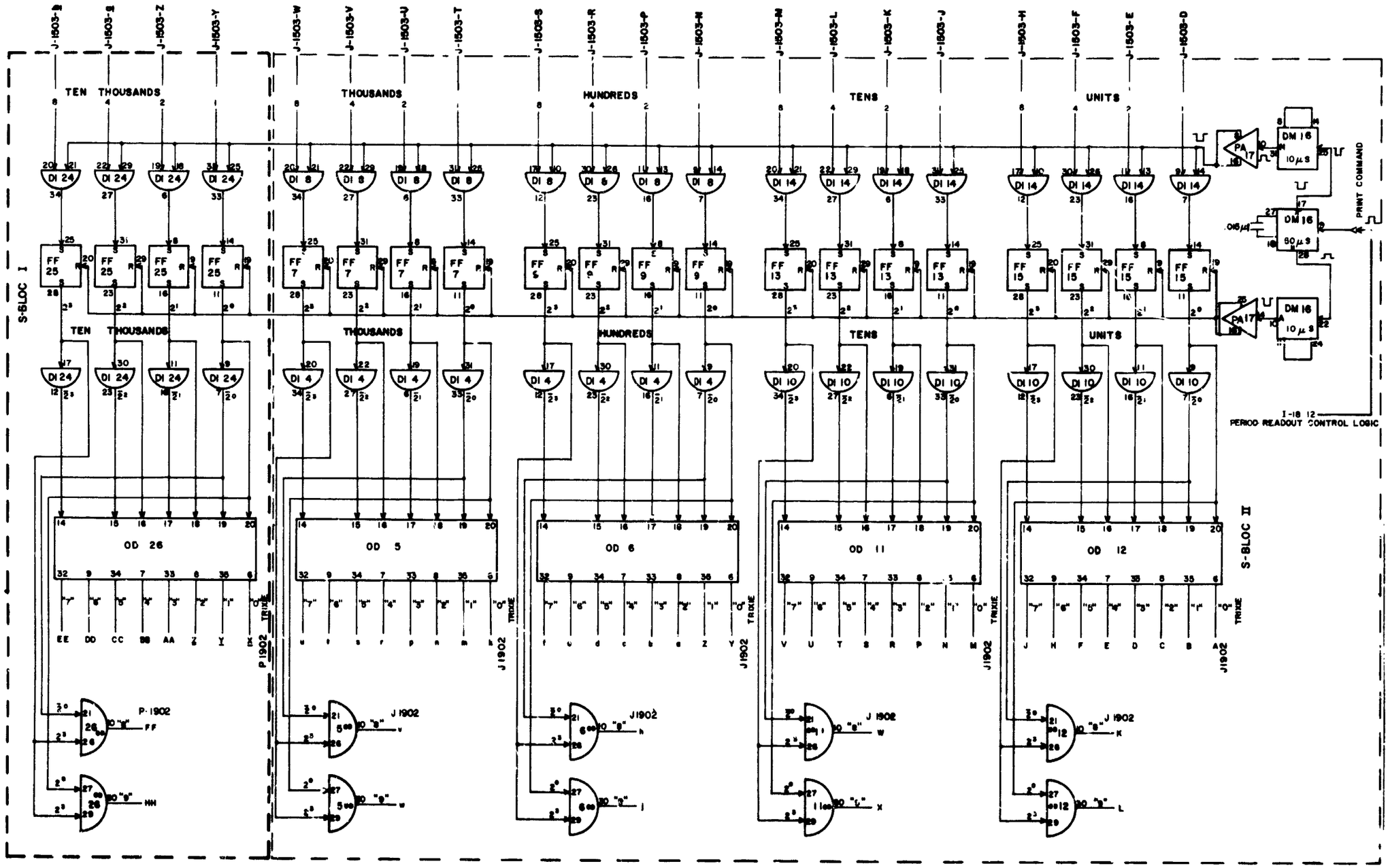


Figure 6-10–Period Readout and Display, Logic Diagram (sheet 1)

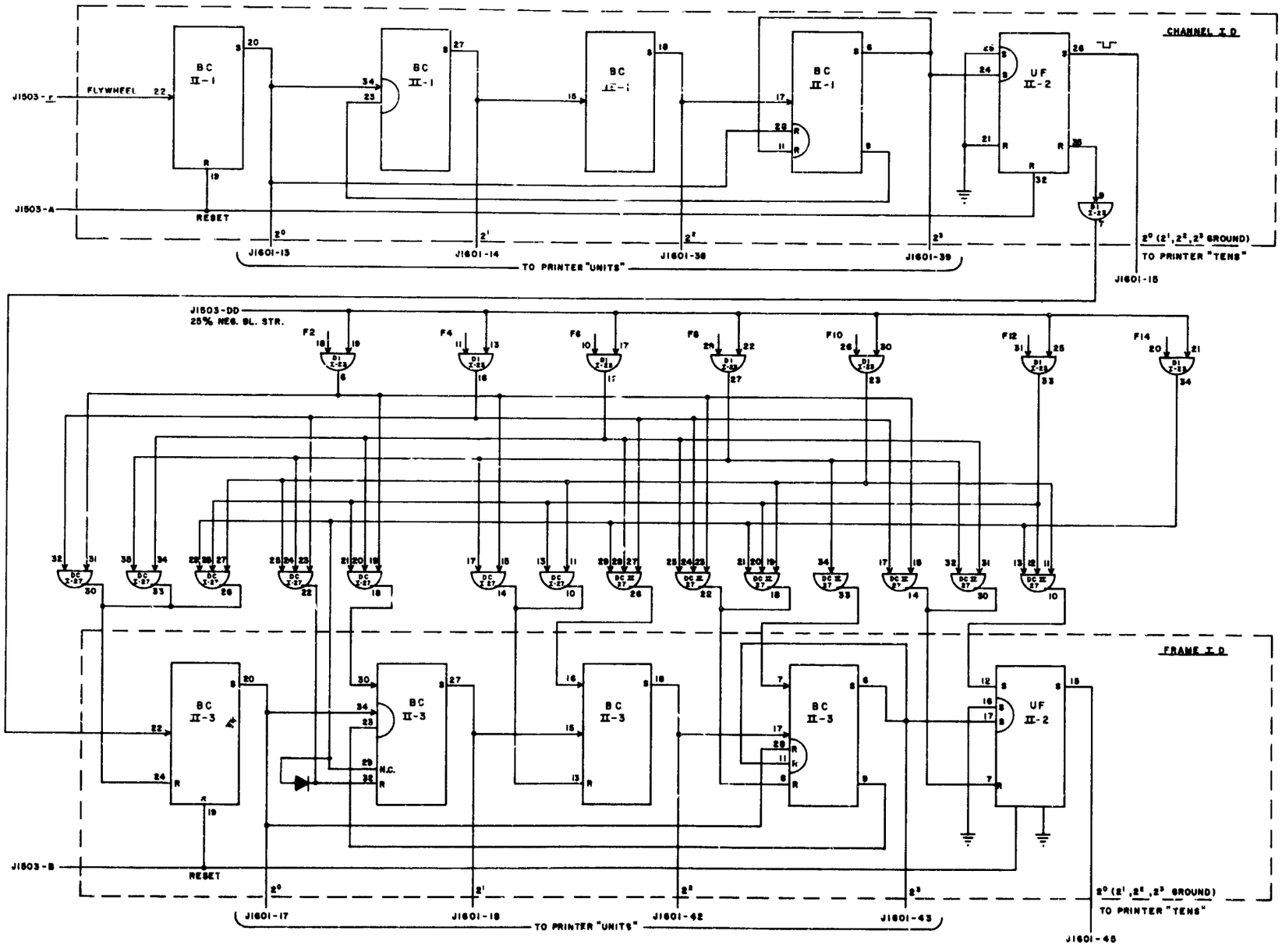
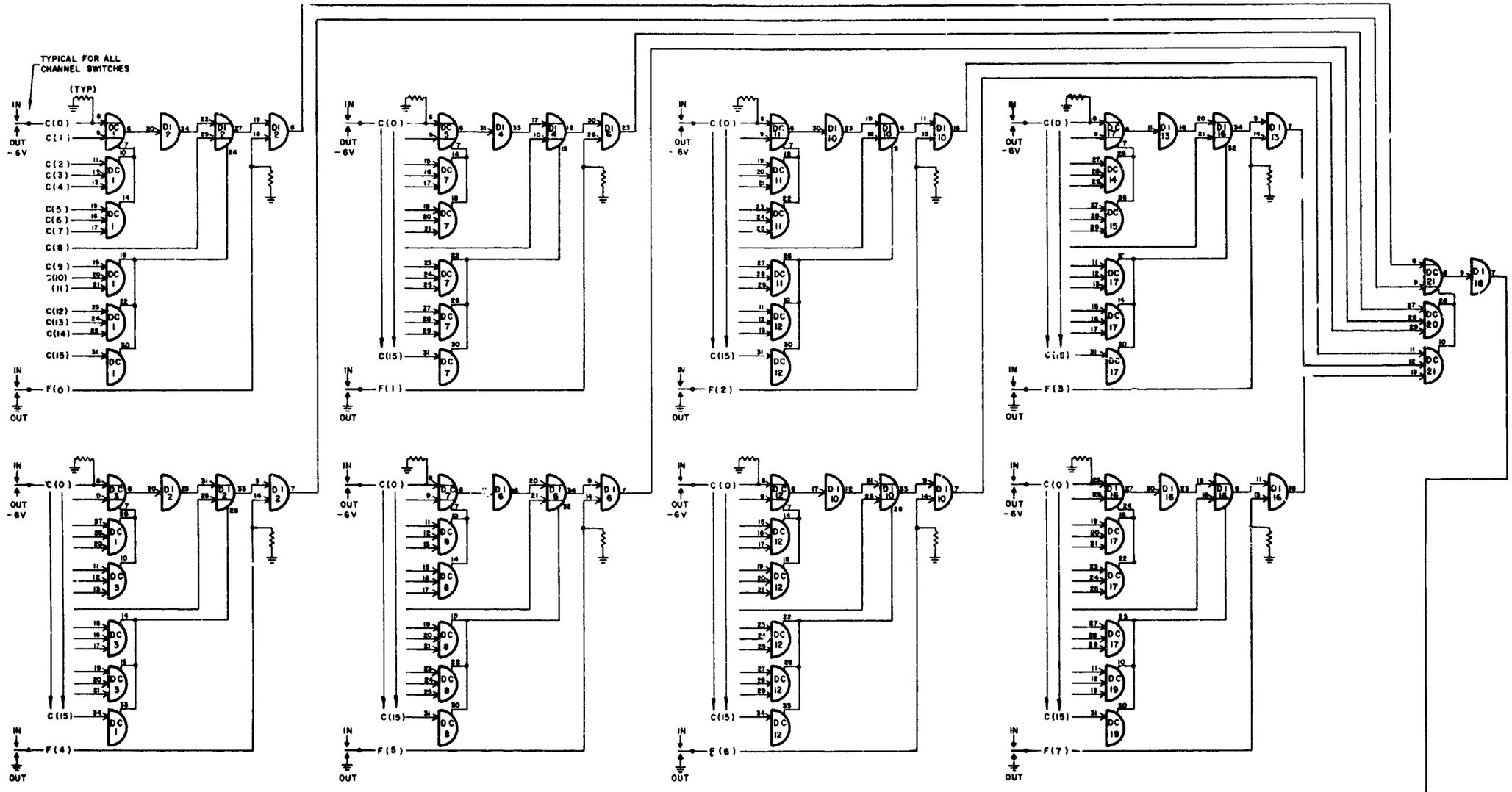


Figure 6-10–Period Readout and Display, Logic Diagram (sheet 2)



NOTE:

1. THE 136 GATE INPUTS MARKED WITH A "C" OR "F" OR SEQUENCE NUMBER SHALL BE WIRED THRU A CONNECTOR TO THE CORRESPONDING SWITCH POLE ON THE "PERIOD CONTROL SWITCH BANK" AS INDICATED.
2. EACH OF THE ABOVE INPUTS SHALL BE TERMINATED BY A 1/4W, 10K RESISTOR.
3. PIN 35 SHALL BE WIRED TO PIN 5 ON ALL DI BOARDS.
4. ALL CIRCUIT CARDS ARE LOCATED IN S-BLOC I.

Figure 6-10—Period Readout and Display, Logic Diagram (sheet 3)

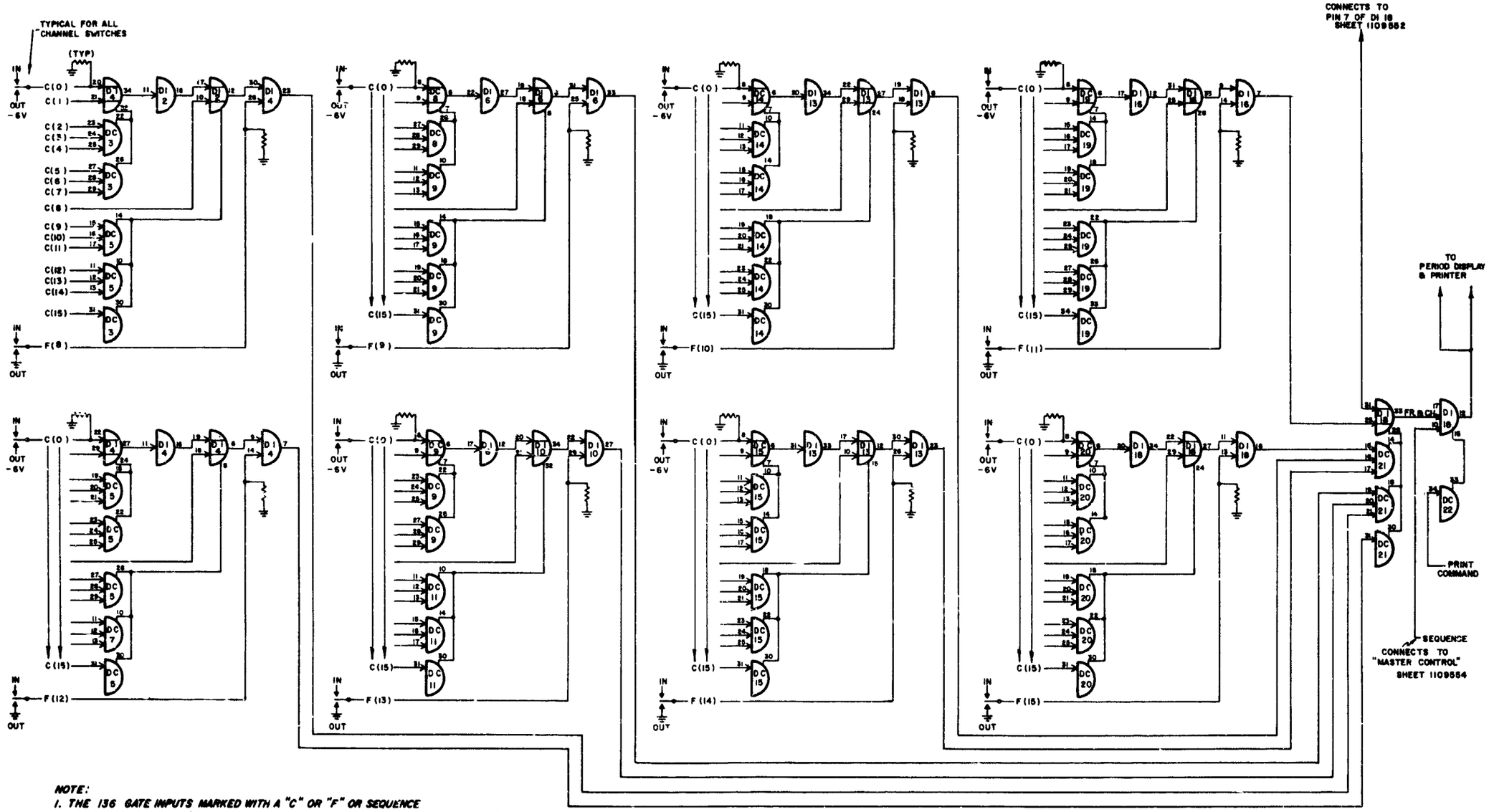
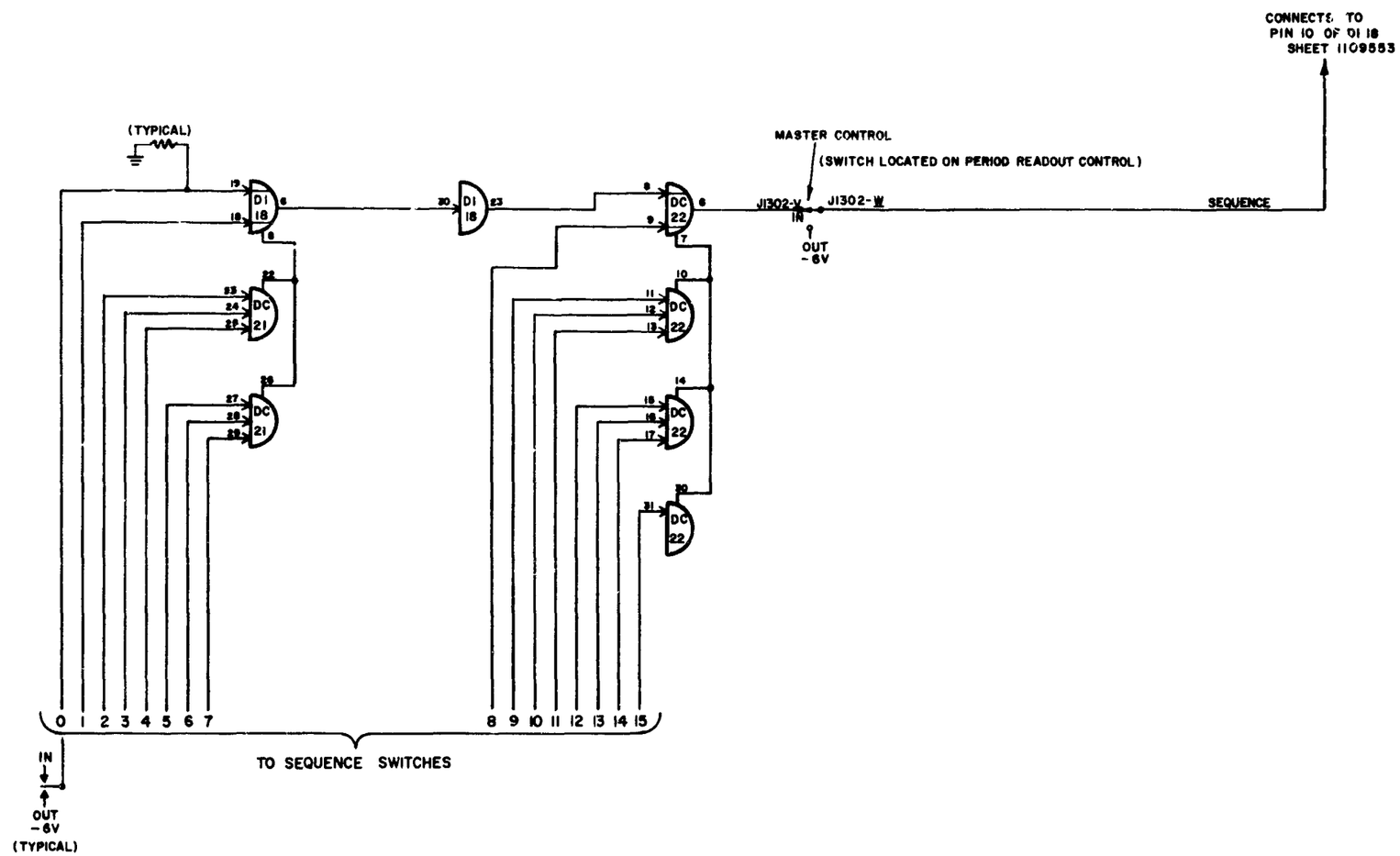


Figure 6-10–Period Readout and Display, Logic Diagram (sheet 4)



NOTE:

1. THE 16 GATE INPUTS MARKED WITH A SEQUENCE NUMBER SHALL BE WIRED THRU A CONNECTOR TO THE CORRESPONDING SWITCH POLE ON THE "PERIOD CONTROL SWITCH BANK" AS INDICATED.

2. EACH OF THE ABOVE INPUTS SHALL BE TERMINATED BY A 1/4W, 10K RESISTOR.

3. PIN 35 SHALL BE WIRED TO PIN 5 ON ALL DI BOARDS.

4. ALL CIRCUIT CARDS ARE LOCATED IN S-BLOC I.

Figure 6-10—Period Readout and Display, Logic Diagram (sheet 5)

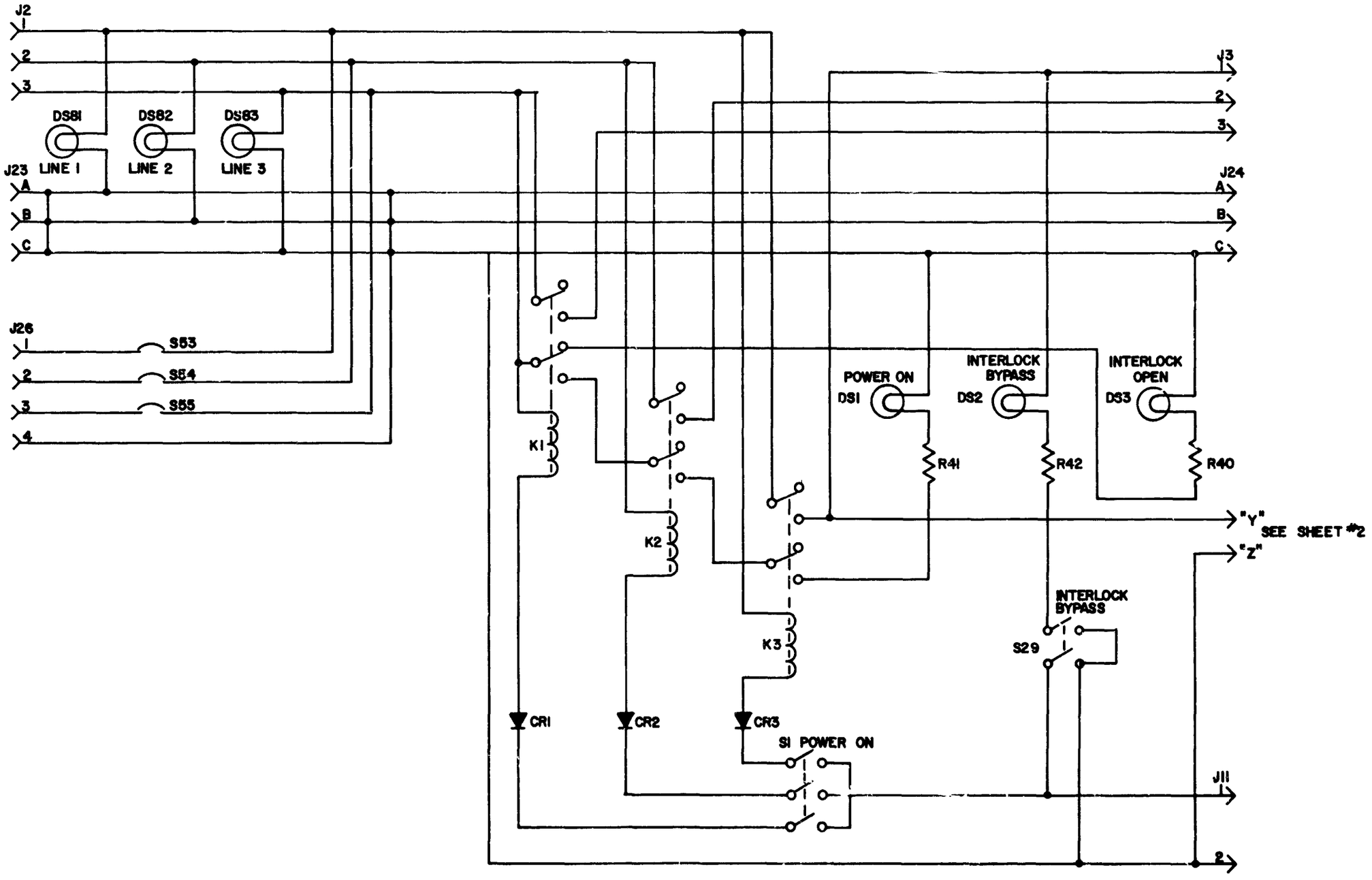


Figure 6-11-1-C Control Panel (sheet 1)

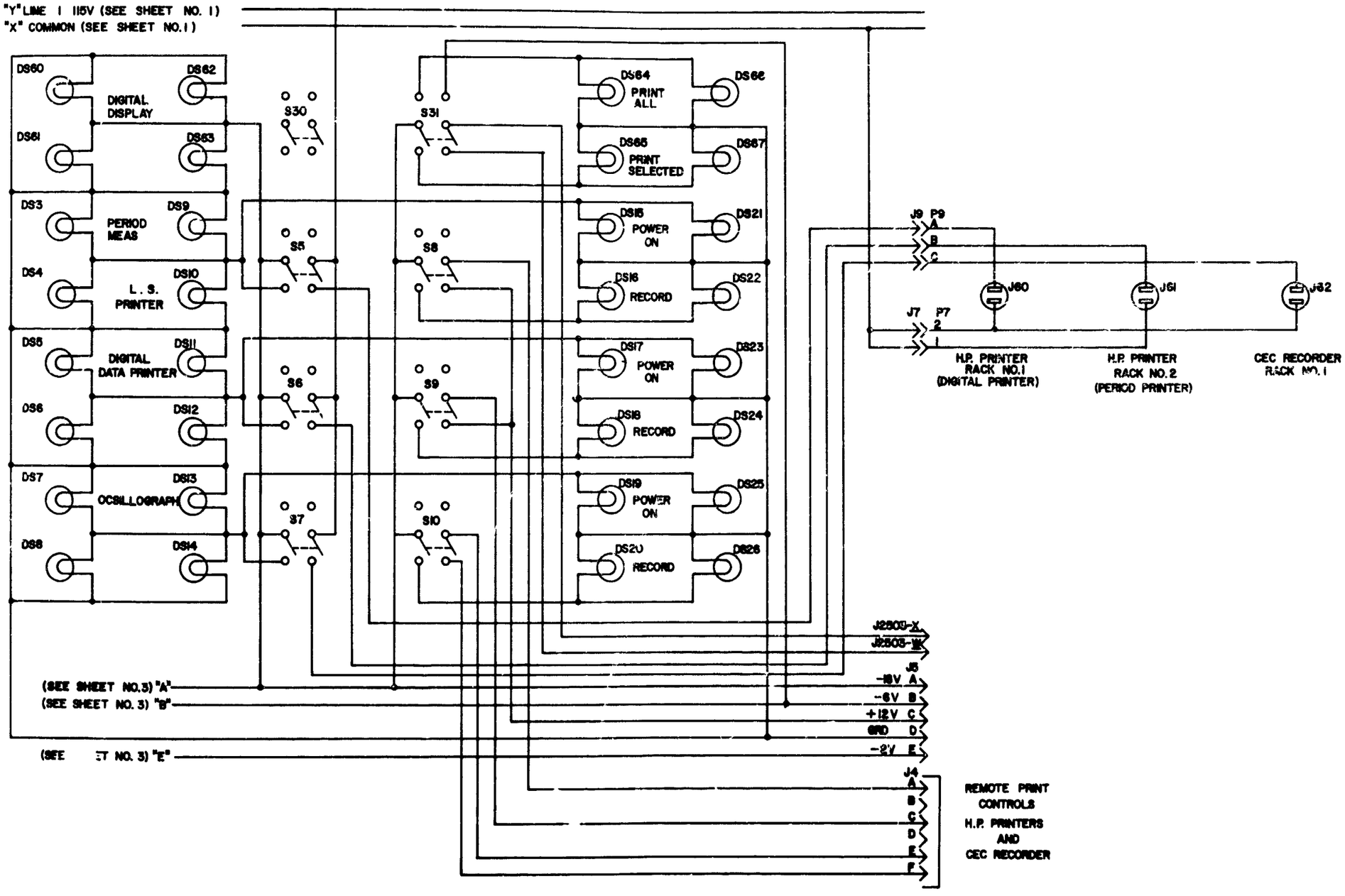


Figure 6-11-1-C Control Panel (sheet 2)

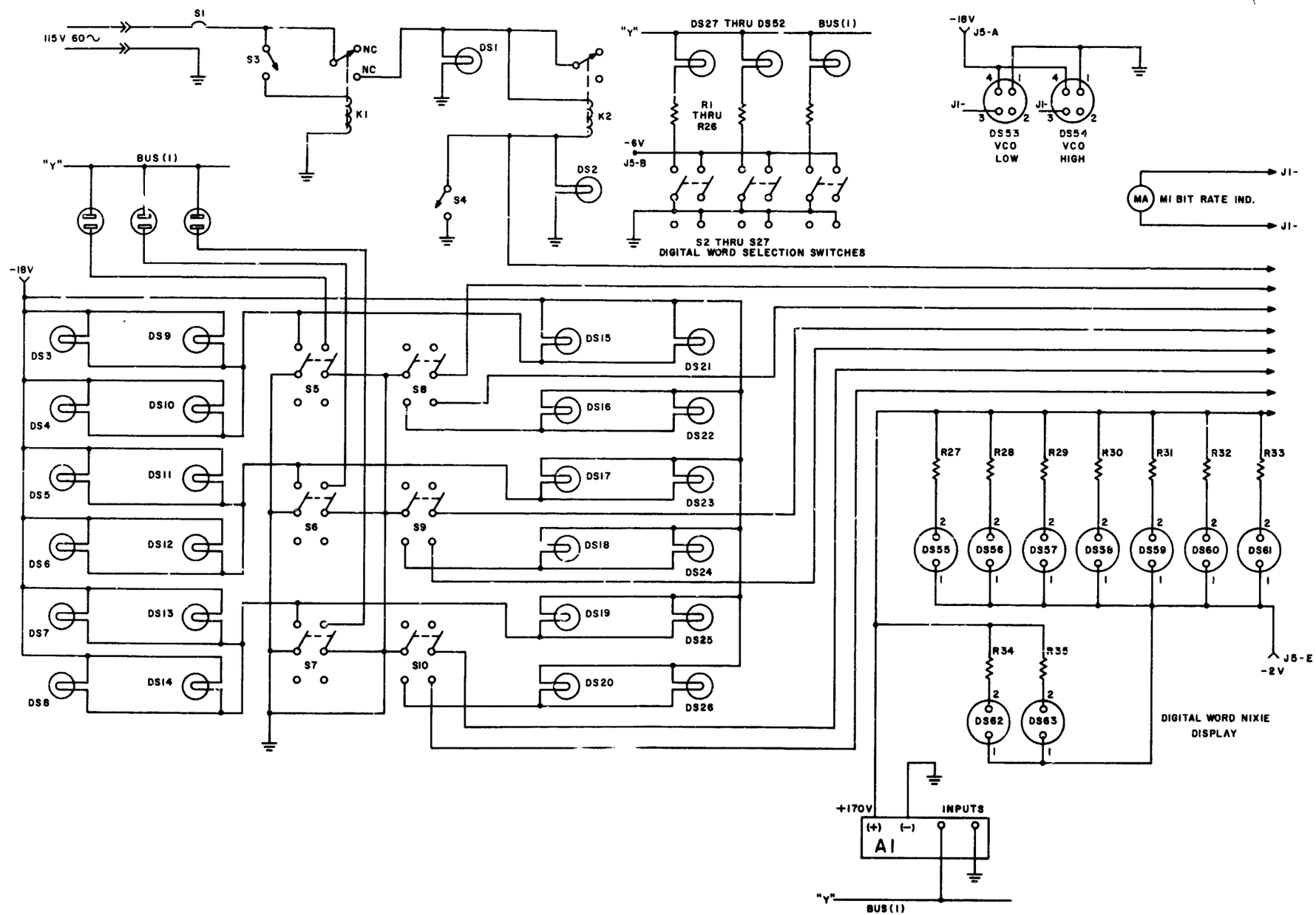


Figure 6-11-1-C Control Panel (sheet 3)

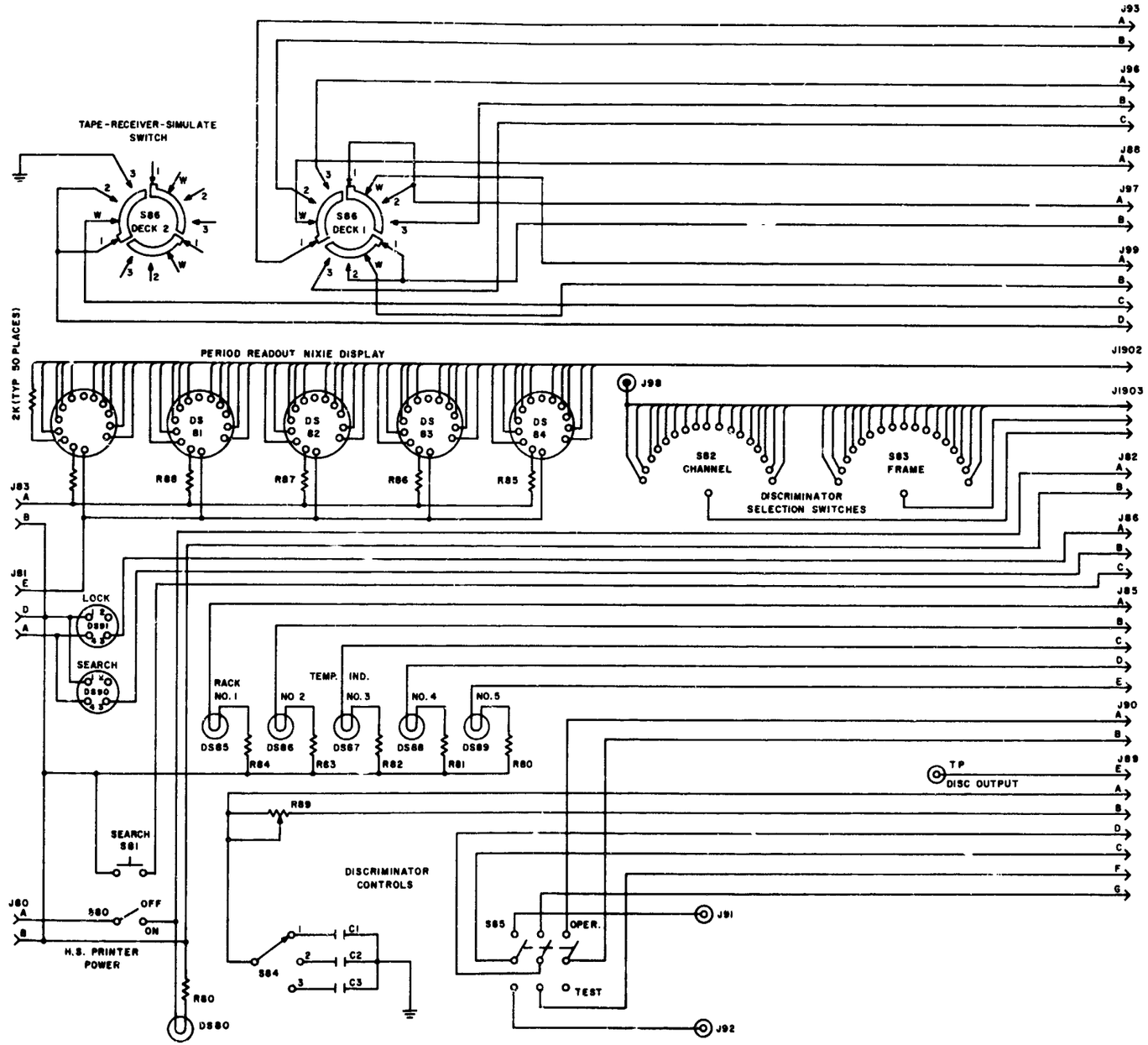


Figure 6-12-2-C Control Panel

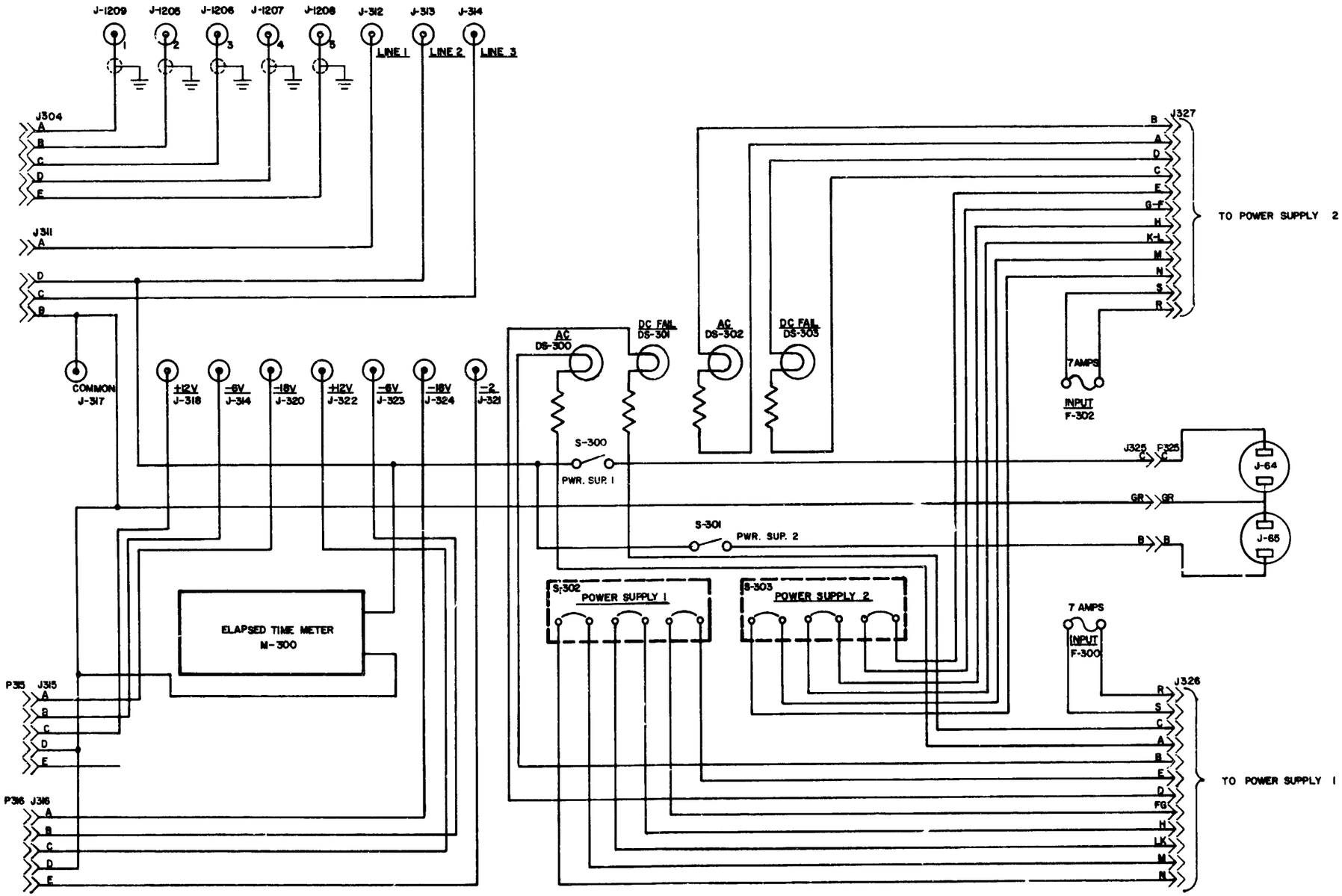
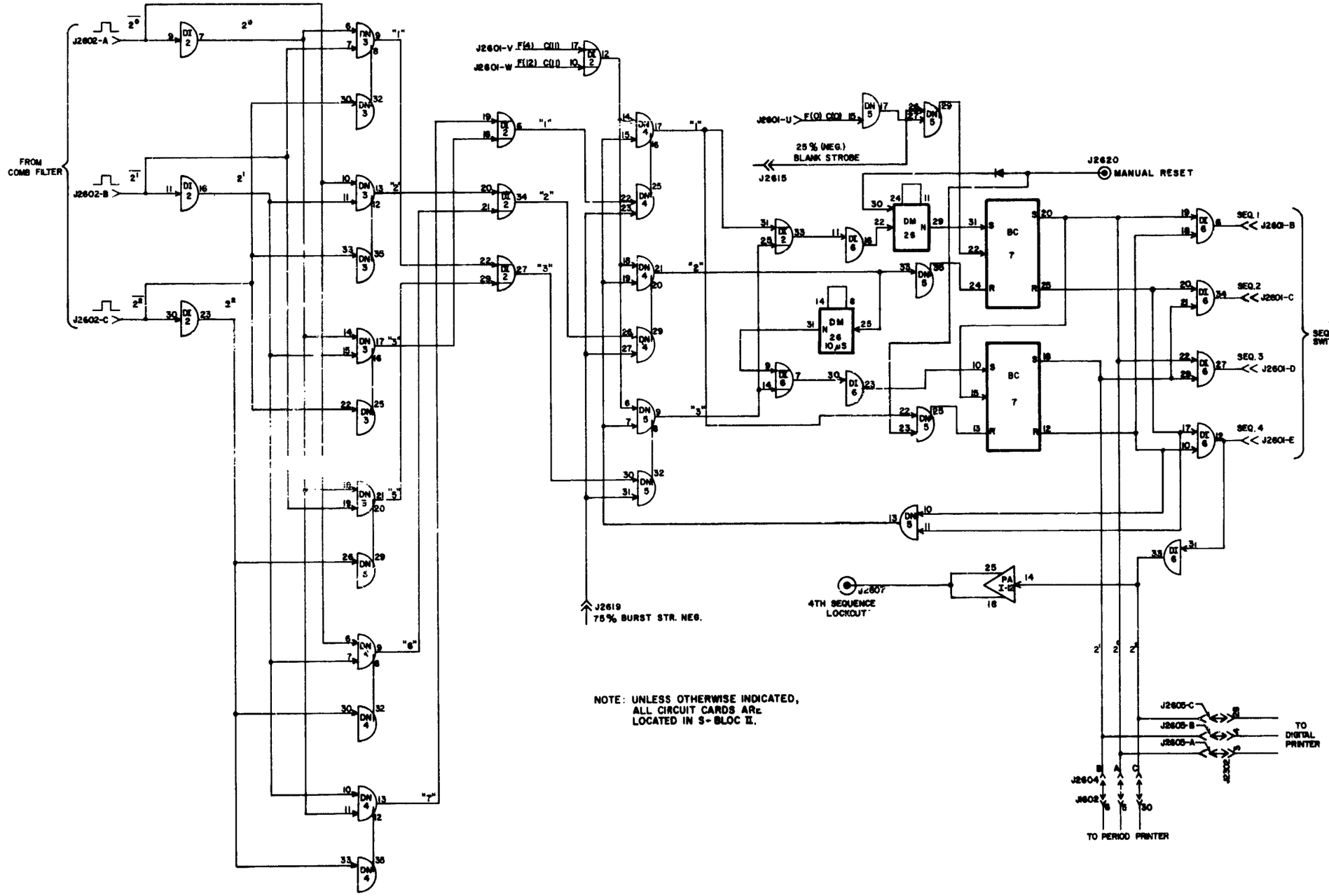


Figure 6-13-3-C Control Panel



NOTE: UNLESS OTHERWISE INDICATED, ALL CIRCUIT CARDS ARE LOCATED IN S-BLOC II.

Figure 6-14–Special Box, Logic Diagram (sheet 1)

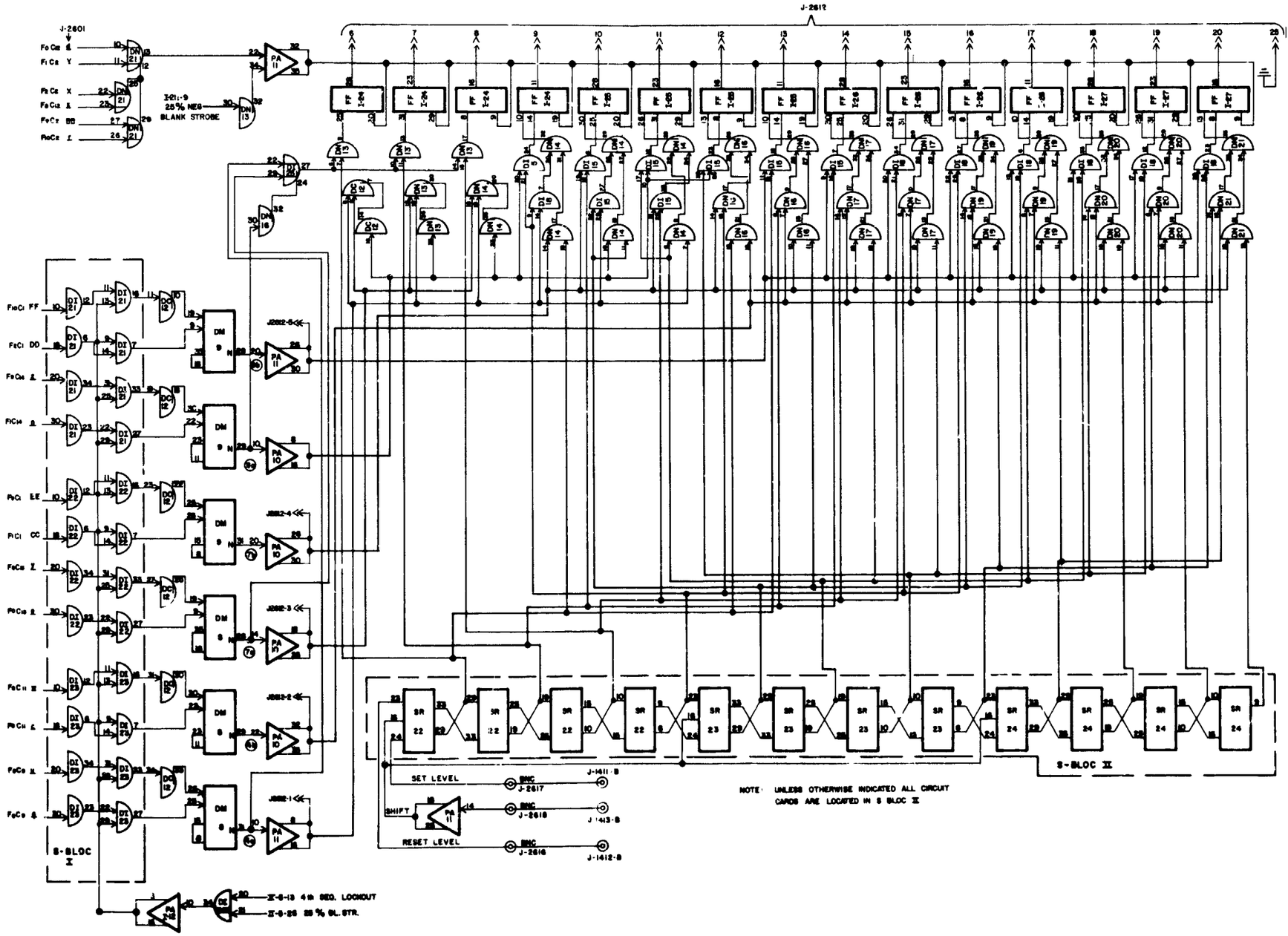


Figure 6-14–Special Box, Logic Diagram (sheet 2)

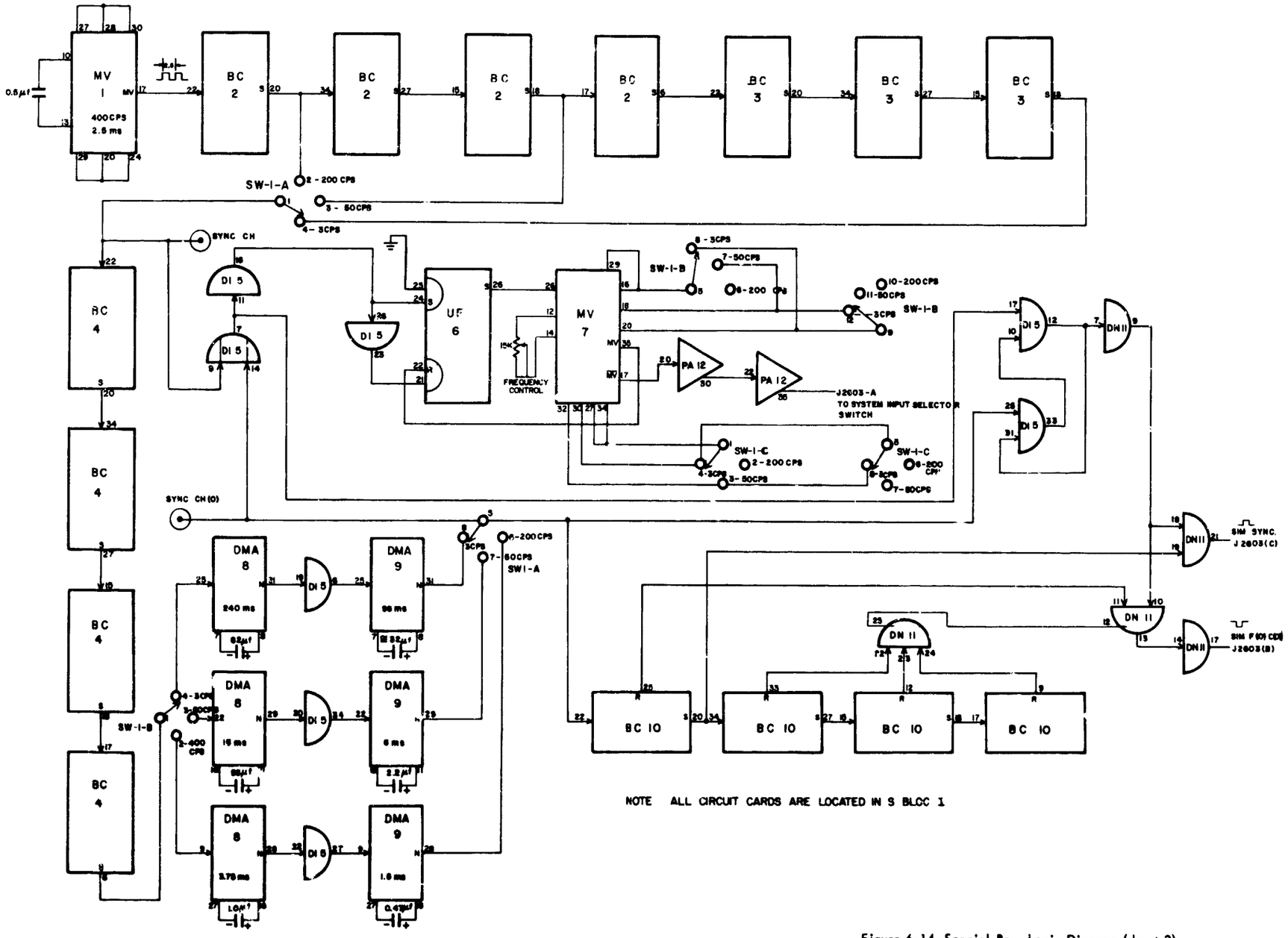


Figure 6-14–Special Box, Logic Diagram (sheet 3)

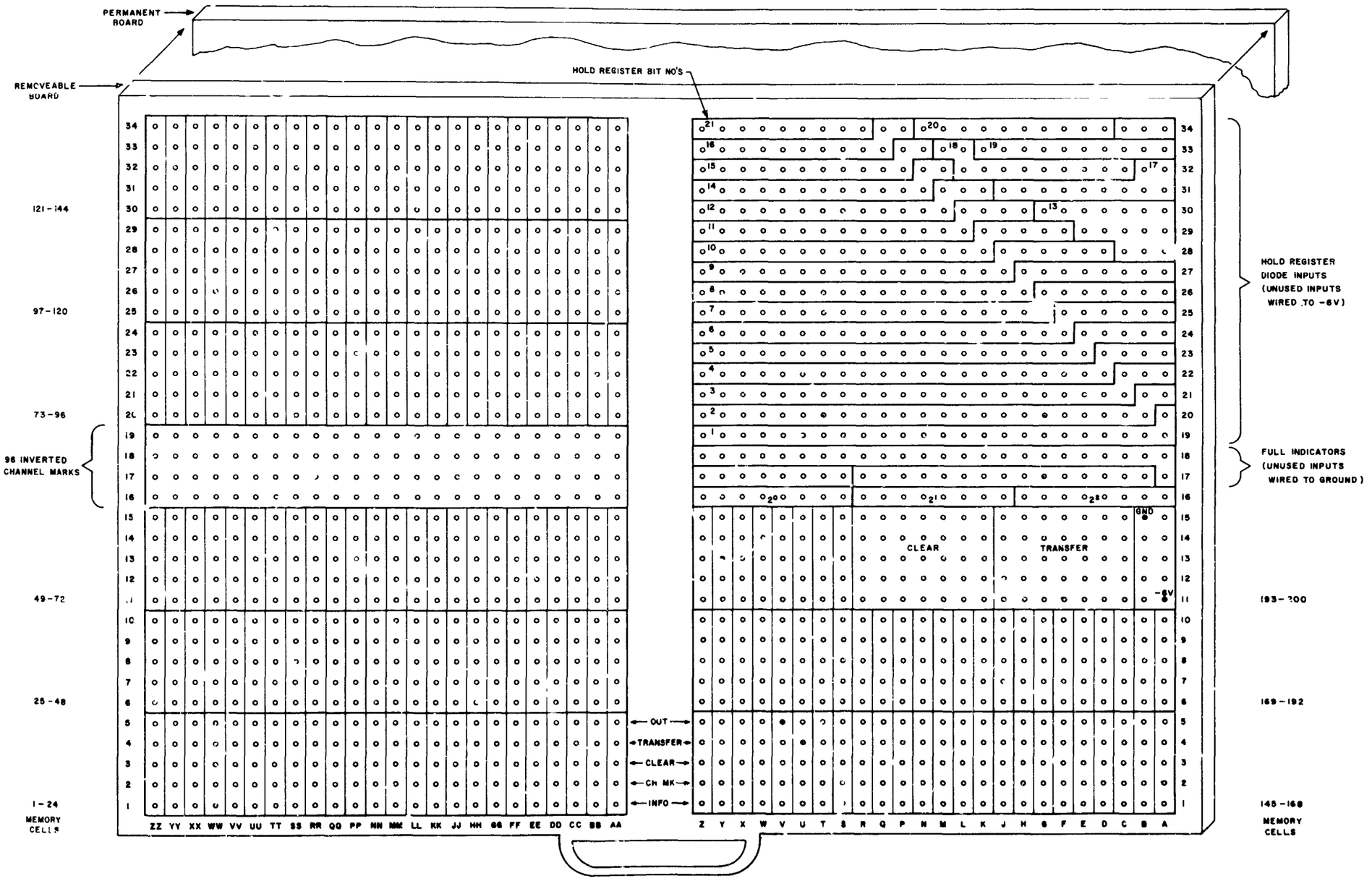
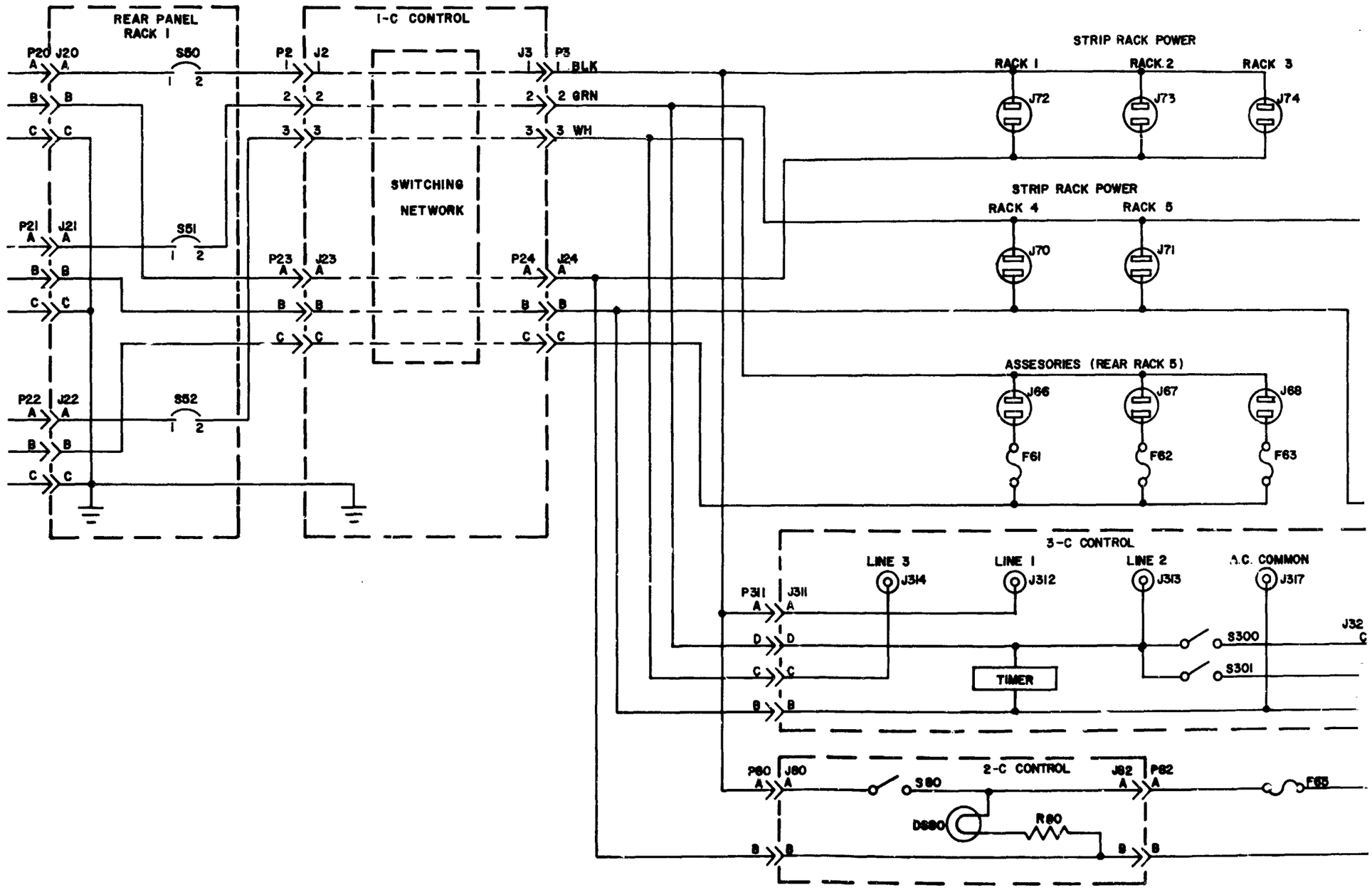


Figure 6-15–Program Board No. 1


REAR PANEL
RACK 1
I-C CONTROL
P20 J20
S50
P2 J2
J3 P3
BLK
2 GRN
3 WH
SWITCHING
NETWORK
P21 J21
S51
P23 J23
P24 J24
P22 J22
S52
STRIP RACK POWER
RACK 1
RACK 2
RACK 3
J72
J73
J74
STRIP RACK POWER
RACK 4
RACK 5
J70
J71
ASSESORIES (REAR RACK 5)
J66
J67
J68
F61
F62
F63
3-C CONTROL
LINE 3
J314
LINE 1
J312
LINE 2
J313
A.C. COMMON
J317
P311 J311
S300
S301
TIMER
J32
P80 J80
2-C CONTROL
J82 P82
S80
F65
D880
R80

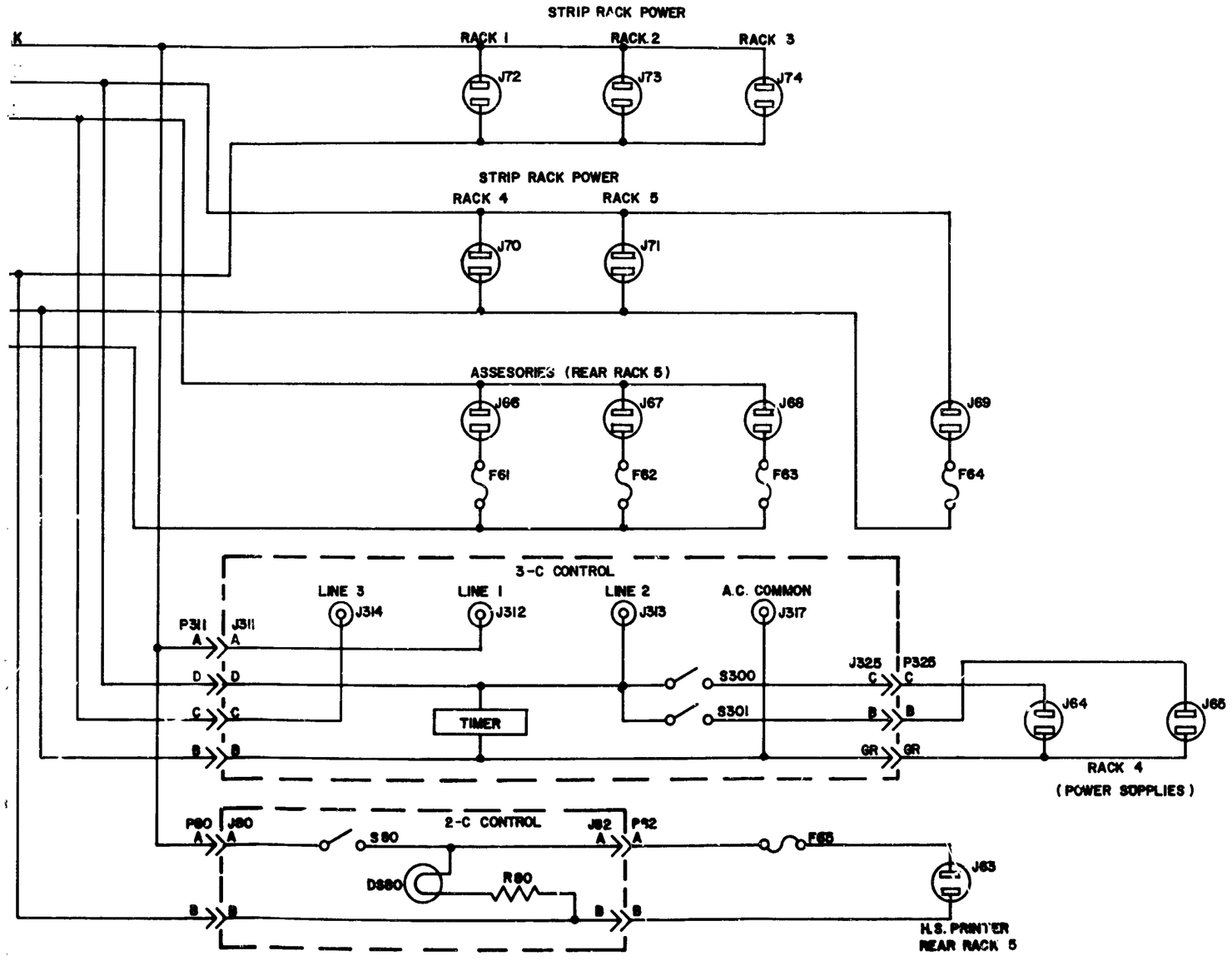


Figure 6-16–Inter-Rack Power Connections

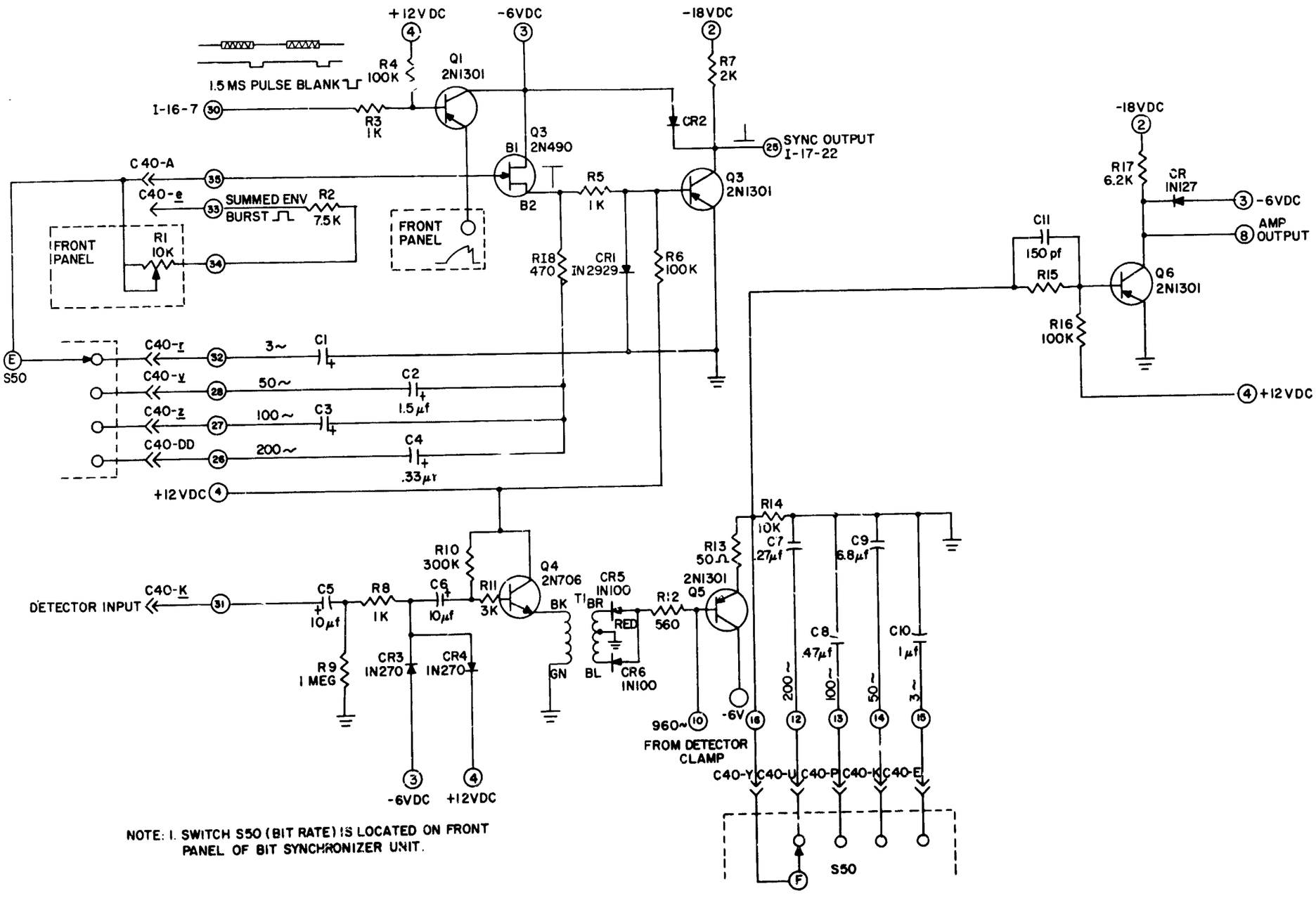
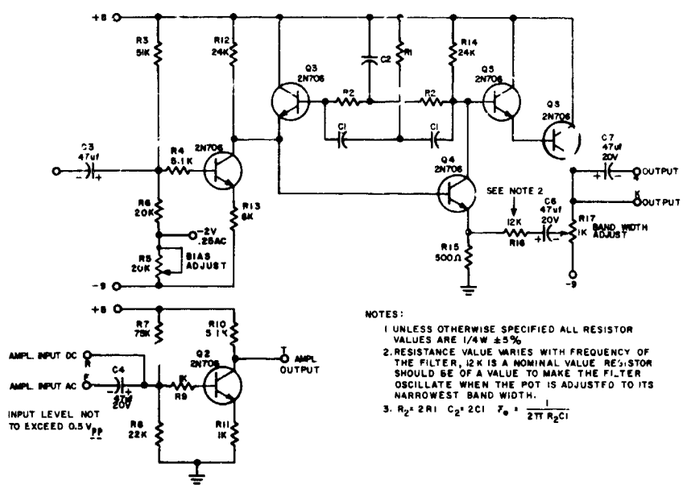


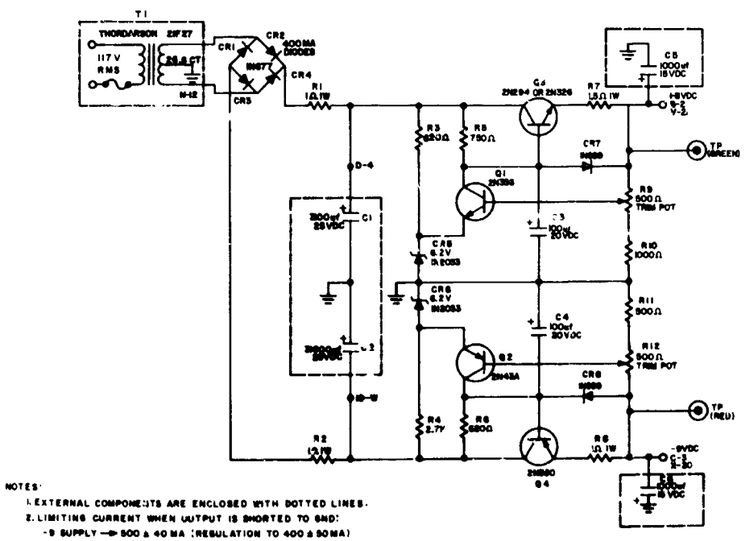
Figure 6-17—Detector, Integrate and Dump Circuit Schematic (sheet 1)



NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE 1/4W ±5%
2. RESISTANCE VALUE VARIES WITH FREQUENCY OF THE FILTER, 12K IS A NOMINAL VALUE RESISTOR SHOULD BE OF A VALUE TO MAKE THE FILTER OSCILLATE WHEN THE POT IS ADJUSTED TO ITS NARROWEST BAND WIDTH.
3. $R_2 = 2R1$ $C_2 = 2C1$ $F_o = \frac{1}{2\pi R_2 C1}$

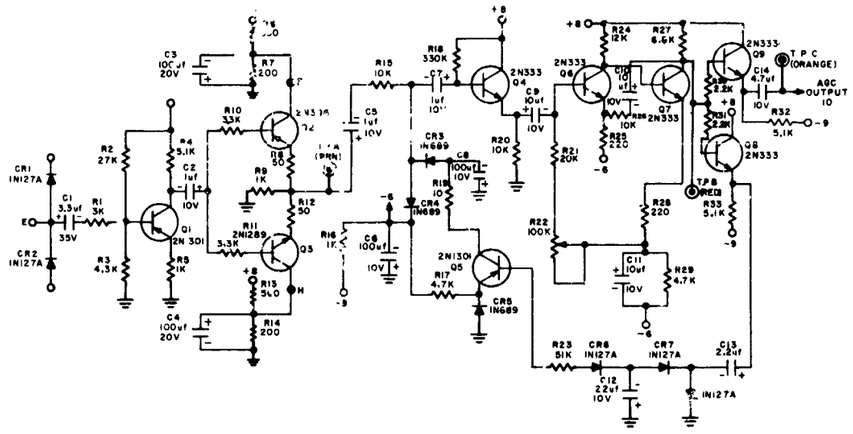
FILTER AND 2X AMPLIFIER



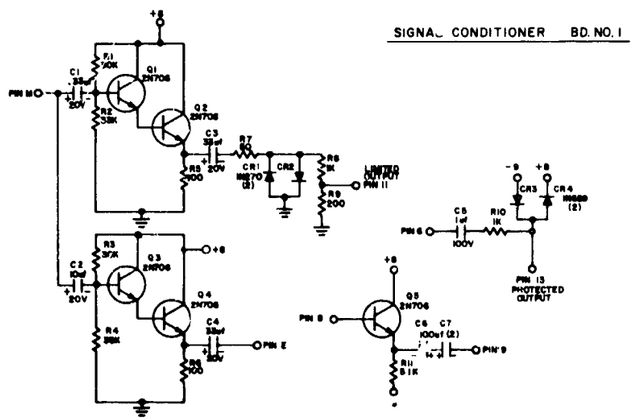
NOTES:

1. EXTERNAL COMPONENTS ARE ENCLOSED WITH DOTTED LINES.
2. LIMITING CURRENT WHEN OUTPUT IS SHORTED TO GND:
   -9 SUPPLY —▶ 500 ± 40 MA (REGULATION TO 400 ± 50MA)
   +8 SUPPLY —▶ 300 ± 50 MA (REGULATION TO 250 ± 50MA)

POWER SUPPLY

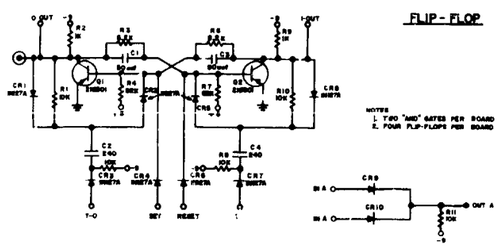


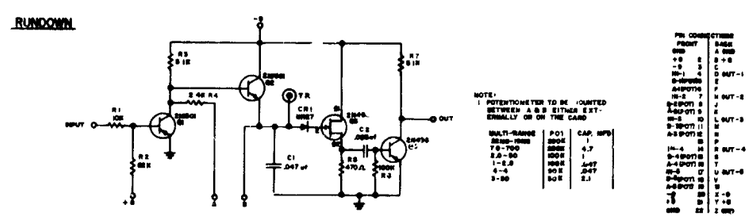
AGC BOARD (INPUT NO. 1C)

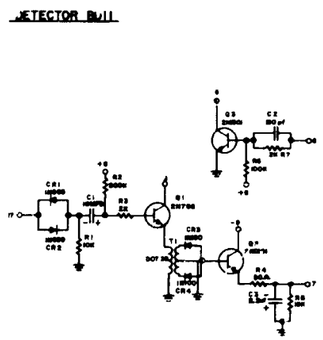


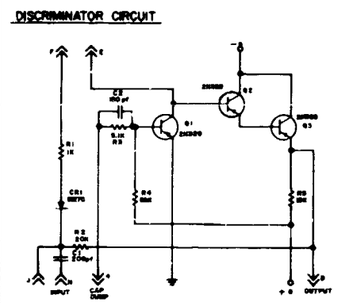
SIGNAL CONDITIONER BD. NO. 1

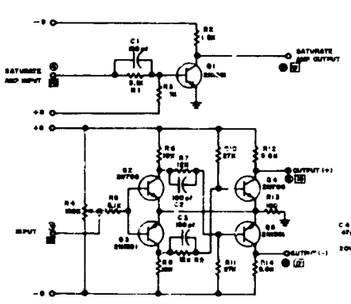
Figure 6-17—Detector, Integrate and Dump Circuit Schematic (sheet 2)











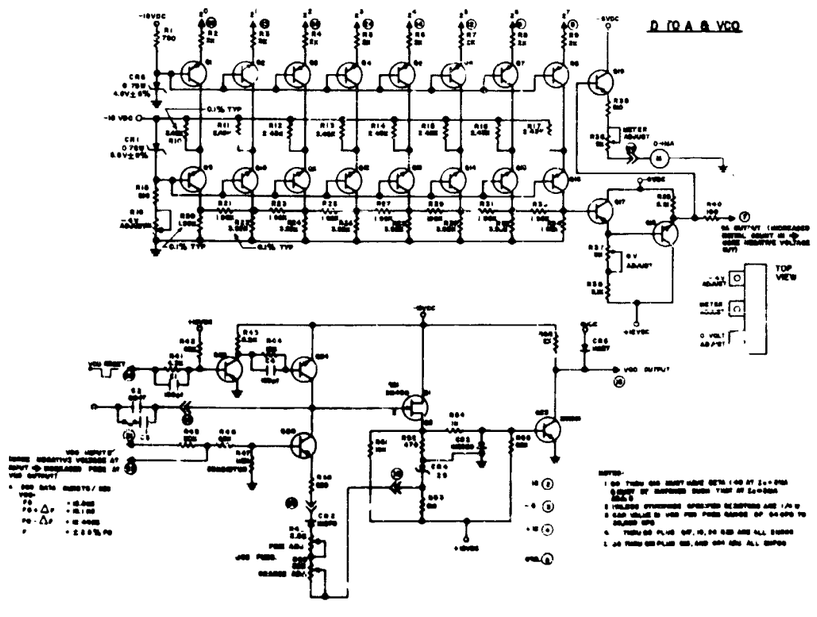
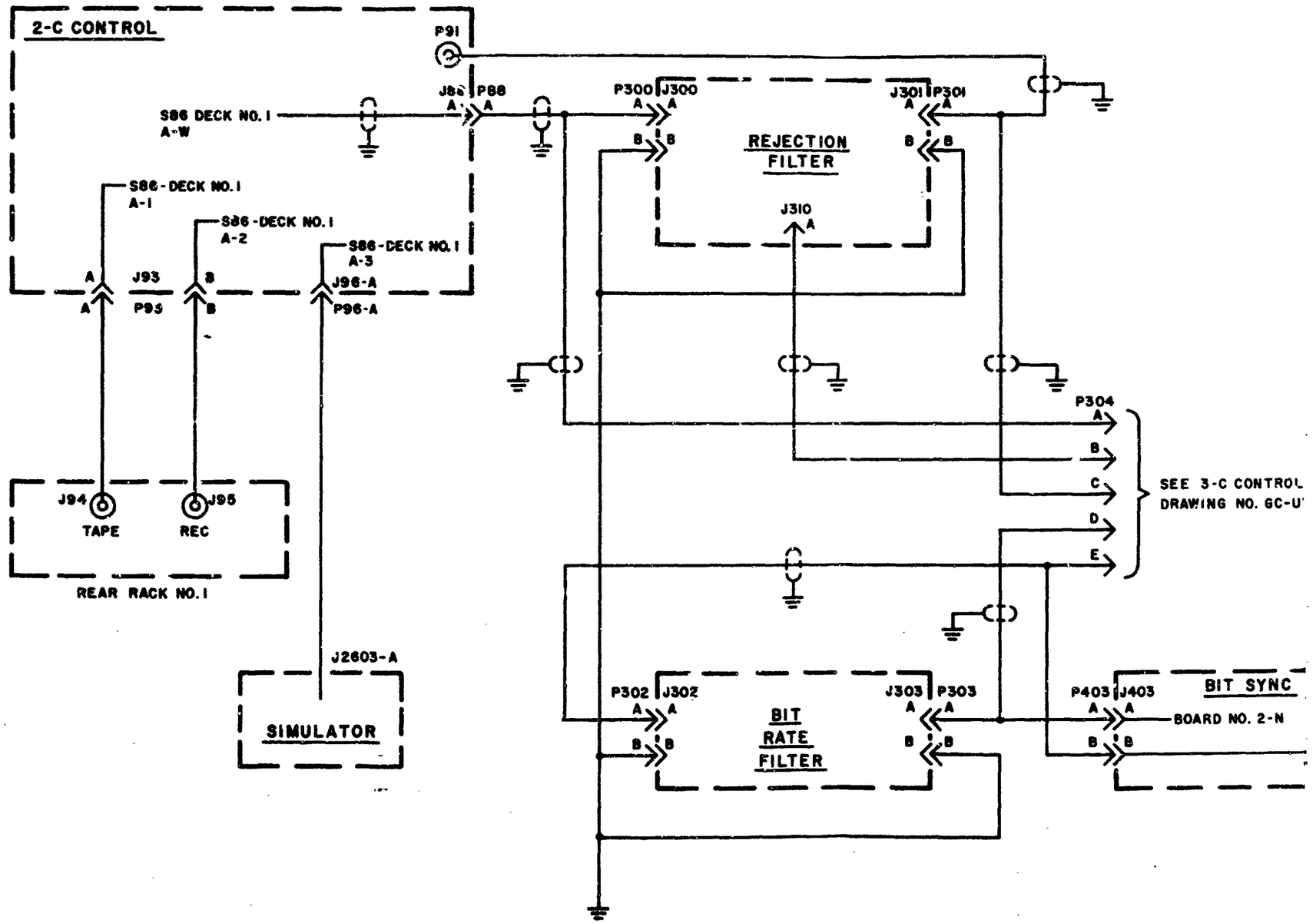


Figure 6-17–Detector, Integrate and Dump Circuit Schematic (sheet 3)


2-C CONTROL
P91
S86 DECK NO. 1
A-W
J88
P88
P300
J300
J301
P301
REJECTION
FILTER
J310
S86 - DECK NO. 1
A-1
S86 - DECK NO. 1
A-2
S86 - DECK NO. 1
A-3
J93
P93
J96-A
P96-A
J94
TAPE
J95
REC
REAR RACK NO. 1
J2603-A
SIMULATOR
P304
SEE 3-C CONTROL
DRAWING NO. GC-U'
P302
J302
BIT
RATE
FILTER
J303
P303
P403
J403
BIT SYNC
BOARD NO. 2-N

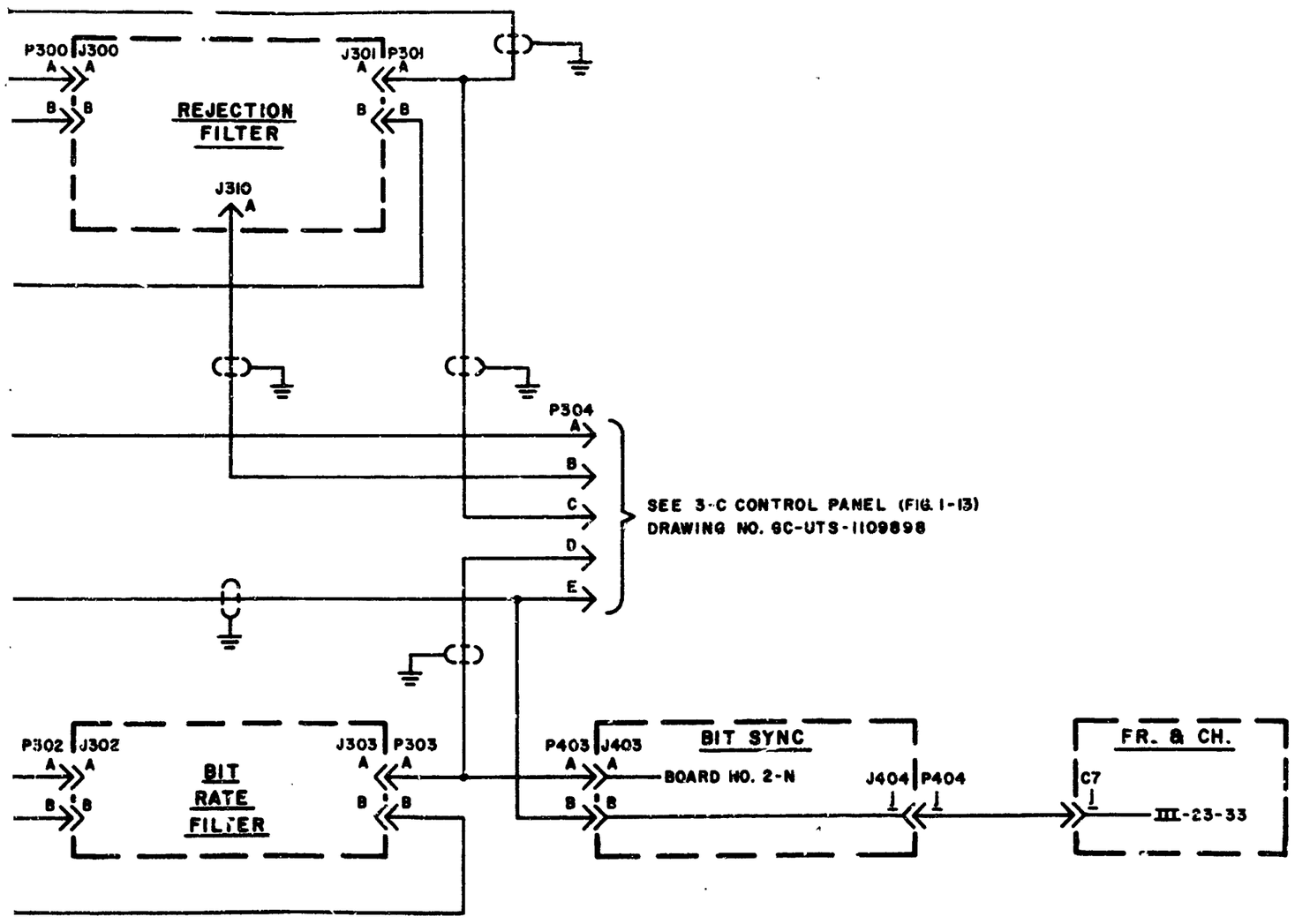


Figure 6-18—Wiring Schematic Filter Connections