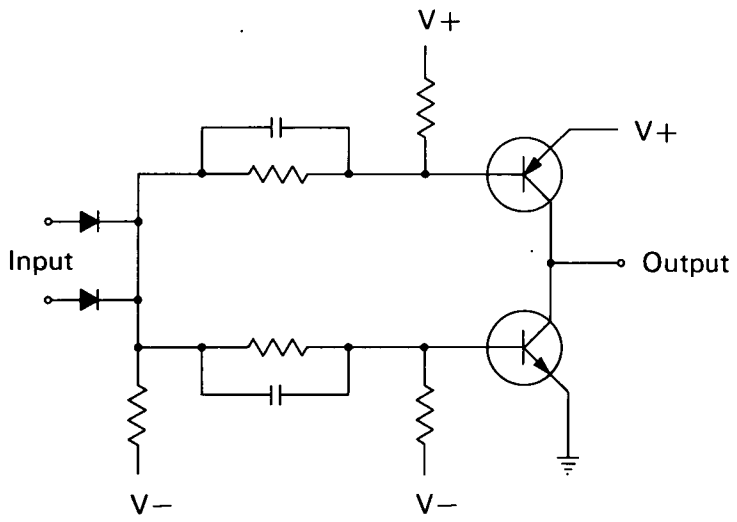
NASA TECH BRIEF

Logic Circuit Exhibits Optimum Performance



The problem: Microelectronic digital circuits are available in many forms of logic and are applicable to many systems used in telemetry and programing. No thorough, comprehensive evaluation of these circuit configurations has been made in terms of power drain, propagation time, or component variations with temperature and load.

The solution: To compare the performance of basic logic circuits to determine the optimum circuit configuration for implementation into microelectronic functions.

How it's done: Seven basic logic circuits were evaluated to determine their performance as NAND and NOR gates, universal flip-flops, and applicable circuits to utilize flip-flops as shift accumulators. The circuits evaluated were Direct Coupled Transistor Logic (DCTL), Resistor-Transistor Logic (RTL), Resistor-Diode-Transistor Logic (RDTL), Emitter Coupled Transistor Logic (ECTL), Transistor-Transistor Logic (TTL), Diode-Transistor Logic (DTL), and Complementary RDTL.

The design constraints imposed on the circuits limited maximum resistance values to 100,000 ohms, power supply voltages to multiples of ±1.35 volts, propagation time to less than 1 microsecond, and repetition rate to 150 kcps.

On the basis of the test results, complementary RDTL offered the best trade-off performance within these constraints and state-of-the-art fabrication technology. This circuit configuration permits NAND and NOR functions to be easily fabricated with similar design and performance characteristics. Switching speeds

(continued overleaf)

are high, and propagation time degrades only slightly at high temperatures. Noise immunity is good. Fan-out requirements impose a high, but not prohibitive beta requirement. Flip-flop power drain is not excessive. AC set and reset are possible, and shift accumulator features are readily available.

Notes:

1. These test results should be of interest to the electronics industry, specifically to designers and manufacturers of integrated digital logic circuits.
2. Inquiries concerning this innovation may be directed to:

   Technology Utilization Officer
   Langley Research Center
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   Reference: B65-10193

Patent status: NASA encourages commercial use of this innovation. No patent action is contemplated.

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