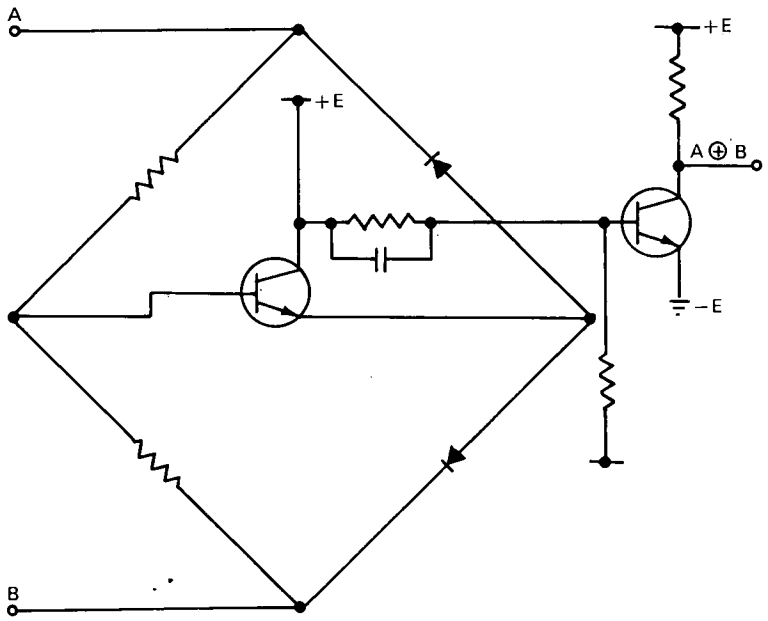
NASA TECH BRIEF

Improved Circuit Minimizes Generation Time of Pseudonoise Check Bits



TWO-VARIABLE MOD-2 CIRCUIT

The problem: To design a computer switching network in which all the check bits in a pseudonoise (PN) sequence are generated in parallel with a minimum propagation time. A PN sequence contains 2^k-1 bits derived from k information or generating bits and is used in certain computer algebraic coding procedures. Excessive computer time is required in earlier designs which use a recycling check bit shift register and an information bit comparator.

The solution: A switching network consisting primarily of parallel and series combinations of modulo 2 (mod 2) adders. This network uses the minimum number of gating levels (hence minimizing the propagation time) and optimally balances the loads on the individual mod 2 circuits.

How it's done: The pseudonoise sequence is described by the recursion formula:

$$X_n = \sum_{i=1}^{k} C_i X_{n-i}$$

where C_i is either 0 or 1, X_n is an information bit, k is the number of information bits, and the sum is obtained by mod 2 addition. For binary digits, this addition is done with *exclusive-or* $\oplus$ logic circuits of the type illustrated. Although in principle any number

(continued overleaf)

(k) of information bits can be processed by an appropriate parallel and series combination of these circuits, the description will be confined to the case of 6 information bits (X_0, X_1, . . ., X_5) for simplicity. In this case, the PN sequence terms or check bits to be generated are (X_6, X_7, . . ., X_{62}) and the recursion relation between the elements of this sequence is:

$$X_n = X_{n-6} \oplus X_{n-5}$$

Using this relation, each of the check bits can be reduced to a mod 2 function of from 2 to 6 of the information bits. Since mod 2 summing is an associative operation, the outputs of the mod 2 functions for two variables can be economically used as inputs to mod 2 functions of higher order. To derive the mod 2 function for 2, 3, 4, 5, and 6 variables, a two-term mod 2 circuit may be cascaded in one of several ways. The deciding factors are minimum propagation time and optimal load balance on the individual mod 2 circuits.

Note:

Inquiries concerning this invention may be directed to:

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Patent status: NASA encourages the immediate commercial use of this invention. It is owned by NASA and inquiries about obtaining royalty-free rights for its commercial use may be made to NASA, Code AGP, Washington, D.C., 20546.

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