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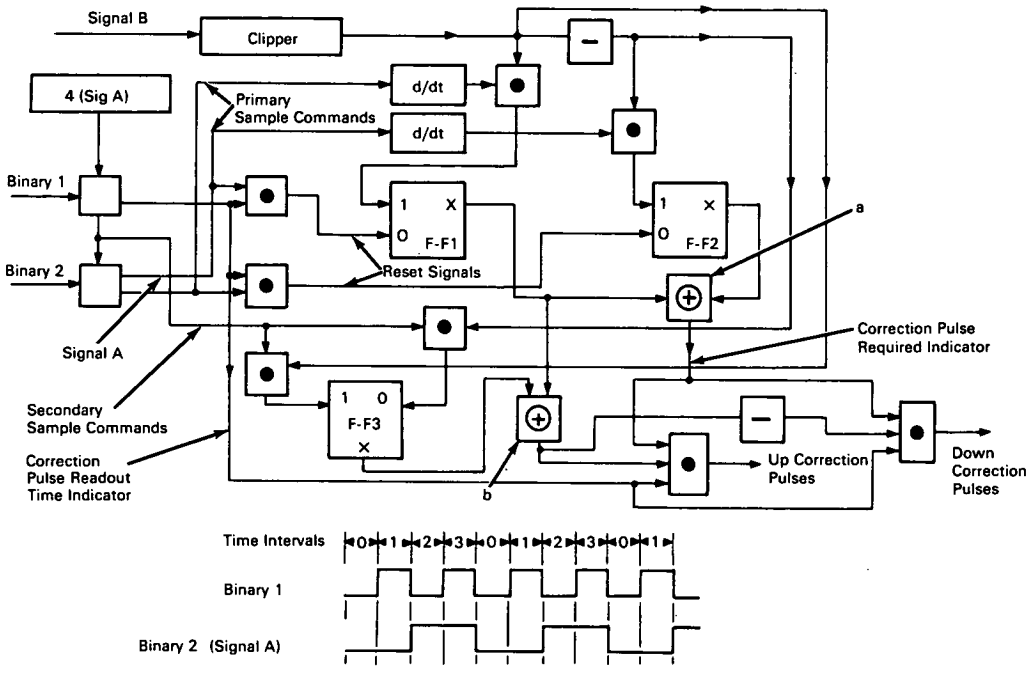
NASA TECH BRIEF

Frequency Correction Device Uses Digital Circuitry



The problem: To design a circuit that generates correction signals to control the frequency of a voltage-controlled oscillator in a system used to acquire and track incoming signals over a wide range of frequencies.

The solution: A digital circuit that samples the frequency of the incoming signal at prescribed time intervals and provides correction pulses to the voltage-controlled oscillator.

How it's done: The voltage-controlled oscillator signal, A, controls a sampling circuit that samples the incoming signal, B, once every half cycle of signal A (primary samples). If the frequencies of the two signals are exactly the same, no correction pulses are produced. If they are not the same, secondary samples taken at intermediate time intervals determine whether correction pulses should be generated to make signal A oscillate at the same frequency as signal B. As indicated in the block diagram, the basic oscillator puts out pulses at a frequency four times that of signal A itself to facilitate the application of necessary logic. This "times four" signal is counted down by the two counter stages (binary 1 and binary 2). The state of these binaries as a function of time interval is graphed below the block diagram. Primary samples are taken

(continued overleaf)

and remembered by the flip-flops during time intervals 0 and 2. During time intervals 1 and 3 one of the two flip-flops is being reset. If the frequencies of signals A and B are the same, both flip-flops (F-F) 1 and 2 will either be positive or negative during time intervals 0 and 2, and there will be no output from the *exclusive or* circuit *a*. In the absence of an output from this circuit, there will be no "up" or "down" correction pulses. When flip-flops 1 and 2 have opposite outputs, correction pulses are needed, and there is an output from circuit *a*. A half cycle prior to this instant, flip-flop 3 samples the signal, and *exclusive or* circuit *b* determines whether an "up" or "down" correction pulse is needed. The inputs to *b* are the samples taken at the beginning of time interval 0 and remembered on flip-flop 1 as well as the samples taken either at the beginning of time interval 1 or 3 and remembered on flip-flop 3. If this comparison is made during time interval 0, the secondary sample obtained at the beginning of time interval 3 is used. If the comparison occurs during time interval 2, the secondary sample at the beginning of time interval 1 is used. When the two samples are the same, the "down" correction pulse *and* gate has an input. When the two samples are different, the "up" correction pulse *and* gate has an input. The "correction pulse readout time indicator" line has an output only during time intervals 0 and 2, so that correction pulses can appear only in these intervals. The correction pulses are sent to an integrator which controls the oscillator.

Notes:

1. When noise is present on the input signal the "up" and "down" correction pulses must be processed by additional circuitry which allows an output only when a certain minimum number of sequential "up" or "down" correction pulses are counted. With this addition, the system will operate effectively when the noise voltage is twice that of the true signal voltage.
2. The circuit may also be used as a sensing device to indicate whether a signal is present on one of several input lines.
3. Inquiries concerning this invention may be directed to:

   Technology Utilization Officer
   Goddard Space Flight Center
   Greenbelt, Maryland, 20771
   Reference: B65-10307

Patent status: NASA encourages the immediate commercial use of this invention. Inquiries about obtaining rights for its commercial use may be made to NASA, Code AGP, Washington, D.C., 20546.

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