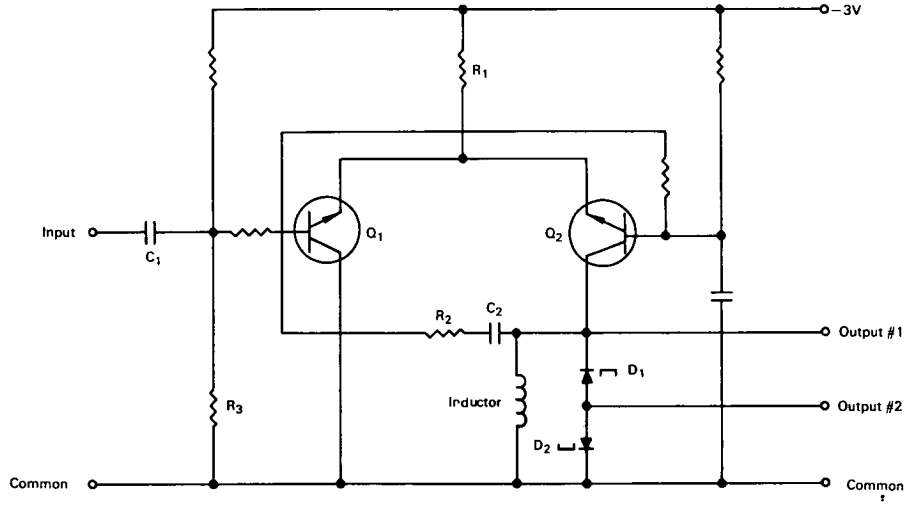
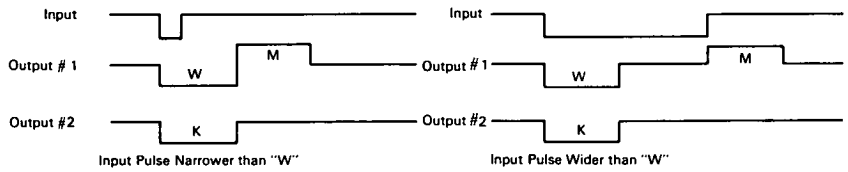
# NASA TECH BRIEF



## Hybrid Circuit Achieves Pulse Regeneration with Low Power Drain




**The problem:** To provide a solid-state, low power drain pulse regenerator circuit capable of output pulse widths as narrow as 100 nanoseconds and independent of input pulse widths. Present circuits differentiate the input pulse, triggering a pulse generator for regeneration, and use gates and timing circuits for frequency limiters and gated oscillators. This circuitry is relatively complex and is characterized by heavy power drain when working with narrow pulses.

**The solution:** A hybrid tunnel diode-transistor circuit forming a solid-state, low power drain pulse regenerator, frequency limiter, or gated oscillator.

**How it's done:** The two transistors form an emitter-follower differential amplifier. Transistor $Q_1$ is normally biased on and $Q_2$ is normally biased off. Bias current through $R_1$ is about 1.5 times that required to trigger tunnel diodes $D_1$ and $D_2$. A negative input pulse turns $Q_1$ off and $Q_2$ on, thus triggering $D_2$ into its high-voltage state. As $Q_2$ is initially turned on, the inductor presents a high impedance, channeling the $Q_2$ collector current through $D_1$ and $D_2$. When current through the inductor increases sufficiently, $D_2$ returns to its low-voltage state and this produces output $W$ whose width is determined by the value of the inductor. Capacitor $C_2$ and resistor $R_2$ form a feedback

(continued overleaf)

loop to hold $Q_1$ biased off. When the input pulse width is smaller than $W$, the feedback voltage falls to zero and resets the amplifier ($Q_1$ on and $Q_2$ off). Continued current flow through the inductor causes $D_1$ to remain in the high-voltage state until the current decays, at which time $D_1$ returns to its low-voltage state, yielding output pulse $M$ (width of $M \approx$ width of $W$). If the input pulse is wider than $W$, the input signal is still present when the feedback voltage drops to zero, thus sustaining current flow through the inductor. The signal pulse $K$ is generated at output number 2 for each input pulse, independent of input pulse width.

**Notes:**

1. When the feedback voltage exceeds the input voltage the circuit will function as either a pulse normalizer or a frequency limiter. If the input pulse period is greater than time $W + M$, the circuit functions as a pulse normalizer. If the input pulse period is less than time $W + M$, the circuit functions as a frequency limiter.
2. If the circuit is direct coupled ($C_1$ replaced by a resistor), it will function as a gated oscillator. In this mode, $R_3$ should be replaced by a tunnel diode to limit input voltage.
3. Input-output polarity combinations are only limited by the choice of NPN or PNP transistors plus connection polarity of the tunnel diodes.
4. Inquiries concerning this invention may be directed to:

   Technology Utilization Officer
   Goddard Space Flight Center
   Greenbelt, Maryland, 20771
   Reference: B65-10314

**Patent status:** NASA encourages the immediate commercial use of this invention. Inquiries about obtaining rights for its commercial use may be made to NASA, Code AGP, Washington, D.C., 20546.

Source: Ciro A. Cancro
(GSFC-382)