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OPTIMIZATION STUDY OF HIGH POWER STATIC INVERTERS AND CONVERTERS

By

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Prepared For

National Aeronautics and Space Administration

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TRW ELECTROMECHANICAL DIVISION
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CLEVELAND, OHIO 44117

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QUARTERLY REPORT #2

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SUMMARY

This is the second quarterly report of the Optimization Study of High Power Static Inverters and Converters. Work on this study began August 1, 1963. This report covers the period from November 1, 1963 through January 31, 1964.

Topics covered in this report include an analytical study of the optimization of transformers, an investigation of inverter circuits using three-phase transformers, investigation and comparison of several techniques for paralleling transistors and comparison and discussion of inverter designs at the 10 KW 3200 cycle level using both silicon transistors and SCR's.

INTRODUCTION

The first quarterly report contained, along with a general discussion of the various types of inverter circuits and examples of the techniques used in their detailed analysis, a preliminary discussion of the specific problems involved in the selection of a design for the 3200 cycle, 10 KW inverter. The results indicated that no technique or switching device possessed a clear advantage, although it was possible to eliminate some methods.

Accordingly, this report contains the results of a more detailed study made to determine quantitatively the relative merits of each scheme. Items discussed include the design and utilization of iron core components, circuits using three-phase transformers, the internal impedance of power switching stages and filters, feedback techniques for minimizing drive requirements and methods of incorporating redundancies in the power stages for reliability improvements. Although these areas were investigated as an aid in optimizing the 3200~ inverter, the results can be applied either directly or with simple and obvious modifications to the other (400~) designs.

In the design of inverters operating at high DC input currents ($>$ 50 amp) the choice of switching elements is made difficult by the fact that SCR's, while capable of handling large currents (250 A avg) in a single unit, are somewhat temperature and frequency limited, provide only moderate

efficiencies, and present a significant "in-use" reliability problem because of the difficulty in turning them off. Transistors, on the other hand, can provide higher efficiency (germanium) or higher temperature operation (silicon) and freedom from turn-off problems; but, because of their limited current capability (50 A) require considerable paralleling with its attendant complexity and increase in parts count in order to handle the necessary currents. (The reader is referred to the first quarterly report of this series, pages 105-125, for a more detailed discussion of these trade-offs).

In order to provide a more definite basis for comparison between the various approaches, inverters utilizing both SCR's and transistors were designed and analyzed in detail. Different circuits were used for the different switching elements, in order to make fullest use of the advantages offered by each. The philosophy behind the selection of each "best" circuit as well as analysis and discussions of those circuits rejected is given in the following section.

Because weight and efficiency are of considerable importance in aerospace inverters, major investigative efforts were directed toward those areas which account for most of the weight and losses in typical inverters. These areas are the output transformers and filters, and the power switching devices (and their drive circuitry, in the case of transistors).

MAGNETIC COMPONENT STUDIES

Optimum magnetic design requires not only optimization of the individual magnetic components (transformers, inductors, etc.) of any given system but also, of equal importance, an optimum choice of the overall system to be used to perform the specified function. (For example, it will be shown that for purposes of paralleling transistors, under some conditions the use of the split transformer technique is superior to the balancing reactor approach from a weight and loss viewpoint. Clearly, when these conditions are encountered, regardless of how well the balancing reactors are designed, their use will result in a poorer overall system than could be obtained by other means.) What is optimum will depend on the specific application since in general, weight and losses cannot be simultaneously minimized.

To obtain quantitative means for optimizing a system of magnetic components, it is first necessary to determine the characteristics of each component in the system as one or more of its parameters is varied. Accordingly, the transformer (as a typical and common magnetic component) was analyzed to see how its weight and efficiency varied with the size and design. In particular, analyses were made of:

1) The optimum design of a transformer of fixed size to operate at a given power rating.

2) The variation of the size, weight, and losses of such a transformer as its rating is varied.

3) The relationship between the size and losses of a transformer operated at constant power.

4) The thermal problems in transformers.

The results obtained from these analyses were then used to investigate the relative merits of several common inverter circuit techniques. The areas investigated were:

1) The weight and loss penalties for using switching elements that must be paralleled.

2) A comparison between different techniques for paralleling. (Balancing reactors versus the split transformer technique.)

3) The use of multiphase transformers to provide simultaneous weight and harmonic reduction.

These analyses and the results obtained from them follow. The mathematically more involved sections are found in the Appendices 2-I through 2-III.

I. Optimum Loading of a Fixed Transformer

The general rule regarding the optimum loading of a transformer is that maximum efficiency occurs when the copper loss and core loss are equal.

This result, which is derived in Appendix 2-I under the assumption that the primary copper loss due to transformer magnetization current may be neglected, can be expressed mathematically as

$$\frac{P_c}{P_r} = 1 \qquad (2\text{-}1)$$

where P_c is the total core loss (hysteresis, eddy current, interlaminar and stray losses) and P_r is a total copper loss (and includes, where applicable proximity and skin effects but not, as indicated above, the copper losses due to the component of the primary current which serves to magnetize the core.) This derivation, however, was based on the conditions of a constant input voltage and variable load. In practice, however, both the input voltage and maximum design load are generally fixed, and all that the transformer designer can vary is the overall size and/or shape of the transformer and the relative losses in the coil and core.

To start, it will be assumed that the size and shape of the transformer are fixed, and only the relative core and coil losses can be varied. For a core of fixed size and given material, operating at a constant frequency, the only way in which the core losses can be reduced is to reduce the

induction level to which the core material is operated. With a fixed size and voltage input, this can only be accomplished by increasing the number of turns on the primary (and hence, in order to maintain the required turns ratio, the secondary turns must be correspondingly increased).

A decrease in core loss in a constant size transformer is thus obtained at the expense of increased copper losses, since not only is the number of turns increased (increasing the winding resistance) but also with the total area available for winding remaining constant, the available cross-sectional area for each turn decreases.

Taking these effects into account, and making use of the approximate empirical relationship

$$P_c = c_1 B^a \qquad (2\text{-}2)$$

where P_c is the core loss/unit volume , B = maximum flux density the core reaches, and c_1 and a are constant (for any given core material and operating frequency), it is shown in Appendix 2-I that the optimum ratio between core loss and copper loss is given by the equation

$$\frac{P_c}{P_R} = \frac{2}{a} \qquad (2\text{-}3)$$

where P_c and P_R are defined as for Equation (2-1).

The relative losses in equal size and weight transformers carrying the same VA with one designed according to Equation (2-1) and the other designed according to Equation (2-3) are computed in Appendix 2-I and the results plotted in Figure 2-1. From this it can be seen that except for the case where $a = 2$ (where the two designs are equivalent), the losses in a transformer designed with equal copper and core loss will be greater than those in a transformer designed for a core loss $2/a$ times the copper loss. The actual differences in loss are not very great, however, as can be seen from Figure 2-1. When these loss variations are translated into efficiency variations, the difference is further suppressed, as shown in Appendix 2-I.

II. Scaling of Transformers

Once an optimum transformer is designed at a given power level, and its weight and losses determined, it is often useful to be able to scale the size of the transformer up and down and thus obtain new designs without extensive calculations. A decision on the various possible methods of paralleling can only be answered with a knowledge of the total transformer weights and losses in the different schemes. Therefore, some useful equations for the scaling of transformers will be developed here. These equations are strictly true only when used to compare transformers of similar construction operating at the same core flux density and copper current density levels.

Consider a transformer with linear dimension L. The window area available for the coils, A_W, is given by $A_W \propto L^2$. For operation at any fixed current density, the cross-sectional area of each turn, A, is directly proportional to A_W and inversely proportional to N, the total number of turns. Also, the current, I, that can be carried in each wire is proportional to the cross-sectional area of that wire. Writing these relations in equation form there results:

$$A_w \propto L^2, \quad A \propto \frac{A_w}{N}, \quad I \propto A \quad \therefore I \propto \frac{A_w}{N} \propto \frac{L^2}{N} \tag{2-4}$$

Therefore, the ampere turn (NI) capability of the coil is given by

$$NI \propto N\left(\frac{L}{N}\right)^2 = L^2 \tag{2-5}$$

When operating at any fixed value of maximum flux density, the volt/turn which the transformer can support is directly proportional to the core cross-section, which is proportional to L^2. Therefore

$$\frac{V}{N} \propto L^2 \tag{2-6}$$

The volt-ampere rating of the transformer is thus given by:

$$VI = \frac{V}{N}(NI) \propto L^2(L^2) = L^4 \tag{2-7}$$

In other words, the rating of a transformer is proportional to the fourth power of its linear dimension. Its weight, W, on the other hand, is

directly proportional to the volume, which is proportional to the cube of its linear dimension.

$$W \propto \text{volume} \propto L^3 \qquad \text{or} \qquad W \propto L^3 \tag{2-8}$$

(Actually, the weight equals (volume of iron x density of iron)+(volume of copper x density of copper), but under the assumptions of the problem, the ratio of the volume of iron to volume of copper remains constant, hence the weight is proportional to the overall volume, even though this volume contains substances of different densities.)

One possible figure of merit for a transformer, its power/weight ratio, s then given by

$$\frac{\text{power}}{\text{weight}} = \frac{VI}{W} \propto \frac{L'}{L^3} = L \tag{2-9}$$

Thus, the figure of merit for a transformer is proportional to its linear dimension.

By combining 2-7 with 2-8, the relationship between weight and power rating may be determined as follows:

$$VI \propto L^4 \propto (W^{1/3})^4 = W^{4/3}$$

or

$$W = k\,(VI)^{3/4} \tag{2-10}$$

Or, the power handling capability of a transformer is proportional to th 4/3 power of its weight, where k is a constant of proportionality.

For the conditions under which the previous equations were derived (namely, constant current density in the windings and constant flux density in the core) the loss per unit volume (or weight) remains constant in all transformer sizes; thus, the total losses are directly proportional to the weight. Or re-writing equation 2-10 after substituting losses for weight, there results

$$\text{Loss} \propto (\text{VI})^{3/4} \qquad (2\text{-}11)$$

The relationships between the size, weight, and losses of scaled transformers have thus been derived. It should be mentioned that in order for these relations to hold, the scaled transformers should all be similar - that is, all their (linear) dimensions should be changed in the same ratio. This is not a difficult restriction to meet in practice since, for example, all transformers made from a square stack of scrapless E-I laminations (which are all constructed with the same ratios) and having the available window area completely filled with wire would fall into this category. Of course, the conductor and core material must be the same for all the transformers. This analysis holds for either toroidal or laminated cores, single or three phase transformers, as long as the similarly condition is met.

In general, smaller transformers may be designed with higher current and flux densities than larger ones due to the fact that it is easier to get

the heat out of a smaller unit. This would reduce the weight of the small transformers but increase the losses still further.

III. Relationships Between Size, Weight and Losses

Appendix 2-II contains an analysis of the losses in transformers delivering constant power as their size (and hence weight) is varied, thus indicating quantitatively the trade-offs involved in transformer design. The results of this analysis indicate that to obtain a transformer which operates at a fixed power level and has a minimum weight-loss product, the smallest transformer designed according to Equation 2-I-20, in which the required core flux density is low enough so that Equation 2-2 is valid, should be used. In other words, the core material should be operated as close to its maximum flux density as possible without violating Equation 2-2.

IV. Transformer Thermal Considerations at 3200 cps

The materials limitation which limits the transformer designer at 60 cycles and sometimes 400 cycles is the saturation of the core material. However, at 3200 cps, the limiting factor is the heat which can be removed from the transformer without an excessive temperature rise. This can readily be seen from the following example.

A transformer will be designed for operation at 3200 cycles with two AL-24C-cores used to form a shell type transformer core. Dimensions of this core are given in Figure 2-2. From curves published by the Arnold Engineering Company for this material (2 mil silectron) the value of "a" (Equation 2-2) equals 1.84. Since, as indicated by the graph of Figure 2-1, the difference in losses between a transformer designed to Equation 2-3 using this value of "a" and one designed with equal core and copper losses will be only about 0.1%, for simplicity the transformer will be designed for equal core and copper loss. Since it has been previously shown (Appendix 2-II) that operation at the highest flux densities yields the minimum weight loss product, the design will first be worked out for a maximum flux density of 14 Kilogauss. (Above 16 Kg, the permeability of Silectron decreases rather rapidly.) If it is arbitrarily assumed that the transformer will have a 1:1 turns ratio and will be wound with #14 copper wire with a winding factor of 40%, the following results can be obtained. (This choice of wire size is completely

arbitrary; the design is only intended to show what can be done with a given core size, and is not an example of designing to a specified voltage and power level.)

The total window area available is 1.73 in^2. The total effective (copper) area of each winding is $\frac{1.73\ (.4)}{2} = .346\ in^2$.

Since the cross-sectional area of #14 wire is $3.225 \times 10^{-3}\ in^2$, the primary and secondary will each consist of $\frac{3.46 \times 10^{-1}}{3.255 \times 10^{-3}} = 107$ turns.

The mean length/turn is $2\ell + 2\ w + \pi\ d = 2(1) + 2(1.25) + \pi\ (3/4)$ = 6.7 in. Assuming the primary and secondary are wound side by side so both have equal lengths of turns, each winding has a resistance of

$$\frac{6.7\ \text{in/turn}}{12\ \text{ft/in}} \times 107\ \text{turns} \times \frac{2.52\ \text{ohms}}{1000\ \text{ft}} = 0.15\ \Omega$$

The weight of the core (from Arnold data) is 2(1.22) = 2.44 lbs. At 14 Kg and 3200 cps, the core loss for 2 mil silectron is approximately 100 watts/lb.

Therefore, the total core loss is 100 (2.44) = 244 watts.

To have a loss of $\frac{244}{2}$ = 122 watts in each of the (2) windings, the current must be such that I^2R = 122 or I^2 (.15) = 122 $I = \sqrt{815} = 28.5$ amps

The voltage that the primary supports is given by[5]

$$V = 2.865N\ BfAS \times 10^{-8} = (2.865)\ (1.07 \times 10^2)(14)(3.2 \times 10^3)(.89)(1.25)^{-4} =$$

$$153 \times 10^1 = 1530 \text{ volts}$$

The total power handled by the transformer is then (1530)(28.5) = 43,500 watts. The efficiency is then given by

$$\eta = 1 - \frac{\text{losses}}{\text{input}} = 1 - \frac{2(244)}{43500} = 1 - 0.0112 = .9888 \cong 99\%$$

This is not only a very high efficiency, but it is obtained from a very small transformer as evidenced by the fact that the current density in the windings is $\frac{4107 \text{ circ mils}}{28.5 \text{ amp}}$ = 144 circular mils/amp.

This is at least 5 times the current density normally used in a unit of this size and indicates that special techniques would be needed in order to hold the temperature of the interior of the unit to reasonable values.

If this same unit is operated at 750 circular mils/amp and the input voltage is correspondingly reduced to keep the core and copper losses

equal, calculations similar to those made previously show that the power rating of the transformer becomes only 2.15 KW. Also, the core and copper losses can be computed to be only at 9 watts each making the efficiency of the transformer 99.16%; only 0.28% more efficient than the same transformer supplying 43 KW. The original transformer (43.5 KW rating) weighed $2.44 + .3\not{\Omega} \times \frac{1 \text{ lb.}}{.203\not{\Omega}} = 3.92$ lbs and had a loss of 488 watts for a weight loss product of 1915 lb. - watts. The same transformer derated to 2.15 KW has of course the same weight of 3.92 lbs. but a loss of only 18 watts. However, if this transformer design were scaled up to 43.5 KW by the methods of the previous section, its weight would be $3.92\left(\frac{43.5}{2.15}\right)^{3/4} = 37.2$ lbs. Since, for similar transformers, the loss is proportional to the weight, the loss is $18\left(\frac{37.2}{3.92}\right) = 171$ watts. Thus the weight-loss product for this transformer is (171)(37.2) = 6350 lb-watts, over 3 times that of the original transformer. Thus, at 3200 cps the electrical rating of the device is virtually completely dependent on its thermal characteristics and environment. This points up the necessity of designing and mounting transformers operating at these frequencies with the same thought given to thermal problems as is done in the case of high power semiconductors.

Since, when mounting, it is much easier to provide a low thermal impedance path from the core than from the coil (because the core has several flat surfaces which can provide low thermal resistance paths to appropriate mounting plates) a compromise design between the first two

designs mentioned above would be to operate the core at its maximum flux level, but to run the coil at more reasonable levels (for example the 750 circuilar mils/amp used in the second design). On this basis, the transformer would still support the 1530 volts of the first case, but th allowable coil current would be only $28.5\left(\frac{144}{750}\right) = 5.5\text{A}$.

This unit thus has a power rating of (5.5) (1530) = 8.33 KW, a weight of 3.92 lbs and a loss of (244 + 9) = 253 watts.

Scaled up to 43.5 KW, this design would weigh

$3.92\left(\frac{43.5}{8.33}\right)^{3/4} = 13.6$ lbs. and would have losses of

$253\left(\frac{13.6}{3.92}\right) = 878$ for a weight-loss product of 11,900 lb-watts.

This is almost twice that of the second transformer design and indicates the desirability of operation in regions where core and copper losses are equalized. However, should weight be of paramount importance and the first design prove thermally impractical because of the difficulty in removing the heat from the windings, this last design saves over 20 lbs., or almost 2/3 the weight of the conventional (second) design, and still operates at an efficiency of 98%.

Since the thermal paths are shorter in smaller devices, this thermal problem would tend to favor splitting up larger units into smaller ones. This idea is investigated in detail in Appendix 2-III, with the result that under conditions where the temperature rise in the unit limits the

maximum flux density that can be used, under conditions of equal internal temperature rise, two transformers, each of half the rating of a single larger transformer, will have a total weight less than that of the single unit. (The losses, however, will also be higher).

V. Multi-Phase Transformers and Circuits Utilizing Them

Up to now, the analysis of transformer optimization has not had to involve any considerations outside the transformer, since the circuitry associated with the transformer would not be affected by the optimization. This ceases to be the case when three-phase transformers are used, as will be brought out in the following discussion.

Of the various possible power switching stages which may be used for three-phase static inverters, some require the use of three single phase transformers, some work only with three-phase transformers and some may be used with either type. More complex transformer construction than the three-phase is also possible and sometimes useful.[4] In order to be able to use a three-phase transformer , the instantaneous sum of the voltages applied to the three windings must equal zero at all times. This condition is imposed by the flux requirements of three phase transformer core design. This requirement is met, of course, by three equal amplitude sine waves each displaced by 120°. It is also met by three equal amplitude quasi-square waves with an "on" time of 120°. Three square waves, even though separated in phase by 120°, do not fulfill this

requirement; thus, inverter power stages which produce square waves cannot use conventional three-phase transformers. The weight savings possible with three-phase transformers will now be investigated.

The core geometry of a single phase transformer made from conventional scrapless E-I laminations is shown in Figure 2-3A. If three of these would be combined into a single transformer, keeping the same coil dimensions and core cross-section, the three-phase transformer would have the core geometry as shown in Figure 2-3B. If it is assumed that the stack thickness of the original transformer is x (i.e. the stack is square), then the thickness of the 3 phase transformer stack will also be x. Since the coils used on the two transformers are identical, the only weight saving will be in the core. The volume of 3 single phase cores of the type illustrated in Figure 2-3A will be $18 x^3$. The volume of one three-phase core is shown in Figure 2-3B will be $14.5 x^3$. Thus, a saving of approximately 20% in core weight is achieved by the use of a three-phase unit. If, for a rough estimate, the core weight is taken equal to the copper weight, the overall weight saving will be about 10%.

The core configuration of Figure 2-3B is not the only possibility, any more than the single phase core shown in Figure 2-3A is the only one available; variation of the dimension ratios are possible and under some conditions quite desirable. (For example, because of the poorer primary copper utilization in static inverter transformers operating with the center-tapped primary scheme it is advantageous to have a larger window area than

provided by the conventional scrapless laminations). It is also possible to take advantage of the flux relationships existing in a three-phase system and arrive at a third type of core structure, shown in Figure 2-3C. Gulow Transformer Company, Inc., the manufacturer of this type of core, claims a 10% weight saving over a conventional three-phase core configuration for this design as well as elimination of magnetic, electrical and physical unbalances caused by the unsymmetrical design of the conventional three-phase core. The draw-back of this system is the added complexity of winding coils for it, particularly if it is desired to make maximum utilization of the window area.

It has already been mentioned that, because of their special magnetic construction, three-phase transformers

1) are lighter than equivalent single phase units.
2) require that the instantaneous sum of the voltages applied to them be always zero

This first item is, of course, an advantge. The second would normally be considered a disadvantage because it prevents the use of single square waves with three-phase transformers. To generate a quasi-square wave usually requires more components and more complex circuitry than a square wave, especially if zero clamping (refer to quarterly report #1, pp 30 ff) is required.

However, the voltage requirement of the three-phase transformer can

be used to provide zero clamping without the use of additonal components. Consider the circuit and waveforms shown in Figure 2-4. If switches S_1 - S_6 are turned on as indicated, it will be observed that

1) There are always two and only two switches on at the same time.

2) Whenever both switches of any phase are off, the sum of the voltages being produced by the other two phases is zero.

Thus, whenever any phase has neither power switch on (and hence its output voltage would, under normal single phase conditions, be undefined) in this three-phase system, the output voltage of that phase must necessarily be zero. Thus, zero clamping is provided by the power switches of the other two phases, working in conjunction with the three-phase transformer. Because this circuit produced 120° quasi-square waves without the need for any additional zero-clamping components, it appeared quite useful and was investigated further.

One item of interest is how the circuit handles load current which is flowing in the secondary of any phase during the dwell (or zero output voltage) time of that phase. This secondary current cannot be balanced by primary current from the same phase, since the only way that primary current can flow is either through the power switch or reactive diode, neither of which can occur when the output voltage is zero. Examination of the circuit and the magnetic relationships required by the transformer

showed that any such secondary current in one phase gave rise to equal currents in the primaries of the other two phases; (for convenience, a 1:1 primary to secondary turns ratio was assumed) one of these induced currents was of such a direction as to represent an energy flow from the d. c. source (and thus went through the power switching element), while the second was in such a direction as to represent a return of energy to the d. c. source (and hence went through a reactive diode). Since the two currents were equal, no net energy was transferred through the inverter to the output of that phase, a condition which must necessarily exist since no energy can be transferred under a zero output voltage condition.

Because this extra current in the power switching elements does not contribute to providing any output power, it results in a less effective utilization of the switching devices than would be possible with a simple square wave inverter. This problem of decreased switch utilization is not limited to this particular circuit, however, as a similar effect will occur in any circuit where the final output voltage is a result of the summation of individual voltage waveforms which are not all in phase. Thus, any of the circuits which provide for harmonic reduction and/or voltage regulation by adding differently phases square waves will be subject to the same problem. However, due to the new way in which the proposed circuit (Figure 2-4) operates, it was deemed advisable to actually compare the switching element currents in this circuit to those in the

more conventional circuits which use phase shifted square waves for harmonic reduction.

The two circuits compared are shown in Figure 2-5. The line to neutral output voltage of each of these circuits is the same, both in amplitude and waveform, and is shown in Figure 2-6. In this waveform, the first harmonic is the 11th, making for relatively easy filtering.

Regardless of whether SCR's or power transistors are used as the power switching element in these circuits, it is the peak value of the current through the switch which is of interest. This is because in the case of transistors, the transistors themselves must have a current rating greater than the peak current, and with SCR's, the commutating circuit must be capable of turning the SCR's off under peak load current conditions. Hence, an attempt was made to determine the peak currents which would occur in the power switching elements in the two circuits. For the case of the conventional circuit utilizing single phase transformers as shown in Figure 2-5B, it is quite easy to put an upper bound on the peak current since, with a peak current of I amperes flowing in each of the three phases, it is obvious that, with the turns ratios as given, the peak current in any primary could not exceed I (.67 + .5+ .16) = 1.33 I amperes. (The number associated with each secondary of the transformers is the turns ratio of that secondary referred to the primary; the angle given with each switch is the phase angle of the output of that switch section compared to the first, which serves as the reference).

Due to restrictions on the phase angles of the impedances which may (according to specifications as outlined in the first quarterly report, page 8) serve as loads on this unit, it is impossible for the peak current in all three phases to occur simultaneously. Thus, the 1.33 I value is in excess of the actual maximum peak current which the switching elements may encounter.

For the three-phase transformer circuit (shown in Figure 2-5A), because of the complex fashion in which currents are transferred from one phase to the other two during the zero voltage periods, it is very difficult to see how to choose the individual phase loads (within the permissible load range) in order to maximize the peak current in any one switching element. However, one attempt to do this yielded a peak primary current of 2.7 I amperes, which is over twice that obtained using the phase shifted square waves.

Since both circuits provide the same output voltage, and require the same number of switches, it is obvious that only half the peak current capability is required of the switching elements in the conventional scheme as compared to those in the three-phase transformer circuit. Since the three-phase transformer circuit also requires a more complex driving circuit, it appears that the 10% transformer weight advantage would be more than offset by the additional weight of the extra switch current capacity needed for operation with the three-phase transformer.

A more complex transformer suitable for operation with an input set consisting of 6 square waves, each shifted by 30° has been described in the literature.[1]

Preliminary investigation of the magnetic paths in this "hexadic" transformer indicates that it would not create the type of circuit problems that the three-phase transformer does. Like the three-phase transformer, the hexadic transformer obtains its weight savings by using less iron in those portions of the magnetic circuit where flux cancellations occur. It is estimated that the hexadic transformer is 20% lighter than its six single phase equivalents. This general area of multiple inverters in connection with multiple transformers to produce stepped waveforms approximating sinusoids will be pursued in more detail in following quarterly reports.

PARALLELING TECHNIQUES AND PROBLEMS

Regardless of the exact nature of the inverter transformers, the switching elements can be considered as an entity.

When the output required of any power switching stage is greater than can be handled with one switching device on each side, the power handling capability of the switch must be increased by paralleling. The simplest method of paralleling is to connect additional power switching elements in parallel with the original one. Although simple, this method suffers from the drawback that, because of the unavoidable differences in

internal impedance of the switching elements, the load current will not be shared equally. As discussed in the first quarterly report (pp 124-125) the two non-dissipative paralleling techniques of interest are the split transformer technique and the balancing reactor technique. These will now be analyzed in turn to determine their relative merit.

I. The split transformer technique

The essentials of the split transformer technique are shown in Figure 2-7. Here, the original (unparalleled) circuit requires a power switching device with a capability of VI watts. The lower circuit indicates the technique used to split the load up into N equal parts, with each power switching stage being required to handle only VI/N watts. Because all the transformer secondaries are connected in series, the same current flows in each, and thus, through transformer action, the primary currents are forced to be identical. This method achieves exact load sharing at the expense of splitting up one large transformer into N smaller ones. The weight and loss penalties that this entails are obtained from the following analysis.

It will be assumed that all of the smaller transformers are identical to one another and similar (in the geometrical sense) to the single large transformer; that is, with all dimensions scaled in the same ratio, the smaller transformers can be made congruent with the

large one. The smaller transformers will also be operated at the same core flux density and winding current density as the larger ones. The analysis proceeds as follows:

Let the large transformer have a power rating of P_I. Then each of the smaller transformers has a rating of P_I/N. If the weight of the large transformer is W_I, then, by equation 2-10, W_N, the weight of each of the smaller ones can be obtained as follows:

$$W_I = k P_I^{3/4} \qquad W_N = k\left(\frac{P_I}{N}\right)^{3/4} = \frac{W_I}{N^{3/4}} \qquad (2\text{-}12)$$

Thus, the weight of N of the smaller transformers will be

$$N\left(\frac{W_I}{N^{3/4}}\right) = W_I N^{1/4} \qquad (2\text{-}13)$$

which is $N^{1/4}$ times as much as the weight of the single large transformer. Since, under the operating conditions assumed above, the losses are directly proportional to the weight, the losses in the N smaller transformers will be $N^{1/4}$ times the losses in the larger transformer.

II. Balancing reactor techniques

The weight (and loss) penalties incurred in using the split transformer paralleling technique have already been analyzed (equation 2-13). Those due to another current balancing scheme, the use of balancing reactors, will now be investigated.

A comparison of using a balancing reactor to equalize the currents in two switching units versus the use of a split output transformer to achieve balance will be examined first. The two methods are shown schematically in Figures 2-8A and 2-8B. The balancing reactor technique operates on the principle that, unless the currents in the two halves of the reactor are equal, a voltage is developed across the inductor in such a direction as to increase the current in that switch tending to carry the least current. Because the same switch will always tend to slack, the balancing reactor must always provide the same polarity voltage when load currents are flowing in it. Thus, an air gap is required in the core to allow the flux to return to zero during the non-conducting halves of each cycle when no current flows and the core must reset itself for the following half-cycle. This air gap, coupled with the relatively few turns required to support the small unbalance voltage results in the balancing reacto having a fairly high magnetizing current. (This could be reduced by over-design of the voltage capability of the unit). The magnetizing current flows through the switch which normally tends to carry more than its share of the load. Therefore, unlike the case of the split transformer technique, in the balancing reactor technique the currents in the switching elements are never perfectly balanced, the unbalance being due to the magnetizing current of the balancing reactor.

In the simple scheme shown in Figure 2-8A, the output transformer is rated at $2\ I_o V$ volt-amperes (where V is the supply voltage and $2\ I_o$ is the D.C. current taken by the switching stage), and the balancing reactor is used at $I_o \frac{v_o}{2}$ volt-amperes, where v_o is the maximum voltage difference required across the switching elements to obtain the desired current balance. However, because of the unidirectional nature of the reactor current, only one-half of the B-H loop of the core of the balancing reactor can be utilized; thus, since only one-half of the voltage capability of the reactor can be utilized, its size and weight will be comparable to one of twice its normal VA rating. Therefore, for purposes of weight and loss estimates, the VA rating of the balancing reactor will be taken as $2\left(I_o \frac{v_o}{2}\right) = I_o v_o$. From equation 2-10, the weight of the single output transformer plus two balancing reactors for the balancing reactor technique will be

$$W_1 = k\left[2\ (I_o v_o)^{3/4} + (2\ I_o V)^{3/4}\right] \qquad (2\text{-}14)$$

Sim , the weight of the 2 split output transformers will be

$$W_2 = 2\,k\,(I_o V)^{3/4} \qquad (2\text{-}15)$$

The ratio of these weights is:

$$\frac{W_1}{W_2} = \frac{k\left[2(I_o v_o)^{3/4} + (2I_o V)^{3/4}\right]}{2k\,(I_o V)^{3/4}} = \frac{1}{\sqrt[4]{2}} + \left(\frac{V_o}{V}\right)^{3/4} \qquad (2\text{-}16)$$

This ratio is plotted in Figure 2-8D for different values of $\frac{V_o}{V}$.

and will be less than I (i.e., the balancing reactor technique will be lighter) for

$$\left(\frac{V_o}{V}\right)^{3/4} < 1 - \frac{1}{\sqrt[4]{2}} \quad \text{or} \quad V > \frac{V_o}{\left[1 - \sqrt[4]{2}\right]^{4/3}} \qquad (2\text{-}17)$$

For a typical V_o of 1.5 volts for a silicon transistor, the cross-over supply voltage for the two techniques (from equation 2-17 or Figure 2-8D) is 18 volts. Above this value, the balancing reactor circuit of Figure 2-8A is lighter (and has smaller losses); below it the split output transformer technique is best.

For balancing more than two switching elements at a time, there are several methods that may be used. The split transformer technique as shown in Figure 2-7 may be used. Balancing reactors of the type shown in Figure 2-8A may be connected in cascade; an example of this for the case of balancing four units is shown in Figure 2-8C.

Although this technique (Figure 2-8C) requires a minimum number of reactors for the number of transistors to be paralleled, it has the disadvantage that if any one of the paralleled elements develops a fault and is cleared from the circuit, the current in the remaining elements is no longer balanced, accelerating failure in the remaining switches.

A. Reference Balancing Technique

One method of avoiding this problem is shown in Figure 2-9. Here the balancing reactors serve to maintain a constant ratio between the current in the reference switch and the current in each of the paralleled power switches Should one of the power switches be cleared from the circuit, all the switches, including the reference, will pick up proportional shares of the load. (If the reference switch fails, the balancing scheme becomes inoperative; for this reason, the reference switch is generally operated at a reduced power level to enhance its reliability.) As an example of this operation, consider the circuit of Figure 2-9 and assume

1. All the switches are operating
2. The total load current is I
3. The turns ratio of the comparison reactors is 5:1 so that the reference switch current is 1/5 of the power switch current.

Let the power switch current be x. Then, the total current is

$$5\,(x) + x/5 = I \qquad (2\text{-}18)$$

which has the solution x = .192 I. Thus, each power switch carries .192 I amps and the reference switch carries .0385 I. If one of the power switches opens, the equation for current division becomes

$$4\,(x_1) + \frac{x_1}{5} = I \qquad (2\text{-}19)$$

This has the solution $x_1 = .238\ I$; each power switch now carries .238 I amperes and the reference switch carries .0476 I. The currents are still balanced, although they are, of course, higher than when all switches were operating. As in the case of the simple circuit using only one balancing reactor, the actual switch currents will deviate from the ideal due to the magnetizing currents of the balancing reactors.

An analytical investigation of the weight penalties inherent in the reference balancing technique will now be undertaken. If there are n power switches, and the current through the reference element can be neglected, the current in each reactor will be I/n, where I is the total current carried by the parallel switch bank. Since 2 switching banks are used for each inverter stage, the total number of reactors needed is 2n. Each reactor must be able to support v_o volts (where v_o, as before, is the maximum unbalance voltage between switch units when all are carrying equal current). Thus, the rating of each reactor (again inserting a factor of two to account for the reduced use of the core capability brought about by the unidirectional current), will be $2\ v_o I/n$ amperes. The ratio of the weight of this system to one consisting of n split transformers is then

$$\frac{\text{wt. of reference balancing technique}}{\text{wt. of split transformer technique}} = \frac{(VI)^{3/4} + 2n\left(2v_o\frac{I}{n}\right)^{3/4}}{\left(\frac{VI}{n}\right)^{3/4}} \qquad (2\text{-}20)$$

$$= n^{-1/4} + 2\left(\frac{2v_o}{V}\right)^{3/4}$$

where equation 2-10 was used to evaluate the relative weights. Thus, it can be seen that the weight (and loss) advantages of this system increase as the number of elements to be paralleled increases and as the supply voltage increases.

As a specific example, with $v_o = 1.5$, $V = 28$ and $n = 6$, using Equation 2-20 yields a ratio of

2-21

$$\frac{\text{wt. of reference balancing technique}}{\text{wt. of split transformer technique}} = 6^{-1/4} + 2\left(\frac{3}{28}\right)^{3/4} = 1.013$$

Thus, under these conditions the split transformer technique is only marginally better than the reference balancing reactor technique and other considerations would probably be the deciding factors.

B. Closed Chain Balancing Reactors

Still another technique using balancing reactors is shown in Figure 2-10. Here, each switch has its current balanced with the two elements on each side of it (and the outside ends are compared with each other, to form a closed chain). With the loop closed, the balancing obtained by this technique is very good; when one of the switches is opened, the loop is opened and the unbalance increases, although the circuit still operates to maintain the balance. If the current carried by the reference transistor is neglected, this scheme has the same weight as the reference balancing scheme.

It does have the advantage that all of the switches are treated equally; any one can fail and the circuit will still operate somewhat. (In the case of the reference balancing scheme (Figure 2-9) failure of the reference switch means complete loss of balance, although balance will be maintained even though one or more of the power switches fail).

As the example worked out in equation 2-21 shows, neither technique (split transformer or balancing reactor) offers any great weight advantage over the other in the power level and voltage range under considerations. However, weight (and losses) are not the only items of significance. Reliability of operation is also extremely important; the problems involved in improving the reliability of the power stage are indicated below.

III. Reliability Considerations

Due to the large number of power switching transistors required in the 10 KW inverter output circuits, provision should be made for the failure of one or more of these individual units without causing inverter failure. Working for the moment with the split transformer circuit and allowing only one failure, the problem is that the switching stage combined output after the failure should have:

1. a high enough fundamental component so that the output voltage regulation requirements can still

be met under the worst loading and input voltage conditions.

2. a low enough harmonic content so that the filtered output voltage can still meet the harmonic specifications

These objectives can be met by either providing an excess of output voltage and harmonic filtering capability so that one power switching stage could be completely removed from the circuit in case of failure or by providing some means of isolating and/or replacing a defective component so that the output of all power switching stages is maintained.

IV. Redundancy Methods Used with the Split Transformer Technique

Examples of two possible redundant techniques suitable for use with the split output transformer approach are shown in Figures 2-11 and 2-12. In these diagrams the FL_n-K_n combinations are one shot, normally open thermal relays which operate in the following fashion: As long as the current through FL_n has never been high enough to cause it to melt, FL_n continues to conduct current and K_n remains open. However, should excessive current cause the fusible link FL_n to open, (just as a regular fuse would) the normally open switch K_n is closed.

In Figure 2-11, any failure of any circuit component which eventually

results in a high current through the fuse link FL_1, closes the contacts K_1, placing a short circuit across the transformer primary (or secondary, if that has the lower current rating), thus effectively replacing it in the overall inverter by a short circuit. (If the transformer were not shorted when FL was opened, then all the voltage generated by the other power switching stages with which this one was connected in series would appear across the output transformer (until it saturated). Thus, the net output voltage would be considerably reduced - once by having no contribution from this transformer and again by having the output contributions from the other transformers dropped across the defective stage. Hence, the need for shorting the transformer when its drive circuit becomes inoperative.

In the circuit of Figure 2-12, the only type of failure that can be corrected is a short in either power switching transistor. When this occurs in S_1 for example, the two identical links FL_2 and FL_3 open, allowing contactors K2 and K3 to close, inserting S_3 into the circuit in place of S_1. Similarly, a failure in S_2 would result in S_3 into the circuit in place of S_2. Since there is only one S_3, it cannot compensate for failure of both S_1 and S_2; should both S_1 and S_2 fail, the transformer would still be shorted by K_2 and K_5, and F would remove S_3 from the circuit. Clearly, this scheme provides correction only for a shorted transistor; should any other trouble develop

in the circuit, the links would still open, but the substitution of S_3 would not solve the problem, so the other links and F_3 would open making that particular power stage an open circuit for the d.c. supply but a short circuit on the a.c. side. It is also questionable whether the single good transistor could supply adequate current to the shorted unit to blow the fuse without itself being damaged.

Examination of the circuits used for these two techniques indicates that the elimination technique shown in Figure 2-11 is the simpler and provides for many more eventualities than the replacement technique of Figure 2-12.

Hence, the circuit of Figure 2-11 is the one tentatively selected for possible application in conjunction with the use of the split transformer technique. Since either of these techniques can result in the transformer primary being shorted, if the primary indicated would be only one phase of a three-phase transformer, the other two phases would not be able to work properly and would fail also. Thus, a technique which involves three-phase transformers must be prepared to sacrifice two additional switching stages for every one that fails (which is not considered an acceptable solution). The alternatives are the use of single phase transformers or multiphase transformers which do not require any special instantaneous flux conditions. Also, if a stage is eliminated, the resulting unbalance in output voltage would have to be made up by the voltage regulator for that phase. Thus, individual

phase voltage regulation would also be required.

V. Redundancy Methods Used with Balancing Reactor Techniques

The problem of increasing reliability through the use of redundancy does not appear as difficult when the balancing reactor technique of paralleling is used. This is due to the fact that the paralleled transistors are actually connected in parallel and when one fails, all that is required is that it be disconnected from the circuit (if it fails short), and the other transistors in parallel with it will automatically assume the increased load. Hence, there is no significant change in output waveform or amplitude when one of several transistors paralleled with a balancing reactor scheme is removed from the circuit because of failure. To avoid difficulties in the balancing reactors, transistors removed from the circuit have their balancing reactors shorted out; this is also accomplished with a fusible link as shown in Figure 2-24.

VI. Transient Problems With Balancing Reactors

The use of balancing reactors to provide for load sharing of controllable switches presents problems not encountered when balancing reactors are used for equalization of current in diodes. These problems arise because of the inevitable difference in switching times of the paralleled units. For example, consider the balancing scheme of Figure 2-8A, shown again in Figure 2-13. Assume that,

for some reason, an inductive load current I_s is flowing in the secondary, and a corresponding primary current I_p is flowing through a reactive diode on the primary side. If S_2 is slower than S_1, and the drive provided is adequate to allow S_1 to carry a current of I_p, then, when S_1 and S_2 receive the signal to turn on, the current buildup will occur initially in S_1. As long as the current in S_1 is less than the transformed secondary current, in order to satisfy the relation $\sum NI = O$ required of the output transformer, D_2 will continue to conduct the amount of I_p not carried by S_1. Since, as long as D_2 conducts, the potential of the end of the transformer to which it is connected must remain at approximately ground potential, the other end, where the center tap of the balancing reactor for S_1 and S_2 is connected, must remain at 2E. However, as S_1 starts to conduct, the voltage across it goes to zero, leaving a drop of 2E across 1/2 of the balancing reactor. Thus, a voltage of 2E is induced in the other half of the primary, giving a total voltage across the yet unconducting S_2 of 4E. This not only places a very high voltage requirement on S_2, but when S_2 finally turns on, it does so into a voltage of 4E, thus doubling its turn-on switching losses. (By the same token, the turn-on losses of S_1 are virtually eliminated, because it turns on into the high impedance provided by the balancing reactor). The high voltage problem can be solved by placing a diode (or diodes) across the balancing reactor windings as shown in

Figure 2-14. This prevents the drop across the balancing reactor from exceeding 2 v_d where v_d is the forward voltage drop across one of the diodes. Since a typical value for v_d is around 0.7 volts, this means that the reactor will be able to correct for differences in switch drop up to 1.4 volts without any interference from the diodes. This value should be sufficient; if it is not, two (or more) diodes could be connected in series to provide 2.8 (or more) volts.

This technique solves the voltage transient problem but starts a new one. Refer to Figure 2-14 and assume that S_2 turns on faster than S_1. As S_2 starts to conduct, the voltage across the balancing reactor will rise in such a fashion as to increase the voltage across S_1 in an attempt to force it to conduct. The voltage across the reactor can rise to no more than twice the forward drop across the diode, however, because at this point, D_B will start to conduct and, under these conditions (i.e. S_1 not conducting) all of I_p could flow through D_B into S_2. If I_p is greater than the maximum current permitted in S_2 (which may be, even in normal circuit operation, since I_p is intended to be carried by both S_1 and S_2 and thus only $I_p/2$ must be within the rating of S_2), S_2 will experience excessive turn-on losses, may be pulled out of saturation by the heavy current, and may even be damaged. This can be solved by inserting a saturable reactor in series with the switching section to limit the current to a small value until both transistors have been turned on fully. A method for accomplishing

this and providing a reset for the cores at the same time is shown in Figure 2-15. In this circuit, the same core is saturated in alternate directions by the two switches. At turn-on, the supply voltage appears across the saturating core until it saturates, at which point the voltage is transferred to the output transformer primary winding. Regardless of which element the voltage is dropped across, it is transformed and appears in series with the supply voltage across the other (open) switch. Thus, the switch is required to withstand 2E, which is no more than it would if the saturating core were not present. A problem occurs, however, when the switch that was on is turned off. The saturated inductance of the saturable reactor tends to maintain the current through it constant. Thus, it increases the voltage across the switch turning off (in an attempt to keep the current constant) increasing the turn off losses.

With proper design and core materials, this effect is very small, as can be seen from the following example. Suppose the current to be taken by each switch section is 100 amperes, the delay required to allow all transistors to become conductive is 10 usec and the supply voltage is 30 volts.

Then, using a supermendur core with a B_{max} of 20×10^3 gauss (or a total ΔB during the delay period of 40×10^3 gauss, since the core goes from $-B_r$ to B_{max} each time, and $B_r \cong B_{max}$ for supermendur)

the turns-core cross-section product is given by:

$$NA_c = \frac{V\,t \times 10^{-8}}{\Delta B} = \frac{30 \times 10^{-5} \times 10^{8}}{2\,(2 \times 10^{4})} = .75\ cm^2 \qquad (2\text{-}22)$$

Allowing each winding to pass through the core twice, a core cross-sectional area of 0.375 cm^2 is required. A magnetics core 50094 of 2 mil supermendur will provide this core cross-sectional area and has a window area adequate for the copper required. The magnetizing current for this core would be .52 amperes; this is the current that would flow when the core was unsaturated. After saturation, of course, the current would be limited by the load (to 100 A, in this case). Under the assumption that the inductance of the saturated core is simply the inductance of a single turn loop, it can be calculated from the following formula[2] once the physical dimensions are known.

$$L\ (\mu hy) = \frac{a}{100}\left[7.353 \log_{10} \frac{16a}{d} - 6.386\right] \qquad (2\text{-}23)$$

where a = mean radius of ring in inches

b = diameter of wire in inches

From the core and wire dimensions, for this case $a \cong 1/2$ in

$b \cong 1/8$ in

Thus, the saturated inductance calculated on this basis is (from substituting into Equation 2-23) is 0.35μhy. Assuming the fall time of the current to be 1/2 of the rise time or 5 usec, the di/dt in this circuit is $100/(5 \times 10^{-6}) = 20 \times 10^{6}$ amp/sec. The voltage across

the "inductor" will then be $e = L\, di/dt = (3.5 \times 10^{-8})(2 \times 10^{7}) = 0.7$ volts. Clearly, this is negligible compared to the E or so volts which will be present from the d.c. supply. (Whether the voltage is E, 2E, or some other value will, in general, depend on the circuit and load). Thus, this proposed technique reduces turn-on losses without significantly increasing the turn-off losses. In order for this technique to operate properly, however, (leading) reactive current must be prevented from flowing through the saturating reactor windings and prematurely resetting the core. Under conditions of an effective leading power factor load (which can occur for some phases in a multi-stepped inverter even if the actual external load is resistive or lagging, because of the phase difference between the load current and the output voltage of the individual stages making up the composite waveform) if reactive current is allowed to flow through the transistor the delay core will be prematurely rest at a time when it would be especially needed. This can be seen by referring to the circuit diagram of Figure 2-15 and the waveform drawing Figure 2-16A which shows the relationship between phase output voltage and current for capacitive, resistive, and inductive loads.

In the capacitive load case, assume S_1 is on and conducting current in the direction indicated (I_1). Then, towards the end of the half cycle, the direction of the current reverses, and D_1 then conducts, resetting the saturable reactor in a direction as to allow current

to flow unhampered into the undotted end. When the half-cycle is over and S_2 turns on, it is immediately able to pull current through its winding on the saturable reactor, because the core had already been reset by the earlier reactive current in D_1. A similar analysis will show that this problem does not exist for loads which appear resistive or inductive to this phase.

The obvious solution to the problem is to prevent reactive current from flowing through the reactor winding. This can be partially solved very easily by moving the reactive diode connection points t the top ends of the saturating reactor winding, as shown in Figure 2-16B. However, even though (as shown in Figure 2-16B) a reactive diode is available to provide a current path which does not include the saturating reactor, if there is a d.c. path to ground from the base of the switching transistors, some current is able to flow through them in the reverse direction with a drop less than or equal to the drop across the reactive diode. This then provides a base current which allows the emitter to act as a collector (and vice versa) and transistor action provides an even lower voltage drop path through the entire transistor (I_r' on Figure 2-16A). If the transistor base is forward-biased, (as it would ordinarily be at the time when reactive current could flow) the reactive current has an even easier path through the transistor because the base collector diode will already be forward-biased. Hence, the reactive current will be able to flow

through the transistor with a very small voltage drop, completely by-passing the reactive diode. A solution to this problem is to reverse bias the transistor base-emitter junction by an amount at least equal to the forward drop of a diode whenever reactive current flows. This can be accomplished by a feedback technique described more fully later in the report (pages 62-65).

Although the saturating core technique virtually eliminates turn-on losses, it introduces losses of its own, since the saturable reactor core is always driven to saturation in each direction. However, the savings in turn-on losses (with presently available transistors) outweighs the additional core losses, making this a worthwhile technique. This concept was investigated in the laboratory, with the results being given in Appendix 2-IV.

VII. Transient Effects With Split Transformer Paralleling

When using the split transformer technique, as long as each power switching circuit has reactive diodes, the maximum voltage that can appear across any power switching element is two times the supply voltage, and even under transient conditions, it is impossible for the current in any transistor to exceed its rating (as long as the load current is within specifications).

Thus no additional parts are required to make a paralleling circuit such as shown in Figure 2-7 safe from transients under practical loading conditions and component tolerances.

SUMMARY OF RESULTS

The results obtained from this study can be summarized as follows:

1) For maximum efficiency, transformers should be operated so that their core loss is 2/a times the copper loss. ("a" is the exponent in equation 2-2). However, there is very little difference in efficiency in transformers operated in this manner and those designed for equal core and copper losses.

2) For transformers designed with the same coil current and core flux densities, the losses are proportional to the weight, and also are proportional to the three-fourths power of the volt-ampere rating.

3) The loss weight product of a transformer is minimized by operating it with its core flux as high as possible, and copper losses in the proportion prescribed by result 1 above.

4) Temperature becomes an increasingly important design factor as the operating frequency is raised; at 3200 cycles, internal temperature rise rather than core saturation or regulation limits the power that can be handled by all but very small transformers.

5) Three-phase transformers, though being themselves lighter than the equivalent single-phase transformers, required over twice the

switching stage current capacity as the single-phase transformers in the circuits investigated. Thus, they were contradicted because of their effect on the rest of the circuitry.

6) Whether the balancing reactor or split transformer paralleling technique will be lighter depends on the number and type of units to be paralleled and the supply voltage. An example of how to determine the optimum method is worked in detail in the body of the report.

7) The problem of providing redundancies in these paralleling schemes is also discussed along with the special circuit problems each method introduces.

SWITCHING ELEMENT LOSS STUDIES

Although many of the losses in power switching semiconductors, being a component and/or materials problem, are beyond the control of the circuit designer, he can effect significant savings in several areas. Basically, losses in power switches (either transistor or SCR) come from the following sources.

1) "on" losses
2) "off" losses
3) switching losses
4) drive losses

The problems associated with minimizing each of these losses will now be discussed.

I. Forward or "On" Losses

The best and most direct method of reducing forward losses is to reduce the current carried by the semiconductors (or, just as well, the number of semiconductors in series with each current path). Examples of this were discussed in the first quarterly report and indicated the undesirability of using d.c. regulators or bridge circuits in inverters operating from low voltage sources. The three-phase transformer circuit discussed on page 131 of the first quarterly report was also rejected for requiring excessive semiconductor current capability.

In both silicon and germanium transistors, adequate drive is essential for keeping forward losses low, since, up to a point, an increase in drive results in a decrease in forward drop across the transistor. (It also means an increase in the drive losses, so maximum drive may not be the optimum).

Germanium transistors have lower forward drop than silicon, and considerable savings may be made here, if thermal considerations permit the use of germanium. The saturated transistor approximates a fixed resistor in the forward direction, so it is the r.m.s. current which actually should be minimized in the case of transistors.

Once on, the forward drop of the SCR is independent of drive and is also largely independent of current in the normal region of operation. This drop has approximately the characterisitcs of that of a silicon diode although it is slightly larger. Thus, the SCR drop is greater than that of a silicon transistor at low currents, but approximately equal at higher currents.

A new line of inverter-type SCR's has an even higher forward drop than the standard SCR, this parameter having been sacrificed to obtain a smaller turn-off-time. Unless the slightly faster turn-off-time and higher dv/dt capability of these units was required (as it would be at higher frequencies and voltages), standard SCR's selected for turn-off-time would result in lower overall losses.

II. Reverse or "Off" Losses

With proper design, reverse losses in all components can be made quite low in comparison to the other losses. With transistors, reverse base bias is all that is required to attain the minimum value. Since this loss is due to highly temperature dependent leakage currents, it can be reduced by lowering the junction temperature of the device. (The mian purpose in lowering junction temperatures, however, is usually reliability, as the small improvement in losses is generally not worth the extra heat sinking required).

III. Switching Losses

Switching losses are of two types: turn-on losses and turn-off losses. With transistors, turn-on losses can be reduced by

1) using transistors with higher switching speeds;

2) providing fast-rising base overdrive at turn-on in order to reduce the switching speed;

3) making the load appear inductive at turn-on so that the voltage across the transistor can drop to a low value as soon as it starts to turn on.

An example of the application of this third rule is found in the saturating inductance inserted in the collector lines of Figure 2-15. The same

ideas can also be applied to SCR's. In fact in many SCR circuits it has been found necessary to insert additonal inductances in series with certain current paths in order to prevent SCR damage due to large currents at turn-on flowing through a small fraction of the total available junction area and causing localized heating.[3] A typical circuit (the McMurray inverter) is shown in Figure 2-17. Here L_C is in the circuit to limit the current when SCR 3 and SCR 6 or SCR 5 and SCR 4 are turned on. When either SCR 1 or SCR 2 is turned on, L_C still serves to limit the initial current through C_C, and L_f, the filter inductance, limits the initial current to the load.

A typical SCR drive circuit which meets the requirements listed above is shown in Figure 2-18A. In this circuit, as the square wave source goes positive, no voltage is applied to the SCR gate until C has had time to charge up through R_1 to the firing voltage of the Shockley diode SD. When this point is reaced, the voltage across the diode suddenly drops, applying nearly the full voltage of C across R_2 and the SCR gate. (R_2 serves only to limit the peak current through the gate, so C soon discharges and the current falls to a level, determined mainly by R_1, which is sufficient to hold the SCR in the "on" condition).

Turn-off losses in transistors can be reduced by

1) using transistors with higher switching speeds;

2) providing fast-rising reverse base drive in order to quickly remove stored charge;

3) making the load appear capacitive (at turn-off). This allows the current through the "on" transistor to drop to zero without requiring (instantaneously) a corresponding voltage change, as would be the case with a resistive load).

It can be seen that there is a conflict between the requirements for reducing turn-on and turn-off losses -- namely for low turn-on losses, an inductive load is needed while reduction of turn-off losses requires a capacitive load. The saturating reactor as used in Figure 2-15 is a partial compromise in that at turn-on, it makes the circuit look very inductive whereas it has virtually no effect at turn-off because it is saturated at that time.

Virtually all of the turn-off losses in SCR circuits occur not in the SCR itself but in the commutating circuit needed to provide the necessary turn-off-pulse. The McMurray circuit, shown in Figure 2-17, is one of the most efficient circuits in this regard, in that the commutation energy is not dissipated each cycle, but rather is stored in the commutating capacitor for the next half cycle.

Because of charge storage, an SCR that was carrying current is a short

circuit in the reverse direction for a short time after the voltage across it is reversed. This must be taken into account in commutating circuits to avoid having unexpected current paths not limited by inductances.

IV. Drive Losses

In general, drive losses are of two types: those actually lost in the driven device and those losses which occur in the circuit used to match the driving source to the given load. This last type of loss increases with the possible variation of input impedance of the power switching device. In the case of SCR's, there is a large variation in gate characteristics from unit to unit; with transistors, temperature accounts for considerable variation. Because SCR drive requirements amount to a very small portion of the total device losses, it is not worthwhile to go to any complexity to reduce them, save for those steps necessary to provide the proper waveform as described under the switching loss section. With transistors (especially silicon), the drive losses can be an appreciable part of the total losses and some added complexity to reduce them may be worthwhile. Two possible drive schemes are shown in Figures 2-18B and 2-18C.

Figure 2-18B shows the situation with fixed square wave drive. Even though the steady state collector current (shown dashed) requires only a level of drive as shown by the dashed line on the drive waveform,

because, under transient conditions, the collector current may become as large as the solid collector current waveform, the drive must always be maintained at a level high enough to adequate for this worst case. Thus, for most of the time, considerable drive power is used which is not required. In addition, the excess drive will increase the turn-off losses. A considerable improvement on this drive is shown in Figure 2-18C. Here, only a small square wave drive is provided by the normal drive source; the remainder of the required drive is obtained from current feedback from the output collector current. Thus, under high load conditions (solid line) the drive is adequate, and under low load conditions (dashed line) the drive has been reduced proportionally, so it is still adequate. This type of drive is near optimum, since the driving signal is adjusted continually and virtually instantaneously in order to provide the necessary drive and no more. This type of drive also eliminates the problem of reactive current flowing in the power switches and upsetting the turn-on delay core reset as discussed earlier in the section on transient effects with balancing reactor paralleling.

10 KW INVERTER STUDY

I. Introduction

In order to obtain a meaningful comparison of the use of SCR's or power transistors for the 10 KW 3200 cycle inverter, it was decided to make comparisons on the basis of the calculated weights, efficiencies, and parts count of paper designs for each.

In arriving at the choice of circuit for each type of inverter, consideration was given to the fact that, for the input voltage and current levels under consideration, phase shift modulation appeared to be the best method for voltage regulation. (This was discussed in the first quarterly report.) For the SCR circuits, it was decided to retain as much as possible the basic advantage of the SCR circuit -- its simplicity. Therefore, a very simple power switching scheme which required a total of only 12 power switching SCR's was used. (The simplest practical parallel inverter scheme, the McMurray-Bedford circuit, uses only 2 power switching SCR's per stage, and no commutating SCR's.) However, as indicated in the first Quarterly Report, the commutating losses in this circuit are excessive at 3200 cycles, being 7.8 times the losses which would result if only the load current flowed in the SCR's. The McMurray circuit, while considerably reducing the commutating losses (by a factor of 5.4), does so at the expense of adding 4 commutating SCR's per power switching stage, for a total of 24 additional SCR's per complete three-phase inverter.

For the transistorized inverters, even though every effort was made to keep the number of transistors in the output switches low, it was found that, at a minimum, 72 would be required.

In view of this large number, it appeared reasonable to divide them up into groups of moderate current capability and then combine their outputs to form a more complex and more easily filtered wave than was obtained with the SCR inverter. Thus, some or all of the weight and space lost in having to parallel units could be made up in the reduced filter requirements. Also, some thermal problems might be eased by having several smaller transformers rather than one larger one.

To compensate for the obvious disadvantage of the unreliability of the large number of transistors required, redundancies were added to each switching section.

A block diagram of the transistor circuit used in shown in Figure 2-19A. Circuits for the individual blocks of Figure 2-18A can be found in Figures 2-20 through 2-26. Loss and weight estimates and parts counts are given in Table 2-2. Descriptions of the function and operation of each of the circuits used as well as an overall description of the operation of the inverter are given in detail in the two sections following.

II. Transistorized Output Stage Inverter

A. General Description

The block diagram of the complete inverter is shown in Figure 2-19A. The master oscillator-pulse shaper provides a series of output pulses at 12 times the inverter output frequency. These are fed to two places: 1) a six phase transistorized flip-flop set which provides an output consisting of 6 square waves, (at the inverter output frequency) each displaced from the next by 30°, and 2) a phase shifter, which is capable of delaying the pulses from the oscillator by any amount from (approximately) 15° to 175° as measured at the fundamental frequency. The pulse output of the delay circuit, which has the same appearance as the pulse output directly out of the master oscillator-pulse shaper, is then fed to another six stage ring connected flip-flop identical to that mentioned above. Its output is another set of 6 square waves at the inverter fundamental output frequency with each displaced from the next by 30°, and the entire square-wave output set displaced from the corresponding ones provided by the first flip-flop set by an amount depending on the delay provided in the delay circuit (15°-175°). These waveforms are shown in Figure 2-19B. These outputs (6 from each flip-flop set) are then amplified by their associated driver amplifiers and fed into the input of the square wave power switching stage where they are further amplified and transformed by various ratios on the output transformer to be added in series with

one another to yield the composite output. The turns-ratios and method of interconnection are shown in Figure 2-5B. With this technique, the output voltage shown in Figure 2-6 contains no harmonics lower than the 11th. This scheme of utilizing all six square wave output voltages to form part of each phase output voltage was chosen in preference to a similar scheme which generates a comparable waveform with the use of only 5 of the 6 available waveforms[4] because the method of using all six square wave voltages gave a more complete distribution of phase loads and allowed all twelve output transformers to be identical. The hexadic transformer described in the above mentioned report could still be used in this scheme. Although the generation of an even more complex waveform than that provided by the six square wave approximation would permit a further decrease in filter size, this was not attempted because of the 6 step scheme, when scaled down to handle the 2 KW inverter, would require just 1 transistor in each power switching element. Clearly, a more complex system than the 6 step approach could not then be scaled down without becoming overly complex for its function at the lower power levels. (The next possible number of steps in a scheme of the type used here is 9, which would mean a 50% increase in the overall complexity.) It should also be mentioned that the filter in a static inverter performs two functions: it not only removes unwanted harmonics from the power stage output, but also acts as a buffer between the power switching stage and the load. This will be further

discussed in the filter section.

The delay of the variable pulse delay circuit is controlled by the voltage and current feedback circuit to maintain the average of the phase voltage outputs at the desired value (or peak current in any or all phases below the 200% overload limit). The individual blocks are discussed in more detail in the following sections.

B. Master Oscillator-Pulse Shaper

The master oscillator determines the final output frequency of the inverter and is chosen to have an accuracy and stability consistent with the inverter output frequency requirements. As indicated in the first quarterly report, the design details and relative merits of the various types of precision oscillators have been well covered elsewhere and will not be duplicated here. Because of the frequency dividing effect of the flip-flops, the output pulses from the master oscillator-pulse shaper must be at 12 times the fundamental output frequency of the inverter. The pulse shaper (if required) serves only to modify the oscillator output into a form suitable for triggering the flip-flops.

C. Six Phase Count-down Circuit

Each six phase count-down consists of 6 flip-flops interconnected in a closed loop with the triggering arranged so that successive input

pulses result in the triggering of successive flip-flops around the ring. Starting circuits are provided to initially set all flip-flops to a predetermined state to insure proper sequencing and output waveforms. Since the input pulses are of constant frequency, the output of each flip-flop is a square wave, displaced from the other flip-flop square wave outputs by multiples of 30° at the fundamental inverter output frequency. (They are, of course, spaced at integral multiples of the period of the input pulses, which are at 12 times the output frequency).

D. Variable Pulse Delay

The purpose of the variable pulse delay circuit is to delay the pulses from the master oscillator to the second flip-flop set so that the output square waves from the second flip-flop set will lag those of the first by a controllable amount. This problem is made difficult by the fact that the time delay required is greater than the period of the input pulses. In fact for operation under short circuit conditions, a delay up to 6 times the period of the input pulse is required. (This much delay amounts to a half period at the fundamental, making the two output voltages from the power stages 180° out of phase, thus cancelling one another and limiting the output current to a low value). One possible solution to this problem is shown in the block diagram 2-20. Here, the incoming pulse train is transformed into a square wave of 6X output frequency by the flip-flops. This square wave is

then passed through a series of variable delays, each of which has the circuit of Figure 2-21, and can delay it on an amount that ranges from 0 to $T_o/12$ (where T_o is the period of the fundamental output). Thus, after 6 delays, the output square wave has a frequency of 6X the inverter output frequency and can be varied from 0 to 180° as measured on the time scale of the fundamental. This square wave is then differentiated and rectified to obtain the delayed pulse train which is then fed into the second flip-flop set. Appropriate circuits are provided to insure that all flip-flops are initially set to the proper state for correct start-up and synchronization.

A simpler technique for accomplishing the same result is the use of a voltage-controlled variable frequency oscillator to produce the second pulse train. When the inverter output voltage is correct, the feedback voltage from the voltage regulator is such as to hold the frequency of the second oscillator in exact synchronism with the master oscillator (although there will be a phase difference). Should an increased load lower the output, the feedback signal increases the frequency of the second oscillator, (thus advancing the phase of the square wave output from the second flip-flop set) until the output voltage is again at the correct level, at which time the second oscillator is again held in frequency synchronism with the master oscillator (though with a different phase difference than before).

Though a much simpler system than the first one discussed, this technique has its disadvantages. Care must be taken that the regulator acts quickly enough and does not overshoot, so that before equilibrium is reached, the phase difference between corresponding square waves from the two flip-flop sets does not slip into the 180 to 360 degree range, making the previously negative feedback positive, causing oscillation of the output voltage. Whether or not the avoidance of this problem would be difficult or easy would require more detailed study than is presently warranted.

E. Driver Stages

The amount of drive power required depends on the drive technique used. For the feedback technique for drive reduction which is proposed, the drive signal consists of two parts: a short duration high current pulse which cancels out the feedback drive which was being provided to the "on" transistors and simultaneously provides turn-on base drive for those which had been off.

Once the switching has been accomplished, only a small amount of drive is required from the driver stage itself, the major part of the drive power being supplied from the feedback circuitry. A circuit capable of providing this type of drive is shown in Figure 2-22. In this circuit, until C has been charged sufficiently through R_1, the Shockley diode does not conduct. However, when the breakover

voltage of the Shockley is reached, it reverts to the conducting state, placing the full voltage of C across the load. R_2 limits the current at the instant that the Shockley diode conducts to the desired value; R_1 provides the steady state current limit.

When the input square wave reverses, the voltage across C decreases from its steady state value and goes through zero as C charges up again through R_1, this time to the negative of its value during the previous half cycle. As the capacitor voltage nears zero, the current through the Shockley diode falls below its holding current, and it regains its forward blocking characteristics. As C continues to charge up through R_1, the voltage across the Shockley starts to rise, just as it did during the first half cycle. The Shockley breaks down when a high enough voltage is reached. The only difference is that now the voltage across C (and hence the load) is the negative of what it was during the first half cycle, thus turning on the transistors that were off and turning off those that were on. The use of a single Shockley diode in a bridge configuration not only saves a Shockley diode over the conventional approach, but also insures symmetry of operation, since the same components produce both the positive and negative half cycles.

The technique of providing a drive proportional to the collector current is shown in Figure 2-23. Here, the Shockley diode drive circuit as shown in Figure 2-22 is represented (during that part of

the cycle after the initial surge of current) by a constant current source, since it has a high internal impedance compared to the load. The turns ratio $\frac{N_B}{N_C} = B$ is chosen such that where B is the minimum current gain of the transistor under the circuit operating conditions. Hence, the total drive to the transistor is (2-24)

$$I_B = \frac{N_C}{N_B} I_c + \frac{N_D}{N_B} I_D \qquad (2\text{-}25)$$

The drive is thus a constant term plus a term directly proportional to the load (collector) current.

As can be seen from 2-67 and the schematic of Figure 2-26, when the circuit is required to supply reactive currents, ($I_C < O$) it is possible for the value of I_B as given in 2-67 to be negative. In fact, this will occur for

$$I_R \geq \frac{N_D I_D}{N_C} \qquad 2\text{-}26)$$

where $I_R = -I_C$ and is the value of the total reactive current flowing in both the reactive diode and transistor.

During the time when the net base drive to the transistor is still positive but reactive current is flowing, the core is being reset. However, under these conditions, the voltage across the core is only about 1 volt, so about 300μ sec would be required to reset the delay core described in pages 44-45.

The determination of the actual length of reset applied to the core proceeds as follows.

With the magnetizing current of the core at about 1 amp, a reasonable value of current which the drive circuit should be able to provide by itself is around 5 amp. Assuming a minimum β of 10, the square wave base drive (on the secondary side of the transformer) is 5/10 = 0.5 amp. The turns ratio of $\frac{N_B}{N_C}$ is then 10. Hence, for reactive currents greater than 5 amperes, the transistor base-emitter diode will be back-biased, and no reactive current will flow in the transistor. Since each transistor alone could safely handle 50 amp peak current, there is no difficulty with values less than that. This is the worst case, and the collector current can be expressed as $I_C = 50 \sin (2\pi (400)\, t)$ (for 400cycles which is a worse case than 3200 cycles). This will have a value between 0 and -5 amp only for a length of time equal to about 42μsec. Hence, this is the time available for prematurely resetting the core. Since, at the voltage available (1 volt) it would take about 300μsec for a complete reset, it can be seen that only about 15% of the delay time of the core has been lost. At high prospective reactive currents, the time required for the reactive current to reach 5 amperes after passing through zero would be even less, hence the loss in delay would be correspondingly less.

F. Output Stage

A schematic of the output stage is shown in Figure 2-24. T_1 with its three secondaries is the output transformer; D_1 and D_2 are the

conventional reactive diodes. T_2 is the saturating reactor which serves to delay rise in collector current until the transistors have had ample opportunity to turn on, and T_3 is the driver-feedback transformer.

The drive circuitry is of the feedback type, both for reduction of normal drive losses and also for proper shunting of the reactive current into the reactive diodes. This necessitates having the drive transformers for each side separate, since a reactive current in one side would result in a turn-on signal to the other side if the drive transformers were coupled.

The transistor collector currents are balanced with balancing reactors connected in a reference balancing scheme. Each transistor is fused in such a manner so as to disconnect it from the circuit in the event it shorts out (collector to emitter). Should any one develop an open, the diodes D_5 and D_6 act to prevent its balancing reactor from supporting all the voltage for awhile and upsetting the balancing arrangement. Should the reference transistor short, the fuseable-link-operated relay converts the reference balancing arrangement over to a different type of balancing scheme wherein the currents in all the transistors are forced to be equal because of the same current circulating in the now series connected secondaries of the balancing reactors. Thus, with this scheme, failure of the reference transistor does not result in failure of the balancing scheme. Diodes

D_7 and D_8 serve the same purpose for the reference transistor that the diodes D_5 and D_6 do for the ordinary power switching transistors; in the event that the reference transistor opens instead of shorts, the balancing reactor secondaries still have a current path. (The operation of the fusible links is discussed on page 30.

Each primary of the two sets of output transformers has its three properly ratioed secondaries connected in series with the secondaries from the other transformers from that set to form a three-phase set of output voltages, each of which, line to neutral, looks like Figure 2-6. The multi-stepped outputs from the two sets of 6 output transformers are then also added in series to yield the final set of three-phase output voltages. The exact waveshape of the total output will vary because of the variation in phase displacement between the corresponding outputs of the two six square wave sets but in any event will contain no more harmonic voltage than the sum of the individual multi-stepped outputs. (The percentage of harmonics will, in general, go up as the phase displacement between the two multi-stepped outputs increases because the fundamental component decreases. If the phase displacement between the outputs is θ, and each has amplitude A_1, the amplitude of the fundamental component of the combined output will be $2A \cos \theta/2$. Similarly, if the amplitude of the nth harmonic in each wave is A_n, then the component of that harmonic in the combined output will be $2A_n \cos n\theta/2$. It can

be seen that the amplitude of, say, the 11th harmonic will have several maxima and minima in the range for $0 \leq \theta \leq \pi$ where the amplitude of the fundamental is a constantly decreasing function.)

For the 10 KW inverter, the number of power transistors required on each side of each switch would be four (the same as the number actually shown on the drawing of Figure 2-24). Since the circuit has been designed so that failure of the reference transistor does not result in failure of the balancing network, the reference transistor is operated at the same current as the other power switches. Under these conditions (4 transistors total per side, with reference transistor carrying full load) the peak collector current in each of the transistors will be less than 75% of their rated maximum under the worst case condition of 200% load on all phases. (The phase angles of the loads were also assumed to be those which would provide the worst possible vector summation of load currents for the phase under consideration). Even should one of the four transistors fail, the remaining three will not be stressed over their ratings on the 200% overload. Similarly, two of the transistors could fail and the unit still carry the normal 100% load.

G. Output Filter

The output filter serves two purposes. The first and most obvious is the reduction of the harmonic content of the power switching stage

output to a value required by the load. The second is the isolation of the load from the power switching stages. The necessity for this latter requirement is made more evident by considering the following. Assume a short circuit is applied to the output. With no filter, the rise of output current would be limited only by the internal impedance of the power switching stages. Hence, there is a very serious problem in getting the overload detection circuit to sense and correct for the overload before damage is done. However, with a filter between the power switching stage and the load, the (shunt sections of the) filter supply the instantaneous current demanded by the load and required to activate the overload detection circuits. Because of the filter impedance, there is a definite time required for the current to build up in the power switching stage. For an example, consider the usual filter circuit shown in Figure 2-25A. With the filter impedances as shown, and a short circuit applied, in 1/4 cycle the current taken from the source can increase by an amount equal to the normal full load current. For filters with elements having a higher impedance relative to the load than this one, the rise is less rapid, and conversely. Previous experimentation with filters has led to the configuration of Figure 2-25B as having a slower rate of rise of current under short circuit conditions for the same element values as the filter of Figure 2-25A. (This has not as yet been verified analytically).

The filter of Figure 2-25C was the configuration tentatively chosen for the 10 KW transistorized inverter and the element values indicated on the figure are those required for the amount of harmonic reduction required by the multi-stepped output of the selected power stage. These were calculated to prevent the amplitude of the lowest harmonic (the 11th) from exceeding 2% of the fundamental under the worst loading and input conditions of no load and maximum input voltage.

H. Voltage and Current Regulator

As indicated previously, the voltage and overcurrent controls operate on the variable pulse delay networks to provide a phase shift between the two multi-stepped outputs such that the fundamental component of the output voltage after filtering is the desired value (or is small enough to limit the current to the specified value). However, because of the interconnections between phases, any voltage control that works in this fashion must of necessity regulate all three phase voltages simultaneously, since there is no means of varying the phase of one and not the other. Since unbalanced loading or unbalanced voltage drops in the filters are the only means by which one phase voltage may be affected differently from the others, if it were not for these effects, it would be possible to voltage regulate only by varying all three phases simultaneously as the proposed system does.

Since some unbalance in phase output voltages is allowed (so long as

no voltage goes out of the specification limits) an analytical investigation was made in order to determine the amount of voltage unbalance that could be expected. As in the case of the determination of the peak current in the transistors, the interconnection of all the phases makes it difficult to determine what the worst loading condition would be. However, a loading condition of 0.8 pf, full rated KVA was used to load one phase, and the other two phases were left unloaded. It was assumed that the filter elements were tuned so that at rated current, the inductive and capacitive reactances in the series section were within 5% of each other. The variations in the magnitude of the phase voltages were then due to:

1. resistive drops in the filter,
2. resistive drops in the output transformer
3. resistive drops in the power switches and reactive diodes.

Similarly, phase shifts in the output were due to

1. phase shift in filter due to inexact tuning of elements,
2. phase shift in the power switching stages due to variations in the current crossover points under unbalanced load. (When the current transfers from a power switching transistor into the corresponding reactive diode, the voltage drop changes from + 0.5 v to -1.0 v for example. The

sign change is due to the fact that the reactive diode drop adds to the output voltage whereas the transistor drop subtracts from it). When the voltage drops and phase shifts due to these different sources were computed, the following results were obtained:

	ØA (rated KVA, 0.8pf)	ØB (unloaded)	ØC (unloaded)
XFMR resistive drop	-0.5%	-	-
Filter resistive drop	-0.2%	-	-
Pwr. stage res. drop*	+ 0.54%	+ 2.16%	+ 0.36%
Filter Ø shift	- 0.7°	-	-
Switching stage Ø shift	- 0.5°	+ 0.4°	-0.3°
Total	-.16% -1.2°	+ 2.16% + 0.4°	+.36%-0.3°

The voltage regulator, which regulates the average of the three line-to-neutral voltages will raise or lower all three voltages until the average change is zero. Hence, in this case, since the average output voltage has risen by 1/3 (-.16 + 2.16+ .36%) = 0.79%, each of the above voltages is lowered by that amount (0.79%) to yield a net output voltage change and phase shift as follows:

ØA	ØB	ØC
-.95%, -1.2°	+ 1.38% + 0.4°	-0.43%, ± -.3°

* This theoretical rise in voltage with load is due to the reactive diode drop (which occurs because of the 0.8 power factor, and actually tends to increase the output) being of greater magnitude than the resistive drop due to increased current in the switching transistors.

Thus, all voltage variations remain in within ± 2% of nominal and the phase separation between any two outputs does not deviate from the ideal by more than 2° (the actual maximum deviation in this case is 1.6°). Hence, no additional circuitry is needed for individual voltage or phase regulation to meet the specifications.

The actual operation of the voltage and overload current feedback system is relatively straightforward. Referring to Figure 2-26, the full wave rectified line-to-neutral outputs of the three phases are averaged by R_1 and C_1 and compared in Q_1 to the reference voltage established by D_1. Similarly, should any of the line currents exceed a certain value, the rectified outputs of the current transformers will exceed the value of the zener voltage and activate the amplifier circuit in the same manner as an overvoltage would. The two output voltages that make up each unfiltered phase output are thus phase shifted with respect to one another until the resultant output is reduced to either satisfy the voltage regulator or, in the event of an overload, to provide a resultant output low enough so that the resultant current is limited to 200%. In the event that this regulator or the magnetic amplifiers which it drives cannot act rapidly enough to prevent transient overcurrents in the transistors in the case of a short circuit or suddenly applied heavy overload auxiliary circuits can be used to temporarily remove the drive from all transistors until the slower acting phase shift regulator has had time to act.

I. D.C. Input Filter

The d.c. input filter serves two purposes. It attenuates any spikes or other high frequency signals on the d.c. input lines, preventing them from damaging the output transistors or causing a malfunction of the inverter control circuitry. The filter also serves to suppress any radio frequency interference generated by the inverter, preventing it from interfering with other equipment. This filer would, of course, be of the low pass type. The filter normally used to attenuate the power switching stage output harmonics performs these RFI reducing functions on the a.c. output lines, so no additional circuitry is needed here.

J. Logic D.C. Voltage Regulator

Because of the wide variation in d.c. input voltage, a voltage regulator is used to supply a constant voltage d.c. to the low level logic and drive circuitry. This improves the stability of operation of these circuits and allows them to be optimized for operation at the known power supply output voltage. If a non-dissipative (switching) regulator is used, this can result in considerable power savings in the driver stage since, with an unregulated supply, a driver stage design which provides adequate drive at the lowest input voltage will be providing considerable overdrive (with its attendant power losses) at high input levels. Many circuits for this purpose are available; further effort

will not be devoted to them here.

K. Start Circuit

When the inverter is first energized, the starting circuit delays the application of B+ to the flip-flops and variable pulse delay circuit until the turn-on transients have subsided and the master oscillator output has reached its steady state value. Combined with the preferential starting in the flip-flops, this results in the inverter always turning on in the same predictable state.

III. SCR Output Stage Inverter

A. General Description

The block diagram for the SCR inverter is given in Figure 2-27. Comparison of this with the block diagram for the transistorized inverter (Figure 2-19A) will indicate the considerable similarity between the two designs. However, in almost all cases, the design of the SCR unit is simpler than that of the transistorized model. This is due to the reduction in number of steps making up the output waveform. Except for this reduction in the number of steps making up the output waveform, and the functioning of the power stage, the operation of this inverter is essentially the same as that of the transistorized inverter described earlier. The individual circuits in the SCR inverter which are different from those used in the

to the appropriate pair of SCR's immediately after the low-level drive to the power SCR has dropped off and before the other power SCR has been turned on. These waveforms are shown in Figure 2-28, and a circuit for producing them in Figure 2-29.

C. Power Stage

The power output stage selected is shown in Figure 2-17 and will be recognized as the McMurray inverter discussed on pages 116-118 of the first quarterly report. This circuit was chosen because it is capable of operating with reasonable efficiency at high frequencies. The six power switches in the SCR inverter have their secondaries interconnected as shown in Figure 2-30, yielding an output voltage waveform as shown in Figure 2-31.

To determine whether or not individual phase voltage or phase angle regulation was required with the SCR inverter, an analysis similar to that carried out for the transistorized inverter was performed. The results of the analysis show that with 0.8 pf rated KVA load applied to ØA only, with ØB and ØC on open circuit, after the voltage regulator has acted, the phase voltages and phase shifts are as follows:

Ø A -3.9%, + 3° ØB + 2.0%, -0.4° ØC + 2.0%, -0.4°

Thus, inverter circuit would not meet the specifications as originally set forth (± 2% on voltage regulation, ± 2° on phase separation). The

transistorized version are discussed below; those circuits which are essentially the same in their operation and purpose and differ only by modification of some parameter will not be examined further. These are the master oscillator-pulse shaper (which now supplies pulses at 6X the inverter output frequency instead of 12X), the variable delay circuit (which now requires only half the number of delay stages as before to accomplish the same function because of the reduction in input pulse frequency), the d.c. input filter, the logic d.c. voltage regulator, the start circuitry, the three-phase countdown circuit (which generates 3 square waves spaced 60° instead of 6 spaced 30°) and the filter (which now, because of the increased harmonic content of the power stage output waveform, must be increased in size to provide additional harmonic attenuation).

B. Driver Stage

The drive waveform requirements of the power switching SCR's are similar to those of the power transistor; a large pulse of current at the beginning to insure quick turn-on of the SCR, then a smaller steady state drive to hold the SCR on should the load current momentarily reverse. In addition to the drive for the power switching SCR's however, a drive for the commutating SCR's is also needed. Preliminary analysis indicates that an adequate commutating SCR drive (for square wave operation) would consist of a high level pulse

increased voltage and phase shifts in this circuit are due to the larger filter required (approximately 3X that of the transistorized inverter) and the higher forward drops of SCR's as compared with transistors.

(Note: This analysis was actually performed for a circuit with output connections as shown in Figure 2-32, the output of which (shown in Figure 2-33) while appearing different, has approximately the same harmonic content as that of Figure 2-31. In fact, Figure 2-33 is the line-to-line output voltage of Figure 2-30, and Figure 2-31 is the line-to-line output voltage of Figure 2-32. The circuit of Figure 2-30 was later chosen as the actual circuit to use for the inverter because of the more even distribution of phase loads obtained with this circuit. It is not expected that a re-analysis would produce significantly differing results).

It was felt that the addition of individual phase voltage and phase shift feedback loops to allow this circuit to meet the original specifications would greatly nullify the simplicity and low parts count advantages of this circuit. Hence, it was felt that one of the specifications which it might be of considerable advantage to modify would be the requirements of phase shift and voltage unbalance under unbalanced load conditions.

D. Voltage and Current Regulator

The voltage and current regulation in the SCR inverter is performed in essentially the same manner as in the transistorized unit (by phase shift techniques). Again, in the event that the proposed circuitry acts too slowly to prevent excessive currents from flowing in the switching elements under conditions of step overloads and short circuits, an auxiliary circuit which fires the appropriate commutating SCR's and stops the turning on of the power switching SCR's can be used. This differs somewhat from the transistorized circuit wherein it is only necessary to remove the drive to prevent overcurrents.

V. Comparison and Results

The anticipated weights and losses of all significant components in both the transistor and SCR versions of the inverter were computed and tabulated. In addition, the total number of components of each type in each inverter was tabulated. The results are given in Tables 2-1 and 2-2. Unless otherwise indicated, these designs were for a 10 KVA unit operating from a nominal 28 volt source built to meet all the specifications given in the first quarterly report (p. 9). It can be seen that the SCR inverter has only about half as many parts as the transistor inverter. However the efficiency of SCR inverter is not as high as its transistor counterpart (64% vs 70%) and it weighs more (62.25 lbs. vs 50 lbs.).

Improvements in efficiency can be obtained by a) increasing the weight of

the transformers and chokes; b) operation at input voltages higher than 28 VDC thus reducing the forward conduction loss because of reduced current levels; c) improvement in the switching devices themselves such as lower saturation resistance and faster switching speeds in transistors and reduced forward drop and turn off time in SCRs.

An analysis of the tradeoff curve between weight and efficiency at various input voltages and power levels for the 3200 cps inverter will be done in following reports. With these tradeoff curves the system designer can choose the inverter design which involves a weight which is just sufficient to reduce the inverter power loss to the optimum point. At this optimum point any further decrease in inverter weight which will cause increased inverter losses is more than balanced by the increased weights of other spacecraft subsystems which must interface with the inverter. These other subsystems such as the power source and the heat sink will increase in weight because they must be sized to handle the increased inverter losses. Conversely an increase in inverter weight from the optimum point will reduce inverter losses but not to the extent that the decrease in other subsystem weights, due to decreased inverter losses, will compensate for the increased inverter weight. Obviously the weight-loss penalties in each interfacing system of the spacecraft must be known before a truly optimum inverter design can be carried out.

With the tentative 3200 cps transistor design which is tabulated in Table 2-1, the power to weight figure of merit is 200 VA per pound of functional weight.

This is approximately five times greater than an equivalent 400 cps inverter design. This difference in the power to weight figure of merit illustrates the desirability of utilizing conditioned 3200 cps power if system considerations permit.

FUTURE WORK

In the next quarter, the design of the 3200 cycle inverter will be finalized and the reliability analysis of it will be started.

The most promising of the possible designs for the low and mid power inverters will be evaluated for weight, efficiency, and parts count as a step in arriving at an optimum design in these power ranges.

More work will also be performed on optimizing multi-stepped waveform inverters, both on the choice of waveform and the design of special transformers for use with these special waveform sets.

APPENDIX 2-I

Optimum Loading of a Fixed Transformer

The general rule regarding the optimum loading of a transformer is that maximum efficiency occurs when the copper loss and core loss are equal. This result can be obtained as follows:

For a constant voltage V_1, applied to the input, the total core loss P_c, will be constant. The total copper loss, P_R (neglecting the primary copper loss due to magnetizing current) will be proportional to the square of the input (or output) current, i.e., $P_R = k_1 I_1^2 = k_2 I_2^2$ (2-I-1) (where k_1 and k_2 are constants of proportionality dependent on the turns ratio and primary and secondary winding resistances of the transformer.) The total loss, P_T is then given by

$$P_T = P_c + P_R = P_c + k_1 I_1^2 \tag{2-I-2}$$

Assuming an output power of P_o into a purely resistive load, the input power, P_{in}, will then be

$$P_{in} = P_o + P_T \tag{2-I-3}$$

The efficiency, η, of the transformer is given by

$$\eta = \frac{P_{in} - P_T}{P_{in}} = 1 - \frac{P_T}{P_{in}} = 1 - \frac{P_T}{P_o + P_T} \tag{2-I-4}$$

The maximum is found by differentiating with respect to the output power

and equating to zero, to obtain:

(2-I-5)

$$\frac{d\eta}{dP_o} = \frac{d}{dP_o}\left(1 - \frac{P_T}{P_o + P_T}\right) = \frac{-(P_o + P_T)\frac{dP_T}{dP_o} + P_T \frac{d}{dP_o}(P_o + P_T)}{(P_o + P_T)^2}$$

This has the solution

$$\frac{dP_T}{dP_o} = \frac{P_T}{P_o} \tag{2-I-6}$$

Since $P_T = P_c + k_2 I_2^2$ and $I_2 = \frac{P_o}{V_2}$

$$\frac{dP_T}{dP_o} = \frac{dP_T}{dI_2}\left(\frac{dI_2}{dP_o}\right) = 2k_2 I_2\left(\frac{1}{V_2}\right) = \frac{P_c + k_2 I_2^2}{I_2 V_2} \tag{2-I-7}$$

This has the solution

$$P_c = k_2 I_2^2 = P_R \tag{2-I-8}$$

which seems to verify the rule given at the beginning of this section, i.e., maximum efficiency occurs when the core loss and copper losses are equal. This derivation, however, is based on the conditions of a constant input voltage and variable load. In practice, however, both the input voltage and design load are generally fixed, and all that can be varied is the overall size (and/or shape) of the transformer and the relative losses in the coil and core. An optimization based on these restrictions will now be derived.

To start, it will be assumed that the size and shape of the transformer are fixed, and only the relative core and coil losses can be varied. This variation is obtained because as the core losses are reduced by decreasing

the induction level, which is done by increasing the number of turns, the resistance of the windings goes up, both because of the increased number of turns and the decreased cross-sectional area available for each turn, thus increasing the copper losses. In order to allow further expansion of these results for cases where the size of the transformer is varied, the parameters of the transformer will be obtained in terms of one of its linear dimensions.

The derivation for the conditions yielding maximum efficiency are as follows:

From empirical results[4], (shown typically in Figure 2-I-1 and Figure 2-I-2), the core loss per unit volume, p_c, can be expressed by the equation

$$p_c = c_1 B^a \tag{2-I-9}$$

where c_1 and a are constants (at any given frequency) and B is the maximum flux density. B as a function of the number of turns on the primary winding, N, the applied voltage, V_o, and the linear dimension, L, can be written.

$$B = \frac{c_2 V_o}{NL^2} \tag{2-I-10}$$

Therefore, p_c, the core loss per unit volume is given by

$$p_c = c_3 \left(\frac{c_2 V_o}{NL^2} \right) \tag{2-I-11}$$

Since the core volume is proportional to L_3, the total core loss P_c is then:

$$P_c = L^3 c_3 \left(\frac{c_2 V_o}{NL^2} \right)^a \tag{2-I-12}$$

The resistance of the winding as a function of L can be determined as follows:

The mean length/turn of wire, ℓ, is directly proportional to L. The window area available for wire, A_w, is directly proportional to L^2.

A, the cross-sectional area of the individual wires of the coil winding, is directly proportional to the window area A_w, and inversely proportional to N, the number of turns. (For simplicity, the transformer may be imagined to have a 1:1 turns ratio, with primary and secondary of equal size wire wound side by side).

ℓ_T, the total length of one winding is proportional to N $(\ell_T = N\ell)$ and R, the total winding resistance, is proportional to the total length of wire, ℓ_T, and inversely proportional to its cross-sectional area. These proportionalities can then be combined to yield an expression for the total winding resistance as reflected to the primary.

$$R \propto \frac{\ell_T}{A} \propto \frac{(N\ell)}{A_w/N} = \frac{N^2\ell}{A_w} \propto \frac{N^2 L}{L^2} = \frac{N^2}{L} \qquad (2\text{-I-}13)$$

$$\text{or } R = \frac{kN^2}{L} \qquad (2\text{-I-}14)$$

where k is a constant of proportionality which takes into account the conductor material and all the constants of proportionality not explicitly indicated in the proportionality equation 2-I-13.

The copper loss, P_R, for an input current I_o is then

$$P_R = I_o^2 R = \frac{I_o^2 k N^2}{L} = \frac{r N^2}{L} \qquad (2\text{-I-}15)$$

where

$$r = k I_o^2 \qquad (2\text{-I-}16)$$

The total loss in the transformer, P_T, is then

$$P_T = P_R + P_c = \frac{r N^2}{L} + c L^3 \left(\frac{V_o}{N L^2} \right)^a \qquad (2\text{-I-}17)$$

With V_o and L_o held constant, the input power is constant; thus, the efficiency (and output power) will be a maximum when

$$\frac{dP_T}{dN} = 0 \qquad (2\text{-I-}18)$$

Equating this derivative to zero results in the equation

$$\frac{dP_T}{dN} = \frac{2rN}{L} - acL^3 \left(\frac{Vo}{L^2} \right)^a N^{(-a-1)} = O \qquad (2\text{-I-}19)$$

which has the solution

$$N = \left[\frac{acL^4 - 2a V_o^a}{2r} \right]^{\frac{1}{a+2}} \qquad (2\text{-I-}20)$$

(The fact that this unique solution for N is indeed a minimum of 2-I-17 and not a maximum is evident from the fact that P_T as given by equation 2-I-17 is a continuous function of N for $N > O$ and $P_T \to \infty$ as $N \to O$ or $N \to \infty$. Therefore, since P_T is finite and continuous for finite $N > O$, it must have an extemum which is a minimum for some finite non-zero N.)

If the value of N as given by equation 2-I-20 is substituted into the valu of P_R and P_C given by equations 2-I-15 and 2-I-12 respectively, and the ratio P_C/P_R is evaluated, the following result is obtained

$$\frac{P_c}{P_R} = \frac{2}{a} \qquad (2\text{-I-}21)$$

Thus, for maximum efficiency in a transformer operating at a given power level, the core losses should be chosen equal to 2/a times the copper losses. ("a" is defined in equation 2-I-9, and is determined empirically from core loss data). Since "a" is not generally equal to 2, this result is in contradiction to the general rule that for maximum efficiency, the core loss is chosen equal to the copper loss. The only assumptions used in this derivation are that the copper losses due to the magnetizing current can be neglected (which is the same assumption used in the derivation of equation 2-I-8), and that the core losses can be adequately represented by equation 2-I-9. That equation 2-I-9 adequately represents the core loss can be seen from the curves of Figures 2-I-1 and 2-I-2 which are taken from a Magnetics Inc. catalog.[4] From these curves the values for "a" and "c" at the operating frequency can be obtained. "a" can be evaluated either by writing the equations for two points on the curve and solving:

$$\text{i.e.} \quad 0.9 = C\,(400)^a \quad \text{which yield } a = 1.44 \qquad (2\text{-I-}22)$$

$$80 = C\,(9000)^a$$

or, if the curves are plotted on log-log paper with equal (physical) length

cycles on both x and y axes, the slope of the straight line, which can be shown to be equal to "a", can be obtained by actual linear measurements made on the graph as shown on Figure 2-I-2. (This value varies with frequency and material).

For 48 alloy at 10,000 cps "a" has the value of 1.45, computed as indicated in Figure 2-I-2. (This is based on sinusoidal excitation; since the slope of the lines decreases as the frequency increases, the value of "a" for square wave excitation will be slightly less than that for sine wave, due to the fact that the square wave contains components of higher frequencies (which have smaller a's) along with the fundamental.) Thus, it has been shown that as the load is varied on a transformer operating at a fixed input voltage, the maximum efficiency is obtained when the copper loss and core loss are equal. However, although this gives the maximum efficiency for the transformer when operated at the given voltage with a variable load, this efficiency is not the greatest of all possible efficiencies obtained by using that transformer to provide a given VA load; with a redesign to operate at an increased flux density (i.e. increased core loss) and reduced copper loss, the same VA can be handled with smaller loss. This can be shown most readily by using ths same transformer under two different conditions: in the first it is operated at voltage and current levels such that its core and copper losses are equal and the power output is P_o. (This corresponds to the usual design technique and will be called Case I.) For the second case, the transformer will be operated to

provide the same output power P_o, but with voltage and current levels such that the core and copper losses are related by the equation

$$P_C = (2/a)\, P_R \quad \text{(This will be called Case II)}$$

Since the dimensions, number of turns, etc., of the transformer are not going to change, in evaluating the losses obtained while operating in each condition, equation 2-I-12 can be simplified to:

$$P_{CI} = c_2 V_I^a \tag{2-I-23}$$

where c_2 is a constant of proportionality, P_{CI} is the core loss under the conditions of Case I and V_I is the applied voltage under these same conditions. Since $P_o = V_I I_I$ (where I_I is the current under Case I conditions) and $P_R = RI_I^2$ where R is the winding resistance, the values of V_I and I_I can be obtained as follows:

$$P_{C\,I} = P_{RI} = I_I^2 R = \left(\frac{P_o}{V_I}\right)^2 R = c_2 V_I^a \tag{2-I-24}$$

Then,

$$V_I^{a+2} = \frac{P_o^2 R}{c_2} \quad \text{or} \quad V_I = \left(\frac{P_o^2 R}{c_2}\right)^{\frac{1}{a+2}} \tag{2-I-25}$$

and

$$I_I = \frac{P_o}{V_I} = \frac{P_o}{\left(\frac{P_o^2 R}{c_2}\right)^{\frac{1}{a+2}}} = P_o^{\frac{a}{a+2}} \left(\frac{c_2}{R}\right)^{\frac{1}{a+2}} \tag{2-I-26}$$

P_{TI}, the total power lost in the transformer under the conditions of Case I is then given by:

$$P_{TI} = P_{cI} + P_{RI} = 2P_{RI} = 2I_I^2 R = 2R\left[P_o^{\frac{a}{a+2}} \left(\frac{c_2}{R}\right)^{\frac{1}{a+2}}\right] \quad (2\text{-I-}27)$$

Similarly, the voltage and current applied to the transformer to result in operation under the Case II conditions are obtained as follows:

$$P_{cII} = \frac{2}{a} P_{RII} = \frac{2}{a} I_{II}^2 R = \frac{2}{a}\left(\frac{P_o}{V_{II}}\right)^2 R = C_2 V_{II}^a \quad (2\text{-I-}28)$$

or

$$V_{II}^{a+2} = \frac{2}{a}\frac{P_o^2 R}{C_2} \quad \text{or} \quad V_{II} = \left[\left(\frac{2}{a}\right)\frac{P_o^2 R}{C_2}\right]^{\frac{1}{a+2}} \quad (2\text{-I-}29)$$

and

$$I_{II} = \frac{P_o}{V_{II}} = P_o^{\frac{a}{a+2}}\left[\left(\frac{a}{2}\right)\frac{c_2}{R}\right]^{\frac{1}{a+2}} \quad (2\text{-I-}30)$$

P_{TII}, the total power lost in the transformer under the conditions of Case II ($P_C = 2/a\ P_R$) is then given by

$$P_{TII} = P_{cII} + P_{RII} = I_{II}^2 R + c V_{II}^a =$$

$$P_o^{\frac{2a}{a+2}}\left[R\left(\frac{ac_2}{2R}\right)^{\frac{2}{a+2}} + c_2\left(\frac{ac_2}{2R}\right)^{\frac{-a}{a+2}}\right] \quad (2\text{-I-}31)$$

The ratio of P_{TI}/P_{TII} can then be evaluated and simplified to:

$$\frac{P_{TI}}{P_{TII}} = 2\Big/\left[(a/2)^{\frac{2}{a+2}} + \left(\frac{2}{a}\right)^{\frac{a}{a+2}}\right] \quad (2\text{-I-}32)$$

A plot of this ratio for values of a from 1 to 3 is shown in Figure 2-1. From this it can be seen that except for the case where a = 2 (where the two designs are equivalent), the losses in a transformer designed with equal copper and core loss will be greater than those in a transformer designed for a core loss 2/a times the copper loss. The actual differences in loss are not very great, however, as can be seen from Figure 2-1. When these loss variations are translated into efficiency variations, the difference is further suppressed, as shown by the following example.

Assume the original design of the transformer (for equal copper and core loss) yielded an efficiency of 95% and the "a" value of the core material was 1.4.

Since, for high efficiency units,

$$P_T \cong P_o (1 - \eta), \tag{2-I-33}$$

$$\Delta \eta \cong \frac{1}{P_o} \Delta P_T \tag{2-I-34}$$

the change in losses can be written $P_T = P_T$ (1-loss ratio). The change in efficiency can thus be written:

$$\Delta \eta = \frac{1}{P_o} (1 - \eta) P_o \text{ (1-loss ratio} \tag{2-I-35}$$

The loss ratio for this case (from Figure 2-1) is 1.015, thus $\Delta \eta$ = -5 (.015)1% = + 0.75% and the new efficiency is then 95.075%. Thus, the improvement is not significant. However, the new transformer will have better load regulation than the original, due to the reduced

copper losses; the no-load losses will be higher than in the original because of the higher core loss. The fact that this design allows the core losses to be increased above the usual amount without penalty (for $a < 2$) is of value in the case of high-frequency transformers, where the core loss generally limits the flux density. (Saturation is generally the limitation in low frequency 60 cps units). Of course, in practice, one is also generally limited to standard sizes of core and wire, thus very small changes in size cannot be effected. Although not of significant practical importance, this result will be useful in further theoretical investigations.

APPENDIX 2-II

Relationships Between Size, Weight and Losses in Transformers

The following analyses of the losses in transformers delivering constant power as their size (and hence weight) is varied indicates the trade-offs involved in transformer design.

Equation 2-I-17 expresses the transformer losses as a function of L, the linear dimension of the transformer. Simplifying this, and combining terms in L results in

$$P_T = \left(1 + \frac{2}{a}\right) P_R = \left(1 + \frac{2}{a}\right) \frac{rN^2}{L} = \left(1 + \frac{2}{a}\right) \frac{r}{L} \left[\frac{acL^{4-2a} V_o^{\,a}}{2r}\right]^{\frac{2}{a+2}} \qquad (2\text{-II-}1)$$

$$= \left(1 + \frac{2}{a}\right) r \left(\frac{ac V_o^{\,a}}{2r}\right)^{\frac{2}{a+2}} L^{\frac{6-5a}{a+2}} \qquad (2\text{-II-}2$$

The variation of the total losses, P_T, with L is obtained by differentiating equation 2-II-1 with respect to L to obtain:

$$\frac{dP_T}{dL} = \left[\frac{6-5a}{a+2}\right] \left(1 + \frac{2}{a}\right) r \left(\frac{acV_o^{\,a}}{2r}\right)^{\frac{2}{a+2}} L^{\frac{4-6a}{a+2}} \qquad (2\text{-II-}4)$$

From the empirical data, $a > 1$ and therefore the exponent of the L term is negative (although the term itself is still positive). Since for $a < 1.2$, the coefficient $\frac{6-5a}{a+2}$ is positive, the curve of P_T versus L is always sloping upward, making P_T an ever increasing function of L. It must, therefore, have a minimum at the lowest possible value of L.

However, the maximum flux density in the core material is related to the applied voltage, V (which is constant), the number of turns on the core, N, and the linear dimension, L, by the equation

$$B = \frac{V}{NbL^2} \qquad (2\text{-II-3})$$

(where b is a constant of proportionality).

Substituting into this equation the value of N in terms of V, L, and the physical and magnetic constants of the core, there results

$$B = \frac{V}{bL^2\left[\frac{acL^{4-2a}V^a}{2r}\right]^{\frac{1}{a+2}}} = \frac{V}{b\left[\frac{acV^a}{2r}\right]^{\frac{1}{a+2}} L^{\frac{8}{a+2}}} \qquad (2\text{-II-4})$$

This equation indicates that B is an ever decreasing function of L. Furthermore, in the limit as L approaches zero, B increases without limit. Since these equations have been derived only for the cases where the core material is not saturated, there is a minimum value of L for which these equations hold. These facts can be combined to give the final result that for a transformer operating at a fixed power level, (and with a core material having a value of "a" less than 1.2) as long as the core does not saturate (and N is given by equation 2-I-20), the smaller the physical size of the transformer, the smaller its losses. Square permalloy 80, made by Magnetics Inc., has a value for "a" at 400 cycles of 1.18, which puts it in this category.

When $a = 1.2$ $\qquad \frac{dP_T}{dL} = 0$ for all L.

(The coefficient $\frac{6-5a}{a+2} = 0$ for $a = 1.2$) Optimum transformers made with cores of material with $a = 1.2$ would have the same losses when operating at the same power level, independent of their size.

For $a > 1.2$ normal design concepts hold, and larger transformers are more efficient than smaller ones (with the same core material and operating at the same power level). With the weight of a transformer also being of considerable importance in space applications, it can be seen that, with $a < 1.2$ we have an ideal situation, where both the losses and the weight are minimized simultaneously as the transformer is made smaller. However, most materials have values of $a > 1.2$, which means that to reduce losses, transformer size (and hence weight) must be increased. (Square supermalloy 80, with $a = 1.18$ has too low a saturation flux density for practical use in these applications). Thus, neither parameter can be optimized without degrading the other. In this situation, one possible solution is to optimize the product of the two. Since the weight is proportional to L^3 (equation 2-58), the weight-loss product can be written

$$WP_T = c_3 L^3 \left(1 + \frac{2}{a}\right) r \left[\frac{acV_o{}^a}{2r}\right]^{\frac{2}{a+2}} L^{\frac{6-5a}{a+2}} \qquad (2\text{-II-5})$$

Combining terms in L in equation 2-48A and then differentiating with respect to L yields:

$$\frac{d(WP_T)}{dL} = c_3 \left(1 + \frac{2}{a}\right) r \left[\frac{acV_o{}^a}{2r}\right]^{\frac{2}{a+2}} \frac{d}{dL} L^{\frac{12-2a}{a+2}}$$

$$= \frac{12-2a}{a+2} \left[c_3 \left(1 + \frac{2}{a}\right) r \left(\frac{acV_o{}^a}{2r}\right)^{\frac{2}{a+2}} L^{\frac{10-3a}{a+2}}\right] \qquad (2\text{-II-6})$$

This is clearly > 0 for $a < 6$ (which covers all commonly used core materials). Thus, since the weight-loss product is an ever increasing

function of transformer size, to obtain a transformer operating at a fixed power level with a minimum weight-loss product, the smallest transformer designed according to equation 2-II-20 that can handle the required core flux without saturating should be used.

These general results are indicated in the graphs of Figures 2-II-1 through 2-II-4. Figures 2-II-1, 2-II-2 and 2-II-3 show the variation in total loss (copper loss plus core loss) of transformers operating at constant power and frequency which are varied in size while their shapes remain fixed. Figure 2-II-1 shows this variation for a transformer made with a core material having a value of "a" (refer to equation 2-I-9 for the definition of "a") less than 1.2; Figure 2-II-2 is for a = 1.2, and Figure 2-II-3 is for the case where a $>$ 1.2. (These transformers are all designed so that their core loss is 2/a times the copper loss). Because, for a constant voltage input, the core flux density is related to the size of the transformer by equation 2-II-4, as the size of the transformer is decreased, the flux level in the core increases until some maximum flux density is reached. Thus, there is a minimum size for a transformer operating at a fixed frequency and power level beyond which size it is not possible to arrive at a design which will satisfy equation 2-I-21 and still have physically realizable flux densities in the core. These minimum sizes are indicated by the dashed lines of Figures 2-II-1 through 2-II-4.

The weight-loss product as a function of size of transformers designed according to equation 2-II-4 is indicated in Figure 2-II-4. Depending on the shape of the transformer and the core and coil materials used, the weight-loss product for different designs will be different for the same size transformer, as shown in Figure 2-II-4. Thus, each curve of Figure 2-II-4 represents a different transformer design (toroidal, E-core, C-core, for example) which is scaled up or down in size to decrease or increase respectively the core operating flux density. (The transformers are all operated at the same constant output power level).

However, in all cases, the minimum value of the weight-loss product will occur at the maximum value of flux density allowed by the core material. (This also corresponds to the minimum transformer size).

APPENDIX 2-III

Thermal Considerations in Transformers

Since the thermal paths are shorter in smaller devices, the thermal problem indicated in section IV would tend to favor splitting up larger units into smaller ones. This is brought out by the following analysis:

Suppose a transformer is designed for a power level of P_o and has a linear dimension (L) equal to L_o.

Looking now only at the thermal problems associated with the core losses, the thermal equivalent model of a transformer core mounted with one side on a heat sink is as shown in Figure 2-III-1. Since the problem is essentially one dimensional, the temperature across the entire core cross-section at any fixed distance x from the heat sink plate will be identical. Let the temperature difference between any point on the heat sink and the plane through the core parallel to the heat sink at a distance x be represented as T(x). Then, as one moves a distance Δx along the core, there will be a temperature differential of ΔT given by $\Delta T = \theta (\Delta x) \phi$ where $\theta \Delta x$ is the thermal resistance of the cross-sectional piece and ϕ is the total heat flux passing through this piece. (θ factors in the thermal resistance of the core material). If heat is being generated equally in all small volumes of the solid, then $\phi = \frac{\varphi_o L_o (L_o - x)}{L_o}$ where φ_o is the heat flux generated per

unit volume of core material. Since the end of the core away from the heat sink is the hottest, its temperature is the one we are interested in and this is given by:

$$T_I = \int_o^{L_o} \Delta T(x) = \int_o^{L_o} \theta\,(\Delta x)\,\phi = \int_0^{L_o} \theta\varphi_o (L_o - x)dx = \theta\varphi_o \frac{L_o^2}{2} \qquad (2\text{-III-1})$$

If the one large transformer (dimenson L_o) is split into two smaller units (each of half the power rating of the original) then the linear dimension of each of these will be (by equation 2-7).

$$L' = \frac{L_o}{\sqrt[4]{2}} \qquad (2\text{-III-2})$$

If the transformers are of similar design, then the core losses/unit volume will be the same in the two units, and hence the thermal rise in the second will be (from equation 2-III-1)

$$T_{II} = \frac{\theta\varphi_o}{2}\left[\frac{L_0}{\sqrt[4]{2}}\right]^2 = \left(\frac{\theta\varphi_o L_o^2}{2}\right)\left(\frac{1}{\sqrt{2}}\right) = \frac{T_I}{\sqrt{2}} \qquad (2\text{-III-3})$$

In other words, (for equal core loss/unit volume) the thermal rise in the smaller unit will only be $1/\sqrt{2}$ that of the larger or, for the same thermal rise, the smaller unit can be designed with $\sqrt{2}$ times the core loss of the larger.

The redesign of the smaller transformer to have $\sqrt{2}$ times the core loss of the larger one proceeds as follows:

With the core loss approximately proportional to B_{max}^{2} (the actual exponent for silectron being 1.84), to increase the core loss by $\sqrt{2}$, the flux level must be increased by approximately $\sqrt{\sqrt{2}} = \sqrt[4]{2}$. Since the coil size will be reduced in the same proportion as the core size, it is reasonable to assume its losses may also be increased by $\sqrt{2}$ (or, in other words, the current can increase by $\sqrt[4]{2}$). Thus, the overall transformer rating has been increased by $\sqrt[4]{2} \cdot \sqrt[4]{2} = \sqrt{2}$. Using the scaling equation (2-40) to reduce the rating to the original, the ratio of the weight of the higher-loss small transformers to the lower loss small transformers is

$$\left[\frac{P_o/2}{\sqrt{2}\,P_o/2}\right]^{3/4} = \left[\frac{1}{\sqrt{2}}\right]^{3/4} = \frac{1}{2^{3/8}} \qquad \text{(2-III-4)}$$

Similarly, the ratio of the weight of the two lower-loss small transformers to the single large transformer is

$$\frac{2\left(\frac{P_o}{2}\right)^{3/4}}{P_o^{3/4}} = \frac{2}{2^{3/4}} = 2^{1/4} \qquad \text{(2-III-5)}$$

Therefore, the ratio of the weight of the two higher-loss small transformers to the single large transformer is:

$$2^{1/4}\left(\frac{1}{2^{3/8}}\right) = \frac{1}{2^{1/8}} = 0.92 \qquad \text{(2-III-6)}$$

Thus, under conditions where the temperature rise in the unit limits the maximum flux density that can be used, under conditions of equal internal temperature rise, two transformers, each of half the rating of a single larger transformer, will have a total weight less than that of the single

unit. (The losses, however, will also be higher, but because of the very high efficiencies possible with transformers at this frequency (3200 cps) this will not generally be a significant consideration.)

APPENDIX 2- IV

BALANCING PARALLELED TRANSISTORS

Object

The object of the experiments detailed in this Appendix was to experimentally verify certain paralleling methods and conclusions reported in a previous discussion. Four areas were investigated; namely, 1) direct paralleling, 2) simple balancing reactor paralleling, 3) referenced balancing reactor paralleling system, and 4) a saturating choke circuit in series with the referenced balancing reactor system.

The types of transistors used in the experiment were chosen to be representative of a general "inverter" power transistor type. The methods and results should be applicable to other transistors (both silicon and germanium) and silicon controlled rectifiers. The experiment was set up to simulate the generalized power switch on one side of a simple square wave inverter stage. This simulated switch was operated at 3200 cps with its "on" and "off" times being equal.

Procedure

The transistor type used for the experiment is the Bendix diffused alloy power (DAP) 2N1073A. The ratings of this transistor are as follows:

maximum ratings

V_{CE}	V_{CB}	I_C	P_C	$T_{STORAGE}$	T_J
Volts	Volts	Amps	Watts	°C	°C
-80	-80	-10	60	-65 to +110	=110

The transfer characteristics are shown on the manufacturers data sheet as follows:

	min	typ	max	unit
h fe;	20	-	60	-
g fe; (V_{CE} = -2^v, I_C = -5.0^a)	6.25	10	-	mhos
$V_{CE_{sat}}$; (I_C = -5^a, I_B = -.5^a)	-	-0.25	-0.5	volts
V_{EB}; (I_{EBO} = -50 ma, I_C = 0)	-	-.75	-	volts

The maximum I_B for safe operating area operation is -1.0 amps.

A total of eight transistors were purchased to provide a selection of transistors for the paralleling experiments. Each transistor had its switching times measured and the saturation voltages measured. The test circuit used to measure these characteristics and the tabulated data are shown in Figure 2-IV-1 and Tables 2-IV-1 and 2-IV-2.

With the switching times and saturation voltages of the transistors known, it is possible to choose two widely unlike transistors for the paralleling

experiment. The transistors used were Nos. 1 and 7. By using two widely different transistors a worst case condition insofar as switching speed was simulated in the experiment.

The drive circuitry for the paralleling experiment is shown in Figure 2-IV-2. This circuit provides the necessary 4 volt, 1 amp drive at each secondary winding to drive up to four transistors into saturation. At the bottom of the figure is a representation of the drive transisotr output voltage. The fast rise and fall times are obtained by using a special low leakage inductance output transformer.

The circuit diagrams used for the various paralleling schemes are shown in Figures 2-IV-3, 2-IV-4, 2-IV-5 and 2-IV-6. The method for measuring the collector currents is indicated on the schematic.

As shown the collector leads of the paralleled transistors are criss-crossed and passed through the probe of a Hewlett-Packard clip-on ammeter. Using this technique, the ammeter read the average DC difference between the currents in the two criss-crossed wires. The collector current in each transistor is the equal to:

$Q_1 = I\,1 \pm I\,c.o.a.$ c.o.a. = clip-on ammeter

$Q_2 = I\,1 \pm I\,c.o.a.$

To view the collector currents on an oscilloscope a special current viewing resistor was built. This resistor has extremely low resistance (3 milliohms) in order to contribute only a negligible balancing effect to the paralleled transistor. Another important feature about the current viewing resistor is its coaxial construction which cancels all inductance and permits viewing of fast rising currents with a minimum of distortion. A sketch of the resistor is shown in Figure 2-IV-1.

The sketch illustrates how the cancellation of inductance in the current viewing end of the coaxial resistor is accomplished. Current enters the center brass termination and divides equally into each tubular resistor as shown by the dotted arrows and sets up a magnetic field according to Amperes Law. At the current viewing end of the coaxial resistor the current is returned through the tubular resistor by the brass arbor to the opposite load circuit termination. The current in the arbor sets up a magnetic field opposite in sense to the field set up by the same current flow in the tubular resistor thereby equating the net external magnetic field in this portion of the current viewing resistor to zero. Only the uncancelled field between the arbor and resistor can contribute to the inductance. A zero magnetic field in the presence of a current flow indicates zero inductance.

A commercially available probe of this general design is made by IRC.

Results

The directly paralleled transistors are shown in Figure 2-IV-3; two transistors Nos. 1 and 7, with different saturation voltages and switching times were used. The transistors shared the current with a ratio of 1.3 to one as shown in the lab data tabulated in Table 2-IV-3.

When the transistors were paralleled by using a balancing reactor as in Figure 2-IV-4 the ratio of current division was reduced to 1.12 to one. The improvement in current sharing is quite significant and is the result of utilization of a very small balancing reactor. The remaining unbalance is due to the magnetizing current required by the balancing reactor. Since this reactor is operated with d.c. current in its windings, it must have an air gap to avoid saturation. This gap, combined with the low number of turns used on each winding, results in a fairly high magnetizing current, which appears as an unbalance in the collector currents.

The balancing reactor used is illustrated in Figure 2-IV-8. The reactor was designed to support V_o across the whole winding. In this case, V_o was 0.25 volts.

$$V_o = (V_{CE} \text{ sat max} - V_{CE} \text{ sat min})$$

$$V_o = 0.5 - 0.25 = 0.25 \text{ volts}$$

Four EE- 24-25 laminations were cemented together to provide the core for the balancing reactor. The net cross-sectional area of the core is:

$4 \times .006'' \times 0.25'' = .006$ square inches.

The necessary turns to support V_o are:

$$N = \frac{V_o \times 10^8}{2\,BfA} \qquad \frac{.25 \times 10^8}{2\,(14 \times 10^3)\,(3.2 \times 10^3)\,(.006 \times 6.45)} = 8 \text{ turns}$$

The eight turns were then center-tapped. This construction results in a very small reactor which will provide a marked increase in transistor utilization.

The next paralleling scheme used a reference transistor balancing reactor system shown in Figure 2-IV-5. The balancing reactors are wound with a three to one turns ratio which forces the paralleled transistors to conduct three times as much current as the reference transistor. This condition assures reliable operation of the reference transistor and sharing of the load current by the paralleled transistors. This method also lends itself to redundant configurations because the loss of any main power transistors will only result in a redistribution of current among the remaining units.

The results of this paralleling scheme were quite good; the transistors shared the load current with a ratio 1.09 to one. The improvement in balancing with the reference transistor scheme is attributed to the decrease in magnetizing current brought about by the increased number of primary turns over the simple balancing reactor scheme (turns were increased from 4 to 8).

At this point in the experiment a saturable reactor was inserted in series with the load line. The reason for using this reactor was to force a delay in the flow of current in the transistors during the turn on portion of the cycle. This technique reduces the turn on losses because the turn on current is low and when the core turns on the collector-emitter voltage will be low which forces the operating point of the transistor into a low dissipation turn on path.

Means for resetting the core by an auxiliary circuit was provided and the circuit was tested. The circuit diagram is shown in Figure 2-IV-6. The CRO photos labeled Figure 2-IV-9, 2-IV-10, 2-IV-11, and 2-IV-12 show the collector voltage and current waveforms before and after the series saturating core is inserted in the circuit. Figures 2-IV-9a and 2-IV-9b show the collector voltages of the two paralleled transistors and Figure 2-IV-10a shows the collector current in one of the transistors.

The load line for this arrangement is shown in Figure 2-IV-12a. Notice the rapid rise of current to its maximum value at the initiation of saturation and the nearly resistive load line.

When the saturating core was inserted into the load circuit as shown in Figure 2-IV-6 the switching characteristics of the paralleled transistors are markedly changed. The collector voltage is unchanged (except for the induced reset voltage pulse) as seen in photo Figure 2-IV-11a and 2-IV-11b. However, the collector current is reduced considerably upon initiation of saturation as seen in photo Figure 2-IV-10b. This is because the saturating core is absorbing the supply voltage until it becomes magnetized. Once the core is magnetized the load current increases to its maximum level. The load line is shown in photo Figure 2-IV-12b and illustrates how the turn on portion of the line closely follows the V_{CE} axis before rated current is conducted.

The saturating series core is also a very convenient method for assuring current sharing in transistors with badly mismatched rise times. Photo Figures 2-IV-13a and 2-IV-13b, shows the collector waveforms of two paralleled transistors. Q_1 is deliberately slowed down with a 5 microfarad capacitor between the base and emitter. Photo Figures 2-IV-15a, 2-IV-16a, 2-IV-17a and 2-IV-18a show the collector currents and load lines for the normally switching transistors. Photo Figures

2-IV-15a and 2-IV-15b show the collector current and load line for the slow transistor while 2-IV-17a and 2-IV-18b show the collector current and load line for its partner.

Figures 2-IV-15c, 2-IV-16c, 2-IV-17c and 2-IV-18c show collector currents and load lines for the transistors with the series saturating choke; the improvement in current balance and switching loss is very obvious here.

Discussion of Results

The methods for paralleling power transistors verifies the theoretical conclusions formulated in the previous text. The simple balancing reactor method for paralleling power transistors worked as predicted but it does exhibit an undesirable characteristic. When one of the paralleled transistors is opened by a failure, the partner to this transistor is forced to carry the net current previously carried by two transistors. This condition is undesirable and is alleviated by the use of the referenced balancing reactor system.

The referenced balancing reactor system for paralleling power transistors worked quite well and has the outstanding feature of providing an equal distribution of current among the paralleled transistors. This equal distribution of current is forced even though a failure occurs and opens one of the paralleled units.

The feasibility of using a saturating core to substantially reduce the turn-on switching losses was also demonstrated.

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2) Reference Data for Radio Engineers, Fourth Edition, International Telephone and Telegraph Corporation, p. 133.

3) Neville Mapham, The Rating of SCR's When Switching Into High Currents, IEEE Conference Paper CP 63-498.

4) Design Manual Featuring Tape Wound Cores, Magnetics, Inc., TWX-300, pp. 45-55.

5) Arnold Silectron Cores, Bulletin SC-107A, page 4.

TABLE 2-1 TABULATION OF WEIGHTS, LOSSES, AND PARTS COUNT FOR TRANSISTORIZED 10 KW 3200V INVERTER

	Number Per Unit	Power Transistors			Signal Transistors			Diodes			Transformers, Chokes			Resistors			Capacitors			Miscellaneous		
		Wt.	Loss	Quan.	Wt.	Loss	Quan.	Wt.	Loss	Quan.	Wt.	Loss	Quan.	Wt.	Loss	Quan.	Wt.	Loss	Quan.	Wt.	Loss	Quan.
Input Filter	1										0.5	10	1				0.5	2.0	1			
Logic D C. Reg.	1	.05	6	1			3			5	.02		1			15			5			
Start Ckt.	1						3			3	.04		2			4			3			
Master Osc. Pulse Shaper	1						4			4	.04		2			10			4			
6 Ø Flip-Flop	2						24			36						108			60			
Variable Delay	1						14			26	.5		19			53			29			
Drivers	12	0.5	6	24						24	.7	24	24	.5	72	24			24	Shockley Diodes 0.5	6	24
Output Stage	12	4.4	2260	96				2.4	505	216	29.4	1330	192							.7	48	96
Output Filter	3										3.3	80	6				1.2	10.5	6	Fuses		
V & I Sense	1						4			14	.5	1	6			15			1			
TOTAL		4.95	2272	121			52	2.4	505	328	35.0	1455	253	.5	72	229	1.7	12.5	133	1.2	54	120

	Weight	Loss	Parts Count
Total of items listed above	45.75 lbs	4370 watts	1236 components
Allowance for weights & losses not itemized above.	4.25 lbs	60 watts	———
TOTAL	50.0 lbs	4430 watts	1236 components

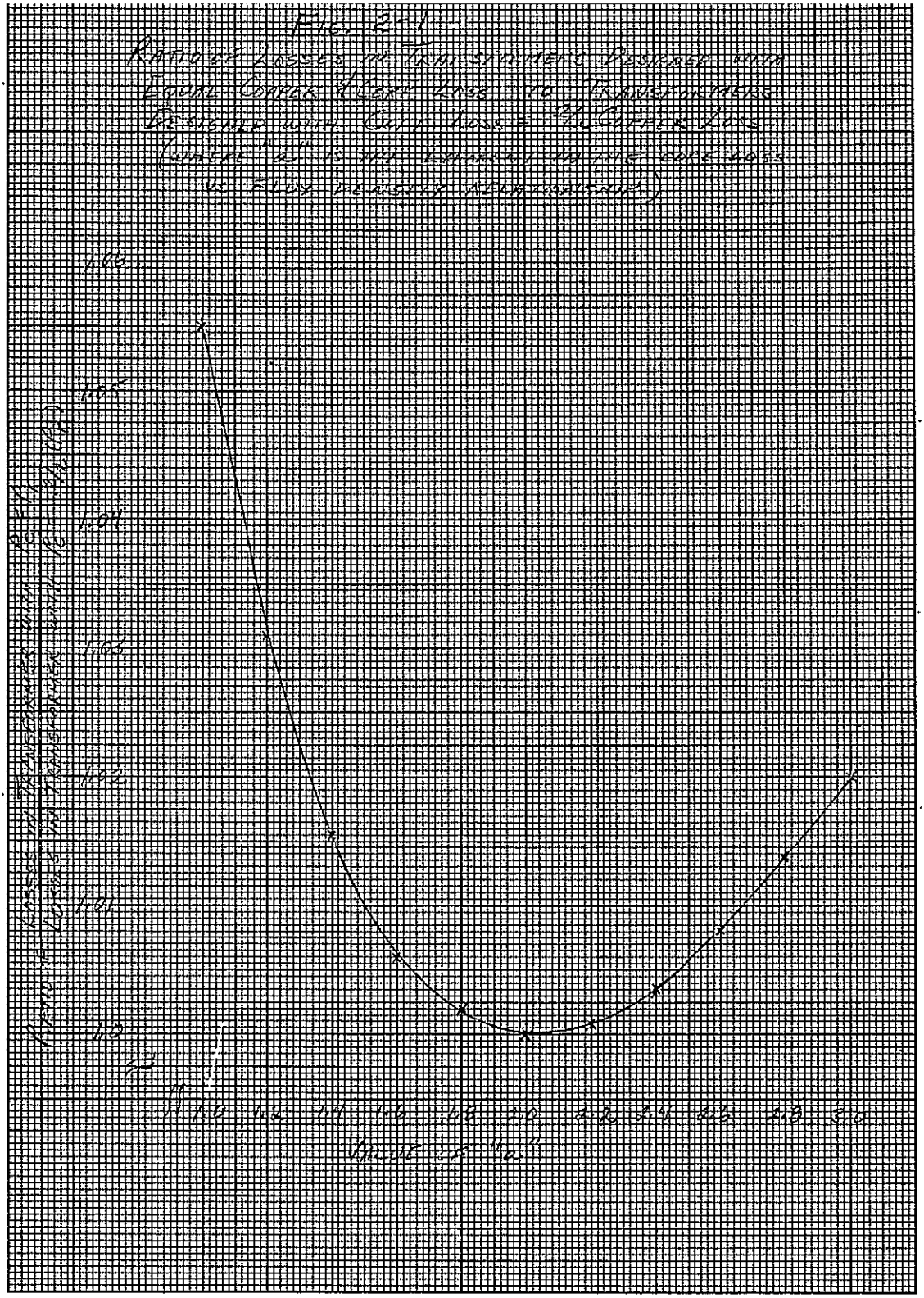
$$\eta = \frac{10,000}{10,000 + 4430} = 70\%$$

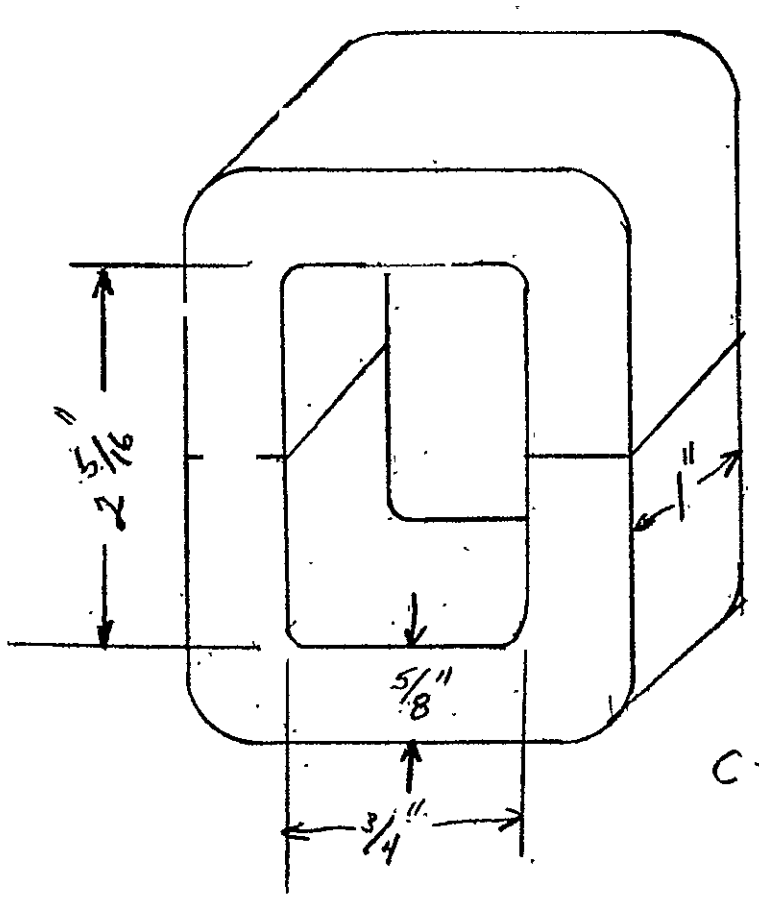
TABLE 2-2 TABULATION OF WEIGHTS, LOSSES, AND PARTS COUNT FOR SCR 10 KW 1200V INVERTER

Functional Block	Number Per Unit	SCR's Wt.	SCR's Loss	SCR's Quan.	Signal Transistors Wt.	Signal Transistors Loss	Signal Transistors Quan.	Diodes Wt.	Diodes Loss	Diodes Quan.	XFMRS, Chokes Wt.	XFMRS, Chokes Loss	XFMRS, Chokes Quan.	Resistors Wt.	Resistors Loss	Resistors Quan.	Capacitors Wt.	Capacitors Loss	Capacitors Quan.	Miscellaneous Wt.	Miscellaneous Loss	Miscellaneous Quan.
Input Filter	1										1.0	20.0	1				0.5	2.0	1			
Logic D. C. Reg.	1						3			5	.02		1			15			5	Pwr. Xstr .05	2.0	1
Start Ckt.	1						3			3	.04		2			4			3			
Master Osc. Pulse Shaper	1						4			4	.04		2			10			4			
3 Ø Flip-flop	2						12			18						54			30			
Variable Delay	1						8			14	.3		10			29			15			
Drivers	6						24			48	.5		18		72	64			36	Shockley Diodes 0.3	3	12
Output Stage	6	9.0	3600	36				2.4	672	12	21.0	858	12				12.0	120	6	0.3	3	12
Output Filter	3										7.5	240	6				3.3	27	6	Power Xstr.		3
V & I Sense	1						4			14	.5	1	6			15			1			
TOTAL		9.0	3600	36			58	2.4	672	118	30.9	1099	58	.5	72	191	15.8	149	107	.65	8	15

	Weight	Loss	Parts Count
Totals of items listed above	59.25 lbs.	5600 watts	583 components
Allowance for weights & losses not itemized above.	3. lbs	40 watts	—
TOTAL	62 1/4 lbs	5640 watts	583 components

$$N = \frac{10000}{10000 + 5640} = 64\%$$





Gross Cross Section
Area = 0.625 sq. in.

Window Area = 1.73 sq. in.

Wt = 1.22 lbs.

← AL-24 (Arnold Eng. Co)

Fig. 2-2

C-Core Dimensions for
Example Transformer

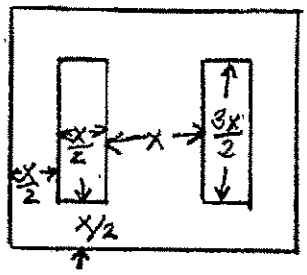


FIG. 2-3A
CONVENTIONAL SINGLE PHASE
EI "SCRAPLESS LAMINATION

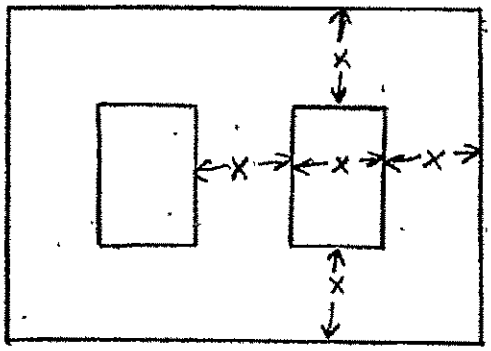


FIG 2-3B
THREE PHASE LAMINATION
WHICH USES SAME COILS
AS FIG 2-7A

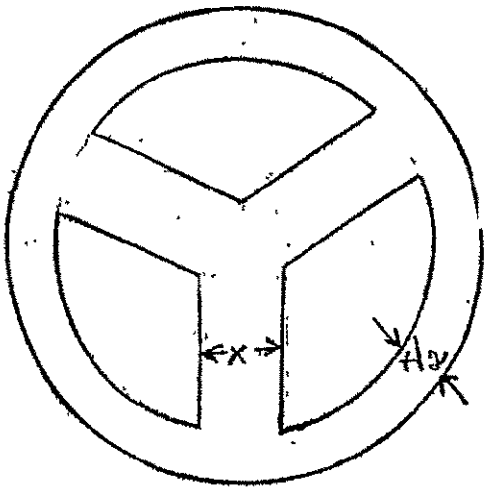


FIG 2-3C
CIRCULAR THREE PHASE
LAMINATION

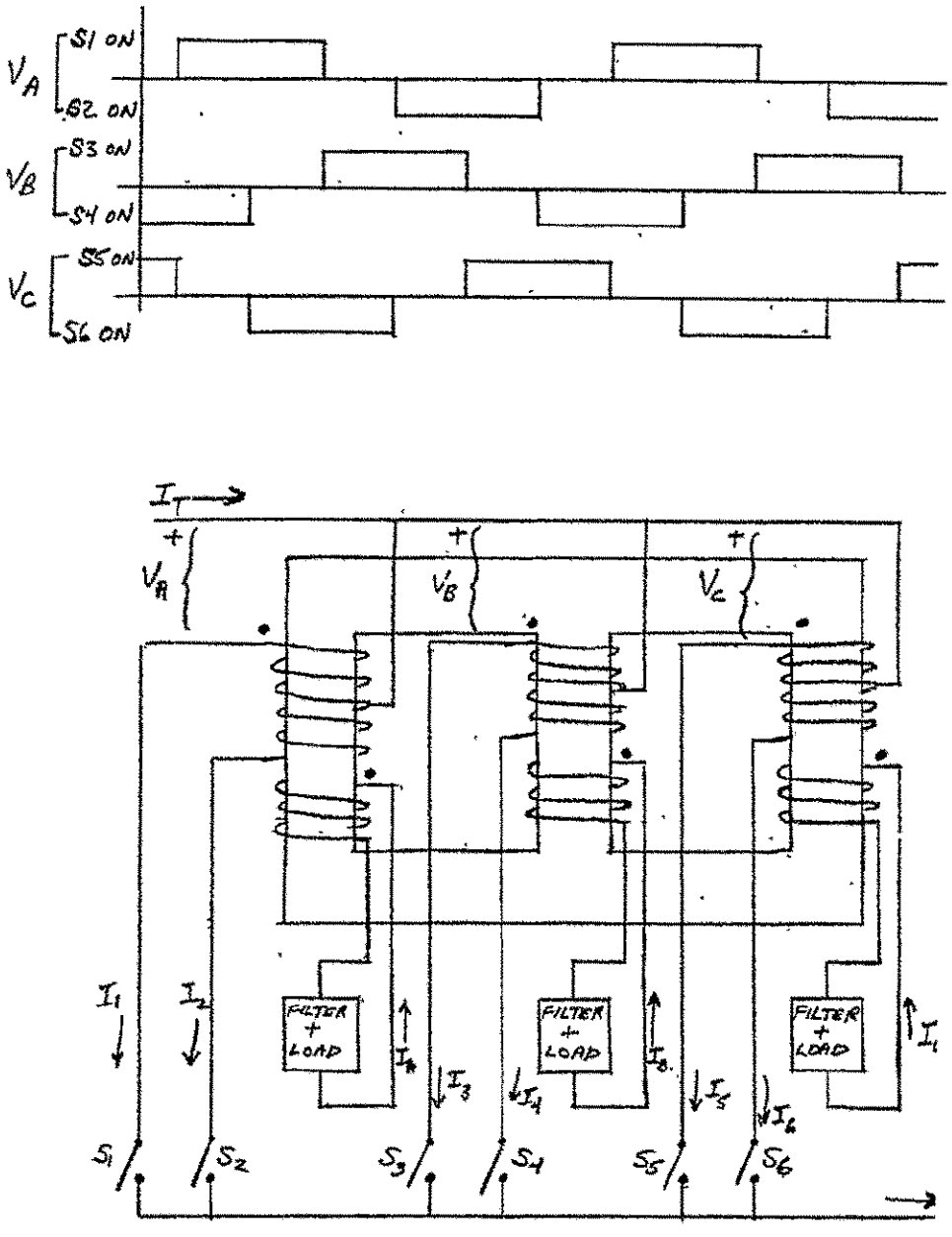
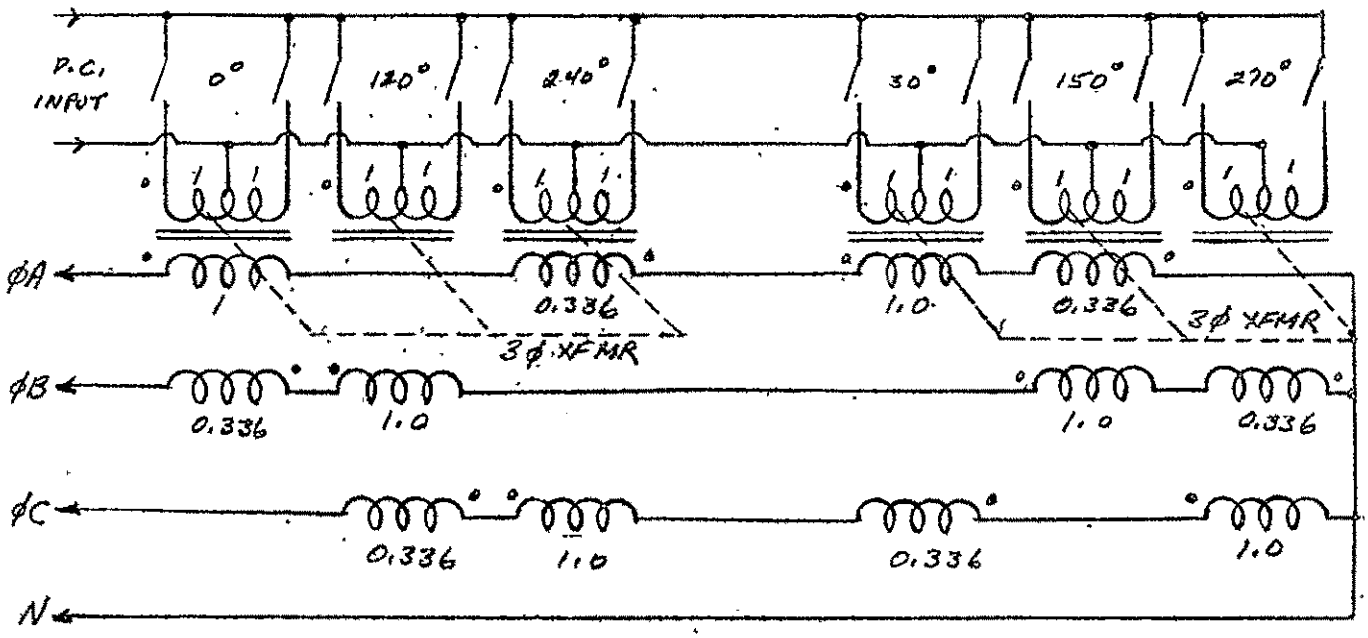


FIG. 2-4

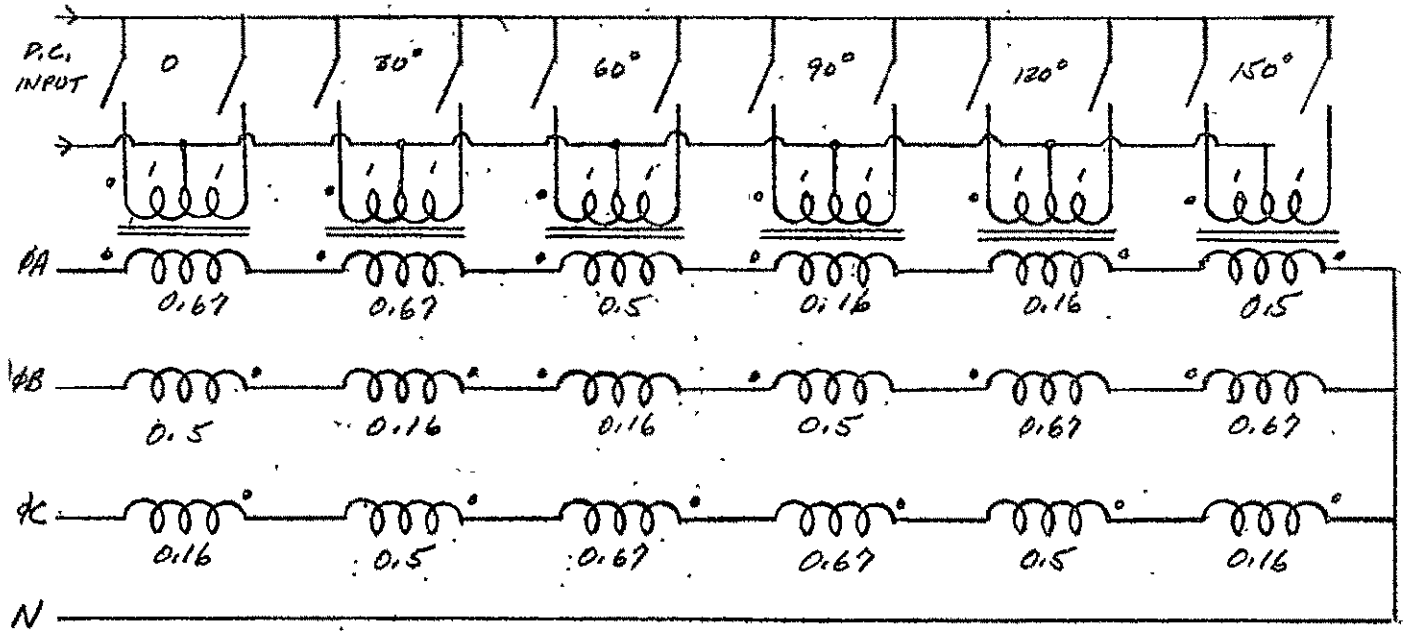
SWITCHING PATTERN FOR THREE PHASE TRANSFORMER WITH 120° QUASI-SQUARE WAVE EXCITATION.



A — MULTI-STEPPED WAVEFORM OUTPUT CIRCUIT UTILIZING THREE PHASE TRANSFORMERS

FIG. 2-5

B — MULTI-STEPPED WAVEFORM OUTPUT CIRCUIT UTILIZING SINGLE PHASE TRANSFORMERS



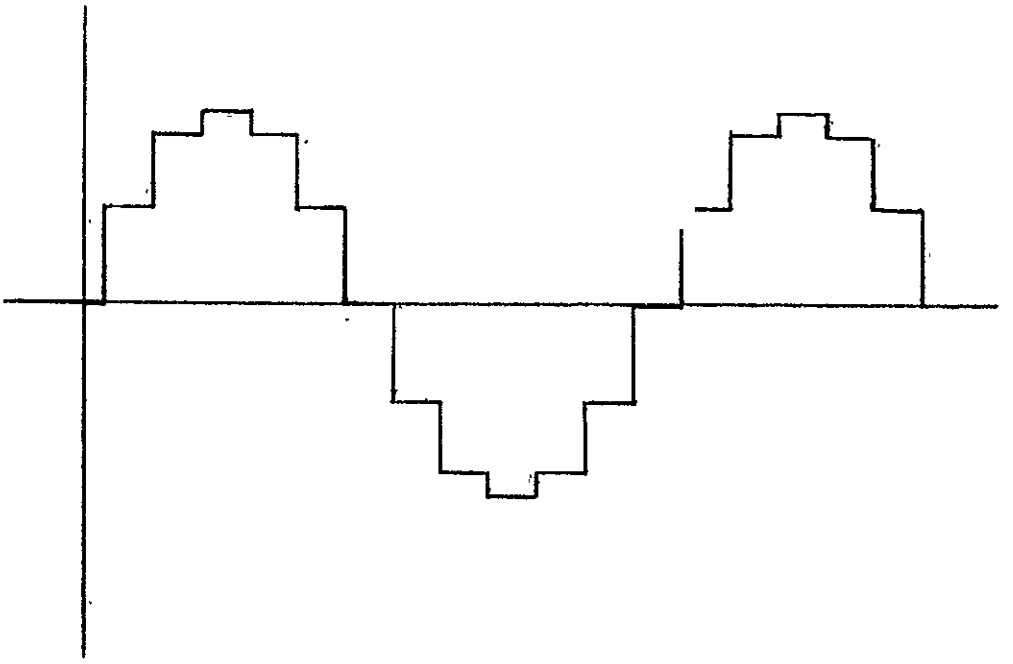


FIG. 2-6
MULTI-STEPPED OUTPUT VOLTAGE WAVEFORM
(COMPOSED OF SIX SQUARE WAVES)

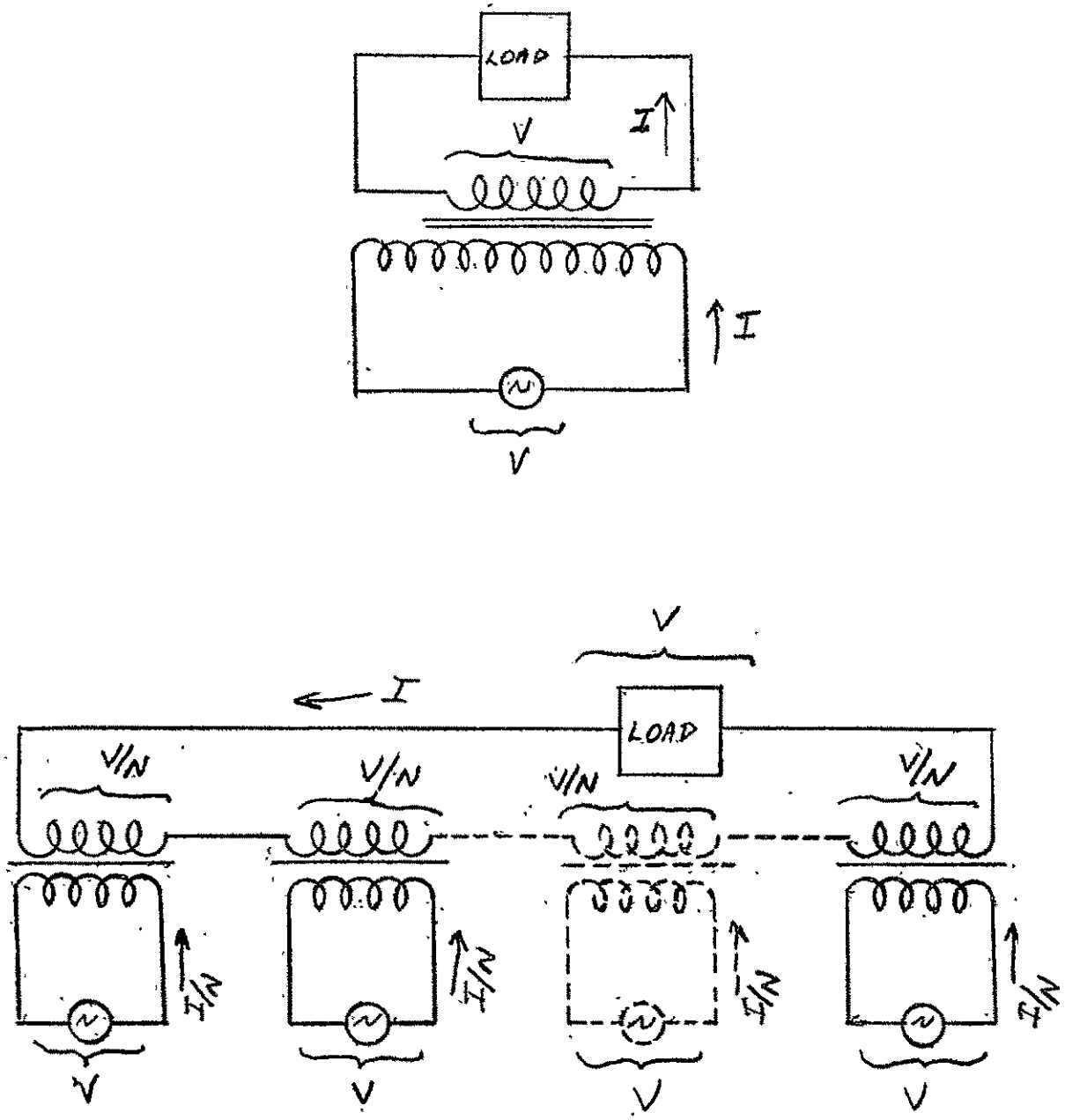


FIG. 2-7 LOAD SHARING BY SPLIT TRANSFORMER TECHNIQUE

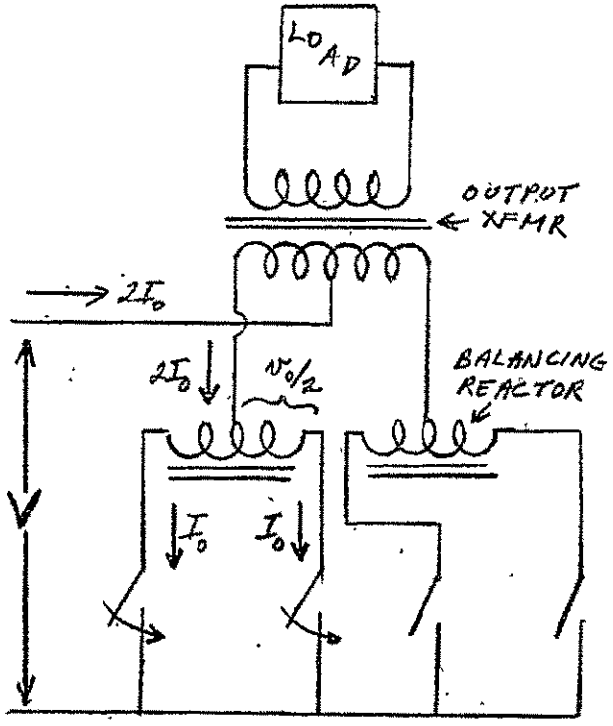


FIG 2-8A LOAD SHARING WITH BALANCING REACTORS

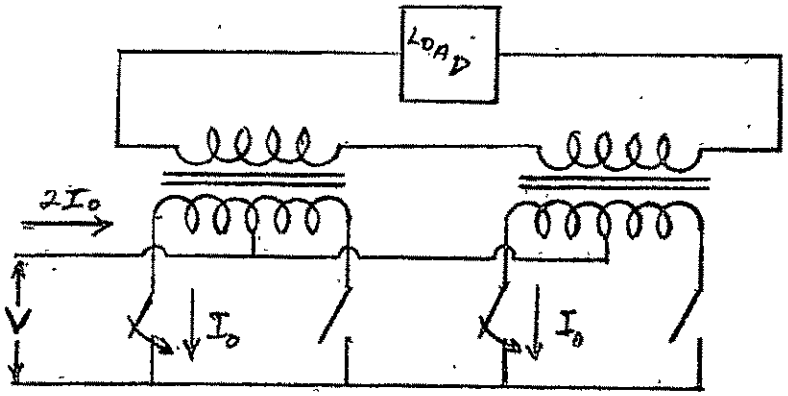


FIG 2-8B LOAD SHARING WITH SPLIT OUTPUT XFMR

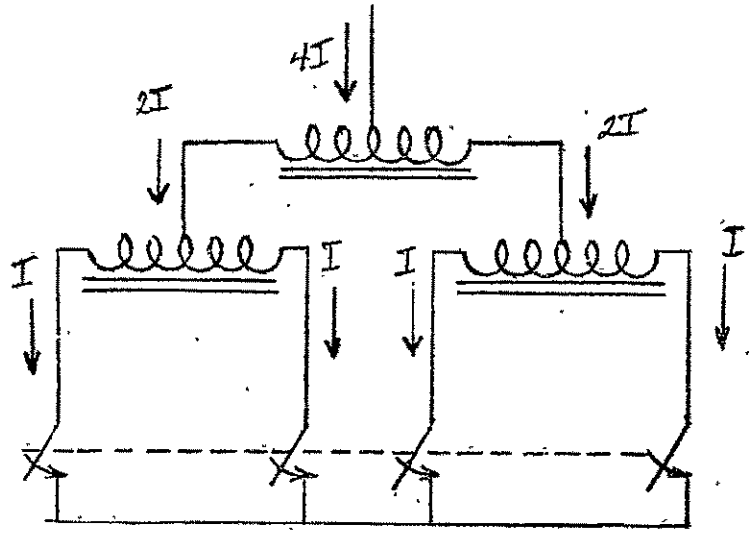


FIG 2-8C LOAD SHARING WITH CASCADED BALANCING REACTORS

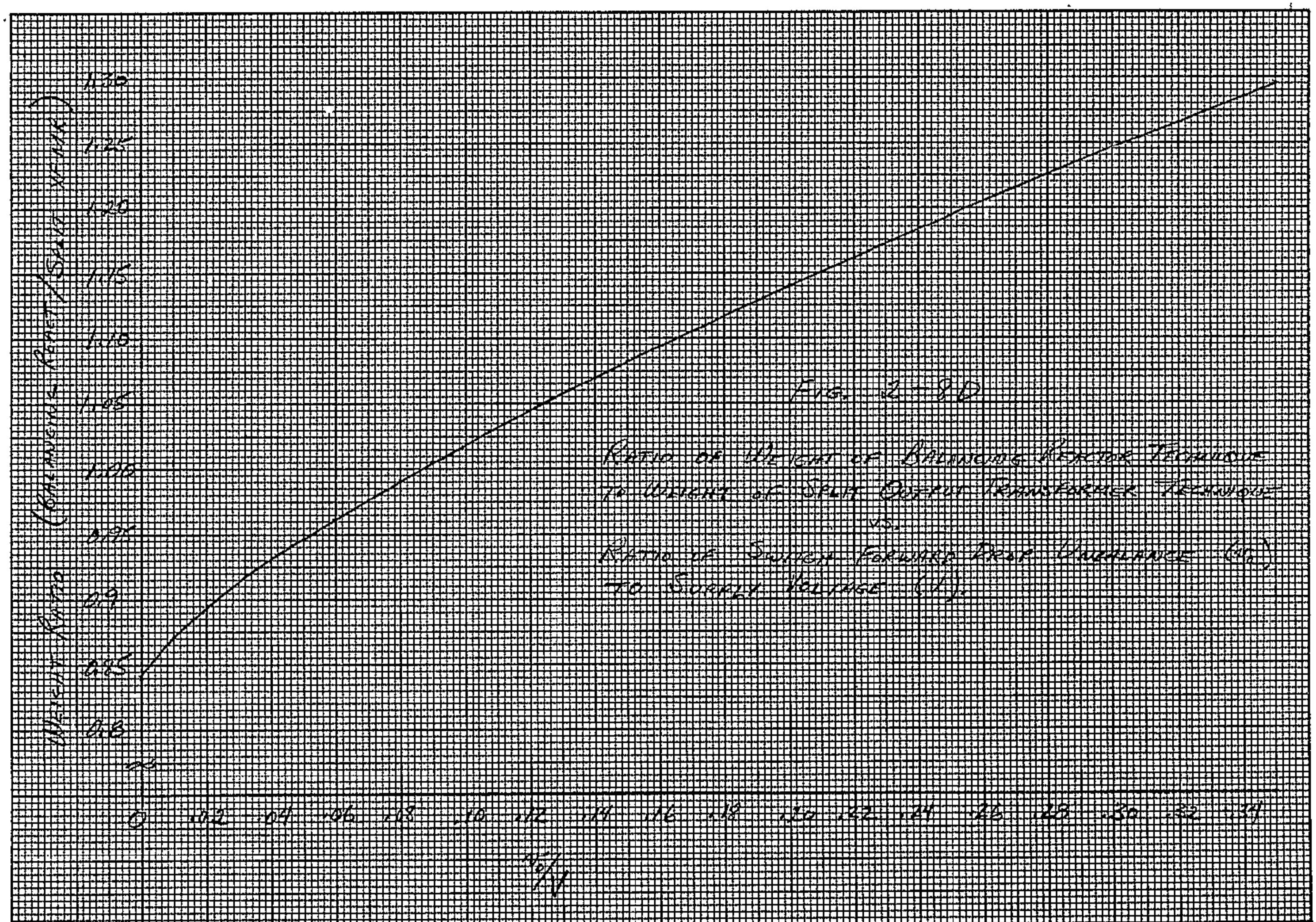


FIG. 2-8D

RATIO OF WEIGHT OF BALANCING REACTOR TECHNIQUE TO WEIGHT OF SPLIT OUTPUT TRANSFORMER TECHNIQUE vs. RATIO OF SWITCH FORWARD DROP UNBALANCE (Vu) TO SUPPLY VOLTAGE (V).

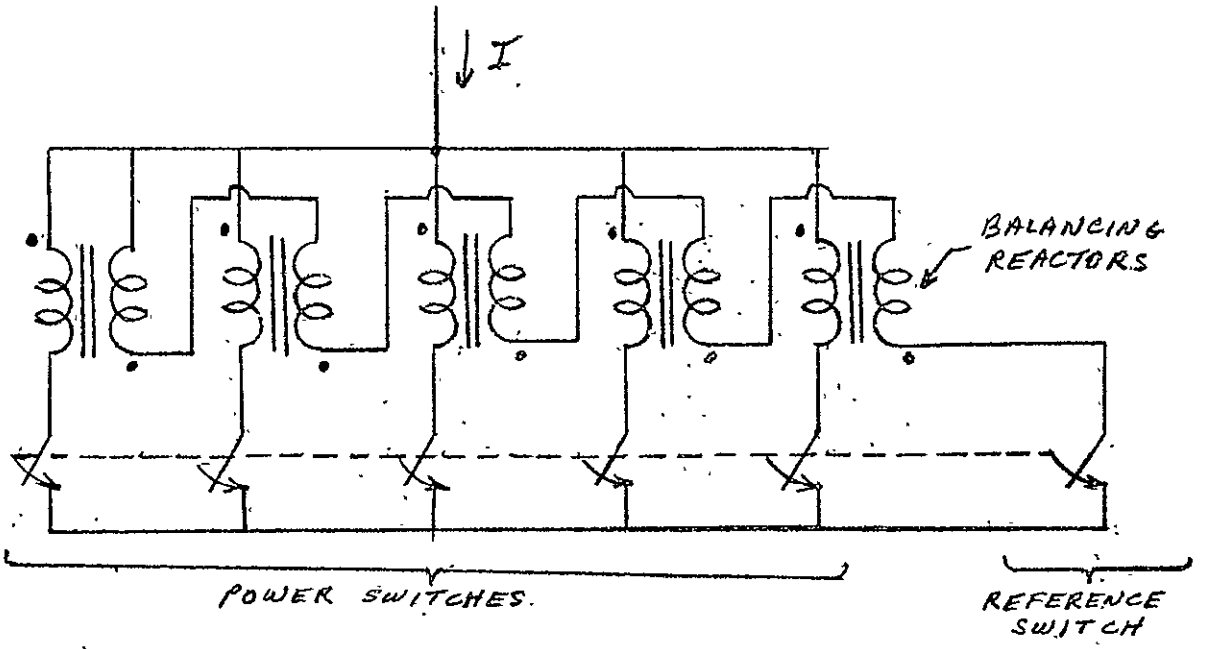


FIG. 2-9 PARALLELING WITH REFERENCE SWITCH AND BALANCING REACTORS

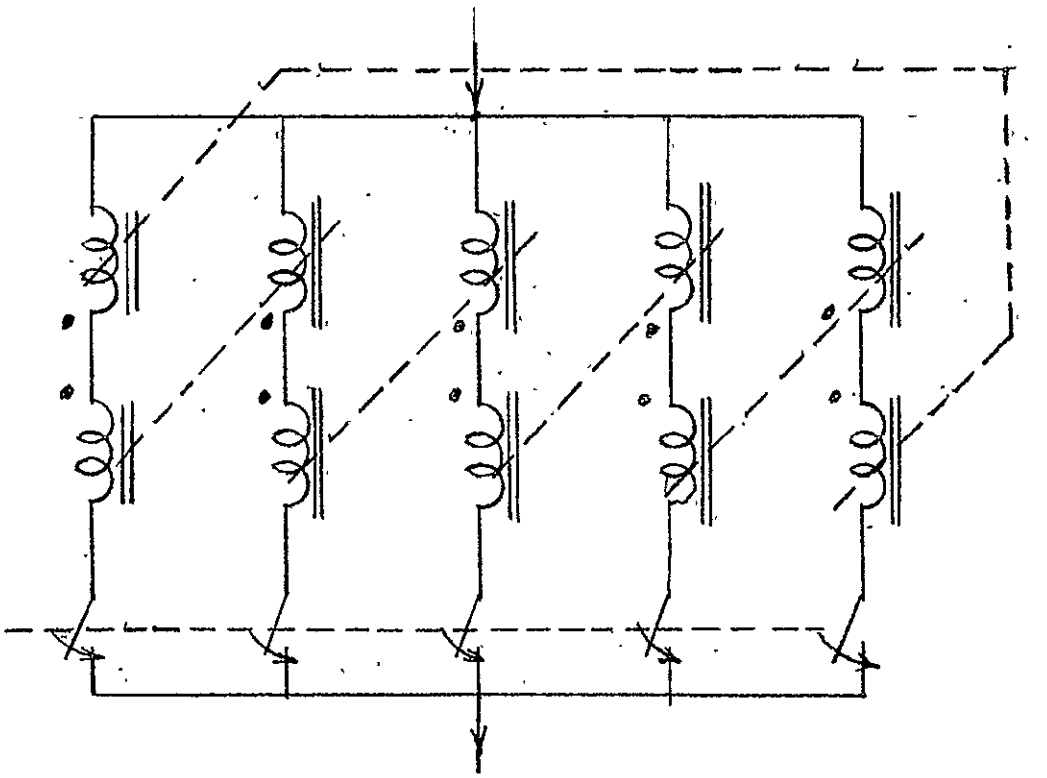


FIG 2-10 PARALLELING WITH CLOSED CHAIN OF BALANCING REACTORS

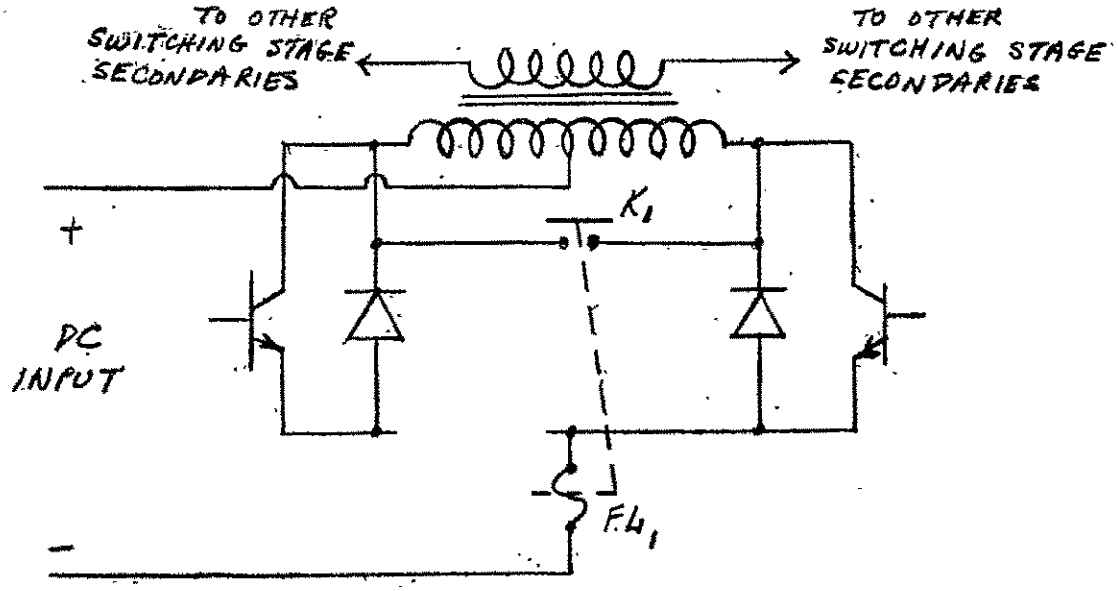


FIG. 2-11 STAGE ELIMINATION TECHNIQUE

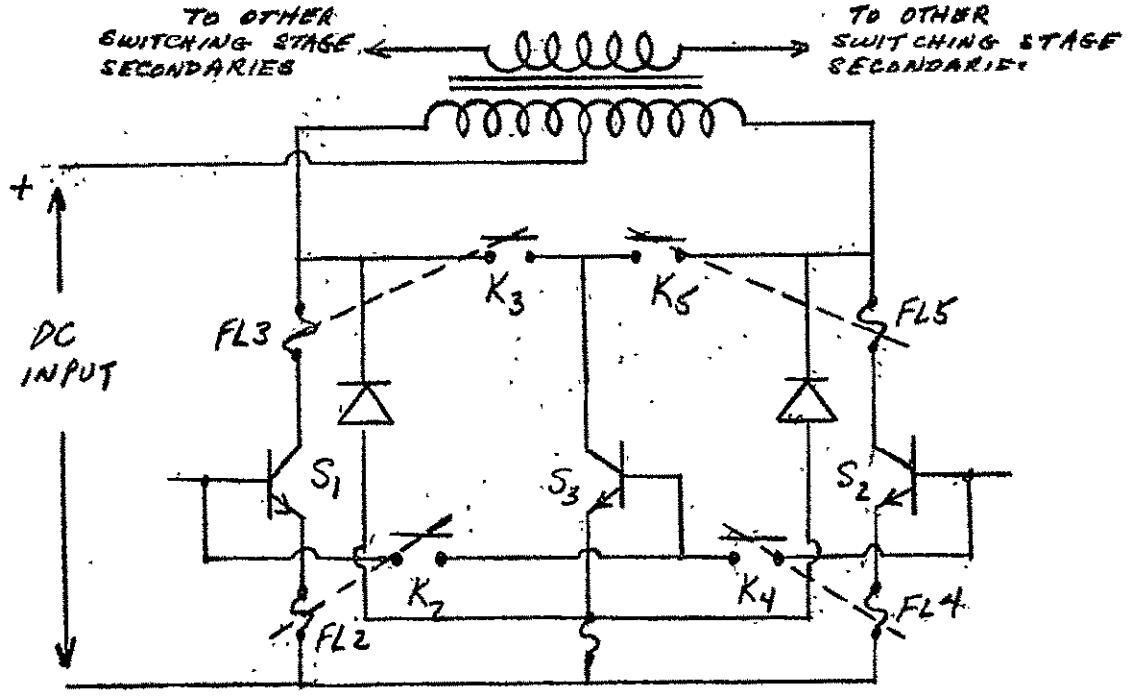


FIG 2-12 PART REPLACEMENT TECHNIQUE

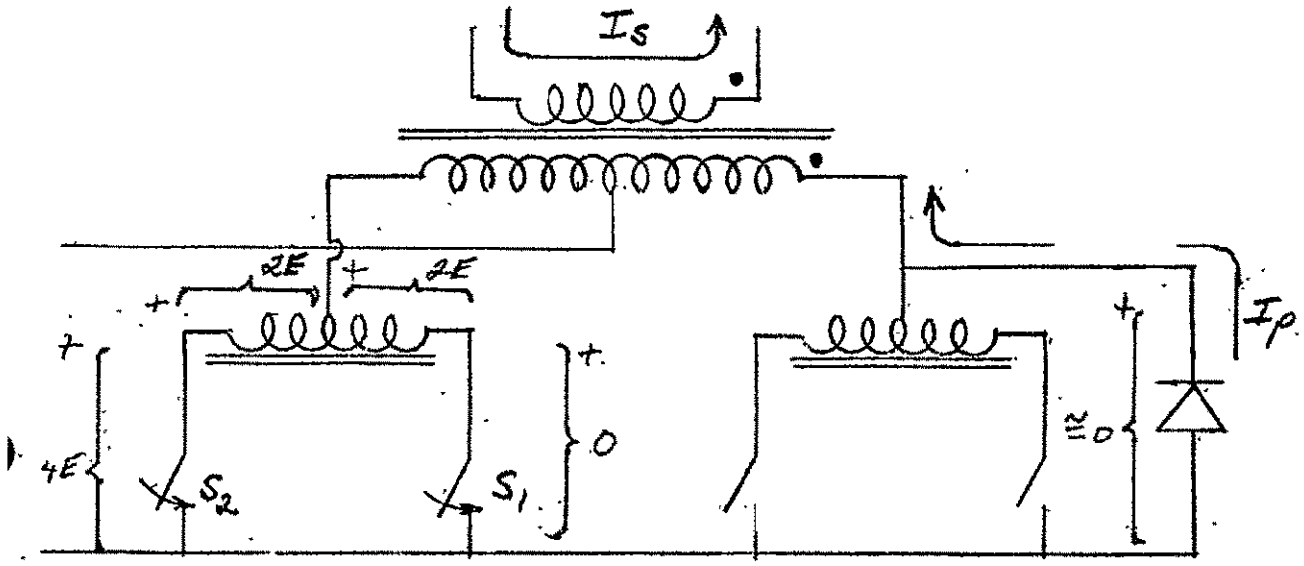


FIG 2-13 BALANCING REACTOR OPERATION WITH INDUCTIVE LOAD AND UNEQUAL SWITCHING SPEEDS, SHOWING GENERATION OF HIGH VOLTAGE SWITCHING TRANSIENTS.

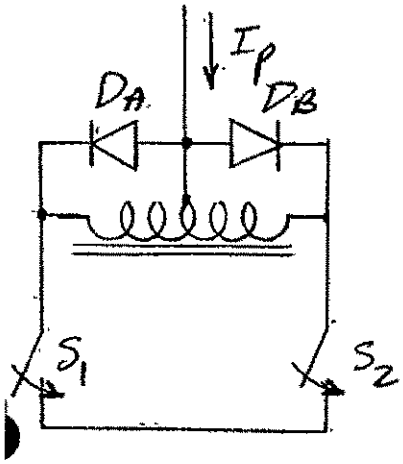


FIG. 2-14 DIODE SUPPRESSION OF BALANCING REACTOR SWITCHING TRANSIENTS

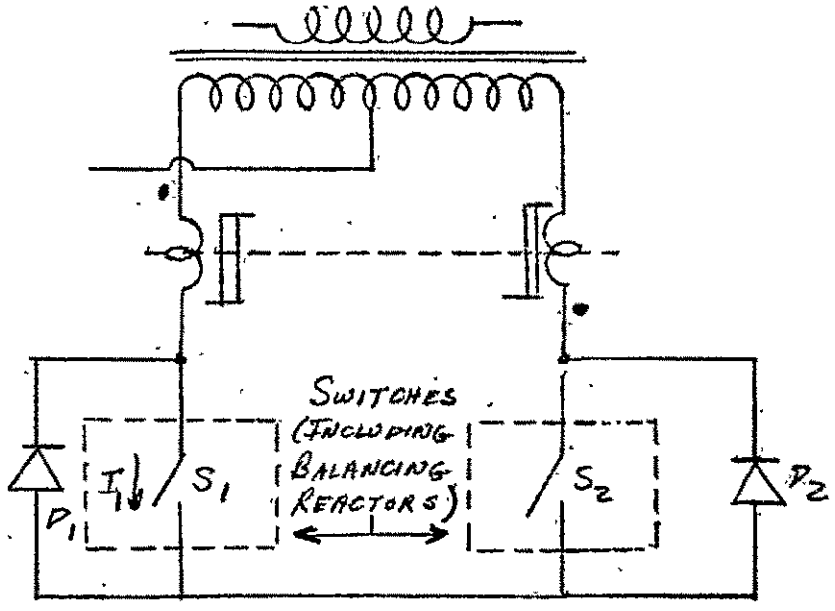


FIG 2-15 USE OF SATURABLE REACTORS TO REDUCE TURN-ON LOSSES

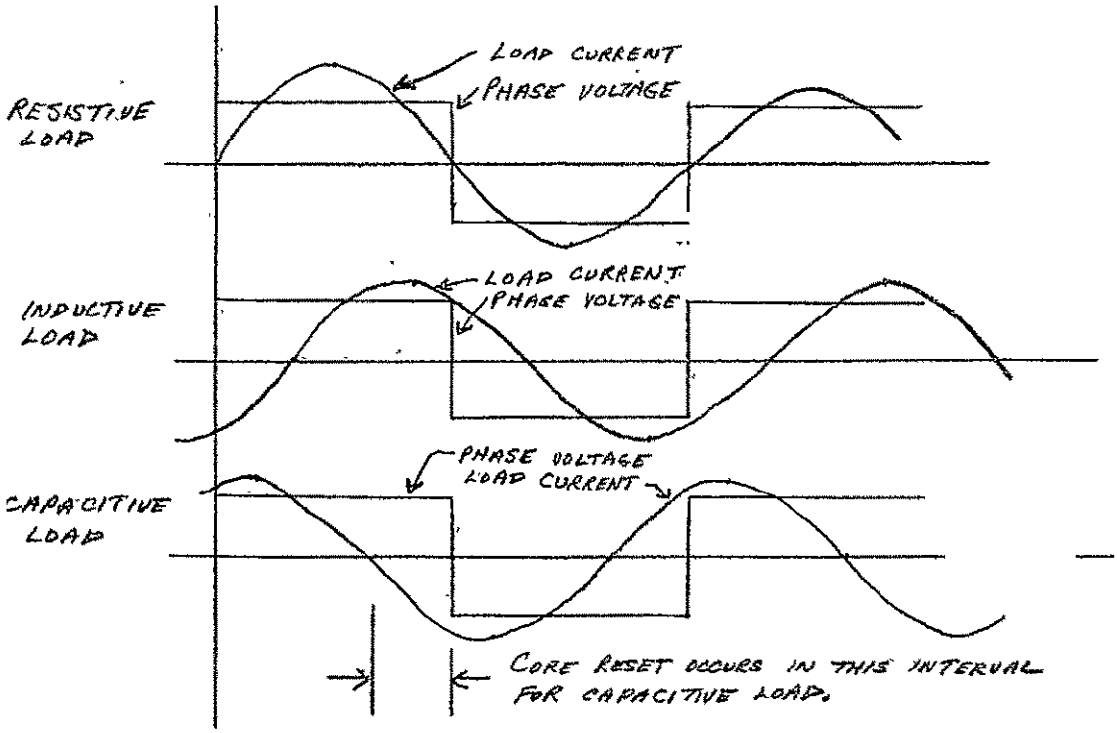


FIG 2-16A RELATIONSHIP OF LOAD CURRENT AND PHASE VOLTAGE FOR VARIOUS POWER FACTOR LOADS

I_R = NORMAL REACTIVE CURRENT PATH

I_r = REACTIVE CURRENT PATH THROUGH BASE-COLLECTOR DIODE OF TRANSISTOR

I_r' REVERSE TRANSISTOR CURRENT DUE TO I_r

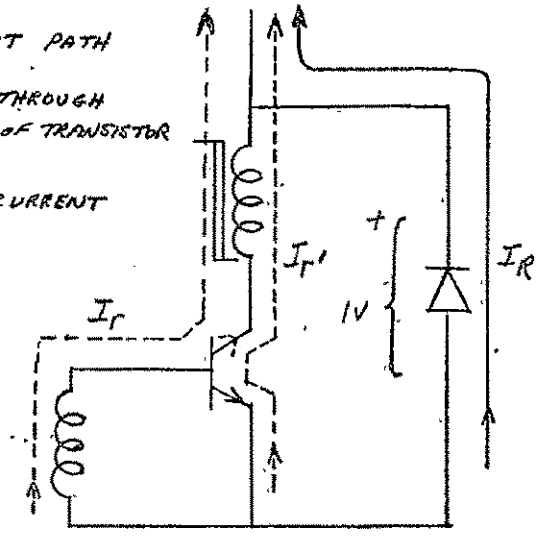


FIG 2-16B
REACTIVE CURRENT PATHS THROUGH TRANSISTOR JUNCTIONS

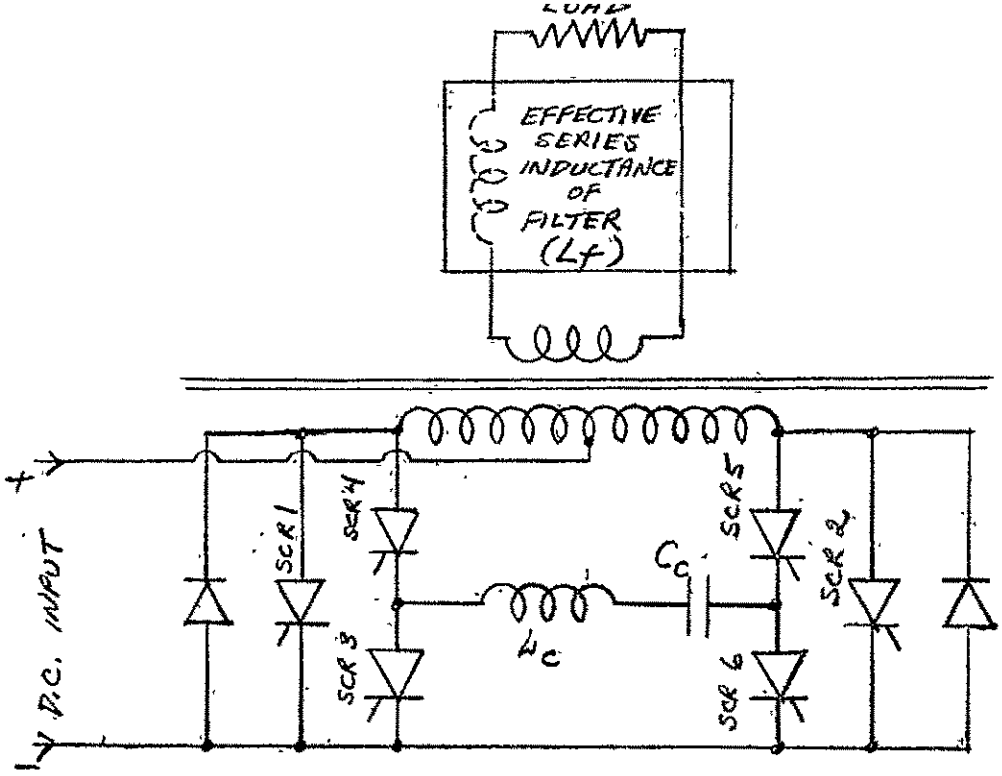


FIG 2-17.

MC MURRAY CIRCUIT, SHOWING SERIES INDUCTANCES

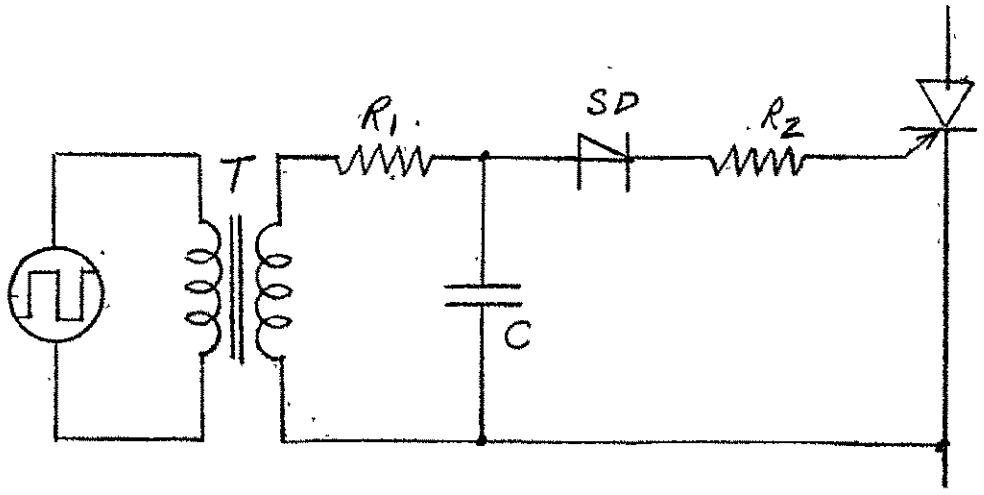


FIG 2-18A

SIMPLIFIED SCR DRIVE CIRCUIT USING SHOCKLEY DIODE

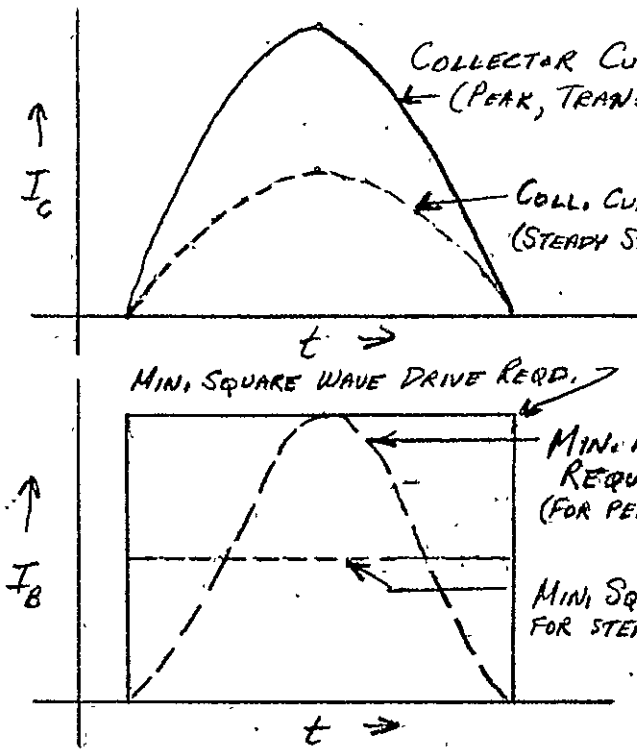


FIG. 2-18B (CONSTANT.)
SQUARE WAVE DRIVE
WAVEFORMS

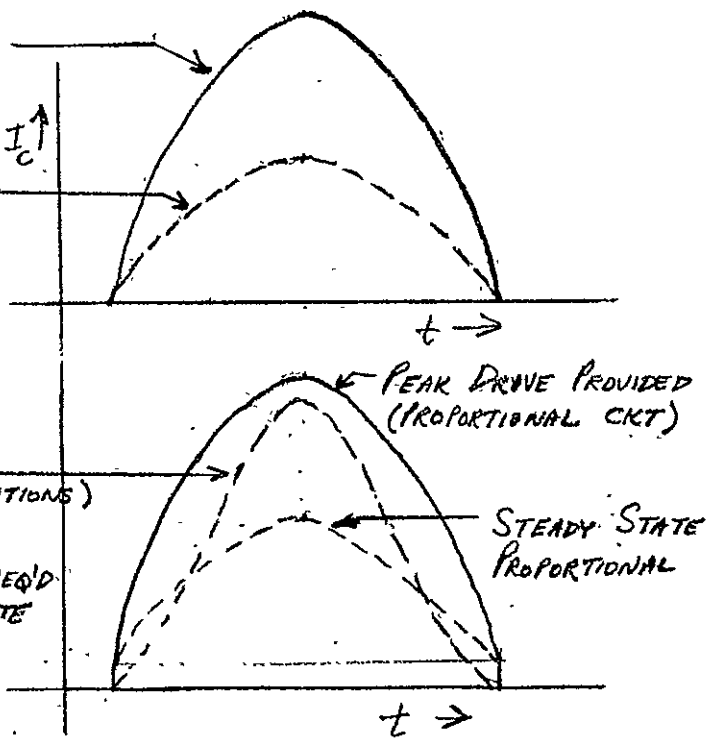


FIG. 2-18C PROPORTIONAL
DRIVE WAVEFORMS

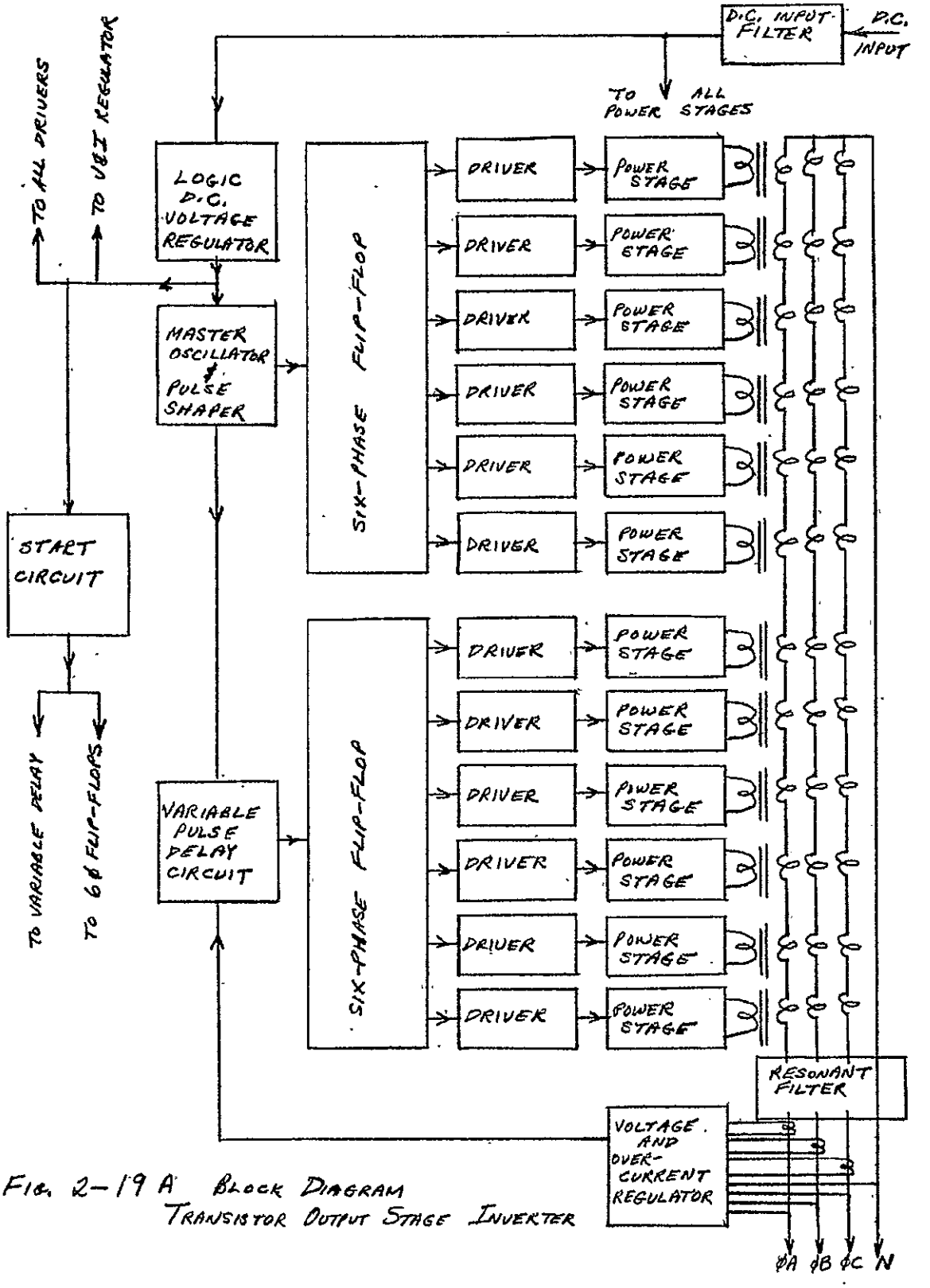


FIG. 2-19 A BLOCK DIAGRAM
TRANSISTOR OUTPUT STAGE INVERTER

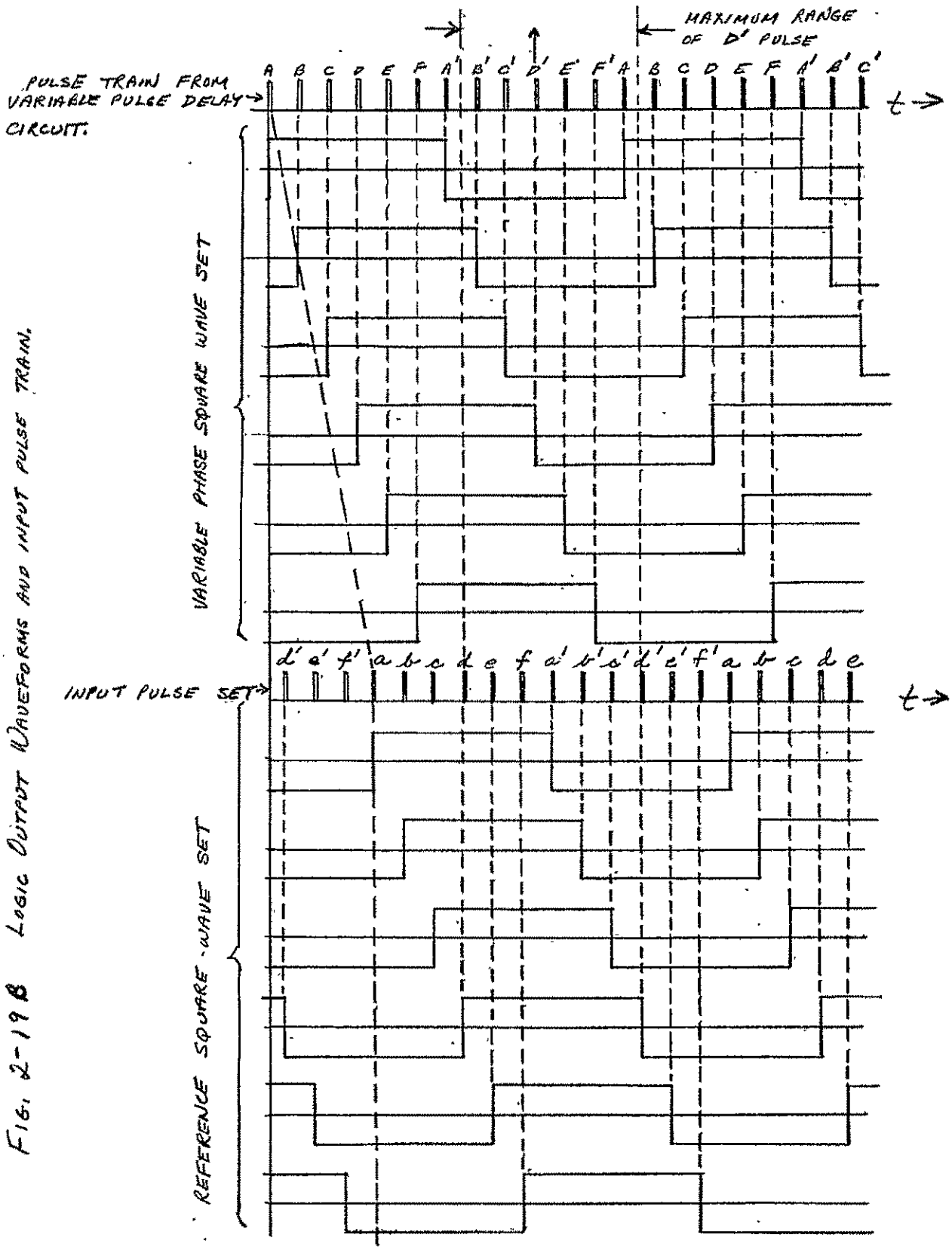


FIG. 2-19B LOGIC OUTPUT WAVEFORMS AND INPUT PULSE TRAIN.

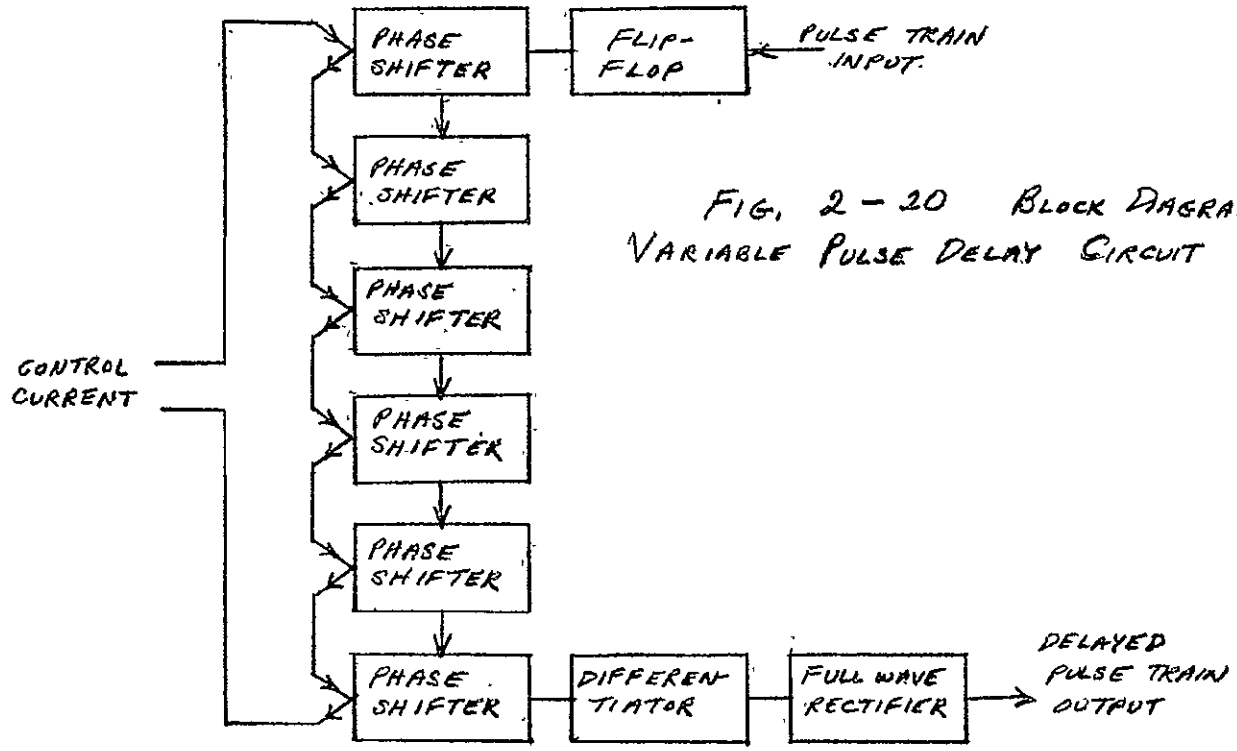


FIG. 2-20 BLOCK DIAGRAM VARIABLE PULSE DELAY CIRCUIT

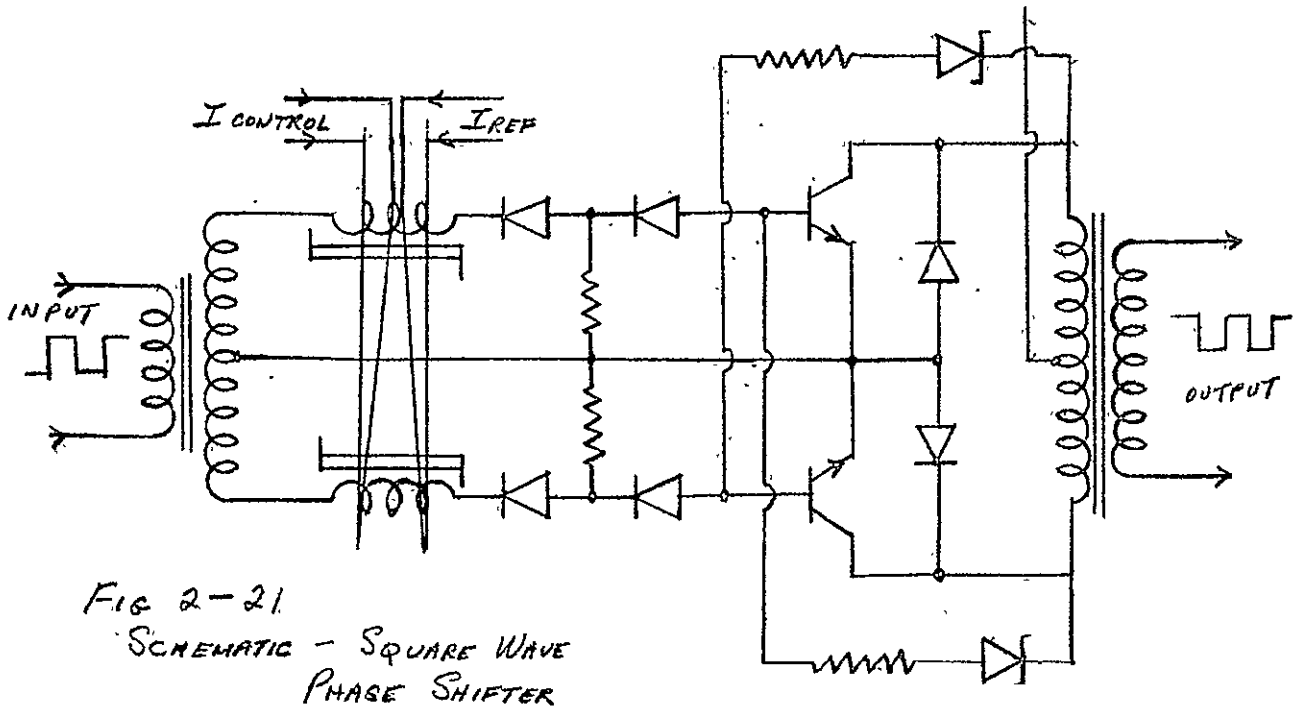


FIG 2-21 SCHEMATIC - SQUARE WAVE PHASE SHIFTER

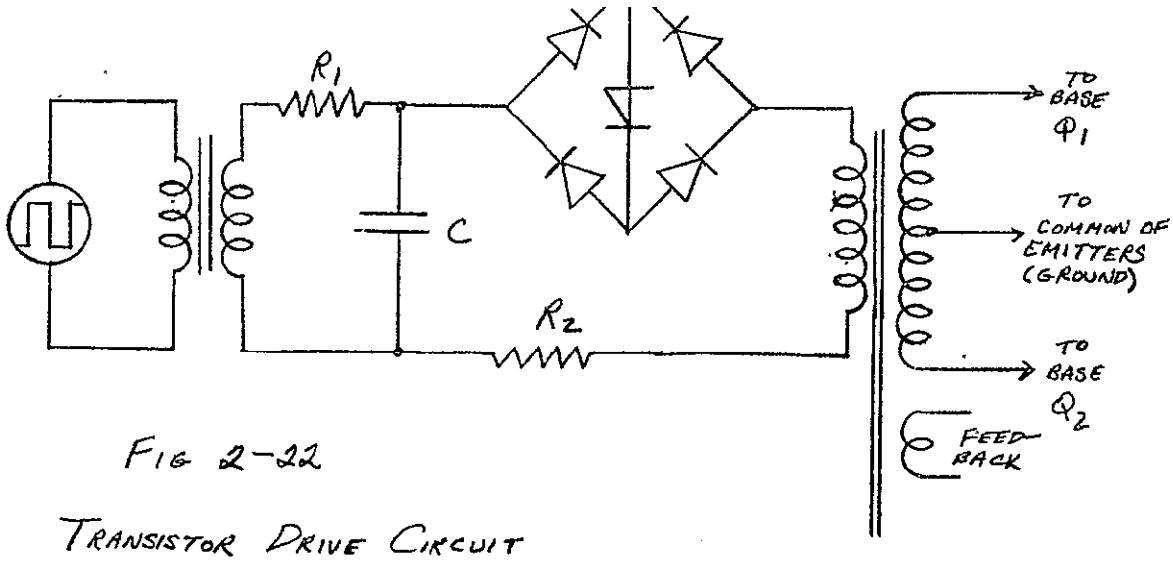


FIG 2-22

TRANSISTOR DRIVE CIRCUIT

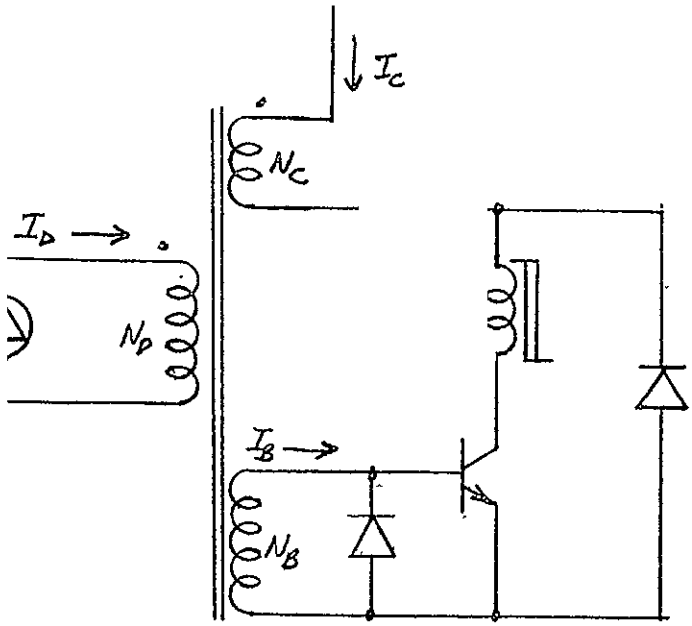
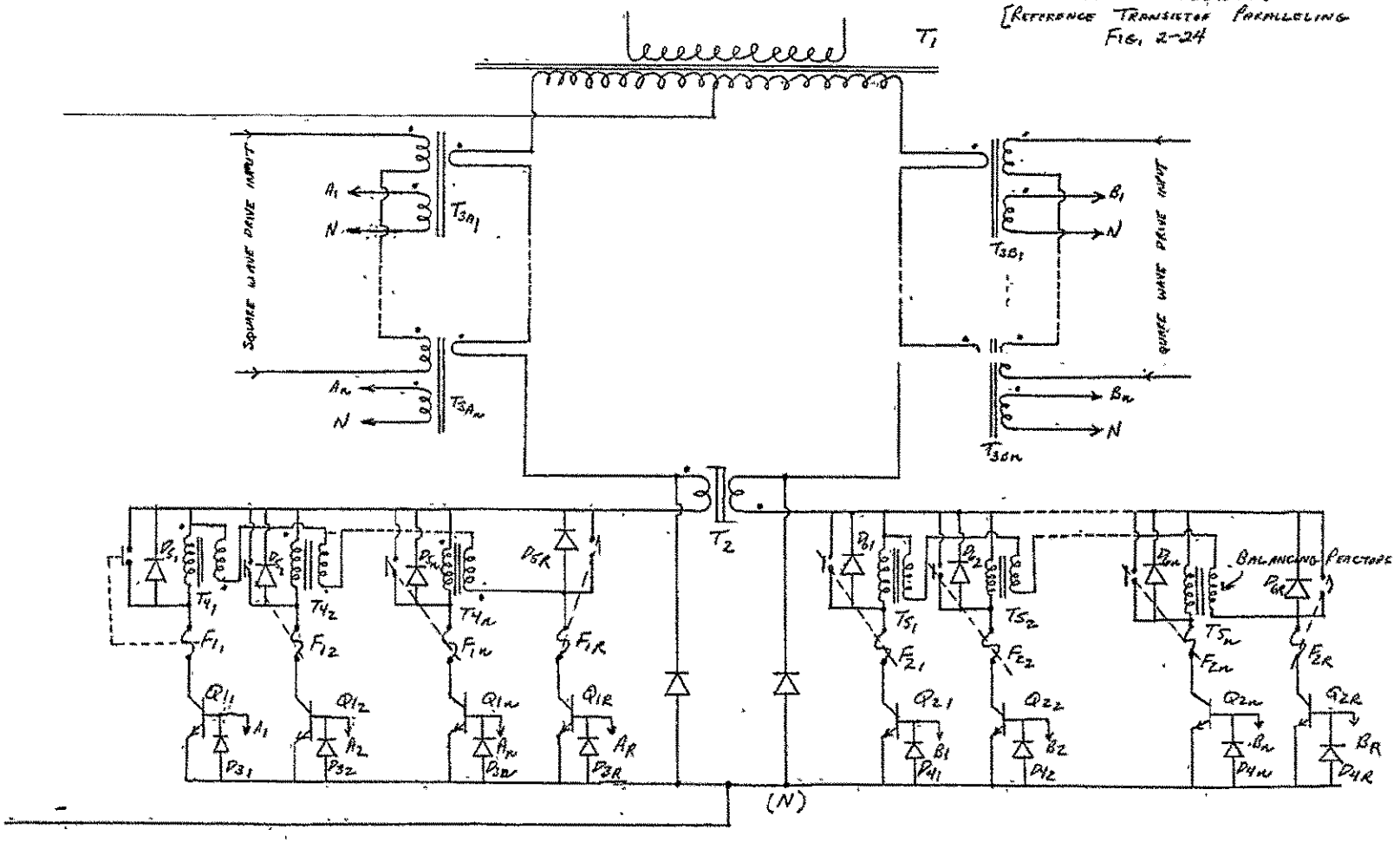


FIG. 2-23 PROPORTIONAL DRIVE SCHEMATIC

TRANSISTOR OUTPUT STAGE [SQUARE WAVE] WITH CURRENT FEEDBACK [REFERENCE TRANSISTOR PARALLELING

FIG. 2-24



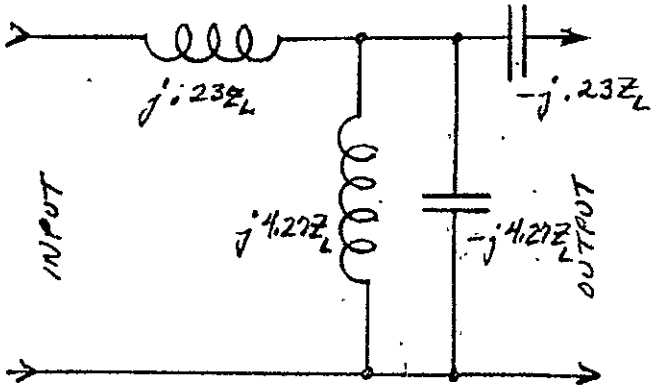


FIG 2-25C
MODIFIED FILTER WITH ELEMENT VALUES SUITABLE FOR SIX-SQUARE WAVE APPROXIMATION

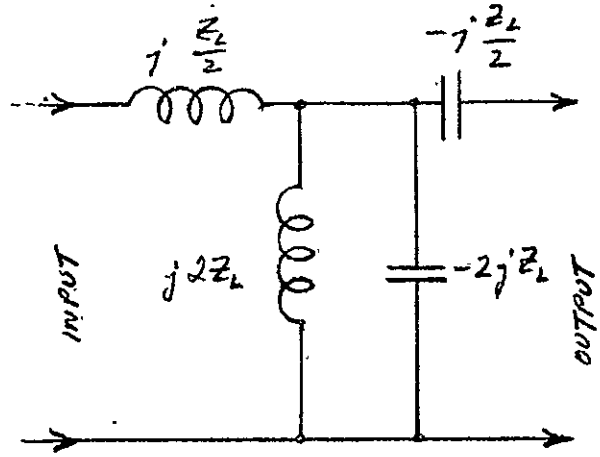
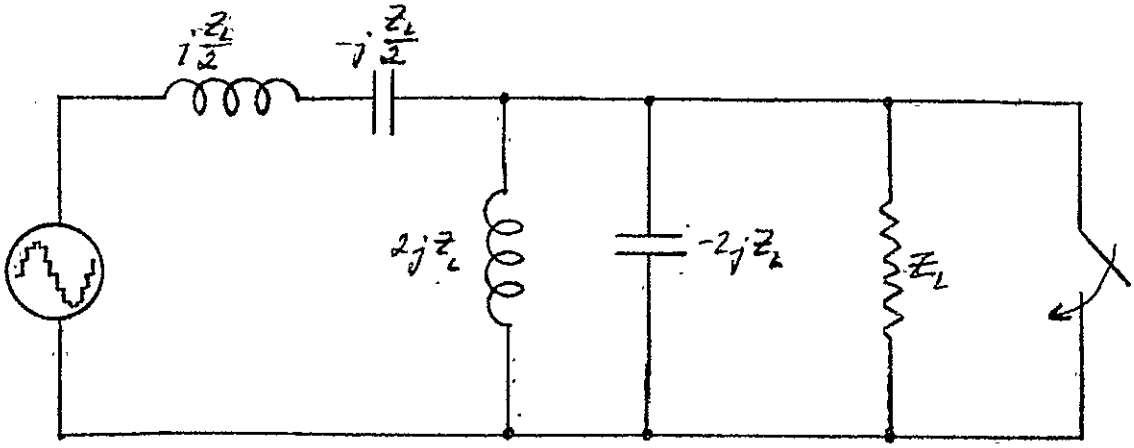


FIG 2-25B
MODIFIED FOURTH ORDER RESONANT BANDPASS FILTER



FILTER CIRCUIT WITH SHORT CKT. APPLIED TO OUTPUT
(CONVENTIONAL FOURTH ORDER RESONANT BANDPASS FILTER)

NOTE: Z_L REPRESENTS THE LOAD RESISTANCE REQUIRED TO HAVE THE INVERTER DELIVER RATED (100%) OUTPUT.

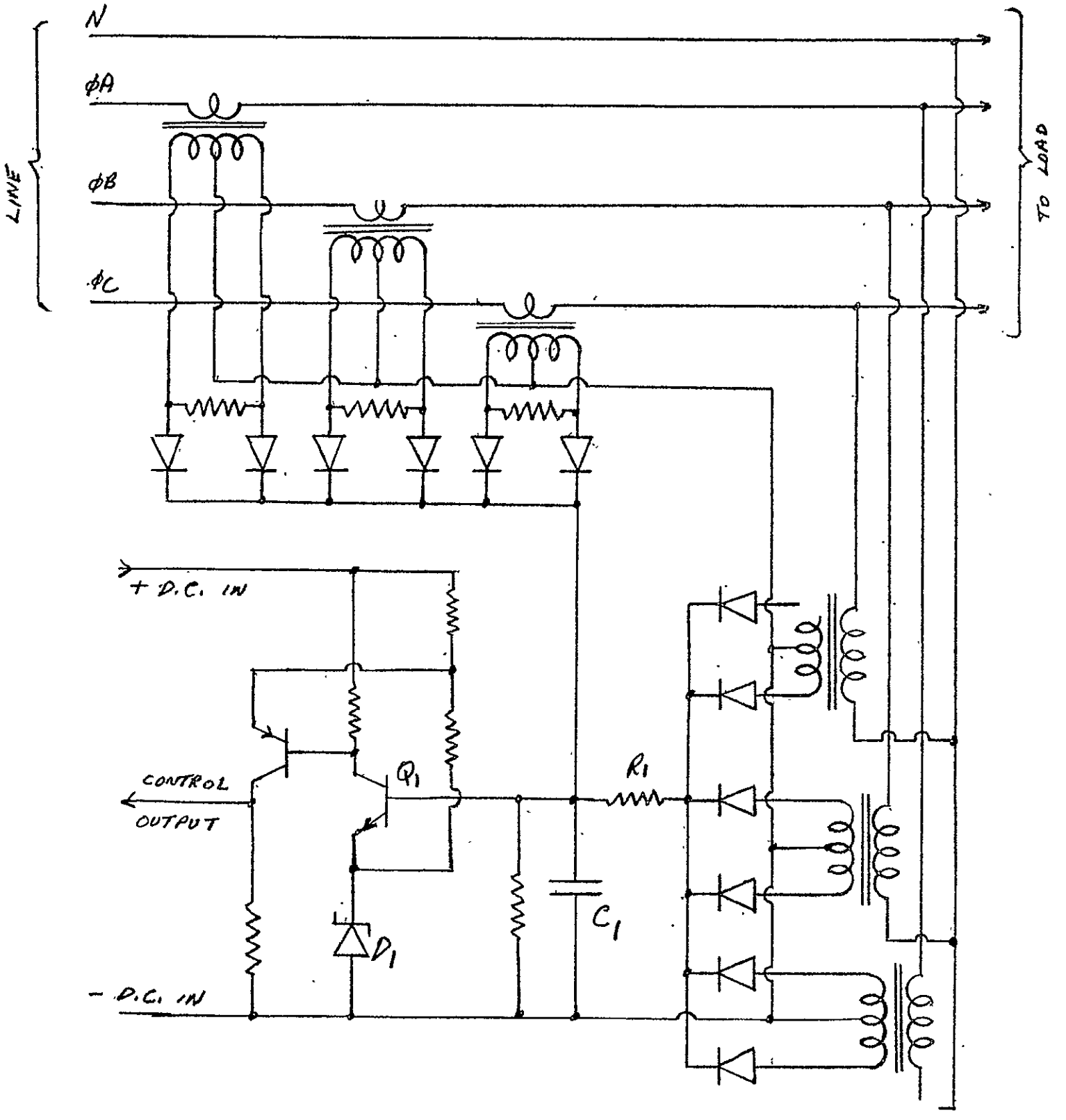


FIG. 2-26 VOLTAGE AND CURRENT SENSING CIRCUITRY

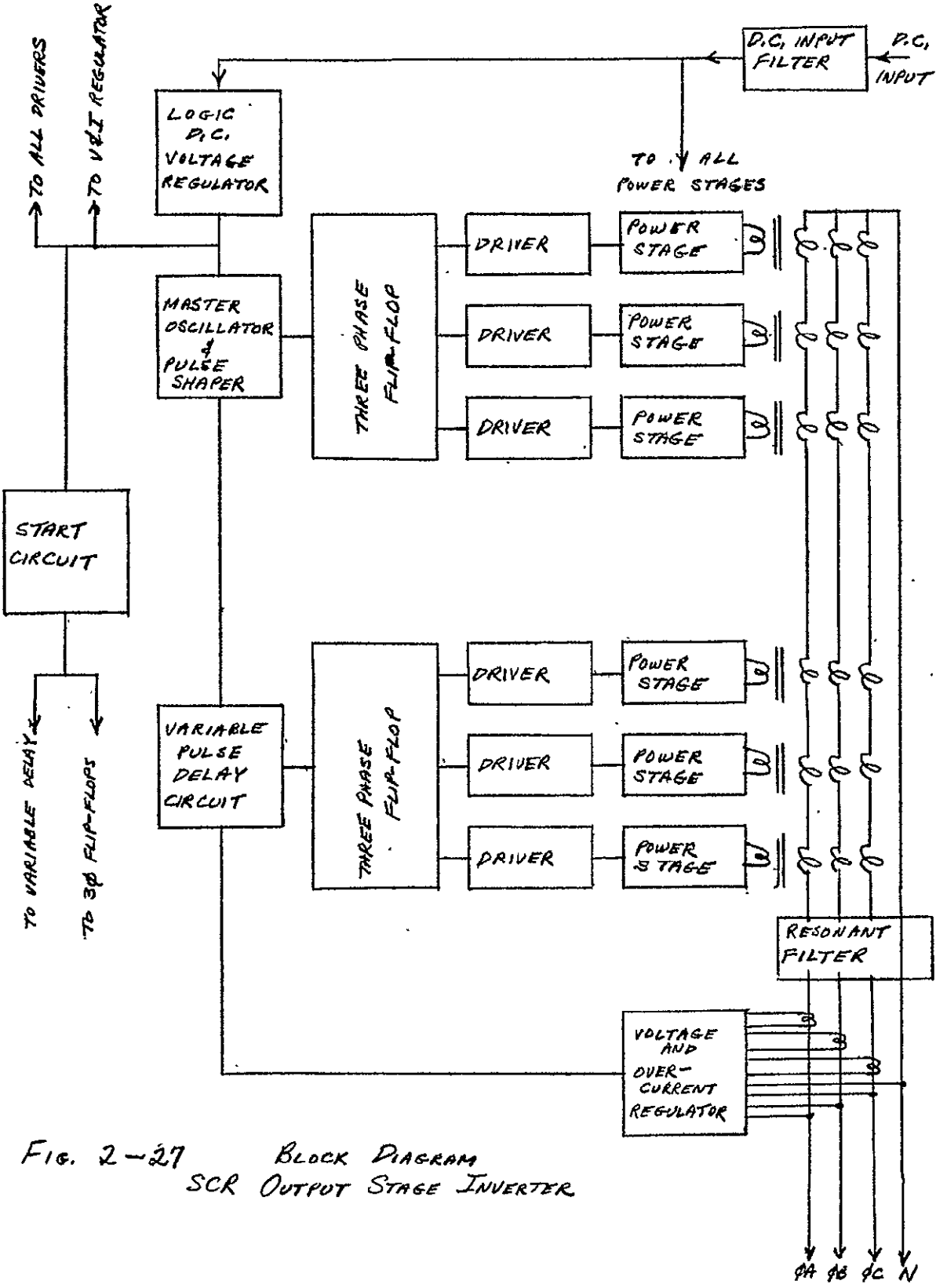


FIG. 2-27 BLOCK DIAGRAM
SCR OUTPUT STAGE INVERTER

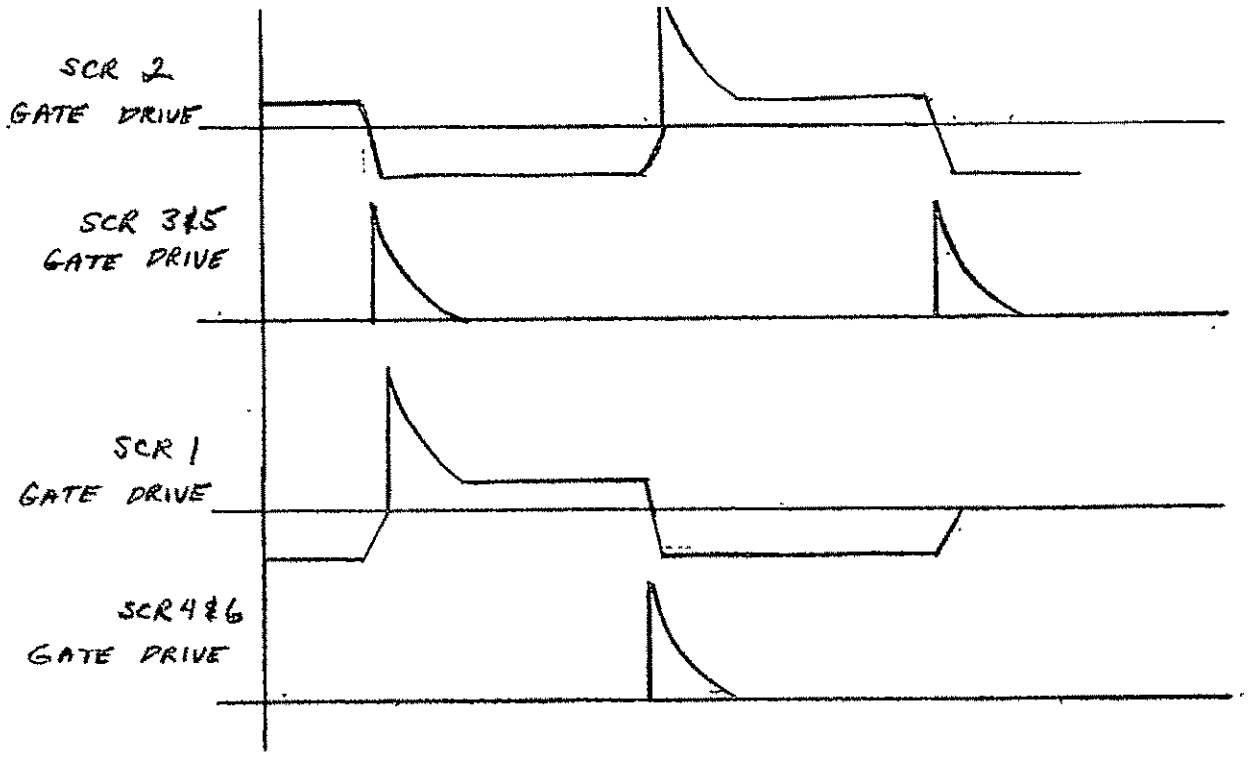


FIG. 2-28 DRIVE WAVEFORMS FOR SCR POWER STAGE (OUTPUT OF CKT. OF FIG 2-32)

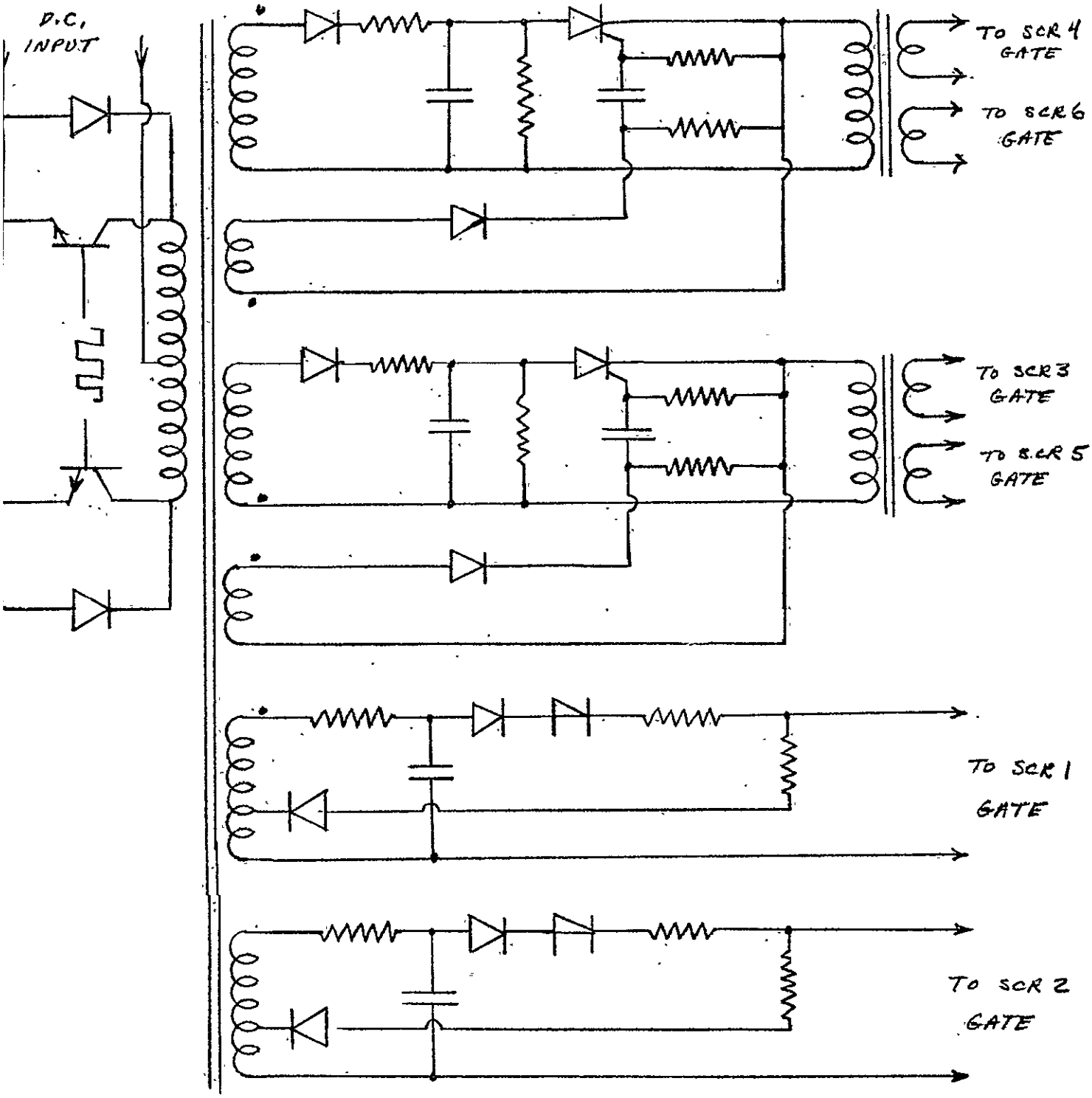


FIG. 2-29 DRIVE CIRCUIT FOR MCMURRAY INVERTER

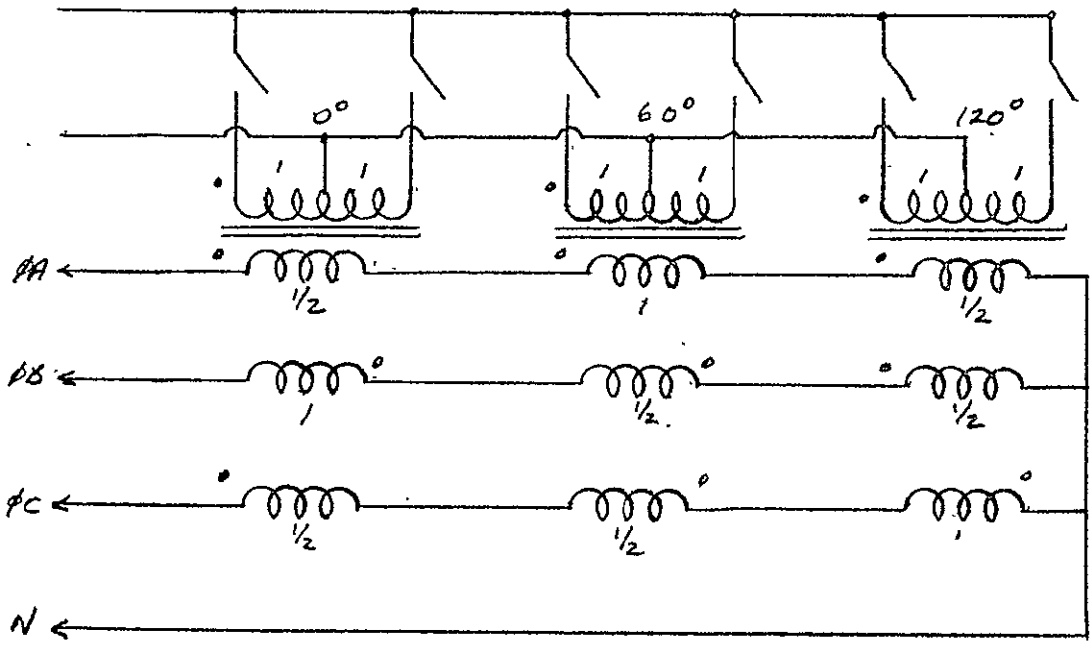


FIG 2-30 TRANSFORMER INTERCONNECTION SCHEME FOR SCR OUTPUT STAGE INVERTER

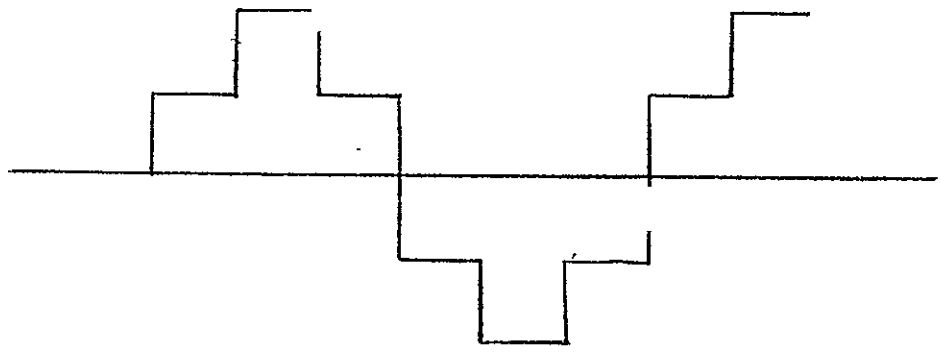


FIG 2-31 LINE-TO-NEUTRAL OUTPUT VOLTAGE OF SCR INVERTER (INTERCONNECTION SHOWN IN FIG. 2-30)

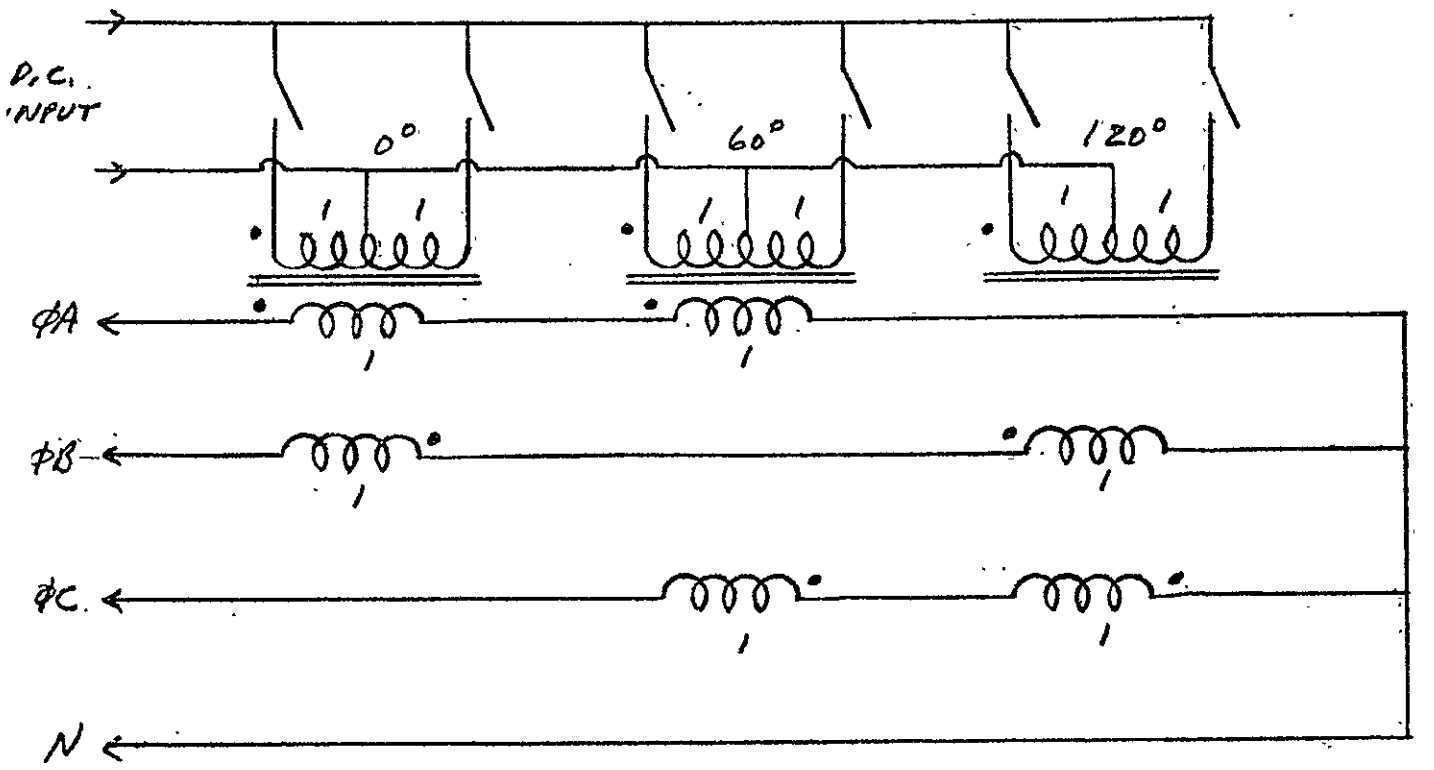


FIG. 2-32 TRANSFORMER INTERCONNECTION SCHEME FOR SCR CIRCUIT ANALYZED.

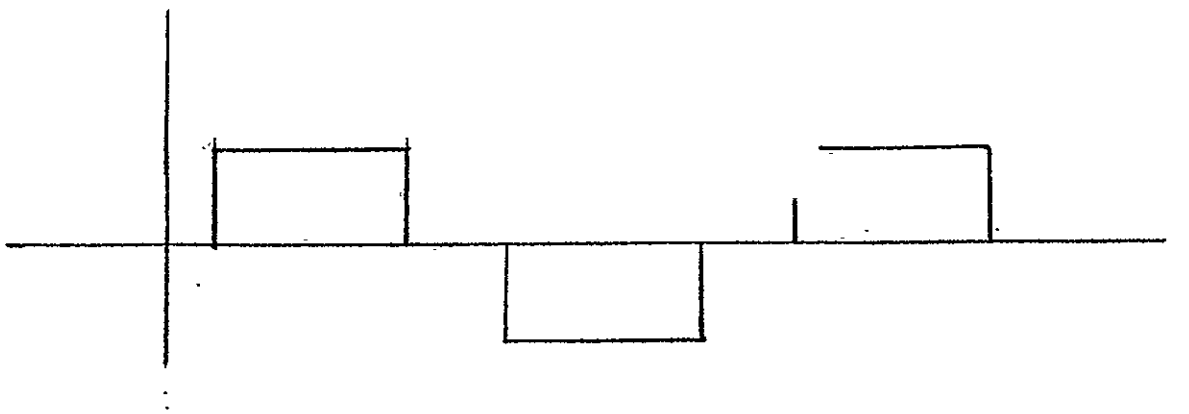


FIG. 2-33 LINE-TO-NEUTRAL OUTPUT VOLTAGE OF SCR INVERTER WITH INTERCONNECTION DIAGRAM OF FIG 2-32.

FIGURE 47 • Core Loss vs. Induction Level for Square Permalloy 80

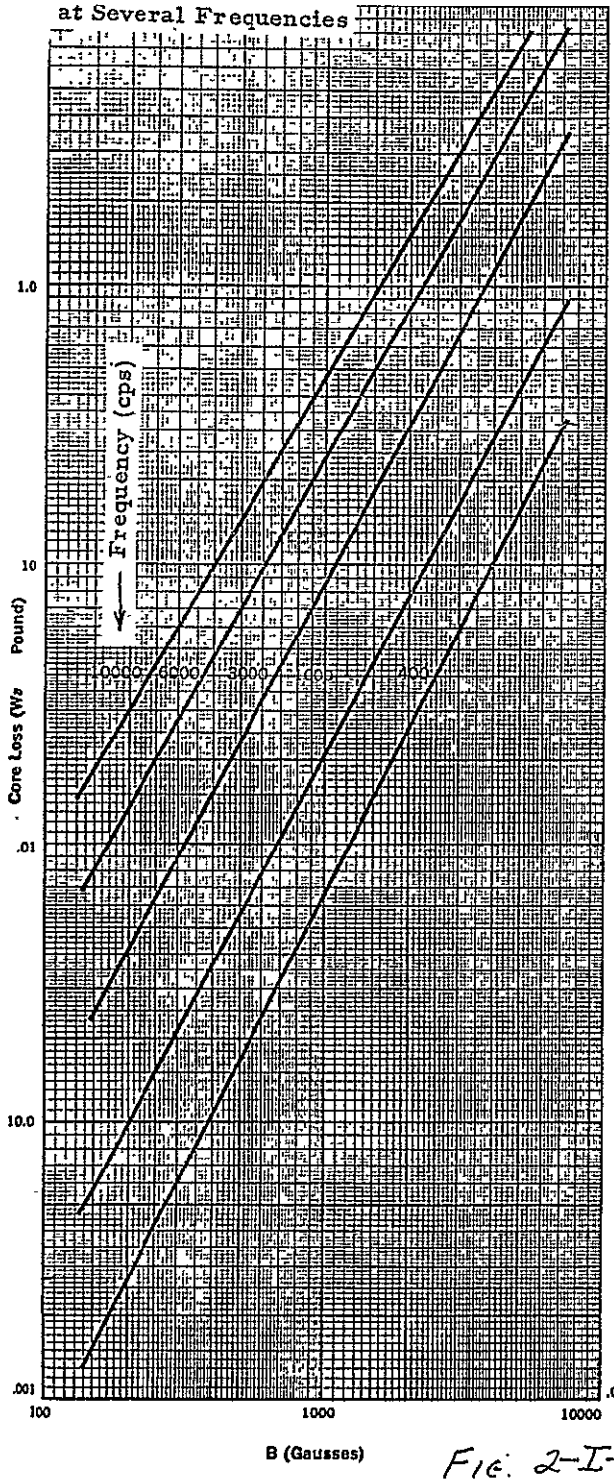
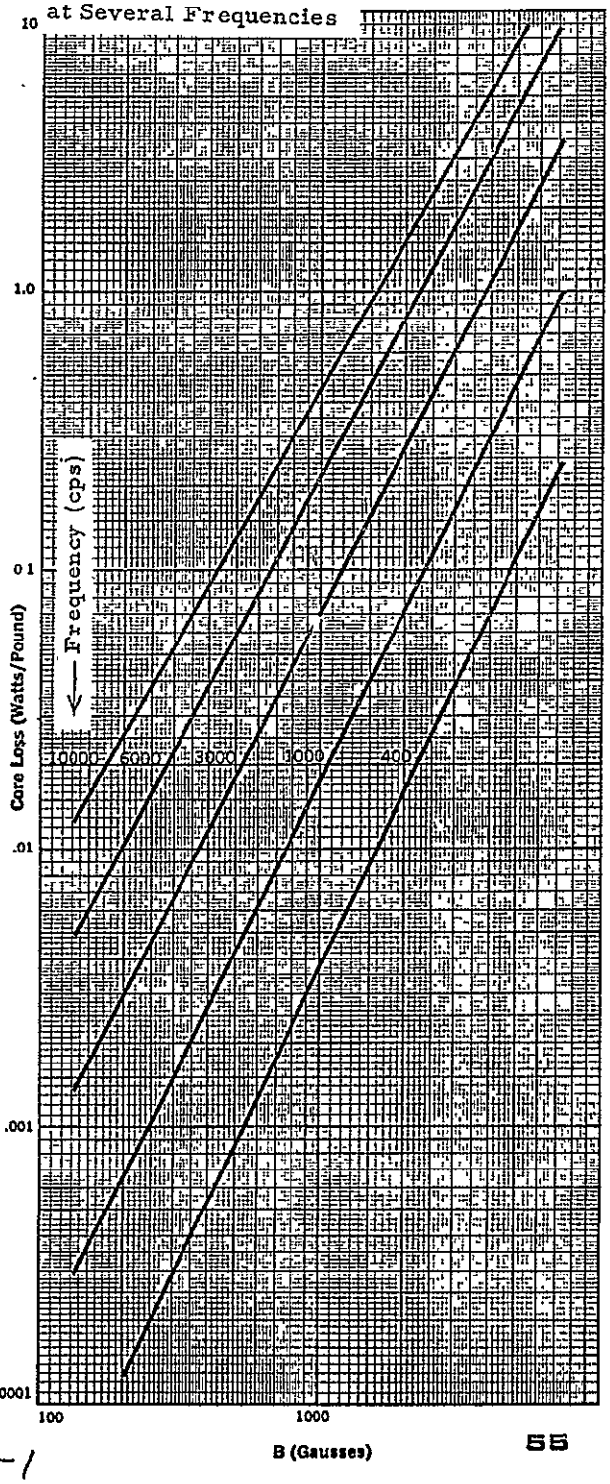


Fig. 2-I-1

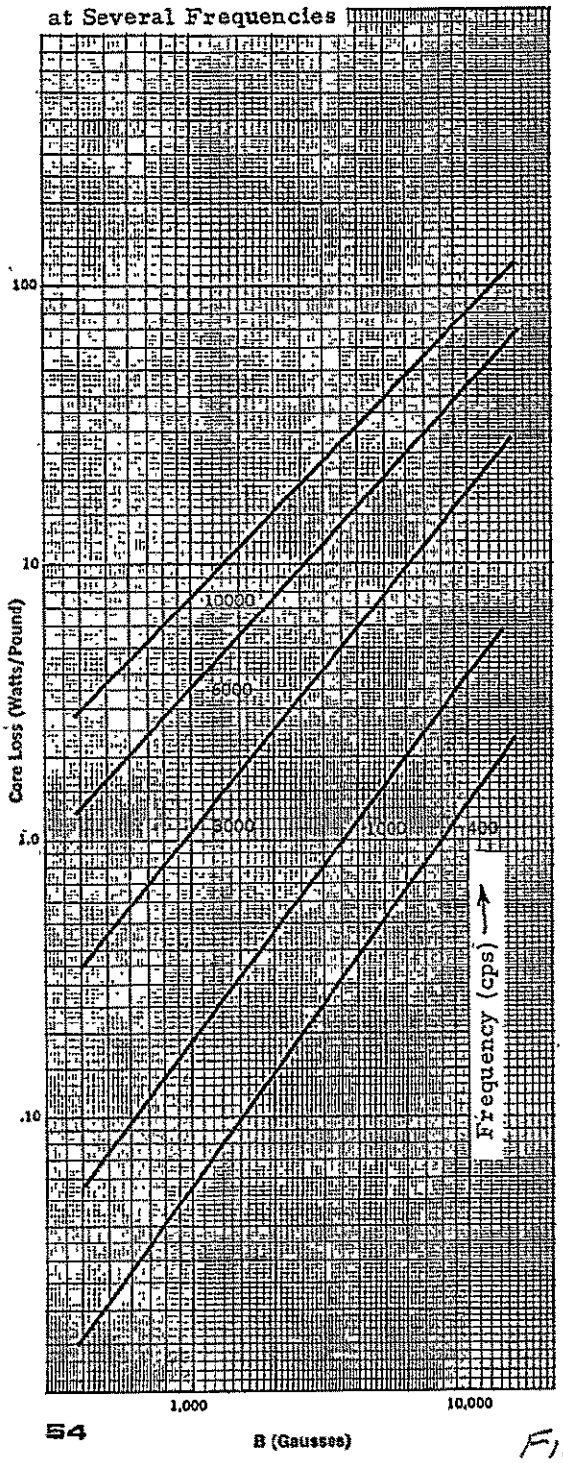
FIGURE 48 • Core Loss vs. Induction Level for Supermalloy



55

CORE LOSS vs. INDUCTION LEVEL

FIGURE 45 • Core Loss vs. Induction Level for Orthonol



54

FIGURE 46 • Core Loss vs. Induction Level for 48 Alloy

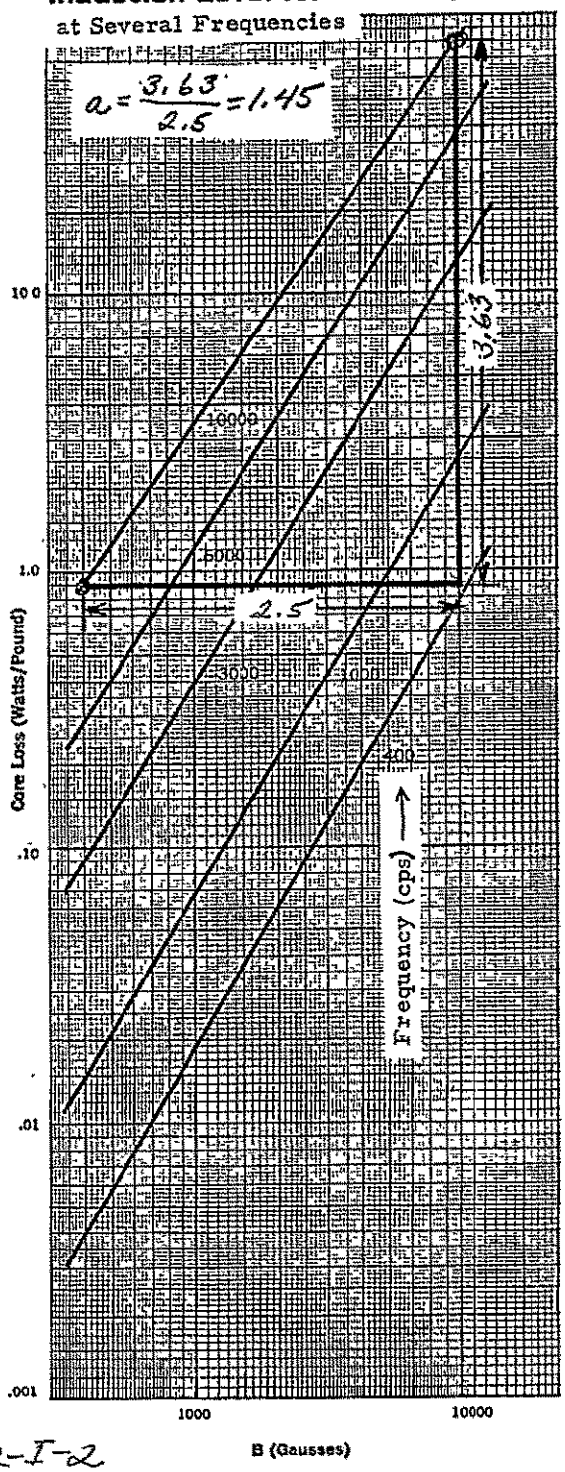


Fig. 2-I-2

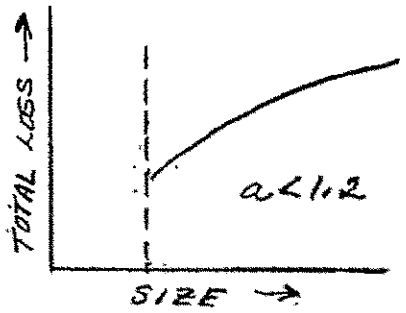


FIG. 2-II-1

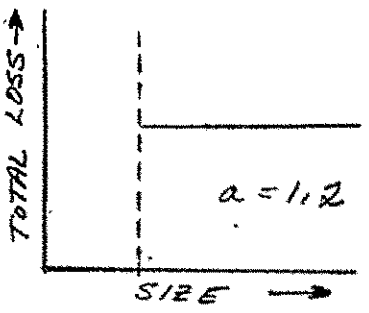


FIG. 2-II-2

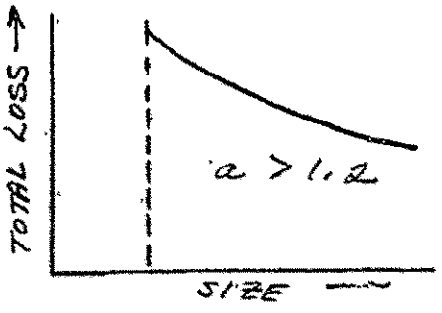


FIG. 2-II-3

VARIATIONS OF TOTAL LOSSES WITH SIZE FOR TRANSFORMERS OPERATED AT CONSTANT OUTPUT POWER AND FREQUENCY FOR DIFFEREN RANGES OF VALUES OF "a". (TRANSFORMERS ARE DESIGNED SUCH THAT CORE LOSS = $(2/a)$ COPPER LOSS.)

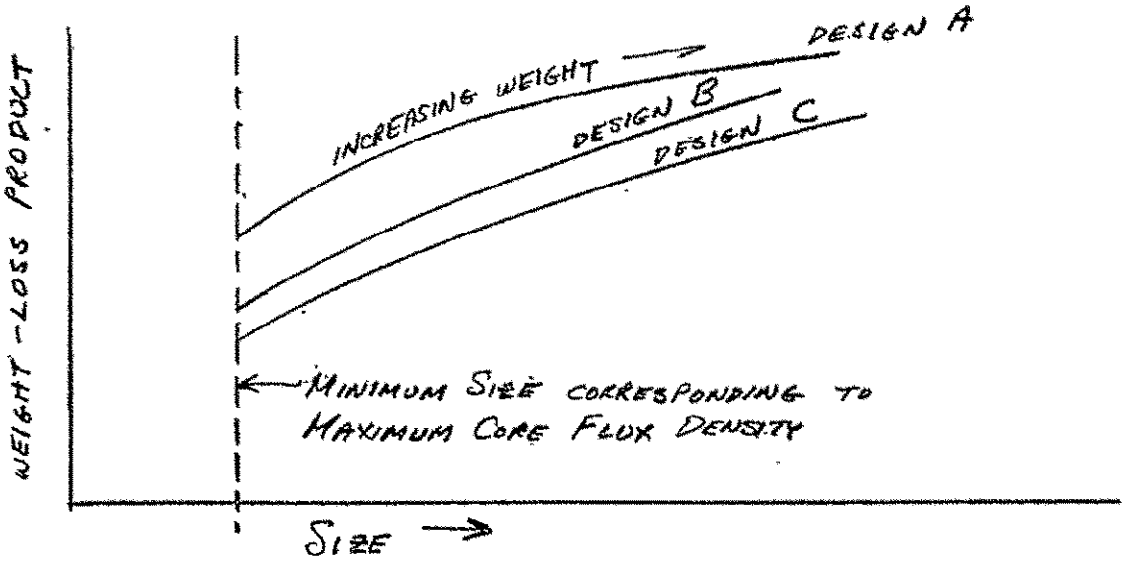


FIG. 2-II-4

VARIATION OF WEIGHT-LOSS PRODUCT WITH TRANSFORMER SIZE

FIG. 2-III-1 ONE DIMENSIONAL HEAT FLOW PROBLEM

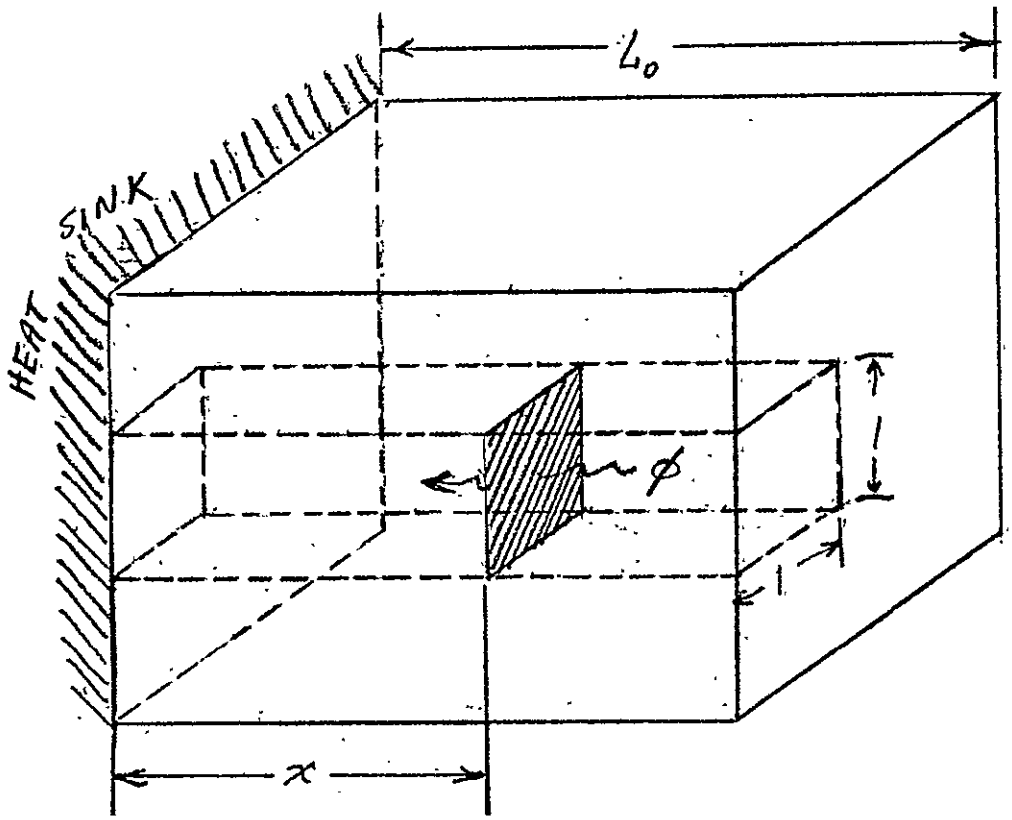
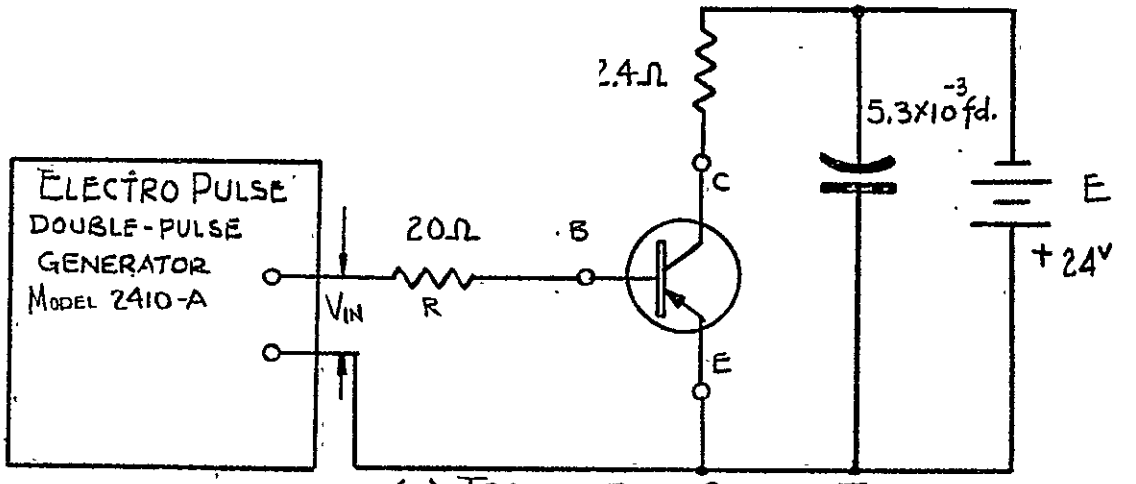
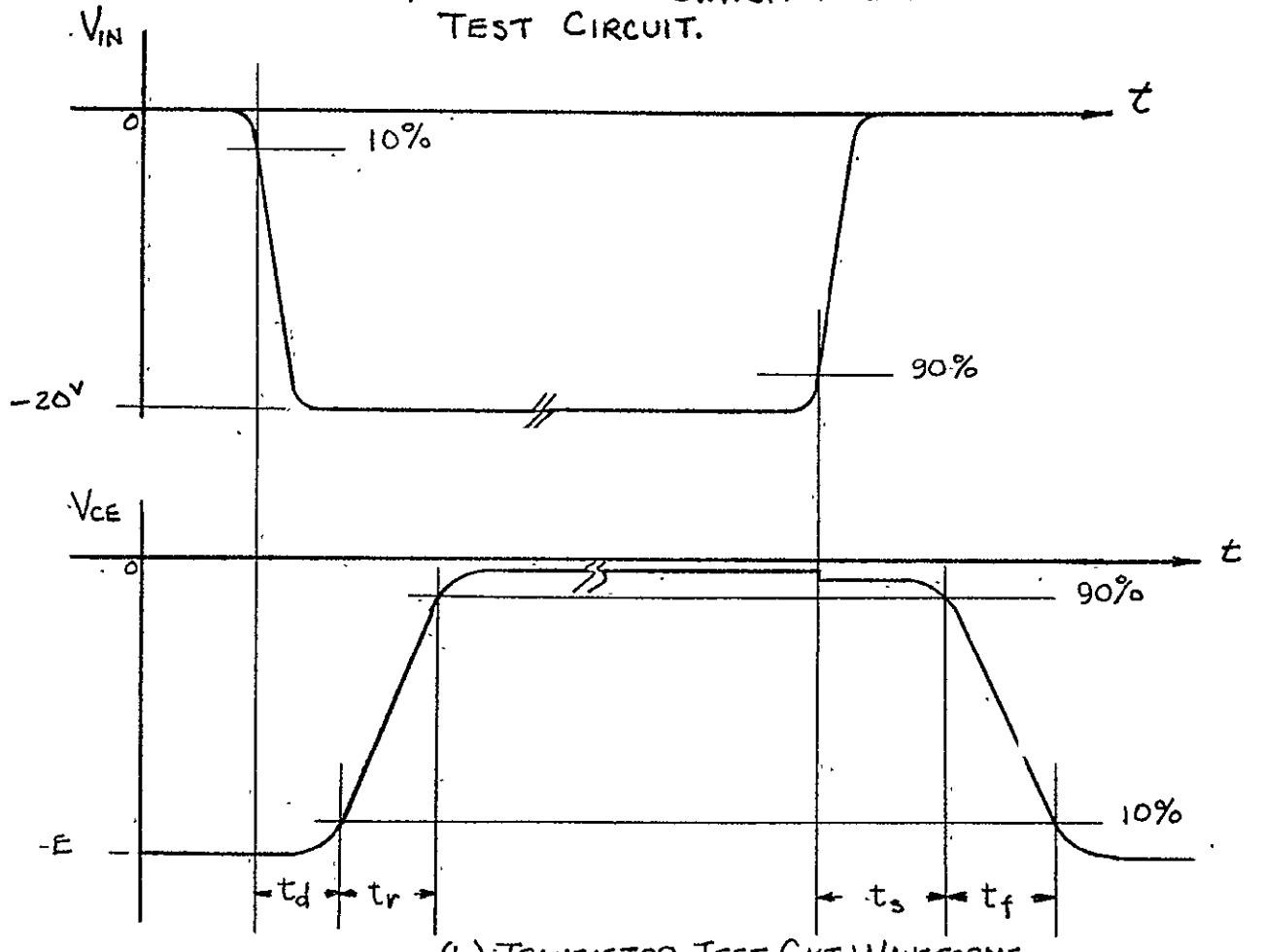


FIGURE 2-IV-1



(a) TRANSISTOR SWITCH TIME TEST CIRCUIT.

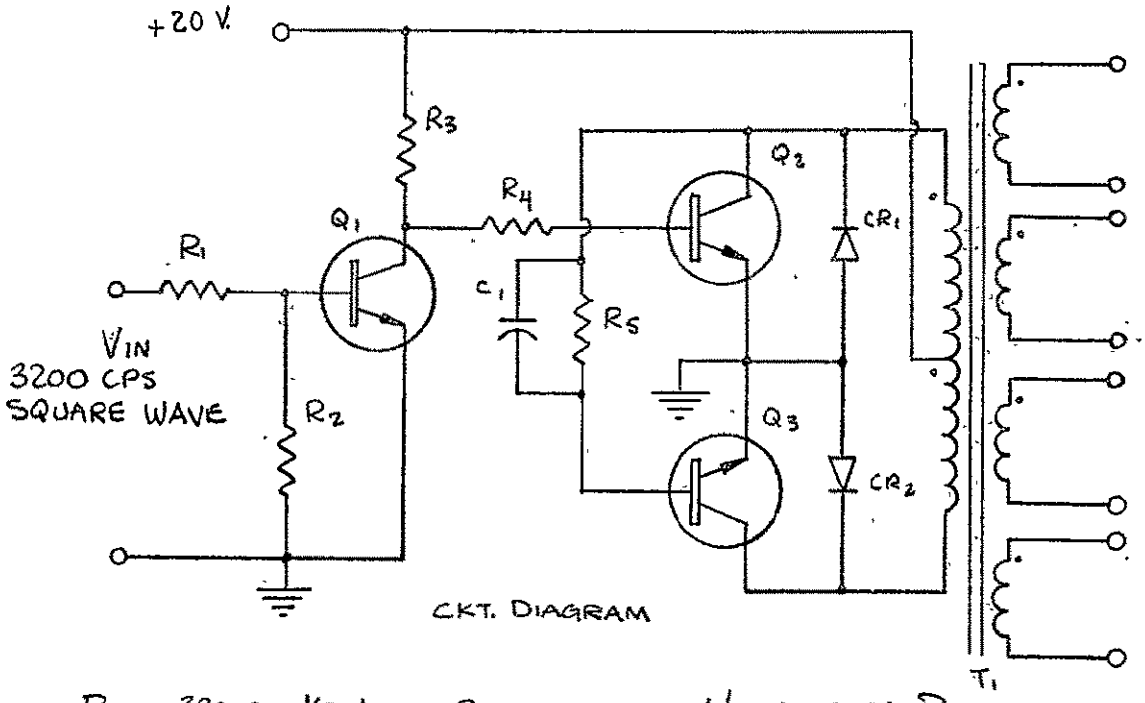


(b) TRANSISTOR TEST CKT. WAVEFORMS

td = DELAY TIME
tr = RISE TIME
ts = STORAGE TIME
tf = FALL TIME

FIGURE 2-IV-2

DRIVE CIRCUIT

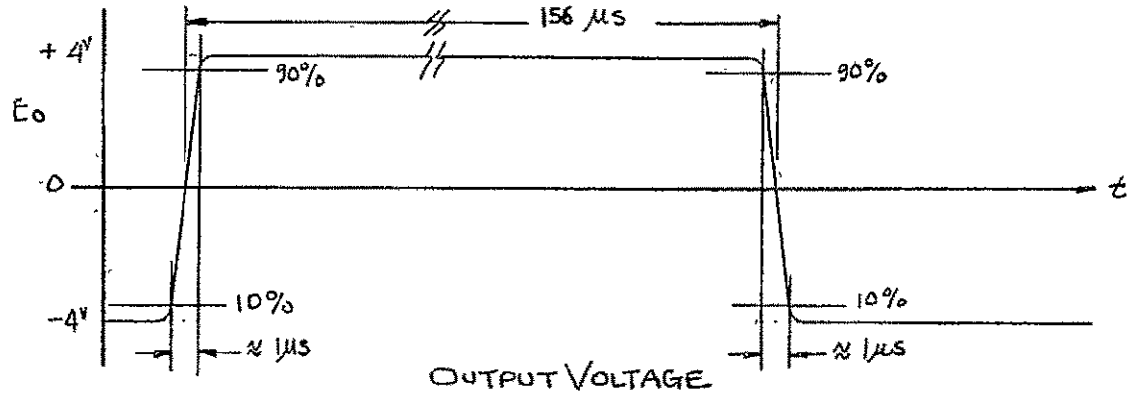


CKT. DIAGRAM

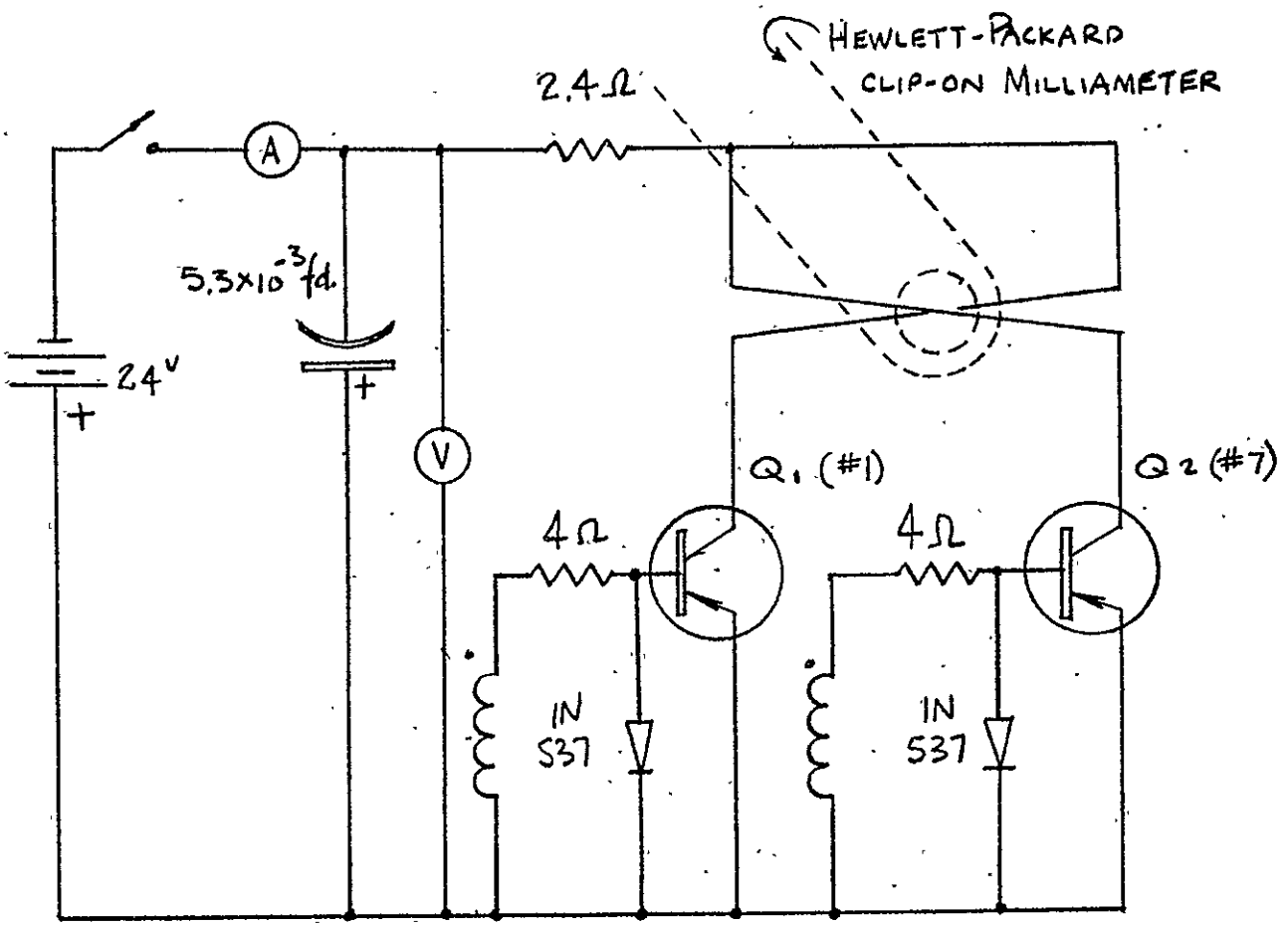
R_1 - 390Ω ½W
R_2 - 5.6K ½W
R_3 - 390Ω 1W
R_4 - 22Ω 1W
R_S - 680Ω 1W

C_1 - .0022 μfd. - 600VDC PAPER
$Q_{1,2,3}$ - 2N2270 - RCA
$CR_{1,2}$ - 1N645

T_1 - CORE - SQUARE STACK OF E1-375 6MIL 48 ALLOY
PRIMARY - 60/60 TURNS NO. 25
SECONDARIES - 12 TURNS NO. 22 EACH.
TRANSFORMER COIL WOUND USING MULTI-FILAR TECHNIQUES.
(PRIMARY AND SECONDARY COILS WOUND TOGETHER)
LEAKAGE INDUCTANCE ½ PRIMARY TO SECONDARY = 73μhy.

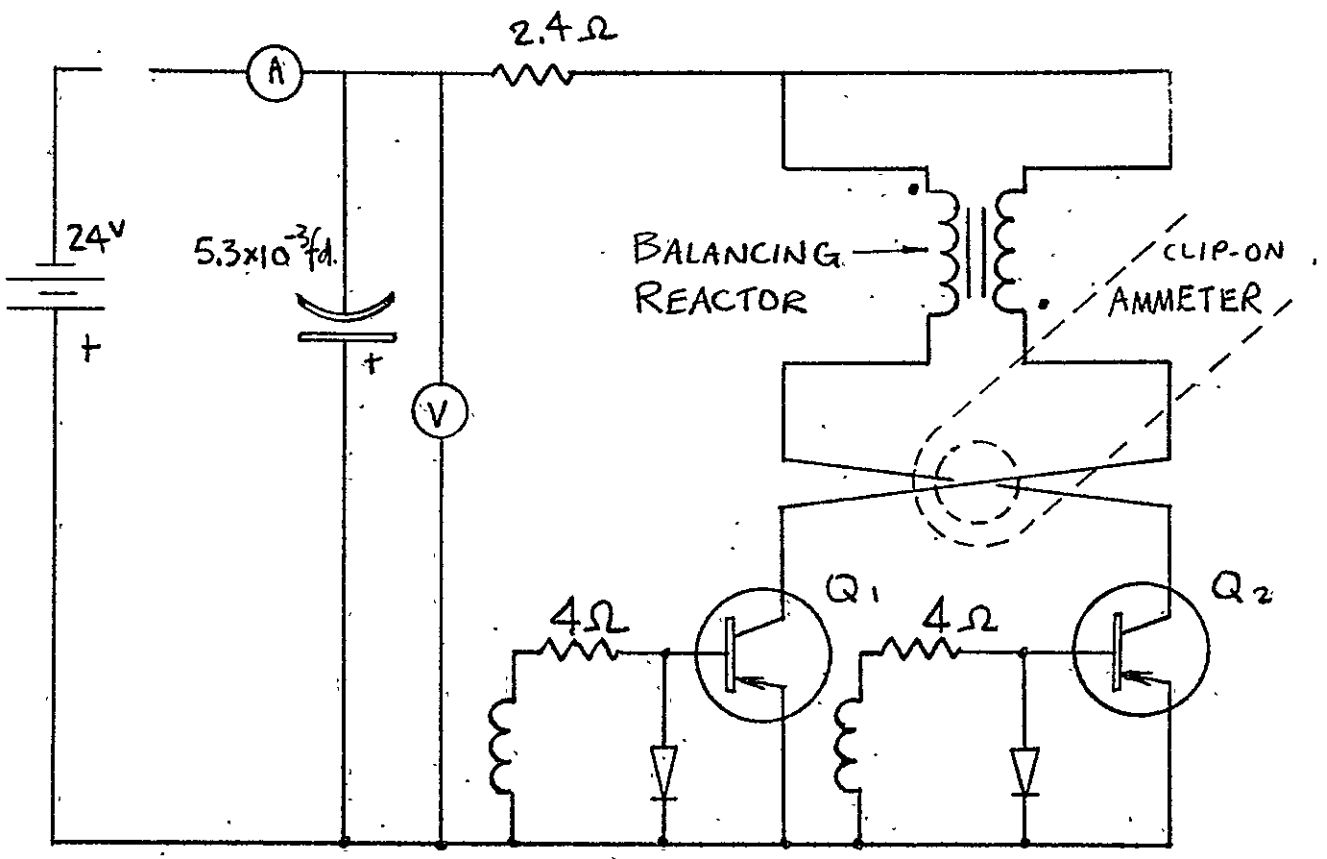


OUTPUT VOLTAGE



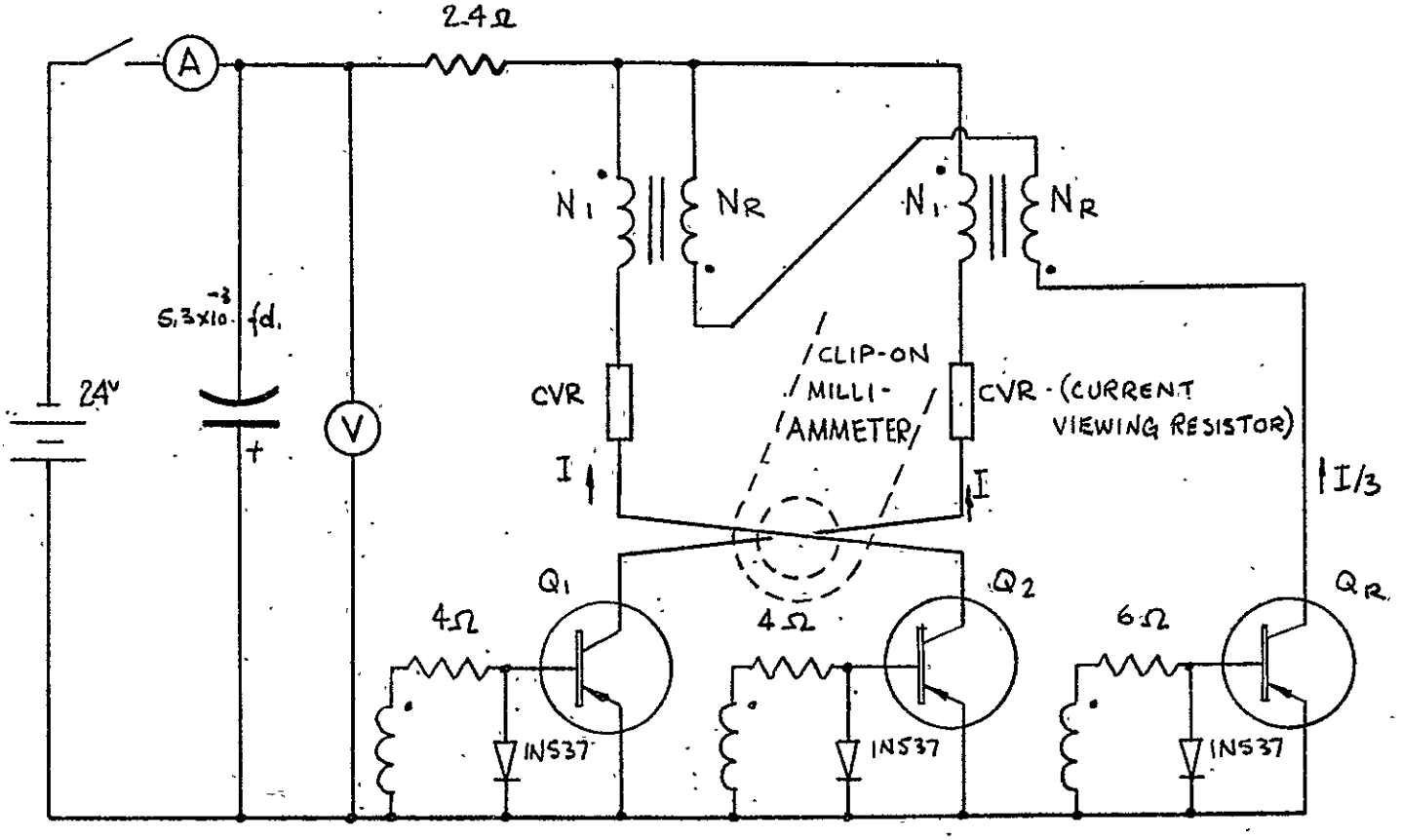
DIRECT PARALLELING

FIGURE 2-IV-3



BALANCING REACTOR PARALLELING

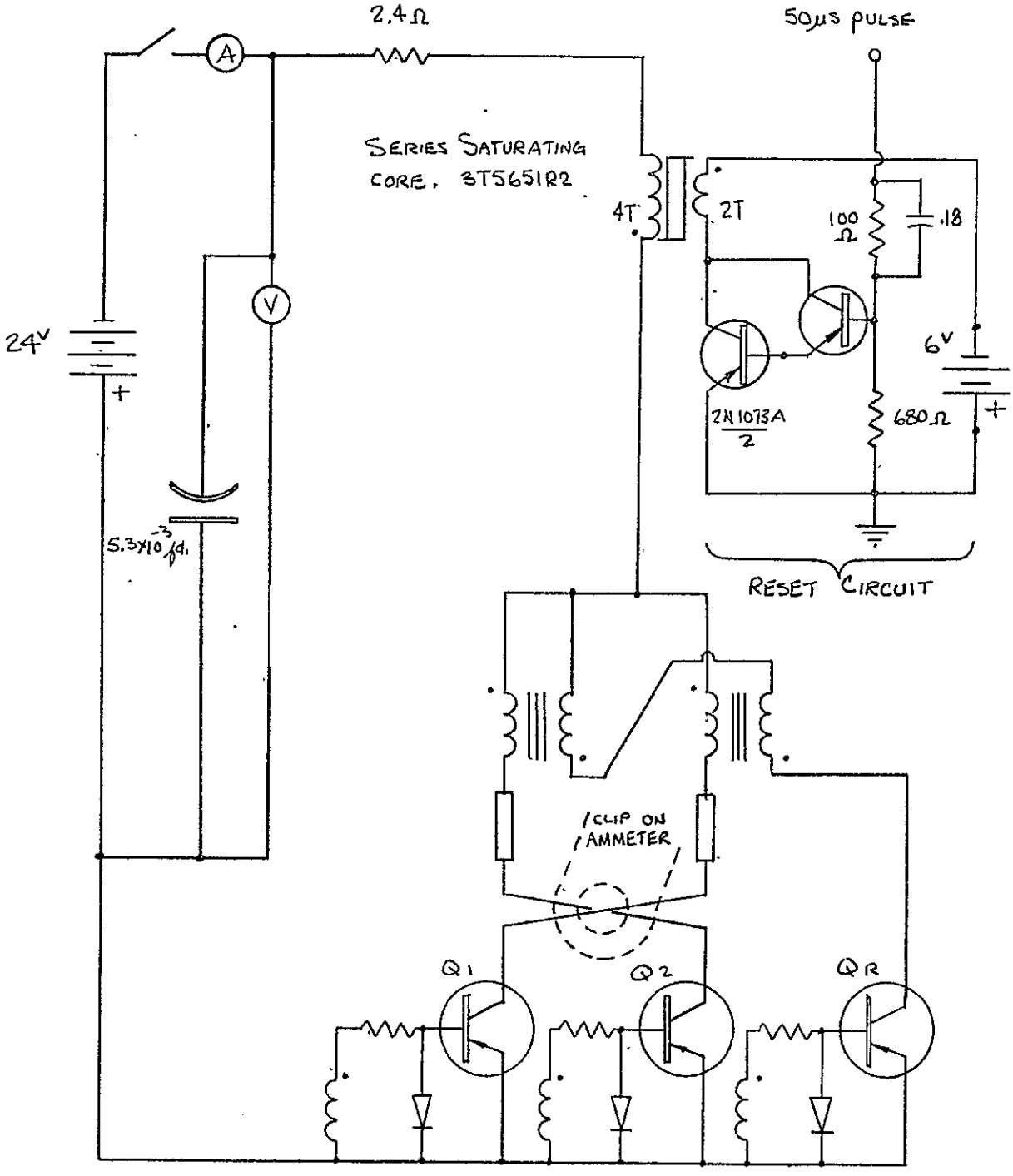
FIGURE 2-IV-4

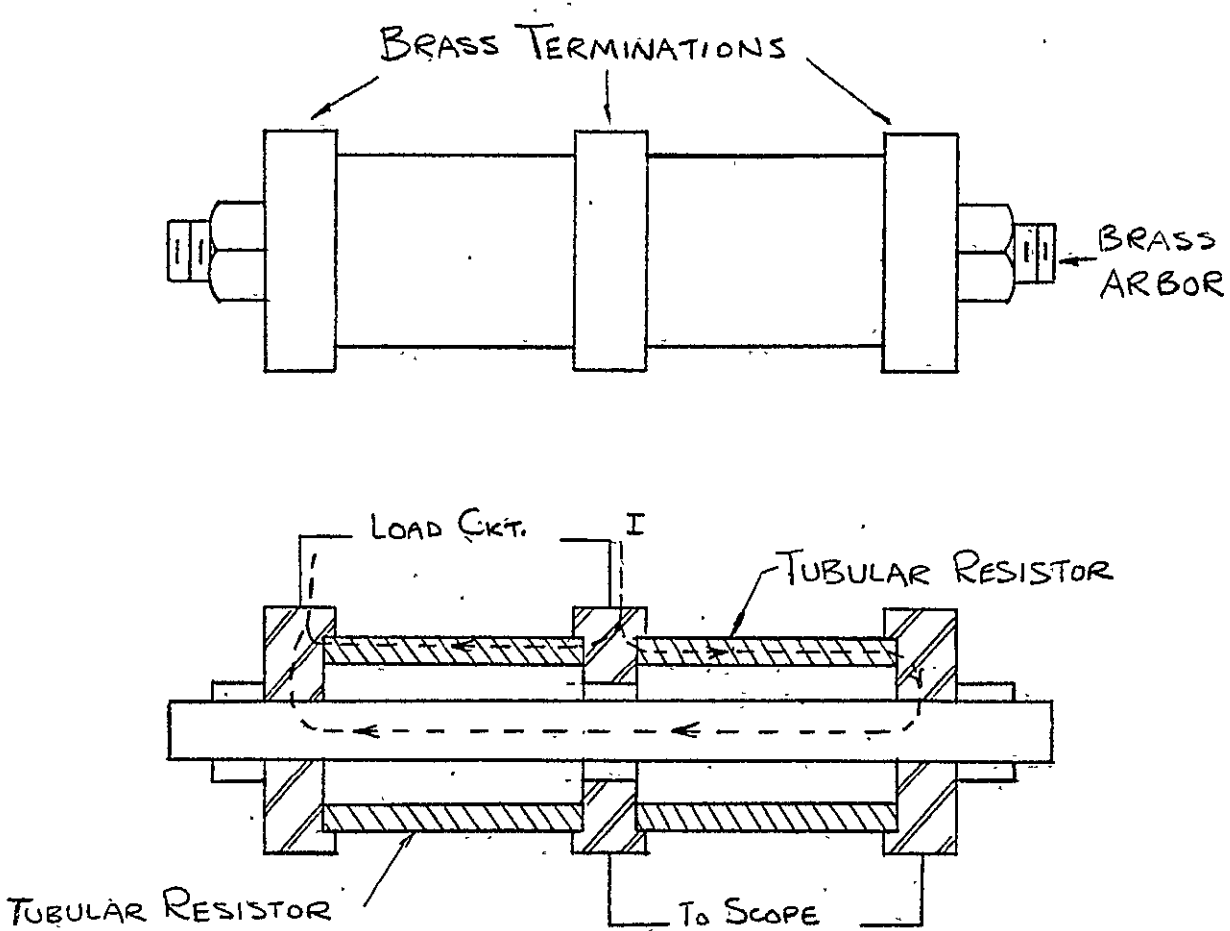


REFERENCED BALANCING REACTOR PARALLELING CIRCUIT DIAGRAM

FIGURE 2-IV-5

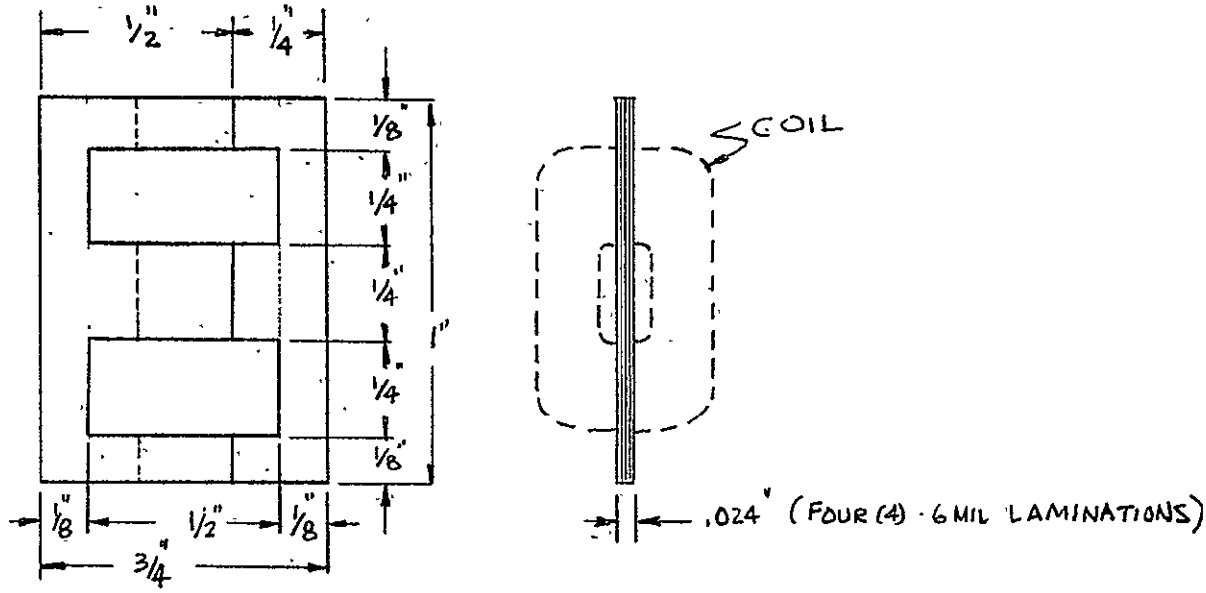
FIGURE 2-IV-6
PARALLELING WITH REFERENCED BALANCING REACTOR AND DELAY CORE.

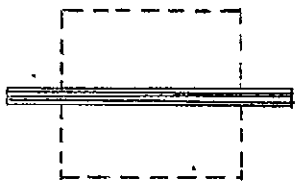




CURRENT VIEWING RESISTOR (COAXIAL)
FIGURE 2-IV-7

BALANCING REACTORS





LAMINATION - EE24-24 -6 MIL 48 ALLOY

SIMPLE BALANCING REACTOR COIL 4/4 TURNS

REFERENCE BALANCING REACTOR COIL $N_1 = 8$ TURNS
$N_R = 24$ TURNS (3:1)

FIG 2-IV-8

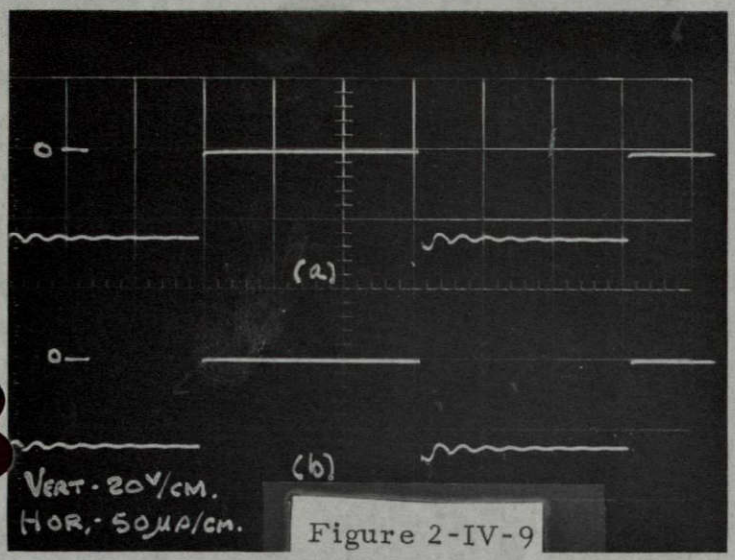


Figure 2-IV-9

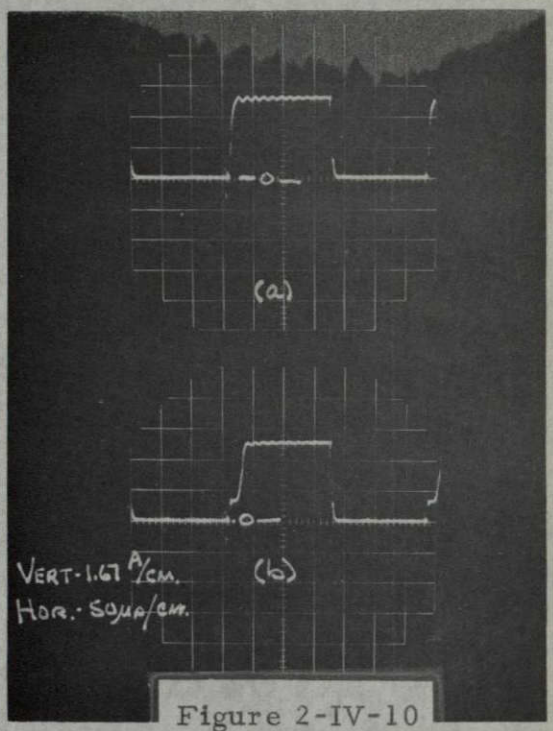


Figure 2-IV-10

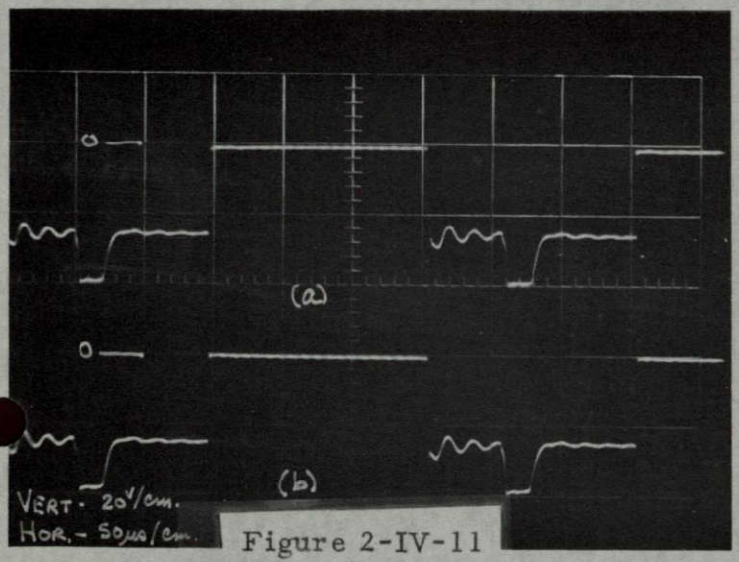


Figure 2-IV-11

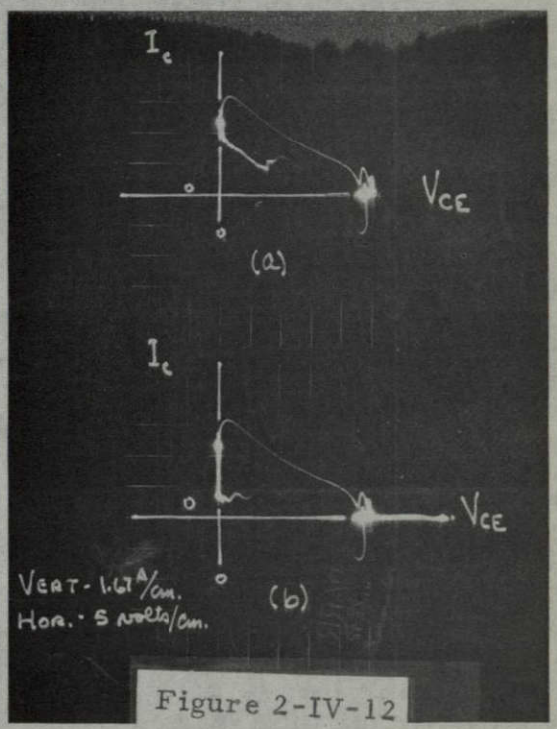


Figure 2-IV-12

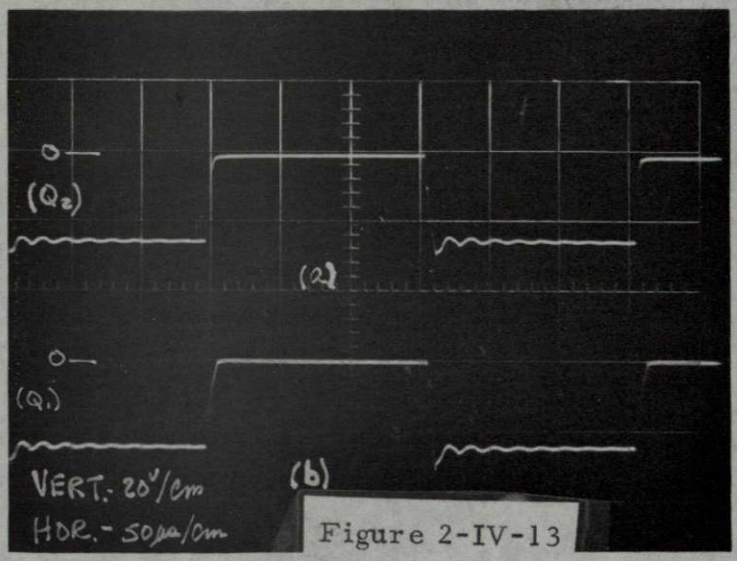


Figure 2-IV-13

Oscillographs

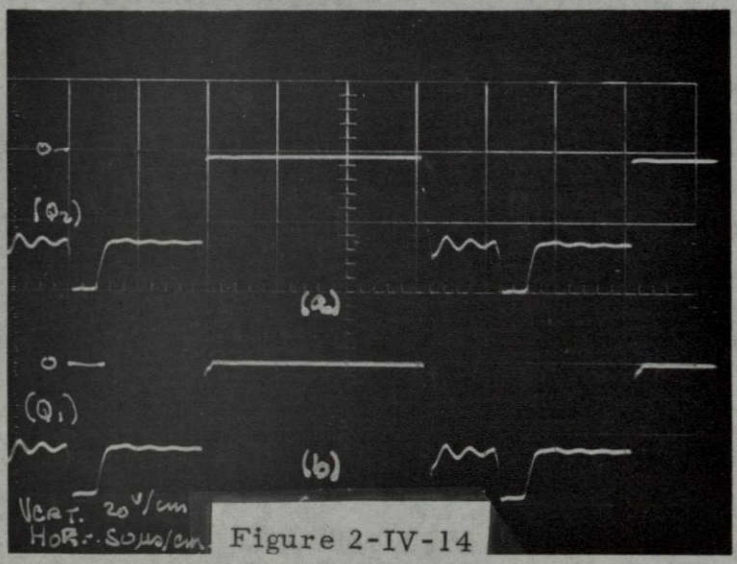


Figure 2-IV-14

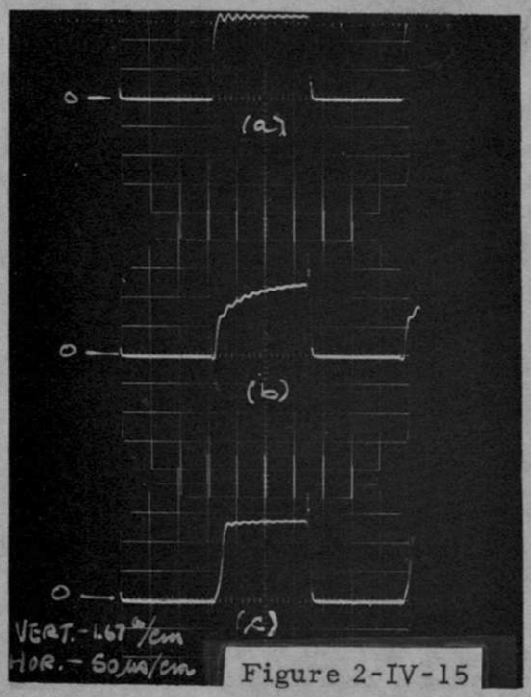


Figure 2-IV-15

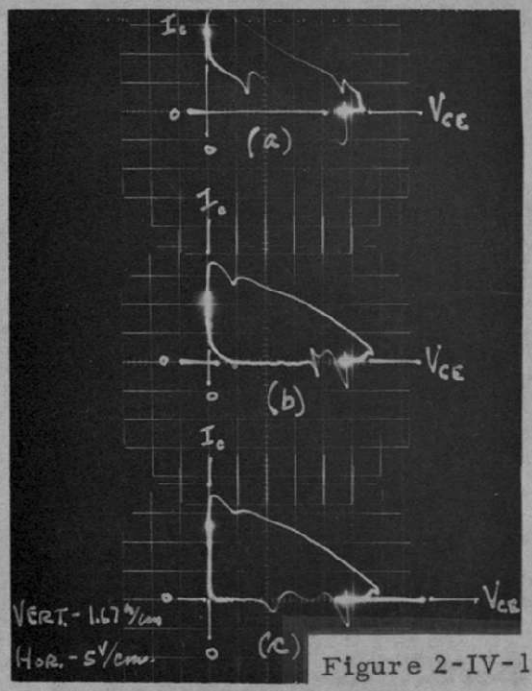


Figure 2-IV-16

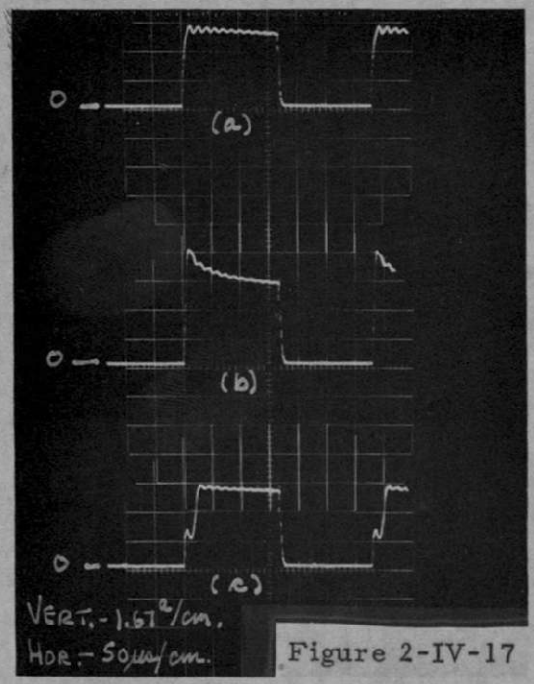


Figure 2-IV-17

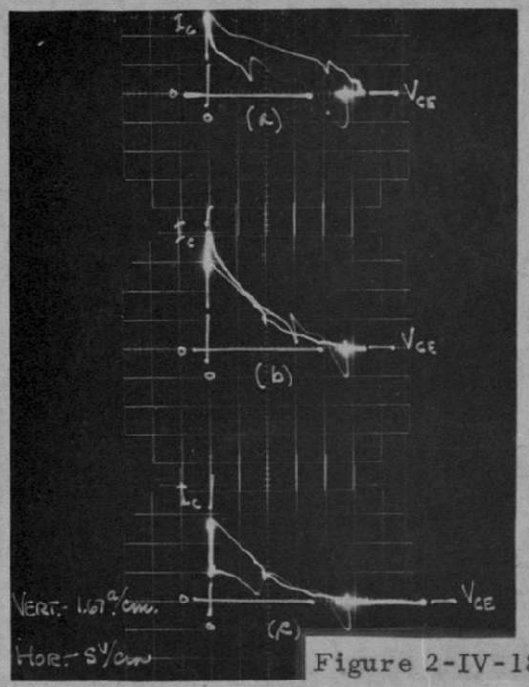


Figure 2-IV-18

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