TEXAS INSTRUMENTS INCORPORATED
Apparatus Division
13500 North Central Expressway
Dallas, Texas 75222

# FINAL ENGINEERING REPORT
# RANGER COMMAND SUBSYSTEM FOLLOW-ON

17-48420-Final

JPL Contract No. 950065

5 May 1964



Prepared for
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

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References: (a) Jet Propulsion Laboratory Contract No. 950065

(b) Texas Instruments Incorporated Proposal No. A62-194 dated 8 October 1962

## SECTION I

## INTRODUCTION

Texas Instruments Incorporated was engaged by Jet Propulsion Laboratory to design and fabricate the digital command detector (Figure 1) and the digital command decoder (Figure 2) for the Ranger Block III Command System as specified under the provisions of References (a) and (b). This report, the final engineering report on the subject equipment, has been prepared in accordance with JPL Specification No. 20017.

The purpose of the Ranger Command Subsystem is to allow ground control over the spacecraft while in flight. The command subsystem receives its data inputs from the spacecraft transponder and generates switch closures which allow real time commands to operate or store data in the central computer and sequencer. The command subsystem also contains an auxiliary clock which will function in the event that the central spacecraft clock fails. This will allow control to be maintained over the spacecraft.

An important feature of this equipment is the means by which the component density is obtained. The digital building blocks used in the spacecraft command detector and decoder are of modular construction. This modular construction technique yields a component density of 100,000 components per cubic foot and an overall package component density of 50,000 components per cubic foot.

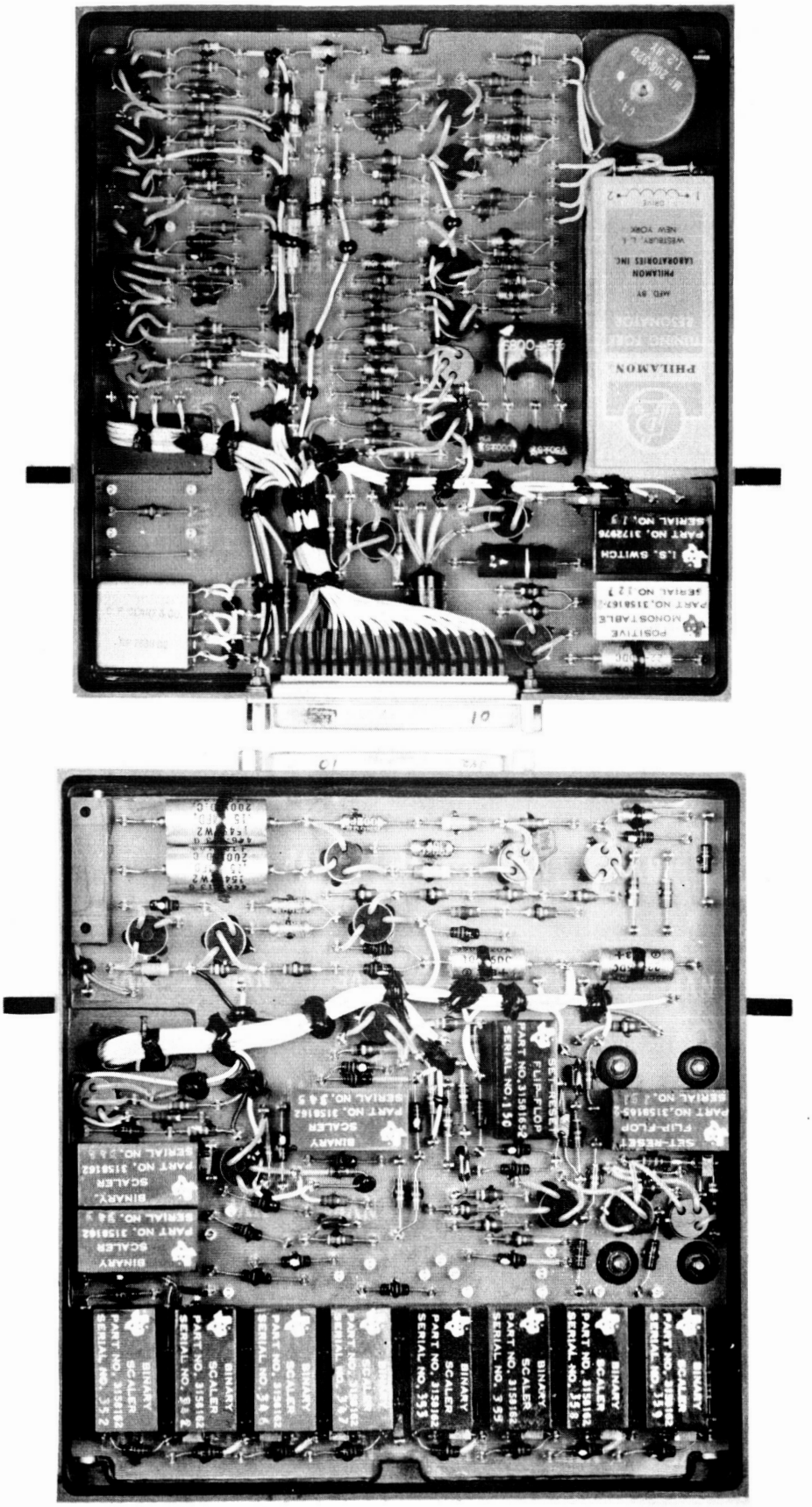


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Figure 1. Top and Bottom View of Digital Command Detector

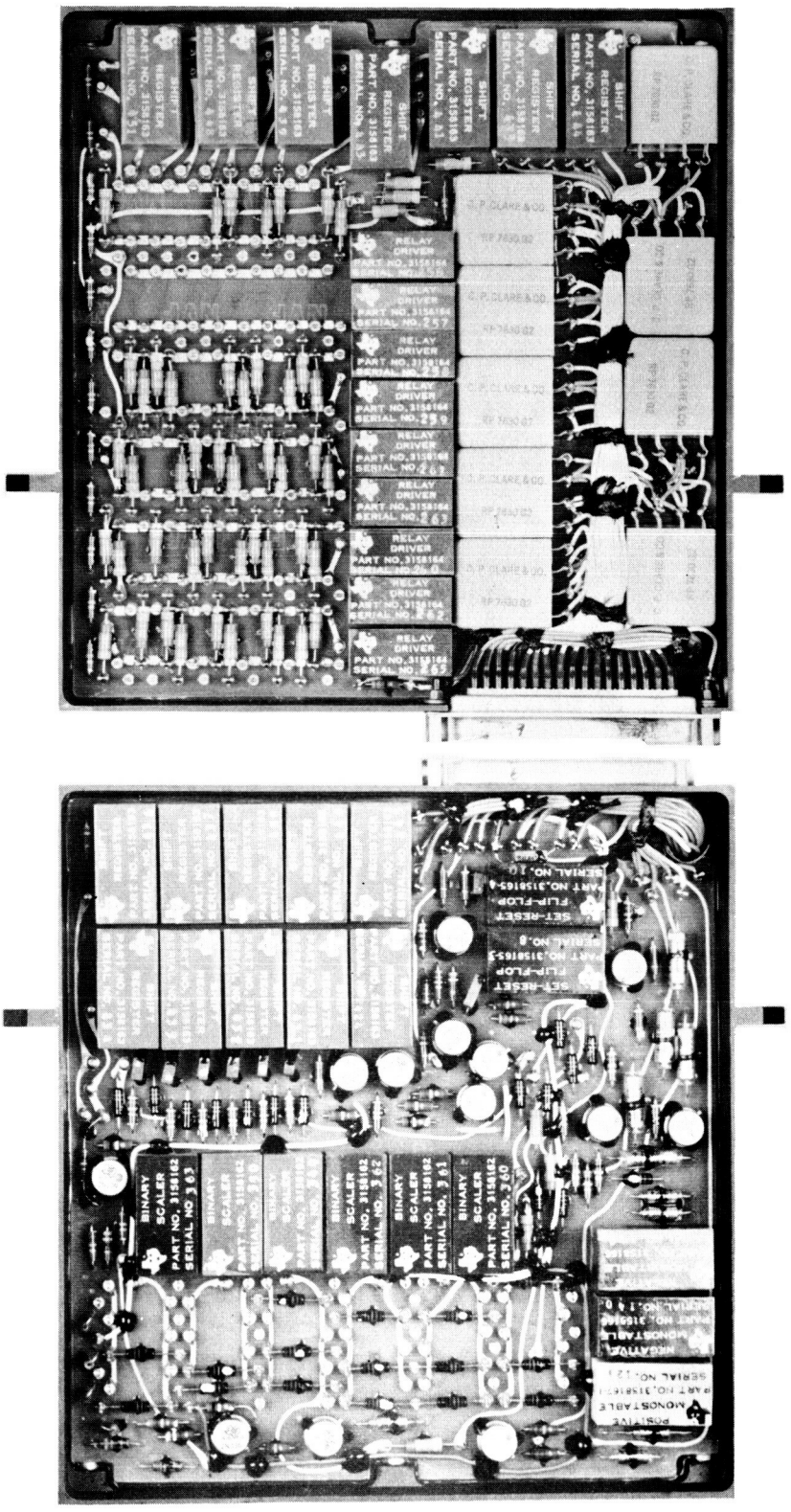


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Figure 2. Top and Bottom View of Digital Command Decoder

## SECTION II

## SYSTEM DESCRIPTION

The command detector and decoder are subsystems of the Ranger Block III Command System. This section describes both units, their functions, and basic theory of operation. The functional description of the two systems will be described separately.

### A. Command Detector System Logic

Figure 3 is a logic diagram of the command detector. The inputs are the FSK tone, AGC signal, 25 pps clock signal, the alert pulse drive and the RTC indication pulse. The detector outputs which go to the decoder are the command word, the dump signal, and the 1 pps sync pulse.

The alert pulse from the detector goes to the CC and S and the RTC indication to telemetry. The command subcarrier is frequency-shift-keyed. This FSK-modulated subcarrier is first passed through the input filter which has a bandwidth of 95 cycles and then through the limiter amplifier. The output of the limiter is received by a driver amplifier. Then the narrowband tuning fork filter receives the signal and further discriminates against any signals which are not precisely at the frequency of the ON tone of the modulated subcarrier. The OFF tone which is removed 30 cycles below the ON tone produces zero output (-25db) from the tuning fork filter.

When the modulated subcarrier is at the ON tone frequency, the output of the tuning fork filter is passed through an output amplifier and then converted to a dc voltage in the envelope detector. When the command subcarrier is at the OFF tone frequency, the filter output is negligible, and the output of the detector is zero. The dc signal from the envelope detector actuates a Schmitt trigger ($ST_1$) which generates ONE or ZERO bits going to the command word and gates ($A_5$).

The output of $ST_1$ is only one of three inputs to $A_5$. A second input is received from $ST_2$, which produces a ONE signal when the AGC voltage is greater than .8 volts at the input of $ST_2$. The output of flip-flop 2 ($F/F_2$) goes to $A_5$ and during normal operation of the logic it produces a ONE input. $ST_2$ and $F/F_2$ then must gate $A_5$ to allow the command word bits from $ST_2$ to be transmitted out of the command detector.

The digital logic of the command detector consists of a series of 11 binary scalers. The scalers count down from 25 pps clock signal to produce a 1 pps sync output and a reset pulse at the end of a 57 second count period.

The auxiliary clock is a free running multivibrator whose output is blocked by the input of the 25 pps sync pulse from the CC and S. The auxiliary clock output is enabled only if the 25 pps input from the CC and S fails open.

The alert pulse drive is taken from count 16 of the decoder and is used to toggle an IP switch. The output of the IP switch is then passed on to the CC and S.

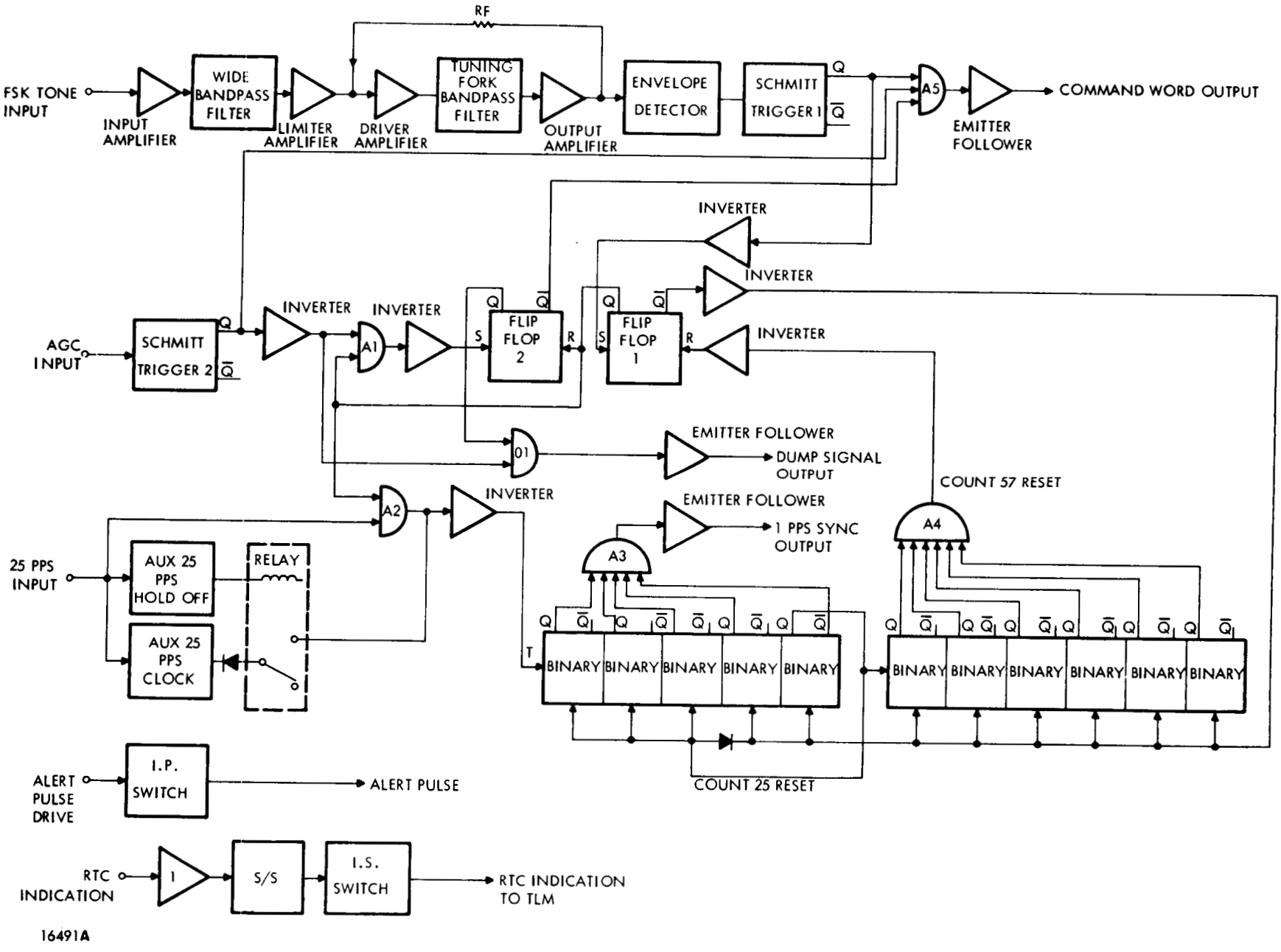


Figure 3. Logic Diagram - Command Detector

The RTC indication pulse is received from the decoder when a real time command relay is energized. The RTC indication pulse is passed through an inverter which toggles a single shot multivibrator. The single shot triggers an IS switch which sends an RTC indication pulse to telemetry. The normal sequence of events in the operation of the command detector are presented in the following paragraphs.

An AGC signal of .8 volts or more is applied to $ST_2$ causing it to produce a digital ONE which goes to $A_5$ as previously described.

A 25 pps clock signal through $A_2$ drives the binary scaler group to produce the sync and reset pulses. $A_2$ and the binary scalers do not begin to count until the first identification bit of a command word is received through the command detector. The first bit of the command word coming out of the detector at $ST_1$ triggers $F/F_1$ to the set condition.

The "set" $F/F_1$ gates $A_1$ so that the AGC signal from $ST_2$ will "set" $F/F_2$ in the event that the AGC signal should fail and $A_2$ so that the clock pulses can start the binary scalers on their counting sequence.

Since the first bit of the command word starts the counting sequence of the binary scaler, the sync output pulses are produced at a rate of one per second coincident with each bit of the command word.

Should the AGC signal drop below 18 volts at any time during the transmission of a command word, $ST_2$ switches and $F/F_2$ is placed in the "set" condition. OR gate (01) received signals from $F/F_2$ and $ST_2$, either of which generates the dump or "not ready" signal which goes to the command decoder indicating that the AGC has failed. Since $ST_2$ has changed state, and $F/F_2$ has gone into the "set" condition, both gating signals to $A_5$ have now become zero, thereby stopping any output of command word signals from the detector going to the decoder. To recapitulate, the loss of AGC produces a dump signal directly and stops the command word output.

The normal length of the command word in the Ranger system is 18 bits. At the end of the command word, the digital logic continues counting until the end of 57 seconds at which time the reset pulse occurs, causing $F/F_1$ to reset which shuts off the gating signal to $A_1$ and $A_2$. The binary digital chain remains at the point where it stopped counting at the end of 57 seconds and is not zero-zet. The identification bit of the next command word through the detector ($ST_1$) sets $F/F_1$, producing a signal to zero-set the digital chain and reset $F/F_2$. At the same time the output of $F/F_1$ operates and gates $A_1$ and $A_2$, starting another command word counting sequence. If AGC should fail between command words after $F/F_1$ is reset, a dump signal output would occur and $A_5$ would be gated off. No output from any received command word signal can occur from the detector as long as the AGC signal is below threshold level.

The use of frequency-shift subcarrier keying in this system improves the noise figure over that which might be expected using an ON-OFF keyed subcarrier. This is possible because a subcarrier is always present at the input and produces amplitude limiting at normal levels. The 95-cycle bandpass of the input filter improves the signal-to-noise ratio by limiting response to frequencies outside

of its response spectrum. A resistor network at the input of the bandpass filter allows adjustment of the limiting threshold of the detector to signals greater than 0.1 volt rms. The basic design of the detector channel is such that effective limiting begins at input levels on the order of 0.1 volt rms. Below this level, the filter and limiter amplifier combination performs as a linear device. Above this level, limiting begins to take place. The center frequency of the bandpass limiter is set midway between the two command subcarrier frequencies, that is, it is located 15 cycles below the frequency of the ON tone and 15 cycles above the frequency of the OFF tone. The narrowband filter which uses a Philamon tuning fork resonator is precisely set to the frequency of the ON tone and rejects signals at the OFF tone frequency with attenuation of better than 20 db. Frequency response of the narrowband filter is shown in Figure 4. The 3 db response of the narrowband filter is 2.5 cps.

B. Command Decoder System Logic

Figure 5 is a logic diagram of the command decoder. The command decoder has three inputs and five groups of outputs. The input signals are the 1 pps sync pulse, the dump signal and the command word (18 bit non-return-to-zero (NRZ) word). The outputs are the real time command, stored time command, alert pulse drive, RTC indication and telemetry. The system bit or pulse-rate-frequency (PRF) is one pulse per second.

The first command bit, a "1" bit, will set the program control flip-flop ($F/F_1$). This opens two gates, $A_1$ and $A_3$, allowing the binary scaler to count sync pulses ($P_1$), output of $S/S_1$, and the shift registers to shift and store the incoming command. A Schmitt trigger ($ST_1$) is used in the command word channel to condition the signal for storing in the memory (shift registers) circuits. Since the memory has a storage capacity of 17 bits and the command word is 18 bits, the first command bit is shifted out or lost.

Event sequences are determined by the program control matrix and the binary scaler. The address decode matrix decodes the address data block of the command word stored in shift registers $SR_1$ through $SR_5$. On the 19th sync pulse, a matrix supply voltage switch applies a voltage pulse, equal in duration to the sync pulse, to the address matrix for interrogating the command word. If the command word is a real time command, a real time command relay will operate for 150 milliseconds nominally. If the command word is a stored command, the enable flip-flop ($F/F_2$) will be set, enabling two gates, $A_4$ and $A_5$, to be opened. Gate $A_5$ allows the stored command relay to energize if a "1" is in the last memory circuit ($SR_1$). Gate $A_4$ allows the sample switch to be turned on when a sample pulse occurs. On stored commands, all 17 bits are transmitted to the stored command output. On the 36th count, a reset pulse is generated resetting the program control flip-flop and the enable readout flip-flop. At count 36 $\overline{Q}$ of $F/F_1$ is applied to AND Gate $A_7$. One hundred and sixty milliseconds later, single shot 3 ($S/S_3$) goes to the one level enabling AND Gate $A_7$ and is inverted and used to reset the counters.

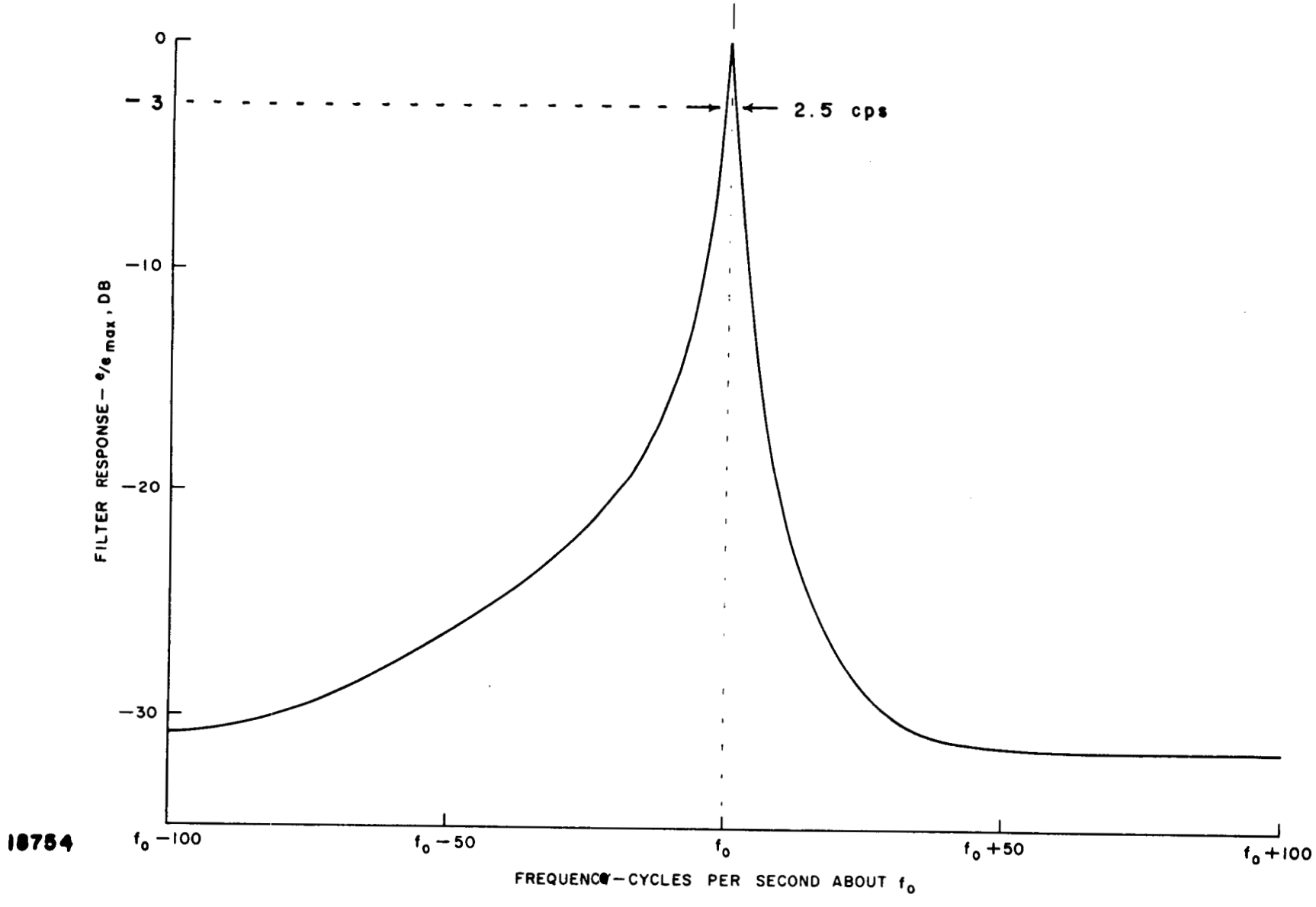


Figure 4. Narrowband Filter Response Characteristics

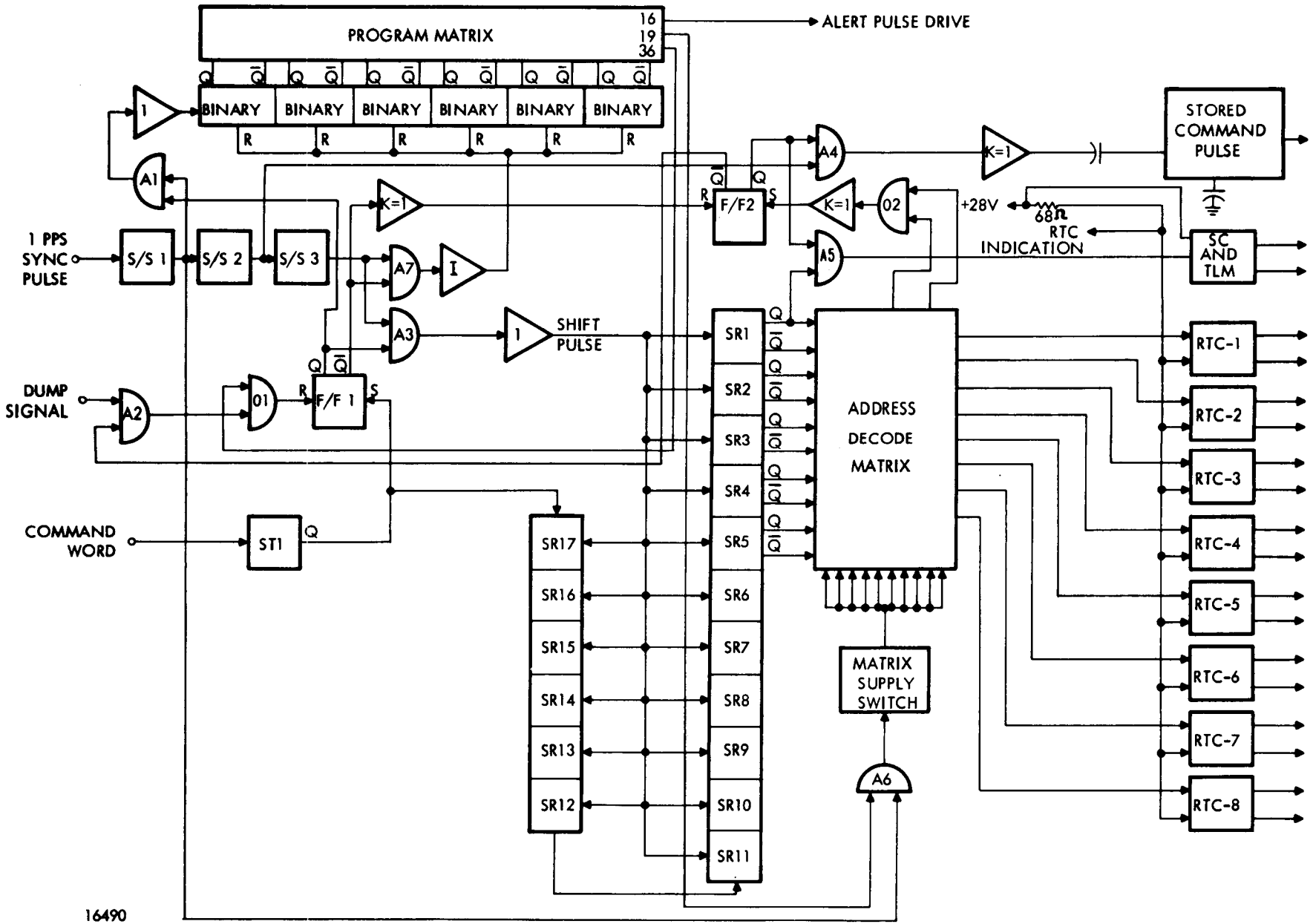


Figure 5. Logic Diagram - Command Decoder

The occurrence of a dump signal during a word transmission resets the command decoder the same as the reset pulse. However, should a dump signal occur after the 19th sync pulse, the dump signal is locked out of the decoder by closing AND Gate $A_2$. Thus, the correct word already stored in the shift registers will be retained and its command carried through. If a dump signal occurs, a "not ready" signal is generated by the telemetry flip-flop ($F/F_3$). The output of the telemetry flip-flop goes to telemetry equipment.

The alert pulse drive is taken from count 16 of the program matrix and passed on to the detector.

The RTC indication occurs every time a real time command relay is operated and this RTC indication is transmitted to telemetry via the detector.

Table I below shows command designation, command code and command description associated with the digital command decoder.

Table I. Command Decoder Designations

| Command Designations | Command Code (Address) | Command Description |
|---|---|---|
| Real Time Commands: | | |
| RTC-1 | 101010 | Roll Override |
| RTC-2 | 110100 | Antenna Hinge Angle Override |
| RTC-3 | 111010 | Antenna Switchover |
| RTC-4 | 110110 | Begin Midcourse Maneuver |
| RTC-5 | 110010 | (1) Telemetry Mode Change<br>(2) Upgrade TV Backup Clock |
| RTC-6 | 100101 | Begin Terminal Maneuver |
| RTC-7 | 101110 | (1) TV Warmup<br>(2) TV Emergency Telemetry<br>(3) Emergency Telemetry Turn-off<br>(4) Turns TV Off |
| RTC-8 | 101100 | (1) Sun Re-acquire<br>(2) Inhibit Motor Burn |

Table I. Command Decoder Designations (Continued)

| Command Designations | Command Code (Address) | Command Description |
|---|---|---|
| Stored Time Commands: | | |
| SC-1 | 110101 | Midcourse Roll Maneuver Duration |
| SC-2 | 111101 | Midcourse Pitch Maneuver Duration |
| SC-3 | 100011 | Midcourse Velocity Increment |
| SC-4 | 110011 | Terminal First Pitch Maneuver Duration |
| SC-5 | 101011 | Terminal Yaw Maneuver |
| SC-6 | 111011 | Terminal Second Pitch Maneuver Duration |

When a real time command is received a preselected relay is closed for 150 milliseconds nominally. The stored time command shifts the 17 digit word to the CC and S computer in the command system.

C. Block III System Changes

The purpose of this section is to show how the present Block III Ranger Command Subsystem differs from systems built previously for JPL by Texas Instruments. The following lists these differences.

1. An auxiliary 25 pulses per second clock and hold off circuitry was added to the detector to protect against CC and S clock failure.

2. RTC-8 was added in the decoder.

3. An IP switch was added to the detector to generate an alert pulse for CC and S.

4. A 68 ohm resistor was added in series with +28V common to all real time command relays in the decoder.

5. An inverter, monostable multivibrator, and IS switch was added in the detector to generate an indication to telemetry if a real time command relay closes.

6. Connector size on the detector was changed from a 25 pin connector to a 37 pin connector.

7. The detector chassis was reduced in width by 1/8 inch and the decoder casting was increased in width by 1/8 inch.

8. All logic diodes external to modules were changed from PS510B to FD126 as discussed in Section III.

9. Set-reset modules were redesigned which is also discussed in Section III.

10. Detector period of operation was changed from 56 to 57 seconds.

11. The reset circuitry of the program control flip-flop in the decoder was changed to eliminate a time race problem. See Section III.

12. Several components were respecified to optimize circuit performance.

13. The cordwood module height was increased to accommodate bending of leads within the module before soldering which produces better solder joints.

## SECTION III

## SYSTEM DIFFICULTIES

There have been several areas where technical difficulties have been encountered during the performance of this modification to the Ranger contract.

The first of these problem areas has been the high reject rate on 2N336 transistors and the low yield of transistors usable in modules. Because of the extremely wide beta range of the 2N336 and previous experience with the transistor in flip-flop modules, the transistors were matched to within 20 units and were selected from the low end of the beta range, 80 to 140. The transistor itself exhibited high reject rates because of beta drift and low beta. JPL requested that units with beta higher than 180 not be used.

The second problem area was encountered when the first decoder was assembled and tested. It exhibited an electrical failure that appeared to be a time race. To eliminate this race from the system the reset circuitry of the decoder was changed. Previously the program control flip-flop ($F/F_1$) was reset when the program counter reached count 36 and in turn reset the program counter to count 0, removing the reset pulse from $F/F_1$. To eliminate this problem the operating pulse $P_3$ used in the decoder was "ANDED" with the flip-flop output. This allowed approximately 160 milliseconds for the program control flip-flop to reset before the counter was reset and thus eliminated the time race.

During preacceptance testing of subsystem No. 2 a third problem area was found in the detector. When the AGC voltage was removed and then returned during a command cycle, $F/F_2$ was properly set to generate a dump signal but was improperly reset when the AGC signal was removed. After investigation it was determined that the cause of this failure was reverse current flowing in a PS510B diode used in an AND gate causing collector triggering.

Further investigation revealed that the reverse current was also the cause of the decoder failure. The original diode used in the command subsystem was a TI 1N645. Upon JPL's request the PS510B diode was substituted for the 1N645 in the last two decoders built for JPL on the Block II phase of the Ranger program. This diode according to published data was an electrical equivalent of the 1N645. Although the manufacturers specifications are equivalent for both the PS510B diode and the 1N645, it has been learned that the TI 1N645 device differs substantially when used as a logic element. Neither device is specified for this application. Both devices are specified for use as rectifiers. The PS510B diode is an alloy junction device while the TI 1N645 is a diffused junction device. The alloy junction inherently has a higher reverse recovery time than the diffused junction and in this case caused a multitude of problems in the logic circuitry.

To eliminate this problem the diode types were changed to FD126 in all logical areas external to modules and the set-reset flip-flops and dc set and reset inputs were redesigned.

A worst case circuit design review review revealed a fourth problem area. Several circuit drivers were found that under worst case conditions could have become degraded in operation. To alleviate the situation a minimum beta requirement was placed on these transistors and several resistor values were changed to increase dc overdrive.

## SECTION IV

## CONCLUSIONS AND RECOMMENDATIONS

The present system, although more than adequate for its mission, can be vastly improved through some relatively simple changes. This section will discuss the changes that Texas Instruments feels would be desirable to incorporate into future command subsystems of this type.

### A. 25 PPS Input Circuitry

With the present circuitry, if the CC and S output to the command subsystem fails in a short mode the system will fail. The output of AND gate $A_2$ will become clamped low and no clock pulse will be generated to the system (Figure 3).

If this circuitry is changed to that shown in Figure 6, there will be protection against both open and short failures at the input and the mechanical relay would be eliminated. The present CC and S detector would be modified and used to select AND gate $A_2$ as the added gate. These outputs would be resistivity OR'ed together to drive the present inverter.

### B. Tuning Fork Filter

The tuning fork filter presently used has a resistive feedback network from the output to the input. This resistor passes noise around the tuning fork filter from the input to the output. The best signal-to-noise ratio that can be expected from the system will be determined by the fixed tuning fork amplifier gain for the signal and the noise passed through and shunted around the filter by the feedback path. The magnitude of noise shunted around the filter is determined by the size of the feedback resistor and the output impedance of the amplifier. The signal-to-noise ratio of the system can be increased by changing the feedback from the present resistor to a unidirectional type network.

It should also be pointed out that the summing point for the input signal and the feedback is the output of the limiter amplifier. The output of the limiter amplifier does not present a constant value of impedance to the feedback and creates an unsymmetrical tuning fork filter drive. It is felt that if this circuit were redesigned a further improvement in the sign-to-noise ratio could be obtained.

### C. Detector Wideband Filter

The purpose of the wideband filter is to discriminate against noise outside of a 95 cycle pass band centered at $f_1$ -15 cps. The present filter has the proper characteristic at the pass band frequencies but as frequencies of the input are increased the filter gain approaches unity. This can be corrected by reversing the position of the inductor and input capacitor of the filter.

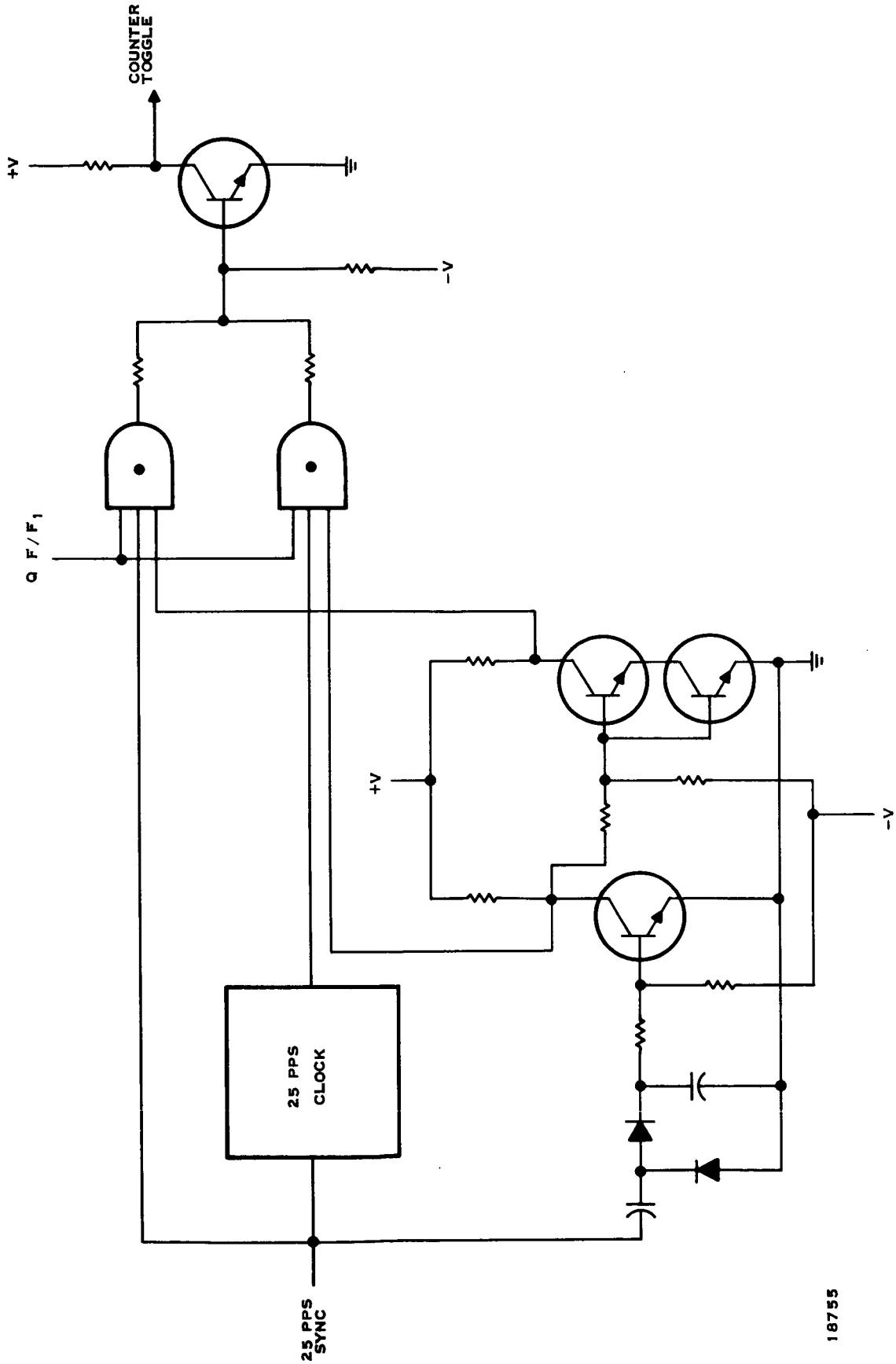


Figure 6. CC and S and Auxiliary Clock Circuitry

D. Single System

The present detector and decoder are built to operate as two separate units which results in a series of redundant operations. If the command system were repackaged as a single system, the series redundancy could be eliminated. This approach would require that all stored time commands be monitored through telemetry on the ground as is presently being done.

The areas where changes are recommended are listed as follows.

1. Elimination of 12 shift registers in the decoder which would require that all stored time commands be monitored from the ground as is now being done. It would also require address interrogation during the 7th rather than the 19th second as is presently the case.

2. Elimination of the program counter in the decoder. This can be accomplished by gating the required counts from the program counter in the detector.

3. Elimination of the monostable multivibrators in the decoder. This can be done by generating the operating pulses $P_1$, $P_2$, and $P_3$ from the counter which divides the 25 pps signal down to 1 pps.

4. Flip-Flop$_1$ in the decoder can be eliminated by using Q of $F/F_2$ in the detector to control the matrix supply switch. This also eliminates the necessity of the dump signal output circuitry in the detector.

5. The command word output emitter follower and AND gate $A_5$ can be eliminated from the detector and ST can be eliminated from the decoder. The controlling function of the gate, the Schmitt trigger, and the emitter follower functions were made unnecessary by the previous step.

If the changes recommended in steps 1 through 5 are incorporated there are several other areas which should be considered. A simplified block diagram incorporating the changes in steps 1 through 5 is shown in Figure 7.

6. Recode the command addresses in such a manner that it would require two bit errors to generate a false command.

7. Change the drive to the two isolation pulse switches to guarantee a positive turn-off. In the present method where the switch is allowed to decay off there is a period of time where the switch transistor is operating as an amplifier. This will amplify any noise present on the positive voltage source.

8. Standardize on a universal type flip-flop rather than use four different packages as is the present case. This will simplify production and thus reduce the cost.

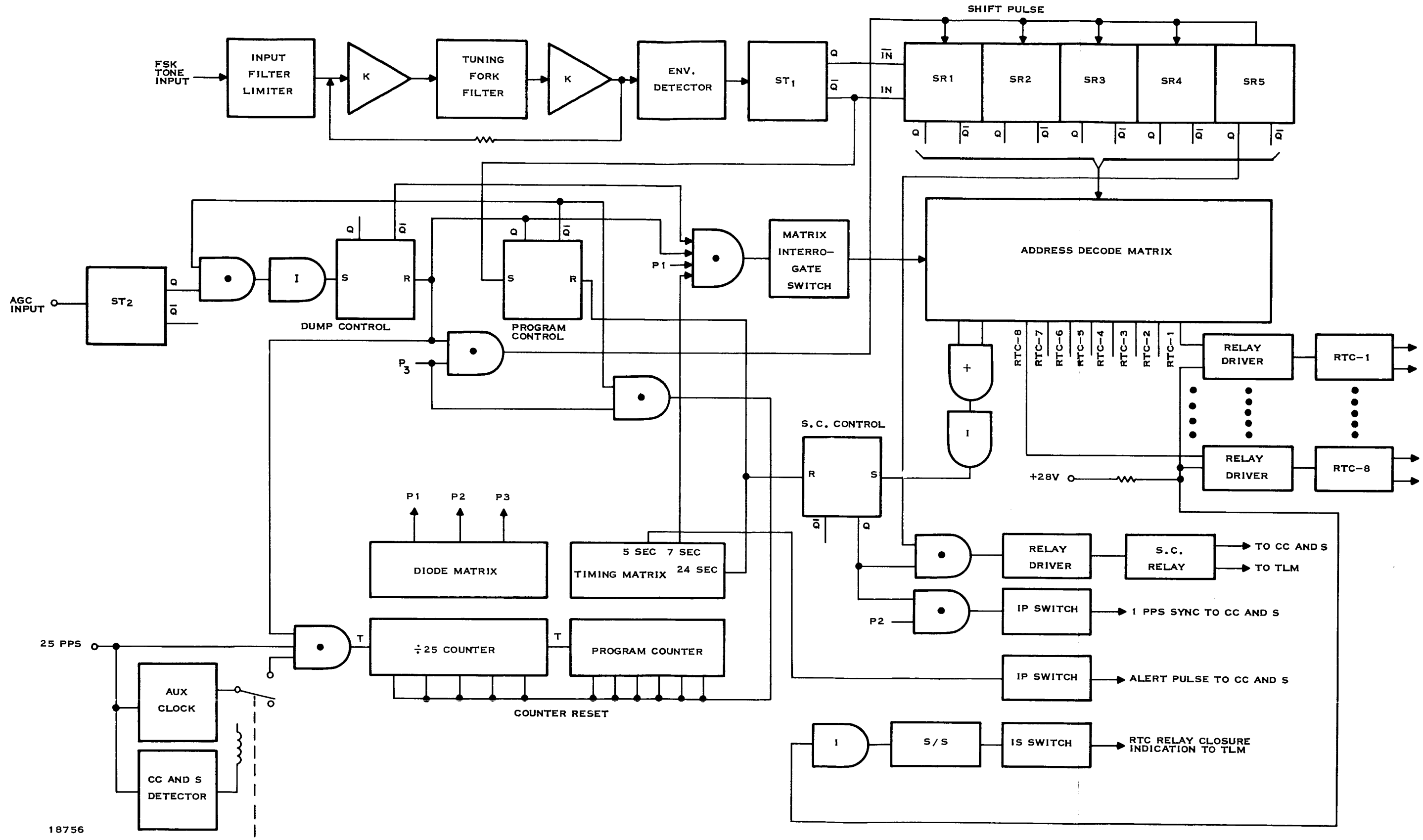


Figure 7. Simplified Command Subsystem

9. Incorporate a start command for the system so that any one bit error will not start system operation.

E. Packaging

The original packaging design approach on the command subsystem was aimed at achieving maximum component density. All trade-offs were made to this end. As a result the present system has an overall density of 50,000 components per cubic foot.

Since the original design effort was made there have been several new workmanship specifications placed on the contract. These specifications, which have grown out of further experience with both Mariner and Ranger spacecraft, are aimed at assemblies averaging 25,000 components per cubic foot. In order to apply these specifications to the command package many exceptions and deletions have been made. The result of this has been a reduction in the effectiveness of the specifications and confusion in their application. This in turn has generated certain inefficiencies in the manufacturing process.

**For future programs it is recommended that the command package be redesigned in line with the applicable workmanship specifications.**

TCMonroe

T. C. MONROE
Project Engineer
Space Systems

TCM:jb

# APPENDIX A

# DIGITAL COMMAND DETECTOR AND DECODER
# TEST PROCEDURES
# AND
# DATA SHEET

| DASH NO. | | |
|---|---|---|
| QTY | | |
| NEXT ASSY NO. | 229 | |
| SIZE | | |
| PROJ NO. | | |

438991 A

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM | ZONE | DESCRIPTION | DATE | APPROVED |
| C | | CN76038(c) BMoran, 6-19-63; (1) REDRAWN PER REDESIGN; (2) ADDED SHEET 4 | 6-19-63 | H. Miller |

# INSPECTION TEST PROCEDURE
# PART I
# INDIVIDUAL TEST
# FOR
# RANGER BLOCK III
# DIGITAL COMMAND DECODER

TEST DATA SHEET 438992 TO BE FILLED OUT AS PART OF THIS TEST PROCEDURE.

| -2 QTY REQD | -1 QTY REQD | ITEM NO. | DWG SIZE | TEXAS INSTRUMENTS PART OR IDENTIFYING NO. | GOVT OR INDUSTRY PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION |
|---|---|---|---|---|---|---|

LIST OF MATERIALS

| | | DATE |
|---|---|---|
| DR | Don Clifton | 6/18/63 |
| CKD | H. Miller M | 6-19-63 |
| ENGR | D. Douglas | 6-18-63 |
| APPD | | |

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

TITLE

TEST PROCEDURE, INSPECTION
PART I
INDIVIDUAL TEST, RANGER BLOCK III
DIGITAL COMMAND DECODER

| DESIGN ACTIVITY RELEASE | | CODE IDENT NO. | SIZE | DRAWING NO. |
|---|---|---|---|---|
| K. McLeod | 6-19-63 | 96214 | A | 438991 |
| | | SCALE NONE | WT | SHEET 1 of 4 |

TI-1E1793-A

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| 1. | TABLE OF TESTS | Paragraph No. |
| 1.1 | Power Consumption | 3.1 |
| 1.2 | Signals | 3.2 |

2. LIST OF TEST EQUIPMENT

2.1 Data Sheets (TI Drawing 438992 ) shall be completed as a part of this test.

2.2 Verify that test equipment designated WORKING STANDARD, or better, is currently certified per TI Standard Procedure No. 12-28.

2.3 Commercial Test Equipment - The following commercially available test equipment (or equivalent) is required to complete the test required by this specification.

2.3.1 **Tektronix 543 Scope - Used for measuring pulse widths and heights.**

2.3.2 **HP410B Voltmeter - Used for measuring voltages having a one second or greater duration.**

2.4 Special Test Equipment - The following special test equipment is required to complete the test required by this specification.

2.4.1 Digital Command Decoder Checkout Instrument (JPL Part No. 3349138). Operation of the checkout instrument is given in TI Report No. 3-60305-3, "Ranger III Digital Command Decoder and Checkout Instrument."

3. TEST PROCEDURE

3.1 Power Consumption

a. Read and record percent current drain on -6V d-c power supply.

b. Read and record percent current drain on +6V d-c power supply.

c. Read and record percent current drain on +12V d-c power supply.

d. Read and record percent current drain on +28V d-c power supply.

3.2 Signals

NOTE: Pulses $P_1$, $P_2$ and $P_3$ refer to the outputs of the positive monostable multivibrator A1 module, the negative monostable multivibrator A4 module, and the negative monostable multivibrator A6 module, respectively. These points can be located in the Decoder system by using Jet Propulsion Laboratory Drawings 3158183 and 3158173. The test points indicated in parenthesis are located on the front panel of the checkout instrument described in Section 2.4.1.

a. Read and record the amplitude and duration of pulse $P_1$.

b. Read and record the amplitude and duration of pulse P2.

c. Read and record the amplitude and duration of pulse $P_3$.

d. Read and record the minimum and maximum amplitude of $\overline{Q}$ of $F/F_1$. (TP1)

e. Read and record the minimum and maximum amplitude of $\overline{Q}$ of $F/F_2$. (TP2)

f. Read and record the minimum and maximum output of the command word Schmitt Trigger. (TP3)

g. Read and record the amplitude and duration amplitude of the CC&S shift pulse. (TP4)

h. Read and record the matrix voltage supply switch amplitude and duration. (TP5)

i. Read and record with reference to +28V the amplitude and duration of the RTC current measurement. (TP6)

j. Read and record the minimum voltage and duration of the sample pulse. (TP7)

k. Read and record the amplitude of the command word pulse train at which the decoder will operate without error. (TP9)

l. Read and record the minimum amplitude of the sync pulse at which the decoder will operate without error. (TP10)

m. Read and record the minimum value of the dump signal which will reset $F/F_1$. Monitor $F/F_1$ at $TP_1$. Monitor the dump signal at TP11.

n. Set the command word level and the sync pulse to 2 volts. After each stored command has been set into the checkout instrument, the checkout instrument should be set to automatic. Each command should recycle at least 5 times.

o. Set up the checkout instrument as in step (n) and repeat for each real time command.

p. Read and record the amplitude and duration of the count 16 pulse. (TP8)

| DASH NO. | | |
|---|---|---|
| QTY | | |
| NEXT ASSY NO. | 229 | |
| SIZE | | |
| PROJ NO. | | |

438992

A

## REVISIONS

| SYM | ZONE | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|---|
| E | | CN75996 (C) B. Moon, 6-19-63; (1) REDRAWN PER REDESIGN | 6-19-63 | H. Miller |
| F | | CN99600 (C) D. Clifton, 6-27-63 (1) SECTION 3.2, SECTION d 2.4V (4 - 6V) WAS: 2 3.2V (3.2V - 6V) (2) SECTION 3.2, SECTION f (-0.5 - +0.4V) WAS: (-0.5 - 0.4V) (3) SECTION 3.2, SECTION i -2.0V MINIMUM WAS: -8V MINIMUM (4) SECTION 3.2, SECTION 1. 2.2V WAS: 2V | 6-27-63 | W. Marchand |

INSPECTION TEST DATA SHEET
PART I
INDIVIDUAL TEST
FOR
RANGER BLOCK III
DIGITAL COMMAND DECODER

THIS DATA SHEET TO BE FILLED OUT AS PART OF TI TEST PROCEDURE 438991 .

| -2 QTY REQD | -1 QTY REQD | ITEM NO. | DWG SIZE | TEXAS INSTRUMENTS PART OR IDENTIFYING NO. | GOVT OR INDUSTRY PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION |
|---|---|---|---|---|---|---|

LIST OF MATERIALS

| | | |
|---|---|---|
| DR Dan Clifton | DATE 6/18/63 | TEXAS INSTRUMENTS INCORPORATED APPARATUS DIVISION DALLAS, TEXAS |
| CKD H. Miller M | 6-19-63 | |
| ENGR D. Haydon | 6-18-63 | TITLE: DATA SHEET, INSPECTION TEST, PART I, INDIVIDUAL TEST, RANGER BLOCK III DIGITAL COMMAND DECODER |
| APPD | | |
| DESIGN ACTIVITY RELEASE L. M. McLeod | 6-19-63 | |

| CODE IDENT NO. | SIZE | DRAWING NO. |
|---|---|---|
| 96214 | A | 438992 |
| SCALE NONE | WT | SHEET 1 of 3 |

TI-1E1793-A

Texas Instruments Incorporated, Apparatus Division

Drawing No. 438992

Page 1 of 2

Component Serial No. _____

Manufacturing Sequence No. _____

Part No. _____

Contract No. _____

# INSPECTION TEST DATA SHEET
# PART I INDIVIDUAL TEST
# RANGER BLOCK III
# DIGITAL COMMAND DECODER

NOTES:

A. This test data sheet to be filled out as a part of TI Procedure 438991. The paragraph numbering corresponds to that of the procedure.

B. Record actual readings at 25°C only in space provided unless otherwise specified.

| | | | +25°C | -10°C | +75°C |
|---|---|---|---|---|---|
| 3.1 | **Power Consumption** | | | | |
| | a. **-6VDC** | **≤100% (20 ma)** | 68% | | |
| | b. +6VDC | ≤100% (200 ma) | 37% | | |
| | c. +12VDC | ≤100% (1 ma) | 20% | | |
| | d. +28VDC | ≤100% (60 ma) | 0% | | |
| 3.2 | Signals | | | | |
| | a. $P_1$ | ≥3.5V (3.5 - 5V) | 3.7 | | |
| | | 150 ms ±33% (100-200 ms) | 168 | | |
| | b. $P_2$ | ≥3.5V (3.5 - 5V) | 3.6 | | |
| | | 10 ms ±50% (5-15 ms) | 13.2 | | |
| | c. $P_3$ | ≥3.5V (3.5 - 5V) | 3.7 | | |
| | | 30 ms ±33% (20-40 ms) | 29.5 | | |
| | d. $F/F_1$ $\overline{Q}$ | ≤0.4V (0 - 0.4V) | .15 | | |
| | | ≥4V (4V - 6V) | 4.2 | | |
| | e. $F/F_2$ $\overline{Q}$ | ≤0.4V (0 - 0.4V) | .25 | | |
| | | ≥4V ( 3 - 6V) | 4.2 | | |
| | f. Schmitt Trigger | ≤0.4V, ≥-0.5V (-0.5-+0.4V) | -.28 | | |
| | | ≥4V (4 - 6V) | .6 | | |
| | g. Shift pulse | ≥4V (4 - 6V) | 4.2 | | |
| | | 30 ms ±50% (20-40 ms) | 28.5 | | |
| | h. Matrix supply pulse | ≥5V (5 - 6V) | 5.3 | | |
| | | 150 ms ±33% (100-200 ms) | 164 | | |

| TEXAS INSTRUMENTS INCORPORATED APPARATUS DIVISION. DALLAS. TEXAS | CODE IDENT NO. | SIZE | DRAWING NO. |
|---|---|---|---|
| SYM F E | 96214 | A | 438992 |
| | SCALE | WT | SHEET 2 |

TI-IE1793-1-A

Drawing No. 438992



| | | | +25°C | -10°C | +75°C |
|---|---|---|---|---|---|
| i. | RTC current | 150 ± 50 msec.<br>-2.0V minimum | 166<br>-2.6 | | |
| j. | Sample pulse | ≤0.2V (0 - 0.2V)<br>10 ms ±50% (5-15 ms) | 0<br>10.6 | | |
| k. | Command Word (minimum amplitude) | Between 1 and 2V | 1.6 | | |
| l. | Sync Pulse (minimum amplitude) | Between 1 and 2.2V | 1.6 | | |
| m. | Dump Signal (minimum value) | Between 0.5 and 2V | 1.2 | | |
| n. | **Stored Time Command Test** | **Correct word check and display** | | | |
| | SC-1 (110101) | | x | | |
| | SC-2 (111101) | | x | | |
| | SC-3 (100011) | | x | | |
| | SC-4 (110011) | | x | | |
| | SC-5 (101011) | | x | | |
| | SC-6 (111011) | | x | | |
| o. | Real Time Command Test | Lamp Indication and word check | | | |
| | RTC-1 (101010) | | x | | |
| | RTC-2 (110100) | | x | | |
| | RTC-3 (111010) | | x | | |
| | RTC-4 (110110) | | x | | |
| | RTC-5 (110010) | | x | | |
| | RTC-6 (100101) | | x | | |
| | RTC-7 (101110) | | x | | |
| | RTC-8 (101100) | | x | | |
| p. | Count 16 | ≥ 3.5V | 4.0 | | |

Time of completion _____

Total Operating time _____

This system conforms to the requirements of TI Individual Test Procedure 438991.

Tested by _____ Date _____

| TEXAS INSTRUMENTS INCORPORATED APPARATUS DIVISION. DALLAS. TEXAS | CODE IDENT NO. | SIZE | DRAWING NO. |
|---|---|---|---|
| SYM F E | 96214 | A | 438992 |
| | SCALE | WT | SHEET 3 |

TI-1E1793-1-A

| DASH NO. | QTY | NEXT ASSY NO. | SIZE | PROJ NO. |
|---|---|---|---|---|
| -1 | 1 | 315825-04 | D | 229 |

439970

A

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM | ZONE | DESCRIPTION | DATE | APPROVED |
| A | | CN99586(C), Dan Clifton, 9-13-63<br>(1) REDRAWN WITH CHANGE<br>(2) CLASSIFICATION CANCELLED BY AUTHORITY OF JIM TAYLOR | 9-16-63 | |

# INSPECTION TEST PROCEDURE
# PART I
# INDIVIDUAL TEST
# FOR
# RANGER BLOCK III
# DIGITAL COMMAND DETECTOR
# SUBSYSTEM

TEST DATA SHEET 439971 TO BE FILLED OUT AS PART OF THIS TEST PROCEDURE.

| -2 QTY REQD | -1 QTY REQD | ITEM NO. | DWG SIZE | TEXAS INSTRUMENTS PART OR IDENTIFYING NO. | GOVT OR INDUSTRY PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION |
|---|---|---|---|---|---|---|

LIST OF MATERIALS

| | | |
|---|---|---|
| DR Dan Clifton | DATE 9-13-63 | TEXAS INSTRUMENTS INCORPORATED<br>APPARATUS DIVISION DALLAS, TEXAS |
| CKD M | 9-16-63 | |
| ENGR | | TITLE: TEST PROCEDURE, INSPECTION, PART I, INDIVIDUAL TEST, RANGER BLOCK III DIGITAL COMMAND DETECTOR SUBSYSTEM |
| APPD | | |
| DESIGN ACTIVITY RELEASE K. M. McLeod | 9-16-63 | CODE IDENT NO. 96214 / SIZE A / DRAWING NO. 439970 |
| | | SCALE NONE / WT / SHEET 1 of 9 |

TI-1E1793-A

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| 1.2 | Bandpass Limiter | 3.2 |
| 1.2.1 | Center Frequency and Bandpass | 3.2.2 |
| 1.2.2 | Limiter Action | 3.2.3 |
| 1.3 | Tuning Fork Filter | 3.3 |
| 1.3.1 | Center Frequency and Bandpass | 3.3.2 |
| 1.3.2 | Off-Frequency Response | 3.3.3 |
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2. LIST OF TEST EQUIPMENT

2.1 Data Sheets (TI Drawing 439971) shall be completed as a part of this test.

2.2. Verify that test equipment designated WORKING STANDARD, or better, is currently certified per TI Std. Procedure No. 12-28.

2.3 Ranger Command Detector Checkout Instrument

2.4 Commercial Test Equipment - The following commercially available test equipment (or equivalent) is required to complete the test required by this specification.

2.4.1 Audio Oscillator - General Radio Oscillator, Type 1302-A or equivalent.

2.4.2 A-C Voltmeter - Hewlett-Packard Model 400D or equivalent.

2.4.3 D-C Voltmeter - Hewlett-Packard Model 410B or equivalent.

2.4.4 Random Noise Generator - General Radio Model 1309A.

2.4.5 Electronic Counter - Hewlett-Packard Model 523B or equivalent.

3. TEST PROCEDURE

3.1 Power Consumption

With the Command Detector connected by test cable to the checkout instrument, energize both equipments and check the power consumption of the detector. Record the percent current drain on each of the three d-c supplies; +28V, +6V, and -6V.

3.2 Bandpass of Wide Band Filter and Limiter

3.2.1 Preparation

a. Disable the internal oscillator by moving the "OSCILLATOR" switch inside the checkout instrument to the off position. Place the "INTERNAL EXTERNAL" Oscillator switch on the front panel to external position.

b. Monitor the oscillator input voltage at TP13. Set the H.P. Oscillator output voltage to 50 mv rms. Maintain this input level while measurint the bandpass of the filter-limiter circuit. Monitor the frequency with the electronic counter. If the output as defined in step c is distorted reduce the 50 mv until a sine wave appears at Q4.

3.2.2 Center Frequency and Bandpass

a. Adjust the oscillator to the frequency near $f_c$ which produces the maximum response at the collector of $Q_4$ and record the rms voltage. Read and record the frequencies above and below $f_c$ where the output is 3 db below the maximum output level.

b. Calculate the center frequency as the average of the two 3 db frequencies and record.

c. Obtain the bandpass of the filter as the difference of the two 3 db frequencies. The bandpass should be 95 $\pm$ 5 cps.

d. Record the output of $Q_4$ at $f_o$ and $f_1$. The output should not be less than -.8 dbs. from the maximum output level.

3.2.3 Limiter Action

Record the outputs at TP1 for input levels at TP13 of 0.05, 0.1, 0.2, 0.5, and 1.0 volts rms at the given frequencies.

3.3 Tuning Fork Filter

3.3.1 Preparation

a. The external oscillator shall be set to a level of 1.0 V rms measured at TP13. The internal oscillator shall remain disabled as in section 3.2.

3.3.2 Center Frequency and Bandpass

a. Adjust the oscillator to the frequency which produces the maximum rms voltage at the base of Q13 on detector board A1. Record this voltage. Read and record the dc voltage at TP2 and the frequency $f_1$ of the external oscillator to the nearest tenth of a cycle per second.

b. Read and record the frequencies above and below $f_1$ where the output at the base of Q13 is down 3 dbs. Obtain the bandpass as the difference of the 3 db frequencies and record. The bandpass should be 2.5 $\pm$ .2 cps.

3.3.3 Off-Frequency Response

a. Increase the oscillator input level to 1.4 volts rms (TP13). Record the filter amplifier output (rms volts) at the base of Q13 on Board A-1 and the detector output (dc volts) at TP-2, for frequencies of $f_1 \pm 10$ cps.

b. Increase the oscillator input level to 2.80 volts rms (TP-13). Record the filter amplifier output (rms volts at the base of Q13) and the detector output (dc volts at TP-2) for frequencies of $f_1 \pm 20$ cps.

c. The maximum limit of the envelope detector output in a and b is less than the threshold level of ST-1 measured in Section 3.4.6.a.

3.4 System Operation

3.4.1 Preparation

Set the checkout instrument to operate in the normal manual mode. Adjust the on tone level to 1 volt rms at TP-13.

3.4.2 Sync Pulse

a. Measure the amplitude of the sync pulse at TP-11.

b. Measure the rise time (Tr) of the sync pulse.

c. Measure the duration of the sync pulse.

3.4.3 Command Word Pulse

a. Measure the dc voltage level of the command word pulse for both the "1" and "0" states at E-57.

b. Measure the rise time of the leading edge of the command word pulse.

3.4.4 $ST_1$ Activation Time

a. Using the oscilloscope measure the time required for $ST_1$ to turn on. This time is measured from the beginning of the on and off keying of the subcarrier with a 1.0V rms input level at TP-13. Connect the sync input (+) to TP-14 and the vertical input to TP-3.

b. Using the oscilloscope as above measure the time required for $ST_1$ to turn off. Sync input should be set for a negative (-) trigger.

3.4.5 Command Word Interval

Using an electronic counter measure the command word interval. Connect the START input (-) of the counter to TP-4. Set the STOP input to (+) and the mode switch to the "common" position.

3.4.6 Threshold Levels

a. The setup for the checkout instrument is the same as for paragraph 3.2.1.a except that the frequency of the oscillator is $f_1$. Vary the input voltage and record the detector output voltage (TP-2) which causes $ST_1$ (TP-3) to turn full on. Record the voltage at TP-3.

Reduce the oscillator input voltage and record the detector output voltage which causes $ST_1$ to turn full off. Record the voltage at TP-3.

b. Monitor the collector voltage of $ST_2$ (TP-5), while varying the AGC voltage control on the checkout instrument. Record the voltage level at terminal E58 on Board A-1 which causes $ST_2$ to turn on. Record the collector voltage at TP-5. Reduce the AGC voltage and record the voltage level at E58 which causes $ST_2$ to turn off. Record the collector voltage at TP-5.

3.4.7 Inhibit Operation

Set the checkout instrument to the normal manual mode of operation. Record the dump signal (E2 on Board A-2) and $F/F_2$ (TP-6) dc voltage levels under the following conditions.

a. Start the cycle with the AGC voltage greater than the threshold level.

b. Start the cycle with the AGC voltage greater than the threshold level and reduce the voltage below threshold within the 1st 18 seconds. Record the dc levels of $F/F_2$ and dump signal before the 56th second.

c. Start the cycle with the AGC voltage above the threshold level. Reduce AGC voltage to zero and then increase its value above the threshold before the 1st 18 seconds. Record the dc levels of $F/F_2$ and the dump signal before the 56th second.

d. Start the cycle with the AGC voltage below the threshold value, let the checkout instrument complete the cycle and record the dump signal and $F/F_2$ voltage levels after the 56th second with AGC on after 56 seconds.

e. Between words when no commoand signals are being transmitted read and record the output voltages of $F/F_2$ and the dump signal with AGC on and with AGC off.

3.5 Alert Pulse

3.5.1 Preparation

The alert pulse circuitry is driven by the clock pulse source in the detector checkout instrument. The control over the input to this circuitry is with the 25 pps amplitude control on the front panel.

3.5.2 Circuit Operation

a. Read and record the maximum and minimum level of the alert pulse at TP-24 with a 4 volt peak input monitored at TP-12.

b. Read and record the alert pulse width at TP-24.

c. Read and record the minimum clock pulse level which will operate this circuit.

c . Record the minimum amplitude of the 25 pps at TP-12 which causes the circuit to operate correctly (1 ± .5).

3.6 Auxiliary Clock Test

3.6.1 Preparation

The SYNC PULSE switch on the front panel of the checkout panel shall be put in the off position.

3.6.2 Auxiliary Clock Test

a. Monitor the time period of the auxiliary clock. Read and record this value. It can be found at TP-20 on the detector checkout instrument. This time period will read 40 ± .4 milliseconds. If the reading falls out of specification adjust the variable resistor until the frequency is correct.

b. Monitor the clock pulse at A2-E3. Record that the 25 pps is present at this point.

3.7 RTC Closure Indication Circuitry

3.7.1 Preparation

Apply a negative going .5 pps to TP-21. This will be with reference to +28V which is on TP-17.

3.7.2 Circuit Operation

a. Starting at zero, increase the magnitude of the 1 pps pulse until the step switch operates. Monitor the step switch at TP-22 with respect to ground. Read and record the magnitude of the 1 pps pulse.

b. Read and record the on level and pulse width of the isolation step switch output.

| DASH NO. | | |
|---|---|---|
| QTY | | |
| NEXT ASSY NO. | | |
| SIZE | | |
| PROJ NO. | | |

A

| REVISIONS | | | | |
|---|---|---|---|---|
| SYM | ZONE | DESCRIPTION | DATE | APPROVED |
| | | | | |

INSPECTION TEST DATA SHEET
(PREACCEPTANCE)

PART I

INDIVIDUAL TEST

FOR

RANGER BLOCK III

DIGITAL COMMAND DETECTOR
SUBSYSTEM

THIS DATA SHEET IS CLASSIFIED

THIS DATA SHEET TO BE FILLED OUT AS PART OF TI TEST PROCEDURE 439970

| -2 | -1 | ITEM NO. | DWG SIZE | TEXAS INSTRUMENTS | GOVT OR INDUSTRY | NOMENCLATURE OR DESCRIPTION |
|---|---|---|---|---|---|---|
| QTY REQD | | | | PART OR IDENTIFYING NO. | | |

LIST OF MATERIALS

| DR | DATE |
|---|---|
| CKD | |
| ENGR | |
| APPD | |
| | |
| DESIGN ACTIVITY RELEASE | |
| | |

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

TITLE

DATA SHEET, INSPECTION TEST
PART I, INDIVIDUAL TEST,
RANGER BLOCK III
DIGITAL COMMAND DETECTOR SUBSYSTEM

| CODE IDENT NO. | SIZE | DRAWING NO. |
|---|---|---|
| 96214 | A | 439971 |
| SCALE | WT | SHEET |

TI 1E1793-A

APPENDIX B

DETECTOR AND DECODER
DRAWING LIST

# DETECTOR DRAWING LIST

| Size | Drawing No. | Changed | Title |
|---|---|---|---|
| B | 3158150 | | PCB Bottom Binary Scaler |
| B | 3158151 | | PCB Top Binary Scaler |
| B | 3158156 | | PCB Top Set-Reset f/f |
| B | 3158157 | | PCB Bottom Set-Reset f/f |
| C | 3158162 | | Binary Scaler Module |
| C | 3158165 | | Set-Reset flip-flop Module |
| B | 3158178 | | Binary Scaler Schematic |
| B | 3158181 | | Set-Reset flip-flop Schematic |
| D | 3158250 | X | Digital Command Detector Subassembly |
| D | 3158254 | | Terminal Board 2, Digital Command Detector |
| D | 3158255 | X | Circuit Board 2, Digital Command Detector |
| D | 3158256 | X | Terminal Board 1, Digital Command Detector |
| D | 3158257 | X | Circuit Board 1, Digital Command Detector |
| J | 3158258 | X | Digital Command Detector Schematic |
| B | 3158259 | X | Wiring List, Point-to-point, Digital Command Detector |
| C | 3158260 | X | Marking Digital Command Detector Subassembly |
| D | 3158262 | X | Chassis, Digital Command Detector |
| B | 3172974 | New | PCB, Bottom, IS Switch |
| B | 3172975 | New | PCB, Top, IS Switch |
| C | 3172976 | New | IS Switch Module |
| B | 3172977 | New | IS Switch Schematic |
| C | 3172980 | New | IS Switch Shield |
| C | 3172981 | New | IS Switch Assembly |
| C | 3172978 | X | Front Panel No. 2 |

## DECODER DRAWING LIST

| Size | Drawing No. | Changed | Title |
|---|---|---|---|
| B | 3158150 | | PCB Bottom Binary Scaler |
| B | 3158151 | | PCB Top Binary Scaler |
| B | 3158152 | | PCB Bottom Neg Monostable |
| B | 3158153 | | PCB Top Neg Monostable |
| B | 3158154 | | PCB Bottom Pos Monostable |
| B | 3158155 | | PCB Top Pos Monostable |
| B | 3158156 | | PCB Top Set-Reset f/f |
| B | 3158157 | | PCB Bottom Set-Reset f/f |
| B | 3158158 | | PCB Bottom Shift Register |
| B | 3158159 | | PCB Top Shift Register |
| B | 3158160 | | PCB Bottom Relay Driver |
| B | 3158161 | | PCB Top Relay Driver |
| C | 3158162 | | Binary Scaler Module |
| C | 3158163 | | Shift Register Module |
| C | 3158164 | | Relay Driver Module |
| C | 3158165 | | Set-Reset f/f Module |
| C | 3158166 | | Monostable Multivibrator (-) Module |
| C | 3158167 | X | Monostable Multivibrator (+) Module |
| D | 3158169 | X | Subchassis, Decoder, Assembly |
| D | 3158171 | X | Digital Command Decoder Subassembly |
| J | 3158172 | | Terminal Board 1, Decoder |
| D | 3158173 | | Circuit Board 1, Decoder |
| J | 3158174 | X | Terminal Board 2, Decoder |

DECODER DRAWING LIST (CONTINUED)

| Size | Drawing No. | Changed | Title |
|---|---|---|---|
| J | 3158175 | X | Circuit Board 2, Decoder |
| B | 3158176 | X | Monostable Multivibrator (+) Schematic |
| B | 3158177 | | Shift Register Schematic |
| B | 3158178 | | Binary Scaler Schematic |
| B | 3158180 | | Monostable Multivibrator (-) Schematic |
| B | 3158181 | | Set-Reset f/f Schematic |
| B | 3158182 | X | Relay Driver Schematic |
| J | 3158183 | X | Digital Command Decoder Schematic |
| C | 3158184 | X | Insulation Sheet, Electrical, No. 1 |
| C | 3158185 | X | Insulation Sheet, Electrical, No. 2 |
| C | 3158186 | X | Digital Command Decoder Marking |
| B | 3158187 | | Wiring List, Digital Command Decoder |