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SUMMARY REPORT

TO

JET PROPULSION LABORATORY

PASADENA, CALIFORNIA

DESIGN, CONSTRUCTION, AND TESTING OF LOW INPUT VOLTAGE CONVERTERS

(2.5-volt and 0.6-volt)

Under Contract No. 951041

23 March 1965

Honeywell

ORDNANCE

A DIVISION OF THE

MILITARY PRODUCTS GROUP

TO

JET PROPULSION LABORATORY

PASADENA, CALIFORNIA

A SUMMARY REPORT

ON

CONTRACT NO. 951041

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(2.5-Volt and 0.6-Volt)

23 March 1965

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I. PURPOSE

The purpose of this contract (Contract No. 951041) was to build two Low Input Voltage Converters for use with direct energy conversion devices. In order to evaluate the trade-off necessary to establish the desirability of utilizing a single large capacity direct energy converter, in preference to several in series, has resulted in this program to develop two models: one to operate at 0.6 volt, and one to operate at 2.5 volts.

The program was aimed at minimizing the volume and weight as much as possible and still retain the high efficiencies which have been achieved by past models.

II. SUMMARY

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During the present program, two Low Input Voltage Converters were designed, constructed, and tested. They were designed to have the lowest weight and volume commensurate with the efficiency specifications. Both units met the efficiency specification and both units made significant reductions in weight and volume. The 2. 5-volt unit is approximately one quarter of the specifications limits for weight and volume. The 0. 6-volt system utilizes a new coaxial design and is one-half the weight and one-third of the volume specified as maximum. See Figures 1 and 2 for illustrative photos of the 2. 5 - volt unit and the 0. 6 - volt system, respectively.

Author I

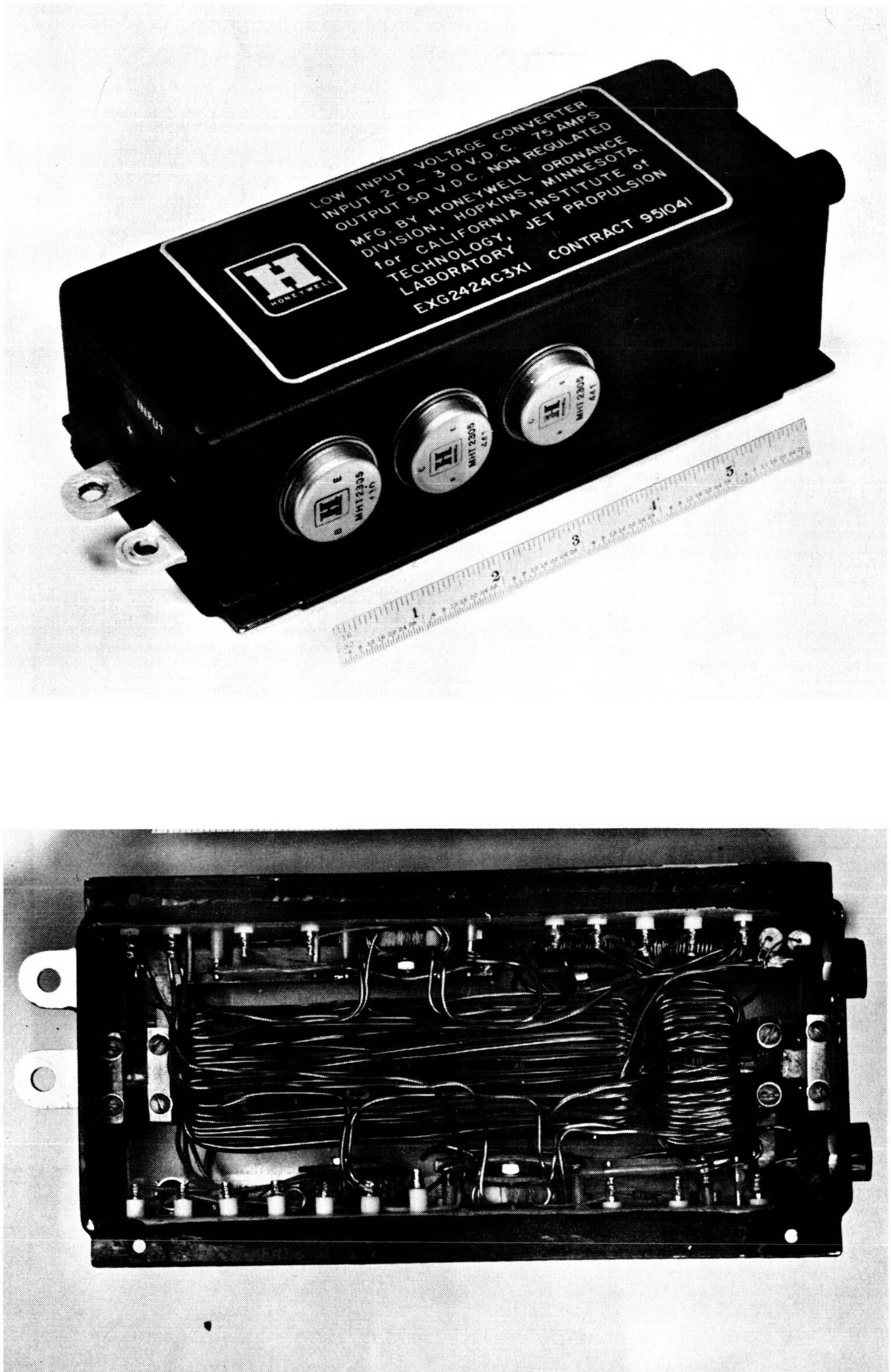

Figure 1 - (a) ASSEMBLED, (b) OPEN VIEW; 2.5-VOLT LIV CONVERTER

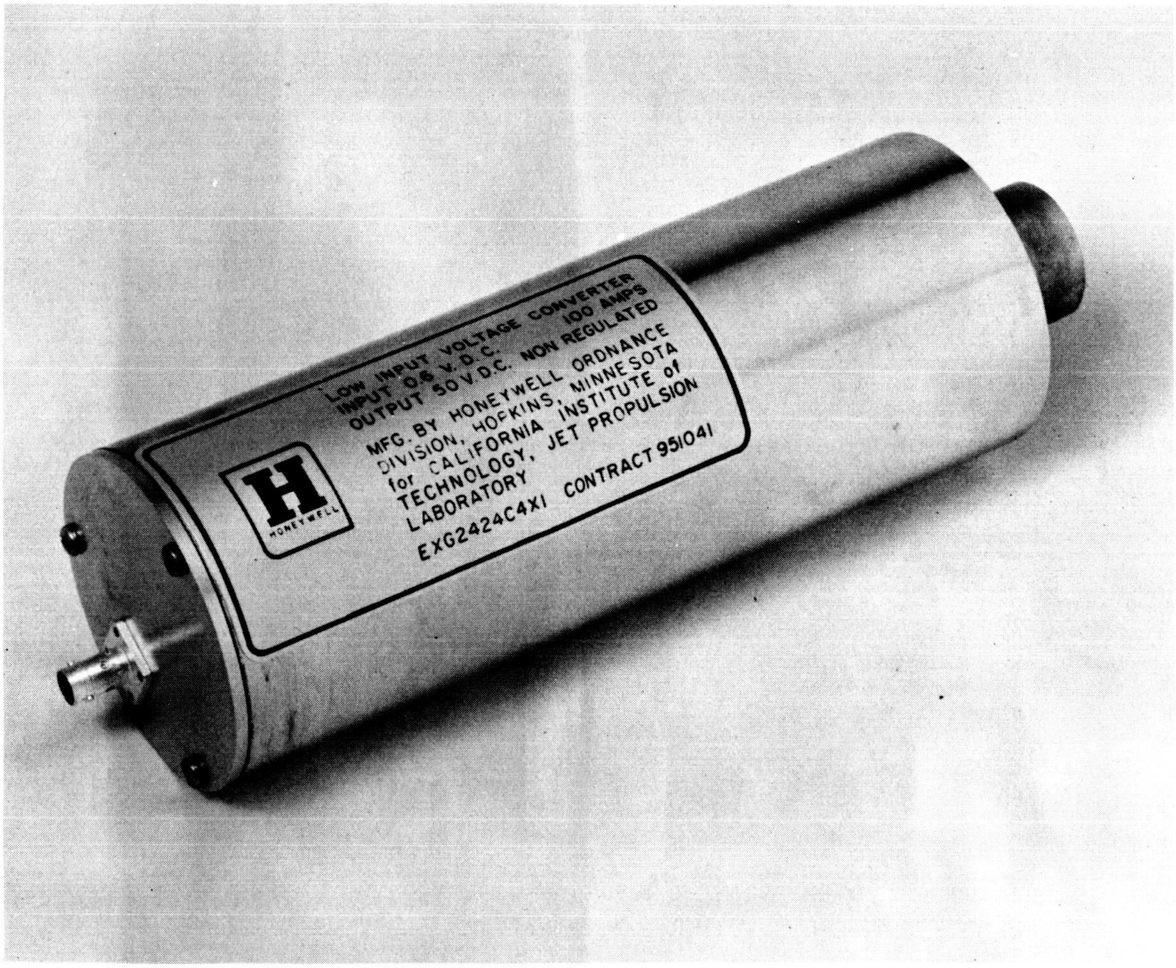

Figure 2 - 0.6-VOLT COAXIAL LIV CONVERTER

III. PROJECT DETAILS

This project supported the design and fabrication of two quite similar units during the same time interval using the same basic general philosophies. Therefore, it is most convenient to discuss the project details first in a general manner which applies to both systems, and then specifically for each of the two systems, so that each of the differences can be properly recorded.

A. GENERAL

The basic concept for Low Input Voltage Converters is shown in Figure 3. Utilizing an input filter to help absorb the switching transients so they do not reflect back to the line, the power is simultaneously applied to the power oscillator and the starting circuit. The starting circuit is necessary to guarantee proper starting of the oscillator at all temperatures and all load conditions. When the power oscillator is in operation, the starting circuit is disabled so it does not draw power.

An auxilliary frequency control circuit is utilized to maintain frequency control and, thus, high efficiency of the power oscillator. The power is then fed to the rectifier, output filter, and load. The output power is sensed and is utilized for helping achieve high switching speeds in the transistor. This is done by the pulse transformer that takes its input from the rectifier and feeds back a signal to control the power oscillator.

B. DETAILED DESCRIPTION OF OPERATION

1. Blocking Oscillator Starting Circuit

The blocking oscillator starting circuit (Figure 4) is used only to start the converter. When the converter is operating, a bias voltage supplied by winding N4 on the power output transformer (T1) turns the blocking oscillator off. The

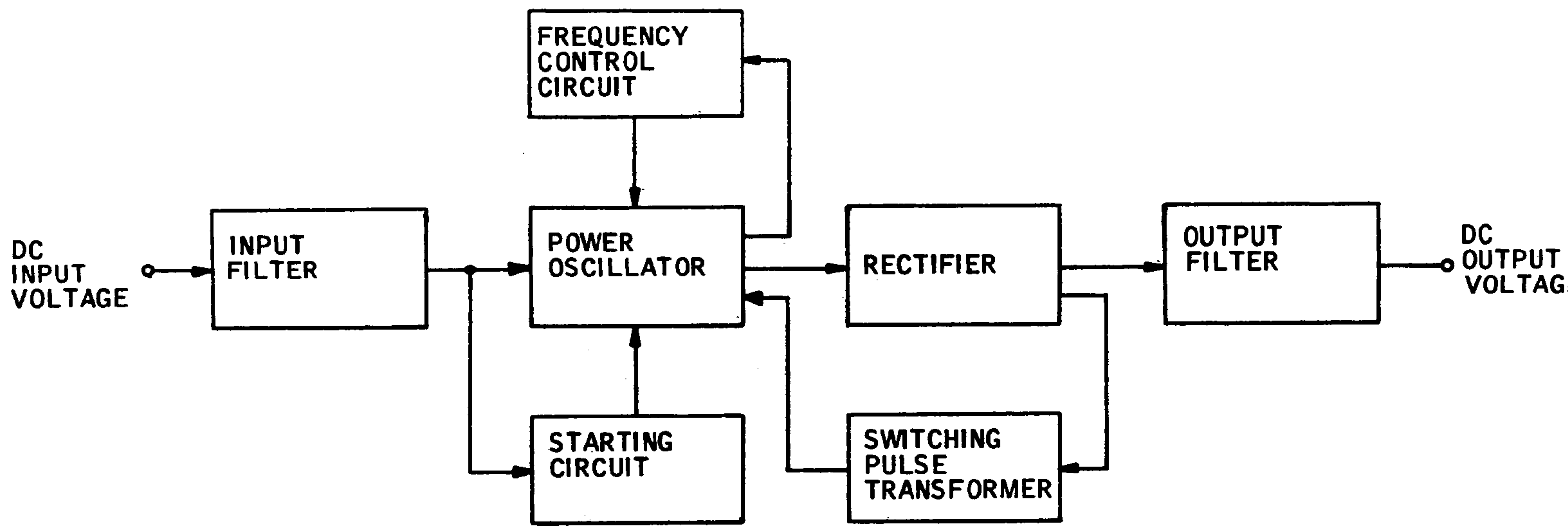

Figure 3 - LIV CONVERTER BLOCK DIAGRAM

blocking oscillator is turned off to avoid the introduction of transients during converter operation and to minimize power dissipation in the circuit. However, a current path exists (through the bias circuit) from the positive input lead, through winding N4 and rectifying diodes CR 3-4 and through R1 back to the negative input which results in power dissipation. This power dissipation can be minimized by diminishing the turns of N4 and/or maximizing the resistance of R1. The minimum number of turns of N4 is determined by the minimum bias voltage necessary to maintain transistor Q3 off. The maximum allowable resistance of R1 is limited by its effects on the starting characteristics of the blocking oscillator.

The capacitor (C2) charging current passes directly through the transistor (Q3) base, and the energy stored in the pulse transformer, while the transistor is on, is used to start the converter when the transistor is off. When the input voltage is greater than the emitter to base turn-on voltage of transistor Q3, a base current will be established. This base current will initially include the charging current of C2 as well as that current flowing through resistor R1 back to the negative input lead. Thus, a collector current flowing through winding N3 will be established with the capacitor charging current providing base drive and also initially aiding collector current flow through transformer action between N2 and N3. The increasing collector current induces a voltage in N2 which regeneratively increases the capacitor charging base current, and transistor Q3 saturates. When the transistor turns off, the energy stored in the transformer core is coupled to the power oscillator through diode CR5. Although the blocking oscillator starts as soon as the input voltage is sufficient to turn on Q3, there is not enough energy stored to turn the converter on until the input voltage reaches the level previously indicated. The operation described above provides reliable converter starting at low input voltages. This circuit configuration makes it possible to reduce the power loss in the starting blocking oscillator to an insignificant value when the converter is operating.

2. Power Oscillator

The basic power oscillator consists of transistors Q1 and Q2, transformers T1 and T2, and inductor L1. Transformers T4 and T5, together with inductor L2, were added to the basic circuit to improve the switching characteristics and will be discussed separately. The starting circuit induces a pulse of current flowing from emitter to base of transistor Q1, which in turn increased the collector current of this transistor. A parallel path exists through winding N1 of current feedback transformer T2 which induces a voltage across N2 tending to bias transistor Q2 further into cut-off. The resultant decrease in collector leakage current of Q2 aids the starting of the power oscillator. The increasing collector current in winding N3 of T2 induces a voltage back into the base winding tending to turn Q1 on harder. Transistor Q1 is driven into saturation and the first cycle of the oscillator is initiated.

When the power oscillator starts, a voltage is developed across winding N4 of output transformer T1, rectified by diodes CR3-4, and applied to the blocking oscillator transistor Q3, turning if off. Thus the blocking oscillator stops consuming power after it has performed its function. If, for any reasons, the power oscillator stops while input voltage is still applied, the blocking oscillator resumes oscillation and attempts to restart the power oscillator.

3. Frequency Control Circuit

The switching of the power oscillator is controlled by choke L1. When the power oscillator switches, the voltage induced in winding N3 of transformer T1 reverses and current starts to flow from N3 through L1 and winding N5 of transformer T2. The initial current through L1 is very small until the core of L1 saturates. At this time, the current increases sharply, developing a voltage in winding N5 of feedback transformer T2. This voltage opposes the feedback voltage produced by the current in the collectors of the power oscillator transistors in the conducting side, turning the conducting side "off" and the other side "on". The core of the current feedback transformer does not saturate during the time interval required to saturate the core of choke L1, so the core loss of T2 is kept low. The frequency depends upon the voltage induced in N3 of transformer T1, so it is not constant but depends on input voltage and load.

4. Switching Enhancement Circuit

Investigations have resulted in circuit improvements which reduced the switching losses substantially and increased the over-all efficiency. This improved switching enables operation at higher frequencies and results in a substantial weight reduction in the LIV converters. Improved switching characteristics have been obtained by back biasing the "switching off" oscillator transistor to a higher voltage during the switching interval. This effectively diminishes the transistor storage time. Higher back bias is now being accomplished by the use of small transformers which effectively decouple the "switching off" transistor base from the feedback transformer for a short period during the switching interval. These reactive components consume very little power and, hence, accomplish rapid switching with high efficiency.

The power oscillator circuit is analyzed in detail as follows: Assuming transistor Q2 is conducting, current flows from the positive line through primary winding NIB (T1) winding N4 (T2), the emitter collector junction of Q2, and then back to the negative line. Current flow through winding N4 (T2) energizes the core of T2 and this induces drive current in winding N2 (T2). Positive feedback of Q2 is provided by transformed T2 winding N2 through decoupling transformer T5 winding N2 to the base-emitter junction of Q2. Back bias to Q1 is provided by winding N1 (T2) through decoupling transformer T4 winding N2 to the base-emitter junction of Q3. An additional back bias current path is provided by the resetting of choke coil L2 during the switching interval.

Transformers T4 and T5 respectively are utilized to decouple the "switching off" transistor for a short period of time during the switching interval. This decoupling enables one to back bias the transistor during turning off to a voltage which is higher than that supplied through the transformer T2. The voltage of transformer T2 is clamped to approximately 0. 55 volt by the forward emitter-base voltage of the transistor which is conducting. The application of the higher back bias voltages reduces the storage time and fall time of the transistor by sweeping the stored carriers out of the base region more rapidly. This, therefore, makes it possible to reduce oscillator switching time, thereby minimizing the associated switching losses.

5. Cycle of Operation

Following the circuit response through one-half cycle, first assume transistor Q2 to be conducting and to be midway through its conducting cycle (no switching transients present). Winding N4(T2) is then serving as the drive winding for current feedback transformer T2. Assuming that the voltage across N2 winding on T5 is zero, the volts per turn on transformer T2 is being determined by the forward emitter-base voltage of Q2 and N2 (T2). The volts per turn established by N2 reflects as a back bias voltage to Q1 through winding N1 (T2).

The voltage across N2(T5) previously assumed to be zero is approximately zero because the product of the Q2 base current and turns N2 is cancelled by nearly equal opposing ampere turns in winding N1(T5). Output current from T1 secondary (N2) forces the opposing current through winding N1 (T5). Transformer T5 is so designed that the ampere turns in winding N1 are greater than or equal to the ampere turns in N2. Therefore, if absolute cancellation is not realized, the diode clamp across winding N4 (T5) will limit the volts per turn induced to a very small value. This results in essentially zero volts across winding N2. When transistor Q2 is switched ON, the T1 secondary current flowing through winding N3 (T4) will induce a high back bias voltage in winding N2 (T4) because the impedance of the back biased transistor (Q1) is high. Thus, the voltage per turn in T4 will be high and this transformer will saturate shortly after the switching interval because the voltage time integral of T4 is small. Thus, transformers T4 and T5 do not affect the circuit operation when it is in the quiescient non-switching portion of the cycle.

The switching interval is initiated when switching reactor L1 saturates. This results in the application of negative feedback power to T2 through winding N5. This causes the rate of change of flux in the core to reverse. The voltage induced in winding N2 reverses and thereby provides a back bias voltage on Q2 and a forward bias voltage on Q1 through N1. When this occurs, Q2 starts to switch off and Q1 starts to switch on. Because inter-base inductor L2 tends to maintain constant current, it reverses its voltage and resets. The energy stored in L2 maintains a current which flows out of the inductor toward the common connection of the base of Q2 and N2 (T5), and into the inductor from the common connection of the base of Q2 and N2 (T5), and into the inductor from the common connection of the base of Q1 and N2 (T4). Winding N2 (T5) presents a considerable impedance to the current pulse and effectively blocks current flow. This causes instantaneous decoupling of winding N2 (T2). This allows the base of Q2 to be back biased to a higher voltage by the resetting of L2. In addition, when secondary current from T1 begins to flow due to the conduction of Q1, the decoupling realized is increased. This is accomplished as the T1 secondary current begins to flow through windings N1 (T4) and N3 (T5). The ampere turns generated in N1 (T5) results in an induced voltage which aids that caused by the resetting of L2 and provides a high back bias voltage to Q2. This effectively sweeps out the stored carriers much more rapidly, resulting in considerably decreased transistor turn off time. It is significant to note that prior to switching, the T5 core had a small induced voltage (clamped to N4) which reset its core during the previous half cycle. Since the core had been previously reset, a high impedance was presented to the switching current during the initial portion of the next half cycle.

Considering the transistor (Q1 for this interval) turning on, it is obvious the incorporation of the decoupling transformers (T4 for this interval) also tend to aid transistor turn on. As stated previously, when the transistors begin to switch, the energy stored in L2 maintains a current which flows into L2 from the common connection of the base Q1 and N2 (T4) when Q2 was conducting. This resets the T4 core so that it will oppose the flow of inductor current during the switching interval. Since the inductor current is now maintained through the base of Q1 this applies more forward bias to transistor (Q1). The maintenance of inductor current through the base emitter junction of Q1 turns it on rapidly. This turn-on is also aided by the drive current induced in winding N1 (T2) flowing through the emitter-base junction of Q1 and completing its path through N2 (T4). The initiation of T1 secondary current also aids the turn on of transistor Q1 because it flows through winding N1 (T4) and induces aiding drive current in N2 (T4). Thus, the forward drive applied to the Q1 base emitter junction is the sum of drive current provided by the reactor L2, the pulse transformer winding N2 (T4), and the feedback transformer winding N1 (T2).

Hence, both turn-on and turn-off are aided by the incorporation of decoupling transformers T4 and T5. With the switching interval completed, Q1 is now conducting and Q2 is turned off. Winding N3 (T2) is now serving as the drive winding for current feedback transformer T2. The voltage per turn on transformer T2 is determined by the forward emitter-base voltage of Q1 and N1 (T2). Similar to a previous assumption, one now assumes the voltage induced in T4 is approximately zero due to the cancellation of the amp-turns in N2 (T4) and N1 (T4). Transformer T5 quickly saturates due to the high voltage impressed by T1 secondary current flowing in N3 (T5). Thus, once again, it is shown that the decoupling transformers T4 and T5 do not affect circuit operation except during switching intervals.

A similar circuit response is characteristic when Q2 switches on and Q1 switches off.

6. Advantages of This Circuitry

Of prime importance to successful circuit operation is the fact that the transformers T4 and T5 are reset by the secondary T1 current each respective half cycle and therefore do not subtract from the reset applied to T2 on each half cycle. This also assures sufficient decoupling due to these transformers. It is also significant that this circuit concept "accounts" for changes in input voltage and current. As stated previously, it is desired that the ampere-turns due to secondary T1 current should be cancelled by the ampere-turns due to base drive current in the transformer connected to the conducting transistor. For a specific set of turns ratios, this is accomplished over the input voltage and current range as the base drive current and secondary T1 currents are both directly dependent on input current and, therefore, track each other over the input voltage and output load range. This is extremely important when considering the input voltage characteristics of the energy sources normally associated with low input voltage converters.

It can be seen that the above arrangement removes the clamp effect of the forward emitter base junction of the conducting transistor from the back biased transistor. Pulse transformers T4 and T5 effectively decouple the back biased transistor from the feedback circuit during the initial portion of the switching interval. In doing so, these pulse transformers provide a higher back bias voltage to the switching off transistors, and this sweeps the stored carriers out of the base region swiftly to accomplish more rapid switching of the power oscillator. A winding N4 and a zener diode clamp CR6 or CR7 is provided on each pulse transformer T4 or T5 so that the forward drive voltage applied by T4 or T5 to the conducting transistor will be limited to a relatively low value. The main forward drive power will then be supplied by transformer T2 through either windings N1 or N2. It is necessary to have T2 provide the main feedback power during the major portion of the cycle in order to maintain the normal induced voltage in the T2 windings. This winding induced voltage is necessary to maintain the off transistor properly back biased during the quiescient portion of the cycle after the pulse transformer saturates.

Oscillator switching is provided by negative feedback from output transformer T1 winding N3 through a saturating reactor L1 and a winding N5 on the current feedback transformer T2. This arrangement controls the power oscillator operating frequency proportional to input voltage so that the power transformers are operated at a nearly constant flux density over the input voltage range. Reactor L1 normally blocks the flow of negative feedback due to a high reactance. However, after a time interval, it will saturate and the negative feedback from T1 will be applied to the feedback transformer T2 winding N5 and it will override the inherent positive feedback and cause the circuit to recycle. During this switching interval, pulse transformers T4 and T5 will accomplish the desired decoupling between the power oscillator transistors and will rapidly back bias the switching "OFF" transistor to a high voltage. This will guarantee rapid switching of the oscillator. Also during this interval, the choke coil L2 will be reset; force additional back bias current into the base of the switching off transistors; and at the same time, it will provide additional forward drive for the switching "ON" transistor.

C. DETAIL DESIGN, 2.5-VOLT CONVERTER (See Figure 4)

1. Feedback Transformer

In the design of the current feedback transformer, the following assumptions were made:

1) Use "Permalloy" as the core material.

2) Design on the basis of a converter frequency of 1KC.

3) Limit the flux density to 25,000 lines per square inch.

4) Three MHT 2305 transistors operating in parallel will be used for transistors Q1 and Q2.

5) Drive these transistors to a forced current gain of 28.

$$\frac{N_1}{N_3} = \frac{N_2}{N_4} = 28$$

6) Assume a base emitter voltage of 0.55 volt at the 75 ampere input current condition.

7) The windings carrying the heavy currents (N3 & N4) will consist of a single turn.

Because the voltage across the transformer is a square wave, the expression $A_c = \frac{V \times 10^8}{4 N f B}$ is used to calculate the necessary core area.

$$A_c = \frac{0.55 \times 10^8}{4 \times 28 \times 10^3 \times 25 \times 10^3} = .0196 \text{ in}^2$$

The toroidal cores chosen for this transformer have an outside diameter of 1.375", an inside diameter of 1.000", and a height of 0.25". With a total input current of 75 amperes and a forced current gain of 28, the base current is 2.68 amperes.

Assuming a current density of 1 ma/cir mil #16 wire would be satisfactory for windings N1 & N2, but because the mechanical factors allowed a larger size wire and it was desirable to reduce the copper losses #14 wire was actually used.

2. Power Transformer

The design of the power transformer was based on the following assumptions and decisions:

1) Using a toroidal core employing "Deltamax" as the core material.

2) Limiting the flux density to 50,000 lines per square in., thereby maintaining a low value of core loss watts per pound.

3) Assuming an operating frequency of 1 KC.

4) Using a core that will allow a single turn primary.

5) Assume a total primary IR drop, exclusive of transistors, of 5 mv at the 75-amp input condition.

6) Assume an average transistor saturation voltage of 45 mv.

From these assumptions and design guides, the necessary core was determined as follows:

$$Ac = \frac{V_{N1} \times 10^8}{4\, N1\, f\, B}$$

$$V_{N1} = V_{in} - [\, V_{CE}(SAT) + \text{IR drop}\,]$$

$$V_{N1} = 2.5 - [\, .045 + .005\,] = 2.45 \text{ volts}$$

$$A_c = \frac{2.45 \times 10^8}{4 \times 1 \times 10^3 \times 50 \times 10^3} = 1.22 \text{ in}^2$$

Four cores were used for this transformer and each core had an outside diameter of 1.34", an inside diameter of .665" a height of 1.135", and a gross core area of 0.5 inch. Three cores were initially used but subsequent testing showed that four were needed in order to meet the efficiency requirements.

The number of turns necessary to obtain the desired output of 50 Vdc at the 2.5-volt, 75-amp input condition was determined as follows:

Primary losses = 0.05 volt (from previous assumptions)

Feedback transformer drop = 0.2 volt

$V_p = 2.5 - 0.07 = 2.43$ volts

Diode voltage drop = 0.7 volt

Secondary IR drop assumed to be 0.1 volt

$Vs = 50 + .7 + .1 = 50.8$ volts

$$Ns = Vs \frac{Np}{Vp} = 50.8 \frac{1}{2.43} = 20.9, \text{used 21 turns}$$

3. Switching Reactor

In order to initiate switching from one transistor to the other, the switching reactor must pass enough current on saturation to reduce the circuit gain to less than unity. To accomplish this a winding of 20 turns (N5T2) was placed on the current feedback transformer and a winding of 2 turns (N3T1) was added to the output transformer.

The voltage induced in the feedback transformer winding is the same as was calculated for the 0.6-volt unit and is 0.393 volts. (See page 26 for calculation)

The voltage induced in the power transformer winding is calculated as follows:

$$V_{N3} = N_3 \frac{V_{N1}}{N_1}$$

$$\frac{V_{N1}}{N_1} = 2.43 \text{ volts} \quad \text{(from previous calculations)}$$

$$V_{N3} = 2 \times 2.43 = 4.86 \text{ volts}$$

The voltage across L1 is then equal to the sum of these two voltages since the windings are connected series aiding.

$$V_{L1} = 4.86 + 0.393 = 5.253 \text{ volts}$$

The necessary reactor NA product was then calculated on the basis of using "Deltamax" as the core material with a saturating flux density of 100,000 lines per square inch.

$$NA = (V/4fB) \times 10^8$$

$$NA = (5.253/4 \times 10^3 \times 10^5) \times 10^8 = 1.31 \text{ turn-in}^2$$

The toroidal core chosen for this application has an inside diameter of 0.550 in., an outside diameter of 0.900 in., a height of 0.125 in. and a core area of 0.013 in^2.

$$N = \frac{1.31}{A} = \frac{1.31}{0.013} = 101 \text{ turns}$$

During subsequent testing of the unit, the number of turns on this inductor and the interbase inductor L2 were changed to operate the unit at a lower frequency with a resulting increase in efficiency.

The wire sizes were chosen so that the winding resistances would allow currents well above the value required to reduce the current gain to zero when L1 saturates.

4. Interbase Inductor (L2)

The design of this component is intimately related to the switching characteristic of the transistors and the base drive current. Past experience has shown that, if maximum current through the inductor is approximately 1/4 the base drive from the current feedback transformer, the inductor will be close to the optimum value. The actual number of turns on the transformer was determined experimentally by varying the number of turns and measuring the efficiency at full load. As stated previously this inductor adds base drive current from transistor turn on through the first half of the "on" period and subtracts base drive during the last half of the "on" period. Although this inductor reduces the switching losses of the transistor, it tends to increase the saturation losses so that the optimum inductor is one which yields the most optimum division of switching and saturation losses.

5. Decoupling Transformer Design (T4 & T5)

Factors affecting the design of these transformers are:

1. Transistor switching time.
2. Ratio of base drive current to load current.

The intent of this design was to keep the current feedback transformer decoupled during the entire turn-off switching interval. The core chosen for this application is a stainless steel bobbin core wound with 39 wraps of .125 in x .001 4-79 MO-PERMALLOY having a saturation flux density of 6.2 kilogauss. This core has an inside diameter of .750" and a height of 0.170". The net core area is:

$$A_c = .039 \times .125 = 4.9 \times 10^{-3} \text{ in}^2$$

$$B(sat) = 40,000 \text{ lines/in}^2$$

$$B \times A_c = 196 \text{ lines}$$

To calculate the number of turns required on winding N3, the following assumptions were made:

1) The transistor switching times would be on the order of 10 μ sec.

2) The voltage appearing across N1 would be approximately 3.0 volts. (Open circuit voltage across T1 secondary less the output voltage and diode drop.)

$$N_s = \frac{3 \times 10^8}{4.44 \times \frac{1}{20 \times 10^{-6}} \times 196} = 6.9 \text{ turns}$$

The number of turns required on winding N2 is determined by the desired back bias on transistors Q1 & Q2. The MHT 2305 transistors are rated for a V_{BE} = 10 volts max.

If seven turns are used in winding N2, the reverse bias across the base emitter junction will be approximately 3.0 volts plus the voltage across N2T2, or approximately 3.55 volts.

To insure proper resetting of the cores, the NI product for winding N1 must exceed the NI product for winding N3 by a margin sufficient to insure saturation of the core. The current in N1 is the output current and is calculated as follows:

$$I_o = \frac{E_{in} \times I_{in}}{E_o} \eta = \frac{2.5 \times 75 \times 0.85}{50} = 3.18 \text{ amps}$$

The base current flowing through winding N2 is 3.45 amps from previous calculations.

The mean magnetic path length for the core used is 2 inches and the required magnetizing force required to insure saturation is 0.25 oersted or 0.5 AT per inch. The required magnetizing force is then 1 ampere turn.

The required number of turns on N3 was then calculated as follows:

$$I_o N3 = Ib\ N1 + 1$$

$$3.18\ N3 = 3.45\ N1 + 1$$

$$N3 = \frac{(3.45 \times 7) + 1}{3.48} = 7.25 \text{ turns}$$

Windings N4 and associated diodes were added to limit the voltage drop across N1 on reset to a low value when resetting the core. Using 30 turns on N4 limits this voltage drop across N1 to approximately 0.16 volt.

	MANUFACTURERS CORE PART NO.	QUANT	MFG.	N1	N2	N3	N4	N5
T1	35E4602	4	MAGNETIC METALS	18FT ½-5/16 ROD	218FT #14 WIRE	2T #24 WIRE	18FT #24 WIRE	—
T2	6T4635-P1	2	ARNOLD	28T #14 WIRE	28T #14 WIRE	1T ½-5/16 ROD	1T ½-5/16 ROD	20T #21 WIRE
T3	A310090-2	1	ARNOLD	160T #27	240T #30	160T #27	—	—
T4	S-625-E-62-H-D 1526F	1	INFINETICS	7T #14	7T #14	7T #14	30T #33	—
T5	S-625-E-62-H-D 1526F	1	INFINETICS	7T #14	7T #14	7T #14	30T #33	—
L1	6T5515D2	1	ARNOLD	150T #21	—	—	—	—
L2	A310090-2	1	ARNOLD	150T #20	—	—	—	—

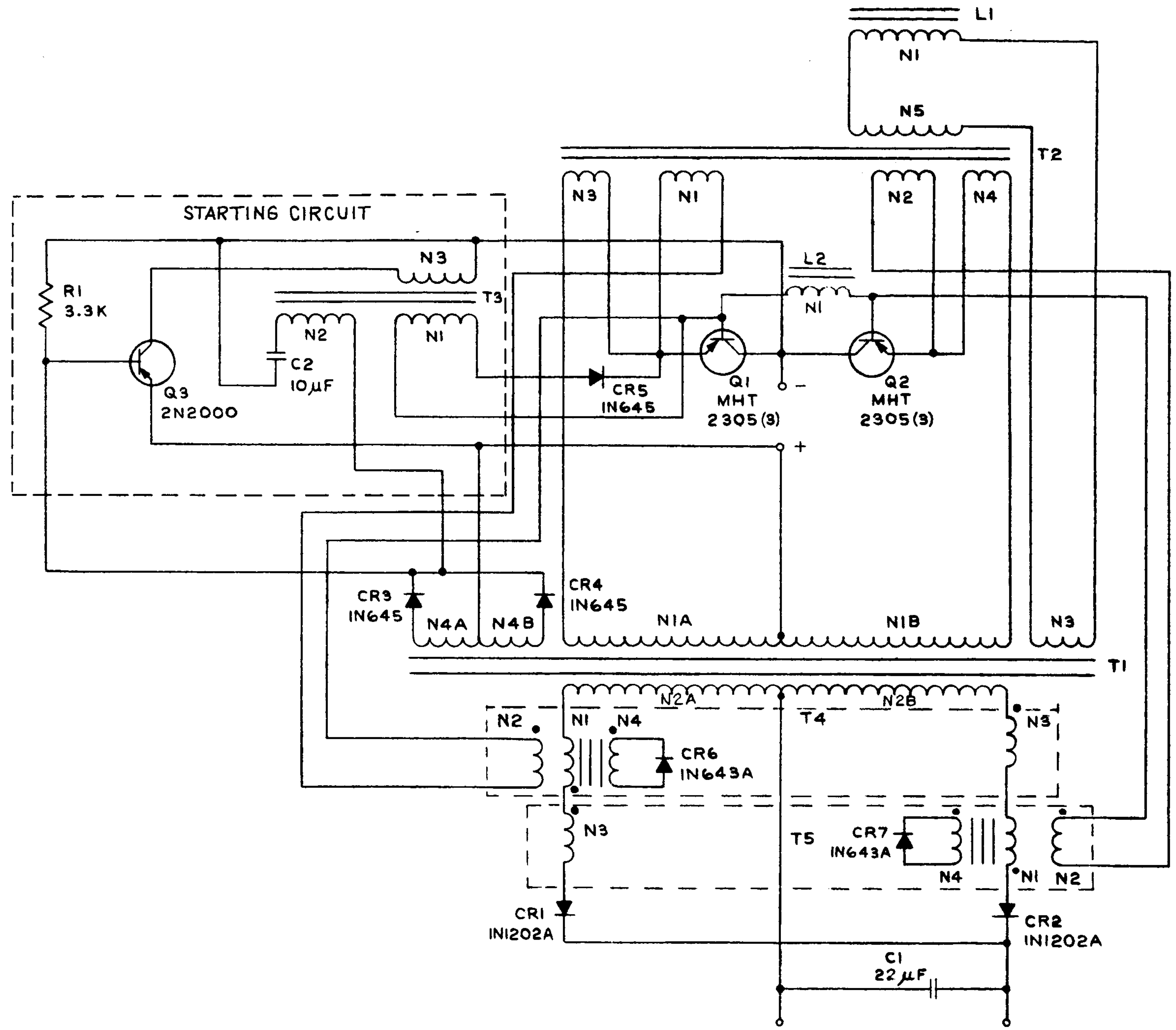

Figure 4 - 2.5-VOLT LIV CONVERTER CIRCUIT DIAGRAM

D. DESIGN, 0.6-VOLT CONVERTER (See Figure 5)

1. Feedback Transformer

In the design of the current feedback transformer the following assumptions and decisions were made:

1) Use "Permalloy" as the core material because of its high saturation flux density and low losses.

2) Design on the basis of a converter frequency of 1KC.

3) Limit the flux density to 25,000 lines per square inch.

4) Utilize Honeywell's MH2101 transistor which was designed especially for use in LIV converters.

5) Drive these transistors at an approximate forced current gain of 28. $\left(\frac{N1}{N3} = \frac{N2}{N4} = 28\right)$

6) Assume a base emitter voltage of 0.55 volt at the 100-ampere input current condition.

7) The winding carrying the heavy currents (N3 and N4) will consist of a single turn.

Because the voltage across the transformer is a square wave the expression $A_c = V \times 10^8/4NfB$ is used to calculate the necessary core area.

$$A_c = \frac{0.55 \times 10^8}{4 \times 28 \times 10^3 \times 25 \times 10^3} = .0196 \text{ in}^2$$

Other factors involved in the selection of the core were the window area necessary to accommodate the co-axial packaging previously designed for NASA-GODDARD and adapted for use on this program, and the availability of the cores.

The toroidal core chosen for this transformer has an outside diameter of 1.375", an inside diameter of 1.000", and a height of 0.25". From this information, the calculated gross core area is 0.0938 in^2.

With a total input current of 100 amperes and a forced current gain of 28, the base current during turn on is $\frac{I_E}{H_{FE}+1} = \frac{100}{28+1} = 3.45$ amperes.

Assuming a current density of 1 ma/cir Mil #16 wire was chosen for the secondary windings (N1 & N2).

2. Power Transformer

The power transformer design was based on the following assumptions and decisions:

1) Use a toroidal core employing "Deltamax" as the core material.

2) Limit the flux density to 50,000 lines per square inch, thereby maintaining a low value of core loss watts per pound.

3) Assume an operating frequency of 1 KC

4) Use a core that will allow a single turn primary, thereby eliminating the need to wind multiple turns of heavy wire.

5) Assume a total primary IR drop, exclusive of transistors, of 5mv at the 100-ampere input condition.

6) Assume an average transistor saturation voltage at 100 amperes of 45 mv.

From these assumptions and design guides, the necessary core was determined as follows:

$$A_c = \frac{V_{N1} \times 10^8}{4\ N1\ f\ B}$$

$$V_{N1} = V_{in} - [\ V_{CE}\ (SAT) + IR\ drop\ ] = 0.6 - [\ .045 + .005] = 0.55\ Volt$$

$$A_c = \frac{0.55 \times 10^8}{4 \times 1 \times 10^3 \times 50 \times 10^3} = 0.275\ in^2$$

The toroidal core chosen for this application has an inside diameter of 1.16 in., an outside diameter of 2.600 in., a height of 0.795 in., and a net core area of 0.365 in^2. Other factors considered in the selection of this core are the space available in the coaxial designed unit, and the availability of the cores.

The number of secondary turns necessary to obtain the desired output of 50 Vdc at the 0.6-volt 100 Adc input condition was determined as follows:

Primary losses = 0.05 volt (from previous assumptions)

Feedback transformer drop = .02 volt

V_p = 0.6 - 0.07 = 0.53 volt

Diode Voltage drop = 0.7 volt

Secondary IR drops including transformer and leads = 0.1 volt

$$Vs = 50 + 0.7 + 0.1 = 50.8 \text{ volts}$$

$$Ns = Vs \frac{N_p}{V_p} = 50.8 \frac{1}{0.53} = 96 \text{ turns}$$

3. Switching Reactor

In order to initiate the switching from one transistor to the other the switching reactor (L1) must pass enough current on saturation to reduce the circuit gain to less than unity. To accomplish this, a winding of 20 turns (N5T2) was placed on the current feedback transformer and a winding of 10 turns (N3T1) was added to the output transformer.

The voltage induced in the feedback transformer winding is:

$$\frac{V_5}{N5} = \frac{V_2}{N2} = \frac{V_1}{N1}$$

$$V_2 = V_1 = 0.55 \text{ volt}$$

$$N2 = N1 = 28 \text{ turns}$$

$$V_5 = 20 \frac{0.55}{28} = 0.393 \text{ volt}$$

The voltage induced in the power transformer winding is:

$$V_{N3} = N3 \frac{V_1}{N1}$$

$$\frac{V_1}{N1} = 0.53 \text{ volt} \quad \text{(from previous calculations)}$$

$$N3 = 10 \text{ turns}$$

$$V_{N3} = 5.3 \text{ volts}$$

The voltage across the inductor, L1, is then equal to the sum of these two voltages since they are connected series aiding.

$$V_{L1} = 5.3 + 0.358 = 5.658 \text{ volts}$$

The necessary reactor NA product was then calculated on the basis of using "Deltamax" as the core material with a saturating flux density of 100,000 lines per square inch.

$$NA = (V/4\ f\ B) \times 10^8$$

$$NA = (5.658/4 \times 10^3 \times 10^5)\ 10^8 = 1.42 \text{ turn - inch}^2$$

The toroidal core chosen for this application has an inside diameter of 0.550 in., an outside diameter of 0.900 in., a height of 0.125 in., and a net core area of 0.013 in^2.

$$N = \frac{1.42}{0.013} = 109 \text{ turns}$$

During subsequent testing of the unit, the number of turns on this inductor and the interbase inductor L2 were changed to operate the unit at a lower frequency with a resulting increase in efficiency. This was possible because of the conservative selection of the cores for the input and feedback transformers.

The wire sizes were chosen so that the winding resistances would allow currents well above the value required to reduce the current gain to zero when L1 saturates.

4. Interbase Inductor(L2)

The design of this component was determined experimentally as described in the design of the 2.5-volt unit.

5. Decoupling Transformer (T4 & T5)

Factors effecting the design of these transformers are:

1. Transistor switching time.
2. Ratio of base drive current to load current.

The intent of this design was to keep the current feedback transformer decoupled during the entire turn-off switching interval. The core chosen for this application is a stainless steel bobbin core wound with 39 wraps of .125 x .001 4-79 MO-PERMALLOY having a saturation flux density of 6.2 kilogauss. This core has an inside diameter of .750" and a height of 0.170". The net core area is:

$$A_c = .039 \times .125 = 4.9 \times 10^{-3} \text{ in}^2$$

$$B(\text{sat}) = 40,000 \text{ lines/in}^2$$

$$B \times A_c = 196 \text{ lines}$$

To calculate the number of turns required on winding N3, the following assumptions were made:

1) The transistor switching times would be on the order of 10 μ sec.

2) The voltage appearing across N1 would be approximately 5 volts. (Open circuit voltage across T1 secondary less the output voltage and diode drop.)

$$N3 = \frac{5 \times 10^8}{4.44 \times \frac{1}{20 \times 10^{-6}} \times 196} = 11.5 \text{ turns}$$

The number of turns required on winding N2 is determined by the desired back bias on transistors Q1 & Q2. The MHT 2101 transistors are rated for a V_{BE} = 13 volts max.

If three turns are used in winding N2, the max reverse voltage across the base emitter junction, even if the entire output voltage of 50 volts is developed across N1, is 12.5 volts. During normal operation, the back bias will be 1.2 volts plus the voltage across N2 T2, or approximately 1.7 volts.

To insure proper resetting of the cores, the NI product for winding N1 must exceed the NI product for winding N3 by a margin sufficient to insure saturation of the core. The current in N1 is the output current and is calculated as follows:

$$I_o = \frac{E_{in} \times I_{in}}{E_o} \eta = \frac{0.6 \times 100 \times 0.8}{50} = .96 \text{ amp}$$

The base current flowing through winding N2 is 3.45 amps from previous calculations.

The mean magnetic path length for the core used is 2 inches and the required magnetizing force required to insure saturation is 0.25 oersteds or 0.5 AT per inch. The required magnetizing force is then 1 ampere turn.

The required number of turns on N3 was then calculated as follows:

$$I_o\,N3 = Ib\,N1 + 1$$

$$.96\,N3 = 3.45\,N1 + 1$$

$$N3 = \frac{(3.45 \times 3) + 1}{.96} = 11.8 \text{ turns}$$

Winding N4 and associated diode were added to limit the voltage drop across N1 on reset to a low value when resetting the core. Using 12 turns on N4 limits this voltage drop across N1 to approximately 0.7 volt.

	MANUFACTURERS CORE PART NO.		MFG.	N1	N2	N3	N4	N5
		QUANT						
T1	289E4602	1	MAGNETIC METALS	18FT COAX	91 DFT #18 WIRE	10T #24 WIRE	2.8FT #24 WIRE	2T #20
T2	6T4635-P1	2	ARNOLD	28T #16 WIRE	28T #16 WIRE	1T COAX	1T COAX	20T #21 WIRE
T3	A310090-2	1	ARNOLD	160T #27	240T #30	160T #27	—	—
T4	S-625-E-62-H-D 1526F	1	INFINETICS	12T #20	3T #14	12T #20	12T #33	—
T5	S-625-E-62-H-D 1526F	1	INFINETICS	12T #20	3T #14	12T #20	12T #33	—
L1	6T5515C2	1	ARNOLD	115 T #21	—	—	—	—
L2	A209257-2	1	ARNOLD	70 T #20	—	—	—	—

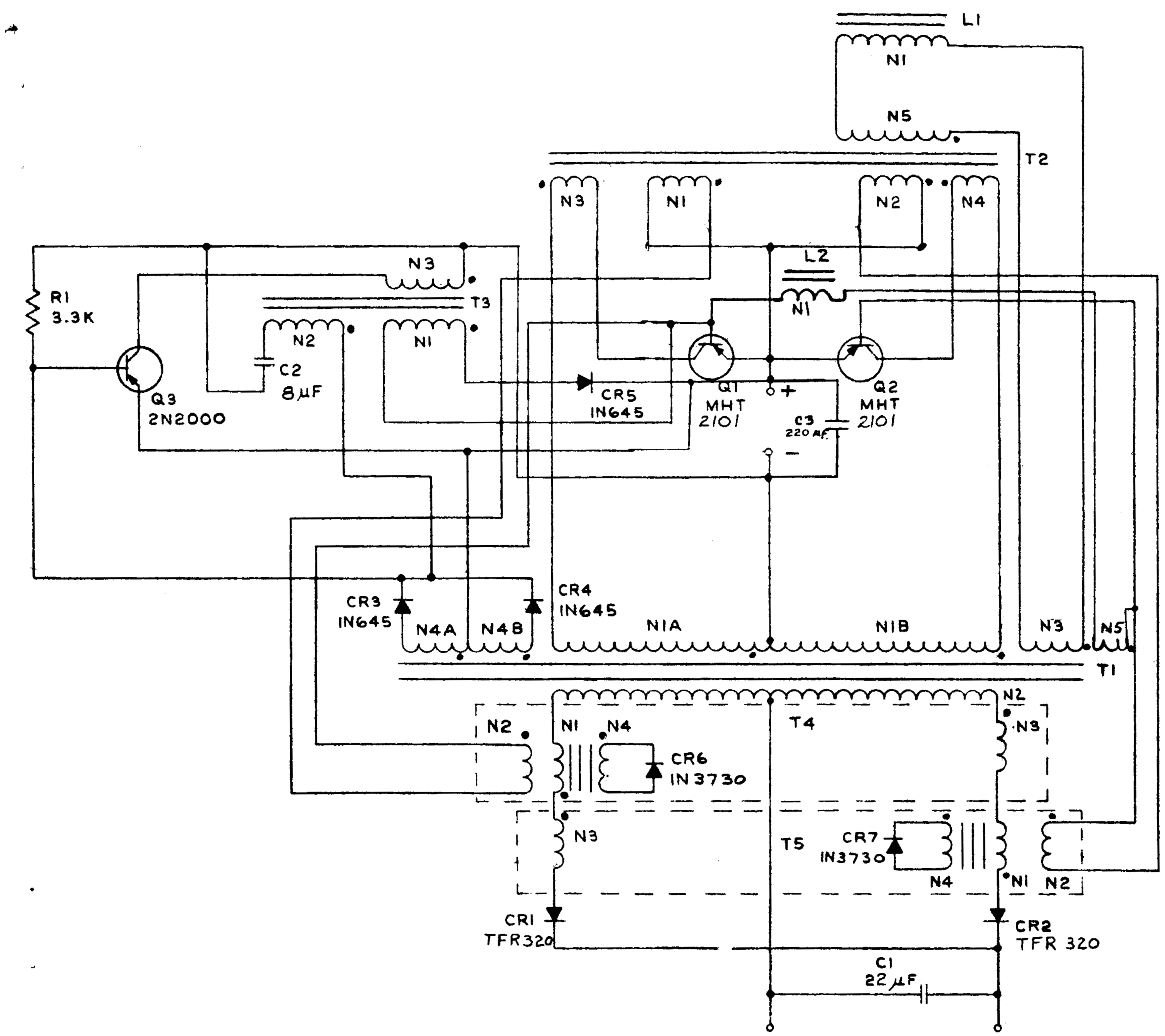

Figure 5 - 0.6 VOLT LIV CONVERTER CIRCUIT DIAGRAM

IV. TEST RESULTS

The test results are included in two reports in the Appendix. OEXM 11, 405 details the test results of the 2. 5-volt converter. OEXM 11, 436 details the test results for the 0. 6-volt converter.

Some difficulty was encountered in obtaining an accurate measurement of the efficiency of the 0. 6-volt unit. The main cause of this difficulty, was the problem of accurately measuring the input power to the system.

During switching there is a period of time (approximately 15 micro seconds) during which both transistors Q_1 and Q_2 are turned off. This reduces the input current to zero; and because of input lead inductance and the regulation of the power source, the input voltage raises to a high spike value.

These input voltage and current wave shapes affect the voltage and current readings in the dc instruments which are used to measure the input. These readings yield calculated input powers that are greater than that actually being applied to the unit.

Ideally, a wattmeter would be used to establish the input power consumption; but wattmeters in this range were not available. Without wattmeters for measuring the input power, the true integral of the instantaneous product of the voltage and current cannot easily be established unless the load is ohmic (i = ke), and therefore the product of the average values of the current and voltage does not equal the average of the product. In this case, the current was at or near zero when the voltage shows a spike.

$$\left(\frac{I}{T} \int_{o}^{t} e\,dt \right) \left(\frac{I}{T} \int_{o}^{t} i\,dt \right) \neq \frac{I}{T} \int_{o}^{t} e\,i\,dt$$

A considerable period of time was spent in trying to eliminate these voltage spikes by adding capacitance and shunt resistors across the power source output terminals but with little success. The fact that the input currents are so high requires very large capacitors to absorb the currents during this short period. Since the period is short, the inductance of the capacitors has to be very low to allow the charge to be accepted within the time allowed. Significant reductions of the voltage spike could not be achieved by adding capacitance.

In order to more properly measure the input power to the converter, the input voltage was measured on a calibrated oscilloscope so that the voltage spike (which occurred at zero current and zero power input) could be ignored. The above testing procedure was necessary only on the 0.6-volt model. The transients present in the higher voltage model were less in actual magnitude (possibly because of lower current levels) and in terms of percentage change they were much less than the transients noted in testing the 0.6-volt model. The problems involved in testing the 0.6-volt model prohibited as extensive testing as for the 2.5-volt model.

The low value of load regulation and the difficulty of accurately measuring the input voltages precluded any accurate measurement of the output impedance level. The unit design minimized the output impedance to such an extent that output voltage regulation for load changes became difficult to measure and verify.

The regulation of the power source was much greater than that of the converter. The change in loading on the power source caused changes in the wave shape and in the apparent input voltage to such an extent that the measurements do not appear meaningful unless the source is standard or specified.

V. RECOMMENDATIONS FOR FURTHER IMPROVEMENTS

It is our recommendation that further investigations in low input voltage conversion be directed toward the following:

1) Adding voltage regulation and overload or short circuit protection circuitry. Excellent efficiencies have been achieved on other units by utilizing pulse width modulation type regulators.

2) Designing to meet the various environmental conditions likely to be encountered such as temperature extremes, radio frequency interference, and shock and vibration.

3) Designing the converter for operation with a specific power source and considering such things as optimizing the input lead resistance and conducting heat transfer tests.

4) Consideration should be given to the possibility of using the high frequency diffused base type transistors in the higher input voltage units. Operation in the 3-20kc range appears feasible with these units and a corresponding reduction in weight and volume would be achieved.

5) Where there is a requirement for minimum magnetic field disturbance, further study of the coaxial design would be required.

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DEV. NO. ~~OEXM 11,405~~

ENGINEERING TEST REPORT

001

RL Carlson 806
RT Mooers 806
SD Heaner 806
L Lingle 806
ER Morey 836
RC Aakhus 824

DATE

PAGE 1 OF 3

ISSUED BY: 31 December 1964

ORDNANCE ENGINEERING EVALUATION

ITEM TESTED

One Low Input Voltage Converter 2.5V @75A Input, P/N EXG 2424C3X1. Manufactured by Honeywell Ord Tech Lab.

OBJECT OF TEST

Conduct tests per paragraph 4.2 of DS 7076-1. This is the pre-shipment test for the Converter.

CONCLUSIONS

At room ambient with an input current of 75 amperes and an input voltage of 2.5V, the converter has an efficiency of 86.4% (required = 85% min.).

The converter weight is 4.20 lbs and the volume is approximately 89.4 cubic inches. Required weight and volume is 16.5 lbs maximum and 370 cubic inches respectively.

The output voltage varies between 34.5 and 60.5 volts depending on the output power, input voltage, and temperature.

Since the above were the only criteria it is concluded that the converter meets the design requirements.

PROCEDURE

The unit was connected as shown in Figure 1 and tested at room ambient conditions. Following testing at room ambient, the converter was placed in a Statham, Model TC-2B Temperature Chamber and the temperature was lowered to -65°F(-54°C). After a minimum of two hours at -65°F and while at this temperature, the converter was again tested. The chamber temperature was slowly raised to +160°F (+70°C) and the unit was allowed to stabilize at this temperature for a minimum of two hours and was then tested while at 160°F.

KEYWORDS:

Converter, LIV

ATTACHMENTS:

Data Sheets
Graphs

DATA BOOK NO.	PAGE	
REQUESTED BY	DATE	WRITTEN BY
~~0-912 126-126~~ Date Started 12-28-64 DEPARTMENT		Completed 12-29-64 APPROVED
~~R L Carlson~~	12-14-64	

G-1046 WHITE
G-1046A DITTO MASTER

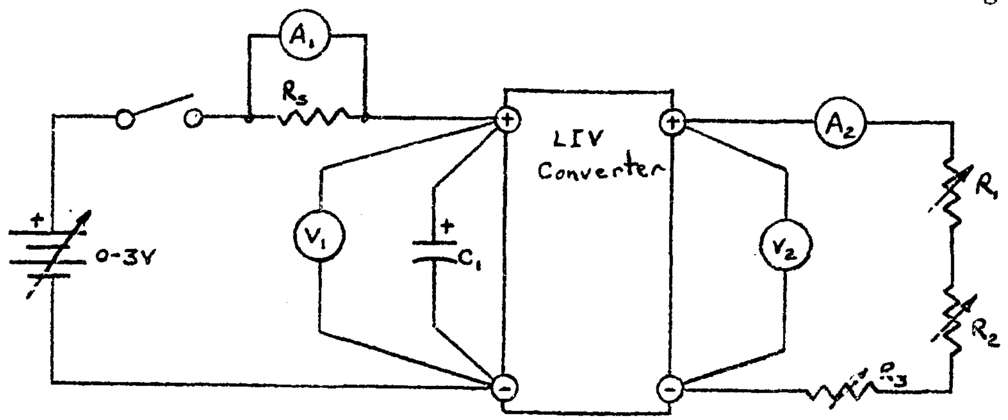


Figure 1
Test Circuit

The converter was weighed on an analytic balance and weighed 1892.289 gm (4.20 lbs). The overall dimensions from the terminal lug tips to the banana jack tips, and base plate side to base plate side were then made and are shown in Figure 2.

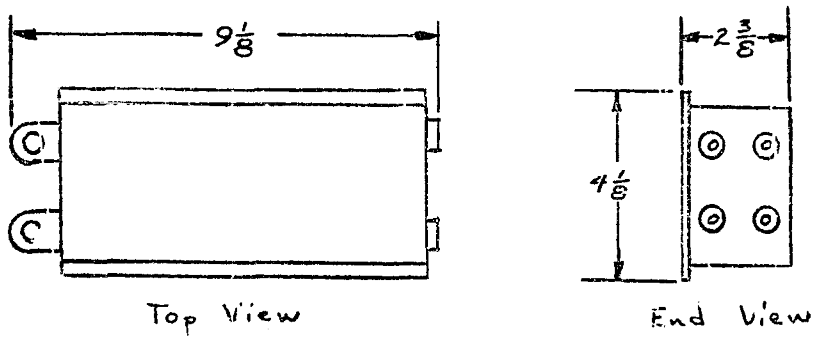


Figure 2
Physical Dimensions

RESULTS

The data obtained is listed in the three attached data sheets. The input current with no load connected is listed as being zero on the data sheets but was actually that listed in Table I below. At room ambient and +160°F with no output load connected, the unit did not go into a switching mode and only a high frequency damped oscillation appeared on the oscilloscope.

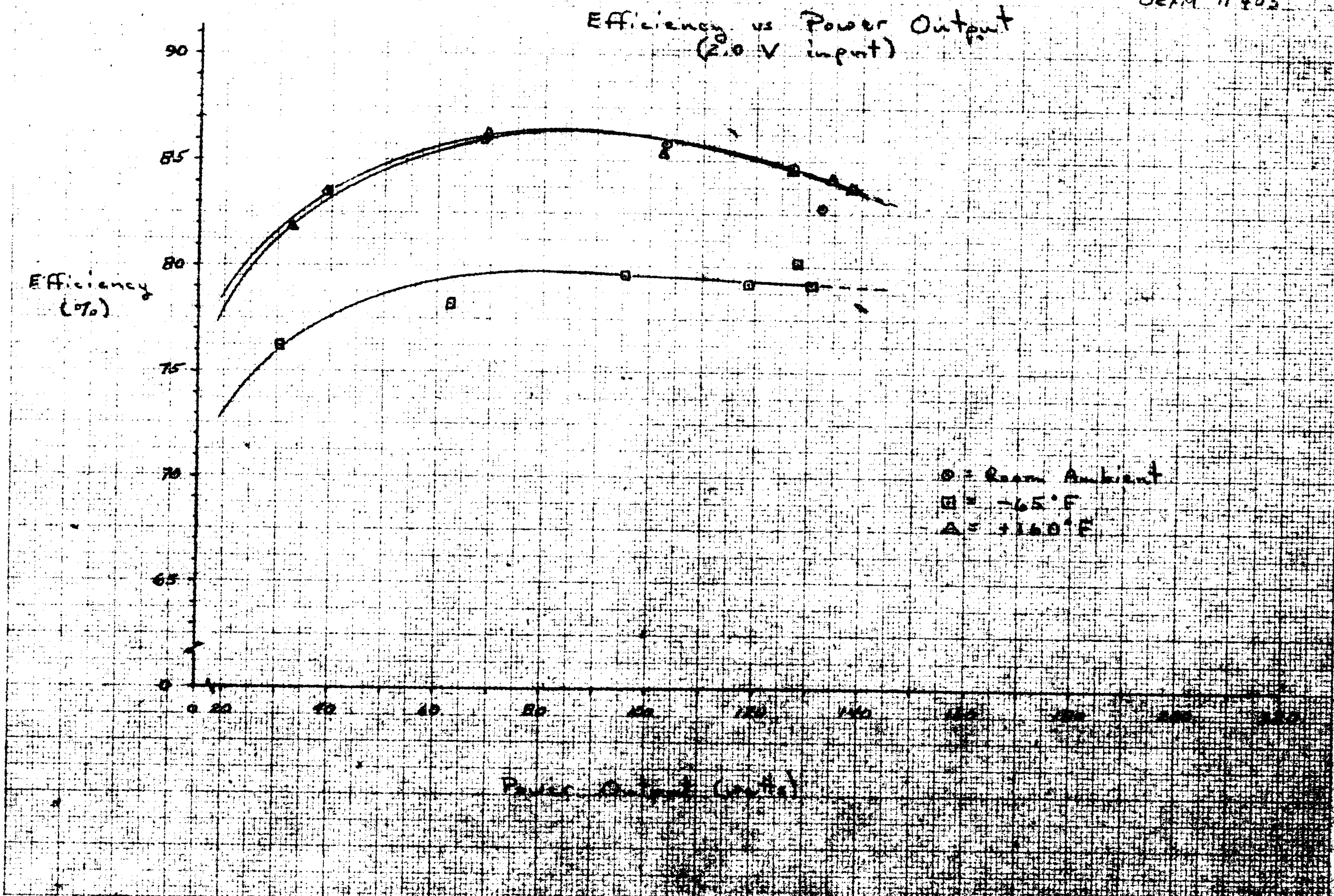
Input Voltage	Temperature		
	-65°F	75°F	+160°F
2.0V	1.38	0.1	0.28
2.5V	1.55	0.1	0.30
3.0V	1.70	0.1	0.30

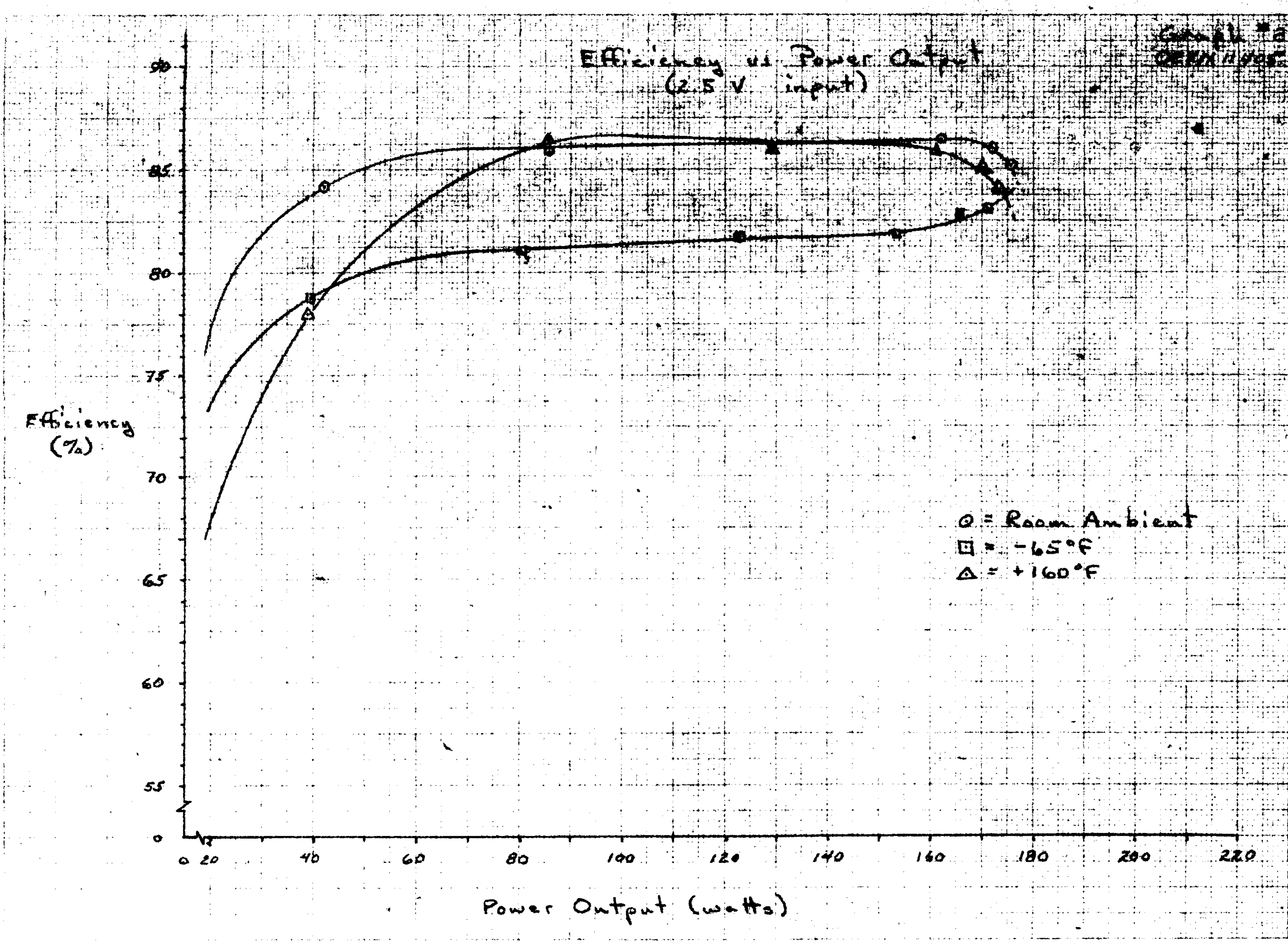
TABLE I
No Load Input Current in Amperes

INSTRUMENTATION

V_1 = 0-3.0 V, Weston #931 (158-016)
V_2 = 0-50V and 0-100V, Weston #931 (158-027)
A_1 = 0-10A and 0-100A, Weston #931 (102-043)
A_2 = 0-0.5A and 0-5A, Weston #931 (102-004)
C_1 = 34,000 uf @15V, Mallory #CG343u15F1
R_1 = 27 , 5A Slidewire, Jagabi (144-029)
R_2 = 108 , 2.3A Slidewire, Jagabi (144-034)
R_3 = 900 , 0.7A Slidewire, Jagabi (144-039)
R_s = 50 mV meter shunt for A_1, Weston (102-020 and 102-050)
Tecktronix #504 Oscilloscope (138-029)

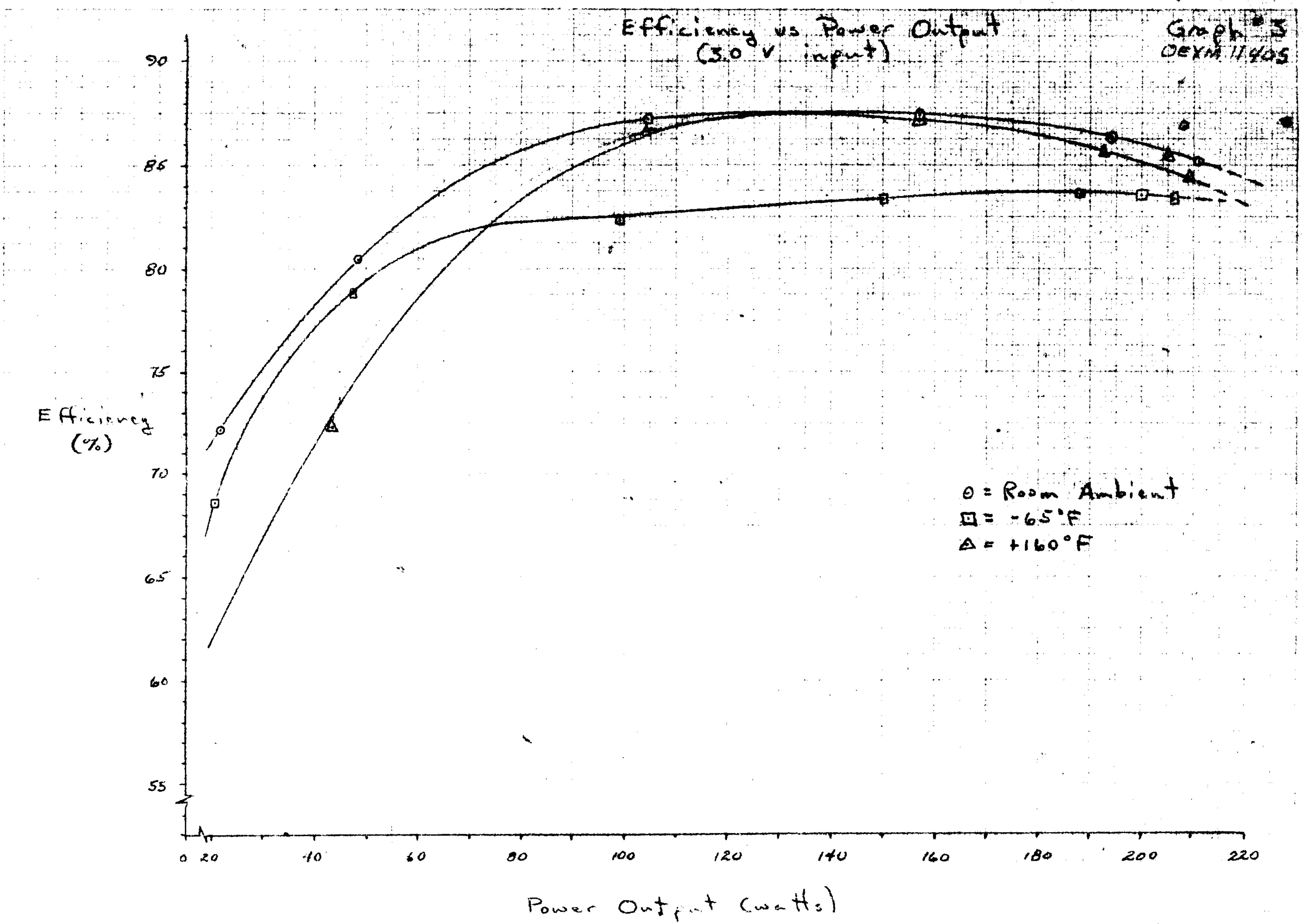
Graph #I
OEXM 11405

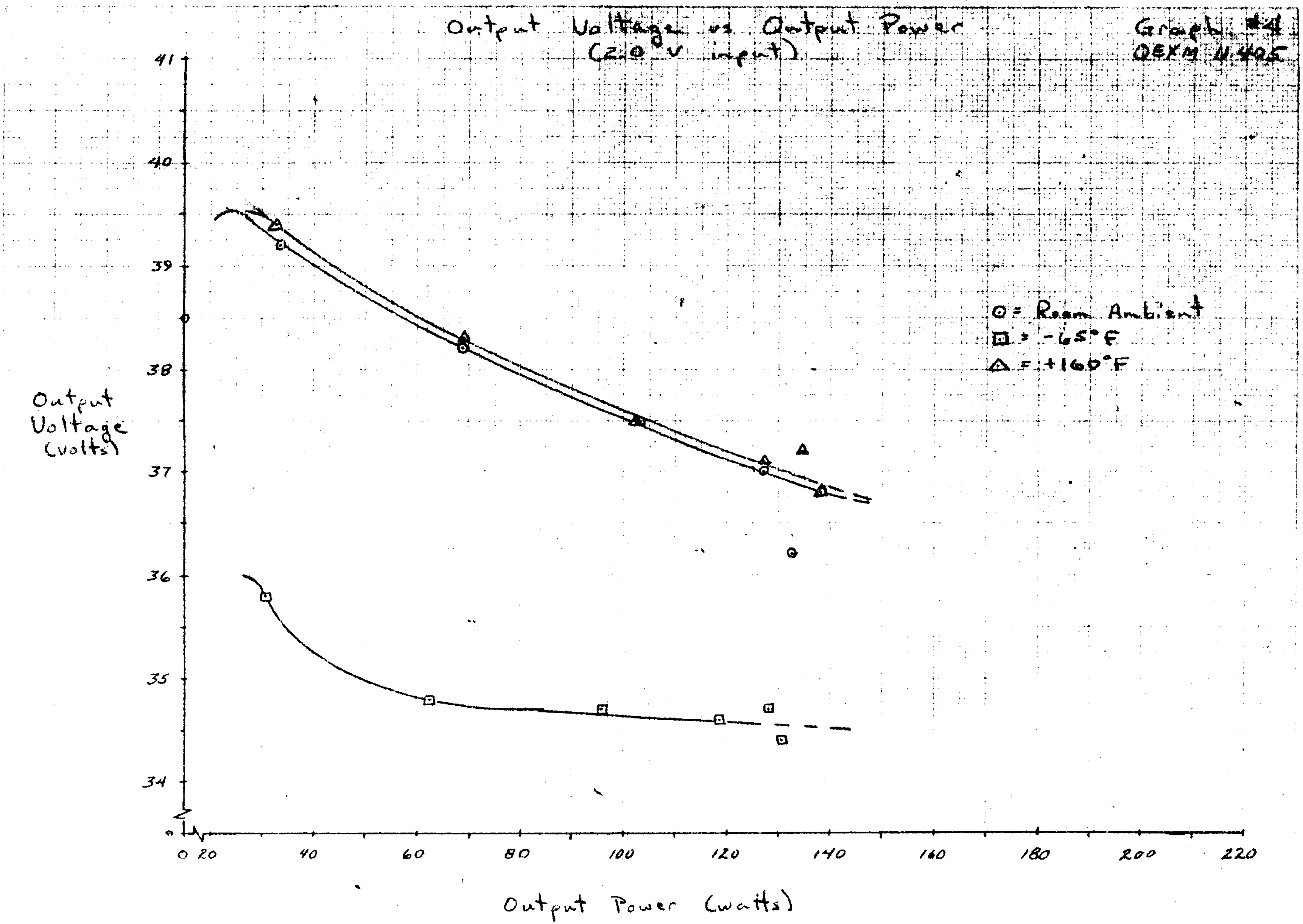


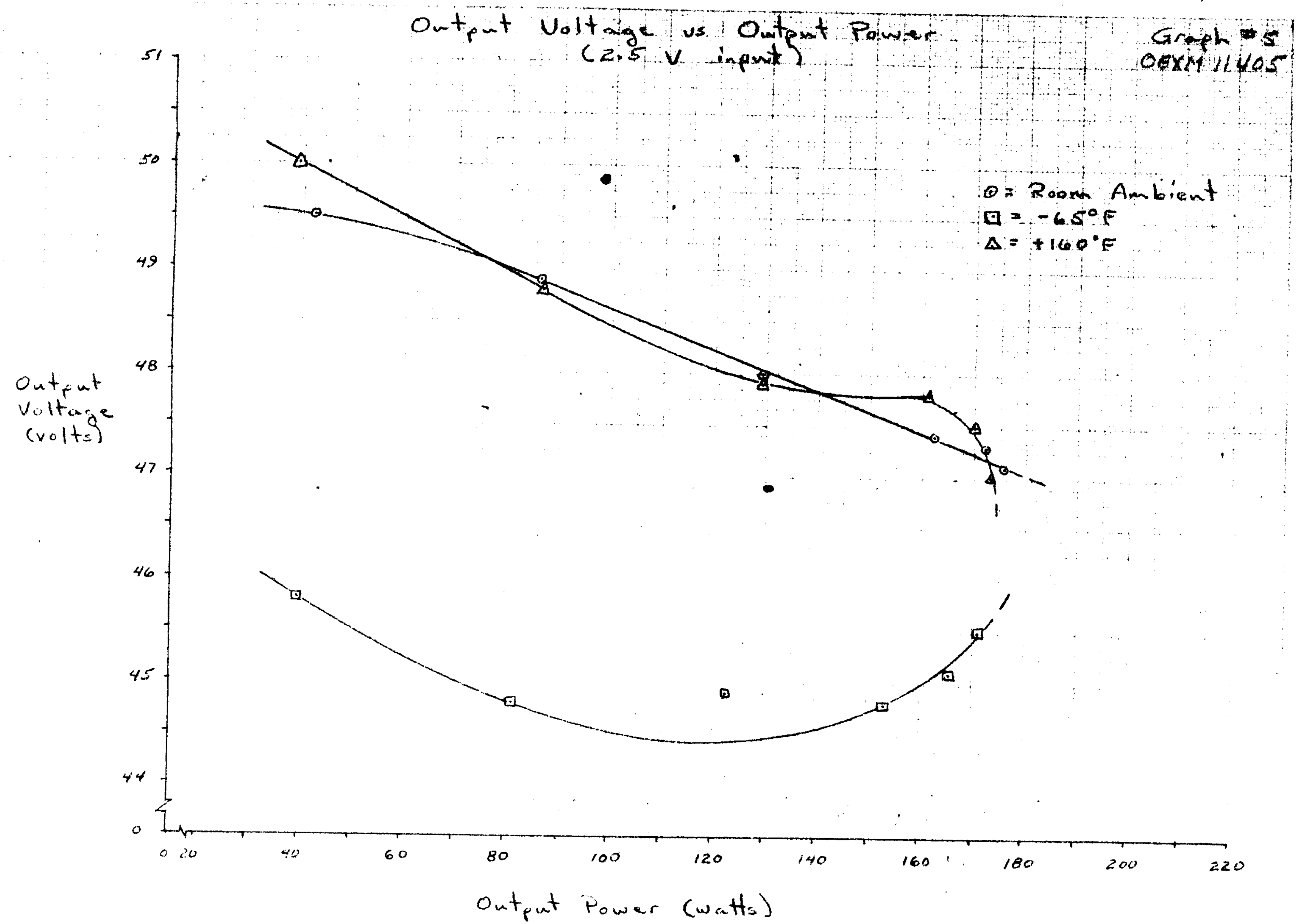


Graph #2
Efficiency vs Power Output
(2.5 V input)
Efficiency (%)
90
85
80
75
70
65
60
55
0
0
20
40
60
80
100
120
140
160
180
200
220
Power Output (watts)
O = Room Ambient
□ = -65°F
△ = +160°F

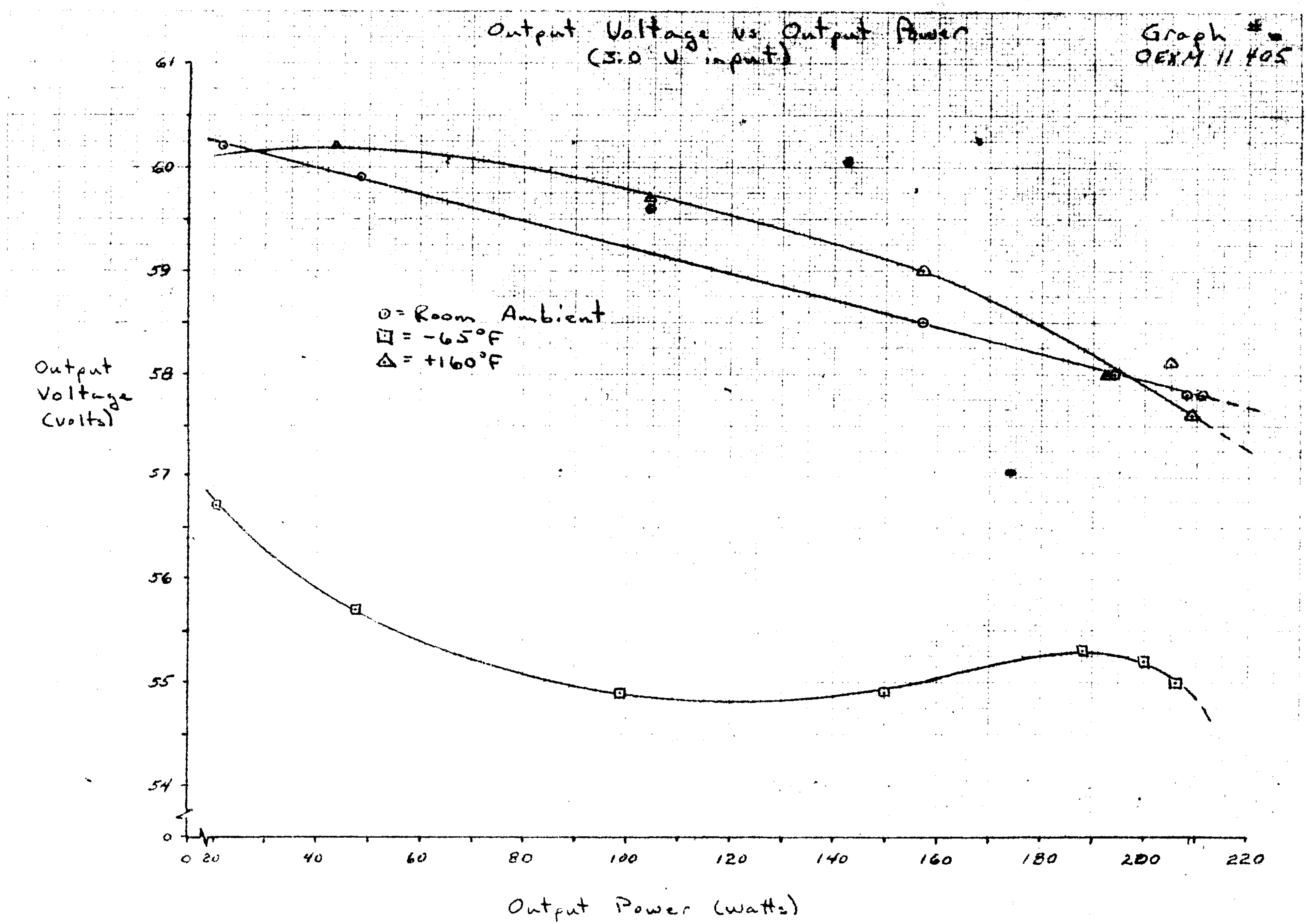
98-3475


Efficiency vs Power Output
(3.0 V input)
Graph # 3
OEXM 11405
90
85
80
75
70
65
60
55
Efficiency
(%)
0
20
40
60
80
100
120
140
160
180
200
220
Power Output (watts)
⊙ = Room Ambient
⊡ = -65°F
△ = +160°F


Output Voltage vs Output Power
(20 V input)
Graph #4
QEXM 11.405
○ = Room Ambient
□ = -65°F
△ = +160°F
Output Voltage (volts)
41
40
39
38
37
36
35
34
0
0
20
40
60
80
100
120
140
160
180
200
220
Output Power (watts)



Output Voltage vs Output Power
(2.5 V input)
Graph #5
OEXM 11405
⊙ = Room Ambient
⊡ = -65°F
Δ = +160°F
Output Voltage (volts)
51
50
49
48
47
46
45
44
0
0 20
40
60
80
100
120
140
160
180
200
220
Output Power (watts)


Output Voltage vs Output Power
(3.0 V input)
Graph #
OEXM 11 405
⊙ = Room Ambient
⊡ = -65°F
△ = +160°F
Output Voltage (volts)
Output Power (watts)
61
60
59
58
57
56
55
54
0
0
20
40
60
80
100
120
140
160
180
200
220

OEXM 11405

LIV Converter
EXG 2424 C3X1

Date 12-29-64 Environment -65°F

I_{in} (Amp)	E_{in} = 2.0 Volts			E_{in} = 2.5 Volts			E_{in} = 3.0 Volts		
	E_{out} (Volts)	I_{out} (Amp)	Freq (cps)	E_{out} (Volts)	I_{out} (Amp)	Freq (cps)	E_{out} (Volts)	I_{out} (Amp)	Freq (cps)
0	38.6	0	15,600	49.1	0	16,400	62.7	0	17,600
3.2	36.2	0.070	6950	46.1	0.064	9260	56.2	0.057	10,400
5	36.2	0.145	5820	46.0	0.138	6770	56.2	0.132	7580
10	36.0	0.372	3390	46.2	0.362	3920	56.7	0.363	4710
20	35.8	0.852	1960	45.8	0.86	2175	55.7	0.85	2500
40	34.8	1.795	1160	44.8	1.81	1417	54.9	1.80	1493
60	34.7	2.75	944	44.9	2.73	1053	54.9	2.73	1190
75	34.6	3.43	835	44.8	3.42	980	55.3	3.40	1138
80	34.7	3.69	807	45.1	3.67	980	55.2	3.63	1123
82.5	34.4	3.79	794	45.5	3.76	980	55.0	3.75	1123

I_{in} (Amp)	E_{in} = 2.0 Volts				E_{in} = 2.5 Volts				E_{in} = 3.0 Volts			
	P_{in} (Watt)	P_{out} (Watt)	E_{out} (Volt)	Eff (%)	P_{in} (Watt)	P_{out} (Watt)	E_{out} (Volt)	Eff (%)	P_{in} (Watt)	P_{out} (Watt)	E_{out} (Volt)	Eff (%)
0	2.76	0	38.6	—	3.88	0	49.1	—	5.1	0	62.7	—
3.2	6.4	2.53	36.2	39.6	8	2.95	46.1	36.9	9.6	3.20	56.2	33.3
5	10	4.77	36.2	47.7	12.5	6.35	46.0	50.8	15	7.42	56.2	49.4
10	20	13.4	36.0	67.0	25	16.7	46.2	66.9	30	20.6	56.7	68.6
20	40	30.5	35.8	76.2	50	39.4	45.8	78.8	60	47.4	55.7	78.8
40	80	62.5	34.8	78.2	100	81.1	44.8	81.1	120	98.8	54.9	82.3
60	120	95.5	34.7	79.6	150	122.5	44.9	81.7	180	150	54.9	83.3
75	150	118.6	34.6	79.2	187.5	153	44.8	81.8	[illegible]	188	55.3	83.6
80	160	128	34.7	80.1	200	165.5	45.1	82.8	240	200	55.2	[illegible]
82.5	165	130.4	34.4	79.1	206	171	45.5	83.1	[illegible]	206	55.0	83.3

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KEYWORDS:
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verter,L.I.V.
G2424C4X1

ATTACHMENTS:

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HONEYWELL Military Products Group

REPORT NO.

DEV. NO. ~~OEXM 11,436~~ 001

ENGINEERING TEST REPORT

DATE

PAGE 1 OF 2

ISSUED BY: February 25, 1965

ORDNANCE EVALUATION ENGINEERING

UNITS TESTED

One Low Input Voltage Converter (EXG2424C4X1, D. 7076-1) made by Honeywell Ordnance Tech. Lab.

OBJECT OF TEST

1. Determine efficiency when the input is 100 amperes at 0.6 volts.

2. Measure the 800-cycle component of output ripple (Vr) under the input conditions of (1) above.

3. Determine the volume and weight of the Converter.

DOCUMENTATION

Efficiency. 84.6%
"800" Cycle Ripple.....0.5 Vrms
Weight. . . . . .6.5 pounds
Volume. . . . . .77 $in.^3$

PROCEDURE

Figure 1 shows the test setup used to check the converter. Note that an oscilloscope was used to measure the input voltage. This provides a means of measuring the d-c level of the input voltage which is complicated with switching transients from the converter, even though a filter is used as shown.

The converter was preshipment checked to the requirements of D.S. 7076 only to the extent documented above.

DATA BOOK NO.	PAGE	
REQUESTED BY	DATE	WRITTEN BY
~~0-936~~	~~30-33~~	~~Started 24 February 1965 Completed 24 February 1965~~
DEPARTMENT		APPROVED
~~R. Carlson~~	~~18 February 1965~~	K. L. Gorlinsky
Engineering, Electromechanical		

OEXM 11405

LIV Converter
EXG 2424 C3X1

Date 12-28-64

Environment Room Ambient

I_{in} (Amp)	E_{in} = 2.0 Volts			E_{in} = 2.5 Volts			E_{in} = 3.0 Volts		
	E_{out} (Volts)	I_{out} (Amp)	Freq (cps)	E_{out} (Volts)	I_{out} (Amp)	Freq (cps)	E_{out} (Volts)	I_{out} (Amp)	Freq (cps)
0	38.9	0	—	49.9	0	—	60.8	0	—
3.2	39.[illegible]	0.067	8060	50.2	0.069	9450	60.2	0.062	10,650
5	39.1	0.150	5960	50.0	0.144	6850	60.6	0.136	7820
10	[illegible]	0.375	3640	50.0	0.368	4170	60.2	0.360	4760
20	39.[illegible]	0.852	2130	49.5	0.850	2470	59.9	0.806	2860
40	[illegible]	1.800	1320	48.9	1.755	1540	59.6	1.755	1725
60	37.[illegible]	2.750	1020	48.0	2.69	1180	58.5	2.69	1333
75	[illegible]	3.44	910	47.4	3.42	1040	58.0	3.35	1235
80	36.2	3.66	862	47.3	3.64	1020	57.8	3.60	1235
82.5	[illegible]	3.75	862	47.1	3.73	1010	57.8	3.65	1205

I_{in} (Amp)	E_{in} = 2.0 Volts				E_{in} = 2.5 Volts				E_{in} = 3.0 Volts			
	P_{in} (Watt)	P_{out} (Watt)	E_{out} (Volt)	Eff (%)	P_{in} (Watt)	P_{out} (Watt)	E_{out} (Volt)	Eff (%)	P_{in} (Watt)	P_{out} (Watt)	E_{out} (Volt)	Eff (%)
0	0	0	38.9	—	0	0	49.9	—	0	0	60.8	—
3.2	6.4	2.63	39.2	41.1	8	3.46	50.2	43.3	9.6	3.73	60.2	38.9
5	10	5.87	39.1	58.7	12.5	7.2	50.0	57.6	15	8.25	60.6	54.9
10	20	14.44	38.5	72.2	25	18.4	50.0	73.6	30	21.7	60.2	72.2
20	40	33.4	39.2	83.5	50	42.1	49.5	84.2	60	48.3	59.9	80.4
40	80	68.8	38.2	86.0	100	85.8	48.9	85.8	120	104.5	59.6	87.2
60	120	103	37.5	85.8	150	129	48.0	86.2	180	157	58.5	87.4
75	150	127	37.0	84.7	187.5	162	47.4	86.4	225	194	58.0	86.3
80	160	132.5	36.2	82.8	200	172	47.3	86.0	240	208	57.8	86.8
82.5	165	138	36.8	83.7	206	175.5	47.1	85.2	247.5	211	57.8	85.2

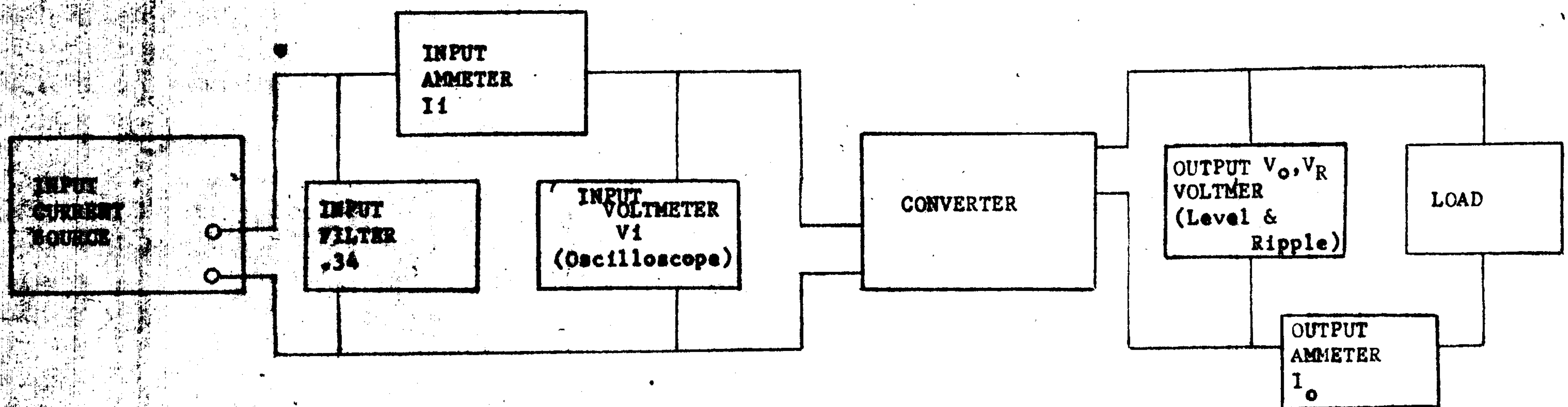
OEXM 11405

LIV Converter
EXG 2424 C3X1

Date 12-29-64 Environment + 160°F

I_{in} (Amp)	E_{in} = 2.0 Volts			E_{in} = 2.5 Volts			E_{in} = 3.0 Volts		
	E_{out} (Volts)	I_{out} (Amp)	Freq (cps)	E_{out} (Volts)	I_{out} (Amp)	Freq (cps)	E_{out} (Volts)	I_{out} (Amp)	Freq (cps)
0	39.8	0	—	50.9	0	—	61.3	0	—
3.2	39.9	0.062	7820	50.9	0.052	9440	61.0	0.060	9620
5	40.0	0.128	5820	50.4	0.116	6810	61.0	0.105	7820
10	39.4	0.333	3575	50.2	0.318	4170	60.7	0.303	4760
20	39.4	0.83	2080	50.0	0.78	2500	60.2	0.72	2940
40	38.3	1.80	1383	48.8	1.77	1490	59.7	1.74	1725
60	37.5	2.73	1000	47.9	2.69	1178	59.0	2.66	1343
75	37.1	3.42	910	47.8	3.37	1064	58.0	3.32	1235
80	37.2	3.62	877	47.5	3.58	1042	58.1	3.53	1220
82.5	36.8	3.75	862	47.0	3.68	1032	57.6	3.63	1220

I_{in} (Amp)	E_{in} = 2.0 Volts				E_{in} = 2.5 Volts				E_{in} = 3.0 Volts			
	P_{in} (Watt)	P_{out} (Watt)	E_{out} (Volt)	Eff (%)	P_{in} (Watt)	P_{out} (Watt)	E_{out} (Volt)	Eff (%)	P_{in} (Watt)	P_{out} (Watt)	E_{out} (Volt)	Eff (%)
0	0.56	0	39.8	—	0.75	0	50.9	—	0.9	0	61.3	—
3.2	6.4	2.47	39.9	38.6	8	2.65	50.9	33.1	9.6	3.66	61.0	38.1
5	10	5.12	40.0	51.2	12.5	5.85	50.4	46.8	15	6.40	61.0	42.7
10	20	13.1	39.4	65.6	25	15.95	50.2	63.8	30	18.4	60.7	61.3
20	40	32.7	39.4	81.8	50	39	50.0	78.0	60	43.4	60.2	72.3
40	80	69.0	38.3	86.2	100	86.4	48.8	86.4	120	104	59.7	86.6
60	120	102.4	37.5	85.3	150	129	47.9	85.9	180	157	59.0	87.2
75	150	127	37.1	84.6	187.5	161	47.8	85.9	225	192.5	58.0	85.6
80	160	134.6	37.2	84.2	200	170	47.5	85.0	240	205	58.1	85.4
82.5	165	138	36.8	83.7	206	173	47.0	84.0	247.5	209	57.6	84.4



$Ii = 100$ A
$Vi = 0.6$ V
$Pi = 60$ W

$I_o = 1.03$ A
$V_o = 49.3$ V
$P_o = 50.8$ W
$V_R = 0.5$ Vrms

Figure 1 - Test setup used to measure Converter efficiency and output ripple.