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A COMPARISON OF BURN-IN AND BAKE AS SEMICONDUCTOR SCREENING TECHNIQUES FOR THE NIMBUS SPACECRAFT PROGRAM

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by

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ABSTRACT:

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This report summarizes and compares the relative effectiveness of high temperature storage (bake) and high temperature operating burn-in as screening techniques for semiconductor devices used in the Nimbus spacecraft program. Data for this report were accumulated from summaries of burn-in and bake screening performed by Nimbus contractors. Results are presented for 162 different types of semiconductor devices, with an overall sample size of 70,300 for an aggregate of 49 million device hours for both screening techniques.

Results indicate that burn-in is superior to bake for every class of semiconductor device and for every manufacturing process used in the fabrication of the devices. Correlation is shown between rated power dissipation and burn-in effectiveness. Statistical significance of the data is evaluated when comparability of types is possible, i.e. where the types were both burned-in and baked.

INTRODUCTION:

Semiconductor device reliability is an essential element in achieving space systems reliability primarily because they are used in very large quantities and form the electronic heart of the systems. The attainment of high reliability in these parts is dependent on two factors:

1. Manufacturing process control which depends to a large extent on the discovery and definition of failure mechanisms present in the design of the devices.

2. Discovery or culling out of defects introduced during device fabrication which affect circuit performance.

It is well established that semiconductor devices exhibit the characteristic of "infant mortality" in which failure mechanism and/or defects in the device manifest themselves in a relatively short time period compared to the expected life of the systems in which they are used. Two methods for screening or weeding out defectives introduced during the manufacturing process from the device population, which have been extensively used, are high temperature storage or bake without power added and power ageing or burn-in which adds power dissipation to temperature and thus more nearly approximates use conditions.

The high temperature storage or bake screen weeds out failure mechanisms or defects which are dependent on temperature alone. Some examples are mechanical stresses of internal lead wire connections to pins induced by thermal expansion at metallic surfaces; poor thermal compression bonds to emitter and base stripes; chemical reactions such as outgassing of surface impurities and changes in the gaseous impurities in the base regions.

Power ageing or burn-in, in addition to the above, detects and culls out failure modes associated with both voltage and current. Those associated with current are due to the formation of hot spots caused by non-uniform junctions, or voids between the semiconductor and the header. Irregularities in the region of the depletion layer leading to punch-through show up as a voltage defect.

Results of studies on 73,000 Minuteman diodes at TRW indicate that use of high temperature with a fixed level of power results in a higher level of failures than does the use of high power at low temperature. The selection of higher ambient temperature assures that the entire device is at an elevated temperature. Thus contaminants which are present may be boiled into the device internal atmosphere which increases the possibility of detecting the placement of contaminants at the device junctions[1]. Burn-in at high temperature thus screens out defects dependent on chemical, electrical, and thermal stresses while bake screens out defects dependent only on thermal stresses.

NIMBUS SEMICONDUCTOR PROGRAM

The high temperature storage (bake) program was implemented by all Nimbus subsystem contractors in late 1961, and consisted of subjecting all silicon semiconductors to a high temperature environment, 100°C, for a period of six weeks or 1000 hours. Germanium devices were baked at 80°C for the same period. The devices screened represented a good cross-section of available commercial and military types and the results indicated that only 1.5 percent of baked units failed. A smaller percentage of these failures, however, was catastrophic (i.e., was of the variety which would seriously degrade the Nimbus mission).

In October 1962, recognized authorities in the field of semiconductor manufacturing and device designs were consulted for comments on a power ageing (burn-in) specification[2]. Based on these comments a specification was drawn up which received Nimbus Project approval in November 1962.

The procedure employed elevated ambient temperatures, 100°C for silicon devices and 50°C for germanium for a period of less than two weeks (300 hours). Power was applied to the device in this environment to increase the junction temperature to a nominal 80 percent of its maximum value. Transistor parameters tested were DC current gain, h_{FE} and reverse leakage current I_{CBO}. Pre- and post-burn-in parameter end points were based on military specification formulas, i.e., 20 percent loss in h_{FE} or 100 percent increase in I_{CBO} were criteria for rejection. Voltage, current, and power ratings were not to be exceeded.

The rationale for this specification was as follows:

a. DC current gain stabilizes when exposed to high temperature after 100 hours.

b. An elevated temperature power condition tends to accelerate thermal chemical and electrical failure mechanisms. It also reduces the requirement for high voltage or current power supplies in the case of power transistors.

c. The 300 hour time period was equivalent to that used in the Minuteman program.

d. The nominal 80 percent of maximum junction temperature was specified as a safety factor to allow for slight variations in thermal resistance from unit to unit.

The specification was transmitted to the OGO Project for information and possible application and was reviewed and endorsed in a memorandum by the Planning Research Corporation, the reliability contractor for the OGO Project, which pointed out that the burn-in requirement used by the Nimbus Project at 80 percent rated junction temperature for two weeks is potentially capable of providing a failure rate reduction for OGO parts. . . by a factor of 2 to 18, the same as Telstar. . .

at significantly less expense and within a minimal time period. "Derated burn-in at expected operating conditions would achieve the same failure rate reduction but would require a burn-in period of 20 weeks."[3]

All semiconductors screened by Nimbus contractors are listed alpha-numerically in Appendix A. Code letters for device manufacturer, process of manufacture and device power dissipation rating are presented for each device type. The code key is shown on page 15 of this report. In addition, the number of devices screened, number rejected and percent rejected are listed separately for each type and manufacturer and are shown for both screening techniques.

Appendix C represents a regrouping of the alpha-numerical types by class of semiconductor device and by process and power ratings. Subtotals are indicated for process-power groups and for power groups. Totals are shown for classes of devices. The results are summarized in the body of the report.

The data were accumulated from reports furnished by Nimbus contractors and for both screening techniques represents a total of 68 transistor types with a total sample size of 25,420 and a total of 102 diode types with a total sample size of 44,907. Total device hours for transistors was 18 million hours and for diodes was 31 million hours for a combined total of 49 million semiconductor device hours.

RESULTS OF SCREENING BY CLASS OF SEMICONDUCTOR DEVICES

A summary of results of burn-in and bake screening for silicon and germanium transistors is shown in Tables 1 and 2, respectively. Also summarized are the results of screening diodes, Table 3. The reject figures include degradation and catastrophic type failures. Observing the ratio of reject rates of burn-in

to bake (relative effectiveness ratio), it appears that burn-in is more effective than bake for all classes of semiconductor devices.

RESULTS OF SCREENING RELATED TO MANUFACTURING PROCESS

An analysis of the data was made relating relative effectiveness of burn-in and bake to the processes employed in the manufacture of semiconductor devices. These processes are described in the semiconductor technical literature and those used in Nimbus applications form a good cross-section of those used by the semiconductor industry.[4] Table 4 indicates the results for silicon transistors.

TABLE 1

SUMMARY OF SILICON TRANSISTORS

	BURN-IN				BAKE				
Class	No.of Types	Units	Rej.	% Rej.	No.ofTypes	Units	Rej.	% Rej.	RER
NPN	27	4146	387	9.3	26	7487	182	2.4	3.8
PNP	15	2407	381	15.8	13	4779	100	2.1	7.6
TOTAL	42	6553	768	11.7	39	12266	282	2.3	5.1

TABLE 2

SUMMARY OF GERMANIUM TRANSISTORS

	BURN-IN				BAKE				
Class	No.of Types	Units	Rej.	% Rej.	No.of Types	Units	Rej.	% Rej.	RER
NPN	1	31	1	3.2	0	-	-	-	-
PNP	9	2534	207	8.2	8	4036	33	0.8	10.0
TOTAL	10	2565	208	8.1	8	4036	33	0.8	10.1

TABLE 3

SUMMARY OF SILICON AND GERMANIUM DIODES

	Burn-in				Bake				
Type	No of Types	Units	Rej	%Rej	No of types	Units	Rej	%Rej	RER
Silicon	78	17404	380	2.2	75	26906	370	1.4	1.5
Germanium	1	105	12	11.4	1	492	4	0.8	14.3

TABLE 4

SILICON TRANSISTOR SCREENING RESULTS BY MANUFACTURING PROCESS

A. NPN TYPES

	Burn-in				Bake				
	No of Types	Units	Rej	%Rej	No of Types	Units	Rej	%Rej	RER
Grown-Diff	1	319	48	15.1	3	55	8	14.5	1.0
Grown	1	153	3	2.0	0	-	-	-	-
Mesa	10	1378	199	14.4	10	970	40	4.1	3.5
Planar	15	2296	137	6.0	14	6462	134	2.1	2.9

B. PNP TYPES

	Burn-in				Bake				
	No of Types	Units	Rej	%Rej	No of Types	Units	Rej	%Rej	RER
Alloy	9	507	70	13.8	6	824	19	2.3	6.0
Mesa	4	1775	286	16.1	6	3492	80	2.3	7.0
Planar	3	125	25	20.0	2	463	1	.2	100.0

The results indicate that the relative effectiveness ratio favors burn-in over bake for every process utilized for both NPN and PNP silicon transistor type. As expected the reject rate for NPN planar types was the lowest since the planar process minimizes semiconductor surface contamination which is a common failure mechanism in semiconductor devices.

The rejects that did occur on the planar devices were current gain degradation failures. The findings in this Table correspond with the findings of the semiconductor industry in the Minuteman program wherein NPN mesa and NPN planar transistor burn-in results were compared, [5] i.e., that planar types had fewer defectives than mesa types. The relative effectiveness ratio (mesa % rejects divided by planar % rejects) was 2.4 as shown in Table 4A.

Comparing NPN and PNP mesa types, the reject rate of PNP types was 1.1 times that for NPN types which tends to support the conjecture of users that shipments of PNP type mesas contain a greater proportion of defectives than NPN mesa types. This conjecture is further supported by the fact that it is easier to fabricate an NPN silicon transistor than a PNP silicon transistor. More NPN silicon types are manufactured than PNP types for this reason which is also reflected in the larger number of NPN types (twice as many) used in the Nimbus subsystems.

Table 5 indicates the results of testing germanium transistors. Here the sample does not reflect a full cross-section of available processes since germanium transistors were utilized only where silicon counterparts were not available at the time the Nimbus subsystems were designed and constructed. The largest number of germanium devices were of the micro-alloy diffused-base type (MADT) used extensively for low energy switching applications in the Nimbus Command clock subsystem.

TABLE 5

GERMANIUM TRANSISTORS SCREENING RESULTS
BY MANUFACTURING PROCESS

	Burn-in				Bake				
	No of Types	Units	Rej	%Rej	No of Types	Units	Rej	%Rej	RER
PNP TYPES									
Alloy	8	336	42	12.5	6	214	15	7.0	1.8
MADT	1	2190	165	7.5	2	3822	18	.5	15.0
Drift	1	8	0	0.0	0	-	-	-	-
NPN TYPES									
Grown Diff	1	31	1	3.2	0	0	-	-	-

The bake of the MADT types was at 55°C, a change from the specified 80°C.

Table 6 indicates the results for silicon and germanium diode screening as a function of manufacturing process.

TABLE 6
SILICON AND GERMANIUM DIODE SCREENING BY
PROCESS OF MANUFACTURE

	Burn-in				Bake				
	No of Types	Units	Rej	%Rej	No of Types	Units	Rej	%Rej	RER
Alloy	13	634	32	5.1	5	2580	80	3.1	1.6
Diffused	44	2781	202	7.3	56	4789	249	5.2	1.4
Mesa	1	70	5	7.1	1	278	2	0.7	10.3
Planar	9	11137	60	.5	12	19199	39	0.2	2.5
*Planar	8	1102	19	1.7	11	4599	35	0.8	2.1
**Gold Bonded	1	105	12	11.4	1	492	4	0.8	14.3
Alloy Diff	11	2782	81	2.9	1	60	0	-	-

*Type FD 177 excluded

**Germanium Diode

Again the relative effectiveness ratio favors burn-in over bake for each process of diode manufacture. The superiority of the planar process over others is indicated by the relatively low reject rate.

Results of Screening Related to Rated Power

When the data are arranged in terms of the rated power of devices at room temperature, the reject rate increases substantially with high rated power, The classification of power is as follows:

Low Power - Less than 1 watt
Medium Power - Between 1 and 10 watts
High Power - Equal to or greater than 10 watts

Tables 7 and 8 relate screening results as a function of power for NPN and PNP silicon and germanium transistors. Low power types include those used in AF, HF, and low noise and switching applications. Medium power types include differential amplifiers and switching transistors. Table 9 shows effectiveness of burn-in and bake methods for screening of diodes.

TABLE 7

SILICON TRANSISTOR SCREENING EFFECTIVENESS
BY POWER RATING

	Burn-in				Bake				
	No of Types	Units	Rej	%Rej	No of Types	Units	Rej	%Rej	RER
Low	5	580	55	9.5	5	920	22	2.4	4.0
Medium	18	3249	233	7.2	17	5998	137	2.3	3.1
High	4	317	99	31.2	4	569	23	4.0	7.8
Low	10	516	70	13.6	7	829	20	2.4	5.7
Medium	6	1891	311	16.4	7	3950	80	2.0	8.2
High	No high power PNP types used								

The higher reject rates for high power NPN transistors over medium and low power types in burn-in is attributable to the formation of hot spots, a failure mode that is not detectable by high temperature storage.

TABLE 8

GERMANIUM TRANSISTOR SCREEN EFFECTIVENESS
BY POWER RATING

	Burn-in				Bake				
	No of Types	Units	Rej	%Rej	No of Types	Units	Rej	%Rej	RER
PNP-Low	8	2293	180	7.5	6	3887	19	0.5	15.0
PNP-High	2	141	27	19.1	2	149	14	9.4	2.0
NPN-Low	1	31	1	3.2	0	-	-	-	-

TABLE 9

SILICON AND GERMANIUM DIODE SCREENING EFFECTIVENESS
BY POWER RATING

	Burn-in				Bake				
	No of Types	Units	Rej	%Rej	No of Types	Units	Rej	%Rej	RER
Low	74	17296	374	2.1	65	26538	359	1.4	1.5
Medium	4	108	6	5.5	6	229	5	2.2	2.5
High	0	-	-	-	4	139	6	4.3	-
*Low	1	105	12	11.4	1	492	4	0.8	14.3

*Germanium Diode

Percentage of Rejects as a Function of Time

The Nimbus Command Clock contractor measured relevant parameters at 100 hour intervals during the burn-in procedure. These measurements were made at room temperature after stabilization at 55°C. The results are shown in Table 10. Corresponding results in terms of percentage rejects for semiconductors subjected to a 1000 hour bake on identical semiconductor types are shown in Table 11.

TABLE 10

BURN-IN TEST RESULTS

Test Time (Hour)	Transistors (3468) (3416 Tested)		Diodes (10,728 Tested)	
	No. Rej	Cum % Rej	No. Rej	Cum % Rej
100	188	5.41	38	.35
200	57	7.06	14	.48
300	42	8.28	12	.60

TABLE II

BAKE TEST RESULTS

Test Tume (Hours)	Transistors (5086 Tested)		Diodes (1545 Tested)	
	No Rej	%Rej	No Rej	%Rej
1000	66	1.30	14	.09

Figure 1 is a graphical presentation of these results. It would appear from this graph that the cumulative percent rejects is still on the increase after 300 hours of burn-in time, and this is probably true. However data on burn-in test fallout recently reported [6] which is reproduced in Figure 1 indicates that for conventional diodes and transistors, the fallout of defectives increases by only 1% between 300 and 1000 hours for transistors and by only 0.8% for diodes for the same time interval.

A graph of percent rejects as a function of time is shown in Figure 2. It is quite evident that the "infant mortality" portions of the curves have been passed.

Significance of Results

With one exception, namely, the screening results of the NPN Silicon grown diffused transistor, the differences in the rejection rates of burn-in and bake techniques displayed in Tables 1 through 11 are statistically significant at confidence levels greater than 99 percent. The hypothesis tested was that the percentage of defects found using the 300-hr burn-in method is the same as the percentage of defects found using the 1000-hr bake method. Rejection of this hypothesis was used to support the engineering judgment that a 300-hr burn-in is indeed superior to a 1000-hr bake program.

Demonstration of the superiority of burn-in over bake rests to a large extent on the true percentage of semiconductors which are defective among those submitted for testing. Where the true percent defect is small, large numbers of devices must be submitted for testing using both methods to statistically demonstrate a difference in the effectiveness of the tests in screening out defective devices.

One type of semiconductor which appears to comprise a small percentage of defectives or at least comprise defectives which elude detection using either test method is the rated low power silicon diode FD177. As can be seen from the listing under Silicon Diode, Appendix C, 10035 diodes of this type were burned in for 300 hours with only 41 defectives showing up. A comparable number, 14600 when subjected to 1000 hours of high temperature storage, produced only 4 defectives. These results are statistically significant as indicated in the listing; however, if added in to the totals for all the rated low power diodes they tend to depress the overall percent defectives found in testing diodes of this type which does not appear to be the case. For this reason, the test findings for silicon diodes is summarized with and without the FD177 type included.

Appendix A lists all the semiconductors tested under the Nimbus Program and the number of defects found among the number tested of each type and the kind of test used (i.e., burn-in or bake). It includes those tested under both kinds of tests and those tested using the burn-in method only and those using the bake method only. For the types screeded using both methods, the maximum probability Q of noting a difference in the number of defects greater than the observed difference is listed. The equation for computing maximum Q is given in Appendix B.

In the comparison of the percent defectives found by each test method, it was assumed that the probabilities of a defective being submitted for either kind of test are the same. It is realized that this might not be the case since semiconductors of a particular type may have been processed at different times and under different processing conditions.

Thus in selecting what appeared to be the better of the two types of screening, there remains the question of which techniques, if either, was favored by the percent defectives among the devices submitted for test. There is no reason, however, to believe that in this respect either kind of test was inadvertantly given an advantage.

Comparison of Screening Effectiveness by Class of Semiconductor Device, Rated Power, and Manufacturing Process

Under the supposition that the same class of devices similar with respect to rated power and made under the same manufacturing process include substantially the same percent defectives on the average, the percentages of devices found to be defective using each kind of test are compared. The comparison of percent defectives between tests for each class, rated power, and manufacturing process are summarized in Appendix C. Again listed with each of these summaries is the maximum probability that burn-in is not superior to bake as evidenced by the sample defect rates. These results likely reflect a more stable situation in which the true percent defects submitted for either test are close. This supposition is based on the fact that the device when categorized by class, rated power, and process are relatively large in number thus tending to more nearly represent defects amont manufacturing output over greater manufacturing time spans and under a variety of different manufacturing environments.

Conclusion:

It has been shown that burn-in of semiconductor devices at elevated temperatures for 300 hours is more effective as a screening technique than high temperature storage for longer time periods. This statement holds for all classes of semiconductor devices, processes of manufacture and rated power dissipation. Statistical testing of the hypotheses that bake screening was as effective as the burn-in technique was carried out using computer methods. Results verified that burn-in was a superior technique.

Acknowledgments:

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CODE KEY FOR APPENDICES A AND C

MANUFACTURING CODE

01	General Electric
02	Fairchild
03	RCA
04	Texas Instruments
05	Delco
06	Raytheon
07	Philco
08	Sperry
09	Hughes
10	Motorola
11	Clevite
12	Wells
13	Hoffman
14	Continental Device Corp.
15	Transitron
16	IRC International Rectifier
17	Western Semiconductor
18	TRW (formerly PSI)
19	AMELCO
20	Computer Diode Corp.
21	Sylvania
22	General Instrument

PROCESS CODE

1	Grown diffused
2	Mesa
3	Planar
4	Alloy
5	Drift or Alloy Diffused
6	MADT
7	Diffused
8	Grown
9	Gold Bonded

POWER CODE

1	Less than 1 watt
2	Between 1 watt and 10 watts
3	Equal to or more than 10 watts

CLASSIFICATION CODE

A	NPN-SI Transistor
B	PNP-SI Transistor
C	PNP-GE Transistor
D	Silicon Diode
E	Germanium Diode
F	NPN-GE Transistor

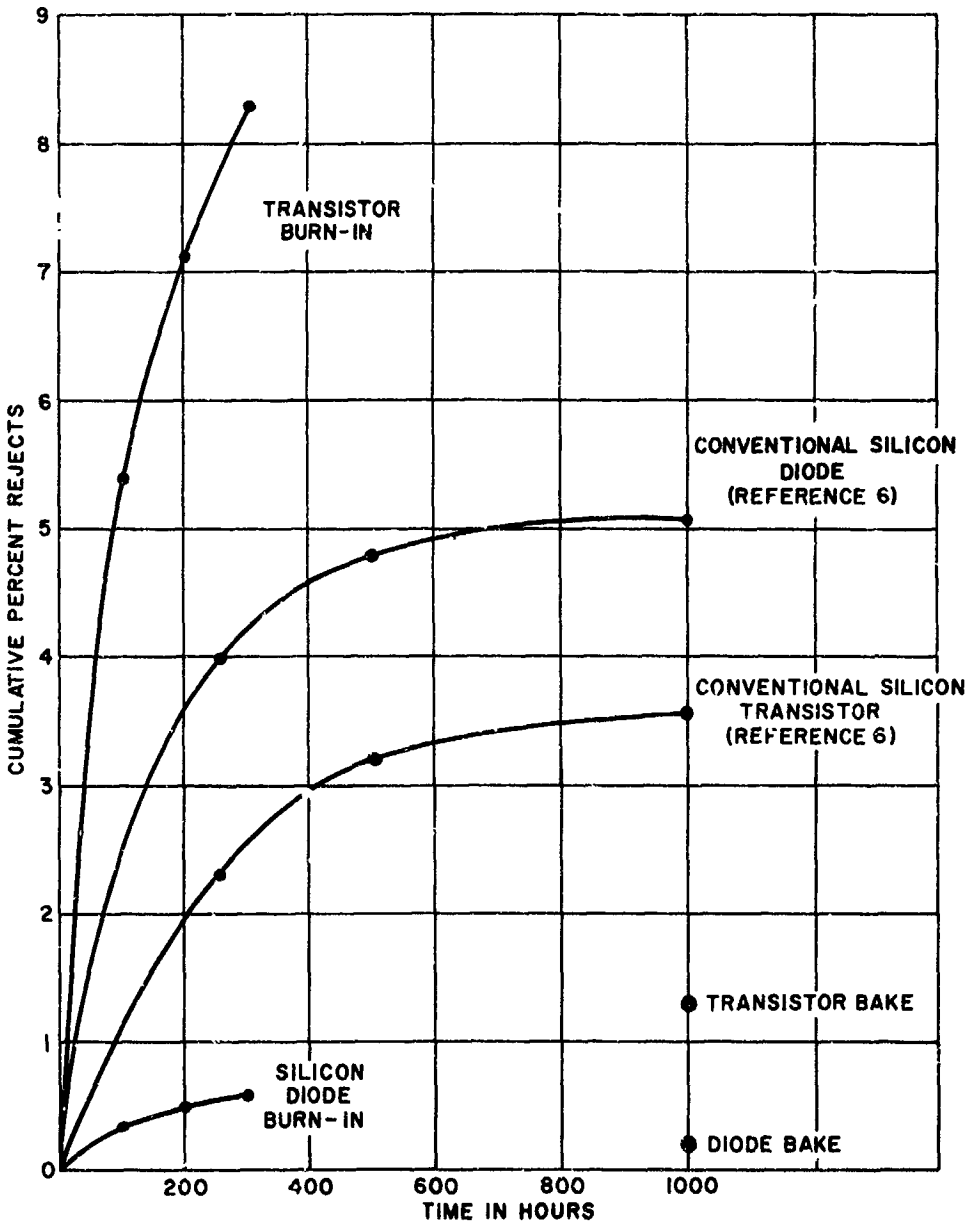

Figure 1-Cumulative Percent Rejects as a Function of Time

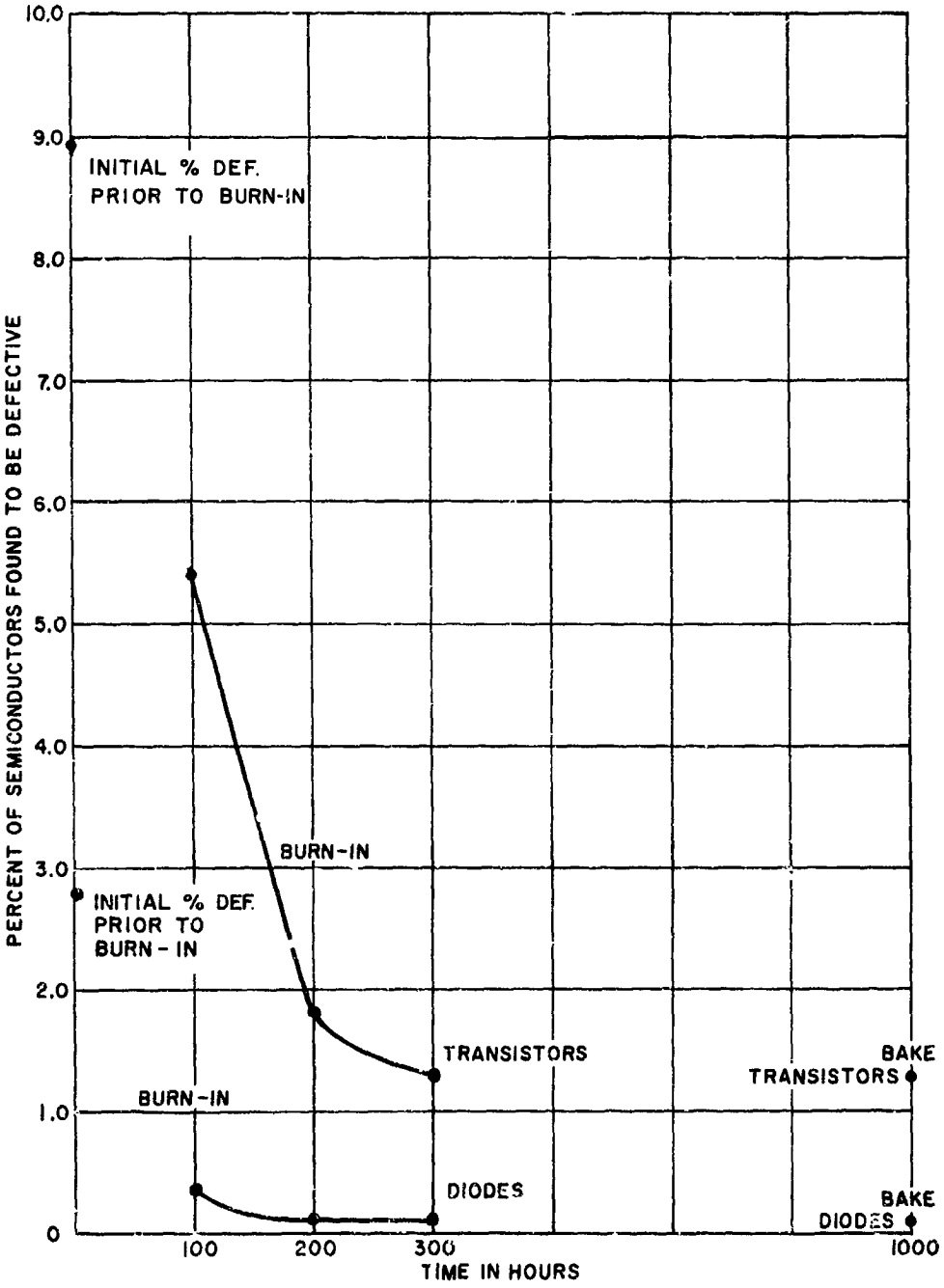

Figure 2–Percent Rejects of Semiconductors as a Function of Time

APPENDIX A

ALPHANUMERIC LISTING OF SEMICONDUCTOR DEVICES

SILICON NPN TRANSISTORS

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results			Bake Test Results			Max. Prob.
				No. Tested	No. Def.	% Defects	No. Tested	No. Def.	% Defects	
2N335A	01	1	1	319	48	15.1	33	6	18.2	.576
2N489	01	1	1	0	0	00.0	10	1	10.0	-
2N657	02	2	2	79	4	05.1	0	0	00.0	-
2N696	02	2	2	0	0	00.0	92	1	01.1	-
2N697	02	2	2	852	76	08.9	50	0	00.0	.005
2N699	03	3	2	8	1	12.5	0	0	00.0	-
2N699	02	2	2	0	0	00.0	75	0	00.0	-
2N706	02	2	2	87	10	11.5	0	0	00.0	-
2N706A	04	2	2	13	0	00.0	22	2	09.1	1.000
2N708	02	3	2	50	3	06.0	0	0	00.0	-
2N718A	02	3	2	471	15	03.1	2238	25	01.1	.000
2N718A	04	3	2	62	2	03.2	0	0	0	
2N720A	02	3	2	0	0	00.0	30	0	00.0	-
2N743	04	2	2	0	0	00.0	90	12	13.3	-
2N753	10	2	2	10	0	00.0	0	0	00.0	-
2N753	14	2	2	0	0	00.0	72	2	02.8	-
2N910	02	3	2	0	0	00.0	48	0	00.0	-
2N911	02	3	2	0	0	00.0	30	1	03.3	-
2N916	02	3	2	376	42	11.2	1963	64	03.3	.000
2N929	04	3	1	14	0	00.0	80	0	00.0	.000

SILICON NPN TRANSISTORS (Cont.)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	No. Def.	% Defects	Bake Test Results No. Tested	No. Def.	% Defects	Max. Prob.
2N930	04	3	1	72	2	02.8	775	12	01.6	.217
2N956	02	3	2	41	1	02.4	250	0	00.0	.047
2N1248	08	1	1	153	3	02.0	0	0	00.0	-
2N1485	03	2	3	129	36	27.9	349	17	04.9	.000
2N1486	03	2	3	59	24	40.7	50	1	02.0	.000
2N1489	03	2	3	80	30	37.5	44	2	04.6	.000
2N1490	03	2	3	49	9	18.4	126	3	02.4	.000
2N1613	02	3	2	396	9	02.3	836	20	02.4	.365
2N1613	03	3	2	0	0	00.0	100	0	00.0	-
2N1671B	01	1	1	0	0	00.0	12	1	08.3	-
2N1708	03	3	2	0	0	00.0	30	0	00.0	-
2N1711	02	3	2	134	10	07.5	36	8	22.2	.943
2N1890	02	3	2	30	0	00.0	0	0	00.0	-
2N2060	02	3	2	12	0	00.0	36	2	05.6	1.000
2N2341	05	2	2	20	10	50.	0	0	00.0	-
2N2369	02	3	2	445	38	08.5	0	0	00.0	-
2N2432	04	3	1	22	2	09.1	10	2	20.0	.708
2N2453	19	3	2	63	9	14.3	0	0	00.0	-
2N2898	03	3	2	100	3	03.0	0	0	00.0	-

SILICON PNP TRANSISTORS

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	Burn-in Test Results No. Def.	Burn-in Test Results % Defects	Bake Test Results No. Tested	Bake Test Results No. Def.	Bake Test Results % Defects	Max. Prob.
2N329A	06	4	1	0	0	00.0	142	4	02.8	-
2N495	07	4	1	47	0	00.0	102	2	02.0	1.000
2N722	02	2	2	323	54	16.7	1823	9	00.5	.000
2N727	04	2	2	9	0	00.0	25	4	16.0	1.000
2N861	07	4	1	29	0	00.0	0	0	00.0	-
2N862	07	4	1	98	2	02.0	155	0	00.0	.060
2N869	02	3	2	74	9	12.2	453	1	00.2	.000
2N943	08	4	1	46	15	32.6	200	2	01.0	.000
2N945	08	4	1	93	36	38.7	75	0	00.0	.000
2N995	02	3	2	13	3	23.1	10	0	00.0	.061
2N1131	02	2	2	0	0	00.0	1067	38	03.6	-
2N1132	02	2	2	1434	232	16.2	472	28	05.9	.000
2N1132	04	2	2	0	0	00.0	100	0	00.0	-
2N1234	09	4	1	9	0	00.0	0	0	00.0	-
2N1259	09	2	1	9	0	00.0	5	1	20.0	1.000
2N1656	06	4	1	170	17	10.0	150	11	07.3	.106
2N2551	09	4	1	15	0	00.0	0	0	00.0	-
2N2593	08	3	2	38	13	34.2	0	0	00.0	-

GERMANIUM PNP TRANSISTORS

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results			Bake Test Results			Max. Prob
				No. Tested	No. Def.	% Defects	No. Tested	No. Def.	% Defects	
2N174A	05	4	3	109	11	10.1	76	3	04.0	.035
2N278	05	4	1	46	11	23.9	0	0	00.0	-
2N384	03	5	1	8	0	00.0	0	0	00.0	-
2N396A	01	4	1	45	4	08.9	10	1	10.0	.5
2N417	06	4	1	0	0	00.0	5	0	00.0	-
2N501A	07	6	1	0	0	00.0	43	0	00.0	-
2N526	01	4	1	13	0	00.0	30	0	00.0	-
2N768	07	6	1	2190	165	07.5	3779	18	00.5	.000
2N1115	01	4	1	0	0	00.0	20	0	00.0	-
2N1303	01	4	1	20	0	00.0	0	0	00.0	-
2N1303	04	4	1	13	0	00.0	0	0	00.0	-
2N1358	05	4	1	58	0	00.0	0	0	00.0	-
2N1547A	10	4	3	0	0	00.0	73	11	15.1	-
2N1762	11	4	3	32	16	50.0	0	0	00.0	-

SILICON DIODES

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	No. Def.	% Defects	Bake Test Results No. Tested	No. Def.	% Defects	Max. Prob.
1N251	14	5	1	480	23	04.8	0	0	00.0	-
1N429	13	4	1	7	0	00.0	7	0	00.0	[illegible]
1N457	02	3	1	0	0	00.0	1057	1	00.1	-
1N457	15	4	1	357	13	03.6	2389	77	03.2	.220
1N458	02	3	1	8	0	00.0	0	0	00.0	-
1N458	11	7	1	0	0	00.0	91	0	00.0	-
1N458	12	7	1	0	0	00.0	38	0	00.0	-
1N482A	04	7	1	0	0	00.0	34	0	00.0	-
1N484B	04	7	1	0	0	00.0	83	1	01.2	-
1N487A	04	7	1	0	0	00.0	20	0	00.0	-
1N538	01	4	1	20	3	15.0	0	0	00.0	-
1N538	04	7	1	21	2	09.5	221	2	00.9	.013
1N625	02	3	1	0	0	00.0	48	2	04.2	-
1N643A	14	5	1	928	5	00.5	0	0	00.0	-
1N645	04	7	1	660	94	14.2	1428	142	09.9	.001
1N646	04	7	1	21	0	00.0	69	1	01.5	1.000
1N647	04	7	1	571	17	03.0	0	0	00.0	-
1N648	15	7	1	0	0	00.0	321	2	00.6	-
1N658	20	7	1	5	0	00.0	0	0	00.0	-
1N658	18	7	1	125	2	01.6	0	0	00.0	-
1N659	02	3	1	18	0	00.0	131	0	00.0	1.000
1N715A	15	7	1	5	0	00.0	12	1	08.3	1.000
1N721A	14	5	1	5	0	00.0	0	0	00.0	-

SILICON DIODES (Cont.)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results			Bake Test Results			Max. Prob.
				No. Tested	No. Def.	% Defects	No. Tested	No. Def.	% Defects	
1N746A	10	4	1	46	0	00.0	26	3	11.5	1.000
1N746A	18	7	1	0	0	00.0	14	0	00.0	-
1N750A	10	4	1	40	0	00.0	0	0	00.0	-
1N751	13	7	1	9	0	00.0	0	0	00.0	-
1N751A	14	5	1	353	19	05.4	0	0	00.0	-
1N751A	04	7	1	11	0	00.0	70	0	00.0	1.000
1N752A	13	7	1	9	0	00.0	0	0	00.0	-
1N752A	04	7	1	0	0	00.0	40	0	00.0	-
1N753A	14	5	1	10	0	00.0	0	0	00.0	-
1N753A	04	7	1	17	0	00.0	40	1	02.5	.975
1N754	10	4	1	25	0	00.0	0	0	00.0	-
1N754A	14	5	1	30	2	06.7	0	0	00.0	-
1N754A	04	7	1	43	6	14.0	26	0	00.0	.017
1N755A	14	5	1	374	13	03.5	0	0	00.0	-
1N756	04	7	1	39	12	30.8	0	0	00.0	-
1N756A	14	5	1	52	0	00.0	0	0	00.0	-
1N756A	04	7	1	0	0	00.0	198	0	00.0	-
1N757	10	4	1	10	0	00.0	0	0	00.0	
1N758A	10	4	1	9	0	00.0	0	0	00.0	
1N758A	14	5	1	511	6	03.1	0	0	00.0	-
1N759A	13	7	1	9	0	00.0	0	0	00.0	-
1N763	15	7	1	9	2	33.3	0	0	00.0	-
1N763A	15	7	1	0	0	00.0	193	5	02.6	-

SILICON DIODES (Cont.)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	No. Def.	% Defects	Bake Test Results No. Tested	No. Def.	% Defects	Max. Prob.
1N764	15	7	1	38	3	07.9	71	0	00.0	.011
1N765	15	7	1	0	0	00.0	69	2	02.9	-
1N791	02	3	1	31	2	06.5	423	15	03.6	.188
1N816	15	7	1	53	1	01.9	447	21	04.7	.800
1N821	15	7	1	8	2	25.0	60	15	25.0	.433
1N823	15	7	1	8	1	12.5	36	2	05.6	.248
1N823A	10	7	1	75	8	10.7	75	4	05.3	.068
1N827	15	7	1	4	0	00.0	0	0	00.0	-
1N914	04	2	1	40	0	00.0	0	0	00.0	-
1N914B	04	2	1	30	5	16.7	278	2	00.7	.000
1N935	10	7	1	0	0	00.0	27	9	33.3	-
1N936A	10	7	1	0	0	00.0	15	3	20.0	-
1N937	10	7	1	15	0	00.0	33	0	00.0	1.000
1N937A	10	7	1	0	0	00.0	8	1	12.5	-
1N938B	10	7	1	18	0	00.0	37	0	00.0	1.000
1N941B	10	7	1	45	0	00.0	27	7	25.9	1.000
1N942A	10	7	1	0	0	00.0	14	2	14.3	-
1N943	10	7	1	10	0	00.0	10	0	00.0	1.000
1N943B	10	7	1	162	1	00.6	55	2	03.6	.853
1N945	10	7	1	23	4	17.4	0	0	00.0	-
1N953A	09	7	1	32	1	03.1	0	0	00.0	-
1N959B	10	7	1	0	0	00.0	18	1	05.6	-
1N962B	10	7	1	8	1	12.5	10	1	10.0	.423

SILICON DIODES (Cont.)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results: No. Tested	No. Def.	% Defects	Bake Test Results: No. Tested	No. Def.	% Defects	Max. Prob.
1N963	10	7	1	5	0	00.0	0	0	00.0	-
1N963B	10	7	1	42	3	07.1	24	0	00.0	.106
1N964B	10	7	1	42	2	04.8	38	0	00.0	.114
1N966B	10	7	1	0	0	00.0	10	0	00.0	-
1N972	10	7	1	56	0	00.0	0	0	00.0	-
1N978A	10	7	1	0	0	00.0	105	1	01.0	-
1N1124A	04	7	2	0	0	00.0	27	0	00.0	-
1N1509	16	4	1	12	4	33.3	4	0	00.0	.122
1N1513	16	4	1	6	4	00.7	0	0	00.0	-
1N1516	16	4	1	8	0	00.0	0	0	00.0	-
1N2988B	10	7	3	0	0	00.0	64	3	04.7	-
1N2992B	10	7	3	0	0	00.0	20	3	15.0	-
1N2999B	10	7	3	0	0	00.0	24	0	00.0	-
1N3001B	10	7	3	0	0	00.0	31	0	00.0	-
1N3016B	10	7	2	0	0	00.0	79	4	05.1	-
1N3020B	10	7	2	10	0	00.0	70	1	01.4	1.000
1N3021	10	7	2	19	0	00.0	0	0	00.0	-
1N3021B	10	7	2	0	0	00.0	4	0	00.0	-
1N3024B	10	7	2	39	3	07.7	17	0	00.0	.15.
1N3026B	10	7	2	40	3	07.5	32	0	00.0	.063
1N3071	02	3	1	157	9	05.7	138	0	00.0	.003
1N3154	14	5	1	25	1	04.0	0	0	00.0	-
1N3154	14	7	1	5	0	00.0	17	1	05.9	1.000

SILICON DIODES (Cont.)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	No. Def.	% Defects	Bake Test Results No. Tested	No. Def.	% Defects	Max. Prob.
1N3156	10	7	1	5	0	00.0	9	0	00.0	1.000
1N3156	10	7	1	15	0	00.0	0	0	00.0	-
1N3189	15	7	1	183	22	12.0	143	1	00.7	.000
1N3730	06	7	1	240	11	04.6	33	1	03.0	.351
650CO	04	4	1	50	2	04.0	154	0	00.0	.020
CD32132	14	5	1	14	2	14.3	0	0	00.0	-
FA2000	02	3	1	0	[illegible]	00.0	130	0	00.0	-
FD100	02	3	1	0	[illegible]	00.0	334	2	00.6	-
FD101	02	3	1	451	4	00.9	1499	7	00.5	.103
FD177	02	3	1	10035	41	00.4	14600	4	00.0	.000
FD200	02	3	1	24	0	00.0	82	2	02.4	1.000
FD292	02	3	1	403	4	01.0	743	5	00.7	.191
FD300	02	3	1	10	0	00.0	14	1	07.1	1.000
MZ17	16	4	1	44	6	13.6	0	0	00.0	-
PS2416	18	7	1	0	0	00.0	40	1	02.5	-
PS2417	18	7	1	7	0	00.0	7	0	00.0	1.000
PS2419	18	7	1	0	0	00.0	73	8	11.0	-
PS8859	18	7	1	4	0	00.0	0	0	00.0	-
PS8890	18	7	1	2	1	50.0	0	0	00.0	-
PS8891	18	7	1	1	0	00.0	0	0	00.0	-
PS8892	18	7	1	3	0	00.0	0	0	00.0	-
TMD02A	15	7	1	10	0	00.0	12	0	00.0	1.000
WZ524	17	5	1	0	0	00.0	60	0	00.0	-

GERMANIUM DIODE

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results: No. Tested	Burn-in Test Results: No. Def.	Burn-in Test Results: % Defects	Bake Test Results: No. Tested	Bake Test Results: No. Def.	Bake Test Results: % Defects	Max. Prob.
1N277	06	9	1	0	0	00.0	35	3	08.6	-
1N277	11	9	1	0	0	00.0	340	0	00.0	-
1N277	12	9	1	0	0	00.0	117	1	00.9	-
1N277	22	9	1	72	9	12.5	0	0	00.0	-
1N277	21	9	1	33	3	09.1	0	0	00.0	-

GERMANIUM NPN TRANSISTOR

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results: No. Tested	Burn-in Test Results: No. Def.	Burn-in Test Results: % Defects	Bake Test Results: No. Tested	Bake Test Results: No. Def.	Bake Test Results: % Defects	Max. Prob.
2N635A	01	4	1	31	1	03.2	0	0	00.0	-

APPENDIX B

PROCEDURE FOR DETERMINING LEVEL OF DIFFERENCE BETWEEN BURN-IN AND BAKE SCREENING RESULTS

Based on engineering considerations, it is asserted that the burn-in screening technique is not inferior to the bake screening technique in culling out defective semiconductors. This assertion rests principally on the fact that certain types of defectives cannot be found by subjecting the semiconductor to a bake program whereas they could be if subjected to a burn-in program.

On the above assertion, the hypothesis is that the bake screening technique is as effective as the burn-in technique, was tested statistically. Since the number of semiconductors subjected to burn-in and bake varies considerably in number by type of semiconductor (this variation requires much in the way of computational effort), it was decided to make the statistical tests using an IBM 1620 computer.

Maximum Probability that Bake Screening Is as Good as Burn-In Screening in Culling Out Defectives

Let

- p = probability that a defective semiconductor by some defintion is introduced for test screening.
- π_1 = probability that burn-in screening will detect a defective
- π_2 = probability that bake screening will detect a defective
- n_1 = number of semiconductors (defectives and non-defectives) which are subjected to burn-in
- n_2 = number of semiconductors (defectives and non-defectives) which are subjected to bake
- d_1 = number of defectives found among the n_1 screened using the burn-in method
- d_2 = number of defectives found among the n_2 screened using the bake method.

Testing the hypothesis that $\pi_1 = \pi_2$, we have for the probability Q that d_1 or more defectives are found in burning-in n_1 semiconductors and d_2 or less defectives are found in baking n_2 semiconductors,

$$Q = \sum_{x_1=d_1}^{n_1} \binom{n_1}{x_1} (p\pi)^{x_1} (1-p\pi)^{n_1-x_1} \cdot \sum_{x_2=0}^{d_2} \binom{n_2}{x_2} (p\pi)^{x_2} (1-p\pi)^{n_2-x_2}$$

Q is thus the probability of observing a difference greater than or equal to $d_1 - d_2$ from samples of n_1 and n_2, respectively. Since p and π cannot be estimated individually from the screening results the value of the product $p\pi$ is selected such that Q, the probability of the observed difference $d_1 - d_2$ being exceeded under the hypothesis $\pi_1 = \pi_2 = \pi$, is maximum. If maximum Q is small, say less than .05, we reject the hypothesis that $\pi_1 = \pi_2$ and accept the alternative; namely, $\pi_1 > \pi_2$; i.e., burn-in is significantly better than bake at a confidence level $\geq$ 95 percent in screening out defective semicondutors.

APPENDIX C

SEMICONDUCTOR DEVICES LISTED
by PROCESS, POWER, AND CLASS

SILICON NPN TRANSISTORS
(CLASS A)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results			Bake Test Results			Max. Prob.
				No. Tested	No. Def.	% Defects	No. Tested	No. Def.	% Defects	
2N335A	01	1	1	319	48	15.1	33	6	18.2	.57
2N489	01	1	1	0	0	00.0	10	1	10.0	-
2N1671B	01	1	1	0	0	00.0	12	1	08.3	-
PROCESS-POWER		1	1	319	48	15.1	55	8	14.5	.338
2N929	04	3	1	14	0	00.0	80	0	00.0	1.000
2N930	04	3	1	72	2	02.8	775	12	01.6	.217
2N2432	04	3	1	22	2	09.1	10	2	20.0	.708
PROCESS-POWER		3	1	108	4	03.7	865	14	01.6	.052
2N1248	04	8	1	153	3	02.0	0	0	00.0	-
PROCESS-POWER		8	1	153	3	02.0	0	0	00.0	-
POWER CLASS 1				580	55	09.5	920	22	02.3	.003

SILICON NPN TRANSITORS (Cont.)
(CLASS A)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	No. Def.	% Defects	Bake Test Results No. Tested	No. Def.	% Defects	Max. Prob.
2N657	02	2	2	79	4	05.1	0	0	00.0	-
2N696	02	2	2	0	0	00.0	92	1	01.1	-
2N697	02	2	2	852	76	08.9	50	0	00.0	.005
2N699	02	2	2	0	0	00.0	75	0	00.0	-
2N706	02	2	2	87	10	11.5	0	0	00.0	-
2N706A	04	2	2	13	0	00.0	22	2	09.1	1.000
2N743	04	2	2	0	0	00.0	90	12	13.3	-
2N753	10	2	2	10	0	00.0	0	0	00.0	-
2N753	14	2	2	0	0	00.0	72	2	02.8	-
2N2341	05	2	2	20	10	50.	0	0	00.0	-
PROCESS-POWER		2	2	1061	100	09.4	401	17	04.2	.000

SILICON NPN TRANSISTORS (Cont.)
(CLASS A)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	Burn-in Test Results No. Def.	Burn-in Test Results % Defects	Bake Test Results No. Tested	Bake Test Results No. Def.	Bake Test Results % Defects	Max. Prob.
2N699	03	3	2	8	1	12.5	0	0	00.0	-
2N708	02	3	2	50	3	06.0	0	0	00.0	-
2N718A	02	3	2	471	15	03.1	2238	25	01.1	.000
2N718A	04	3	2	62	2	3.2	0	0	0	-
2N720A	02	3	2	0	0	00.0	30	0	00.0	-
2N910	02	3	2	0	0	00.0	48	0	00.0	-
2N911	02	3	2	0	0	00.0	30	1	03.3	-
2N916	02	3	2	376	42	11.2	1963	64	03.3	.000
2N956	02	3	2	41	1	02.4	250	0	00.0	.047
2N1613	02	3	2	396	9	02.3	836	20	02.4	.365
2N1613	03	3	2	0	0	00.0	100	0	00.0	-
2N1708	03	3	2	0	0	00.0	30	0	00.0	-
2N1711	02	3	2	134	10	07.5	36	8	22.2	.943
2N1890	02	3	2	30	0	00.0	0	0	00.0	-
2N2060	02	3	2	12	0	00.0	36	2	05.6	.000
2N2369	02	3	2	445	38	08.5	0	0	00.0	-
2N2453	19	3	2	63	9	14.3	0	0	00.0	-
2N2898	03	3	2	100	3	03.0	0	0	00.0	-
PROCESS-POWER		3	2	2188	133	6.1	5597	120	02.0	.00
POWER CLASS 2				3249	233	07.1	5998	137	02.2	.00

SILICON NPN TRANSISTORS (Cont.)
(CLASS A)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results			Bake Test Results			Max. Prob.
				No. Tested	No. Def.	% Defects	No. Tested	No. Def.	% Defects	
2N1485	03	2	3	129	36	27.9	349	17	04.9	.000
2N1486	03	2	3	59	24	40.7	50	1	02.0	.000
2N1489	03	2	3	80	30	37.5	44	2	04.6	.000
2N1490	03	2	3	49	9	18.4	126	3	02.4	.000
PROCESS-POWER		2	3	317	99	31.2	569	23	04.0	.000
POWER CLASS 3				317	99	31.2	569	23	04.0	.000
CLASS A				4146	387	09.3	7487	182	02.4	.000

SILICON PNP TRANSISTORS
(CLASS B)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	Burn-in Test Results No. Def.	Burn-in Test Results % Defects	Bake Test Results No. Tested	Bake Test Results No. Def.	Bake Test Results % Defects	Max. Prob.
2N1259	09	2	1	9	0	00.0	5	1	20.0	1.000
PROCESS-POWER		2	1	9	0	00.0	5	1	20.0	1.000
2N329A	06	4	1	0	0	00.0	142	4	02.8	-
2N495	07	4	1	47	0	00.0	102	2	02.0	1.000
2N861	07	4	1	29	0	00.0	0	0	00.0	-
2N862	07	4	1	98	2	02.0	155	0	00.0	.060
2N943	08	4	1	46	15	32.6	200	2	01.0	.000
2N945	08	4	1	93	36	38.7	75	0	00.0	.000
2N1234	09	4	1	9	0	00.0	0	0	00.0	-
2N1656	06	4	1	170	17	10.0	150	11	07.3	.196
2N2551	09	4	1	15	0	00.0	0	0	00.0	-
PROCESS-POWER		4	1	507	70	13.8	824	19	02.3	.000
POWER CLASS 1				516	70	13.6	829	20	02.4	.000

SILICON PNP TRANSISTORS (Cont.)
(CLASS B)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	No. Def.	% Defects	Bake Test Results No. Tested	No. Def.	% Defects	Max. Prob.
2N722	02	2	2	323	54	16.7	1823	9	00.5	.000
2N727	04	2	2	9	0	00.0	25	4	16.0	1.000
2N1131	02	2	2	0	0	00.0	1067	38	03.6	-
2N1132	02	2	2	1434	232	16.2	472	28	05.9	.000
2N1132	04	2	2	0	0	00.0	100	0	00.0	-
PROCESS-POWER		2	2	1766	286	16.1	3487	79	02.3	.000
2N869	02	3	2	74	9	12.2	453	1	00.2	.000
2N995	02	3	2	13	3	23.1	10	0	00.0	.061
2N2593	08	3	2	38	13	34.2	0	0	00.0	-
PROCESS-POWER		3	2	125	25	20.0	[illegible]	1	00.2	.000
POWER CLASS 2				1891	311	16.4	3950	80	02.0	.000
CLASS B				2407	381	15.8	4779	100	02.1	.000

GERMANIUM PNP TRANSISTORS
(CLASS C)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results			Bake Test Results			Max. Prob.
				No. Tested	No. Def.	% Defects	No. Tested	No. Def.	% Defects	
2N278	05	4	1	46	11	23.9	0	0	00.0	-
2N396A	01	4	1	45	4	08.9	10	1	10.0	.531
2N417	06	4	1	0	0	00.0	5	0	00.0	-
2N526	01	4	1	13	0	00.0	30	0	00.0	-
2N1115	01	4	1	0	0	00.0	20	0	00.0	-
2N1303	01	4	1	20	0	00.0	0	0	00.0	-
2N1303	04	4	1	13	0	00.0	0	0	00.0	-
2N1358	05	4	1	58	0	00.0	0	0	00.0	-
PROCESS-POWER		4	1	195	15	07.7	65	1	01.5	.021
2N384	03	5	1	8	0	00.0	0	0	00.0	-
PROCESS-POWER		5	1	8	0	00.0	0	0	00.0	1.000
2N501A	07	6	1	0	0	00.0	43	0	00.0	-
2N768	07	6	1	2190	165	07.5	3779	18	00.5	.000
PROCESS-POWER		6	1	2190	165	07.5	3822	18	00.5	.000
POWER CLASS 1				2393	207	08.7	3887	19	00.5	.000

GERMANIUM PNP TRANSISTORS (Cont.)
(CLASS C)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results			Bake Test Results			Max. Prob.
				No. Tested	No. Def.	% Defects	No. Tested	No. Def.	% Defects	
2N174A	05	4	3	109	11	10.1	76	3	04.0	.04
2N1547A	10	4	3	0	0	00.0	73	11	15.1	-
2N1762	11	4	3	32	16	50.0	0	0	00.0	-
PROCESS-POWER		4	3	141	27	19.1	149	14	09.4	.0
POWER CLASS 3				141	27	19.1	149	14	09.4	.004
CLASS C				2534	234	09.2	4036	33	00.8	.0

SILICON DIODES
(CLASS D)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	No. Def.	% Defects	Bake Test Results No. Tested	No. Def.	% Defects	Max. Prob.
1N914	04	2	1	40	0	00.0	0	0	00.0	-
1N914B	04	2	1	30	5	16.7	278	2	00.7	.000
PROCESS-POWER		2	1	70	5	07.1	278	2	00.7	.00
1N457	02	3	1	0	0	00.0	1057	1	00.1	-
1N458	02	3	1	8	0	00.0	0	0	00.0	-
1N625	02	3	1	0	0	00.0	48	2	04.2	-
1N659	02	3	1	18	0	00.0	131	0	00.0	.
1N791	02	3	1	31	2	06.5	423	15	03.6	.1
1N3071	02	3	1	157	9	05.7	138	0	00.0	.00
FA2000	02	3	1	0	0	00.0	130	0	00.0	-
FD100	02	3	1	0	0	00.0	334	2	00.6	-
FD101	02	3	1	451	4	00.9	1499	7	00.5	.
FD177	02	3	1	10035	41	00.4	14600	4	00.0	.
FD200	02	3	1	24	0	00.0	82	2	02.4	1.00
FD292	02	3	1	403	4	01.0	743	5	00.7	.19
FD300	02	3	1	10	0	00.0	14	1	07.1	1.000
PROCESS-POWER		3	1	11137	60	00.5	19199	39	00.2	.000
PROCESS-POWER *		3	1	1102	19	01.7	4599	35	00.8	.01

SILICON DIODES (Cont.)
(CLASS D)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results			Bake Test Results			Max. Prob.
				No. Tested	No. Def.	% Defects	No. Tested	No. Def.	% Defects	
1N429	13	4	1	7	0	00.0	7	0	00.0	1.000
1N457	15	4	1	357	13	03.6	2389	77	03.2	.220
1N538	01	4	1	20	3	15.0	0	0	00.0	-
1N746A	10	4	1	46	0	00.0	26	3	11.5	1.000
1N750A	10	4	1	40	0	00.0	0	0	00.0	-
1N754	10	4	1	25	0	00.0	0	0	00.0	-
1N757	10	4	1	10	0	00.0	0	0	00.0	-
1N758A	10	4	1	9	0	00.0	0	0	00.0	-
1N1509	16	4	1	12	4	33.3	4	0	00.0	.122
1N1513	16	4	1	6	4	00.7	0	0	00.0	-
1N1516	16	4	1	8	0	00.0	0	0	00.0	-
650CO	04	4	1	50	2	04.0	154	0	00.0	.027
MZ17	16	4	1	44	6	13.6	0	0	00.0	-
PROCESS-POWER		4	1	634	32	5.1	2580	80	03.1	.003

SILICON DIODES (Cont.)
(CLASS D)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	No. Def.	% Defects	Bake Test Results No. Tested	No. Def.	% Defects	Max. Prob.
1N251	14	5	1	480	23	04.8	0	0	00.0	-
1N643A	14	5	1	928	5	00.5	0	0	00.0	-
1N721A	14	5	1	5	0	00.0	0	0	00.0	-
1N751A	14	5	1	353	19	05.4	0	0	00.0	-
1N753A	14	5	1	10	0	00.0	0	0	00.0	-
1N754A	14	5	1	30	2	06.7	0	0	00.0	-
1N755A	14	5	1	374	13	03.5	0	0	00.0	-
1N756A	14	5	1	52	0	00.0	0	0	00.0	-
1N758A	14	5	1	511	16	03.1	0	0	00.0	-
1N3154	14	5	1	25	1	04.0	0	0	00.0	-
CD32132	14	5	1	14	2	14.3	0	0	00.0	-
WZ524	17	5	1	0	0	00.0	60	0	00.0	-
PROCESS-POWER		5	1	2791	81	02.9	60	0	00.0	.119

SILICON DIODES (Cont.)
(CLASS D)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	No. Def.	% Defects	Bake Test Results No. Tested	No. Def.	% Defects	Max. Prob.
1N458	11	7	1	0	0	00.0	91	0	00.0	-
1N458	12	7	1	0	0	00.0	38	0	00.0	-
1N482A	04	7	1	0	0	00.0	34	0	00.0	-
1N484B	04	7	1	0	0	00.0	83	1	01.2	-
1N487A	04	7	1	0	0	00.0	20	0	00.0	-
1N538	04	7	1	21	2	09.5	221	2	00.9	.013
1N645	04	7	1	660	94	14.2	1428	142	09.9	.001
1N646	04	7	1	21	0	00.0	69	1	01.5	1.000
1N647	04	7	1	571	17	03.0	0	0	00.0	-
1N648	15	7	1	0	0	00.0	321	2	00.6	-
1N658	20	7	1	5	0	00.0	0	0	00.0	-
1N658	18	7	1	125	2	01.6	0	0	00.0	-
1N715A	15	7	1	5	0	00.0	12	1	08.3	1.00
1N746A	18	7	1	0	0	00.0	14	0	00.0	-
1N751	13	7	1	9	0	00.0	0	0	00.0	-
1N751A	04	7	1	11	0	00.0	70	0	00.0	1.000
1N752A	04	7	1	0	0	00.0	40	0	00.0	-
1N752A	13	7	1	9	0	00.0	0	0	00.0	-
1N753A	04	7	1	17	0	00.0	40	1	02.5	.975
1N754A	04	7	1	43	6	14.0	26	0	00.0	.017
1N756	04	7	1	39	12	30.8	0	0	00.0	-
1N756A	04	7	1	0	0	00.0	198	0	00.0	-
1N759A	13	7	1	9	0	00.0	0	0	00.0	-
1N763	15	7	1	9	2	33.3	0	0	00.0	-

SILICON DIODES (Cont.)
(CLASS D)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results			Bake Test Results			Max. Prob.
				No. Tested	No. Def.	% Defects	No. Tested	No. Def.	% Defects	
1N763A	15	7	1	0	0	00.0	193	5	02.6	-
1N764	15	7	1	38	3	07.9	71	0	00.0	.011
1N765	15	7	1	0	0	00.0	69	2	02.9	-
1N816	15	7	1	53	1	01.9	447	21	04.7	.800
1N821	15	7	1	8	2	25.0	60	15	25.0	.433
1N823	15	7	1	8	1	12.5	36	2	05.6	.248
1N823A	10	7	1	75	8	10.7	75	4	05.3	.069
1N827	15	7	1	4	0	00.0	0	0	00.0	-
1N935	10	7	1	0	0	00.0	27	9	33.3	-
1N936A	10	7	1	0	0	00.0	15	3	20.0	-
1N937	10	7	1	15	0	00.0	33	0	00.0	1.000
1N937A	10	7	1	0	0	00.0	8	1	12.5	-
1N938B	10	7	1	18	0	00.0	37	0	00.0	.[illegible]
1N941B	10	7	1	45	0	00.0	27	7	25.9	.[illegible]
1N942A	10	7	1	0	0	00.0	14	2	[illegible]	[illegible]
1N943	10	7	1	10	0	00.0	10	0	[illegible]	[illegible]
1N943B	10	7	1	162	1	00.6	55	2	[illegible]	[illegible]
1N945	10	7	1	23	4	17.4	0	0	00.0	-
1N953A	09	7	1	32	1	03.1	0	0	00.0	-
1N959B	10	7	1	0	0	00.0	18	1	05.6	-
1N962B	10	7	1	8	1	12.5	10	1	10.0	.423
1N963	10	7	1	5	0	00.0	0	0	00.0	-
1N963B	10	7	1	42	3	07.1	24	0	00.0	.106
1N964B	10	7	1	42	2	04.8	38	0	00.0	.114

SILICON DIODES (Cont.)
(CLASS D)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	No. Def.	% Defects	Bake Test Results No. Tested	No. Def.	% Defects	Max. Prob.
1N966B	10	7	1	0	0	00.0	10	0	00.0	-
1N972	10	7	1	56	0	00.0	0	0	00.0	-
1N978A	10	7	1	0	0	00.0	105	1	01.0	-
1N3154	14	7	1	5	0	00.0	17	1	05.9	1.000
1N3156	10	7	1	5	0	00.0	9	0	00.0	1.000
1N3156	10	7	1	15	0	00.0	0	0	00.0	-
1N3189	15	7	1	183	22	12.0	143	1	00.7	.000
1N3730	06	7	1	240	11	04.6	33	1	03.0	.351
PS2416	18	7	1	0	0	00.0	40	1	02.5	-
PS2417	18	7	1	7	0	00.0	7	0	00.0	1.000
PS2419	18	7	1	0	0	00.0	73	8	11.0	-
PS8859	18	7	1	4	0	00.0	0	0	00.0	-
PS8890	18	7	1	2	1	50.0	0	0	00.0	-
PS8891	18	7	1	1	0	00.0	0	0	00.0	-
PS8892	18	7	1	3	0	00.0	0	0	00.0	-
TMD02A	15	7	1	10	0	00.0	12	0	00.0	1.000
PROCESS-POWER		7	1	2673	196	7.3	4421	238	05.4	.000
POWER CLASS 1				17296	371	02.1	26538	359	01.4	.000
POWER CLASS 1 (NO FD177)				7261	310	04.5	11938	355	03.0	.000

SILICON DIODES (Cont.)
(CLASS D)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	No. Def.	% Defects	Bake Test Results No. Tested	No. Def.	% Defects	Max. Prob.
1N1124A	04	7	2	0	0	00.0	27	0	00.0	-
1N3016B	10	7	2	0	0	00.0	79	4	05.1	-
1N3020B	10	7	2	10	0	00.0	70	1	01.4	1.000
1N3021	10	7	2	19	0	00.0	0	0	00.0	-
1N3021B	10	7	2	0	0	00.0	4	0	00.0	-
1N3024B	10	7	2	39	3	07.7	17	0	00.0	.154
1N3026B	10	7	2	40	3	07.5	32	0	00.0	.063
PROCESS-POWER		7	2	118	6	05.1	229	5	02.1	.046
POWER CLASS 2				118	6	05.1	229	5	02.1	.046
1N2988B	10	7	3	0	0	00.0	64	3	04.7	-
1N2992B	10	7	3	0	0	00.0	20	3	15.0	-
1N2999B	10	7	3	0	0	00.0	24	0	00.0	-
1N3001B	10	7	3	0	0	00.0	31	0	00.0	-
PROCESS-POWER		7	3	0	0	00.0	139	6	04.3	-
POWER CLASS 3				0	0	00.0	139	6	04.3	1.000
CLASS D				17414	377	02.2	26906	370	01.3	.000
CLASS D (NO FD177)				7379	336	04.6	12306	366	02.9	.000

GERMANIUM DIODES
(CLASS E)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	No. Def.	% Defects	Bake Test Results No. Tested	No. Def.	% Defects	Max. Prob.
1N277	06	9	1	0	0	00.0	35	3	08.6	-
1N277	11	9	1	0	0	00.0	340	0	00.0	-
1N277	12	9	1	0	0	00.0	117	1	00.9	-
1N277	22	9	1	72	9	12.5	0	0	00.0	-
1N277	21	9	1	33	3	09.1	0	0	00.0	-
PROCESS-POWER		9	1	105	12	11.4	492	4	00.8	.000
CLASS E				105	12	11.4	492	4	00.8	.000

GERMANIUM NPN TRANSISTOR
(CLASS F)

Type	Mfr Code	Mfr Proc.	Rated Power	Burn-in Test Results No. Tested	No. Def.	% Defects	Bake Test Results No. Tested	No. Def.	% Defects	Max. Prob.
2N635A	01	4	1	31	1	03.2	0	0	00.0	-
PROCESS-POWER		4	1	31	1	03.2	0	0	00.0	-
CLASS F				31	1	03.2	0	0	00.0	-