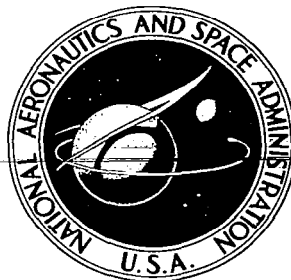


**NASA CONTRACTOR
REPORT**



009590



NASA CR-229

**PCM TELEMETRY:
A NEW APPROACH USING
ALL-MAGNETIC TECHNIQUES**

by C. H. Heckler, Jr., and J. A. Baer

Prepared under Contract No. NAS 1-3380 by
STANFORD RESEARCH INSTITUTE
Menlo Park, Calif.

for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • MAY 1965



PCM TELEMETRY: A NEW APPROACH USING
ALL-MAGNETIC TECHNIQUES

By C. H. Heckler, Jr., and J. A. Baer

Distribution of this report is provided in the interest of
information exchange. Responsibility for the contents
resides in the author or organization that prepared it.

Prepared under Contract No. NAS 1-3380 by
STANFORD RESEARCH INSTITUTE
Menlo Park, Calif.

for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

ABSTRACT

The feasibility of an all-magnetic PCM telemetry system has been studied and the logic design of a twelve-channel PCM telemetry system has been made. The design requires some seven hundred magnetic cores and fifty transistors. The system is completely digital, departing from the conventional design, which requires the amplification of analog signals. During this study, several novel magnetic circuits have been found. An investigation of the reliability of magnetic cores was also made. It has been found that three large producers of magnetic cores have no record of in-service failures for this class of element.

CONTENTS

ABSTRACT	iii
LIST OF ILLUSTRATIONS	vi
LIST OF TABLES	vii
I INTRODUCTION	1
II SUMMARY	5
III BACKGROUND	7
IV INVESTIGATIONS	11
A. Magnetic Circuits	11
1. Balanced Magnetic Comparator	11
2. MAD Circuits	18
3. All-Toroid Circuits	31
B. Driver Circuits	54
1. Weight Current Drivers	54
2. Timing Generator and Logic Drivers	57
C. Sense Amplifier	63
D. A Magnetically Implemented Telemetry System	63
1. Logic Description	63
2. System Specification	73
E. Reliability	75
V AREAS FOR FURTHER RESEARCH	79
APPENDIX A ARROW NOTATION	81
APPENDIX B CORE SIZE RELATIONS	83
APPENDIX C SYMBOLS	87
APPENDIX D PROGRAM COUNTER: CHANNEL COMMUTATION SEQUENCE	89
APPENDIX E TIMING TABLE	91
REFERENCES	95

ILLUSTRATIONS

Fig. 1	Balanced Magnetic Comparator	13
Fig. 2	MAD Flux Source and Switch	20
Fig. 3	MAD Stopper Circuit	23
Fig. 4	Physical Layout: MAD Composite Circuit	28
Fig. 5	All-Toroid Stopper Circuit.	33
Fig. 6	Composite Circuit	37
Fig. 7	Flux Gain Circuits	41
Fig. 8	Current Gain Circuits	42
Fig. 9	AND Circuits	47
Fig. 10	OR Circuits	48
Fig. 11	NEGATION Circuit	49
Fig. 12	Composite Circuit: Shunt Removed	52
Fig. 13	Composite Circuit: Complete Assembly	53
Fig. 14	Elementary Driver Circuit	55
Fig. 15	Pulse Current Sources	58
Fig. 16	Efficient Multipulse Current Source	58
Fig. 17	Magnetic Logic Design: 12-Channel Telemetry System	64
Fig. 18	Digital Channel Input Circuit	66
Fig. 19	Insulation Test Method	77
Fig. 20	Arrow Notation	82

TABLES

Table I	List of Logic Circuits	46
Table II	Telemetry System Specification	73
Table III	Specifications for System Shown in Fig. 17	74
Table IV	List of Components	74

I INTRODUCTION

Recent advances in telemetry have resulted in the increased use of digital techniques for the implementation of telemetry systems. Thus, use has reached a maximum in the pulse code modulation (PCM) systems. The performance requirements that have fostered these advances are continually changing and indicate a yet greater application of digital techniques in the telemetry field. One such performance requirement that continues to increase is reliability; for as system complexity increases, it cannot be at the expense of system reliability. It follows then that merely to maintain system reliability at its present level, more complex systems* will require an improvement in the reliability of their most critical components and/or inclusion of redundancy techniques. Redundancy techniques may, in theory, always be applied, but at an increase in price/power and complexity. The broader the application, the greater the price. The reliability of components may be improved by tightening process controls in manufacture and assembly, replacing the critical components with other components of higher reliability, or minimizing the number of the critical components (before applying redundancy techniques). But this is merely to maintain the same system reliability. To achieve higher system reliability, the alternative approaches are the same; however, the reliability increase is not directly proportional to the improvement effort.

The use of digital all-magnetic circuit techniques offers an interesting potential solution to the reliability problem. These circuits use only magnetic ferrite elements and wire, both of which are inherently stable and very reliable. The number of semiconductor components required in a system is greatly reduced by the application of all-magnetic techniques, and redundancy techniques may be applied to the remaining semiconductor elements more efficiently. An additional feature of this type of circuit is the fact that power consumption is directly proportional to the speed of circuit operation. The circuits are non-volatile and do

*It is assumed here that good engineering practices are used in all cases, that environmental conditions are the same, and that the differing uses of the elements in one system or the other does not degrade their reliability. Any detailed reliability analysis of a system would require that these factors be considered.

not require standby power. Thus, they offer the potential of power economy through variation of the operating speed according to the redundancy content of the sampled data or other criteria.

The terminal objective of this contract--Feasibility Study for the Application and Design of an All-Magnetic Digital Data Handling System--is to provide, at the end of the second phase, a breadboard model of an all-magnetic PCM telemetry system to demonstrate the capability of all-magnetic techniques. The performance of this model, together with the results of the first phase, will provide the basis for evaluating the merits of this approach. For the first phase, covered by this report, the specific objectives were to:

- (a) Investigate the application of magnetic techniques to high and low level commutation, signal amplification, analog-to-digital-conversion, arithmetic manipulation of digital information, and storage of digital information and to determine if any of these operations may be combined by the use of magnetic circuitry.
- (b) Generate a logical design of a pulse code modulation telemetry system based upon all-magnetic circuit techniques.
- (c) Apply known all-magnetic techniques and a minimum of semiconductor components to provide the required logic functions.
- (d) Breadboard test critical magnetic circuits.
- (e) Determine a set of specifications that describe the expected system performance and characteristics.
- (f) Delineate areas of research effort most likely to produce a further reduction in semiconductor components.

In the Phase I study of the application of all-magnetic circuit techniques, their relation to future systems has been a constant consideration, so that circuits or techniques which appear to operate at, or close to, the limits of their capability have been discarded.

Digital magnetic techniques have not been previously applied to PCM telemetry systems. Because the form of the information from the sensors is an analog signal, a hybrid system is involved. Therefore, certain questions needed to be answered to determine the feasibility of applying all-magnetic circuit techniques to realize a typical system: What portion of the system must be analog? What are the factors which determine the analog/digital circuit mix? Before these could be answered, more basic questions had to be answered: Must the information be commutated in analog form? Can magnetic elements be directly connected

to the sensors, and, if so, are these elements compatible with the type used to implement digital logic? Also, questions that relate to the general applicability of all-magnetic techniques had to be answered: Can low-level, high-level, and digital sensors be arbitrarily intermixed and commutated? Can the logic for information processing and control be performed using the all-magnetic technique? How reliable are these digital magnetic elements and how do they react to various environments? Finally, what is the power consumption of a system implemented by use of the all-magnetic circuit techniques? The investigations conducted during the first phase answered these questions and culminated in a detailed logic design based upon all-magnetic circuit techniques.

II SUMMARY

The feasibility of an all-magnetic PCM telemetry system has been studied during the first phase of this project. The organization of the system for the use of all-magnetic circuit techniques was determined by studying each of the functional blocks comprising the system and evaluating the capabilities of various magnetic circuits to implement these functions. Three findings of this study have been major factors in determining the logic design which resulted from this study. First, a magnetic circuit can have sufficient sensitivity for direct connection to many of the commonly used sensors; this permits comparison at the signal level of the measurand. Second, the functions of comparison, commutation, and programming for each channel may be efficiently combined into one composite circuit. Third, the power losses in the current drivers for the all-magnetic circuits can be significantly reduced.

Based upon the results of these studies, a detailed logic design has been prepared. This design is different from that for semiconductor systems: analog information amplification has been eliminated, and the sampling of channels is effected by commutation of digital control signals. The elimination of the requirement to commutate analog information has made possible a completely digital design.

The logic design is for a twelve information channel PCM telemetry system. Six analog channels are supercommutated. Four analog, two digital, and the two synchronization channels are prime-commutated. The four prime analog channels are of varying sensitivity and accommodate both high and low level sensors. This design requires seven hundred magnetic cores, fifty transistors, and thirteen diodes. Digitizing to seven bit accuracy is accomplished in less than one hundred microseconds. The power consumption of this system has been calculated to be less than ten watts.

An unsuccessful attempt was made to find a failure mode for manganese-magnesium ferrite elements and to establish the reliability of magnetic elements on a quantitative basis. In-service failures have not been detected in the field; if they do occur, they are not identifiable.

Future research may reasonably be expected to reduce the number of semi-conductor components, to reduce the power requirements, or to improve the performance of the system.

III BACKGROUND

The purpose of this section of the report is to provide a setting for the sections that follow. Here we attempt to put into perspective the detailed investigations that are described, and to show our method of approach.

The body of knowledge relating to all-magnetic logic circuits has increased markedly in recent years.^{19*} Several applications of these techniques have been made to portions of systems and to feasibility models designed to illumine the logic capabilities of these techniques. Knowledge of the present state of the art indicates that certain portions of a telemetry system are realizable by using these techniques. Their applicability to other portions of a PCM telemetry system has not been established by virtue of previous studies. This is due principally to the unique functional requirements of such a system, one of which stems from the inherent hybrid nature of these systems. They generally accept input information in analog form and yield output information in digital form. In order to make an honest feasibility determination, it was felt essential that application of all-magnetic techniques to the whole system must be considered. This meant considering the interface between the sensors and the magnetic elements, establishing the performance requirements of the system, examining the capabilities of the all-magnetic circuits to provide the required performance, and finally determining the mixture of analog and digital circuits.

This feasibility study started with an investigation of the interface between the sensors and magnetic elements. Initially, the electrical characteristics of various sensors were obtained. This information was used to investigate the possibility of driving magnetic elements directly from the sensor without intervening semiconductor amplifiers. Because magnetic elements are current-actuated devices, the current output of the sensors was of major interest. The few cases reported in the literature 1, 2, 3, 4 were not found to be suitable for general application to a PCM telemetry system. On a previous project,⁵ a procedure was initiated for testing the uniformity of magnetic cores wherein two cores were driven by a common drive current and their outputs were connected

*References are listed at the end of the report.

in series opposition. When the cores had identical characteristics, the cancellation was excellent, and only a very small output signal was obtained. It was observed at the time that only a small differential environment acting in the cores--i. e., temperature, current, or strain--produced a significant unbalanced indication.

Consideration of the sensitivity exhibited by this technique led to the conception of the balanced magnetic comparator circuit (abbreviated BMC), wherein the measurand current, derived directly from the sensor, is threaded through previously balanced cores to produce an unbalanced signal. The feasibility of using this technique has been experimentally verified during the course of this project and is reported in detail in Section IV. This circuit has been found to be sufficiently sensitive to generate a detectable, unbalanced output signal for the one-bit-out-of-seven resolution required and is sufficiently simple to allow the use of one BMC associated with each telemetry channel. By use of the method of successive approximations, it is feasible to digitize directly at the magnetic element where the analog information enters the system. The output of this stage then is treated as a binary quantity--either it is present or it is not--although it may vary widely in magnitude.

For the BMC circuit to be useful in a system to be implemented with magnetic logic, it must be possible to efficiently digitize the measurand information. The presence of the measurand current on the BMC alone does not produce an output indication; but its presence in conjunction with other pulses (referred to as the Read and Restore pulses) does produce an output. Commutation is effected by sequentially applying a group of these pulses to the BMC associated with first one channel and then another. This function can be combined with the programming function to sequentially select the channels in a predetermined sequence and may be implemented by the use of known, all-magnetic techniques. However, the requirement for commutating seven pairs of pulses to each BMC coupled with the required temperature range of operation made it desirable to determine an alternative method for achieving this logic function.

As a result of this investigation, a new class of all-magnetic circuits has been found. These circuits are called "stopper" circuits and were designed to overcome certain problems encountered in the application of previously known

techniques to realize this logic function. Stopper circuits have made it possible to efficiently combine the functions of the commutator, the programmer, and the BMC in one circuit. Two forms of this circuit have been investigated experimentally and are reported in detail in Section IV.

To complete the digitizing process, a weight generator capable of supplying all combinations of seven binary weighted currents is required. The logic associated with the weight generator is capable of being implemented by a slightly modified form of the stopper circuit. Intimately associated with this logic are two buffer storage registers, one for use with analog channels and one for digital channels, which provide the necessary buffering between the digitizing bit rate and the system output bit rate. A circuit has been conceived to generate the required weight current to the necessary or desired precision, but the initial tests on this circuit have not been completely successful. This circuit is discussed in more detail in the following section.

The remaining logic function necessary to be implemented, to complete the system, is the timing generator. This logic function may be realized by using a modified stopper circuit connected to form a series of four ring counters. A major concern in realizing this function is one of power consumption, for the power required to operate magnetic circuits is directly proportional to the frequency of operation. The front end of the counter must operate at the frequency of the oscillator specified to be no lower than 100 kc. The second ring counter is operated at $1/4$ of the oscillator frequency. The power consumed in operating these two ring counters accounts for more than half of the power consumed in this system. Most of the power dissipated in operating magnetic circuits heretofore has occurred in the current drivers. This has led to an investigation of the drivers to determine available means for decreasing this source of power dissipation. Two methods of power reduction have been conceived and are discussed in more detail in the following section.

The major goal of this program has been to generate a logic design to demonstrate the feasibility of implementing a telemetry system utilizing all-magnetic logic techniques. It was to this end that the above investigations aimed at determining the ability of all-magnetic circuitry to perform the required functions were undertaken. These results have been used to generate the logic design of a

telemetry system. A discussion of the final logic design and of the system characteristics is also given in detail in the following section.

A parallel investigation inquiring into the actual reliability of magnetic elements was conducted. The results of this investigation verified the high reliability attributed to the magnetic element. The reliability of magnetic elements has been much discussed but very little quantitative data is available. The field experience has been so good with the particular class of magnetic elements investigated here (memory-toroids) that very little empirical data on failures has been accumulated. The details of this investigation are given in Section IV.

IV INVESTIGATIONS

A. Magnetic Circuits

1. Balanced Magnetic Comparator

a. General Description

The balanced magnetic comparator is a circuit containing magnetic elements that respond to the difference in amplitude between two currents that are applied to separate windings of the circuit. As it is used here, the comparator is a null device that is activated by a read pulse. When current having an unknown amplitude is applied to the comparator, an output voltage pulse is generated. When this unknown current is matched by a current having equal amplitude, the comparator produces a null indication, zero output voltage. With the output of the comparator connected to a suitable detecting circuit, the sense amplifier, and a set of known currents, to be sequentially applied to the comparator, it is possible to determine the amplitude of this unknown current. The unknown current may be the output from a sensor, which is the analog of some measurand such as temperature.

It should be noted that this procedure is a departure from the method of measurement that is presently used in telemetry systems. In these systems the voltage output from a sensor is compared to a standard voltage. For such use sensors are classified as low-level and high-level indicating sensor outputs of 0 to 20 millivolts and 0 to 5 volts respectively. The balanced magnetic comparator is a low-input impedance device, so this voltage classification of sensors is not a sufficient description for this application. In discussing this problem with personnel at the Langley Research Center, we find that there is a large class of sensors that have characteristics that are compatible with this comparator circuit. In fact, it appears that most of the sensors that are inherently capable of high reliability are compatible with this magnetic device. To be compatible a sensor must produce a direct current that is a function of the measurand. This function need not be a linear one since each individual sensor is calibrated in situ. The sensor needs to be

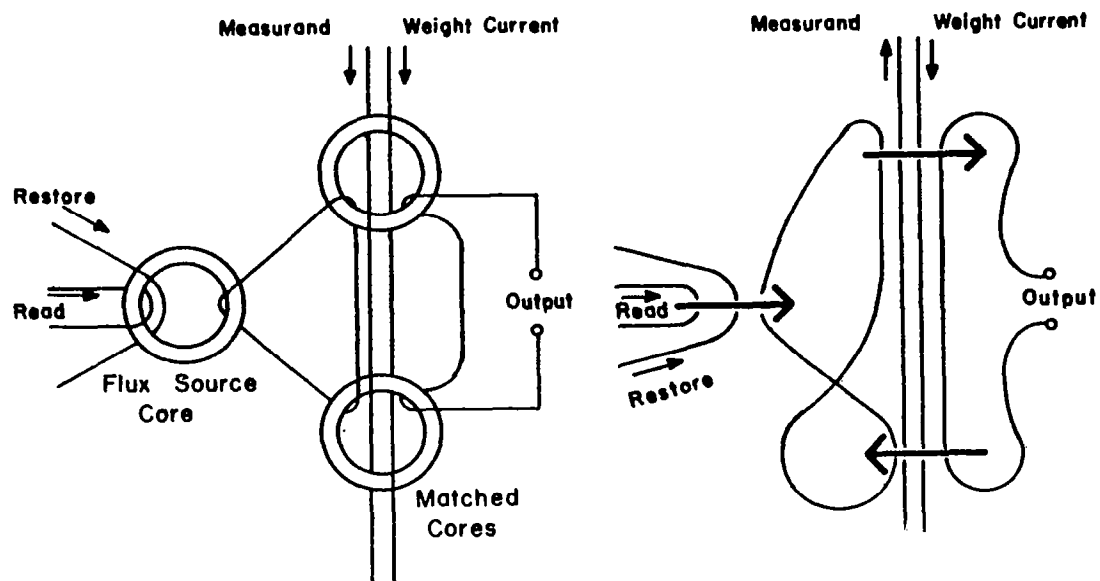
capable of delivering a current of 1 milliampere full scale into a load of a few ohms. The output impedance of the sensor per se is not important, since only a small series inductance is required to effectively isolate the sensor and comparator as far as switching voltages are concerned.

A key feature of the balanced magnetic comparator is that it samples, quantizes, and digitizes without amplification of the analog signal. In the typical telemetry system, amplification of dc signals is required between the sensor output and the comparator input. The necessity for doing this has been eliminated, at least for many kinds of sensors.

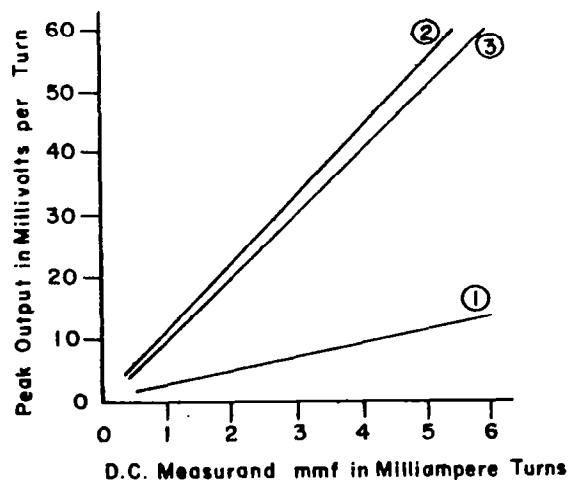
b. Idealized Circuit Operation

In Fig. 1 schematics of two realizations of the balanced magnetic comparator are given along with a typical output voltage characteristic. To understand the operation of this circuit, consider the following step-by-step sequence for the toroid version shown in Fig. 1(a). The sequence is described with references to a common schematic method of representation shown on the left in the figure. Another method of representation that has certain advantages is introduced in this figure. This arrow notation is used exclusively later on in the report and is described in Appendix A and Fig. 20.

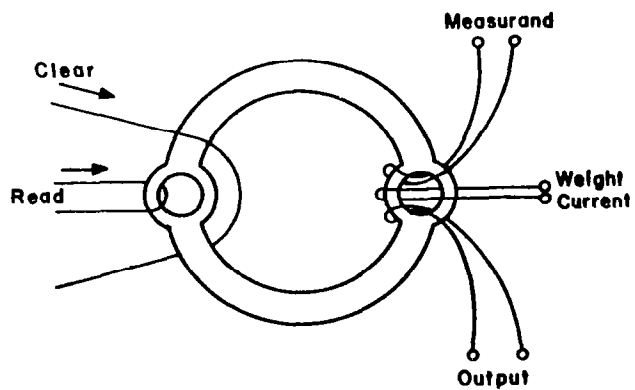
The three ferrite toroids are all similar to each other and all have the same nominal flux capacity, and for our purposes all windings can be considered as being only one turn of wire. Assume that initially all toroids have been saturated, so that the flux is in the clockwise direction; this will be referred to as the "cleared" state because it contains no information. Now a current pulse is applied to the read winding that threads the flux source. The pulse has sufficient amplitude to completely switch the flux source, so that it becomes saturated in the counterclockwise direction. If the loop that couples the flux source to the matched pair is considered lossless, then the one unit of flux from the flux source is transferred to the matched pair. Now if the measurand, weight current, and output windings have no current in them, and also if the two cores of the matched pair are truly identical, then each core of the pair receives one-half unit of flux. A subsequent restore pulse will clear the circuit. Note that if the circuit elements are assumed to be ideal, the voltage across the output winding is zero during this read-restore cycle.



(a)



(b)



(c)

FIG. 1 BALANCED MAGNETIC COMPARATOR

For the second read-restore cycle, assume that there is a small direct current flowing in the measurand windings. The mmf that results from this current is small and cannot by itself switch the core, but it can modify the flux switching rate in the matched pair during the read period. For this reason a greater amount of flux is switched in the bottom core than in the top core when there is coupling loop current flowing, i. e., during the read period. This differential flux switching causes a voltage pulse to be present across the output winding. Likewise, when the restore winding receives a pulse of current, there is now a different amount of flux switched in the two output cores and a net voltage is induced in the output windings.

It is now evident that a current through the weight current windings could be used to precisely balance the effect of the current in the measurand windings, and that this condition can be detected by observing the voltage across the output windings during the read and restore periods. If this current in the weight current windings has a known value, then the value of the current in the measurand windings can be determined. It is also evident that the current in the weight current windings need not be direct current; it can be a flat topped current pulse that is turned on before the read winding is energized and turned off after the read winding is de-energized. If the amplitude of the weight current pulse is changed sequentially in time and in synchronism with the read-restore cycle, then by successive approximations one can determine the amplitude of the measurand current and effect the conversion into a digital representation. (This procedure is discussed in more detail later on in this report. Also see reference 6.)

In principle, similar operation to that just described for the toroid circuit can be obtained using a multiaperture device (abbreviated MAD). This circuit is shown in Fig. 1(c). No experimental work was done with this MAD circuit, but there may be merit in such an approach (although probably not with the geometry shown in the figure). The ready availability of different types of toroids and the favorable test results obtained with the toroid version left little motivation for investigating the multipath approach at this time. Furthermore, balanced switching and multiturn windings would be difficult to achieve. It should be noted that these toroid and multiaperture balanced magnetic

comparator circuits have points of similarity to the balanced switch described by Crane and English⁴ and the magnetically balanced circuit described by Newhall and Perucca⁷.

c. Performance Characteristics

Along with the circuits in Fig. 1, the graph, Fig. 1(c), plots the peak output voltage as a function of the measurand current, with the weight current being maintained at zero. These data are from a test that was performed on a particular toroid circuit (Ampex type 802-40 cores were used). Curve number one depicts the output voltage that is observed during the read period, curve two depicts the voltage observed during the restore period, and curve number three shows the influence of temperature. A substantial increase is effected in the sensitivity of the circuit if the restore-period voltage is taken as the useable output rather than the read-period voltage. For this mode of operation the weight current pulse must remain on for the duration of the restore pulse. The sensitivity for curve number one is 2.5 mv/ma and for number two it is 12.5 mv/ma.

There are two reasons for this increase in sensitivity. The first is that a greater mmf drives the cores at restore time than at read time. This is because the clock current not only passes through the restore winding, as shown in Fig. 1(a), but it also passes through windings on the matched pair that are not shown in the figure. These windings have a polarity such that the restore current through them drives the cores in the clear direction. It is not possible to simply add windings to get a similar effect at the read period, because this would destroy the flux limited property that is essential to the transfer from the flux source. The second reason for the sensitivity increase is a more subtle one, and one that is not fully understood at this time. Experiment shows that during the restore period the matched cores switch at virtually identical rates for the first portion of their switching period, and then for the last portion of this period the switching of the bottom core (the one with the most flux in it) predominates. That is, the differential flux is "squeezed" out of the circuit in a short period and hence at a higher voltage. This "squeezing" is probably due in part to the fact that the top core, which has the smallest amount of flux in it, has the greatest total mmf applied to it since the measurand current aids the restore current in this core. It is also probably due to an inherent property of

the core material, since it is known that the waveform (voltage vs. time) for a partially preset core is dependent upon the amount of flux that is preset and upon the rate at which the flux is preset.^(8,9,10) This feature needs to be examined in greater detail.

Another subtle effect observed while testing certain ferrite materials as matched toroids is believed to result from the formation of 360° domain walls.¹¹ During our testing we observed that the degree to which two cores had similar switching characteristics was a function of their previous flux switching history. This would result in a poor signal-to-noise ratio under dynamic operating conditions. No detailed evaluation of materials was made as it was deemed inappropriate for this first phase. We anticipate that better materials will be found in the future, but, for the present, the characteristics that have been obtained are quite satisfactory.

The matching of pairs of toroids has turned out to be a fairly simple and straightforward procedure. It should be recognized that it is not necessary for the cores to have identical flux capacity, but it is necessary that the flux in the two cores switch at the same rate over a substantial portion of the switching period when they are subjected to identical mmf. Furthermore, it is necessary only that two toroids match each other, but it is not necessary that one pair be matched to any other pair.

Curve number three of Fig. 1(b) shows the influence of core temperature upon the sensitivity of the circuit. This curve shows the restore-period voltage output at -20° C, and indicates a sensitivity of 11 mv/ma. The other two curves are for a core temperature of +25° C. At 100° C the operation is similar except that the slope of the curve is increased to 16 mv/ma.

In Fig. 1(a), the measurand windings are shown as one turn on each of the matched output cores. We have wound as many as 100 turns of wire on a matched pair of 50-80 mil toroids, which produced a sensitivity of 1 mv/ma with the toroids presently being used. The maximum amplitude of the measurand current that can be applied is determined by the threshold of the toroids; for those presently used this will limit the current to about one-fourth ampere through one turn, or about two milliamperes through 100 turns.

The resolution of the balanced magnetic comparator is limited by the noise output from the practical circuit when the measurand current is zero. Under the conditions that prevailed when the data were taken, the noise was less than 5 millivolts. It is of course true that the resolution of the system as a whole depends upon other factors as well. Assuming that the sense amplifier can discriminate between signal and noise when the signal-to-noise ratio is 2:1, we can predict that a current of 10 microamperes can be detected.

The encoding interval, required for a given telemetry application, is a function of the rate of change of the measurand current amplitude.* For the balanced magnetic comparator in the form described here, the encoding interval is about 96 microseconds for a 7 bit accuracy. This encoding interval places a theoretical limit of 13 cycles per second on the frequency content of the analog signal. The conventional manner for overcoming this limitation is to use sample-and-hold techniques that involve storing non-quantized information. There appear to be means for increasing this upper frequency limit that are compatible with the magnetic approach taken in this project and that do not require non-quantized storage. This has not been investigated since for this application the maximum frequency content of the signals from the sensors is about 1 cycle per second.

d. Possible Improvements

In the discussion above dealing with the magnetic characteristics of ferrite, it was noted that no attempt was made to optimize the material characteristics that are important for this application, although several ferrite materials were briefly examined. This approach is consistent with the intent of this phase of the investigation; we are examining feasibility but are not optimizing. However, there are several things in addition to using different magnetic materials which could result in more desirable characteristics than have been obtained thus far. For example, it should be possible to improve the sensitivity by a factor of approximately 2 by using two cores in each of the three positions where one is now used. This would double the flux changed in a given

*Aliasing error also limits the rate of change of the continuous analog signal, but it is related to the repetition rate, i.e., the number of encoding intervals per unit time. (12, 13, 14)

time interval; hence, twice as much output voltage would be obtained. Matching the cores would be more difficult, but initial tests indicate that it should certainly be practical to do so, with the absolute noise level remaining approximately the same as it now is for the single core case. Winding the two-core units would be somewhat more difficult, and the overall system power requirement would be increased slightly.

Another method of doubling the sensitivity would, in addition, double the noise level. This method simply requires two-turn instead of one-turn windings for the output.

It appears that the noise present in the output windings might be considerably reduced if the only flux linking the coils were the flux that is internal to the ferrite itself, i.e., eliminate the air flux. It appears feasible to plate a winding onto the ferrite in a manner that would virtually eliminate this air flux linkage. Some speculation indicates that a two-turn output winding of this type could result in doubling both the sensitivity and the resolution limit at the same time!

The preliminary fabrication work that has been done with the balanced magnetic comparator and with the composite module described below indicate that improvements in fabricating techniques should be made, and also that this can be accomplished with a reasonable effort.

2. MAD Circuits

a. The Composite Module

1) Introduction. In the analog-to-digital conversion technique that we propose, it is necessary for the balanced magnetic comparator be "turned on" at the appropriate times and be "off" at other times. This can be achieved by driving the flux source associated with a specific channel only when it is desired to encode that particular channel. The comparator is "off" when the flux source is not driven by the read and restore pulses, and the presence of current in the measurand and weight current windings does not produce an output voltage. Therefore, a conceivable mode of operation is to commutate the read and restore clock pulses under the control of a programmer. Such a scheme might make use of a current steering switch to direct the clock current pulses.¹⁵

An alternate approach, the one followed here, does not require the commutation of clock pulses. The read and restore clock pulses are directed simultaneously to all the comparator flux sources through series connected windings. However, only one selected flux source is permitted to switch. This selection and control of the flux source can be accomplished by using a MAD¹⁶, as we describe in this section of the report, or by using a new toroid circuit that we describe in the next section. Both circuits have been experimentally investigated to determine the feasibility and desirability of using them for this application.

We have considered using the MAD, because it can perform the "on" and "off" switching of the flux source that is required for commutation, and it can also be used in the programmer. All logic functions can be realized using MAD all-magnetic logic techniques, and these techniques have been developed to the point where their practical advantages and limitations are known.^{17, 18} In considering the MAD approach, the possibility of using toroids in a new circuit was conceived. The toroid circuit had some potential advantages that led us to investigate the circuit experimentally in the laboratory. Both the MAD and toroid circuits were investigated in parallel, the former because the relatively sophisticated state of the art gave assurance of a reasonable degree of success, the latter because of its potential. (To anticipate our conclusions, it now appears that either the toroid or the MAD circuit can be used, with the balance in favor of the toroid circuit for this project.) The MAD or toroid stopper circuit in combination with the balanced magnetic comparator is used in each channel and is designated as the composite module.

2) Idealized Operation. Let us consider briefly the operation of a MAD as a switch and a flux source. In the schematic shown in Fig. 2, the flux-source toroid is replaced by one minor aperture of a MAD. If it is possible to switch flux around the minor aperture to which the matched toroids are coupled, then this minor aperture acts as the flux source. However, if the MAD is cleared with the flux all saturated in one direction around the major aperture, then there is no flux switching possible for read and restore pulses of limited amplitude. Therefore, the comparator can be turned off by saturating the MAD in the clockwise direction by means of a current pulse through the clear winding.

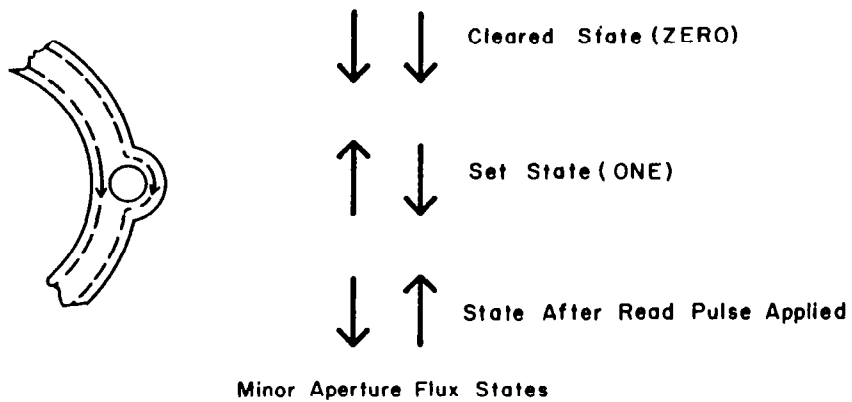
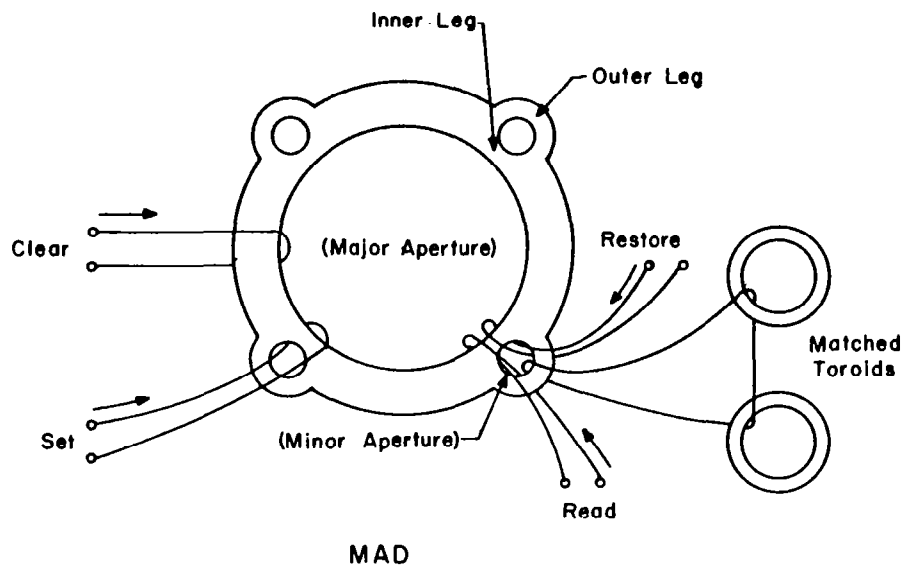


FIG. 2 MAD FLUX SOURCE AND SWITCH

The comparator can be turned on by switching one-half of the total flux capacity around the major aperture in the counterclockwise direction by means of a current pulse on the set winding, since this permits localized switching around the minor aperture.

When the MAD is in the cleared state it is possible to set the core spuriously by driving hard on the read or restore winding. If this minor aperture were not loaded by the coupling loop linking the matched toroids, then the MAD could be set through these windings by a current equal to the current required in the set winding. This is the maximum amplitude that can be applied to the read and restore windings for normal operation. Note the magnetomotive force that is available to switch flux around the minor aperture is twice the magnetomotive force that tries to switch flux around the major aperture. This is because of the "figure eight" winding on the minor aperture. (Fig. 2 shows one turn on both the inner leg and the outer leg. In practice, the optimum turns ratio for these windings is usually not 1:1.)

We see from this cursory explanation that a MAD can serve as flux source and as a switch to turn the balanced magnetic comparator on and off. It is further evident, since there are several apertures, that if one MAD can be set from another MAD, there exists the potential for combining the switching, commutating, and programming functions in one basic module. All-magnetic logic techniques have been treated in the literature for the reader who wishes more detailed information.^{17, 19}

There are three characteristics of the MAD as a switch that need to be considered a little further for our purposes. The first of these arises from the fact that the magnetic material around the minor apertures is not in general well saturated when the core as a whole is saturated. This is because there is excess magnetic material around these apertures. The geometry of the MAD in Fig. 2 makes it impossible (with reasonable current magnitudes) to completely saturate all of the material in the inner leg associated with a minor aperture. Even if a more favorable geometry is used, manufacturing tolerances apparently make it impractical to saturate all parts of the core to the same degree. The best (in a sense) that one can achieve is to make sure that a particular minor aperture region is saturated. This, however, is at the expense of a reduced degree of saturation in other parts of the core. The end result of this saturation

problem is that the circuit connected to the MAD must be able to tolerate a small amount of flux switching around the minor aperture when the MAD is in its cleared state. A method of providing this tolerance is to place a small core on the output coupling loop and to drive this core by a clock pulse so the residual flux switching around the minor aperture is balanced by the flux switching of this so called "clipper" core. This is a practical and commonly used technique to allow for this necessary flux switching.

A second characteristic of the MAD as a switch is also due to the core geometry and can also be balanced by a clipper core. This characteristic is the increase in the amount of elastic flux from the minor aperture region above that present in a regular toroid. If only a small portion of a flux path is saturated, as it is here, the remainder of the path has a significantly higher permeability than it would if saturated²⁰ and, consequently, this increased amount of elastic flux is present.

The third switch characteristic is also related to the geometry of the MAD. As mentioned above, it is possible to spuriously set the MAD and therefore turn the switch on merely by driving the read or restore windings with a high amplitude current. This is an important characteristic because the matched toroids in the balanced magnetic comparator require a switching current of one to two amperes, and, therefore, a high amplitude read/restore current is needed. Also, for general logic applications, it is highly desirable to be able to drive hard on the output aperture. In principle it would be possible to increase the upper limit of this current amplitude by increasing the path length around the major aperture. However, this increased threshold would in turn require an increased current amplitude in the set winding, and this would mean an increase in system power. The next portion of the report is addressed to this third characteristic, spurious setting.

b. The "Stopper" Circuit

It would enhance the capabilities of a MAD circuit if it were possible to change in a controlled manner the minimum required current amplitude for switching around the main aperture. One technique that has been used in the past is to provide a pulse current source that acts as a bias to decrease the threshold on a MAD at the time that it is conditionally set from the preceding

stage. This has a disadvantage in that it requires that the pulse amplitude be maintained within narrow tolerance limits. The method proposed here does not have this restriction; additionally, this method increases the threshold rather than decreasing it.

In Fig. 3 a partial schematic of a "stopper" circuit is shown. (The name stopper comes from the action of the circuit in that it "stops" the flow of flux in a certain path at certain times.) The stopper circuit consists of three toroids that are coupled to the outer leg associated with the input minor aperture.

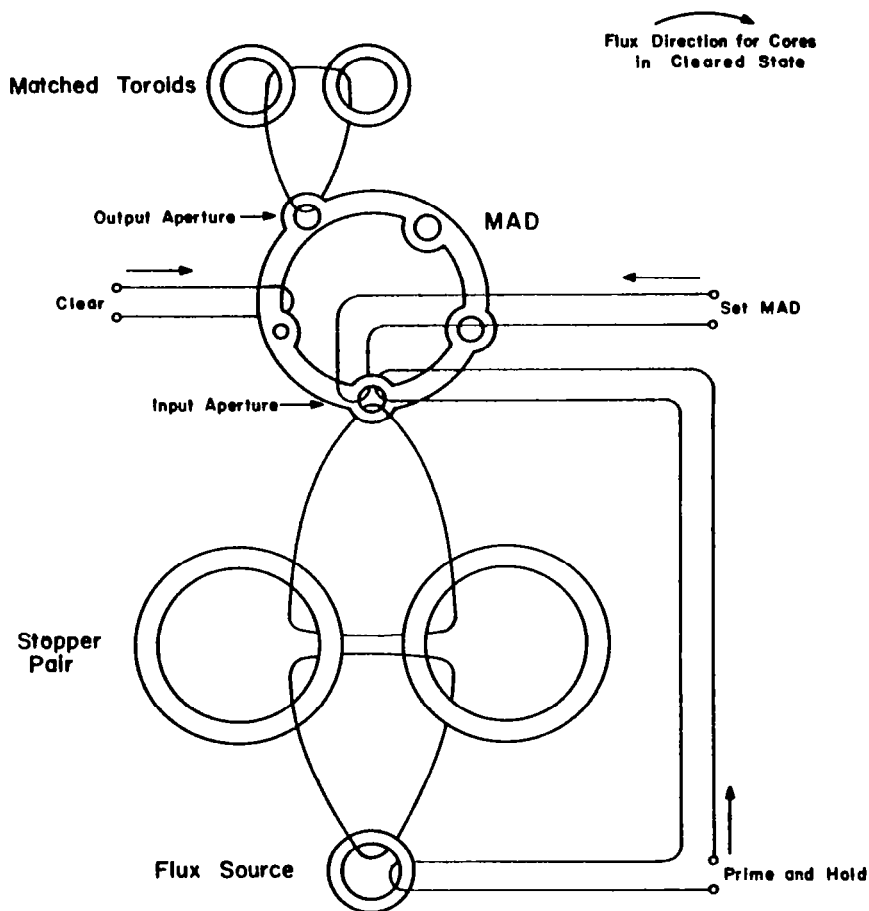


FIG. 3 MAD STOPPER CIRCUIT

The coupling loop connecting the two large toroids to the MAD is an extremely low-impedance conducting path, and it is referred to as the stopper loop. The purpose of this circuit is to prevent any flux change in either direction in the outer leg at certain prescribed periods in the operating cycle. At other periods, this circuit should permit the flux to change, therefore, the threshold for switching flux through this path is changed in a controlled manner. To extend this variable threshold effect to the main aperture, it is further necessary to hold the inner leg in the clear state at certain periods in the operating cycle. This is accomplished by a pulse of current from the clock source.

In order to understand this action more fully, let us go through a cycle of operation of the circuit shown in Fig. 3. Assume that the flux capacity of each toroid shown is equal to the flux capacity of the outer leg of the MAD. As an initial condition, assume that the flux in all cores is at remanence after having been saturated in the clockwise direction. The first event that occurs is a current pulse applied to the set winding. This pulse has sufficient amplitude to switch flux around the major aperture and saturate the inner leg associated with the input aperture. As before in Fig. 2, it is now possible to switch flux around the output aperture. The next event is the simultaneous occurrence of (1) a current pulse on the prime and hold windings and (2) the resetting of the flux from the previous stage (not shown) which had initially set the MAD. The current pulse in the prime and hold windings switches the flux source for the stopper pair of toroids and switches flux locally (primes) around the input aperture. The voltage induced in the set winding is balanced by the flux being reset in the previous stage. Currents in the two loops that link the stopper pair of toroids create magnetomotive forces which have polarities that add in the stopper core located on the right-hand side in the figure and that subtract in the left stopper core. This causes the right stopper core to completely switch and the left core to remain in the clear direction.

The flux from the source toroid has been completely transferred into the right stopper core, if the coupling loops are assumed lossless. This flux source toroid has dynamically biased the stopper cores, so that the current in the stopper loop can be likened to the measurand current in the balanced magnetic comparator. The stopper loop current required to completely "tip"

the flux into the right stopper core is much less than the current that would be sufficient by itself to switch the core. Therefore, the amplitude of the driving current in the prime and hold winding, which must supply this current when flux is switched locally around the input aperture, is likewise small compared to that required to switch flux around the major aperture of the MAD. Note that at this point in the cycle the inner leg of the input aperture has been saturated in the clear direction and the outer leg has been saturated in the set direction.

The third event to consider is application of an alternating current through the output aperture and a simultaneous application of a pulse (or series of pulses) to the prime and hold winding. Any tendency for the output drive current to cause flux to switch around the main aperture in the set direction is minimized by the holding mmf on the inner leg of the input aperture. Likewise, any tendency for switching around the major aperture in the clear direction is minimized by the stopper coupling loop that ideally constitutes a perfect shorted turn. The current in this shorted turn is in the direction that causes both of the stopper cores to switch. This loop current must, therefore, be limited to the threshold value for these cores, if the shorted turn condition is to be maintained.

Now let us consider a cycle of operation in which no flux is transferred at set time (a ZERO transfer). After the transfer period has occurred the next event, is to pulse the prime and hold windings, as before. This time there is no flux to prime around the input aperture, so the inner leg is merely driven further into saturation, and the flux source for the stopper pair is switched as before. This time there is no tipping current in the stopper loop, so the flux from the flux source is divided equally between the two stopper toroids. Furthermore, the simultaneous switching of these cores to 50% of their saturation value induces zero net voltage in the stopper loop, so no loop current results from this switching. At the conclusion of this pulse period, flux in the inner leg of the input aperture is in the clear direction, as it was for the ONE transfer (see Fig. 2). This demonstrates that the flux state of this leg is independent of the information state of the MAD at this period in the cycle. The flux in the outer leg is also in the clear direction now, which is different than in the ONE transfer. This time when a drive is applied to the output aperture, any current in the stopper loop tries to switch the left stopper toroid back to the clear state and tries to switch the right stopper toroid further into the set direction. The

current amplitude that will switch the stopper cores is now less than the amplitude required in the ONE case, because the cores are now in a soft, partially-switched condition. If this soft threshold current value for the stopper cores is equal to the hard threshold value for the MAD, then the output drive current amplitude, ideally, can be twice that of the MAD without the stopper circuit.

To recapitulate, the stopper circuit enhances the operation of a MAD by permitting an increase in the output drive mmf above its normal value. It does this by putting a shorted turn around the path wherein the flux state is information sensitive at the time output is taken. At the appropriate time this shorted turn is made to appear as a high impedance so that flux is permitted to change. The stopper circuit was conceived for this telemetry application, but its utility is much broader in scope.

Before we discuss the practical limitations of this circuit we will briefly turn our attention to another circuit using a MAD and stopper cores. This second circuit can be understood by referring to Fig. 3 and making a few circuit modifications mentally. First we eliminate that portion of the prime and hold winding which links the MAD, and then we remove the stopper loop from the input aperture and connect it through the major aperture. For this configuration, the flux source for the stopper cores is driven at the time a ONE or ZERO is being transferred to the MAD rather than after the transfer. When a ONE is transferred, the flux change around the major aperture is now linked by the stopper loop and a tipping current is developed in the loop. When an output aperture is subsequently driven, flux changes around the major aperture are minimized by the stopper loop, since the flux source does not dynamically bias the stopper cores at this time. The advantage of this circuit over the one discussed above is that the impedance of the stopper loop can be decreased because the cross section area of the wire is not limited by the area of the minor aperture. The disadvantage of this circuit is that it requires a greater current amplitude from the preceding stage to set the MAD. This second circuit has not been tested experimentally; it was derived from the toroid version of the stopper circuit that will be discussed in detail in the following section.

c. Performance Characteristics

It is evident that the key to the performance of the stopper circuit is the low impedance of the coupling loop which connects the MAD with the stopper toroids. This was recognized at the outset of the work, and it is true at the present time, that the loop impedance is the factor that limits the output driving current amplitude. Measurements show that the stopper loop current amplitude does not reach the threshold value of the stopper cores until the drive current has been increased substantially beyond the maximum value that the circuit will tolerate. The maximum drive that the circuit will tolerate is that value which will cause a build-up of the flux set into the MAD when the output aperture is repeatedly pulsed. This condition is referred to as "ZEROS building to ONES." The buildup arises in this circuit because the impedance of the stopper loop does not permit a sufficiently large demagnetizing current to flow.

One approach to minimizing these loop losses is to use the modified circuit (cited above) in which the stopper loop threads the major rather than the minor aperture and accept the increase in power consumption. Another approach is to use the multipath equivalent of the MAD and stopper core combination to avoid the use of a copper loop.* The most suitable approach for this phase of the project was to maintain the circuit as schematically represented in Fig. 3 and to reduce the loop impedance by making the conductor cross-sectional area large and its length small. The physical placement of the cores and the coupling loops of an experimental circuit are represented by the drawing in Fig. 4. The MAD shown here and in Fig. 3 is AMP Incorporated type 496871-1; however, the MAD in Fig. 4 has been altered by reducing its thickness to 20 mils. This reduction decreases the loop impedance substantially because the section of the loop passing through the minor aperture of the MAD has the smallest cross section area; the area of the minor aperture limits the size of conductor that can be placed in it. The remaining portions of the loop have large cross-section areas to minimize their contributions to the impedance. As shown in Fig. 4, there is a large piece of copper that completes the continuity of the coupling loop around the outside of the cores. The portion of the loop going through the

*D. R. Bennion of SRI has devised a multipath equivalent to this circuit.

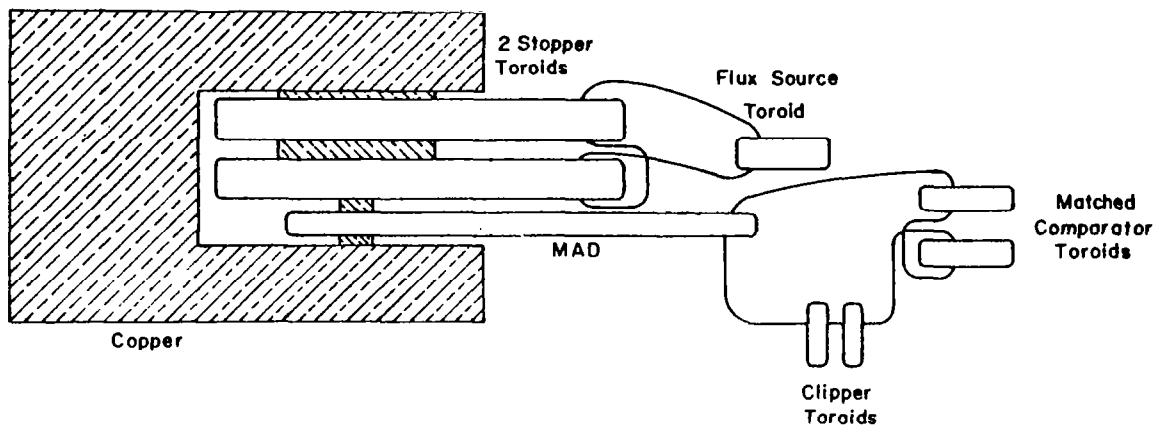


FIG. 4 PHYSICAL LAYOUT: MAD COMPOSITE CIRCUIT

minor aperture of the MAD is #22 wire, and the portion through the stopper toroids is #8 wire. The impedance of the loop consists of a fraction of a milliohm resistance and a series inductance in the order of a nanohenry.

There were really two reasons for reducing the thickness of the MAD. First of all, the flux content on one leg of the MAD is greater by a factor of 3 than the flux content of the 50-80 toroid. In a "thick" MAD stopper circuit, the flux level set into the MAD is determined by the toroid, so the flux capacity of the MAD is greater than necessary; therefore, a reduction in thickness is feasible. This reduction in thickness (1) permits the decrease in loop resistance, and (2) decreases the noise output of the MAD. As discussed briefly in a previous section of this report there is some inelastic flux that can be switched around a minor aperture even when the core as a whole has been saturated. Furthermore, there is a greater elastic flux component from the minor aperture region than from a simple toroidal shaped core. In decreasing the thickness of the MAD, we have reduced the elastic and inelastic components of the output noise to the same relative degree that the maximum available output flux was reduced. Since this reduction does not reduce the ONE level, we have effected a reduction in the signal to noise ratio. Note that clipper cores are shown in Fig. 4 and that they are required in the circuit even with this noise reduction. The clipper

cores used in the experimental circuit are RCA type 400 M1, and the matched toroids and the stopper flux source are Ampex type 802-40.

As with the balanced magnetic comparator, no extensive evaluation was made of the materials used in this circuit. Instead, we have judged on the basis of previous experience, a small amount of experimentation, and on published manufacturer's data. While the latter is useful, it has severe limitations because the information is usually given on the basis of the core memory applications for which they are intended.

The stopper core characteristics are of particular interest in this circuit. It is important that the material in these cores has a high value for both the hard threshold and the soft threshold. The soft-threshold value limits the amplitude of the stopper loop current when a ZERO is in the MAD, so this threshold is particularly important. Another characteristic that we single out is the average dynamic switching resistance of these stopper toroids. This resistance is the average switching voltage divided by the average value of the current, above the threshold, required to produce complete switching. In this application the average voltage is fixed within narrow limits by system constraints not related to the stopper per se. Therefore, the higher the switching resistance, the smaller the current amplitude required to switch the core. This is reflected in the operating circuit as a decrease in the current amplitude required in the prime and hold winding at the priming time. In this manner any tendency of the flux from the inner leg of the input aperture to switch around the main aperture rather than into the outer leg (see Fig. 3) is minimized.

The stopper toroids used in the most successful experimental circuit were cut ultrasonically from General Ceramic's S-4 material. The same type of stopper core is used in the toroid version of the stopper circuit (in fact it was first used in that circuit). We discuss some further ramifications of the stopper core characteristics in the section dealing with the toroidal circuit.

The circuit as shown in Fig. 3, except for a modification discussed in the next paragraph, was tested in the laboratory and found to work satisfactorily. It was possible to transfer flux from the minor aperture of the MAD to the matched comparator toroids over the temperature range of -20°C to $+100^{\circ}\text{C}$. The drive current through a 1 - 1 turn figure eight winding could be

varied from one-half ampere to one ampere over this temperature range. The test consisted of measuring the amount of flux transferred from the MAD to the matched toroid pair when the MAD was in the set condition and when it was in the clear condition. For both of these conditions 14 successive pairs of read/restore pulses were applied to insure adequate tolerance to changes under repetitive pulse operation. (During actual operation in the telemetry system there would be 7 successive pairs of read/restore pulses applied to encode to 7 bits.)

An additional test was made to measure the effectiveness of the MAD in turning off a channel. With the MAD in the cleared state, 100 milliamperes of measurand current was put through the measurand windings on the comparator cores. This current value is adequate to give a marked unbalance in any residual flux that is transferred into the matched pair, and is representative of conditions that might be experienced in a telemetry system. It was found that the output from the matched comparator toroids was essentially unchanged for a measurand current range of 0 to 100 milliamperes; therefore, the MAD plus the clipper cores act as an effective switch.

The circuit modification cited above is an expedient that was taken to minimize the time required to get meaningful data. It consisted of an additional winding linking one of the stopper toroids and was driven by a clock pulse to aid the stopper loop current in tipping flux into that stopper core when a ONE signal was in the MAD. The particular stopper cores and the MAD tested in this circuit apparently did not have completely compatible characteristics.* Without this circuit modification some flux is switched around the major aperture of the MAD during the priming operation instead of going into the outside leg of the input aperture and from there into a stopper toroid. This unsettling reduces the ONE level of flux in the MAD, and it occurs even though the stopper toroids are dynamically biased by the flux source. This means that the dynamic switching resistance of the stopper cores is too low. Using stopper toroids of somewhat smaller diameter would be one straightforward way of overcoming this problem. This reduction in path length is possible since the threshold of these stopper cores is greater than is made use of in circuit operation. (Recall

*After completing the laboratory experiments upon this circuit, a non-uniformity in the stopper core geometry was discovered. This non-uniformity bears on this problem.

that it is the stopper loop impedance that limits the drive current amplitude.) Other solutions include using a different material for the stopper cores or a modification (not tested) in the manner of driving the circuit.

d. Summary and Evaluation

The MAD version of the stopper circuit is capable of acting as an effective switch and flux source for the balanced magnetic comparator over the temperature range of -20°C to $+100^{\circ}\text{C}$. The logic capability that has been previously developed for the MAD can be applied to the programming function, and, in addition, the techniques that will be discussed in connection with the toroid version of the circuit can be applied. The limitation of the MAD version at present in terms of how hard it can be driven to take an output is imposed by the impedance of the stopper coupling loop. Although care was taken to reduce this impedance to a low value, still further reduction is feasible for the investigated circuit and for a slightly modified circuit. In addition, there is another circuit that was not investigated that is inherently capable of lower loop impedance, but which would require more power from the clock source.

The improvement that the stopper circuit gives over a conventional MAD circuit was not determined in a definitive fashion, but it is somewhat disappointing. To attach a number to the improvement afforded we can say that the effective threshold is increased by about 50% at room temperature. There remain some effects that are not completely understood at this time that should be further investigated before this circuit is applied to a system. These effects are related to the multipath geometry of the MAD. Available time did not permit a fuller study of these effects during this phase of the work.

The circuit, though workable, can surely be improved, but optimization was not a goal in this investigation and the test results are to be considered preliminary in nature. Winding configuration, turns ratio, and material properties are attractive candidates for optimizing circuit performance.

3. All-Toroid Circuits

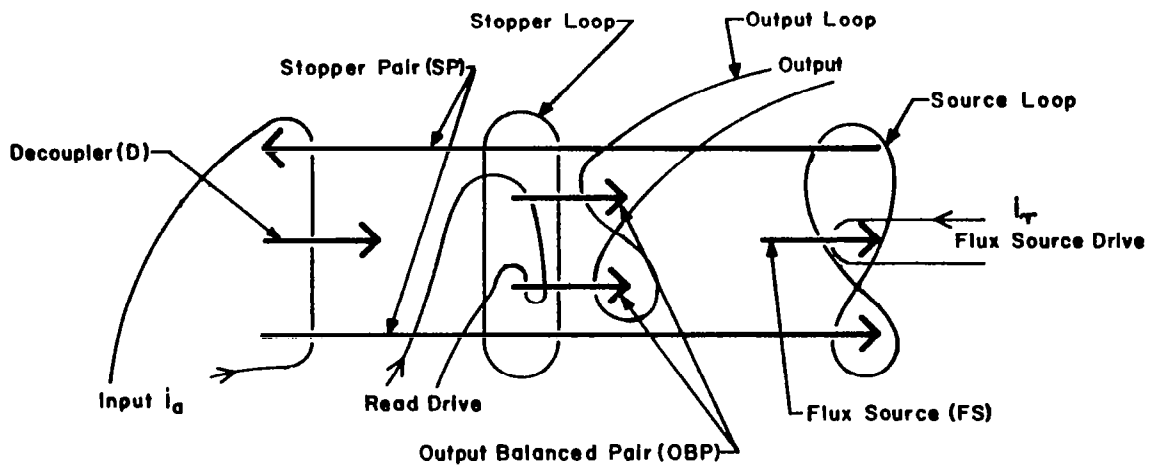
a. The Stopper Circuit

Approximately one month after the conception of the original stopper circuit, a variant form of this circuit was conceived which uses only toroidal

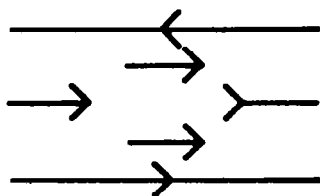
cores and offers several desirable features. The toroid version which has been investigated and tested in the laboratory is not a straight toroid equivalent of the stopper circuit which uses the MAD. The intent was to obtain a circuit with the capability of directly driving the BMC circuit the seven times required to digitize. For this reason, selection was based on which circuit arrangement of each form appeared at the outset to offer the greatest potential for realizing this result. The advantages seen for the toroidal form were that: (1) The noise signal (ZERO output) would be quite small; (2) Selection of different materials for the toroids would provide the desired characteristics for the different parts of the circuit. In other words, the constraint that the circuit performance be obtained from the characteristics realizable from a single material is removed; (3) A greater selection of materials is available in toroidal form and at essentially no waiting period for delivery; and (4) Modification of the circuit design may be accomplished more readily and without requiring construction of a new complex tool.

1) Basic Operation. Operation of the all-toroid stopper circuit is as follows: The circuit in its Clear, ZERO, and ONE states is shown in Fig. 5(a), (b), and (d) respectively. It is helpful to note that it is the state of the output balanced pair which is the significant difference between the ZERO and ONE states. The notation used here is explained in Appendix A. At each input time the flux-source drive is applied to the flux-source core causing it to switch to the set state. This induces a voltage in the coupling loop threading this core which, in turn, causes a current to flow. This current couples the stopper pair of cores. The stopper cores are large diameter toroids ideally having matched characteristics so that for a ZERO transfer, characterized by the absence of an input signal, the coupling loop current produces equal switching in each. In the stopper circuit all cores are of equal flux capacity, so that complete switching of the flux source core results, in this instance, in each of the stopper cores being half set*. The equal switching of these cores causes equal voltages to be induced in the stopper loop by each core. The polarities of these voltages are opposite and hence cancel, with the result that current is not produced in the stopper loop. This ZERO state is shown diagrammatically in Fig. 5(b). When a

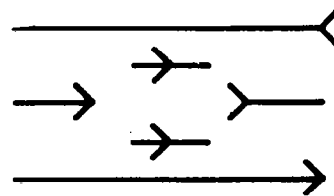
*This assumes ZERO resistance in the source loop. In practice, the resistance in the loop produces a small flux loss which subtracts from the flux set in each stopper core.



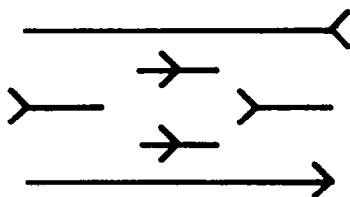
(a)
Windings And Clear State



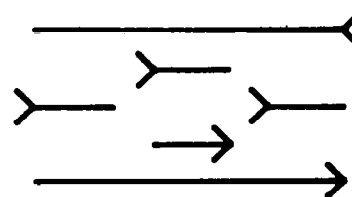
(b)
ZERO State



(c)
Undecoupled ONE State



(d)
ONE (set) State: Pre Read



(e)
Set State: Post Read

FIG. 5 ALL-TOROID STOPPER CIRCUIT

ONE is to be transferred into such a circuit, an input signal is applied in coincidence with the flux source drive. The input current produced by this signal, through the lower stopper core, opposes the action of the source loop current and causes it to switch slowly. The input current passing through the upper stopper core acts in the same direction as the source loop current and causes it to switch more rapidly. The input current passing through the decoupler core drives it in the clear direction and therefore the state of this core is not altered.

When the value of the input current, i_a , is equal to or greater than a prescribed value, the lower stopper core will not switch at all, with the result that the upper stopper core becomes completely set. As before, the flux source is also completely switched. However, when only the upper stopper core is switched, the resultant voltage induced in the stopper loop is not compensated for by voltage induced in its opposite member, with the result that a current is produced in the stopper loop in the direction that causes the output balanced pair to be driven in the set direction. Again, since the output balanced pair have ideally identical characteristics, each is set an equal amount. Remembering that the flux capacities of the cores are nearly identical, the complete switching of the upper stopper core results in each of the output balanced pair being half set*. This is shown in Fig. 5(c).

The input signal is typically generated from another magnetic element which must then be cleared. This develops a signal on the input winding of opposite polarity and produces a current in the set winding opposite to that which caused the ONE to be set into this stage. The direction of this current through the decoupler core is in the direction to set it. By the action of this core switching, the magnitude of the current is limited to a value below the threshold of the stopper cores; thus they do not switch, thereby providing the necessary decoupling between stages.²¹ This results in the decoupled ONE flux state shown in Fig. 5(d).

When a ONE is transferred into a stopper circuit, as described above, the output balanced pair is switched. There is an output winding on these cores which is connected to a load (or to a succeeding stage). It is necessary

*The difference between the idealized and the practical case is negligible here due to the very low resistance achieved for this loop.

that no signal be induced in this output winding at this time, i. e., that the output be decoupled at set time. This is accomplished by the manner in which the output winding is placed on the output balanced pair.

The output winding wound on these cores threads each core in opposite sense, with the results that the voltages induced by a ONE transfer cancel and that no output loop current is produced. An output signal is produced by applying the read-drive current to the output balanced pair through the read-drive winding. This winding also threads these cores in opposite sense, so that the read current drives the upper of the balanced output pair toward the set state and its opposite member toward the clear state. When the stopper circuit contains a ONE, each of the output balanced pair is half set and therefore free to switch in the direction urged by the read-drive current. As each core switches, it induces a voltage in both the stopper and the output loops. The voltages induced on the output loop add and produce an output loop current. The voltages induced in the stopper loop are of opposite polarity, and, since they are equal in magnitude, they cancel. The result is that no loop current flows in the stopper loop. This post-read set state is shown diagrammatically in Fig. 5(e). When a stopper circuit contains a ZERO, the state of the output balanced pair is as indicated in Fig. 5(b). The application of the read-drive current pulse will not produce switching in both cores, because, in each case, although one will be driven in the direction of the set state, the other one will be driven in the direction of the clear state--the state which it is already in. Therefore a current is produced in the stopper loop. Because the stopper loop resistance is very low, the induced voltage is very small. Since the flux change is proportional to this voltage, very little flux change will occur in this output core. It is this small flux change which induces the ZERO output or the noise signal.

The relationship between the flux change and the stopper loop resistance is a central factor in the operation of these circuits. Applying the Kirchhoff voltage law, we can write for the stopper loop:

$$\frac{d\phi}{dt} - L \frac{di(t)}{dt} - i(t)R = 0, \quad (1)$$

where:

- ϕ = flux (of the core switching)
- L = total inductance of the circuit
- R = stopper loop resistance
- $i(t)$ = stopper loop current.

By integration we find the flux change ($\Delta\phi$)

$$\int \frac{d\phi}{dt} dt = \Delta\phi = L\Delta I + R \int i_{(t)} dt , \quad (2)$$

since

$$i_o = i_f = 0 . \quad (3)$$

Here i_o and i_f are the initial and final values of the stopper loop current. Then,

$$\Delta I = 0 \quad (4)$$

and

$$\Delta\phi = R \int i_{(t)} dt . \quad (5)$$

The maximum value of $i_{(t)}$ is constrained to be

$$\overline{i_{(t)}} = I_T , \quad (6)$$

where I_T is the threshold value of the stopper core.

It can be shown that

$$\int_{t=0}^{t=t_1} i_{(t)} dt_{\max} = \overline{i_{(t)}} \cdot t_d = I_T \cdot t_d \quad (7)$$

where t_d is the duration of the drive pulse and t_1 is the time at which $i_{(t)}$ reduces to the threshold of the balanced output pair I_{TB} . The maximum flux change $\overline{\Delta\phi}$ then is

$$\overline{\Delta\phi} = RI_T t_d . \quad (8)$$

b. Composite Circuit

The stopper circuit forms the nucleus of the composite circuit that provides the functions of commutation and programming. A second output circuit acts as the flux source of the BMC. This circuit is shown in Fig. 6(a) and contains four cores more than the basic stopper circuit. They are the balanced pair of the BMC and an additional output balanced pair which is the flux source for the BMC (called the flux source pair). The ability to control the occurrence of an output from a balanced output pair by setting in a ONE or ZERO provides the

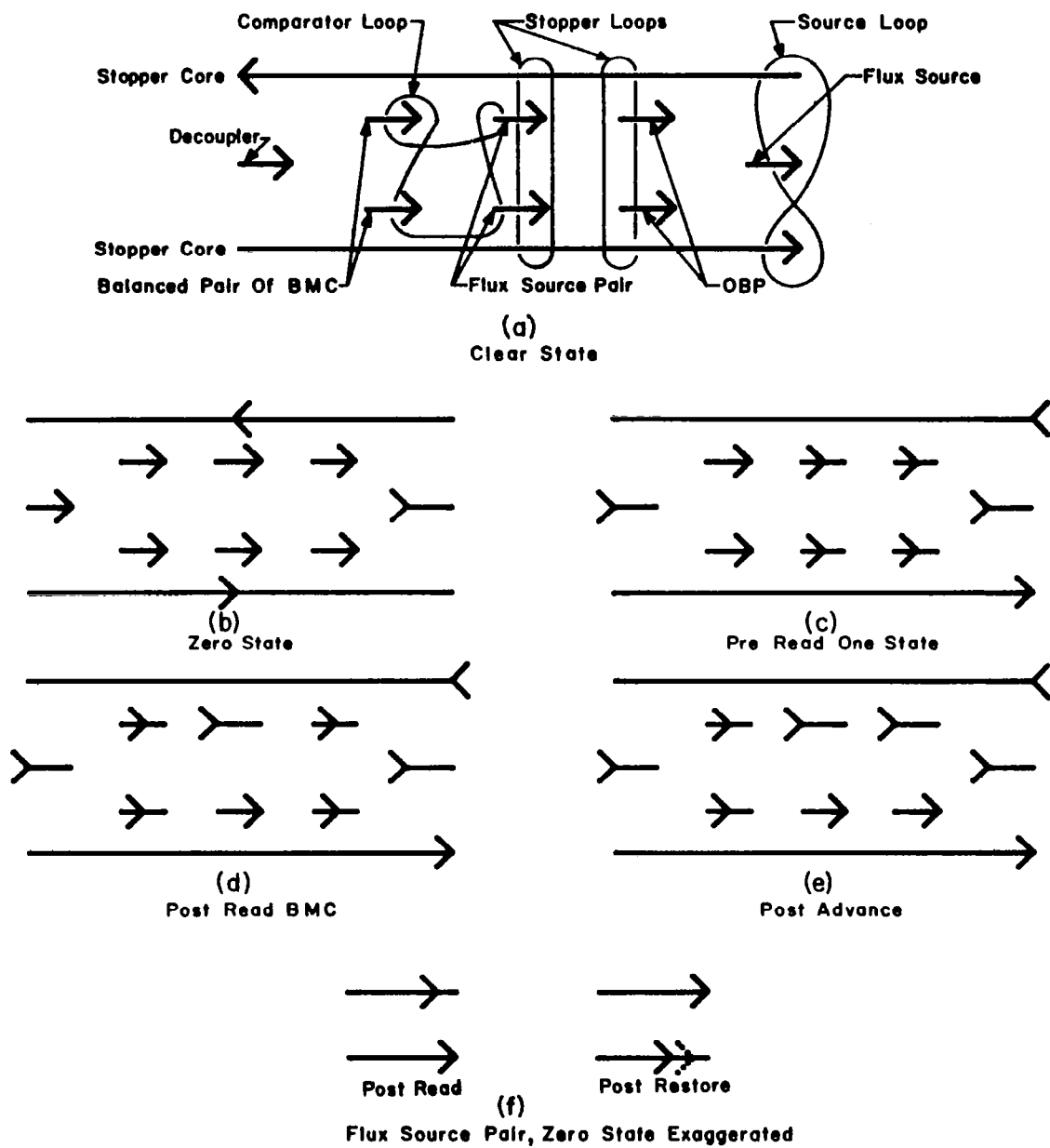


FIG. 6 COMPOSITE CIRCUIT

switching operation basic to the commutation function. However to be able to digitize the measurand, a single output pulse is not sufficient. To digitize to a seven bit resolution by the method of successive approximation requires seven consecutive comparisons and therefore seven outputs. These are obtained by adding a restore winding on the flux source pair.

Application of a read pulse to the flux source pair induces an output voltage in the manner described under basic operation, when the composite circuit contains a ONE. This causes the BMC pair to be switched differentially: the amount being a function of the magnitude of the measurand relative to that of the weight current. This post-read state is shown in Fig. 6(d). The restore pulse is next applied and drives the flux source pair in a sense opposite to that of the read pulse. This then restores the source pair which in turn clears the BMC pair to the pre-read ONE state, as shown in Fig. 6(e). The circuit is now ready for the application of another read pulse which produces an output nearly identical to that produced by the first read pulse. The read and restore drive pulses are alternately applied seven times to the composite circuit to achieve the necessary seven consecutive comparisons.

When a composite circuit contains a ZERO, as shown in Fig. 6(b), the BMC pair is not driven because the output from the flux source pair is inhibited by the action of the stopper loop current, as explained under basic operation. This ZERO output or noise signal must be small in order that the "off" channels do not interfere with the commutation of the "on" channel. The magnitude of this noise is largely determined by the resistance of the stopper loop for the flux source pair, which permits a small amount of flux change in the output pair. The need for the very small noise signal stems from the cumulative nature of this flux change. The noise is produced by the small amount of switching of that half of the flux source pair which is driven in the set direction. This effect is exaggerated and shown as the post-read state in Fig. 6(f). When the restore pulse is applied, this core is driven to the clear state, while its opposite member is driven in the set direction. It is able to switch an equal amount of flux (indicated by the dashed arrow) as the voltages, which are induced in the stopper loop by the switching of both cores, cancel. For the remainder of the duration of the restore drive pulse, stopper loop current will flow. This causes an additional small amount of flux to be switched, which is indicated by the solid arrow

in the figure. The effect is repeated at each application of a drive pulse and thus the total noise flux accumulates. For the noise signal produced by the last drive pulse to be sufficiently small, the additional flux change produced by each drive must be very small, hence the requirement that the stopper loop resistance must be very small. Practically, the flux change added by each drive must be less than 1%.

For the composite circuit to perform the programming function, it is necessary to transfer a ONE from one composite circuit to the circuit associated with the next channel to be commutated. To do this a second output balanced pair is used, as shown in Fig. 6(a). The use of two output pairs increases the value of the current required to set a ONE into the circuit by the amount of current required to set an output pair into the half-set state. The two outputs are completely isolated from each other as long as the stopper cores are not switched. Therefore, after the flux source pair has been driven by the seven pair of read/restore pulses, the output balanced pair is still in the half-set state.

The output winding and the drive winding (here referred to as the advance winding) are wound as already described. The output winding connects directly to the input winding of the next composite circuit.

c. Gain Circuits

To completely transfer a ONE so that the receiving circuit is fully set, the conditions related to flux and current gain must be met.²² First, the output current must be greater than the input current required to fully set a circuit to the ONE state. Second, the flux change linking the output winding must be larger than the flux change linking the input winding by an amount sufficient to compensate for losses in the coupling circuit. These conditions may be met in the stopper circuits by adjusting the number of turns used for the drive and output windings. The single-turn windings have been used to simplify the description of the operation. However, we are quite fortunate in having several other methods of accomplishing both flux and current gain.

The basic mechanism for obtaining current gain is in the selection of material characteristics and relative size of the stopper and output cores. An elementary treatment showing the minimum size relationship between the

stopper and output cores is given in Appendix B. Several circuits for providing gain are shown in Figs. 7 and 8. Fig. 7(a) shows flux doubling by means of multiple turns on the output winding. The operation of this output circuit is similar to ones already described, except that the flux linkage is twice that of the basic circuit (and the available current is half).

Fig. 7(b) illustrates a doubling scheme which increases output flux linkage by a different output decoupling configuration. Here the winding on the output balanced pair is as before, but the output winding also threads the stopper cores. The sense of this winding is such that for a ZERO transfer, where both stopper cores switch equally, the induced voltages cancel. For a ONE transfer, the upper stopper and output cores switch fully, and the induced voltages cancel in the output winding. In this manner each core in the output balanced pair is saturated in an opposite state, and the drive pulse causes each core to switch to saturation in the opposite sense. The flux change linking the output winding in this case is double that of the basic circuit.

Fig. 7(c) illustrates a circuit which might more properly be called a double circuit, however the stopper loop is common to both sets of cores. For convenience, let us refer to the outer group of cores as stopper circuit A and the innermost set of cores as stopper circuit B. There is no decoupling core used in this circuit, since stopper circuit A is set by a ONE transfer in the normal manner. Stopper circuit B is set by the output signal produced when the preceding stage is then cleared. This circuit performs the function that the decoupler core normally would, and at the same time adds to the flux transferred.

The circuit shown in Fig. 7(d) uses a different concept. This circuit accepts only a portion of the flux available from the preceding circuit. Thereafter it uses the inhibiting action of the current still flowing in the input winding. For a ZERO transfer, there is no signal on the input winding. The two stopper cores linked by the source loop are switched equally, exhausting the capacity of the flux source. When the lower stopper core switches, it causes the auxiliary source core to be switched, since they are coupled by the auxiliary loop. When the auxiliary source drive is applied in conjunction with the ONE clock drive, no further switching occurs, since it drives the auxiliary source core in the direction of the state which it is already in. The ONE clock is of insufficient magnitude to cause switching of either stopper core that it threads.

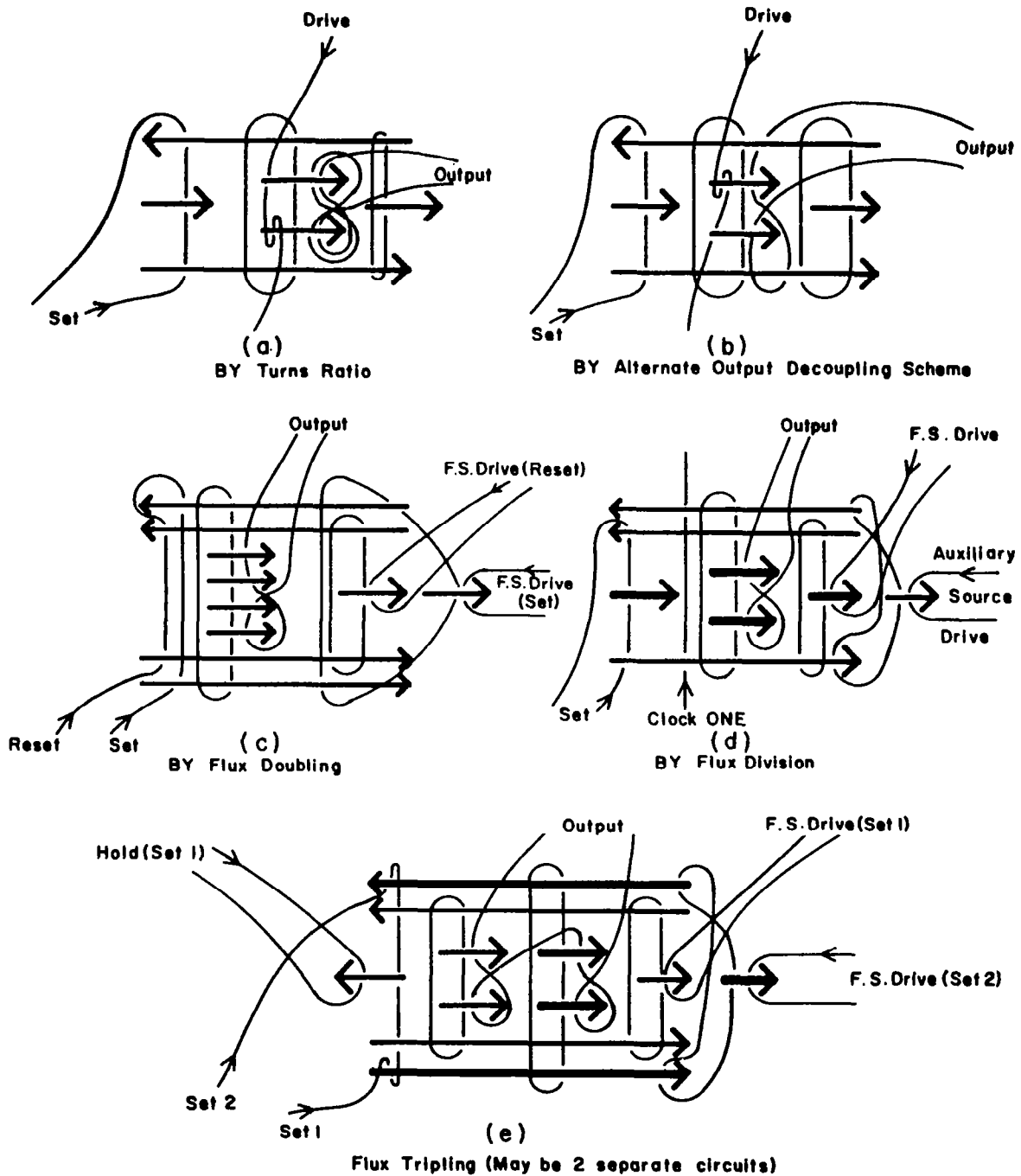


FIG. 7 FLUX GAIN CIRCUITS

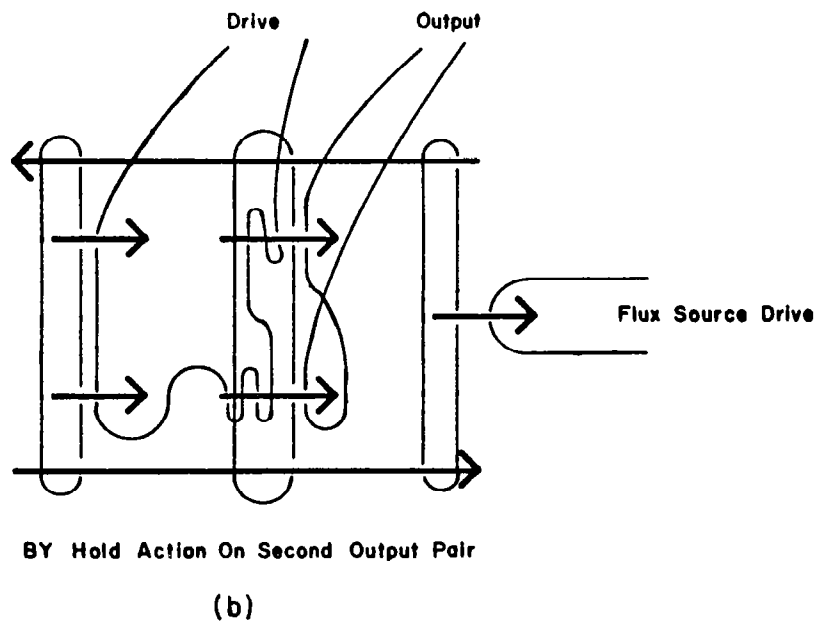
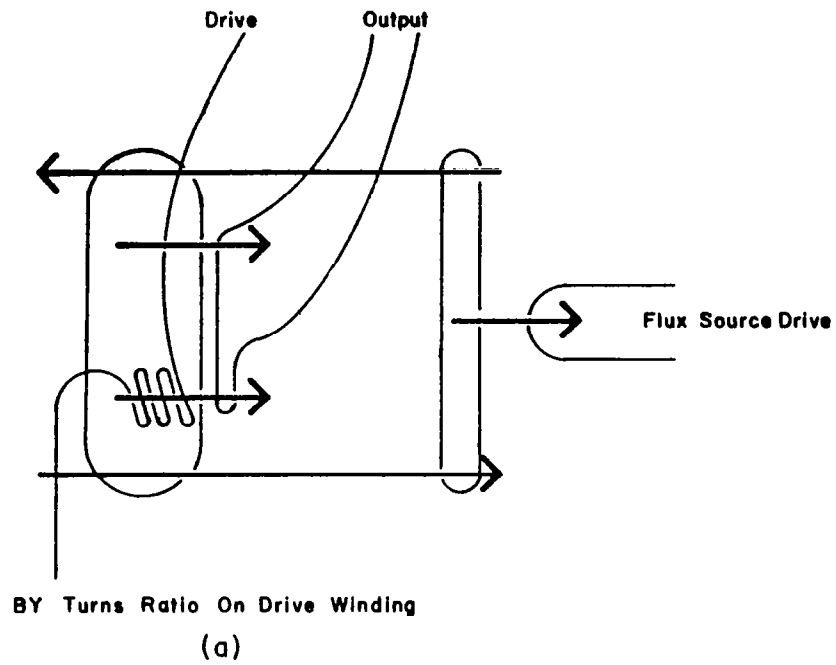


FIG. 8 CURRENT GAIN CIRCUITS

During a ONE transfer, the current in the set winding opposes the current from the flux source core through the lower stopper core and thereby prevents it from being switched. When the middle stopper core (with the associated partial switching of the output balanced pair coupled through the stopper loop) has fully switched, neither the flux source core nor the output pair from the preceding stage have fully switched.

The input appears as a low-impedance circuit to the previous stage and the input current continues, slightly increased to retard further switching of the output pair. This input current continues to inhibit switching of the lower stopper core until the source drive pulse terminates. Note that the auxiliary source core has not been switched since the lower stopper core has not been switched. When the auxiliary source drive is applied in this case, it switches the auxiliary source core and produces a current in the auxiliary source loop in a direction to switch both the upper and lower stopper cores. The direction of the ONE clock is such that it inhibits the lower one and aids the upper one, causing it to fully switch and set additional flux into the output balanced pair. The output from this circuit is as previously described.

The circuit shown in Fig. 7(e) is similar to the flux doubling circuit. In this circuit it is possible to achieve flux tripling, or the circuits may be divided and a straight transfer made to one circuit and a double flux transfer made to the other. To obtain this flux gain, two advance pulses are required. After the first advance, which is achieved in the normal manner, an advance drive pulse is applied to the transmitter in a sense opposite to the first. After the first output, the state of the output balanced pair is the same as produced by the alternate decoupling winding circuit in Fig. 7(b). The application of the second advance pulse drive then causes both output pairs to switch fully from one saturated state to the other. The flux linkage produced on the output winding is double that of the first advance drive. This input results in greater flux set in the second stopper circuit. The decoupling core is switched when the transmitter is cleared, since the output cores were not left in their clear state after the second advance drive. The output is obtained by connecting the windings of the two balanced pairs in series. This circuit may also be wired as in the flux doubling circuit by using a single stopper loop and placing all of the output cores on it.

The circuits for obtaining current gain are shown in Fig. 8. In Fig. 8(a), the winding configuration for obtaining current gain is shown. The multiple turns are placed on the output core which is driven in the clear direction. In this manner, the operation of the circuit when in the ZERO state is not altered, since at this point the output cores are both in the clear state and one is merely driven further in the clear direction and the other core is driven in the set direction, as before.

When the circuit contains a ONE, both cores have been partially set and the application of the drive pulse causes both to switch. However, the one core is driven harder toward the clear state. Stopper loop current will flow due to the unequal switching rates, and it will reach a value that will cause equal switching in both cores. For the three-turn winding shown, this current will be equal to the applied drive pulse. Since the stopper loop current is in such a direction as to subtract from one and add to the other core, each will have a drive equal to twice the applied drive. Thus, the output current which may be obtained is equal to twice the value less the current required to switch the output cores.

In the circuit shown in Fig. 8(b), the increase in output current is obtained by employing two output circuits. The drive current can be approximately twice normal value in this case, and hence the obtainable output current is likewise increased. When the circuit contains a ZERO, the drive pulse drives the one balanced core in the set direction and produces a stopper loop current. This current is in excess of the threshold of the stopper core, and so this current tries to switch it in the set direction. This in turn produces a current in the other stopper loop, but the drive pulse keeps the output pair associated with this loop in their clear state and the two stopper loop currents oppose each other in the bottom stopper loop. The result is that none of the cores switch.

When the circuit contains a ONE, the drive pulse causes both balanced cores of the one stopper loop to switch. The induced voltages cancel in this loop and current is not produced. In the other stopper loop, however, these cores were also set and the drive pulse causes these cores to be driven toward the clear direction, producing a current in the stopper loop. As long as this current doesn't exceed the threshold of the stopper core they will not be

switched. It is the magnitude of the current which may be applied to these cores by the drive pulse which determines the magnitude of the drive to the balanced output pair in the first loop. This is seen to be double the value of the normal circuit.

These circuits for obtaining both flux and current gain have been briefly described to indicate the various approaches possible. It should also be noted that various combinations of these circuits may be made to achieve both flux and current gain in the same circuit.

d. Logic Circuits

The stopper circuit is capable of providing a variety of logic functions. A list of these functions is given in Table I. As previously discussed, the basic functions required to provide a general logic capability are realizable. The ability to realize additional functions as well as being able to realize several functions by alternate circuits increases the logical flexibility.

The circuits that accomplish the repetitive outputs and fanout (in time) of 2 have been briefly described in connection with the composite circuit. The fanout (in time) of 3 is an extension of the same method. The last three functions listed in the table have not been used to realize the logic design but are included for completeness. The OR, AND, and NEGATION circuits are shown in Figs. 9, 10, and 11. Here those windings that are not pertinent to the logic function are omitted.

The threshold AND circuit is shown in Fig. 9(a). When the flux source drive is applied, an inhibit current is simultaneously applied through the stopper cores in a direction opposite to that required to set a ONE into the circuit. In the absence of inputs A and B the action of this inhibit current will cause an unbalance in the switching of the two stopper cores (the lower stopper core tending to switch more rapidly), which will produce a current in the stopper loop. This stopper loop current is in the direction to drive the output balanced pair in the clear direction (and so does not effect them). This stopper loop current acts on each stopper core to (nearly) cancel the effect of the applied inhibit current. The presence of one input signal, A or B, merely counteracts the effect of the inhibit clock current. The occurrence of both the A and B inputs causes the circuit to be set in the same manner as for a straight transfer.

Table I

LIST OF LOGIC CIRCUITS

Straight transfer	$A = U$
3 input OR	$A + B + C = U$
3 input OR	$A + B + C = U$
3 input AND	$A \cdot B \cdot C = U$
3 output AND	$A \cdot B \cdot C = U$
Fanout doubling	$A = U \cdot V$
Fanout (in time) 3	$A_{(t)} = U_{(t_1)} \cdot V_{(t_2)} \cdot W_{(t_3)}$
Repetitive Outputs 10 (at full drive)	$A_{(t)} = U_{(t_1)} \cdot U_{(t_2)} \cdot U_{(t_3)} \cdots U_{(t_{10})}$
Negation	$\overline{A} = U$
Sheffer stroke (NAND)	$\overline{A} + \overline{B} = U$
Pierce stroke (NOR)	$\overline{A} \cdot \overline{B} = U$
Exclusive OR	$(A + B) \cdot (\overline{A} \cdot \overline{B}) = U$

Figure 9(b) illustrates a 3 input inhibit AND circuit where the input winding is replaced with an additional stopper loop. Here the circuit inputs, including the inhibit clock, are made to the input core which is added to this loop. At the time of the flux source drive, the magnitude of the inhibit current is equal to that of two input currents, so the presence of up to two inputs will not switch the core from its clear state. The presence of three inputs overrides the inhibit current and, by switching the input core, produces a current in the input loop of the proper magnitude to set in a ONE. When the input signals terminate, the inhibit pulse will remain, since it must be of longer duration than the input signals, and tend to switch the input core back toward the clear state. This induces a current of opposite polarity in the input stopper loop and causes the decoupling core to switch. This limits the current below the threshold value of the stopper cores and the ONE set into the circuit is prevented from being disturbed by this terminal effect.

In Fig. 9(c), an output AND circuit is shown. In implementing this function, the outputs of two circuits are connected in parallel. When both outputs are present, the currents add to provide the necessary magnitude to set a ONE into the following circuit in a normal manner. For this reason the

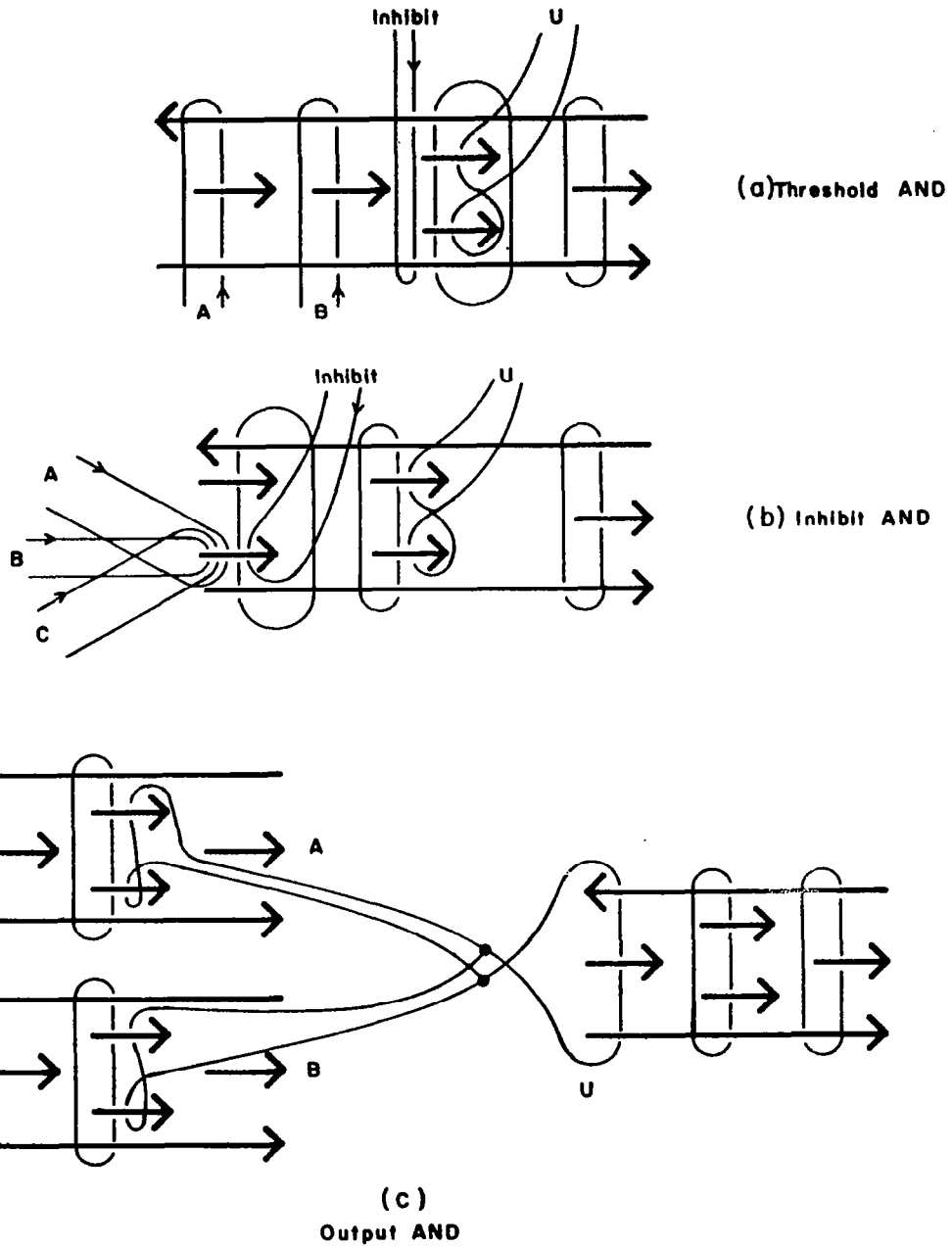
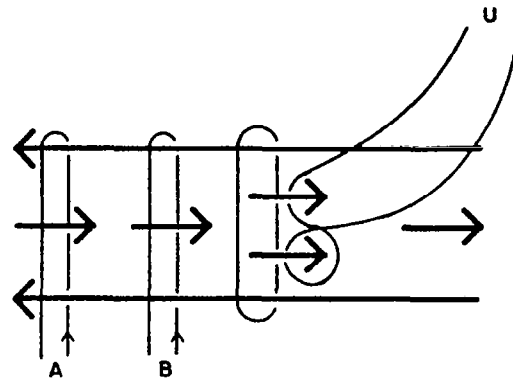
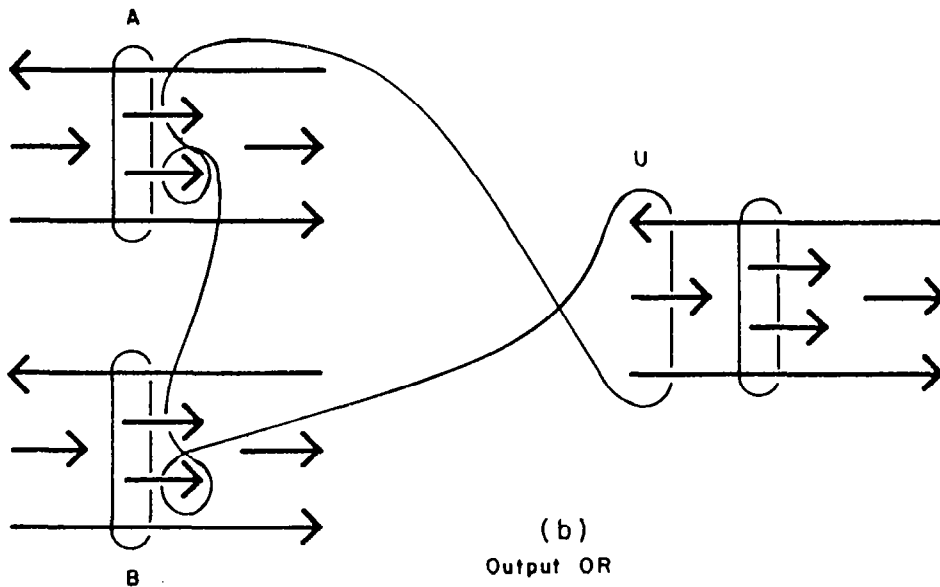


FIG. 9 AND CIRCUITS



(a)

Input OR

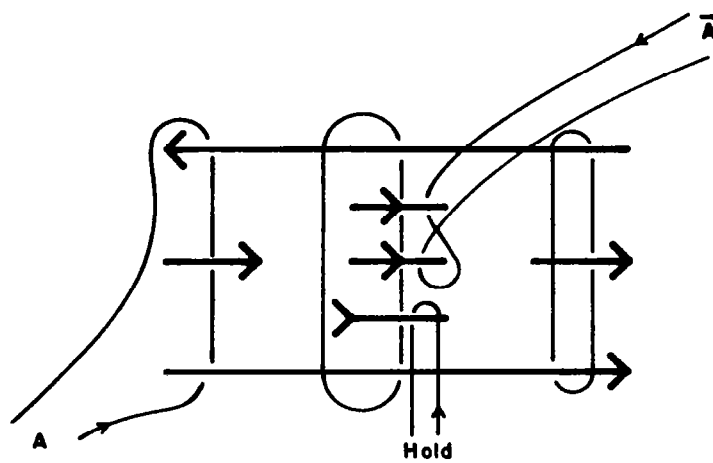


(b)

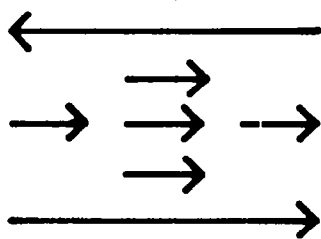
Output OR

FIG. 10 OR CIRCUITS

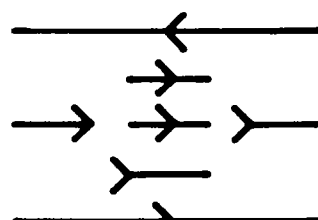
magnitude of the drive on the output balanced pair is reduced so that each circuit provides half of the required set current. When only one logic input, say B, is present, the current produced by this signal takes the lowest impedance path, which is the output winding of the A circuit. This current acts in the same direction as the drive current applied to this output balanced pair and results in an



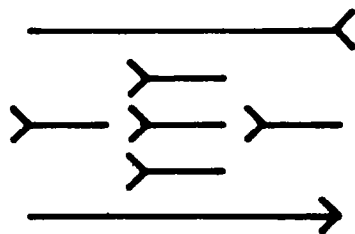
(a)
Negation, Clear Primed State



(b)
Clear State



(c)
ZERO State



(d)
ONE State

FIG. 11 NEGATION CIRCUIT

increase in the stopper loop current. The circuit is designed so that this current is below the threshold value of the stopper cores, and there can be no switching. This prevents an input signal from being impressed on the following stage.

The circuits in Fig. 10 show two methods of providing the OR function. The input OR circuit in Fig. 10(a) provides two input windings each threading a separate decoupling core, so that the presence of either input will result in a ONE being set into the circuit. The decoupling core on the other input switches and limits the current in this winding to a small value. The presence of both A and B inputs merely causes a ONE to be set in somewhat more rapidly.

The circuit of the output OR function is shown in Fig. 10(b). This function is accomplished by connecting the output windings of the circuits, whose outputs are to be ORed together, in series with each other and with the input winding of the following stage. The occurrence of an output from one circuit, say A, produces a current in this winding which opposes the applied drive in both circuits. When the B circuit contains a ZERO, it does not switch and the current acting on this circuit merely causes a reduction in the stopper loop current. This current also flows through the input winding of the following circuit, setting it into the ONE state in the normal manner. When both circuits are in the ONE state, a ONE is again set into the following circuit. However, the circuit becomes fully set when the two input circuits have only half completed their switching. The current increases slightly at this time which prevents further switching of the output circuits. Since both stopper cores are already saturated in the input circuit, no further switching can be produced; and thus the circuit remains fully set.

The circuit which performs the Negation function is shown in Fig. 11. In the operation of this circuit, it is desired to have the output balanced pair in the half-set state when in the logical ZERO state. To accomplish this, a third core is used in the stopper loop. When the circuit is cleared, all three cores threaded by the stopper loop are placed in the saturated states, as shown in Fig. 11(b). A prime pulse is then applied to the lower or prime core. This causes the balanced pair to achieve the half-set state shown in Fig. 11(e). A hold current is applied to this prime core at both input and output time, to keep

it in the primed state. Note that in the ZERO state, shown in Fig. 11(c), an output will be produced when a drive pulse is applied. The state of the output balanced pair is identical to the ONE state of the previously described circuits.

When the circuit is placed in a ONE state, shown in Fig. 11(d), the balanced pair is saturated in the set state. Application of a drive pulse tries to switch each in an opposite sense. The one core is saturated in the set state and cannot switch. The drive on the other core, which is in a direction to switch it, gives rise to a current in the stopper loop which prevents the core from switching, provided the magnitude of the current is below the threshold value of the stopper cores. The only difference between the Negation ONE state and the normal ZERO state is that the direction of the stopper loop current is reversed.

e. Experimental Results

Experimental models based upon the basic stopper circuit, the composite circuit, have been fabricated and tested in the laboratory. These experimental circuits are shown in Fig. 6 with the exception that two 3-1 turn drive windings were used (this is shown in Fig. 8(a)). The drive through the three-turn winding is always applied in the clear direction. These circuits contain two stopper loops to provide isolated outputs. One is the programmer output circuit and the other is the flux source pair associated with the BMC circuit which is completely contained in the experimental composite modules.

For the operation of these circuits, the resistance of the stopper loop is of prime importance. Therefore, various circuit fabrication methods were considered in order to find ways to achieve low stopper loop resistance and inductance. The experimental circuits were fabricated in the manner implied by the representation of the circuit in the arrow notation, shown in Fig. 6, considering this to be an exploded end view of the cores. A circuit assembled in this manner is shown in Figs. 12 and 13. The low resistance was achieved by the use of large diameter wire passing through the center of both the stopper and output balanced pairs of cores. These are shown protruding out of each of the output balanced pair. The largest diameter wire is associated with the flux source pair, because the magnitude of the resistance is most critical here. The low inductance has been achieved by using a flat copper

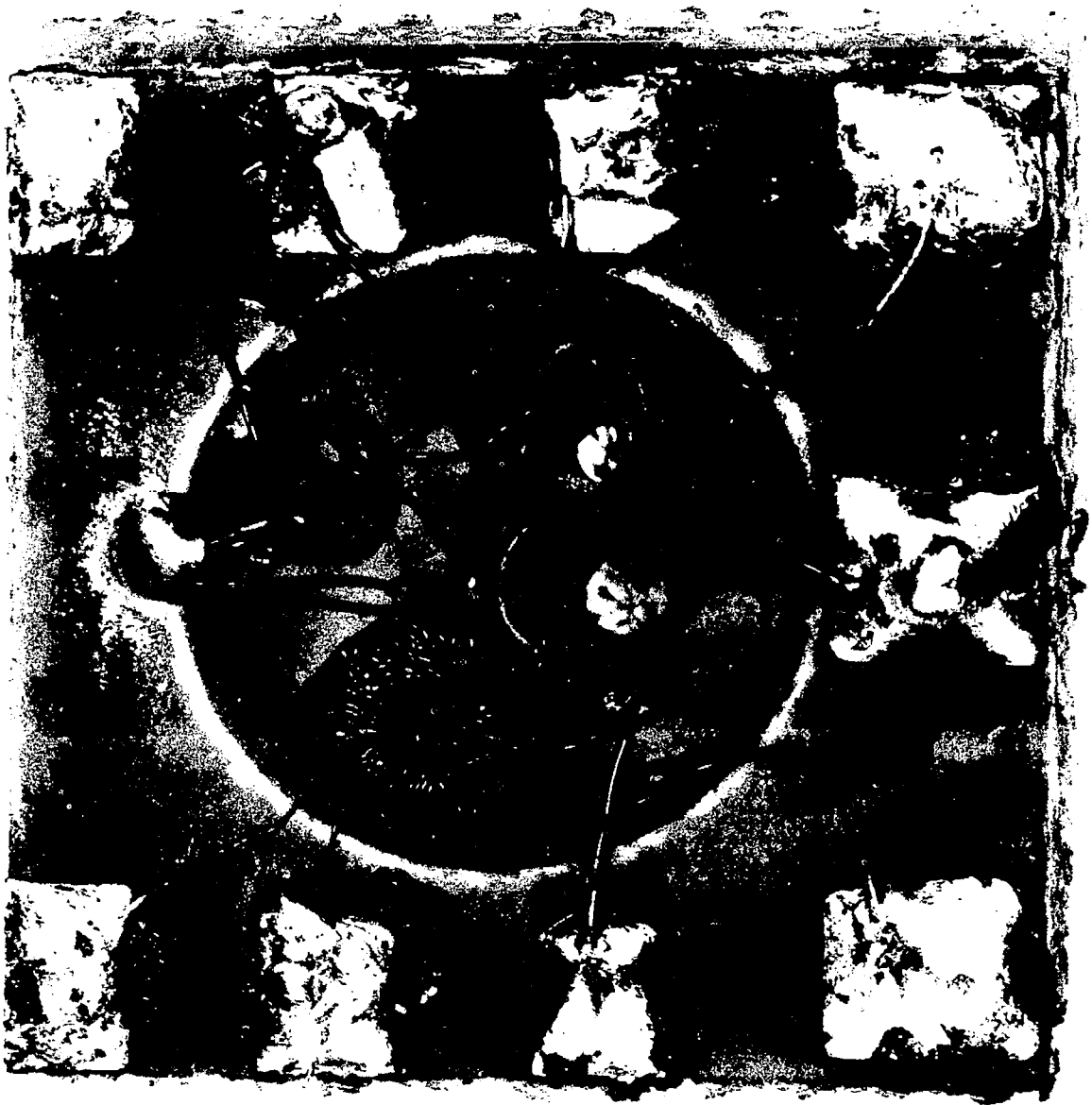


FIG. 12 COMPOSITE CIRCUIT: SHUNT REMOVED



FIG. 13 COMPOSITE CIRCUIT: COMPLETE ASSEMBLY

shunt, which is shown in Fig. 13 and which completes the electrical connection of the stopper loops. The shunt is common to and completes both loops, and it has a resistance about one third that of the large diameter conductor through the flux source pair. This loop has a calculated resistance of less than 0.2 milliohms.

The experimental investigation of this circuit established the high degree of isolation between the two output circuits. It also established that a minimum of ten consecutive read/restore drives could be applied to effect ten comparisons, when the circuit contained a ONE, and when the circuit contained a ZERO, the noise build-up was within predicted limits. These circuits were typically operated using two microsecond pulses with a two microsecond spacing between the read and restore pulses. Under these conditions the BMC circuit was switched in approximately one microsecond, and the output current obtainable from the output balanced pair was in excess of two amperes. This value is greater than that required to set in a ONE, and so the circuit exhibited current gain as expected, but which was below the value predicted from design considerations.

Subsequent investigation has established that a low threshold value and non-uniform thickness of the stopper cores were a major factor. The stopper cores were cut ultrasonically from larger cores (MAD's) which were on hand and marked as Indiana General S-4 material. These cores had a threshold value less than 70% of the characteristic value for S-4 material. Using a higher threshold material for the stopper cores and insuring a uniform cross-section is expected to materially improve the circuit operation.

B. Driver Circuits

1. Weight Current Drivers

The weight current drivers generate pulses of current having accurately controlled amplitudes. These drivers are a part of the weight current generator which includes a programmer and logic that is described later in this report.

Only a limited effort has been expended in developing a suitable driver circuit. This is an area that will receive attention in future work. There are

"brute force" methods available for achieving the necessary output characteristics, but these methods are wasteful in terms of power and number of semiconductors required. Our present thinking is in terms of one or possibly two transistors per driver, and there are seven drivers in the system.

A circuit which illustrates certain desirable characteristics is shown schematically in Fig. 14. This circuit uses feedback to control the amplitude of the collector current. The control element is the now familiar balanced pair that is driven by a flux source toroid. This source could be the output of a stopper circuit, which would logically control the circuit activation.

The tipping mmf for the balanced pair is the difference in amplitude of the mmf's from the collector current winding and the reference current winding. It is significant to note that when the flux source is switched and a voltage pulse

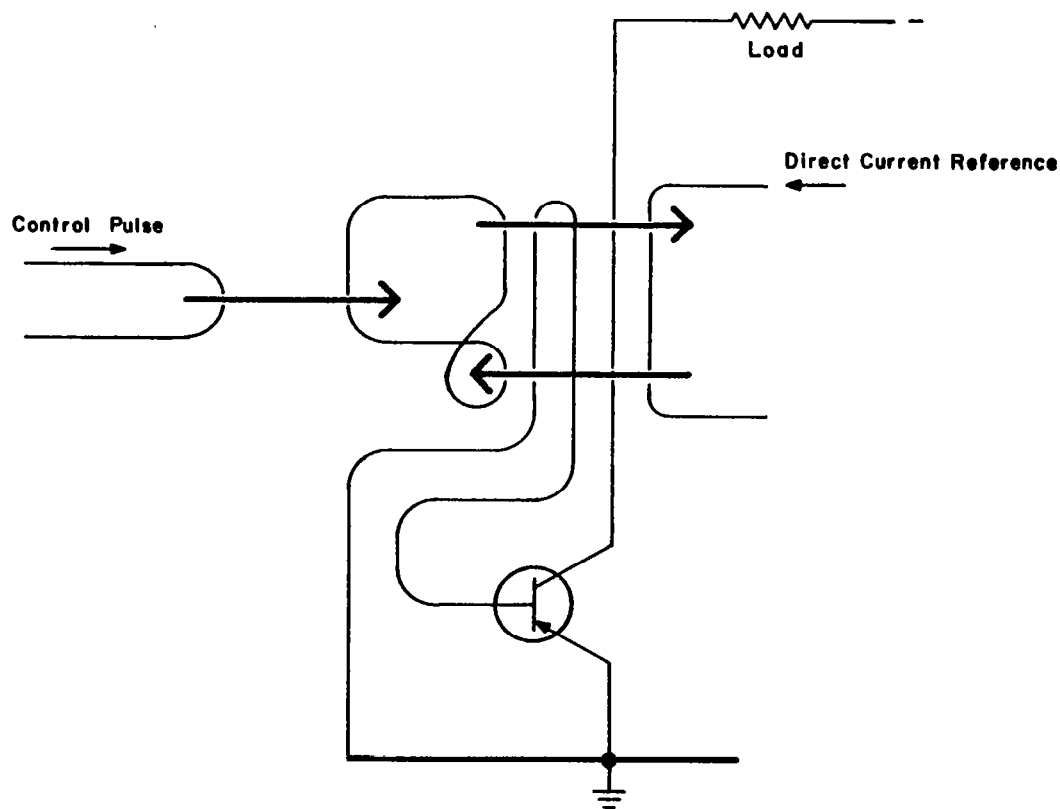


FIG. 14 ELEMENTARY DRIVER CIRCUIT

is present on the feedback winding, the amplitude of this pulse is proportional to the amplitude of the differential mmf and not to its time derivative. If a linear pulse transformer were used as the feedback control element, then integrating networks would be required to achieve amplitude sensitivity. The feedback voltage causes base current to flow in the transistor so that the collector current value is changed until there is no longer an amplitude difference in the mmf's between the reference winding and collector winding.

The use of feedback to accurately control amplitude is desirable since this makes it possible to use the same reference source for all the weight current drivers. In order to generate the seven current amplitudes that are needed from the seven drivers, appropriate turns ratios can be put on the balanced pair in each circuit.

Another desirable characteristic that this circuit provides is tolerance to temperature variations. The null point and sensitivity of the balanced pair is reasonably constant over a 100° C temperature range (see discussion and graph for the balanced magnetic comparator). A diode inserted in the base feedback circuit should minimize the effect of the transistor threshold variations with temperature.

Brief laboratory testing showed that the circuit does work qualitatively as expected and also emphasized the importance of the core switching characteristics upon circuit operation. The latter can be appreciated by assuming that the tipping mmf is constant throughout the period that the flux source is being switched and noting that the feedback voltage waveform will then be roughly triangular in shape. This in turn would make the collector current waveform have this same general shape rather than flat-topped. This difficulty can be overcome by increasing the gain in the feedback loop or by controlling the shape of the core switching waveform.

As stated at the outset of this section, only a limited effort has been expended on this driver problem during this phase of the work. The objectives that we expect to achieve during the next phase of work are to provide an input OR, proper turn-on and turn-off of the circuit, temperature tolerance, and precise current amplitude control.

2. Timing Generators and Logic Drivers

a. Desirable Characteristics

Digital magnetic circuits generally require pulses of current as the power source. A current source is needed rather than a voltage source, because the impedance of a string of cores on a line is a function of the information state of the core. Therefore, if a voltage source were used, the current magnitude would vary as a function of the information state. This could result in faulty operation, or at best very narrow tolerance limits. A high-impedance source, a current source, is also dictated by the effect that loading has on the switching speed and effective threshold of a core, and the resulting demagnetizing current that flows through other cores. This requires that the impedance of the source be high at all times.

The necessity for a high-impedance source for magnetics has resulted in high power consumption when the magnetic circuits are driven at a fast repetition rate, since the high impedance is obtained at the expense of power dissipation. The new drivers described below do not have this high power dissipation associated with them.

It is often desirable to generate several current pulses, or phases, as a sequential group upon the receipt of a synchronizing signal in order to simplify the logic structure. This multiphase characteristic is another feature of the drivers described below.

For spacecraft applications of magnetics still another feature of the power supply, one that is highly desirable, is that of reliability. High system reliability cannot be achieved without commensurate driver reliability. High reliability is a characteristic of the pulse power supplies described below because semiconductor components are minimized.

b. Evolution of Proposed Driver Circuits

It should be emphasized at the outset that the driver circuits we will be discussing have not been tested experimentally. However, the principles upon which circuit operation is based are well known and related circuits have been used practically.²³

The characteristics just described will be discussed by referring to several circuit diagrams (Figs. 15 and 16). Figure 15(a) illustrates one method that is currently being used to obtain current pulses. The capacitor C is charged through the resistor R_c to E volts. When the switch S is closed, the capacitor is discharged and current flows in a core circuit that has its switching

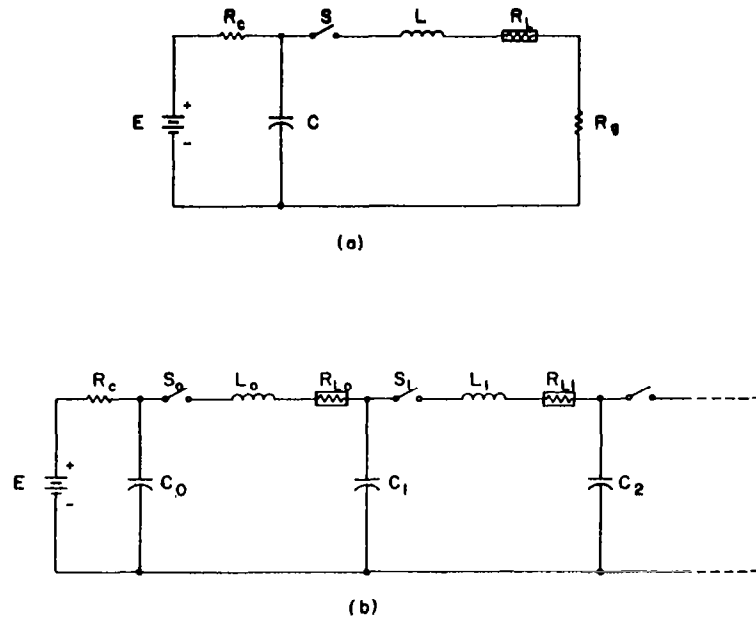


FIG. 15 PULSE CURRENT SOURCES

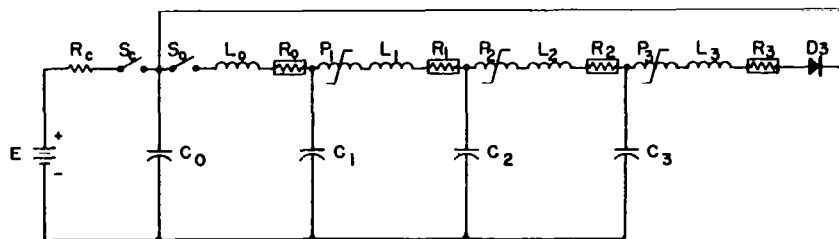


FIG. 16 EFFICIENT MULTIPULSE CURRENT SOURCE

resistance represented by R_L . By making the resistance of R_g many times greater than the maximum value of R_L , the current amplitude is made insensitive to the information state of the cores. The circuit is critically- or over-damped by R_L and R_g , so a unidirectional current pulse is obtained.

In Fig. 15(b), a proposed circuit is shown in which the resistor R_g has been replaced by a capacitor. Here other circuit stages can be connected by switch S_1 , etc. First consider the operation of the circuit with S_1 open. When S_0 closes the capacitor discharges as before, but the circuit is not critically damped and the charge is transferred to the capacitor C_1 . All of the charge on C_0 is transferred to C_1 by resonant charging when the current pulse through R_{L0} has passed from zero to a maximum and back to zero again. At this time, the switch S_0 is opened and the switch S_1 is closed simultaneously. Now the charge that resides on C_1 is discharged through R_{L1} , etc. By virtue of this energy transfer from capacitor to capacitor, we see that it is possible to efficiently generate many pulses in time sequence. The circuit could eventually be terminated by a resistance R_g as before. This would mean that several pulses have been generated with essentially the same power dissipation in the source as was present for the single pulse case.

Now let us consider the means by which a high impedance is obtained in this circuit without adding a resistor in series with each load. It can be seen that this is possible by examining the equation for the current in the first stage with S_1 open. Dropping the subscripts and setting $C_0 = C_1 = 2C$, the equation is:

$$i = \frac{E}{\omega_0 L} \epsilon^{-\frac{Rt}{2L}} \sin \omega_0 t = \frac{E}{\omega_0 L} \epsilon^{-\frac{\omega_0 t}{2Q_0}} \sin \omega_0 t ,$$

where $\omega_0 = \left\{ LC \left(1 + \frac{1}{4Q_0^2} \right) \right\}^{-1/2}$ and $Q_0 = \frac{\omega_0 L}{R}$. The maximum value of the

current between $\omega_0 t = 0$ and $\omega_0 t = \pi$ is the quantity of interest. If Q_0 is a very large number then $\epsilon^{-\omega_0 t / 2Q_0}$ is approximately equal to one, and the current maximum has the approximate value $E / \omega_0 L$. If Q_0 is 10, then the current

maximum is about 8% less than for the lossless case with $Q_0 = \infty$. Therefore, we conclude that if Q_0 is high enough, the current peak during the first half-cycle is substantially independent of the resistance value and hence independent of the information state of the cores.

Let us go back for a moment and try to apply this approach to obtain a high impedance for the circuit in Fig. 15(a) with the resistance R_g equal to zero. This time the switch S must be opened just as the current goes through zero. Note that if this were done, the initial charge on the capacitor would at this time again reside on the capacitor, but with reversed polarity. This charge would then leak off through the resistor R_c resulting in the power dissipation that we are seeking to avoid. To make effective use of the high Q_0 as a means for obtaining a high impedance source, a multistage circuit is required.

c. An Efficient Multipulse Driver

The circuit shown schematically in Fig. 16 makes use of the principles discussed above for the realization of an efficient multiphase pulse-current source. The key circuit element in this driver is an inductor having a core of square-loop magnetic material. When used in this manner, these inductors are termed "pulsactors;" they are designated P_1 , P_2 , and P_3 in the figure. This new circuit is based upon work initially done in the radar field with the Melville pulse compression network.^{23, 24}

In the circuit in Fig. 16, assume that the capacitor C_0 has been charged, switch S_c has been opened, and that switch S_0 is then closed. As before C_0 discharges, this time into C_1 and also into the network in parallel with C_1 . Now assume that P_1 has been previously saturated and that this discharge current starts the core switching toward the other saturation state. This pulsactor is designed such that the current required to do this switching is very small compared to the current that flows into the capacitor C_1 at this time. During this period the pulsactor acts like an open switch having a small shunt leakage current. The voltage-time integral across the pulsactor is designed to be essentially equal to the voltage-time integral that appears across C_1 during the first half-cycle of the discharge of C_0 . Therefore, as the discharge current just reaches zero, P_1 saturates. This in effect closes the

"switch", and the charge on the capacitor is now permitted to flow through the saturation inductance of P_1 and the inductor L_1 into C_2 . The switch S_0 is opened at the instant the pulsactor "switch" closes, so there is no reverse current flow through L_0 and R_0 . The saturation inductance of P_1 plus the inductance of L_1 equals the inductance of L_0 , so the discharge period of C_0 and C_1 are the same.

The capacitor C_1 discharges into C_2 in the same way that the first stage transfer took place. However, this time when C_2 is fully charged and P_2 has been saturated, the discharge current can flow through P_2 and P_1 . Since this current is in the direction to reswitch P_1 , the current magnitude through P_1 is small compared to that through P_2 . Therefore, the discharge of C_2 both drives a load, R_2 , and resets the previous stage. This same type of circuit behavior is present in the conventional Melville circuit, but there the discharge period of C_2 is much less than that of C_1 , so very little resetting of P_1 occurs. Since in our case, the discharge periods are essentially equal, P_1 is almost completely reset to its initial state, and very little time need be subsequently allotted to resetting.

This process of charging and discharging continues down the line until the last capacitor is charged, C_3 in this case. Since S_c and S_0 are open during the discharge of C_3 , C_3 discharges into C_0 and at the same time resets P_2 . Furthermore, since there are loads and therefore losses in each stage of this pulse source, the charge that is returned to C_0 is smaller in value than the charge that it had at the initiation of the cycle. To restore the level of charge to the initial value the switch S_c is now closed.

Note that the energy represented by the charge on C_0 just prior to the closing of switch S_c is not dissipated in a resistance in this circuit. This represents a substantial reduction in the required input power. Ideally, the only energy that has been dissipated is that which has been made use of in the load of each stage, and the remaining energy has been retained by feedback.

After C_0 is recharged, S_c is opened and, except for the state of P_3 , we are ready to repeat the operation. P_3 has not yet been reset to its initial condition. This reset can be accomplished many ways, one being to put

a separate reset winding on the pulsactor and place this winding in series with R_0 . P_3 would then be reset by the discharge of C_0 .

The purpose of the diode in the last stage is to prevent the discharge of the capacitor C_0 except as dictated by the switch S_0 . The switches S_0 and S_c will be transistors in a physical circuit. These will be triggered on (or off) at appropriate times and can be held on (or off) by feedback loops from succeeding portions of the network.

There remains one characteristic of this pulse-current source that has not been discussed. This is the impedance the source offers to a core that is being driven by another stage or by another pulse source. Since we no longer have the switches S_1 , etc., of Fig. 15, the circuit loops are not opened during the interpulse period. This problem will need to be considered for each individual pulse source and the circuits to which it is connected. It is probable, however, that no difficulties will arise from this situation if the pulse source has a sufficiently high Q_0 , so that it acts like a constant current source when a pulse is being generated. For example, if two identical stages are used to set and reset the same core, then when one source is switching the core with a unit value of current, the other stage will have at most about one-tenth of a unit of current flowing in it if the Q_0 of the circuits is 10.

The circuit schematic in Fig. 16 is the basic unit proposed for all the drivers in this system with the exception of the weight current driver. Several variations that add versatility to the basic circuit have been briefly considered. Some of these variations arise because there are two types of Melville circuits. The basic circuit we propose here is akin to the series type Melville circuits, but there is also a shunt type circuit that interchanges the positions of the pulsactors and capacitors. The operation of these two circuits is similar, but there are distinctions that may make one better suited than the other for a particular application. For example, the pulse width of one stage can be made greater than the preceeding stage using the shunt circuit; also, the shunt circuit has less run-down from stage to stage, but the pulsactors need to be reset explicitly.

In summary, this new pulse source creates an efficient, high-impedance, externally-synchronized, multiphase source that uses a minimum number of semiconductors.

C. Sense Amplifier

The purpose of the sense amplifier is to detect a signal in the presence of noise and to amplify the signal to a predetermined level. We anticipate using conventional transistor circuitry to implement this amplifier. Noise will be discriminated against by making the amplifier polarity sensitive, by providing an amplitude threshold, and by strobing the amplifier to activate it only at prescribed time intervals.

Future possibilities include the use of the tipping mmf approach to magnetically implement the amplifier, and also the use of component redundancy techniques²⁵ to minimize malfunction due to semiconductor failure.

D. A Magnetically Implemented Telemetry System

1. Logic Description

One of the objectives of this project has been to generate a logic design for a typical telemetry system using all-magnetic logic techniques to determine the feasibility of this approach. A typical telemetry system has been defined (for the purpose of this project) as consisting of six supercommutated channels, six prime channels, and two prime synchronization channels. Two of the prime channels will be digital and combined, will represent the state of 14 SPST switches. The accuracy of the system is to be 7 bits, the output bit rate is to be between 500 and 1,000 bits per second, and the primary time source is to be a crystal controlled clock operating at 100 kc or above. The system is to operate over a temperature range of 60° C minimum, however a temperature range of 100° C is to be actively sought. Power for this system is to be supplied from a single voltage source not to exceed 30 volts. This is exclusive of the precision voltage source required for generating binary weight currents.

The logic diagram showing the design of this system is shown in Fig. 17. Throughout this section, reference to this figure is implied by reference to specific logical units, i.e., channel B, buffer register, or program counter. The symbology used is described in Appendix C. This logical design is based on the capabilities of the circuits described in the preceding sections. It is to be noted that this logic design represents but one of several possible designs.

Alternate methods have been found for performing all the required logic functions with the exception of the comparison function. The particular design selected does not necessarily represent an optimum one as the emphasis was on establishing feasibility. However, this design is representative of what may be accomplished by the use of all-magnetic circuit techniques. It is important to note that the validity of this study does not hinge upon the requirement that each and every logic circuit perform precisely as anticipated. The comparison circuit upon which a large segment of the logical design is based has been heavily tested in the laboratory to preclude this possibility.

a. Master Programmer

In this design, the sensor for each analog channel--supercommutated channels 1 through 6 and prime channels A through D--is directly connected to its associated BMC circuit. The maximum output of each sensor is in itself insufficient to cause switching of the balanced magnetic elements, but it is connected in such a manner as to produce an unbalance signal. The BMC circuit is used as a null detector as described in a preceding section. Each digital sensor is directly connected to a small toroidal core referred to as the digital sensor input core and abbreviated DSI. They are associated with each of the digital channels E and F. The outputs from seven such cores are connected in turn to the BMC associated with one digital channel. In the case of the digital channels, the weight currents are not connected to the BMC, but instead are connected so that the output from each of the weight current drivers threads one of the seven small toroids in each digital channel. This is shown schematically in Fig. 18. When each DSI core is read out by the appropriate weight current pulse, an output signal will be developed on the output winding threading it if the digital sensor is closed. Alternatively, an output will not be developed if the digital sensor is open. The effect of an output developed by a DSI core on the BMC is to produce an unbalance indication, which in turn will appear as a binary ZERO in the corresponding bit position of the output word for that digital channel. This information is stored in the associated bit position in the digital channel output buffer register abbreviated ORD. This is shown as the third horizontal row of logic elements, from the top, in the weight current generator section of Fig. 17.

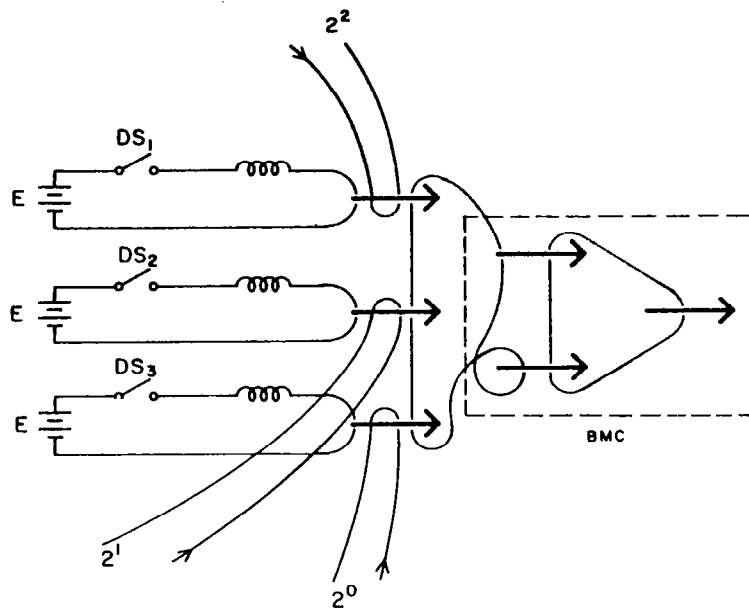


FIG. 18 DIGITAL CHANNEL INPUT CIRCUIT

The mode of operation for the digital channels differs from that of the analog channels in that only one weight generator driver is turned on at a time; that portion of the logic needed for the analog channels is disabled at this time. The two channels allotted to the synchronization code, channels sync 1 and sync 2, are operated as digital channels--the difference being in the manner in which the BMC circuit is unbalanced. The weight currents for those bit positions which are to contain a ZERO are threaded through the appropriate BMC in the same direction as in the analog channels. When a weight current driver is turned on, a ZERO or a ONE is transferred into the associated bit position of the buffer store (ORD) according to whether or not the current threads the BMC.

Each BMC is driven by an output from the stopper circuit associated with that channel. Commutation is accomplished by transferring a ONE into the stopper circuit associated with the channel that is next in the predetermined commutation sequence, and then by clearing the ONE out of the channel for which digitizing has just been completed. Where the next channel is uniquely

assigned, the programming function is simply implemented by means of a direct transfer between the appropriate stopper circuits. (The stopper circuits associated with each channel that provide the programming function hereafter are simply referred to as programmers. They are shown in Fig. 17 as the second vertical row of logic circuits, from the left, in the comparator, programmer, and commutator section.) This is the case for the transfers between the supercommutated channels. The programmers for these channels provide the complete commutation and programming function and are collectively referred to as the superchannel programmer.

For those cases where the commutation sequence is not unique, the output from the programmer is connected to the inputs of all other programmers to which commutation must be effected in order to realize the necessary frame commutation sequence. This provides one input of a two input inhibit logic AND gate which is formed at the input of each of the stopper circuits associated with these latter channels. An eight stage counter circuit, called the program counter, determines the sequence in which these channels are to be commutated and provides the necessary second input to effect transfer to the selected channel. This is the case for the transfer out of the last supercommutating channel--channel 6--which must alternately be transferred to channel A, channel C, channel E and channel sync one.

The program counter circulates a ONE, properly phased relative to the ONE sequencing through the super channel programmer so that when the output from channel 6 occurs it will provide the necessary gating input on one of the four channel input gates. The program counter is shown as the third vertical row of logic elements, from the left, in the comparator, programmer and commutator section of Fig. 17. The phase relation between the program counter and the channel commutation sequence is tabulated in Appendix D. The input to each odd stage of this counter is likewise an inhibit logic AND gate. The negation output produced from the channel 6 programmer provides an enabling input to each of these counter stages whenever channel 6 does not contain a ONE. Under these conditions the program counter acts in a normal fashion and recirculates the ONE. The output from each even stage is connected to the succeeding odd stage and also to the input of one of the odd prime channels. This provides one input to the AND gates formed at each of these inputs. Normally,

transfer into the prime channels is inhibited due to the lack of an enabling pulse from channel 6. When the ONE is transferred out of channel 6, the condition of the input gates on the odd prime channels and the input gates on the odd stages of the program counter are reversed: the odd prime channels are enabled and the odd stages of the program counter are inhibited. The enabling pulse output from channel 6 is presented simultaneously to all of the odd prime channels and an output from an even stage of the program counter is presented to one of the odd prime channels resulting in the transfer of the ONE to the appropriate prime channel. The ONE has been transferred from both a super channel programmer and the program counter, with the result that both are void of a ONE.

The transfer out of each odd prime channel programmer is uniquely defined, so that when the conditional transfer has been made to the odd channel, A for example, commutation will be to the next even channel, channel B in this example. An output from all of the even prime channel stages is connected in a logical OR to provide the input to supercommutating channel 1 so that the transfers from every even prime channel is to channel 1. A second output from each of the even prime channels provides for a unique transfer to one of the odd stages in the program counter. The output from each even prime channel goes to a different odd stage of the program counter. In this manner the phase of the ONE circulating in the program counter is shifted after the commutation of each prime channel pair. It is the phase of the ONE circulating in the program counter that determines the selection of the next pair of prime channels. For example, if the transfer had been made to the programming circuit of channel A upon the transfer out of channel 6; the succeeding transfer out of channel B would be made to the input of channel 1 and also to the input of the third odd stage in the program counter, two stages ahead of its position had the program counter been operating in its normal cyclic mode. At the next transfer out of channel 6, the corresponding transfer from the program counter would be out of the first even stage into channel C. In this manner all of the prime channels are sequenced by pairs, producing the frame commutation pattern 1, 2, 3, 4, 5, 6, A, B, 1, 2, 3, 4, 5, 6, C, D, 1, 2, 3, 4, 5, 6, E, F, 1, 2, 3, 4, 5, 6, sync, sync.

b. Timing Generator

The function of the timing generator is to provide timing signals for all of the control signals needed during the interval bounded by commutation to adjacent channels. These signals fall into three general categories: those needed to provide channel commutation; those which are needed to produce digitizing; and those which provide the serial-by-bit system output. The logical design used to accomplish this function effects a compromise between the number of transistors and the number of cores required. Four ring counters are used together with the necessary drivers. Because the power requirements of magnetic circuits are directly proportional to the operating speed and the number of elements operated at this speed, the length of the counters are adjusted to take advantage of this characteristic. The shortest of these counters, a four-bit counter, is the high speed counter, the input of which is the output from the crystal controlled oscillator circuit at a frequency of 125 kc. The majority of the power required to operate the timing generator is consumed in this circuit. The output of this 4-stage counter provides the input to the following 6-stage counter which operates at $1/4$ of the clock frequency, or a little more than 31 kc. The power required to operate this counter will be less than half that required to operate the 4-stage counter. The output of the 6-stage counter forms the input for the next 10-stage counter. The power consumption of this counter is less than that of the 6-stage counter, as it operates at $1/6$ the speed of that counter, or $1/24$ that of the 4-stage counter. The same considerations apply here and power consumption will be less than 11% of that of the 4-stage counter. The output of the 10-stage counter then provides the input for the final 14-stage counter. This counter operates at $1/10$ the speed of operation of the 10-stage counter or $1/240$ of the high speed 4-stage counter. This counter is three and a half times longer than the 4-stage counter and thus dissipates less than 1.5% that of the 4-stage counter. This final counter provides the timing and the read-out pulses which serially read out the buffer store and produce the system output at 520.83+ bits per second.

Producing the 7-bit output word requires only an odd number of counter stages, but in order to obtain a cyclic counter an even number of stages is required. It was found convenient to make this counter twice the bit length and to produce each output from two stages, one in the first half and one in the last half of this counter.

The read/restore pulse drive, L_2 , is turned on to provide seven pairs of drive pulses, with a sixteen microsecond interval between pulse pairs. L_2 is turned on once during each channel commutation interval. This is accomplished by controlling the presence of the signals on the inputs of the AND circuit formed at the driver input. These input signals are produced by the T_9 output from the even stage driver of the 4-stage counter which drives certain stages in each counter and additionally provides the inhibit signal for the AND circuit. This T_9 drive pulse occurs every sixteen microseconds, and it determines the interval between pulse pairs when all input signals are present. The presence of a signal on each input line is controlled by the states of the appropriate stages in the three other counters, each of which is connected to one input and provides the following timing control: the 8-stage counter determines the number of pulse pairs; the 10-stage counter determines the time position of the encoding aperture in the interval between successive bits of the system readout; and the 14-stage counter determines that the digitizing occurs between the readout of the seventh bit of one channel and the first bit of the succeeding channel.

Drivers L_3 and L_4 are turned on in a similar manner. These drivers provide the odd- and even-drive pulses for the operation of the logic circuits associated with the weight current generator and the buffer store registers. These drivers are to be turned on alternately. This is accomplished by adding a fourth input to the AND circuit formed at the input of each of these drivers. This input is obtained from the 4-stage counter, the first odd stage is connected to driver L_3 , and the second odd stage is connected to driver L_4 .

These three drivers then, are turned on only during the encoding interval for each channel. Driver L_2 is turned on seven times, driver L_3 is turned on four times, and driver L_4 is turned on three times during each channel commutation interval. The detailed timing for this system is given in Appendix E. The timing pulses used to drive the odd- and even-channel commutating pulse drivers, L_1 and L_5 , are provided by outputs from the 14-stage counter. The drivers are alternately turned on every 13,440 microseconds to produce a channel commutation rate of 74.4+ channels per second. This is the basic clock rate for operation of the master programmer: both the programmer circuits associated with each channel, and the program counter. The complete program requires 32 channel commutations for a total elapsed time of

430,080 microseconds for a frame rate of slightly less than 2-1/3 frames per second. It is interesting to note here that the output of channel sync two would be the logical point to obtain the input to an additional long term counter. For example, replication of the counter used in the timing generator would provide an additional countdown of some 3,360 for a total elapsed time of approximately 24 minutes. The additional power consumption resulting from such an addition would be but a few milliwatts.

c. Weight Current Generator and Output Buffers

The weight current generator provides the weighted currents necessary to digitize by the method of successive approximation.⁶ The weight currents must be turned on, initially, in order of decreasing weight. When a comparison yields the result that the measurand current is equal to or greater than the sum of the weight currents applied, that driver is to be turned on for the remaining comparisons necessary to complete the digitizing of the measurand being sampled. The logic to implement the sequential turn-on of the weight current (or bit) drivers is provided by a ring counter seven stages long, referred to as the weight generator programmer (WGP). This commutation is effected in a similar manner to that for the channel commutation. The WGP is shown as the second horizontal row of logic elements in the Weight Current Generator section of Fig. 17. The stage containing the ONE determines the bit driver to be turned on at comparison time by the read drive pulse τ_2 . As the ONE steps through the ring counter, the bit drivers are turned on in order of descending weight. The logic to allow for the repetitive turn-on of a bit driver under logical control is provided by the conditional transfer of the ONE from the ring counter into the bit position associated with each driver in the analog storage register (or output register analog ORA). The analog storage register is shown as the top horizontal row of logic elements in the weight current generator section of Fig. 17. The read drive pulse τ_2 is also applied to each bit storage position in this register, providing a signal to turn on each driver having a ONE in its associated bit position. The conditional transfer is accomplished by the inhibiting action of the output from the sense amplifier, which prevents the transfer of a ONE from the WGP. The output from the sense amplifier occurs for comparisons where the measurand is less than the sum of the weight currents.

When the digitizing of the measurand information is completed, there remains in the buffer storage register the binary representation of the measurand current. Up to this point, this storage register has served the purpose of providing the memory required to achieve repetitive turn-on of the weight current drivers. However, since the form of the stored information to achieve this operation is the binary representation of the measurand current, this register also serves the purpose of providing the speed buffering between the digitizing bit rate of 62.5 kc and the output bit rate of 520.83+ bits/per second. This is achieved by a direct readout of the storage register from the 14-stage ring counter of the timing generator. This output from each storage register stage is isolated from the output which connects to the associated weight current driver. The isolated outputs from all of the stages are connected to form a logical OR which provides the binary, bit serial output of this system on a single output line.

For the digital and sync prime channels, the repetitive turn-on of the bit drivers must be suppressed so that only the sequential turn-on of the drivers occurs. This is accomplished by providing a second 7-bit storage register, the digital storage register. The ONE transfer out of the weight generator programmer is directed either to the analog storage register or the digital storage register, depending upon the state of a special control circuit. This circuit keeps track of whether a digital or analog channel is being sampled. When this circuit contains a ONE, the transfer is directed into the digital storage register. A ONE is transferred into this control circuit upon commutation to prime channel E or to sync 1 under control of the program counter stage associated with these channels. The ONE so inserted into the control cores at this time remains there for two commutation intervals, since the prime (including sync) channels are commutated to by pairs. This circuit is then cleared by the even channel clear pulse. When this circuit is in the ZERO state, the ONE transfer out of the weight generator programmer is directed to the analog storage register. The conditional transfer is effected in a manner analogous to the conditional transfer between the program counter and the prime channel programmer. (The major logical difference is the addition of the inhibit pulse from the sense amplifier.) Upon completion of the sequential turn-on of the weight drivers, the state of seven digital sensors (or seven bits of the sync

pattern) is stored in the digital storage register. This information is read out serially-by-bit by the same readout pulse, derived from the 14-stage counter in the timing generator, as is used to read out the analog storage register. After the last bit of the channel word has been read out of the storage registers, they are cleared by the action of the channel advance drive pulse, τ_0 or τ_{49} .

2. System Specifications

The specifications defining a typical telemetry system, upon which the investigations undertaken in the first phase of this project have been based, were arrived at jointly with Langley technical personnel and form the basic specifications of the preceding logical design. They are given in Table II. Additional specifications describing the system performance are given in Table III.

Table II

TELEMETRY SYSTEM SPECIFICATION

SAMPLING SCHEME: Six supercommutated channels designated 1-6, six prime channels designated A-F, and two prime channels allotted to a synchronization code. The sampling sequence will be 123456AB123456CD123456EF123456 sync.

CHANNEL SENSITIVITY: All supercommutated channels will be maximum sensitivity. Two prime channels (A and C) will be minimum sensitivity. Two prime channels (B and D) will be 5 ma full scale. Two prime channels (E and F) will be digital and together will represent the state of 14 SPST switches. All analog inputs should be isolated from system ground.

ACCURACY: Seven bit.

SYNCHRONIZATION CODE: 11111010011000

SPEED OF OPERATION: Output bit rate should be in the region of 500-1000 bits/second. A crystal controlled clock operating at not less than 100 kc should be used as a frequency reference.

TEMPERATURE RANGE: A minimum operating temperature range of 60°C should be achieved. The ultimate goal should be a 100°C range of operation.

POWER SUPPLY VOLTAGE: Any single dc voltage not exceeding 30 volts.

Table III

SPECIFICATIONS FOR SYSTEM SHOWN IN FIGURE 17

Maximum channel sensitivity:	1 milliamps full scale
Encoding interval:	96 microseconds
Power consumption:	less than 10 watts
Number of magnetic circuit modules:	81
Number of magnetic circuit drivers:	13 5 for logic, 8 for the timing generator
Number of weight current drivers:	7
Sense Amplifier:	1
Oscillator circuit:	1

Based upon the use of the all-toroid version of the stopper circuit and the use of the high-efficiency pulse driver circuit, the estimated number of components required by this system is given in Table IV.

Table IV

LIST OF COMPONENTS

Magnetic elements	702
50/80 memory cores	500
30/330 stopper toroids	162
pulsactor cores for drivers	40
Transistors	50
for logic drivers	10
for timing generator drivers	16
for weight current generator drivers	14
for sense amplifier	7
for oscillator	3
Diodes, for drivers	13
Capacitors, for drivers	40
Inductors, for drivers	40

E. Reliability

The original intent of this study was to attempt to determine a reliability figure for magnetic ferrite elements. There has existed a strong feeling that magnetic ferrite elements were "quite reliable," however no acceleration life tests were known to have been attempted in order to determine a reliability figure and establish it on a firm basis. To accomplish this, first a failure mechanism must be found (or postulated on theoretical grounds), and secondly a method for accelerating the failure process must be established. In an attempt to determine if a failure mode was known--or suspected--discussions were held with technical personnel from three ferrite core manufacturers: Ampex Computer Products Co., division of Ampex Corp.; Electronic Memories, Inc.; and the Electronics Division of Indiana General. The results of these discussions may be summarized concisely as--magnetic ferrite cores of the manganese-magnesium class do not fail in service--so long as they are operated within their physical limits, even when operated in severe environments including temperatures up to at least 250°C. * No one contacted in these discussions had firsthand knowledge of even a single magnetic core failure after it had been assembled and tested in a memory array. It is apparent that the reason a quantitatively based reliability figure for such magnetic elements has not been established is that there is no failure data.

With this finding, the reliability of the assembled magnetic circuits would appear to be determined by factors other than the inherent reliability of the magnetic element. The reliability portion of this study was redirected toward the factors affecting the reliability of magnetic circuits. The approach has been to investigate all known possible modes of failure from a "physics of failure" standpoint, rather than relying on the meager data available from failure reports. The aim of improving the understanding of failure modes is to insure that the near perfect reliability inherent in magnetic devices is not jeopardized at any point during fabrication, assembly, or packaging of circuits into systems.

*Data supplied by Indiana General resulting from tests of core characteristics under conditions of prolonged exposure at elevated temperatures show essentially no change over a four month period when the temperature was maintained at 275°C.

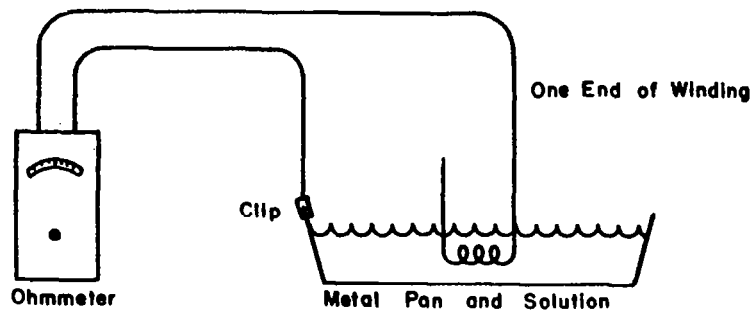
During the wiring and assembly of circuits, it is possible to damage the ferrite by excessive mechanical stress caused by either the holding jig, or by pulling wire around a sharp corner of an aperture in the ferrite. Three rather distinct cases result: (1) If the stress is high enough, the core breaks, and the damage is obvious. The net result is higher production cost, rather than decreased reliability; (2) If the core damage is slight (so that a corner chips, for example) the effective area of the aperture leg is decreased, resulting in the switched flux becoming marginal; and (3) The core material is stressed so that a crack is started, causing a latent mechanical defect with the potential of developing into a serious magnetic defect at some later time.

Case (2) is serious, but is usually detectable by careful electrical testing. This kind of defect has been observed in completed circuits. Case (3) is the most serious, but has not been observed in the newer, high-quality ferrites. Such a defect would be hard to detect, partially because it would be very infrequent and partially because it may be masked by cases (1) or (2).

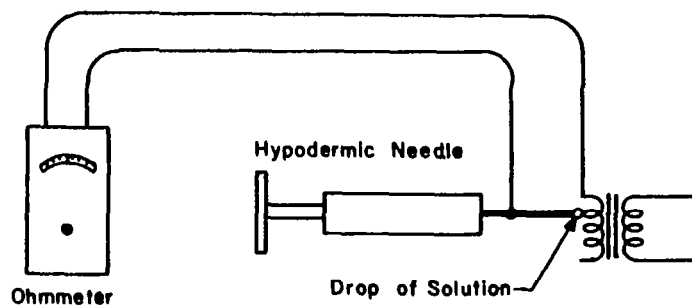
To eliminate damage while holding cores for winding, we have made experimental holders which are weak enough so that safe mechanical stresses in the cores are not exceeded. Looking for defects in the wire insulation provides a measure of stress of the core. The theory is that if the insulation is undamaged, then the stress on the core produced during winding is low enough to be safe.

To detect wire insulation defects, we have used a conductive solution test. The completed magnetic circuit is immersed in a water and detergent solution, and the insulation resistance from winding to solution is measured. Note that the wire should be tested before being used to wind a circuit. This test is depicted in Fig. 19(a).

An alternate method is to use a hypodermic needle to apply the conductive solution to selected windings or winding sections. This is shown in Fig. 19(b).



(a)



(b)

FIG. 19 INSULATION TEST METHOD

V AREAS FOR FURTHER RESEARCH

During the investigations undertaken in the first phase of this project, several areas have been uncovered where further research is indicated. This additional effort would be expected to produce significant improvements in system performance over those provided by the feasibility design arrived at in this first phase. These improvements would be in the form of a further reduction in the number of semiconductor components, a reduction in the power requirements, an increase in system accuracy to eight bits, an extension in the temperature range of operation, and an increase in the channel sensitivity in order to permit the use of higher impedance sensors.

The first area, the one which offers the opportunity for the greatest improvement, is the timing generator. It is in this portion of the logic that over half of the power in the system is consumed and sixteen--just under one third-- of the transistors are accounted for. Two approaches to effect a reduction in power and in the number of semiconductors offer promise. They are to obtain a more efficient magnetic means for counting down from the (relatively) high frequency crystal oscillator or to find a suitable high-stability, low-frequency oscillator.

The generation of weight currents is another area that needs further study. The drivers that provide these currents use fourteen transistors, the second largest number required to provide a logic function. It does not appear possible, at the outset, to eliminate all semiconductors to implement this function; however, it may be possible to replace some of the transistors by diodes, since it is generally simpler to apply redundancy to diodes than it is to transistors. In the present design, the encoding interval is determined in large part by the time required to reset the magnetic cores that control the magnitude of the weight currents. To increase system accuracy, this interval would have to be reduced. Additional effort directed at eliminating this reset time could result in reducing the encoding interval to under fifty microseconds, a reduction by a factor of two.

The sense amplifier is completely implemented by semiconductors. Although this circuit requires only seven transistors, it appears possible that this function may be performed completely by using magnetic circuits. The study of this area

would also include the problem of writing into memory directly from magnetic elements, a requirement anticipated for future systems.

Additional study of the balanced magnetic comparator circuit and the stopper circuit should result in improvements in both. These circuits are new and have the potential of increased performance over that required for this design. This is illustrated by the fact that very little effort has been spent in optimizing either circuit; in addition, the effect of materials on the performance has been but briefly examined.

The preceding areas offer potential improvements based upon present system requirements; consideration of requirements of future systems indicates additional areas for detailed study. Recognition of these areas does not stem from a specific study of future systems (we have made none), but rather from the attempt to be cognizant of potential future requirements, in order that the circuits used in the present design would be useful in these future systems. Studies of these areas would be directed at providing logic and circuit techniques to permit the use of higher frequency sensors; circuits to provide a long-term low-power counter; a capability to change the channel commutation rate and/or channel commutation program under both internal and external command; and expansion of the logic design to allow data preprocessing.

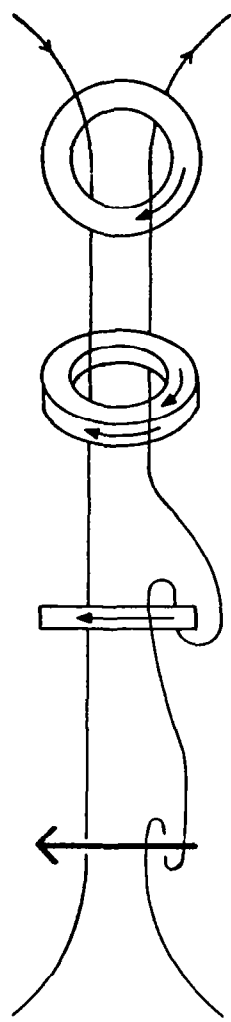
APPENDIX A

ARROW NOTATION

The arrow notation used throughout this report is an adaptation of the mirror notation.²⁶ This new notation has been found to be a useful and efficient means of representation for the all-toroid circuits. Each core is represented by a horizontal line segment, representative of an edge view of a core. The clear state is indicated by the direction of an arrow tip located on the segment. A winding which threads a core is represented by a vertical line that is broken above and below the line segment. A non-threading wire which passes a core is an unbroken line.

This is perhaps best explained by referring to the pictorial derivation of Fig. 20 which starts with a plane view and traces the evolutionary steps through to the arrow notation. Two conductors are shown threading each representation, one from the top, and one from the bottom of the figure. The direction of current in each is indicated by the arrow tip. Both produce flux changes in the core as indicated by the arrow.

In this notation, the length of the line segment indicates the relative size (diameter) of the core and the line thickness indicates the relative flux capacity of the core. The position of the arrow tip provides a convenient method for indicating the state of the core: when the arrow tip is placed at the front of the line segment (forming an arrow) the core is in its fully cleared state; when the arrow tip is located at the rear of the line segment, the core is in the fully set state; and when the arrow tip is located along the line segment, the core is in a partially switched state. The relative portion of the flux in the clear state is indicated by the relative portion of the line segment behind the arrow tip. These conditions are shown in Fig. 20(b).



(a)

←
Full Clear

—→
Full Set

—→
Full Set:
Double Flux Capacity

—←
 $\frac{3}{4}$ Set

—←
 $\frac{1}{2}$ Set

←—
 $\frac{1}{4}$ Set

(b)

FIG. 20 ARROW NOTATION

APPENDIX B

CORE SIZE RELATIONS

A. Core Size Requirements for Stopper Circuit Operation

Flux source drive must be equal to:

$$I_{Tf} + i_{mf} + I_T + (i_m/2) \quad (1)$$

where:

$$\left. \begin{array}{ll} I_{Tf} &= \text{Threshold of flux source cores} \\ I_{Tm} &= \text{Threshold of stopper cores} \\ i_{mf} &= \text{Excess drive required for flux source} \\ i_m &= \text{Excess drive required for stopper cores} \end{array} \right\} \text{ for equal } t_s.$$

The drive applied to the set input is not to exceed the stopper threshold I_T . Considering all cores identical in material characteristics and scaled linearly, one requirement for circuit operation is:

$$i_m/2 + I_T - I_{T0} - i_{m0}/2 \geq i_m \quad (2)$$

where:

$$\begin{array}{ll} I_{T0} &= \text{Threshold of output balanced pair} \\ i_{m0} &= \text{Excess drive required to switch output balanced pair,} \end{array}$$

or:

$$I_T - i_m/2 \geq I_{T0} + i_{m0}/2 \quad (3)$$

for a particular case where

$$I_{T0} = I_{Tf} = .31 \quad (4)$$

and

$$i_{m0} = i_{mf} = .26 \quad (5)$$

Substituting (4) and (5) into (3), we obtain:

$$I_T - i_m/2 \geq .44 \quad . \quad (6)$$

We define $M = \frac{\text{Diameter of Stopper Core}}{\text{Diameter of flux Source Core}}$, then,

$$M = \frac{I_T}{I_{Tf}} = \frac{i_m}{i_{mf}} \quad \text{or} \quad I_T = M I_{Tf} \quad (7)$$

and

$$i_m = M i_{mf} \quad , \quad (8)$$

then substituting (4), (5), (7) and (8) into (6), we obtain:

$$\begin{aligned} M(I_{Tf} - i_{mf}/2) &\geq .44 \\ M(.18) &\geq .44 \\ M &\geq .44/.18 \\ M &\geq 2.45 \quad , \end{aligned} \quad (9)$$

B. Output Current Determination

The output current which can be obtained by employing a 3:1 turn drive winding on the output pair is derived as follows:

To obtain core switching in both cores:

$$i_d + i_s - i_0 = I_{T0} + \frac{i_{m0}}{2}; \quad 3i_d - i_s - i_0 = I_{T0} + \frac{i_{m0}}{2}$$

$$i_d + i_s - i_0 = 3 \cdot i_d - i_s - i_0$$

$$\text{and} \quad \bar{i}_s = I_T$$

$$\text{then} \quad i_d = I_T$$

where:

i_d = drive current, i_s = stopper loop current and i_0 = output current.

$$i_0 = 2 I_T - I_{T0} - i_{m0}/2 \quad (10)$$

To allow transfer from stage to stage:

$$i_0 = I_{\text{set}} = I_T \quad (11)$$

as for the above case,

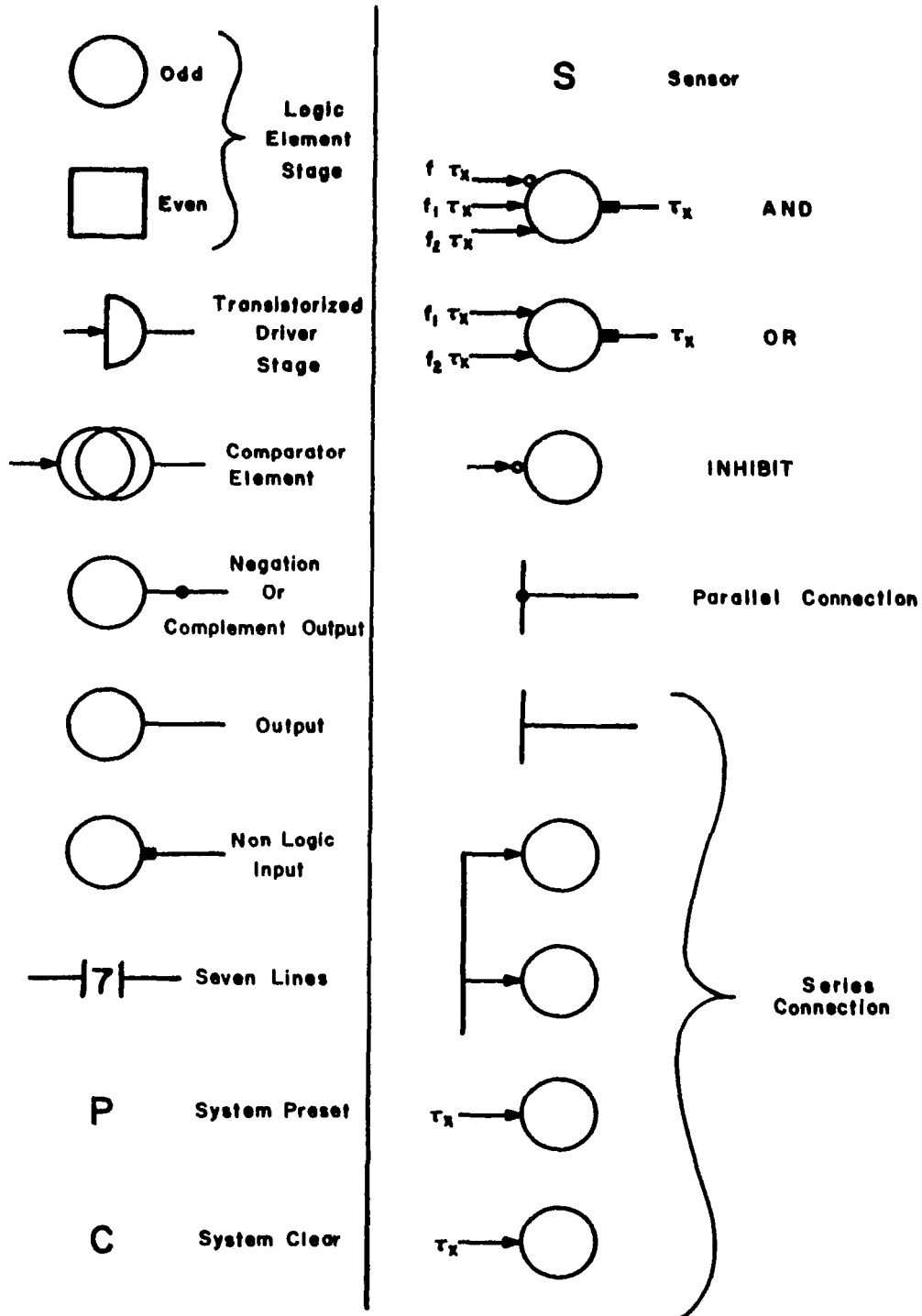
$$I_T = M \cdot I_{T0} \quad (12)$$

$$i_0 = I_T \left(2 - \frac{1}{M} \right) - \frac{i_{m0}}{2} = I_T \left\{ \left(2 - \frac{1}{M} \right) - \frac{i_{m0}}{2I_T} \right\} \quad (13)$$

$$= I_T \left\{ \left(2 - \frac{1}{2.45} \right) - \frac{.26}{2.31} \right\}$$

$$i_0 = 1.16 I_T . \quad (14)$$

Appendix C



Symbols

APPENDIX D PHASE RELATION

Program Counter: Channel Commutation Sequence

Channel Commutated	Program Counter Sequence
1	3
2	4
3	5
4	6
5	7
6	8
A	A
B	B
1	5
2	6
3	7
4	8
5	1
6	2
C	C
D	D
1	7
2	8
3	1
4	2
5	3
6	4
E	E
F	F
1	1
2	2
3	3
4	4

Channel commutated**5****6****S****S****1****2****Program Counter Sequence****5****6****S****S****3****4**

APPENDIX E TIMING TABLE

Elapsed time in microseconds			Pulse Width	
τ_0	0	Channel Advance Odd	2 usec	
τ_1	4	Channel Clear Odd	4 usec	
τ_2	32	WG output	6 usec	} 2^6
		Read WG Programmer	2 usec	
τ_3	32-1/2	Read BMC	2 usec	
τ_4	35-1/2	Restore BMC	2 usec	
τ_5	40	Clear WG	6 usec	
τ_{5a}	40	Restore WG Programmer	2 usec	
τ_{5a}	40	Advance odd WG Programmer	2 usec	} 2^5
τ_6	44	Clear odd WG Programmer	2 usec	
τ_7	48	WG output	6 usec	
		Read WG Programmer	2 usec	
τ_8	48-1/2	Read BMC	2 usec	
τ_9	51-1/2	Restore BMC	2 usec	
τ_{10}	56	Clear WG	6 usec	} 2^4
τ_{10}	56	Restore WG Programmer	2 usec	
τ_{10a}	56	Advance even WG Programmer	2 usec	
τ_{11}	60	Clear even WG Programmer	2 usec	
τ_{12}	64	WG output	6 usec	} 2^4
		Read WG Programmer	2 usec	
τ_{16}	76	Clear odd WG Programmer	2 usec	

Elapsed time in microseconds			Pulse Width
τ_{17}	80	WG output	6 usec
		Read WG Programmer	2 usec
			} 2^3
τ_{21}	92	Clear even WG Programmer	2 usec
τ_{22}	96	WG output	6 usec
		Read WG Programmer	2 usec
			} 2^2
τ_{26}	108	Clear odd WG Programmer	2 usec
τ_{27}	112	WG output	6 usec
		Read WG Programmer	2 usec
			} 2^1
τ_{31}	124	Clear even WG Programmer	2 usec
τ_{32}	128	WG output	6 usec
		Read WG Programmer	2 usec
			} 2^0
τ_{36}	140	Clear odd WG Programmer	2 usec
τ_{37-41}		Unused	
τ_{42}	1920	Read 2^6	2 usec
τ_{43}	3840	Read 2^5	2 usec
τ_{44}	5760	Read 2^4	2 usec
τ_{45}	7680	Read 2^3	2 usec
τ_{46}	9600	Read 2^2	2 usec
τ_{47}	11520	Read 2^1	2 usec
τ_{48}	13440	Read 2^0	2 usec
τ_{49}	13444	Channel advance even	2 usec
τ_{50}	13448	Channel clear even	4 usec
$\tau_{50'}$	13454	Digital Channel Advance	2 usec
$\tau_{50''}$	13458	Digital Channel Reset	2 usec

Elapsed time in
microseconds

Pulse Width

τ_{51} to τ_{97} =

Repeat of τ_2 to τ_{48}

$\tau_{98} = \tau_0$

REFERENCES

1. R. A. Dye, "Magnetic Variable Time Delay Line," Master of Science Thesis, University of California, (1958).
2. R. W. Mathews, et al., "Cyclops Cores Simplify Earth-Satellite Circuits," Electronics, Vol. 31, No. 8, pp. 56-63, (February 28, 1958).
3. G. G. Lendris, "A Discrete Compensator For Sampled-Data Systems Using Magnetic Cores as Storage Elements," Contract AF 18(600)-1521, Electronics Research Laboratory, University of California, AD 264 355, (May, 1961).
4. H. D. Crane and W. K. English, "Signal Switching with Magnetic Elements," Proceedings of the International Conference on Nonlinear Magnetics, Session 10-2 (April 1963).
5. E. K. Van De Riet and C. H. Heckler, Jr., "Research on General Digital Logic Systems Utilizing Magnetic Elements and Wire Only," Final Report, Contract AF 19(604)-5909, AFCRL-TR-60-352, SRI Project 2925, Stanford Research Institute, Menlo Park, California (1960).
6. G. L. Hollander, "Criteria for the Selection of Analog-to-Digital Converters," Proceeding of the National Electronics Conference, Vol. 9, pp. 670-683 (September 1953).
7. E. E. Newhall and J. R. Perucca, "Exploitation of Initial Conditions to Achieve Flux Gain and Nondestructive Readout in Balanced Magnetic Circuits," WESCON paper number 5. 1 (1963).
8. E. M. Gyorgy and J. L. Rogers, "Some Switching Properties of Square Loop Ferrites," Proceedings of the Conference on Magnetism and Magnetic Materials, pp. 637-640 (February 1957).
9. V. W. Hesterman, "Flux Switching Properties of a Partially Set Core," Technical Report 5, Contract Nonr 2712(00), SRI Project 2697, Stanford Research Institute, Menlo Park, California (November 1963).
10. D. Nitzan and V. W. Hesterman, "Flux Switching in Multipath Cores," Report 3, JPL, Contract 950095 under NASw-6, SRI Project 3696, Stanford Research Institute, Menlo Park, California (to be published).
11. F. G. Hewitt and W. M. Overn, "History Effect of Time-Limited Excitation," Journal of Applied Physics, Vol. 34, No. 4 (Part 2), pp. 1117-1118 (April 1963).
12. R. A. Runyan, "A Comparison of Encoding Techniques for Telemetry and Data Handling," 1956 National Telemetering Conference Report, pp. V-3-1 to V-3-4 (August 1956).

13. A. J. Mallinckrodt, "Aliasing Errors in Sampled Data Systems," NATO Advisory Group for Aeronautical Research and Development, Report 316, Contract AF 04(611)-648, AD 294 172 (April 1961).
14. L. W. Gardenhire, "The Use of Digital Data Systems," National Telemetering Conference (May 1963).
15. J. A. Rajchman and H. D. Crane, "Current Steering in Magnetic Circuits," IRE Transactions on Electronic Computers, Vol. EC-6, No. 1, pp. 21-30 (March 1957).
16. H. D. Crane, "A High-Speed Logic System Using Magnetic Elements and Connecting Wire Only," Proceedings of the IRE, Vol. 47, No. 1, pp. 63-73, (January 1959).
17. D. R. Bennion and H. D. Crane, "All-Magnetic Circuit Techniques," Advances in Computers, edited by F. L. Alt, Vol. 4, pp. 54-133.
18. D. J. Morris, "Performance of an All-Magnetic Shift Register," Proceedings of the IEE (London), Vol. 111, No. 2, pp. 291-302 (February 1946).
19. D. R. Bennion, H. D. Crane, and D. C. Engelbart, "A Bibliographical Sketch of All-Magnetic Logic Schemes," IRE Transactions on Electronic Computers, Vol. EC-10, pp. 203-206 (June 1961).
20. R. W. McKay, "Reversible Component of Magnetization," Journal of Applied Physics, Supplement to Vol. 30, No. 4, pp. 56S-57S (April 1959).
21. D. C. Englebart, "High Speed Components for Digital Computers," Quarterly Engineering Report 2, Contract AF 33(616)-5804, SRI Project 2548, Stanford Research Institute, Menlo Park, California (1959).
22. D. R. Bennion and H. D. Crane, "Design and Analysis of MAD Transfer Circuitry," Proceeding of the Western Joint Computer Conference, pp. 21-36, (March 1959).
23. J. A. Baer and C. H. Heckler, Jr., "Research on Reliable and Radiation Insensitive Pulse-Drive Sources for All-Magnetic Logic Systems," Final Report, Contract 950104 under NASw-6, SRI Project 3729, Stanford Research Institute, Menlo Park, California (1962).
24. W. S. Melville, "The Use of Saturable Reactors as Discharge Devices for Pulse Generators," Proceedings of the Institute of Electrical Engineers (London) Part 3, 98, pp. 185-207 (May 1951).
25. J. Goldberg, J. A. Baer, and R. C. Minnick, "Development of Techniques for Improving the Reliability of Digital Systems Through Logical Redundancy," Stanford Research Institute, Final Report Phase III, Contract M-44501 under NASw-6, Project 3196, Stanford Research Institute, Menlo Park, California (1963).
26. M. Karnaugh, "Pulse-Switching Circuits Using Magnetic Cores," Proceedings of the IRE, Vol. 43, No. 5, pp. 570-584, (May 1955).