NASA CONTRACTOR REPORT

NASA CR - 61053

NASA CR - 61053

APOLLO LOGISTICS SUPPORT SYSTEMS MOLAB STUDIES

DIGITAL COMMAND SYSTEM FOR A LUNAR MOBILE LABORATORY

Prepared under Contract No. NAS8-5307 by

J. M. Patten

HAYES INTERNATIONAL CORPORATION
Missile and Space Support Division
Apollo Logistics Support Group

For

NASA - GEORGE C. MARSHALL SPACE FLIGHT CENTER
Huntsville, Alabama

March 31, 1965

DIGITAL COMMAND SYSTEM

By

J. M. Patten

ABSTRACT

A command, by definition, is a unique signal that, when transmitted and received, initiates the operation of prescribed function.

The MOLAB will be commanded to perform a wide variety of prescribed functions throughout its useful life on the moon's surface. The sphere of influence will extend to all major disciplines associated with the vehicle such as power, navigation, mobility, scientific instrumentation, and communication.

This report will concern itself with five discrete phases of command and control; i.e., an analysis of the proposed Gemini/Apollo digital command system, a listing of MOLAB functions that will require commands, a proposed system in point design that will satisfy these command requirements, a discussion of codes and coding technique, and a summary of multi-aperture magnetic core functions.

CR-61053

APOLLO LOGISTICS SUPPORT SYSTEMS MOLAB STUDIES

DIGITAL COMMAND SYSTEM FOR A LUNAR MOBILE LABORATORY

By

J.M. Patten

Prepared under Contract No. NAS 8-5307 by

HAYES INTERNATIONAL CORPORATION
Missile and Space Support Division
Apollo Logistics Support Group

For

ASTRIONICS LABORATORY

NASA-GEORGE C. MARSHALL SPACE FLIGHT CENTER

PREFACE

This report was prepared by Hayes International Corporation, Apollo Logistics Support Group, Huntsville, Alabama, for the George C. Marshall Space Flight Center under the authorization of Task Order H-34, Contract NAS8-5307.

The NASA Technical Liaison Representative was Mr. E. C. Hamilton of the MSFC Advanced Studies Office (R-ASTR-AE).

This work completed a 120 man-day effort beginning on 1 February 1965 and ending on 31 March 1965.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 APOLLO DIGITAL COMMAND SYSTEM

The commands will originate in an assembly called the DCS (Digital Command System), manufactured by Radiation Incorporated. This unit has the ability to store up to 525 words with a length of 40 bits/word. Within this unit encoding will take place, giving the proper sub-bit code for both the vehicle address and the message. Parity checks will be performed for both horizontal and vertical veracity. An additional verification will be performed by receiving the RF transmission, decoding the transmission, and re-inserting the message back into the encoder for bit by bit comparison.

The DCS will transmit a command seven times or until two verifications of an acceptable message are received from the transit vehicle. A built-in delay --- up to three seconds --- is used to accommodate the RF transmission time. These two verification pulses coincide with the acceptance into the input shift register of the vehicle and the acceptance of the core memory of the shift register content.

The length of an individual command can vary from 16 to 40 bits/word. Two intermediate lengths of 25 and 35 bits also are considered "standard" word lengths. The meaning of an individual bit is an arbitrary point with the exception of the first three bits which always constitute the vehicle address. The entire message may be composed of two or more transmissions ; i.e., the message may be of such a length as to require two or more separate transmissions for a complete transfer of information.

Priority is designated by a unique combination of bits which classifies the message type.

The transmission of the sub-bits is performed by combining a one kc subcarrier and a two kc subcarrier which is modulated by the sub-bit train. This combination then is used to modulate a 70 kc subcarrier which in turn phase-shift modulates the transmitting carrier (S-band). The command receiver accepts the pulse train and, after the S-band carrier has been removed, sends the pulse train to a "pre-modulated processor" where discrimination of the 70 kc subcarrier is performed. The audio signal then is processed by a series of modules which acquire sync and sub-bit detection. The message then is routed to a designated storage position and held for operation.

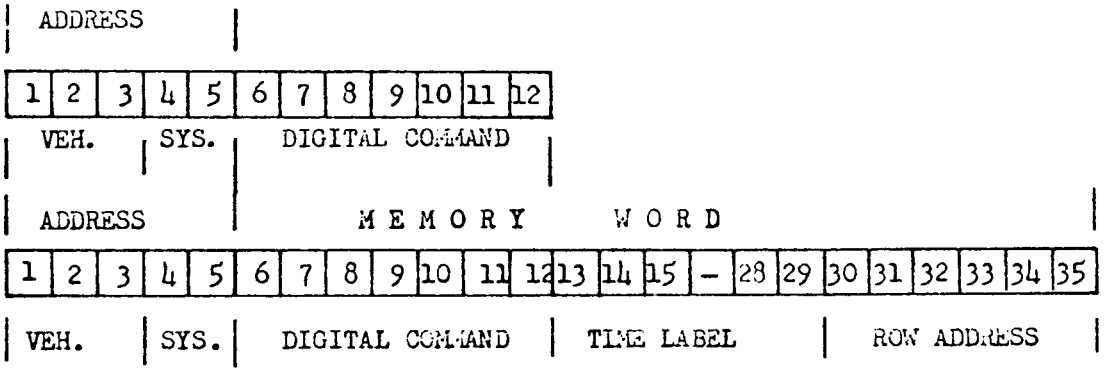
The on-board timing can be updated at will with a minimum error of 1/8 of a second. The write portion of the buffer memory is phased with the read time to prevent the simultaneous action of these two functions.

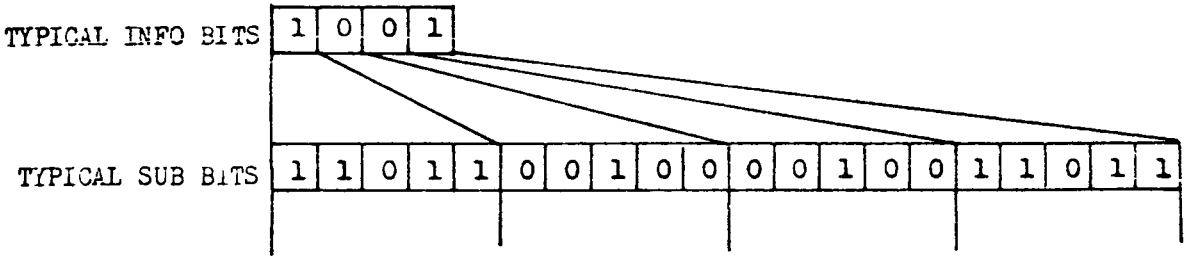
The "memory" referred to is the guidance computer storage which is the recipient of all command messages.

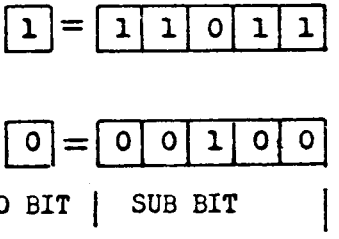
2.0 GROUND STATION ENCODING FOR THE GEMINI COMMAND SYSTEM

Prior to sub-bit encoding at the ground station, the digital command pulse train format is as represented in Figure 1. This format may assume one of two configurations: 1) a real time command (R.T.C.) in which the commanded function essentially is acted upon at the time of transmission, and 2) a stored program command (S.P.C.) in which the commanded function is performed in some finite future time.

The 5 bit address of both formats furnishes a 3 bit vehicle address and a 2 bit system designation for directing the subsequent code groups to a R.T.C. or a S.P.C. performance. The R.T.C. message contains a total of twelve bits --- seven of which are reserved for denoting discrete commands (2^7 or 128 commands). The S.P.C. message format is composed of 35 consecutive bits which are used in the following manner: seven bits for discrete command function totaling 127 messages (provision is made only for 64 commands in the core storage, however), 17 bits are reserved for a time label (2^{17}), and six bits are reserved for core storage address. During the encoding process at the ground station, each of these "information bits" is represented by five sub-bits, which is the form in which they (the information bits) are transmitted.







DIGITAL COMMAND FORMAT

FIGURE 1

3.0 THE GEMINI/APOLLO DIGITAL COMMAND LINK

A comparative study on the Apollo and Gemini command links illustrates a great similarity in basic design and operation. The Gemini configuration is presented herein because of a more extensive format and an exclusive on-board buffer storage which makes it somewhat more applicable to the MOLAB.

The capsule will be receptive to a variety of unique digital commands. These commands share a common format of vehicle address, subsystem designation, and specific instruction. These commands have the additional property of being essentially acted upon in real time or of being stored on the vehicle in a core memory for post reception action. Regardless of the "time of action" function, the digital commands are composed of five sub-bits which constitute a single information bit. The use of sub-bits greatly increases the security of the command system and reduces the possibility of a false command being acted upon.

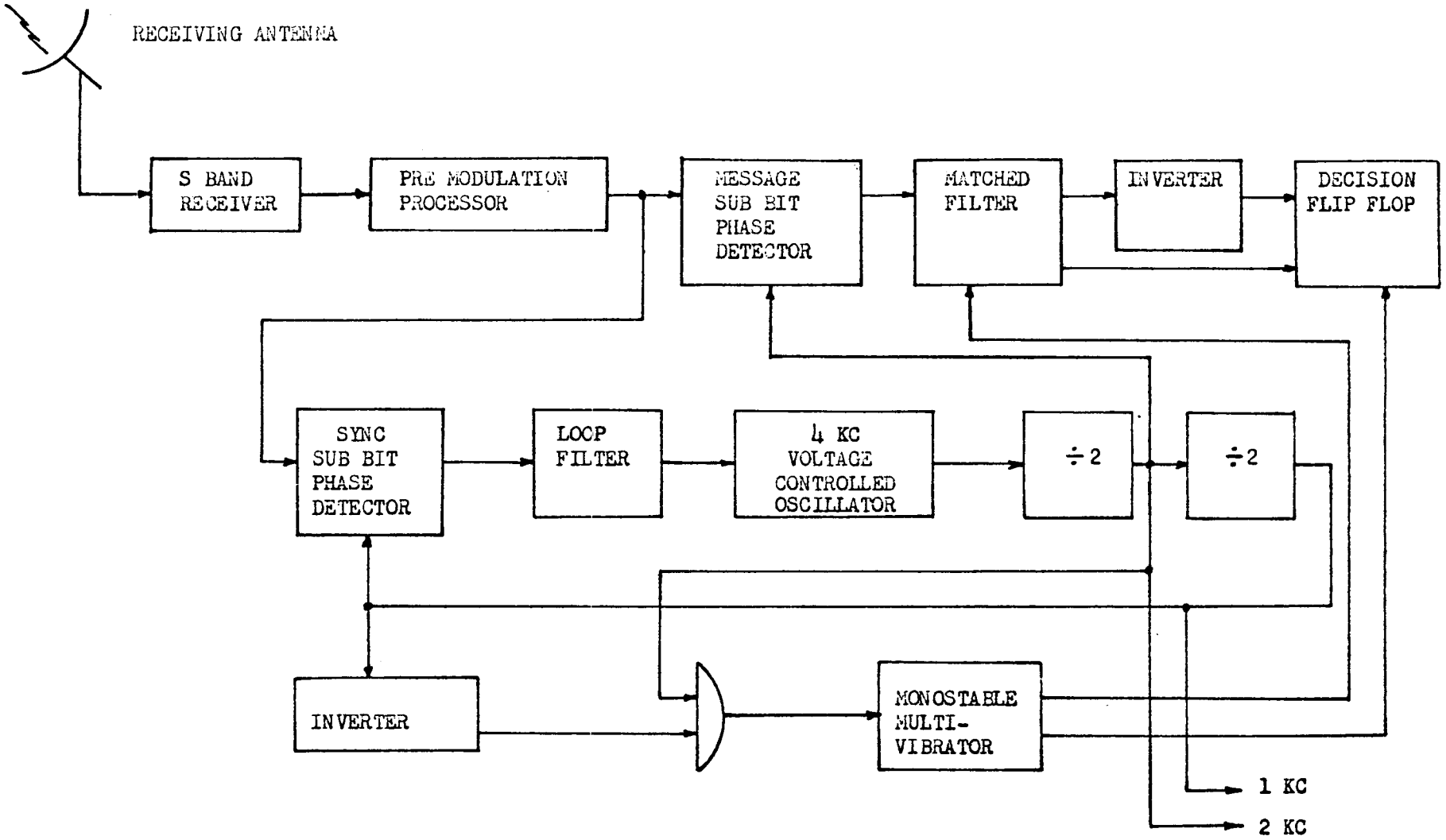
A digital command, which is comprised of serial form sub-bits, is used to phase shift key (PSK) a two kc subcarrier oscillator. The output from this oscillator then is summed linearly with a phase coherent one kc sync subcarrier. This composite signal is used to modulate a 70 kc subcarrier prior to insertion into the S-band phase modulated transmitter. In summary --- PSK/FM/PM.

Phase shift keying is the method used in the encoding of the binary message and results in a binary command having a 0 ± 7.2 degrees phase shift

(ϕ_1) and a binary "zero" having a 180 $\pm$ 7.2 degree phase shift (ϕ_2). The bit repetition rate is one kc (exactly equal to the coherent sync rate) and will give a message information rate of 200 bits/second. (1000/5 = 200)

Upon reception of the phase modulated signal, the S-band carrier is removed and the video signal is fed to the Pre-modulated Processor which contains a 70 kc discriminator. The discriminator's audio output then is divided into two interacting circuits within the sub-bit detector, i.e., the message sub-bit phase detector, and the sync sub-bit phase detector (see Figure 2). The composite signal that contains the two subcarriers, which are orthogonal, is applied to a somewhat conventional phase-lock loop circuit. This loop contains a four kc V.C.O. which is modulated by the phase difference between the incoming sync signal and the local four kc V.C.O. which is modulated by the phase difference between the incoming sync signal and the local four kc ocillator. This generator will experience two divisions resulting in a local one kc signal. The modulation of the four kc V.C.O. is such to reduce the phase difference and, when the phase relationship is at 90 degrees (quadrature), sync lock will occur. (The signal lags the one kc carrier by 90 degrees.) Within the loop, clock pulses are extracted after each frequency division; thus a coherent two kc and a one kc clock pulse is available for additional work within the message sub-bit detector.

The message sub-bit detector uses a product demodulation technique of detection by being multiplied by the coherent two kc clock pulse. The



BLOCK DIAGRAM OF SUB BIT DETECTOR LOGIC FIGURE 2

resultant of this multiplication when integrated over a 1 bit time exhibits a polarity characteristic that is commensurate with the phase (i.e., a "one" or "zero" bit). This output then is applied to a matched filter where the charge induced into a capacitor is sampled or integrated with respect to charge. Since this charge $\left(\frac{4AB}{2}\right)$ is a function of the cos ϕ_1 and ϕ_2 and, by definition, can assume only one of two angles, the product must be either negative or positive. The sampling is performed by shortening the integrating capacitor to ground via a switching transistor.

A matched filter amplifier amplifies and then inverts the signal before passing it on to a decision flip-flop which assumes the polarity of the matched filter output and which makes the train of sub-bits available for entry into the information bit decoder.

Synchronization of the individual stages is maintained by using the common basis of the four kc reference signal. The clock pulse for the matched filter integration is derived by inverting the one kc reference pulse (circuit drawn from the four kc oscillator) and "anding" with the two kc reference pulse. This clock pulse triggers a multivibrator in which the rise time operates the "interrogate and dump" circuitry and the fall time triggers the decision flip-flops. Phase lock also is indicated by generating a one kc reference signal that is in-phase with the incoming pulse train. This in-phase one kc differs from the one kc clock associated with the sub-bit detector in that this clock is 90 degrees out-of-phase. The phase detector output is integrated and fed to a threshold detector to prevent false lock on noise. During the "out-of-lock" condition, the

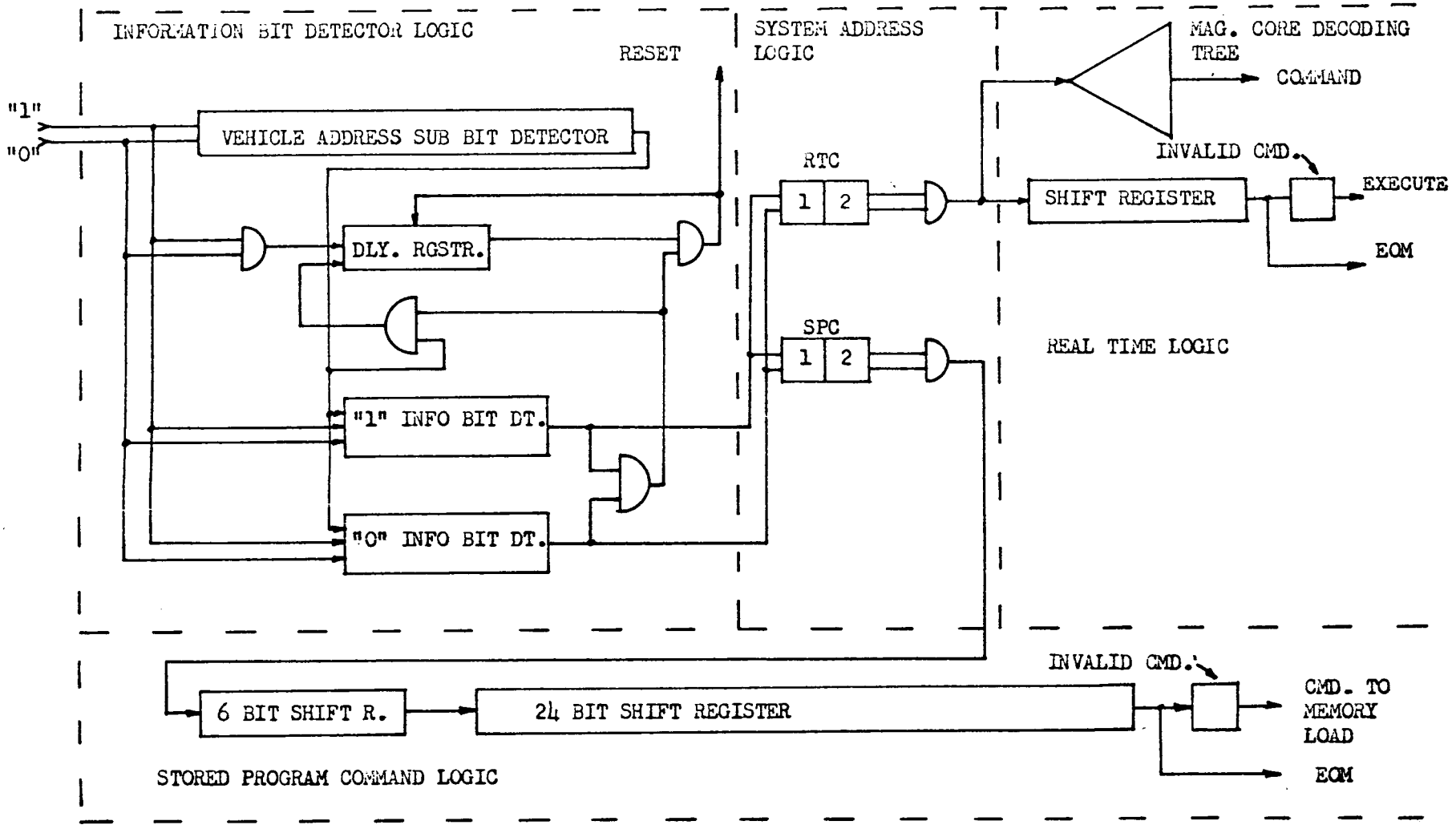
integrated output voltage from the phase detector is zero with an overall time constant for the detector being approximately 100 milliseconds.

3.1 DIGITAL COMMAND ASSEMBLIES

The digital command pulse train (see Figure 1) as received from the sub-bit detector is applied to two information bit-detectors. Both detectors are required, as the coding for the vehicle address differs from the message coding. The vehicle address detector is a solid-state magnetic decoding tree* which will detect the first 15 sub-bits (three information bits) and, if the 15 sub-bits are valid, an output from the decoding tree will enable additional detection to be performed. (See Figure 3.) In the event that the initial vehicle address is not valid (either due to noisy signals or the reception of an alternate vehicle address) no output will occur, thereby preventing an additional decoding process.

With the vehicle address correctly received, the next 10 sub-bits are decoded and are checked for operational mode, i.e., real time command (R. T. C.) or stored program command (S. P. C.). If these two information bits (10 sub-bits) are "zero", an enabling pulse will be sent to the stored command assembly. Conversely, if the two bits are "ones", the real time command assembly will receive the enabling pulse. By

*Magnetic decoding by use of multi-aperture core is discussed in detail in Section 7.0 of this report.



BLOCK DIAGRAM OF INFO BIT LOGIC AND COMMAND INPUTS FIGURE 3

using these two codes (00 and 11), distance protention* is generated within the system, and if a non-valid code is detected, neither assembly will be enabled.

Assuming the enabling of the R. T. C. assembly, the next seven information bits are directed through a magnetic core decoding tree, which chooses the discrete command. A counting of information bits also is performed within this assembly (by shift register) and, after seven valid information bits and one invalid bit (five sub-bits) have been received, an EOM (end of message) pulse is generated. This pulse acts as a R. T. C. execute command for the decoding tree terminus. Information is extracted from the last core by inserting the signal to a diode capacitor integrator. If the EOM signal is not generated after decoding, the capacitor is discharged by a loading resistor.

An alternate condition is the enabling of the S. P. C. assembly which consists of two shift registers in series (6 bit and 24 bit), a magnetic core decoding tree, and the core loading logic. (See Figure 4.) This assembly starts a bit count after the S. P. C. enable has been generated and shifts 24 information bits through the two registers. After the 24th bit has been entered, the memory row decoding tree is enabled. When a total of 32 valid bits have been shifted, the time label and the discrete command are located in the memory input register

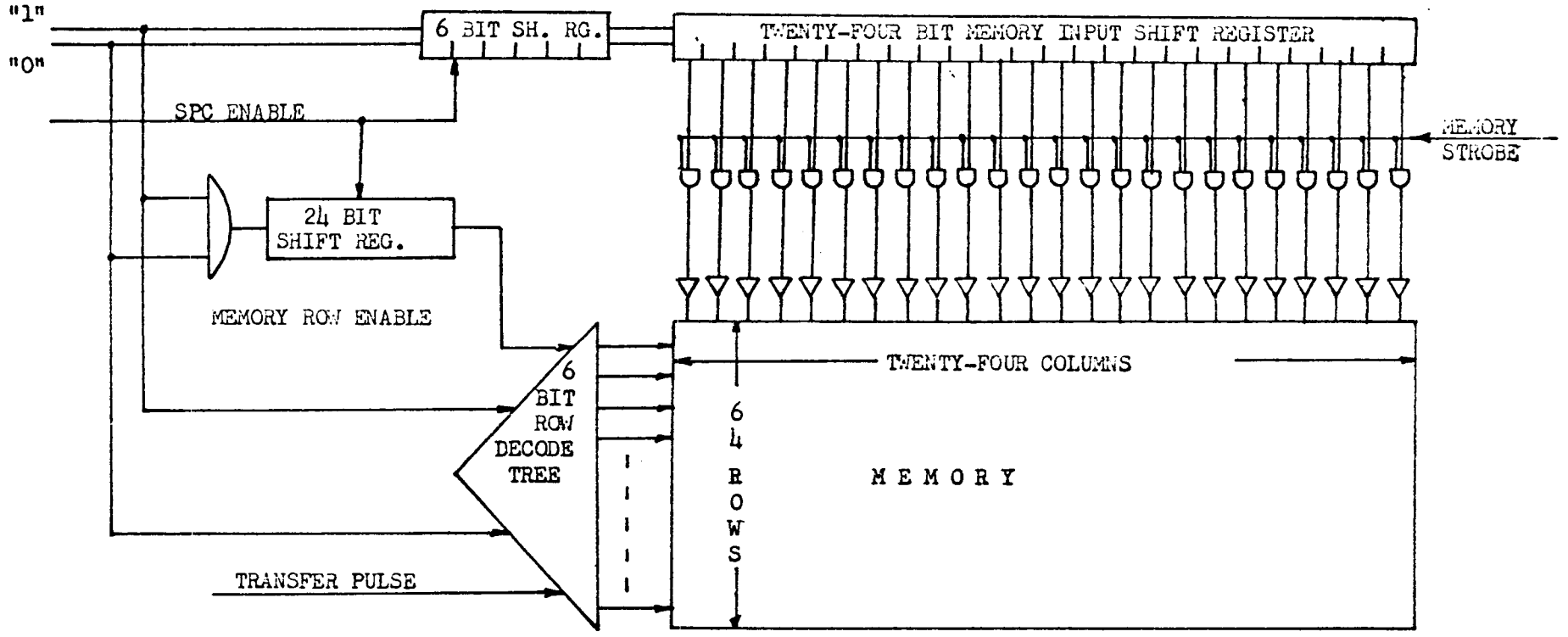
---

*See Section 8.1 for details on distance protected codes.

and the six memory row selection bits have reached the decoding tree terminus. The next five sub-bits, if invalid, will indicate an EOM and initiate a strobe for command and time label entry to the core memory. The core memory, as shown in Figure 4, consists of 24 columns and 64 rows using multi-aperture, non-destruct cores. Each of the 64 rows contains a complete stored command, including the operational message and time label. Entry is made to the memory by firing the column drivers which are associated with a zero bit in the input register. After a three microsecond delay, the row driver is fired. Coincidence of column and row driver currents produce a clear state in the associated core. Without the column drive, as in the case with a "one" in the input register, the core is set by the row driver. (See Figure 5.)

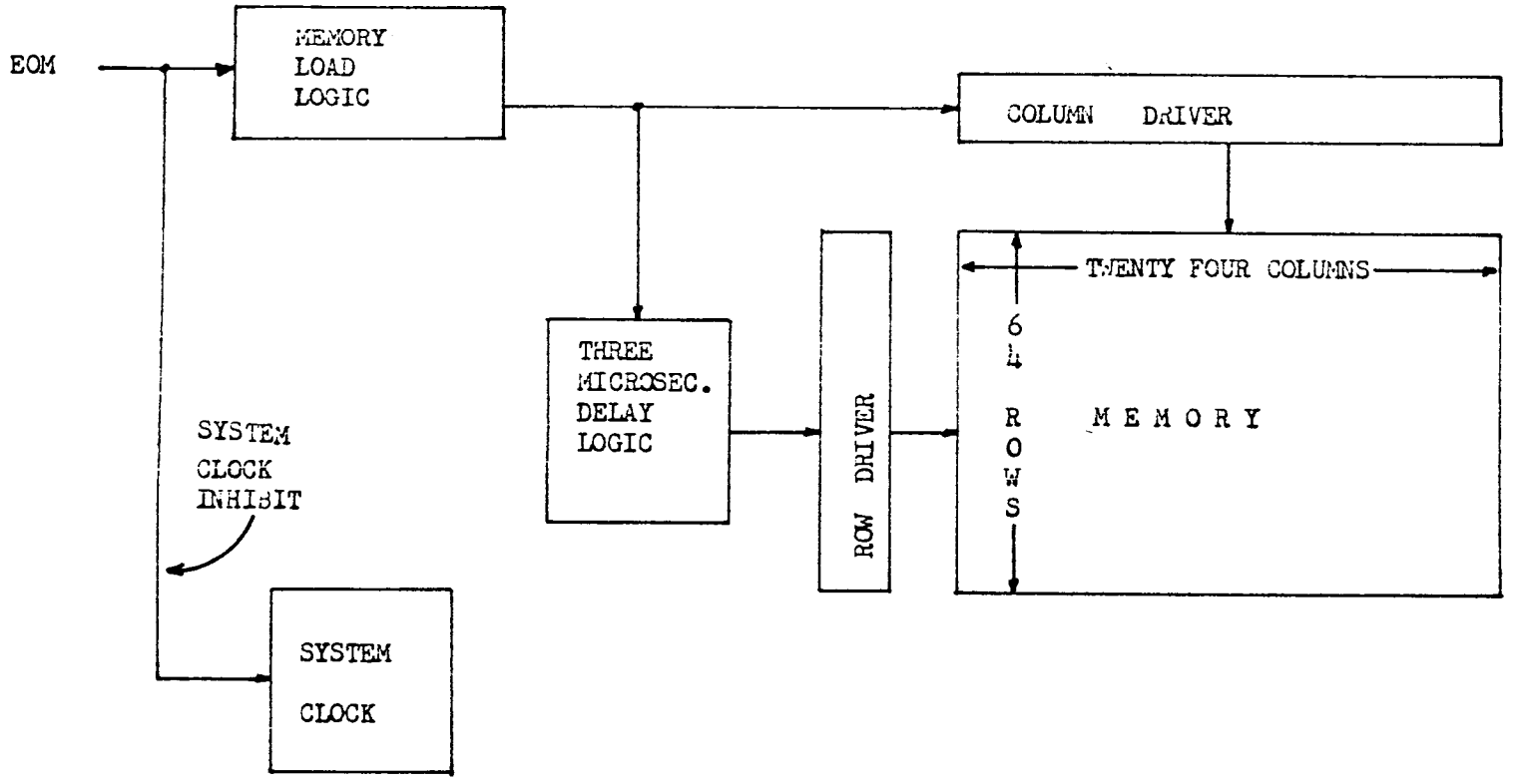
Synchronization for core memory and command execution originates in the vehicle clock which operates at 2^{17} cycles per second. The output of this clock is counted down by a 17 stage flip-flop assembly (see Figure 6) with the final stage operating at one cps. Buffer amplifiers are inserted into the flip-flop circuits for extracting synchronized clock pulses to operate various sections of the memory read circuitry. The time accumulator is a product of the vehicle clock in which the output is used for coincidence checking the stored commands. The accumulator is designed so that the total accumulation will not exceed 131,072 seconds (36 hours, 24 minutes, and 32 seconds).

The memory-read cycle is a continuous operation of sensing the core content, making a time comparison and, if agreement is achieved between

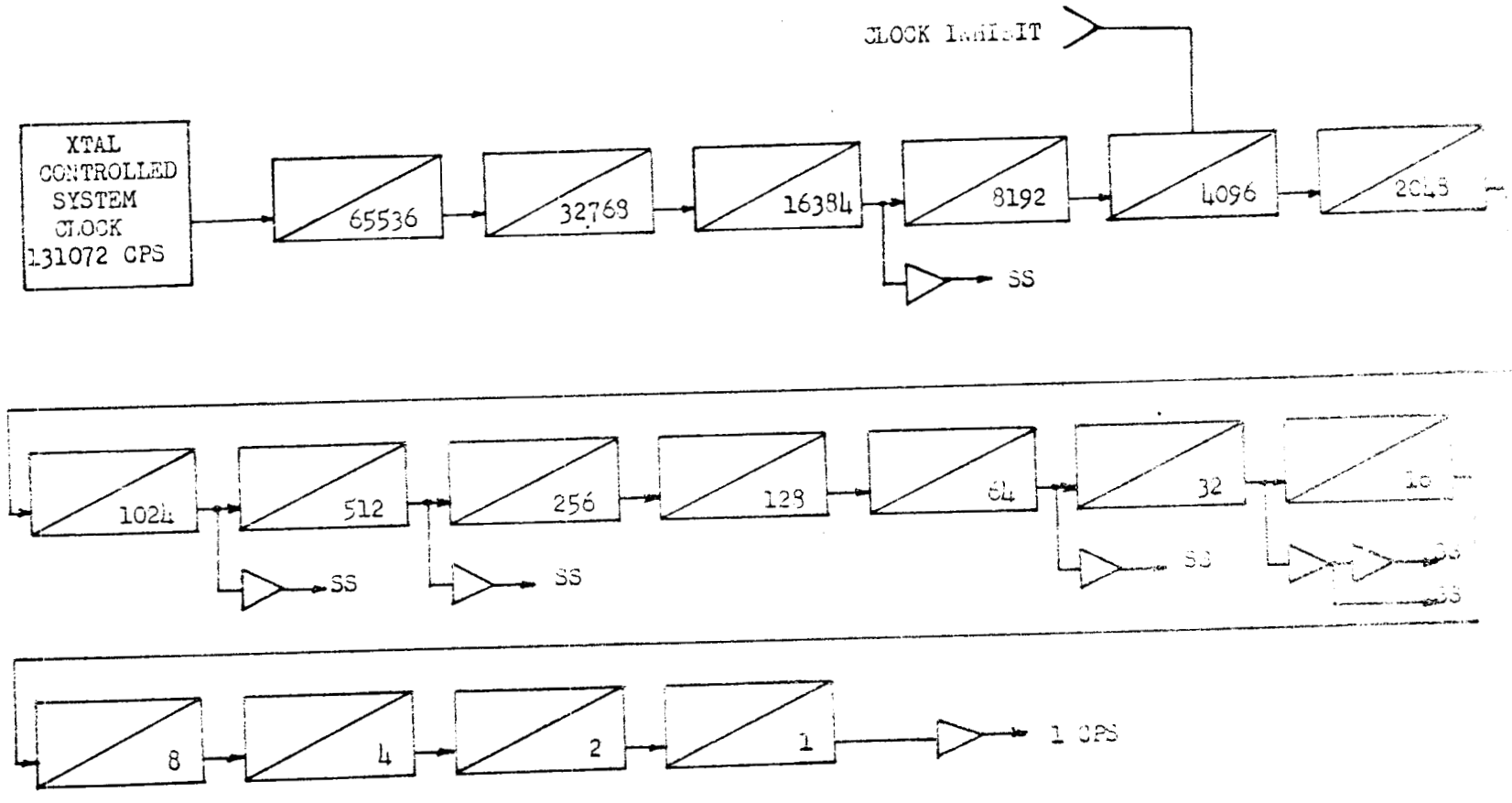


BLOCK DIAGRAM OF MEMORY LOAD LOGIC

FIGURE 4



BLOCK DIAGRAM OF MEMORY LOAD DELAY LOGIC FIGURE 5



NOTE: SS SYSTEM SYNCHRONIZATION

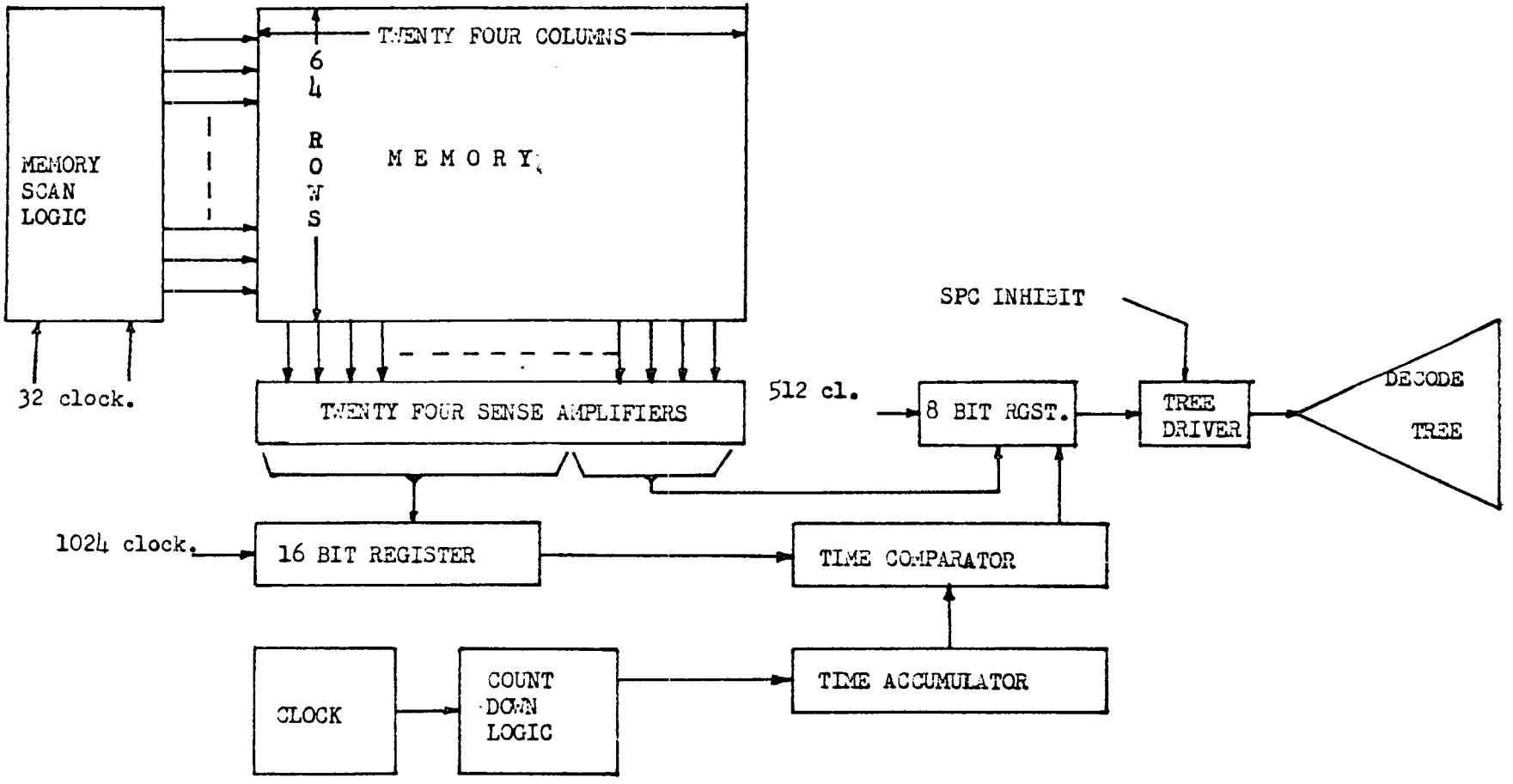
BLOCK DIAGRAM OF SYSTEM CLOCK COUNTDOWN LOGIC

FIGURE 6

memory time and vehicle time, the activation of the command (see Figure 7). The cycle is initiated at row 63 due to its updating process of the time accumulator, and all rows are sequentially scanned in 1/64 of a second for each row. The transfer from the core to two memory output registers is done via 24 sense amplifiers (one per memory row). These registers are sized for 16 bits and eight bits with the former accepting the 16 least significant time label bits and the 8 bit register accepting the seven command bits plus the most significant time label bit. Two outputs from the vehicle clock provides clocking for serially shifting the contents of the output register to two sources: the time comparitor and the stored program decoding tree. A 1024 cps clock is used for the 16 bit output register and a 512 cps clock is used for the 8 bit register.

The time comparitor, which uses basic digital logic, acts as a series coincidence gate with a reset pulse capability if disagreement is noted. If all stored time bits disagree, the time comparitor will generate 17 reset pulses within the 1/64 of a second scan time.

During the time that time-comparison is being conducted, the command message is decoded in a magnetic decoding tree. The output from the last core is integrated and if the time comparitor does not generate a reset pulse, an execute command is generated from the time comparitor and the command function is initiated.



BLOCK DIAGRAM OF MEMORY OUTPUT

FIGURE 7

4.0 COMMAND SYSTEM CONCEPTUAL DESIGN

The conceptual design for the MOLAB digital command system is an outgrowth of the Apollo/Gemini system with many of its characteristics maintained. Changes were introduced, where necessary, to accommodate the larger number of commands associated with the roving vehicle and its scientific gear.

Preparation for this design study was performed by initiating a tentative list of possible MOLAB commands and, by written contact with the cognizant groups, an edited version of the command listing was made which serves as a working paper. This command list is reproduced in Tables I, II, and III. The column titles are self-explanatory with the exception of "Minimum Time Increment", "Duty", and "Priority". The "Minimum Time Increment" refers to the resolution required in time for the actuation of a stored command. It appears from this table that the greatest demand involves a one-second time increment which is compatible with the Apollo/Gemini system. The "Duty" factor relates to single command usage. The "Priority" listing is a notation of those functions which could cause a catastrophic condition if the commands were not acted upon immediately.

From this table a determination was made with respect to the number and type of commands: 356 real time commands (R.T.C.) and 241 stored program commands (S.P.C.). To maintain an operational simplicity, all commands were considered "discrete" even though the resulting action would be proportional. An example of this method is typlified in the

COMMAND LIST FOR MOLAB

TABLE 1

Subsystem	Commanded Parameters	Name or Function	Commands Required	Command Function	R.T.C.	S.P.C.	Minimum Time Increment	Duty	Priority
Locomotion	Speed	Regulator	2	On/degree/off	Yes	No	-	200 or 1/30 sec	Top
	Steering	3-6 Motors	4	Left/right/ctr	Yes	No	-		Top
	Clutch	4-6 Units	2	Engage/disengage	Yes	No	-		Top
	Brakes	4-6 Units	2	On (incremental) off	Yes	No	-		
Power	Fuel cell	Activation 4 units	2	On/off	Yes	Yes	1 min	8/mission	Normal
	Inverters	Activation 5 units	10	On/off	Yes	Yes	1 sec	1/min	Normal
	Converters	Activation 10 units	20	On/off	Yes	Yes	1 sec	1/min	Normal
	Battery Charger	Activation 2 units	4	On/off	Yes	Yes	1 min	1/min	Normal
Video	Zoom Lens	2 Tandem Units	3	Fwd/rev/stop	Yes	No	N.A.	1/min	Normal
	Mono/Stereo	2 Cameras	4	Left only, right only flip/flop, normal	Yes	No		Emergency	Normal
	Electronics	2 Cameras	4	On/off	Yes	No		10/mission	Normal
	Beam Current	2 Cameras	6	Increase/ decrease/stop	Yes	No		1/min	Normal
	Orientation	2 Cameras	10	x, y, stop, fwd, & rev	Yes	No		10/min	Normal
	Frame Rate	2 Tandem Cameras	2	One of two	Yes	No		5/mission	Normal
	Optical Filter	2 Cameras	2	On/off	Yes	No		1/10 min	Normal
Communi-cations	Amplitron	4 Amplitrons	8	On/off	Yes	No	N.A.	30/mission	Normal
	Exciter	2 Exciters	4	On/off	Yes	No		30/mission	
	S.C.O.	5 S.C.O.'s	10	On/off	Yes	No		30/mission	
	Receiver	2 Receivers	4	On/off	Yes	No		Once	
	Antenna	Main Dish Orientation	5	x, y, & stop	Yes	No		30/min	
	Antenna	Directional & Non-directional	2	Switch ckt.	Yes	No		Once	
	Antenna	Initial Erection	1	Single cmd.	Yes	Yes		Once	Normal

TABLE 1 (CONTINUED)

Subsystem	Commanded Parameters	Name or Function	Commands Required	Command Function	R.T.C.	S.P.C.	Minimum Time Increment	Duty	Priority
Activation & Operative Checkout	Steering	3-6 Motors	4	Left/right/center	Yes	No	-	Once	Normal
	Clutch	4-6 Units	2	Engage/disengage	Yes	No	-	Once	Normal
	Brakes	4-6 Units	2	On(incremental) off	Yes	No	-	Once	Normal
Navigation (2)	Heading	Rough alignment	2	Reference system	Yes	No	-	5 min	
	Vertical	Vertical erection	4		Yes	No	-	10 min	
	Heading	Fine alignment	2		Yes	No	-	1 hr	
	Heading	Earth AZ readout (ant.)	2		Yes	No	-	2 hr	
	Heading	AZ readout 0 + CS	2		Yes	No	-	1/2 hr	
	Heading	Torque d.g. in azimuth	2	Reference system	Yes	No	-	1/2 hr	
	Start Coord.	Coordinates in memory	4	Computer	Yes	Yes	1 min	1 hr	
	Present position	Readout from computer	4		Yes	No	-	1 min	
	Distance	Adjust weighing functions	2		Yes	Yes	1 min	4 hr	
	Sightings	R.D. AZ & el. via T.V.	6	Computer	Yes	No	-	1 min	
Scientific Instruments	Deployment	17 Experiments EEIC	17	Initial deployment	Yes	Yes	1 min	1/day	Normal
	Activation	26 Experiments	52	On/off	Yes	Yes	1 min	1/day	Normal
	Readout	26 Experiments	26	Write cmd.	Yes	Yes	1 min	1/day	Normal
Checkout System	Computer	Write	1	Operation	Yes	No	-	1/day	Normal
		Read	1	Operation	Yes	Yes	1 min	1/day	Normal
		Execute	1	Operation	Yes	Yes	1 min	1/day	Normal
		Stop	1	Operation	Yes	No	-	1/day	Normal
Activation, Checkout, & Unloading	Tiedown Explosive Bolts	0-10 Bolts	1	Activate	Yes	No	-	Once	Normal
	Slow Rotation Motor	1 Motor	4	On/off	Yes	No	-	1/5 sec	Normal

TABLE 1 (CONTINUED)

Subsystem	Commanded Parameters	Name or Function	Commands Required	Command Function	R.T.C.	S.P.C.	Minimum Time Increment	Duty	Priority
	Ramp Extension	2 Motors	3	On/off	Yes	No	-	Once	Normal
	Axel Support Bolts Blown	4-6 Bolts	1	Activate	Yes	No	-	Once	Normal
	Wincheo Off.	2 Motors	4	On/off	Yes	No	-	1/5 sec	Normal
Telemetry	Normal System	Prime telemetry	2	On/off	Yes	Yes	1 min	4/day	Normal
	Critical System	Secondary telemetry	2	On/off	Yes	No	-	Emergency	Normal
	Tape Recorder	Write function	2	On/off	Yes	Yes	1 min	4/day	Normal
	Tape Recorder	Read function	2	On/off	Yes	Yes	1 min	4/day	Normal
Navigation (System #1)	Star Tracker	Navigational stars	57	Select coordinates from core memory	Yes	Yes	1 sec	6/hr	Normal
		Earth/sun	2	Select coordinates from core memory	Yes	Yes	1 sec	6/hr	Normal
		Course/fine	2	Adjustment	Yes	Yes	1 sec	6/hr	Normal
		Activation	2	On/off	Yes	No		6/hr	Normal
	Inertial Platform	Activation	2	On/off	Yes	Yes	10 sec	Emergency	Normal
		Quick erect	1	Operation	Yes	Yes	10 sec	Once	Normal
		Gyro activate	1	Operation	Yes	Yes	10 sec	Once	Normal
		Gyro htr. override	2	On/off	Yes	No	-	Emergency	Normal
	Normal/ Critical	Activation	2	On/off Off/on	Yes	No		1 sec	Normal
		Roll	1	Operation	Yes	No		1 sec	Normal
		Pitch	1	Operation	Yes	No		1 sec	Normal
		Yaw	1	Operation	Yes	No		1 sec	Normal
		Latitude	1	Operation	Yes	No		1 sec	Normal
		Longitude	1	Operation	Yes	No		1 sec	Normal
		Vertical	1	Operation	Yes	No		1 sec	Normal
	Computer	Navigational program	1	Operation	Yes	No	1 sec	10/hr	Normal
		Selected input	1	Navigation	Yes	No		10/hr	Normal

TABLE 1 (CONTINUED)

Subsystem	Commanded Parameters	Name or Function	Commands Required	Command Function	R.T.C.	S.P.C.	Minimum Time Increment	Duty	Priority
Environmental Control	Valves	Activation	20	On/off	Yes	Yes	1 sec	8/mission	Normal
	Temperature Cycle	Activation	10	On/off	Yes	Yes	1 sec	8/mission	Normal
	On/off Functions	Activation	6	On/off	Yes	Yes	1 sec	8/mission	Normal

TABLE 2 - ANTICIPATED COMMANDS

The following table lists the anticipated commands with notations of the manner of operation:

LOCOMOTION	R.T.C.	S.P.C.
Speed	2	--
Steering	4	--
Clutch	2	--
Brakes	2	--
	10	
POWER		
Fuel Cells	2	2
Inverters	10	10
Converters	20	20
Battery Charger	4	4
	36	36
VIDEO		
Zoom Lens	3	--
Mono/Stereo	4	--
Electronics	4	--
Beam Current	6	--
Orientation	10	--
Frame Rate	2	--
Optical Filter	2	--
	31	
ACTIVATION AND OPERATIVE CHECKOUT		
Steering	4	--
Clutch	2	--
Brakes	2	--
	8	

TABLE 2 (CONTINUED)

NAVIGATION (SYSTEM NUMBER TWO)	R.T.C.	S.P.C.
Heading	2	--
Vertical	4	--
Heading	2	--
Heading	2	--
Heading	2	--
Heading	2	--
Start Coordinates	4	4
Present Position	4	--
Distance	2	2
Sightings	6	--
	30	6
TELEMETRY		
Normal System	2	2
Critical System	2	--
Tape W. (Write)	2	2
Tape R. (Read)	2	2
	8	6
COMMUNICATIONS		
Amplitron	8	--
Exciter	4	--
S.C.O.	10	--
Voice Receiver	4	--
Antenna (Main Dish)	5	--
Antenna Direct/Non-Direct	2	--
Antenna Initial Erection	1	1
	34	1

TABLE 2 (CONTINUED)

SCIENTIFIC INSTRUMENTS	R.T.C.	S.P.C.
Deployment	17	17
Activation	52	52
Readout	26	26
	95	95
CHECKOUT SYSTEM		
Write (Computer Input)	1	1
Read (Computer Input)	1	1
Execute (Computer Input)	1	1
Stop (Computer Input)	1	1
	4	2
ACTIVATION, CHECKOUT, AND UNLOADING		
Tiedown Explosive Bolts	1	--
Slow Rotation Motor	4	--
Ramp Extension	3	--
Axle Support Explosive Bolts	1	--
Winched Off	4	--
	13	
NAVIGATION (SYSTEM NUMBER ONE)		
Navigation Stars	57	57
Earth/Sun	2	2
Course/Fine	2	2
Activation	2	2
Activation	2	2
Quick Erect	1	1
Gyro Activate	1	1
Gyro Htr. Override	2	--

TABLE 2 (CONTINUED)

NAVIGATION (SYSTEM NUMBER ONE) (CONT'D)	R.T.C.	S.P.C.
Activation	2	--
Roll	1	--
Pitch	1	--
Yaw	1	--
Latitude	1	--
Longitude	1	--
Vertical	1	--
	77	67
COMPUTER (NAVIGATIONAL)		
Navigational Program	1	--
Selected Input	1	--
	2	
ENVIRONMENTAL CONTROL		
Valves	20	20
Temperature Cycle	10	10
On/Off Functions	6	6
	36	36

TABLE 3 - TENTATIVE COMMANDS FOR MOLAB

The following is a compilation of the tentative commands for the MOLAB:

Subsystem	R.T.C.	S.P.C.
Power	36	36
Video	31	--
Communications	34	1
Locomotion	10	--
Telemetry	8	6
Environmental	36	36
Scientific Experiments	95	95
Checkout System	4	2
Navigation*	77	65
Computer (Navigational)	2	--
Activation Checkout and Unloading	13	--
Activation and Operative Checkout	8	--
	356	241

*This navigation system contains the greater number of commands and is used as the "worst case" condition for sizing.

zoom lens requirement for television. A single command for forward action is transmitted which would engage a reversable motor to drive the zoom lens mounting in a forward direction. Once initiated, this action would continue until a "stop" command was received or the lens mounting had been extended to the limit of its travel. To retract the lens, a "reverse" command would be transmitted and the complementary action would result. Variations of this discrete proportional commanding system can be extended to the motive subsystems for controlling the vehicle.

By definition, a real time command is one which creates action, essentially at the time of reception. The only delay encountered results from the transmission and decoding time (about 1.33 seconds). A stored program command, by definition, is a command which when received is stored with a "time of action label" in an on-board core memory. These stored commands are examined once a second for time coincidence with an internal (vehicle) clock and, if a match occurs, the command is performed.

The command link from earth to the vehicle will be operational during the following modes:

1. Unloading and Checkout - Tiedown bolts, ramp extension, complete vehicle checkout, scientific instrument deployment, television, vehicle locomotion, etc.

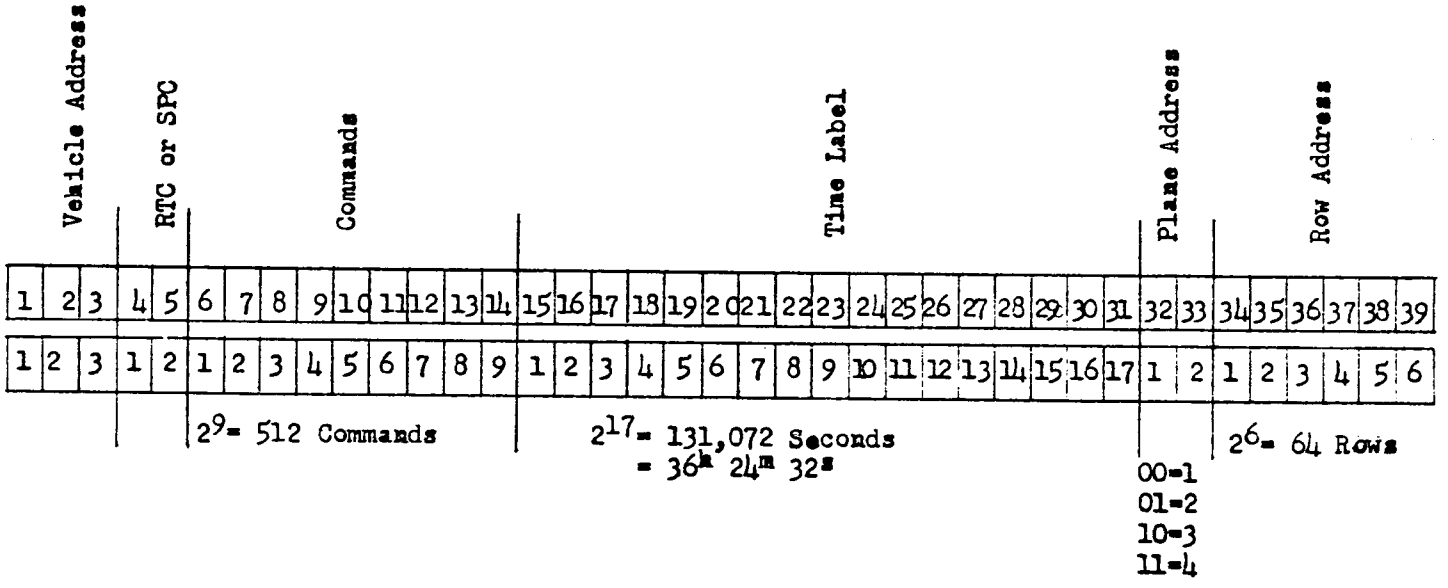
2. Dormant - Scientific experimental control, vehicle checkout, housekeeping, etc.

3. Unmanned Roving - Television, vehicle locomotion, navigation, etc.

The noted commands are representative and are listed only to indicate a general type of command.

The command pulse train will originate in a DCS. (digital control system) unit located on earth. This highly flexible unit allows up to 37 bits to be used in a discretionary manner and each bit of information will undergo encoding into a 5 sub-bit code which then is transmitted at 1000 bits per second. Within the MOLAB vehicle a sub-bit detector reconstitutes the pulse train to its original form (see Figure 8). A R.T.C. consists of 14 info bits with the first 3 bits allotted to vehicle address, the next 2 bits allotted to subsystem designation, and the following by 9 bits allotted to the discrete commands. A digital command system intrinsically doubles the number of integers with each additional bit. This inherent characteristic inevitably causes an over-design in the system as the quantity of exact numbers is limited. This is reflected in the choice of 2^9 bits for the command portion of the pulse train. The decimal equivalent of 2^9 is 512 and, with 356 R.T.C. anticipated 156 "spare" command possibilities remain available for expansion.

The maximum rate at which a real time command may be transmitted is 200/14 or approximately 14 commands per second. This number is indicative only of a maximum rate and does not include retransmission of the command for verification. (Note: This point is discussed in Section 5.0.) The R.T.C. capability will be exploited to its fullest extent during the



64X4 = 256 Words

26 Columns X 256 Rows = 6656

Memory Bits

Length of RTC = 14 Bits
Length of SPC = 39 Bits

Maximum Number of RTC = 512
Maximum Number of SPC = 256

Total Number of Sub-bits/Command
RTC = 70
SPC = 195

Format for MOLAB Digital Command System

Figure 8

unmanned roving modes (unloading from the transport vehicle and rendezvous with the arriving astronauts). During this period, the locomotion television and navigation predominate. During the dormant phase, the R.T.C. functions primarily will be directed to scientific and housekeeping systems. It also is anticipated that complete system checkouts will be performed on a periodic basis during this time.

A stored program command requires 39 bits for complete encoding. The first 14 bits perform the same function as an R.T.C. format, followed by 17 bits which act as a time label for the command. The following two bits (numbers 32 and 33 in the pulse train) are used for core memory plane address, and the six remaining bits function as a memory row address. The storage capacity of the memory is 256 words or 6656 bits, which exceeds the anticipated stored commands by 15. The maximum number of stored commands transmitted would be 200/39, or approximately five per second.

The time label of 17 bits when equated to seconds will provide 36 hours, 24 minutes, 32 seconds of time delay for a command instigation. A brief analysis was made (see Appendix) for the minimum time available at Goldstone, California, in which commands could be transmitted within any one 24-hour period. This study indicates a minimum 9.2 hour "see time" which in turn would require a storage capacity of 14.8 hours on the MOLAB. In the interest of safety, an additional bit was included in the time label to accommodate an unforseen contingency.

Currently, the DCS unit is programmed to transmit a command seven times in succession or until an "accept" pulse is received from the vehicle.

In addition to numerous parity checks, an independent receiver/decoder/bit-comparitor is used at the ground station to add confidence in the transmitted code. An analysis was made of the statistical possibilities of an erroneous code being received and acted upon. A 10^{-9} probability using a standard 150 sub-bit code was indicated.

Primarily, the changes in the Apollo/Gemini equipment will occur in the receiving modules. Some of the major changes are presented below and are based primarily on the 35 bit Gemini format (Figure 1). Additional modification with respect to packaging and electronic logic undoubtly will be required.

1. Vehicle Address - Bits 1-3

   No change anticipated

2. R.T.C. and S.P.C. Subsystem Designation - Bits 4-5

   No change anticipated

3. Command - Bits 6-14

   An increase of 2 bits is required to accommodate the added number of commands

4. Time Label - Bits 12-31

   No change anticipated

5. Plane Address - Bits 32-33

   An additional address command is required to designate the particular memory plane to be used

6. Row Address - Bits 34-39

   No changes anticipated

The overall change has been minor and the 4 bit increase over the Gemini format is within the capabilities of the operational DCS unit manufactured by Radiation, Inc. Changes will be required within the decoding system and are listed below in the order of appearance within the assemblies:

1. The length of the R. T. C. shift register will be expanded to accommodate two additional bits with the EOM coming after the ninth command bit (the fourteenth bit with the pulse train).

2. The R. T. C decoding tree will be expanded by two additional branches to accommodate the additional code possibilities.

3. The R. T. C. relay logic also will be expanded to accommodate the additional command functions.

4. The two input shift registers for S. P. C. will be expanded to an eight and twenty-six bit capacity.

5. The input delay register for S. P. C. will be expanded to twenty-six bits.

6. Additional logic will be necessary to decode the plane address.

7. The core memory will be expanded to 26 columns @ 64 rows with four core planes in operation.

8. An addition to the memory write logic will be necessary in order to operate in all four planes.

9. Additional read sense amplifiers will be needed to accommodate the additional memory capacity.

10. The memory scan logic will be increased to sequentially scan all memory planes.

11. The input clock pulse to the memory scan logic will be two synchronized 128 p.p.s.

12. The output shift registers will be of a sixteen, an eight, and a two bit capacity. The clocking for these registers will be 4096, 2048, and 512 p.p.s. respectively.

13. The S.P.C. decoding tree for commands will be expanded by two branches.

14. The system countdown clock logic will be altered to provide the following clock rates: 128, 512, 2048, and 4096 pulses/second.

4.1 DESIGN PARAMETERS

4.1.1 PRIORITY

The use of priority indication in the format was not attempted in this study because of the detailed information required from each subsystem to logically determine its rank. However, a simple one bit priority indication could be inserted in the R.T.C. format with little additional complexity. This bit, probably adjacent to the vehicle address bit, would flag the system to receive an emergency message.

4.1.2 VERIFICATION

Several methods may be used for message verification which employ the telemetry link to report back to earth on the code validity. Transponding the entire message for bit by bit comparison is an approach which is very time consuming over the lunar distance, and although it is the safest method, would require almost four seconds per command --- an intolerable delay for many functions. Transmitting an "acceptance" pulse denoting the reception (and action upon) of a valid code group will give a degree of assurance, but in many situations the normal telemetry channels will give similar information. It should be noted that during the dormant and some unloading phases the time is not critical and the luxury of command verification may be feasible.

The mobility subsystem generally requires that minimum time be spent in commanding the vehicle, which precludes an elaborate verification

system. A possible scheme to assure greater decoder acceptance is the use of a "majority match" system in which at least the majority of the sub-bits must be correct to denote an information bit. This method, while allowing a greater number of commands to "get through", also would increase the probability of an erroneous action. As noted earlier in this report, the probability of an erroneous command is about 10^{9} probability. The odds are that about one out of a hundred "correct" commands will not be accepted by the decoder.

4.1.3 DISTANCE PROTECTED CODING

The assignment of a unique command to a unique function should be performed using distance protected techniques rather than an arbitrary designation. This technique provides for code separation of commands that control irreversible or critical functions. A case-in-point would be a "left" or "right" turning command associated with the mobility subsystem. In this example the left and right commands should be mutually different by several binary numbers. This added protection is most desirable when time does not permit verification.

4.1.4 SIGNAL LOSS AND ATTITUDE SENSING

To further protect the roving vehicle from an unsafe attitude, it is recommended that an output from limiting pitch and roll sensors will be logically "ored" to the stop and brake set mobility functions. Under this regimen the vehicle can act independently without the inherent transmission time delay. It also is advocated that this same "or" gate be

coupled to a command receiver signal sensor that would detect a loss of command link. Implementation of this signal would be with the idling pulses originating in the DCS unit or through a carrier AGC.

4.2 COMMAND PHILOSOPHY

The design as outlined in these pages does not use the toggle method for commanding a function, i.e., a single command that reverses the status such as on/off, up/down, left/right, etc. Although this method would reduce the total number of commands required, the hazard of an incorrect command is increased. This method must rely on telemetry to reflect the current condition and in some applications would require an interlock to the DCS for reliable operation.

5.0 COMMAND PHILOSOPHY CONCEPTUAL DESIGN SUMMARY

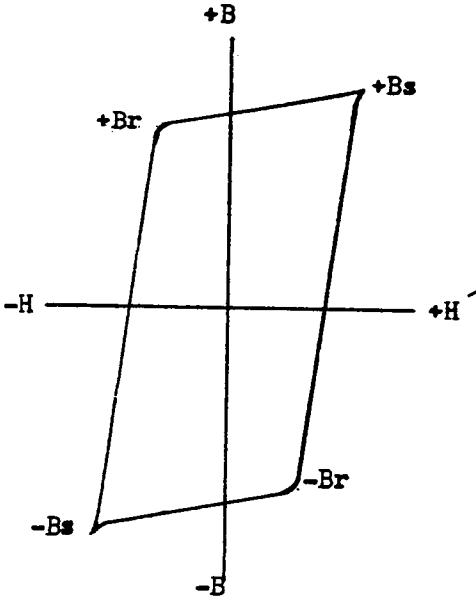
Many approaches could be made in the command and control design, but logic dictates that the first appraisal be of the Apollo oriented system. Since many of the MOLAB functions are different and are performed in a mission unlike either Gemini or Apollo, it is reasonable to assume that some changes in the basic design will be necessary. However, with the exception of some locomotion requirements, (see Table One) all other functions can be accommodated by this same MOLAB system. It is possible that the requirement of 30 commands/second necessary for guiding the MOLAB could be reduced and still be in line with other subsystems.

The preliminary design as presented was to establish the upper limits for the system based on current knowledge. Admittedly, the design assumes a worst case condition in respect to stored command capacity, but history shows that subsystem complexity tends to grow rather than decrease and the added design margin is thought to be justified.

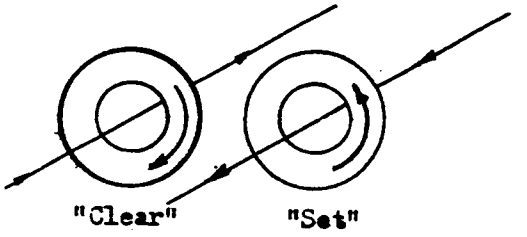
6.0 MULTI-APERTURE MAGNETIC CORES

The flux path direction within a magnetic core is a function of the current direction used to magnetize that core. This magnetic flux will be retained within that core after the removal of the current if the initial current was of sufficient magnitude. This succinct description can be shown graphically by noting the hysteretic loop generated by a core. (See Figure 9, Sketch 1.) Two distinct states of a core are shown, i.e., a "clear" state corresponding to $-B_r$-B_s and a "set" state corresponding to $+B_r$ $+B_s$. B_s is the maximum flux intensity reached during the time of action magnetization, and B_r is a numerical or remanent flux intensity reached after the magnetizing current has been removed. For convenience, the direction of the magnetizing current and the direction of the flux paths within the cores are as shown in Figure 9, Sketch 2. Clockwise rotation of the flux is considered as a clear or zero core state and counterclockwise rotation is an indication of a set state. (Binary one.)

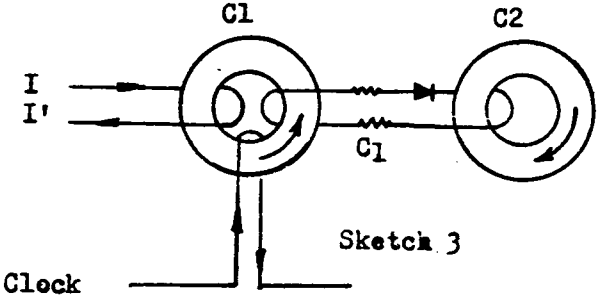
The ability of a core to transfer its state to an adjacent core upon command forms a basic tool in the magnetic core decoding technique. An illustration of core sense transfer is given in Figure 9, Sketch 3. With the two cores in a clear state a current is passed through input I and I' in a direction to set core C_1. The coupling loop (CL) between C_1 and C_2 contains a blocking diode oriented to prevent C_2 from also being set at this time. An additional conductor through core C_1 (clock) is then pulsed in a direction that returns C_1 to a clear state. During this flux change from a set to a clear state a current is induced in the coupling loop between C_1 and C_2. The magnitude and direction are such to set C_2. This



Sketch 1



Sketch 2



Sketch 3

Basic Magnetic Core Configuration

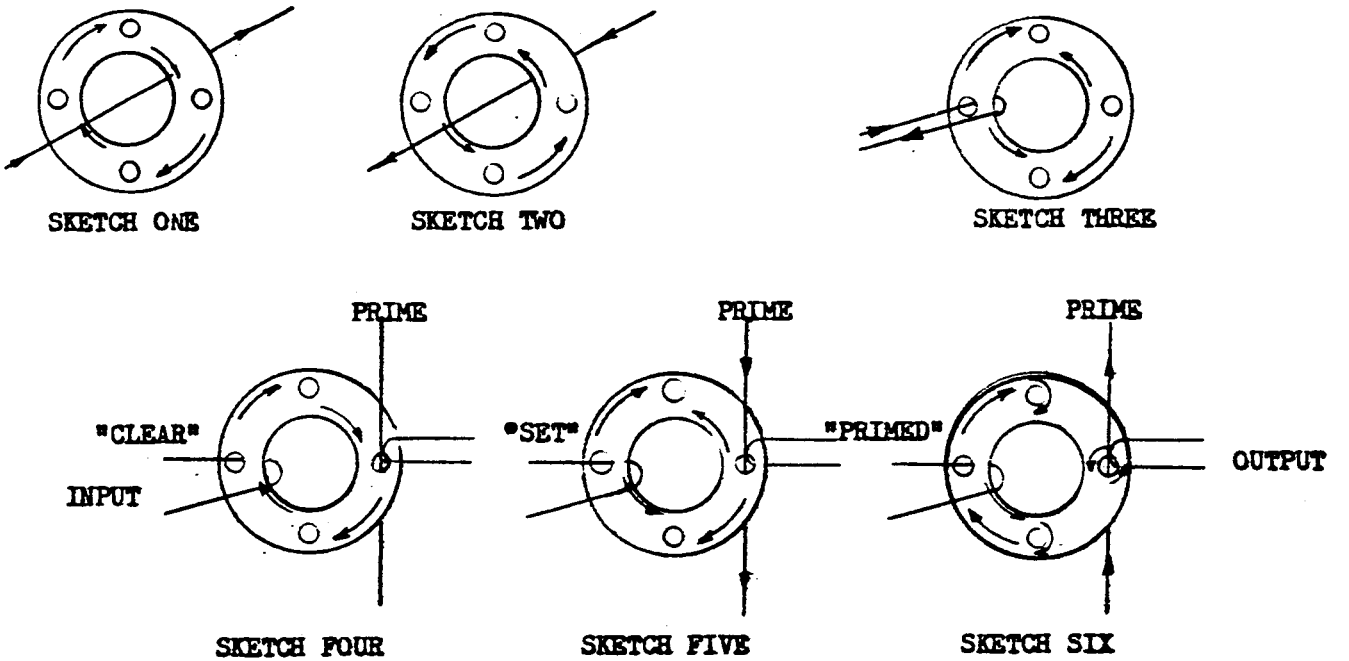
Figure 9

process of first setting a core followed by a clear pulse to induce a set condition in a coupled core can be continued through "n" cores. The number of clock pulses necessary for transfer is $C_p = C^{n-1}$, where C_p equals the number of clock pulses and C^n equals the number of cores in series. Additional circuitry is necessary, however, to limit the magnitude of induced current and to prevent current coupling in the reversed direction.

The use of multi-aperture devices or MAD (multi-aperture device) cores permit a somewhat easier approach. The construction is similar to the standard core with the exception that additional small openings or apertures have been placed through the core rim. (See Figure 10, Sketch 1.)

This configuration exhibits unique properties when the major apertures are used in conjunction. If a current carrying wire is threaded only through the major aperture, the characteristics are identical to a conventional core (Figure 10, Sketches 1 and 2); however if a conductor is passed through the major and one minor aperture with the current oriented to "set" the core ("set pulse"), only half of the flux within the core will be affected (See Figure 10, Sketch 3). This will occur because the current coupling will only exist under the inner portion or "leg" of the core. The resulting configuration shows the outer leg in a "clear" state and the inner leg in a "set" state of the same core.

When an additional conductor called a "prime" is passed through one minor aperture and is energized, the following conditions exist. (See Figure 10, Sketches 4, 5, and 6.)



BASIC CONFIGURATION OF MULTI-APERTURE CORES

FIGURE 10

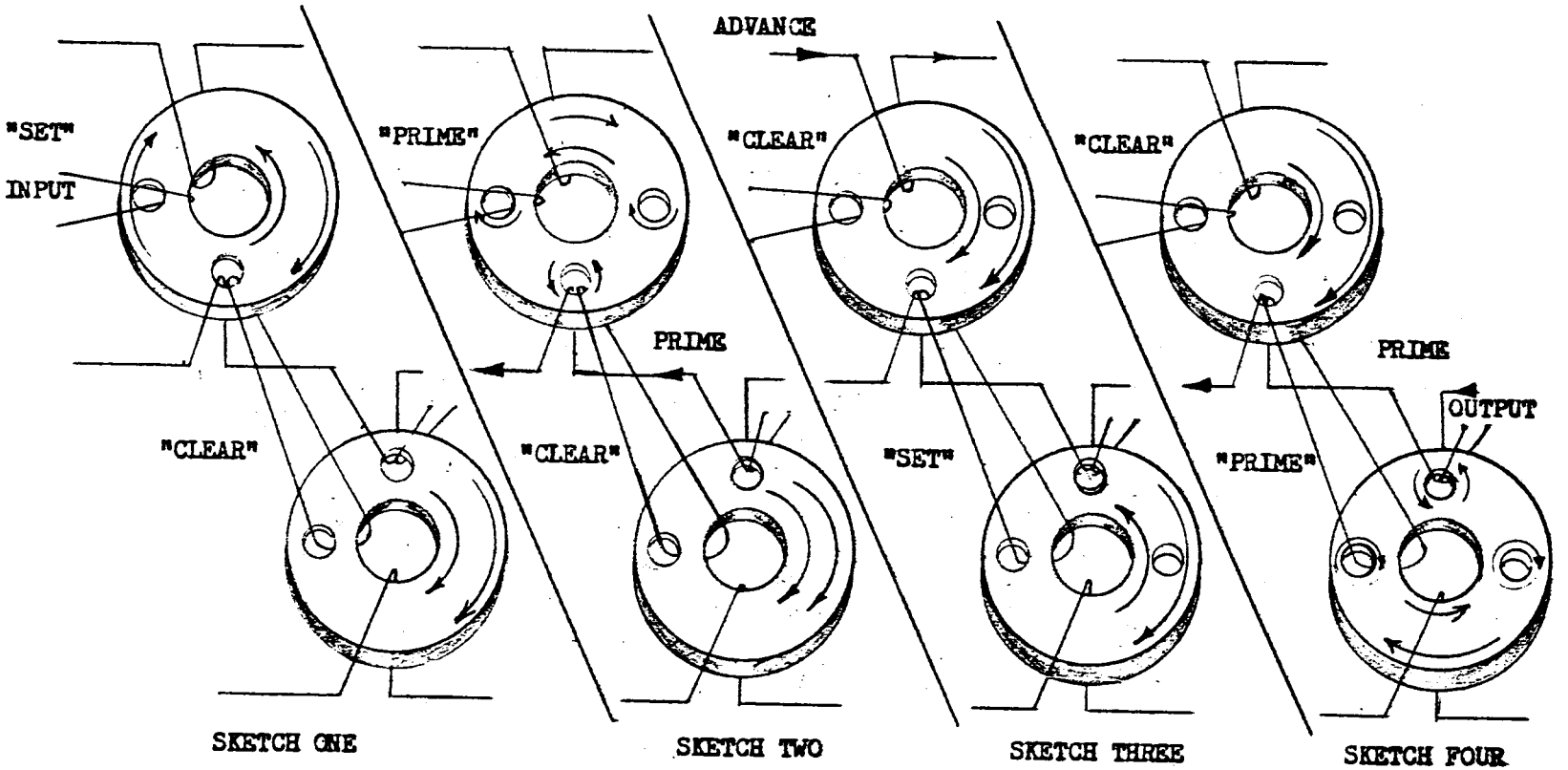
1. In a cleared core with the current oriented downward, there will be no change in the flux pattern. When this current is less than a predetermined magnetude and is directed upward, a flux change will not occur because of the core's geometry. (See Figure 10, Sketch 4.)

2. In a set core, if the current direction is downward, no flux reversal will occur because the coupling exists under the outer leg. (See Figure 10, Sketch 5.)

3. In a set core, if the current direction is upward, a flux switch from the inner to the outer leg will occur around that minor aperture. In effect, a decoupled core has been created within the core body (Figure 10, Sketch 6). This low amplitude current is known as the priming pulse.

To return a set core to a clear state, an additional conductor threaded through the major aperture is required. The nomenclature is either "advance" or "clear" for the current pulse on this conductor.

When it is desired to transfer a state from one core to a subsequent core, three major pulses are required: set, prime, and advance. This sequence is illustrated in Figure 11, in which the first core was considered in a set state (Figure 11, Sketch 1). In Sketch 2, a prime pulse to core one has reoriented the flux pattern around the lower minor aperture. This flux change in core one was too small for the induced current in the coupling loop to set core 2, which remains in a clear state. An advance pulse through the major aperture of core 1

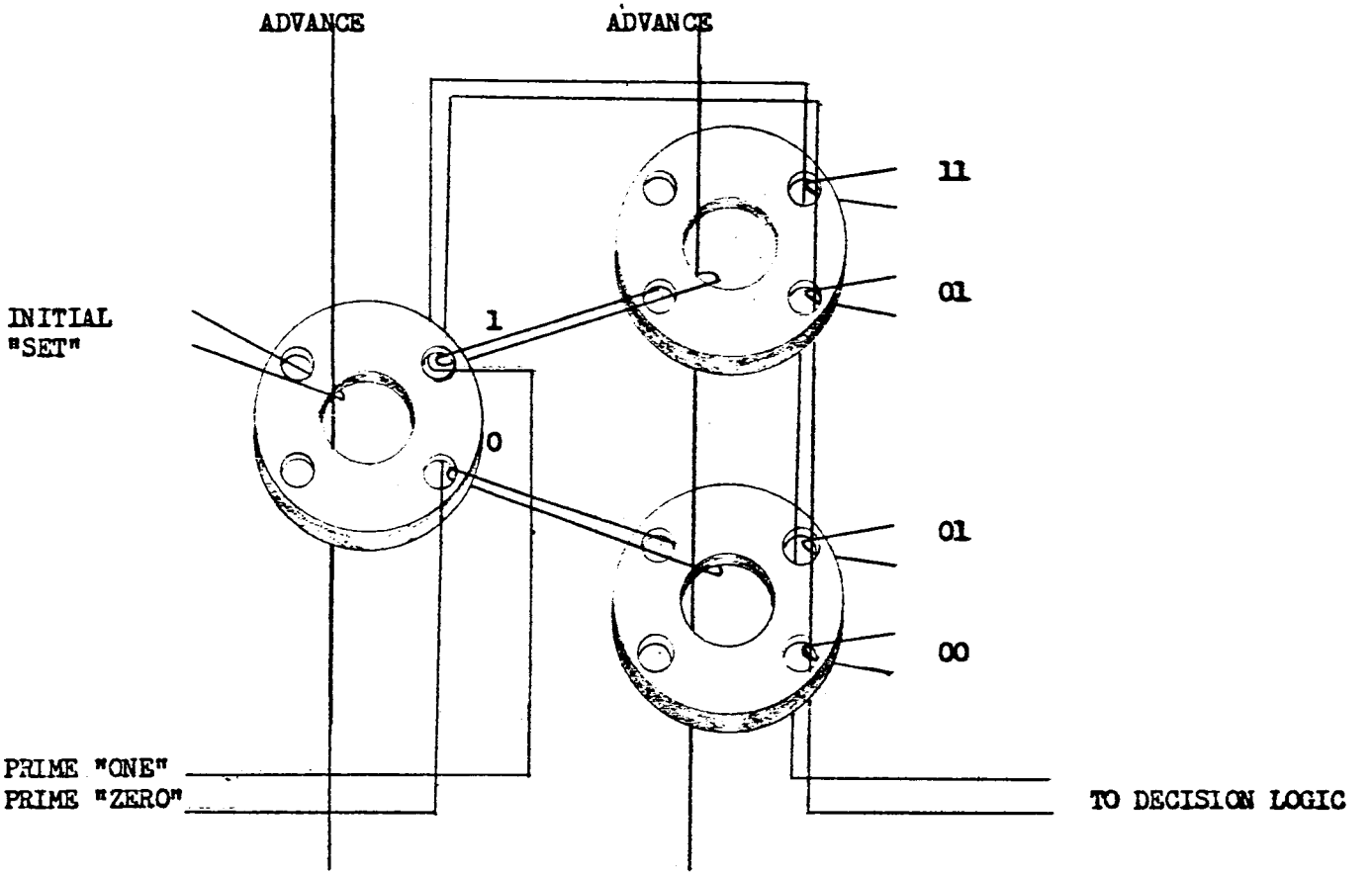


TRANSFER OF CORE STATE

FIGURE 11

clears that core and reverses the flux path under the coupling loop. The current induced in the loop sets core 2. At this time, core 1 is in a clear state and core 2 has been set (see Sketch 3). If a prime pulse is given again, core 2 will be primed around the upper minor aperture and, since core 1 was in a clear state, no change will occur in this core (Sketch 4). This process can continue through "n" cores. Conversely, if the first core of Sketch 1 had been in a clear state when primed, no flux change would have occurred and the subsequent advance pulse merely would have tended to drive the core further toward the clear state. In essence, a clear was transferred from core 1 to core 2.

The usefulness of this core design can be extended to decoding a binary sequence by assembling the cores as illustrated in Figure 12. In this configuration, two prime conductors are used and designated as either the "one prime" or "zero prime". Each decoding tree core has one minor aperture for detecting "one's" and another for "zero's". The prime conductors are threaded through all their respective minor apertures in series and terminate in a decision logic circuit. This circuit is coupled to a shift register in which the code in question has been placed. As this code is shifted from the register to the decision logic, either the "one prime" or the "zero prime" conductor is energized (code dependent). The first core in the tree receives an initial set pulse followed by the priming of either the one or zero aperture. An advance pulse is given to the first core which causes a current induction into the coupling loop associated with the primed aperture. The sequence of priming, setting, and advancing continues for each bit in the code until



MAGNETIC CORE DECODING TREE

FIGURE 12

the unique terminus is reached. In a decoding tree, the number of cores required is equal to 2^{n-1}.

The multi-aperture cores can be read out or sensed by two methods: a destructive or dynamic and a non-destructive or static method. The former method uses a conductor which is passed through the major aperture and an output occurs when the core is shifted. The latter method (non-destructive) is taken across the outer leg of a minor aperture. This sense conductor is driven with a sine wave of about 350 kc at 400 ma. At this current level the major/minor axes of the core is not disturbed but the output wave shape is altered to an easily detectable degree by the flux state of the core. This method of non-destruct readout is employed in the Gemini command and control system.

7.0 SUMMARY OF MULTI-APERTURE MAGNETIC CORES

This digital tool possesses some desirable characteristics which makes it attractive for MOLAB application. Versatility, non-destruct readout, and the elimination of coupling diodes within the memory are a few major features. Yet, several aspects need to be considered when employing a device with such a short history: the frangibility of a completed matrix, the effect of temperature extremes or variations, and the complexity envolved in supporting equipment.

If the above questions can be favorably answered, then the MOLAB vehicle can benefit from these cores in two ways: as a solid state decoder and in the temporary storage of commands. Further study will be necessary before a complete guarantee can be given.

8.0 CODES AND CODING TECHNIQUE

Since this broad catagory encompasses such a vast array of disciplines, only those that may influence the digital command system for a roving vehicle will be presented. Two major schemes will be developed; i.e., the distance protected codes and the codes using parity checks.

8.1 DISTANCE PROTECTED CODES

When a series of discrete pulses are transmitted via an RF link, the transmission is degraded by noise present in the transmitting medium. Primarily, this noise manifests itself in "white Gaussian noise" with added noise steming from more local origins (atmospheric disturbances, etc.). The possible effect of this disturbance on a pulse train is the addition or deletion of an intended pulse which results in an incorrect code or pulse train. The probable number of errors occurring within a finite group of pulses (binary code) can be statistically determined with the major variable being the signal/noise ratio at the command receiver.

Returning to the possibility of the receiver detecting an erroneous code, a very simple sequence will illustrate the error probability; e.g.,

0 0

0 1

1 0

1 1

An inspection of these four codes will show that in 50% of the codes an alteration of either a one or a zero then will result in unintended sequence.

Initial Code	Addition of a "one"	Addition of a "zero"
0 0	0 1 or 1 0	- -
0 1	1 1	0 0
1 0	1 1	0 0
1 1	- -	0 1 or 1 0

Separating this sequence into groups that would require more than a mere addition or deletion of a pulse will offer greater protection from action upon an erroneous code. This, then, is the basis for "distance protected codes".

To further exemplify this coding, two distinct groups may be extracted from this sequence.

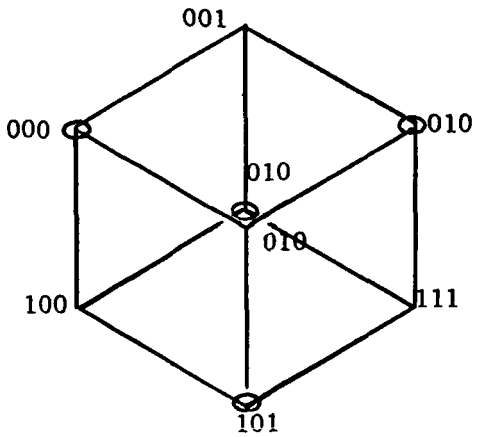
Group	Initial Code	Addition of a "One"	Addition of a "zero"
#1	0 0	0 1 or 1 0	- -
	1 1	- -	1 0 or 0 1
#2	1 0	1 1	0 0
	0 1	1 1	0 0

It is apparent that by selecting a particular code(s) within a finite family of possible codes, a degree of self protection can be achieved. In the above groups (both 1 and 2), the addition or deletion of a bit did not result in portraying a code that would be acted upon as in each group the only matrices that would be present are those given under "initial code".

Obviously, this sequence of only two binary digits is too limited for most command applications, but to achieve this self protection within a

large family becomes difficult if only the inspection method is used.

Hamming has described a method of creating a three-dimensional model for determining single-error detecting codes; that is, a code which can be displaced by a single digit and which will not represent another command. For relatively few codes, his method is simple and accurate; for example, if single-error detecting codes were desired from a sequence of three successive bits (0 - 7 decimal count), a three-dimensional model would be:



The code determination is performed from this model by assuming a starting point at one vertex and then traversing to the next protected code by moving through one right angle. The acceptable codes are illustrated in the sketch by noting those vertices that are circled. For reference, those codes are listed below:

0 0 0

0 1 1

1 1 0

1 0 1

It is evident that in each selected code a change of at least two bits is necessary in order to duplicate any outer code. This Hamming

method of code determination by models can be extended by placing a "cube within a cube"; however, with many bits (say, five or six), the construction and interpretation becomes unwieldy.

To more easily determine distance protected codes when using a more extensive pulse train, the Karnaugh-Vetch mapping method offers an easier approach. In this model, all possible codes are evident with the selection of distance protection being made by visual plotting of the "x" and "y" coordinates. The example of the Kernaugh-Vetch code map as given in Figure 13 is a single-error detecting code with an arbitrary start at 0 0 0 1 0 0 0 1; however, many possible code sequences may be constructed using a different initial vertex. This map method may be extended for use in determining not only single-error detecting codes as illustrated, but also single-error correcting double-error detecting and double-error correcting and detecting codes.

It should be noted, however, that with each additional "condition" that is attached to the code group, the total number of protected codes that can be realized from a finite series of digits is reduced.

8.2 PARITY CHECKED CODES

In parity checked codes, at least one position within the code is used to check the validity of that sequence. One of the most common schemes is to use an "odd" parity check in which the number of "one's" appearing within any one code sequence is always "odd" (1, 3, 5, etc.). This condition is maintained by adding either a "one" or a "zero" in the parity check position

Major \ Minor	00				01				11				10				Major
	00	01	11	10	00	01	11	10	00	01	11	10	00	01	11	10	Minor
00		A		B	C		D			E		F	G		H		
00	01	I		J			K		L	M		N			O		P
	11		Q		R	S		T			U		V	W		X		
	10	Y		Z			AA		AB	AC		AD			AE		AF
	00	AG		AH			AI		AJ	AK		AL			AM		AN
01	01		AO		AP	AQ		AR			AS		AT	AU		AV	
	11	AW		AX			AY		AZ	BA		BB			BC		BD
	10		BE		BF	BG		BH			BI		BJ	BK		BL	
	00		BM		BN	BO		BP			BQ		BR	BS		BT	
11	01	BU		BV			BW		BX	BY		BZ			CA		CB
	11		CC		CD	CE		CF			CG		CH	CI		CJ	
	10	CK		CL			CM		CN	CO		CP			CQ		CR
	00	CS		CT			CU		CV	CW		CX			CY		CZ
10	01		DA		DB	DC		DD			DE		DF	DG		DH	
	11	DI		DJ			DK		DL	DM		DN			DO		DP
	10		DQ		DR	DS		DT			DU		DV	DW		DX	

FIGURE 13 - CODE DETERMINATION FOR SINGLE-ERROR DETECTION USING KARNAUGH-VETCH MAP WITHOUT PARITY CHECK

Explanation:

A code is read from this matrix by first noting the major horizontal designation, then the minor designation. The next four bits are determined by first reading the two major vertical bits, then the two minor vertical entries.

as a function of the "ones" in the message body. Too, an "even" parity check can be used with the parity bit by maintaining an even number of "ones".

Although this very simple method has had wide acceptance in the hard-wired systems, the amount of confidence is proportional to the message length. Within a message, if an odd number of bits change their characteristics, then the single parity check will work. But if the change occurs in an even number of bit positions, the ability to detect an error vanishes. Other drawbacks to this method include the inability to correct a code and the inability to establish the position in which an error occurred.

R. W. Hamming, in his paper for the Bell System Technical Journal, describes a method by which the number of parity check bits becomes a function of the message length. This same method also isolates the particular bit in error. For simplicity, the single-error correcting code will be used to illustrate the principle, but this same operation can be extended to very elaborate parity checks which can correct several errors within a code sequence.

In a single-error correcting code with parity checking:

n = number of bits in sequence

m = number of bits used in this sequence for message information

k = parity check bits

Therefore:

$k = n-m$

The "checking number" which describes the positional error (if an error has been detected) is derived by observing the true or not true condition of

the "k" bits with respect to "m" bits; i.e., if the parity bit (k) is not true (or non-agreement) with respect to a checked position in the "m" code, a "one" is entered in a register reading from right to left. Conversely, a "zero" is entered in the same register if a true condition is detected. The summation of the binary number in the register denotes the position in error within the message sequence. This checking number must describe the $m + k + 1$ separate identities so that

$$2^k \geq m + k + 1,$$

which is a function of k. With $n = m + k$, then

$$2^m \geq \frac{2^n}{n + 1}$$

This inequality will give the maximum "m" for a given "n".

If an example is taken (say $n = 7$), then:

$$2^m \leq \frac{128}{8}$$

$$2^m = 16$$

$$m = 4$$

Therefore:

$$n = 7$$

$$m = 4$$

$$k = 3$$

Having established "k", the positions over which each k-bit has influence is determined. The first parity bit validates all binary counts ending in a

binary "one", as shown in:

Decimal Equivalent	1	= 1
	3	= 1 1
	5	= 1 0 1
	7	= 1 1 1
		etc.

The second parity check bit validates all binary counts in which the second position contains a "one"; i.e.,

Decimal Equivalent	2	= 1 0
	3	= 1 1
	6	= 1 1 0
	7	= 1 1 1
	10	= 1 0 1 0
		etc.

The third parity check bit validates the binary count in which the third position contains a "one"; i.e.,

Decimal Equivalent	4	= 1 0 0
	5	= 1 0 1
	6	= 1 1 0
	7	= 1 1 1
	12	= 1 1 0 0
		etc.

The positions within the pulse train occupied by the parity bits are 1, 2, 4, 8, etc., which have the advantage of mutual independence.

The format of this code (n = 7, m = 4, k = 3) using an even parity check is given below:

3rd parity check				3	3	3	3	
2nd parity check		2	2			2	2	Decimal Number
1st parity check	1		1		1		1	
	0	0	0	0	0	0	0	0
	1	1	0	1	0	0	1	1
	0	1	0	1	0	1	0	2
	1	0	0	0	0	1	1	3
	1	0	0	1	1	0	0	4
	0	1	0	0	1	0	1	5
	1	1	0	0	1	1	0	6
	0	0	0	1	1	1	1	7
	1	1	1	0	0	0	0	8
	0	0	1	1	0	0	1	9
	1	0	1	1	0	1	0	10
	0	1	1	0	0	1	1	11
	0	1	1	1	1	0	0	12
	1	0	1	0	1	0	1	13
	0	0	1	0	1	1	0	14
	1	1	1	1	1	1	1	15
Function	k_1	k_2	m	k_3	m	m	m	
Position	1	2	3	4	5	6	7	

To illustrate the code-correcting ability of this scheme, assume the code for a decimal 10 in the above format.

Decimal 10 = 1 0 1 1 0 1 0

Inserting an error in the train = 1 0 1 1 0 0 0, then by comparing parity bits.

	Given k	Correct k	Validity
k_1	1	1	0 (true)
k_2	1	0	1 (not true)
k_3	0	1	1 (not true)

When the validity checks are entered in a register from right to left,

110 ⟵ Register = decimal 6

and the binary count is read to the decimal equivalent. This will give the positional error; i.e., sixth place (reading from the left).

Using this small number (7) for "n" requires that 3/7 of the word be devoted to parity checking, but extending the code group to approximately 39 bits (the proposed MOLAB format) would require only 5 parity bits as

$$2^m = \frac{2^n}{n+1}$$

$$m \log^2 = \frac{549 \times 10^9}{40}$$

$$m \log^2 = 13.7 \times 10^9$$

$$m = \frac{10g\ 1.37 + \log 10^{10}}{0.301}$$

$$= \frac{(0.136 + 10.0)}{0.301}$$

$$= \frac{10.136}{0.301}$$

$$m = 34$$

$$k = 5$$

This coding technique can be expanded to:

a. Single error detecting

b. Single error correcting

c. Single error correcting - double error detecting

d. Double error correcting

However, the number of active codes decreases with each additional qualification as is shown in the following formulas:

$$a = \frac{2^n - 2}{n - 1}$$

$$b = \frac{2^n}{n + 1}$$

$$c = \frac{2^n}{n + 2}$$

$$d = \frac{2^n}{n + 3}$$

APPENDIX

ANALYSIS OF STORAGE REQUIREMENTS FOR TIME LABEL ON MCLAB VEHICLE

In an effort to size the required storage time for commands, an analysis was made of the "see time" of the moon from Goldstone, California. This analysis was based on the following data:

1. The moon's ecliptic exceeds the sun's ecliptic by 5.8", which permits the moon to extend its zenith position to about 28-1/2° north and south latitude.

2. The "look angle" of Goldstone's antennas is assumed to be within 5° of the horizon.

3. A worst case condition within any 24 hour period would exist when the moon's ecliptic would position that body at 28.5' south latitude.

By noting the sketch in Figure 14, two times the length of side "b" will give, in relation to time, the number of additional hours that the moon would be hidden from latitude 35° N (Goldstone). The added time to "acquire" the moon at 5° above the horizon must be included. Therefore, if the moon were positioned over the equator, the hours of moon view would be η radians for 12 hours.

To determine the cord length "b" using spherical trigonometry:

1. $\text{Sin } a = \tan b \cos \beta$

2. $\tan b = \dfrac{\sin a}{\cos \beta + 5^\circ}$ (look angle of Goldstone's antennas)

3. $\tan b = \dfrac{\sin 35^\circ}{\cos 28.5 + 5}$

4. $\tan b = \dfrac{0.57358}{1.5108}$

5. $\tan b = 0.3835 = 21^\circ = 0.366$ radians

The conversion to a time base is

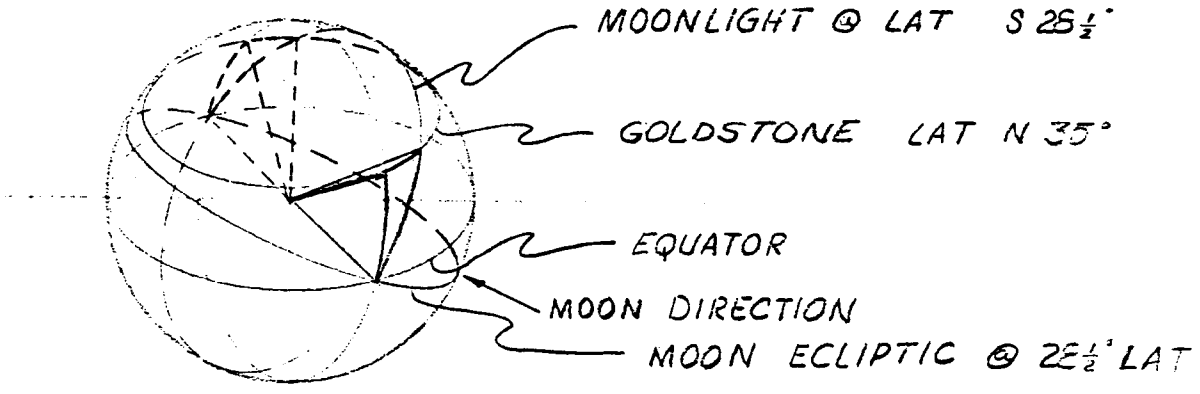
$$t = \frac{\pi - 26}{w_e}$$

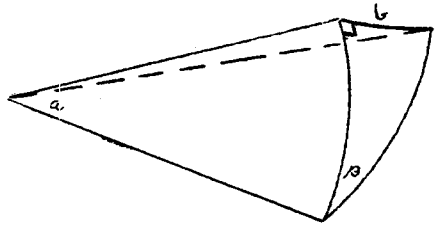
Where $w_e = \pi/12$ hours

$$t = \frac{3.1416 - 0.732}{w_e}$$

$$t = 9.2 \text{ hours}$$

The figure of 9.2 hours results in a maximum time of 14.8 hours that will be required for storage of commands issued for Goldstone. Admittedly, this is a worst case condition, as the moon's travel has been negated in this study --- a factor which would tend to increase the view time.


MOONLIGHT @ LAT S 28½°
GOLDSTONE LAT N 35°
EQUATOR
MOON DIRECTION
MOON ECLIPTIC @ 2E½° LAT
SOUTH POLE


b
a
B

1. Hamming, R. W., "Error-Detecting and Error-Correcting Codes", The Bell System Journal, Volume XXVI, April, 1960

2. Clark, R. C., "Diagrammatic Method of Code Construction", AIEE Transactions, January, 1959, pp 817 - 823

3. Karnaugh, M., "The Map Method For Synthesis of Combinational Logic Circuits", AIEE Transactions, November, 1953, pp 593 - 599

4. Gilbert, E. N., "Synchronization of Binary Messages", IRE Transactions, September, 1960, pp 470 - 477

5. Bowen, J. S., "To Branch or Not to Branch", AMP, Incorporated, 1962

6. Huskey and Korn, Computer Handbook, McGraw-Hill

7. Nichols and Rauch, Radio Telemetry, J. Wiley and Sons

8. Cerni, R. H. and L. E. Foster, Instrumentation for Engineering Measurements, J. Wiley and Sons

9. Shannon, C. E. and Warren Weaver, The Mathematical Theory of Communication, The University of Illinois Press

10. Monroe, A. J., Digital Processes for Sampled Data Systems, J. Wiley and Sons

11. NASA Communication Control, "C & C Subsystem Engineering Analysis Report Gemini Agena Target Vehicle", AD 412660, July, 1963

DISTRIBUTION

INTERNAL

DIR
DEP-T
R-DIR
R-AERO-DIR
-S
-SP (23)
R-ASTR-DIR
-A (13)
R-P&VE-DIR
-A
-AB (15)
-AL (5)
R-RP-DIR
-J (5)
R-FP-DIR
R-FP (2)
R-QUAL-DIR
-J (3)
R-COMP-DIR
R-ME-DIR
-X
R-TEST-DIR
I-DIR
MS-IP
MS-IPL (8)

EXTERNAL

NASA Headquarters
MTF Col. T. Evans
MTF Maj. E. Andrews (2)
MTF Mr. D. Beattie
R-1 Dr. James B. Edson
MTF William Taylor

Kennedy Space Center
K-DF Mr. von Tiesenhausen

Hayes International Corporation (5)
Missile And Space Support Division
Apollo Logistics Support Group

Scientific and Technical Information Facility
P.O. Box 5700
Bethesda, Maryland
Attn: NASA Representative (S-AK RKT) (2)

Manned Spacecraft Center
Houston, Texas
Mr. Gillespi, MTG
Miss M. A. Sullivan, RNR
John M. Eggleston
C. Corington, ET-23 (1)
William E. Stanley, ET (2)

Donald Ellston
Manned Lunar Exploration Investigation
Astrogeological Branch
USGS
Flagstaff, Arizona

Langley Research Center
Hampton, Virginia
Mr. R. S. Osborn