THIRD QUARTERLY REPORT
ON
MOLECULAR POWER SUPPLY
SYNCHRONIZER
FOR THE PERIOD
NOVEMBER THROUGH JANUARY 31, 1963

JPL ORDER 950237
under
NAS 7-100

Westinghouse Electric Corporation
Astroelectronics Department
Newbury Park, California

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LIST OF ILLUSTRATIONS

CONTRACT OBJECTIVES AND GENERAL APPROACH

The contract objectives have remained the same as those outlined in previous reports, as has the general approach. However, further design work on the interconnection pattern has shown that it is not possible to perform all the required connections without using .0005 inch lines in some places. While this can be done with our existing techniques, it was felt that the increased resistance in the lines, particularly the ground, and decrease in reliability was not at all advisable.

A redesign of the basic logic element layout was done to:

1. increase the number of crossover tubs,
2. optimize the shape and location of the existing ones for the connections required.

Utilizing the new design, a much more satisfactory layout has been designed but has not been finalized at this writing. The feasibility of the NPN portion of the output switches has been proven, with satisfactory devices fabricated and tested. The PNP portion has been designed. Finally, the package design has been completed and a subcontract let for procurement.

AUTHOR

A change of project management has been effected from C. F. Inniss to D. A. Deardorf, who has been associated with the project for the past several months.

PROJECT BREAKDOWN

There has been a change in the PERT type diagram necessitated by the redesign of the logic elements for interconnection reasons. This chart is shown in Figure 1, effective February 1, 1963. Figure 2 is the tabulation of path lengths from this PERT diagram. The longest path length is now 60 weeks for the above mentioned reasons. This represents an eight week over-ride from original target completion date. Every effort is being made to decrease this time.

The tasks will be discussed in the following order:

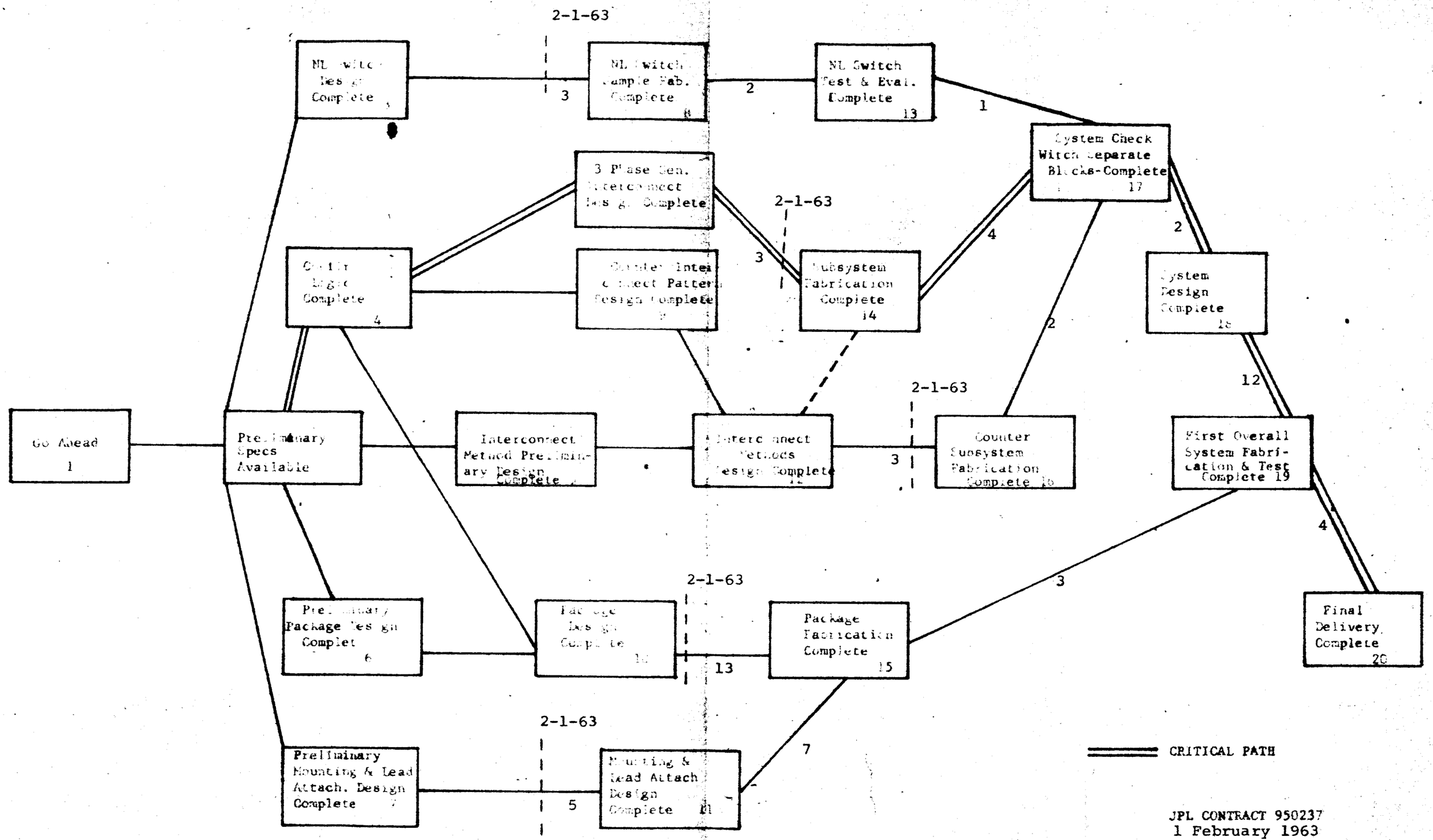
(a) Interconnect pattern design

(b) Output switch design

(c) Packaging design

(d) Partial system fabrication

(e) Overall system and fabrication.



JPL CONTRACT 950237
1 February 1963

FIGURE 1

J.P.L. CONTRACT 950237

TABULATION OF PERT CHART PATHS

1 FEBRUARY 1963

To 2-1-62	35	To 2-1-62	35	To 2-1-62	35	To 2-1-62	35	To 2-1-62	35
2-1-62 - 8	3	2-1-62 - 14	3	2-1-62 - 16	3	2-1-62 - 15	13	2-1-62 - 11	5
8 - 13	2	14 - 17	4	16 - 16	2	15 - 19	3	11 - 15	7
13 - 17	1	17 - 18	2	17 - 18	2	19 - 20	4	15 - 19	3
17 - 18	2	18 - 19	12	18 - 19	12			19 - 20	4
18 - 19	12	19 - 20	4	19 - 20	4				
19 - 20	4								
	59		60		58		55		54

Figure 2

INTERCONNECT PATTERN DESIGN

A great deal of effort has been expended on this task. A complete layout with the "microstroke" elements was made. This included the five binary counter stages and the three phase generator, all properly connected to perform this function. However, to do this, it was ncessary to use .0005 inch wide lines in several places with .0005 inch spacings. This can be done with our current photo masking techniques, but working to such tolerances over a large area is extremely difficult. Shown in Figure 3 is a drawing of a single binary counter layout. Figure 4 presents the array of five at a reduced scale. Masks were made and test evaporations performed. Resolution was good, but tolerances were very close. Resistance measurements varified the calculations which showed marginal operation would result due to voltages developed in the aluminum ground return. Thus, exhausting all possible approaches short of a basic redesign of the layout, it was undertaken.

For reliability reasons, as discussed above, redesign of the basic logic element layout was undertaken. The drawing

in Figure 5 shows a typical layout without interconnections. The asymmetry of the unit results from a four unit arrays to easy connection problems without extending the area per device any more than necessary. The number of crossover tubs was increased and their shapes optimized for this extensive system. Work on completing the interconnection pattern design followed immediately and has since shown that the complete system layout can be accomplished with no line or spacing less than .001 of an inch and with a ground line width of as large as .003" in some areas. This final drawing is in preparation at this writing.

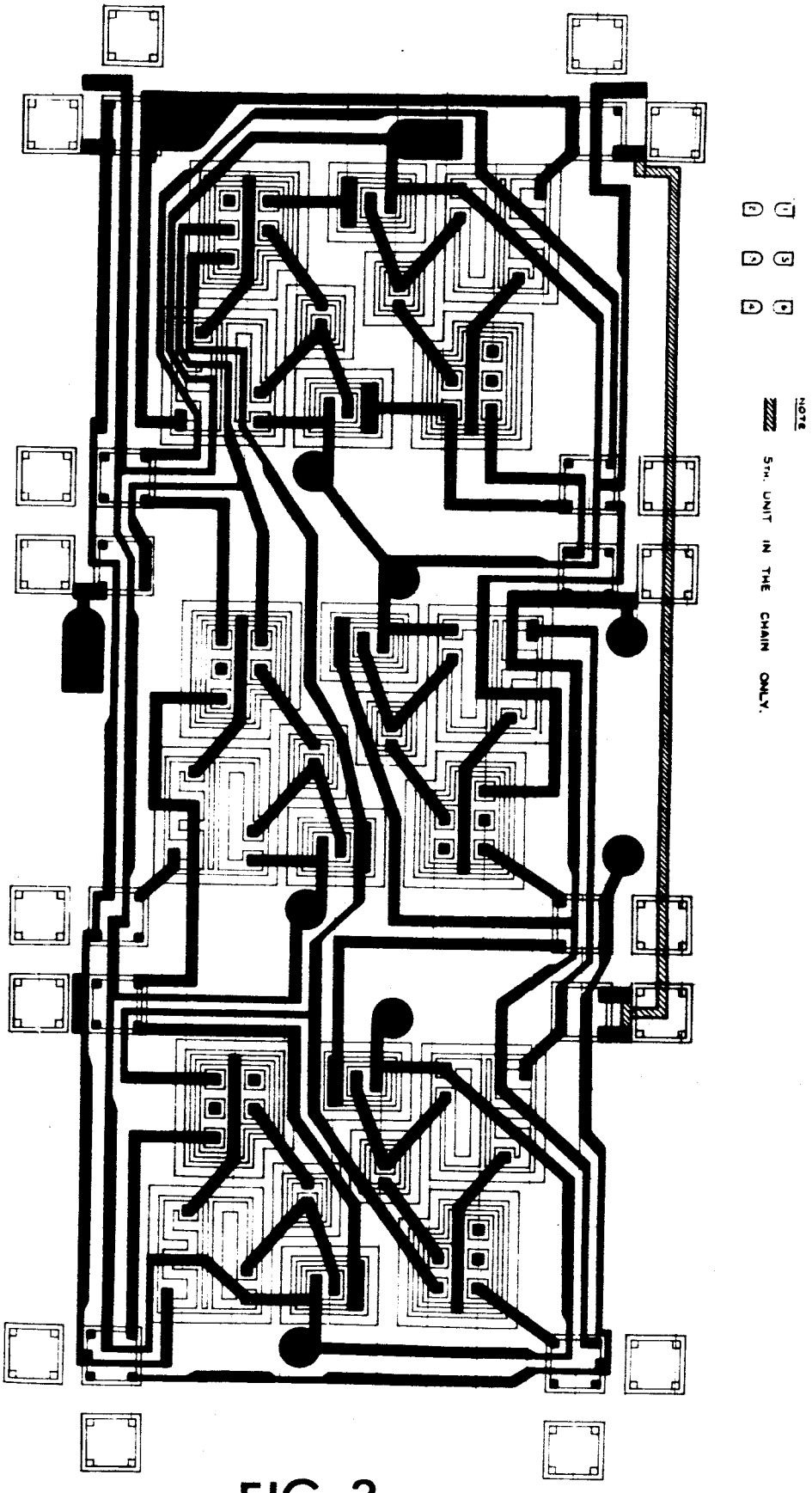


FIG. 3

SINGLE BINARY COUNTER

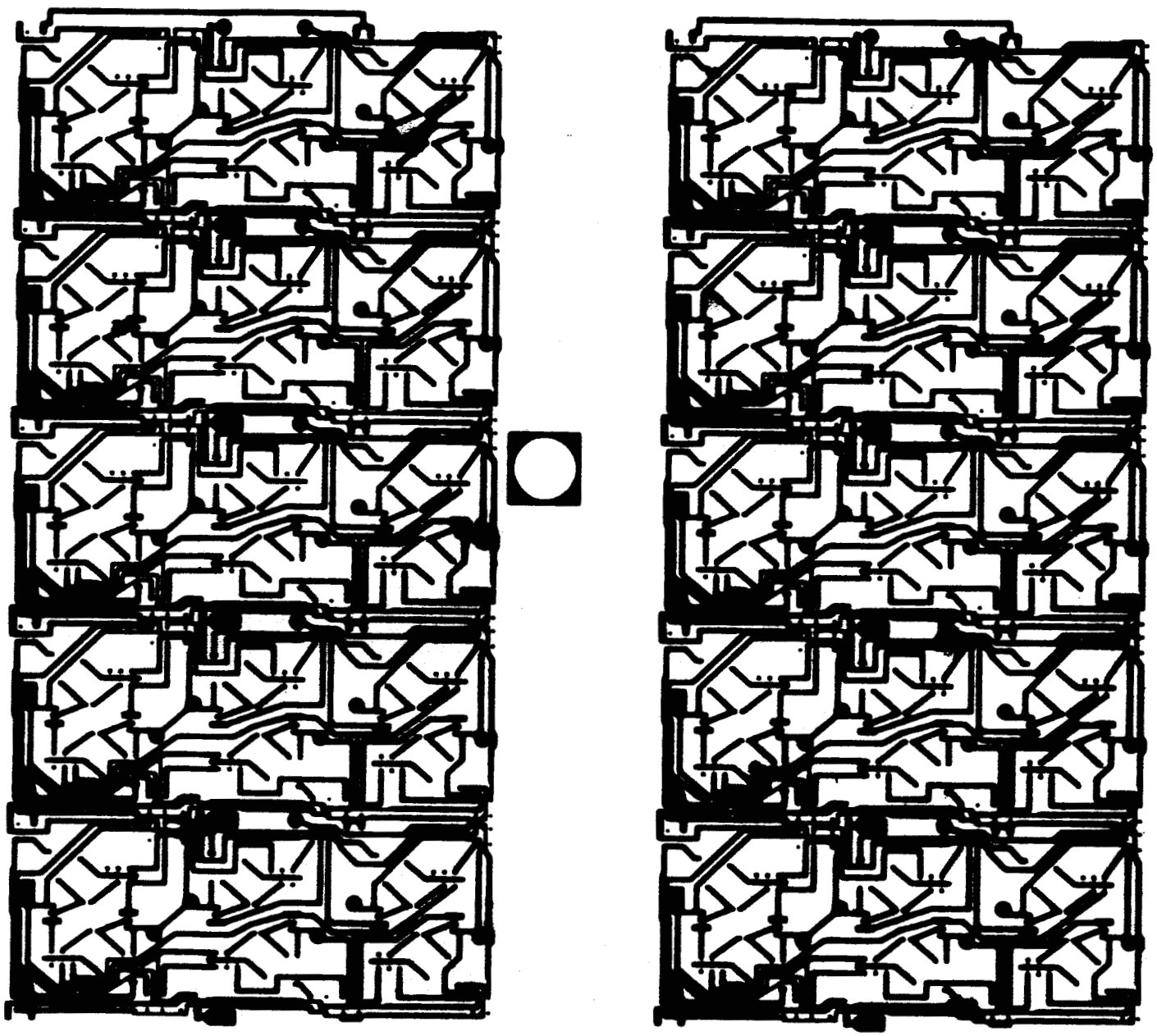


FIG. 4

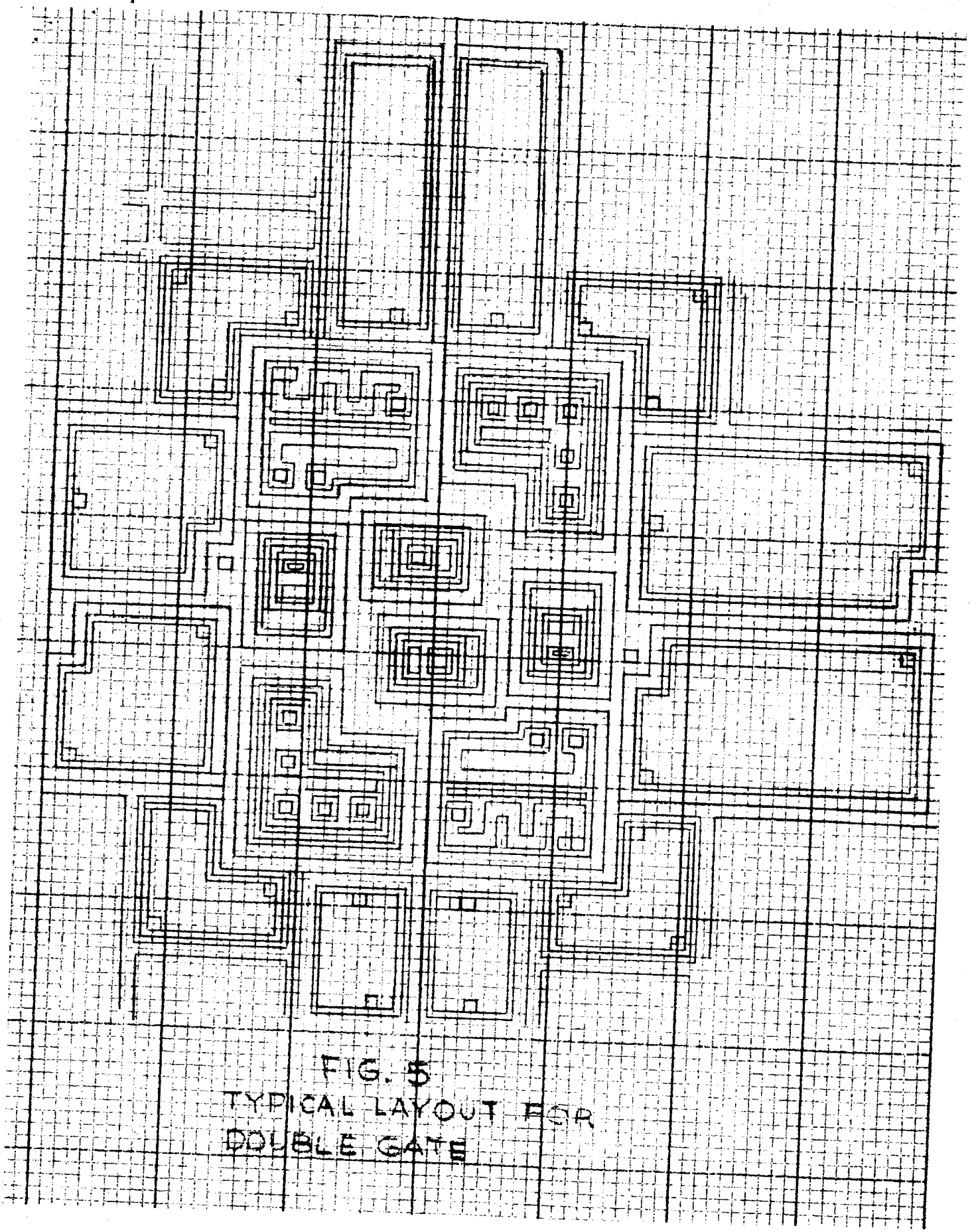


FIG. 5
TYPICAL LAYOUT FOR
DOUBLE GATE

OUTPUT SWITCH DESIGN

The NPN portion of the output switch was fabricated in the manner shown in the previous quarterly report. Typical parameters are shown below.

OUTPUT

V_{CER} = 68 Volts

h_{FE} = 30

R_{Load} = 5K

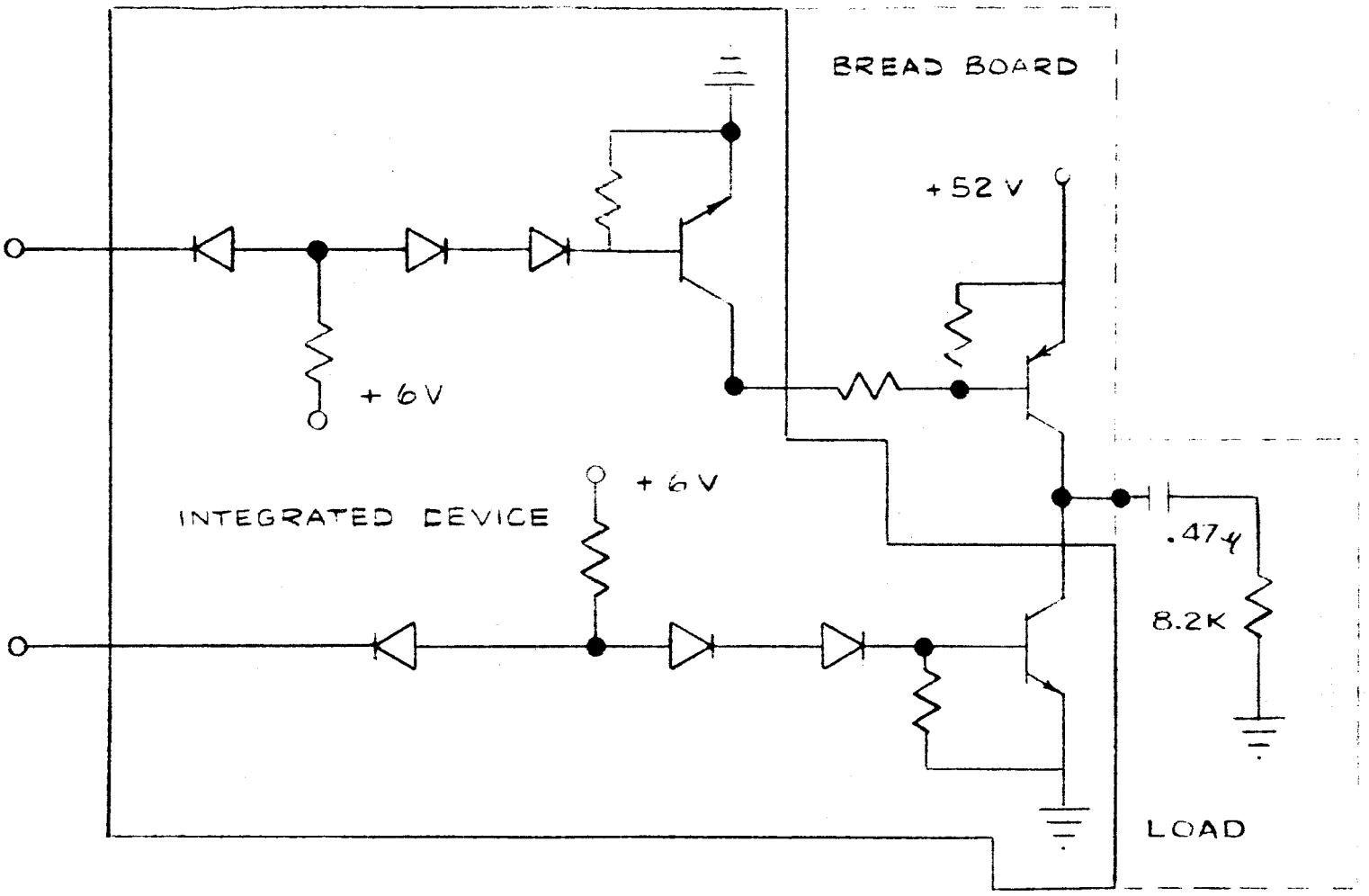
V_{Offset} = 100 millivolts at I_B = 1.6 ma, I_C = 0

V_{CBO} = 85 Volts

$V_{Isolation}$ = 110 Volts

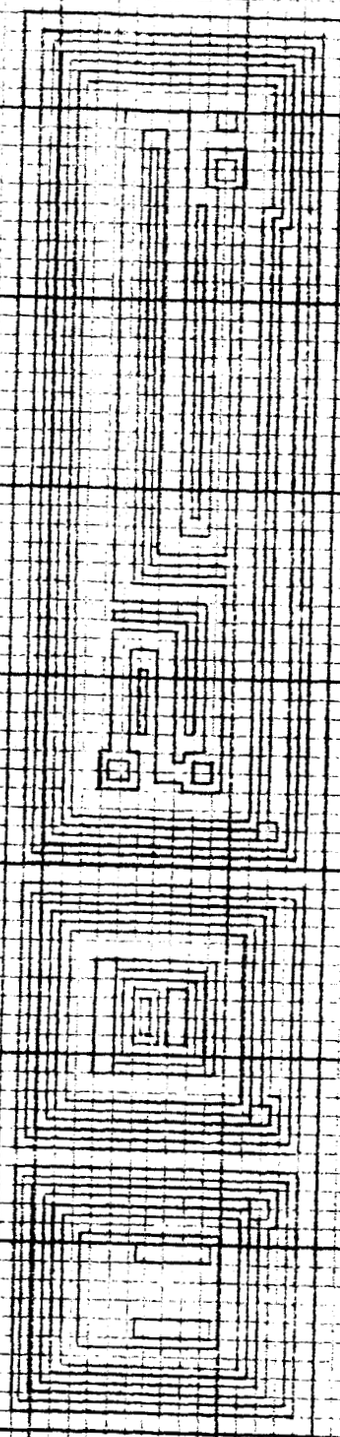
Samples of these devices were tested functionally under environmental conditions of -55°C to + 100°C. Rise and fall times of less than 5 micro seconds were maintained over the complete range. The offset voltage was less than 200 millivolts under all conditions. A breadboard of the PNP portion with a simulated load was used for the tests as shown in Figure 6. The devices discussed were of a large geometry variety because masks were available at no cost. Subsequently, masks of the final design w e r e obtained and runs are in process.

Design of the PNP has been completed. A diagram of the layout is shown in Figure 7. The length to width ratio is purposely large to better accommodate the packaging. Photo reduction is now in process.



FUNCTIONAL TESTS OF NON LINEAR LOAD SWITCH

FIGURE 6



PNP PORTION OF
OUTPUT SWITCH

FIG. 7

PACKAGE DESIGN

Design of the package has been completed, and a subcontract let to Eitel-McCullough for the fabrication of 100 pieces. The package is made with copper flanges and will be cold welded. Pins are nickel brazed through the high alumina ceramic base.

A moly-manganese metalization covers the area between the pins, which, when gold plated, provides direct mounting of the dice. This manufacturer is currently supplying such substrates to power transistor manufacturers for mounting even larger dice than this contract requires. In order to prove further that no thermal matching material is required, tests will be performed prior to completion of the package so that a tungsten substrate could be incorporated if needed. Figure 8 is a drawing of the header and lid.

Referring to Figure 8, the pin locations will be as follows: clockwise from the top, starting from the blank pin: (1) 38.4KC input, (2) 6 Volt supply, (3) ground, (4) not used, (5) not used, (6) 2.4KC output, (7) 52 volts supply, (8), (9), (10) three phase outputs, (11) not used. Unless a further improvement in the layout can be made, this will be the final configuration. Study of a means of grounding the base independently for improving the noise immunity of the system is being investigated.

REVISIONS				
SYM	DESCRIPTION	BY	DATE	APPROVAL

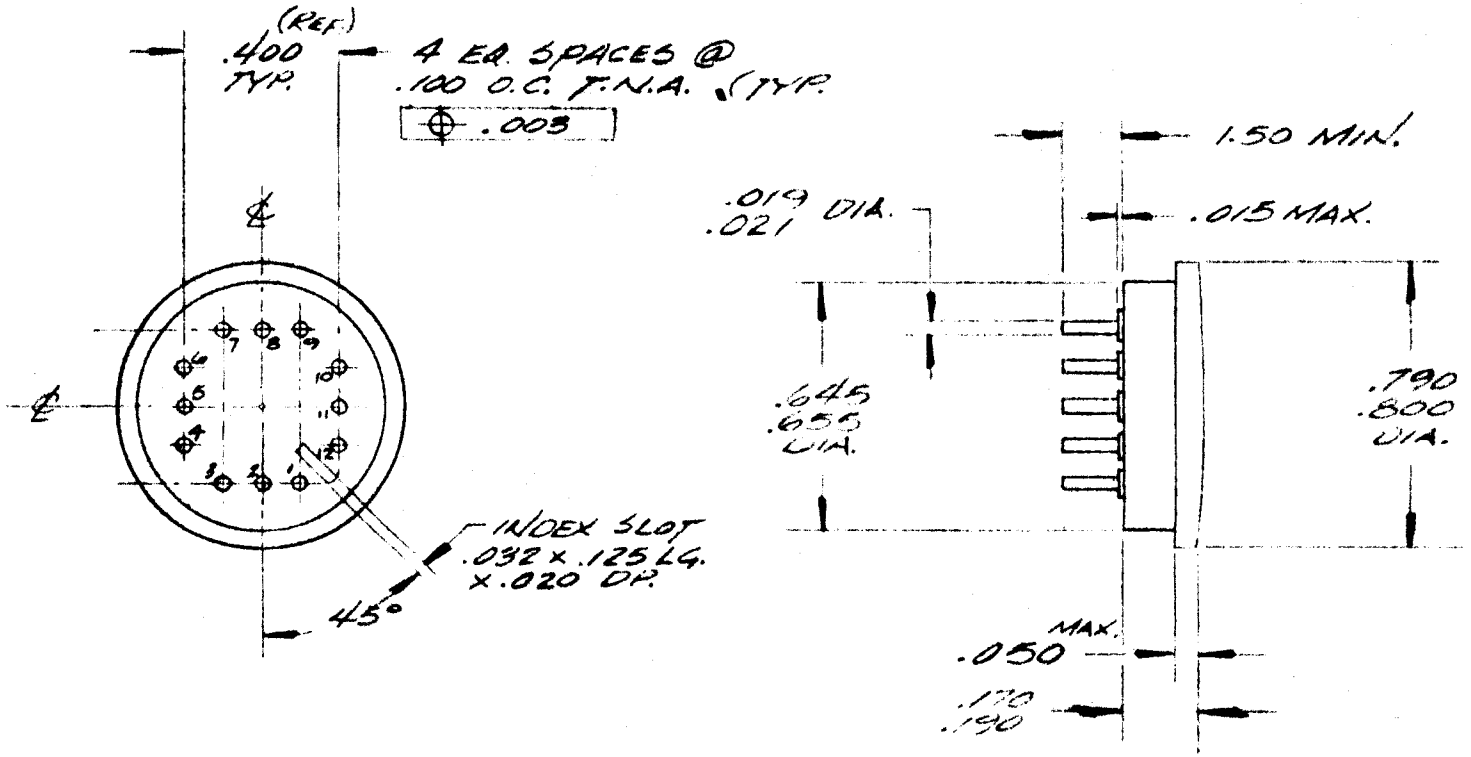


FIG. 8

ITEM NO.	QTY.	SHEET NO.	PART NUMBER	DESCRIPTION	SUGGESTED SOURCE

MATERIAL:
BODY - 96% Al_2O_3 / COPPER
LEADS - NICKEL

FINISH
PLATING: 100 μ INS. OF
HIGH PURITY ACID GOLD

TOLERANCES AND NOTES
UNLESS OTHERWISE SPECIFIED

DECIMAL .XXX ±.005 .XX ±.010 FRACTIONAL ±1/64 ANGULAR ±0° 30'

BREAK ALL SHARP EDGES .010
ALL DIMENSIONS INCHES
DO NOT SCALE THIS DRAWING

DRAWN	J. YEOMANS	DATE 2-18-63
CKD.		DATE
ENGR.	R.B. LAMPLEIGH	DATE 2-18-63
APPD.		DATE
APPD.	R.B. LAMPLEIGH	DATE 2-18-63
RELEASED		DATE 2-18-63

Westinghouse
ELECTRIC CORPORATION
ASTROELECTRONICS LABORATORY
NEWBURY PARK, CALIFORNIA

J.P.L. COLD WELD
HEADER

SCALE	DWG.		
	A SIZE	710057	B

SHEET 1 OF 3

PARTIAL SYSTEM FABRICATION

As reported previously, binary counters have been made on a single substrate. Further extension of this task has been delayed until revised interconnect masks are available.

OVERALL SYSTEM FABRICATION

Overall system fabrication will commence upon completion of the layout.