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ANALOG TO DIGITAL CONVERTER FOR THE S-57 ION-CHAMBER EXPERIMENT

by Joseph C. Thornwall

Goddard Space Flight Center

Greenbelt, Md.

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SUMMARY

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This paper describes the circuits used in an analog-to-digital (A-D) converter designed for satellite application. The average power requirements are minimized by using linear and non-linear magnetic circuits wherever possible. The analog input voltage is encoded by sequential comparisons with a reference voltage. The sequencing is accomplished with one-bit magnetic ring counters and the reference voltages are generated and summed in windings of blocking oscillator transformers.

Author

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INTRODUCTION

This paper describes an 8-bit analog-to-digital converter (Figure 1) using magnetic-core and solid-state components in pulse operation. All of the circuits are pulse-type with the exception of two telemetry input amplifiers, one data output gate, one transistor flip-flop and a DC comparator circuit. The input amplifiers were necessary to improve the rise and fall time of the telemetry

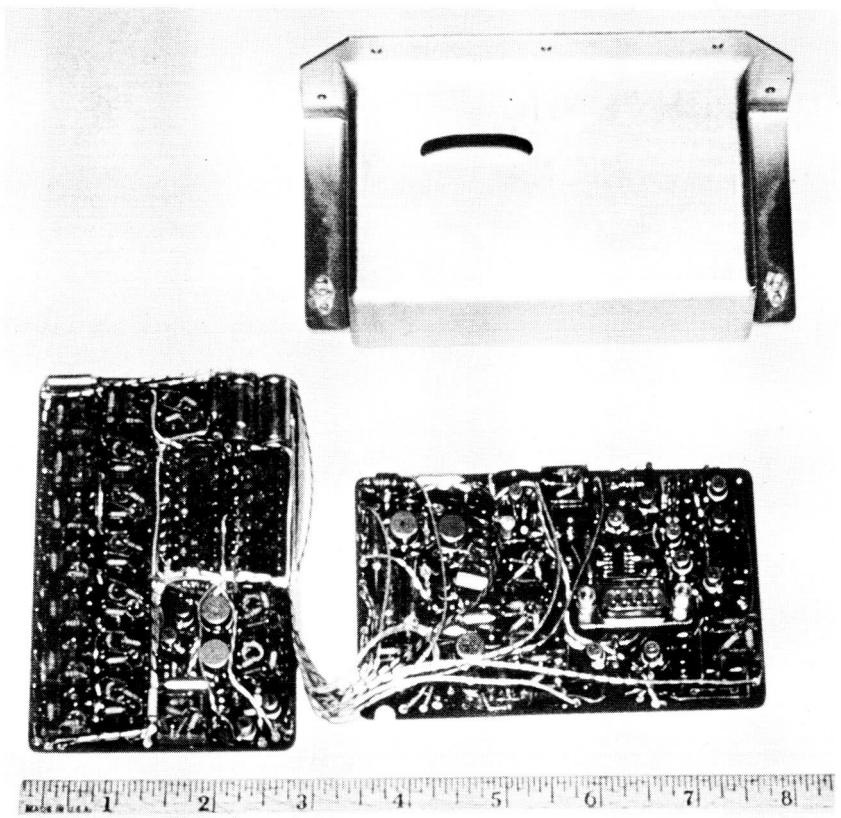


Figure 1a—Analog-to-digital converter (unassembled).

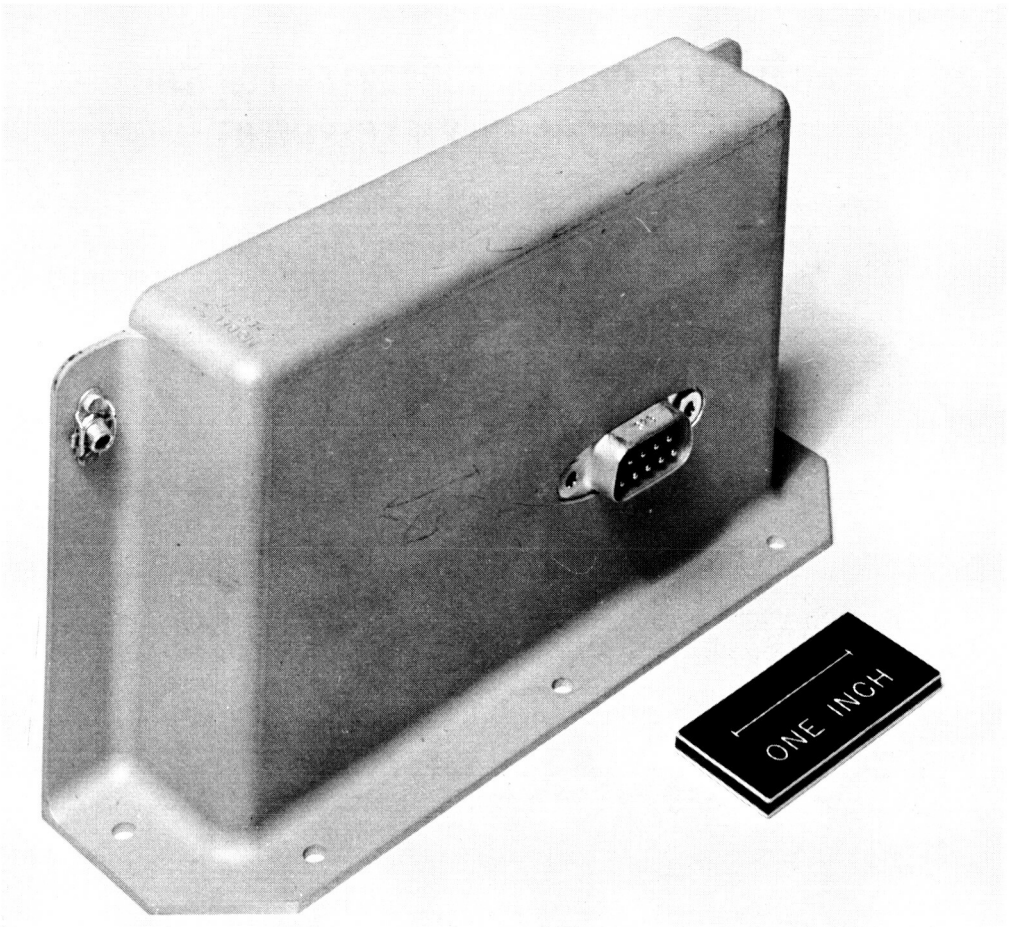


Figure 1b—Analog-to-digital converter (assembled).

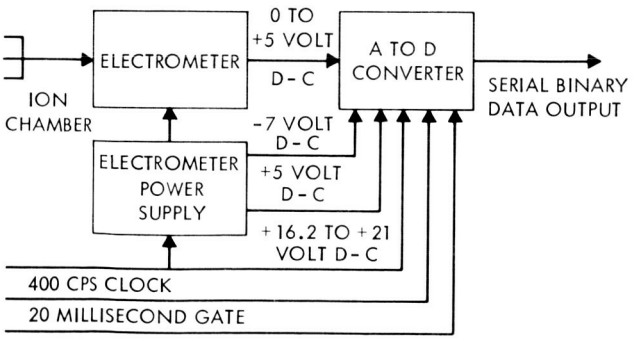


Figure 2—System block diagram.

signals and the flip-flop was required to convert the output binary number pulses to DC levels suitable for use by the data handling system. Figure 2 is a simple overall system block diagram showing how this converter fits into the system.

A pulse-circuit magnetic-core design approach was used for the following reasons: to minimize the average power consumption; to provide low impedance circuits to reduce cross coupling problems in a relatively high component density package; to make possible a high base current overdrive design, for good circuit operation at low temperatures, without increasing the average power consumption; to take advantage of the inherent reliability offered by magnetic components; and to make use of the multiterminal possibilities available in magnetic components and as a result reduce the number of components required.

ENCODING

This converter uses a comparison method of encoding the analog input voltage (Reference 1). Figure 3 is a simple block diagram of the converter. This block diagram will be used to illustrate, element by element, the encoding method. The analog voltage to be encoded is applied to one input of a two-input comparison circuit. A reference amplitude pulse voltage is applied to the other input. An output signal from the comparison circuit will occur when the amplitude of the reference input pulse is greater than the amplitude of the analog voltage input.

There are eight voltage sources available from the reference pulse generators. Each of these eight voltages is weighted in a binary fashion and can be controlled to sum all or any combination of these weights. If the maximum analog voltage is 5.1 volts, then the minimum analog voltage weight is .02 volts. Table 1 is a list of the voltage values of all eight levels.

The 400 cps clock input signal is applied to a sequencer, a control circuit and a gate. This input signal serves to time and control the formation of the binary number.

The word gate pulse input allows eight clock pulses to be applied to the converter during the gate interval.

The sequencer provides a means of triggering the reference voltage pulse generators sequentially, from the most significant amplitude (S_8) first, to the least significant amplitude (S_1) last.

The control circuit is arranged to continue to trigger particular reference pulse generators. This circuit can continue to hold a reference pulse generator on the remaining bits in the word after the sequencer trigger. That is; S_8, would be triggered for 7 more clock pulses; S_7, for 6 more; etc. Thus S_1, the last bit of the word, does not require further holding.

The comparison circuit is used to determine whether or not the control circuit will continue to hold a reference voltage pulse generator. If a comparison circuit output signal *does* occur, when the sequencer triggers a reference voltage pulse generator, then the control circuit *will not* continue to trigger this reference generator on subsequent clock pulses. Conversely, if a

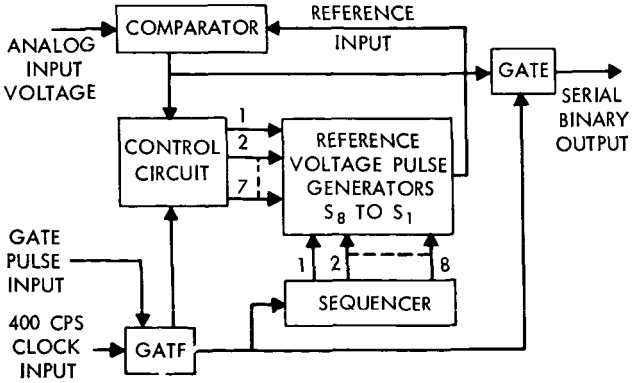


Figure 3—Encoding method.

Table 1

Voltage Values for Reference Pulse Generator Outputs.

Voltage Source	Binary Weight	Voltage Amplitude (volts)
S_1	2^0	0.02
S_2	2^1	0.04
S_3	2^2	0.08
S_4	2^3	0.16
S_5	2^4	0.32
S_6	2^5	0.64
S_7	2^6	1.28
S_8	2^7	2.56

comparison output signal *does not* occur then the control circuit *will* continue to trigger this reference generator on subsequent clock pulses. This represents the two conditions in which the reference voltage pulse amplitude has and has not, respectively, exceeded the amplitude of the analog input voltage. For each reference voltage amplitude smaller than the analog voltage input, the reference voltage generator added at that time will be held, and for each reference voltage pulse generator amplitude producing a reference sum larger than the analog voltage, the pulse generator added at that time will be dropped for the remainder of the bits in the word. Any of the 255 possible combinations can be found in just eight intervals of time.

The output gate in Figure 3 permits a "one" to appear in the output whenever there is no output signal from the comparison circuit, indicating that this binary weight is required; and it permits a "zero" to appear in the output whenever there is an output signal from the comparison circuit, indicating that this binary weight is not required to represent the analog voltage amplitude. In this way the binary number is formed serially at the output as each comparison is made.

To illustrate by an example, assume the analog voltage input is 3.55 volts. The first of eight clock pulses causes the sequencer to trigger reference voltage pulse generator S_8. This produces a reference voltage pulse of 2.56 volts. This voltage is less than the analog voltage therefore the control circuit is set up by the comparator to continue pulsing this reference voltage pulse generator for the remaining seven clock pulses in the word and a "one" is formed in the binary output. The next clock pulse produces a trigger from the sequencer output number 2 and at the same time the control circuit triggers S_8 to produce a total reference voltage pulse amplitude of 3.84 volts ($S_8 + S_7$). This is a larger voltage than the analog input therefore the control circuit is not set up to trigger this reference voltage generator on the remaining clock pulses and a "zero" is formed in the binary output. The next clock pulse produces a trigger from sequencer output number 3 and at the same time the control circuit triggers S_8 to produce a total reference voltage pulse of 3.20 volts ($S_8 + S_6$). This is a smaller voltage than the analog input, therefore the control circuit is set up to hold this reference voltage generator for the remainder of the word and a "one" is formed in the binary output. If this procedure is followed for the remaining clock pulses it will be seen that the binary number 10110001 will be formed. This adds to a total of 3.54 volts or 0.01 volts less than the actual analog input voltage. The accuracy can be no better than +0.02 volts, the minimum voltage increment. This means that any binary number may represent an actual analog input voltage between the represented binary voltage number and a value just under the represented binary number plus 0.02 volts.

MEMORY ELEMENT CONTROL CIRCUIT

Figure 4 illustrates a familiar type of gating operation, using a bistable "flip-flop" and gate combination. This d-c gate controls the flow of a signal input, allowing it to be passed or blocked, depending on the state of the flip-flop. The state of the flip flop is controlled by the set, reset and toggle inputs. The flip flop is a memory element in this scheme which may or may not allow the

signal to appear on the output and continues to "remember" one way or the other, until commanded to change.

When duty-cycle requirements are low (as in this design), an analogous pulse-type memory element is a more efficient gating control. Figure 5 shows such an analogous pulse-type memory element gate arrangement (Page 149 of Reference 2). A nonlinear-core transformer, shown by the circle, is combined with a linear-core transformer in a one-shot blocking oscillator (BO) circuit, shown by the square marked BO. The three inputs to the nonlinear transformer are defined as: read, enable, and disable. In Figure 4 these terms are analogous to signal in, reset and set, respectively. If the nonlinear transformer has been previously enabled, an output pulse will occur for each read pulse. If the nonlinear transformer has been previously disabled, there will be no output for each read pulse. The BO acts as a delay element and places the nonlinear transformer in the proper state so that, if an output does occur, the next read pulse will produce an output.

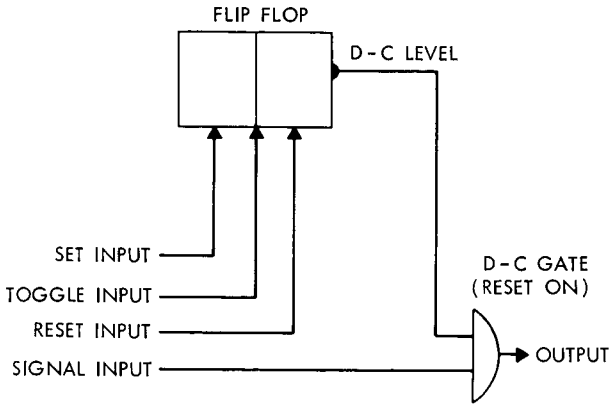


Figure 4—DC flip-flop and gate.

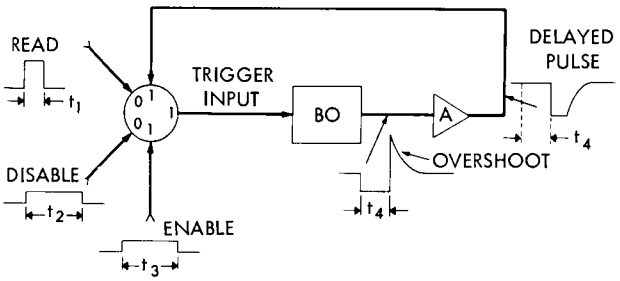


Figure 5—Memory element.

There are four pulse widths to consider when using this circuit; t1, t2, t3 and t4 in Figure 5. Pulse width t1 should be equal to or less than pulse width t4. This is necessary because at the end of the time t4 the core will be switched to the "1" state by the overshoot from the BO. If there is a continuing read pulse during the overshoot interval the core may not be switched into the "1" state, as desired, because of the two simultaneous inputs of opposite sign.

The read pulse was arranged to switch the nonlinear core in 0.5 microseconds. This switching time was used to obtain a large voltage per turn and at the same time not produce a trigger pulse too narrow to affect good triggering of the BO. More voltage could be obtained but for a smaller period of time. A commercially available nonlinear core was used in this application. This core has a maximum switching time of the order of 20 microseconds. If the disable pulse t2 is arranged to switch the core in 20 microseconds then the trigger voltage ratio between a read and a disable input will be 20/0.5 or 40:1. This means that the number of turns required to produce a peak voltage trigger pulse of 5 volts, 0.5 microseconds, during the read input will produce only a 5/40th volt, 20 microsecond pulse during the disable input interval. This is far below the minimum trigger voltage required to trigger the BO.

There is an additional trigger pulse, occurring during the read pulse interval, that must be considered. This is the noise voltage pulse produced when the nonlinear core has not been

enabled and a read pulse is applied. This pulse causes the noise flux of the core to be switched. If sufficient excitation is applied to switch the full flux in the core in 0.5 microsecond, then this same excitation produces a 0.05 microsecond pulse when the noise flux is being switched. The amplitude of this pulse is 0.23v/turn in the circuit used in this converter. This voltage must be kept below the BO trigger voltage threshold. Tests on the 2N861 transistor in the BO circuit indicate that a 0.05 microsecond pulse has to have a magnitude of 4.2 volts to trigger the BO. A 6-turn trigger voltage winding produces a noise voltage of 1.38 volts peak, which is 1/3rd the BO trigger threshold.

The enable pulse width, t3 may have any width sufficient to switch the core. The enable pulse may be applied to the input of the amplifier A (Figure 5) instead of to a separate winding on the core. Also a single amplifier may be used to enable, read or disable a number of cores simultaneously.

Figure 6 shows one application of memory element circuits. This is a toggle-input core flip-flop made up of two memory elements with the BO overshoot outputs of each unit cross-coupled to the other unit. This flip-flop was used to obtain two-phase pulses for driving alternate shift lines of the sequencer. In this circuit the disable and enable inputs are in series, allowing a single pulse to control both elements simultaneously. In this connection, unlike that of the single memory element, he enable-disable pulse may switch the cores at any speed. There is no requirement to switch slowly. This may be explained as follows. The enable-disable input of Figure 6 disables core number 1 and enables core number 2. If core number 1 triggers BO 1 the output from A1 will enable core number 2, which is in the same direction as the enable input. If core number 2 switches the trigger pulse to BO 2 is of the wrong polarity to trigger this BO. This shows that there are no spurious conditions in the circuit that will result in the wrong core being enabled or disabled because of a BO being triggered on a disable input.

REFERENCE VOLTAGE PULSE GENERATOR

A circuit diagram of a reference voltage pulse generator is shown in Figure 7. This circuit is the same as the BO circuit shown in Figure 8 except that a nonlinear core is used and a reset is provided. Eight of these pulse generators are required for an eight-bit converter.

A resistance pad was used to adjust the amplitude of the binary-weighted voltage pulse on the output of each generator. This method of adjustment was used because there is a limit to the amount of voltage step-down that can be achieved without seriously degrading the pulse waveform. The turns ratio on all of the pulse

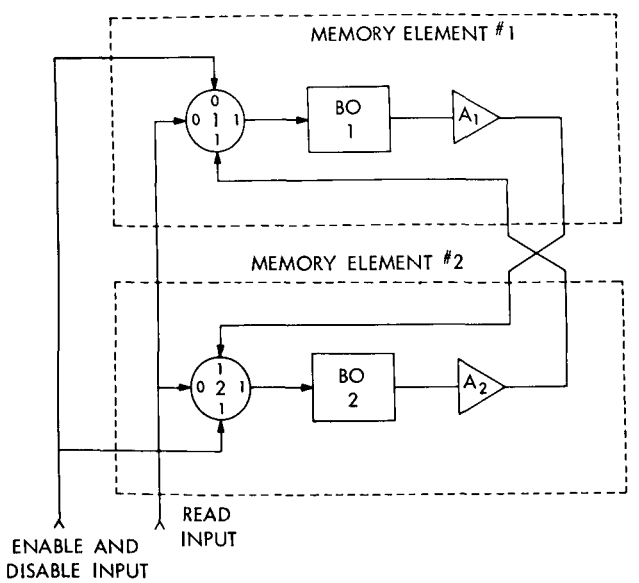


Figure 6—Core flip-flop.

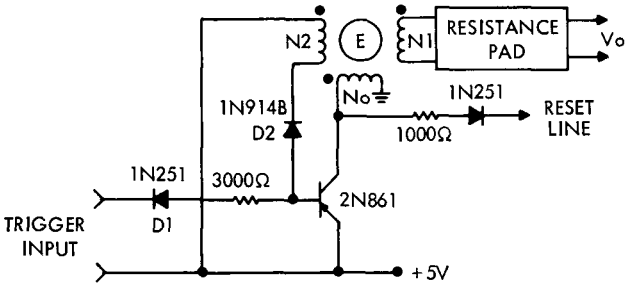


Figure 7—Reference voltage pulse generator.

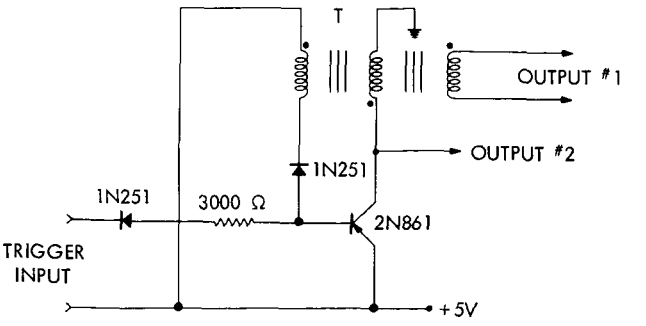
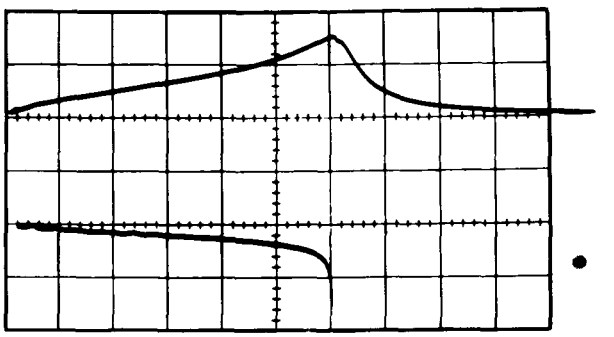


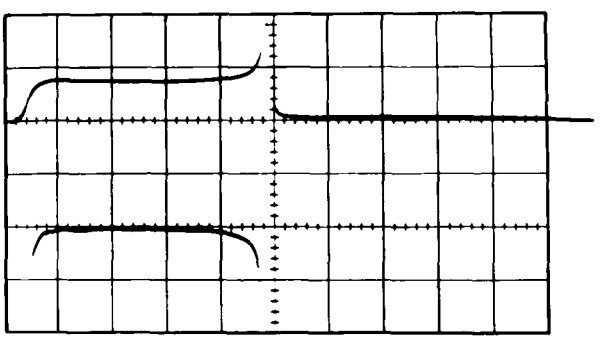
Figure 8—Blocking oscillator.

generators of binary weight 2^5 or less was limited to 0.33.

There are two major reasons for using a nonlinear core in this generator instead of a linear core; (a) smaller capacity coupling between the output and primary winding, and (b) better waveform. The windings on a nonlinear core may be segment-wound and still produce an acceptable waveform. This is not true for a linear core transformer, in which the windings must be distributed one over the other in order to obtain an acceptable waveform. Where capacity is not a problem, the use of a linear core will allow a less complex circuit. Figure 9 shows the difference between the voltage output waveform obtained with the two cores. This difference is caused by a continually changing collector current over the width of the pulse with the linear core and a substantially constant collector current with the nonlinear core. This causes a change in the transistor V_{ce} saturation voltage over the width of the pulse in the linear core and results in a droop in the output pulse, while the V_{ce} saturation voltage remains essentially constant over the width of the pulse in the nonlinear core and results in a relatively constant voltage amplitude across the top of the pulse.



LINEAR CORE WAVEFORMS. TOP TRACE IS COLLECTOR CURRENT, 20 ma./cm. BOTTOM TRACE IS COLLECTOR VOLTAGE, 0.5 VOLT/CM. HORIZONTAL RATE, 1 μsec/cm.



NONLINEAR CORE WAVEFORMS. TOP TRACE IS COLLECTOR CURRENT, 50 ma./cm. BOTTOM TRACE IS COLLECTOR VOLTAGE, 0.5 VOLT/cm. HORIZONTAL RATE, 0.5 μsec/cm.

Figure 9—Nonlinear-core and linear-core blocking oscillator waveforms.

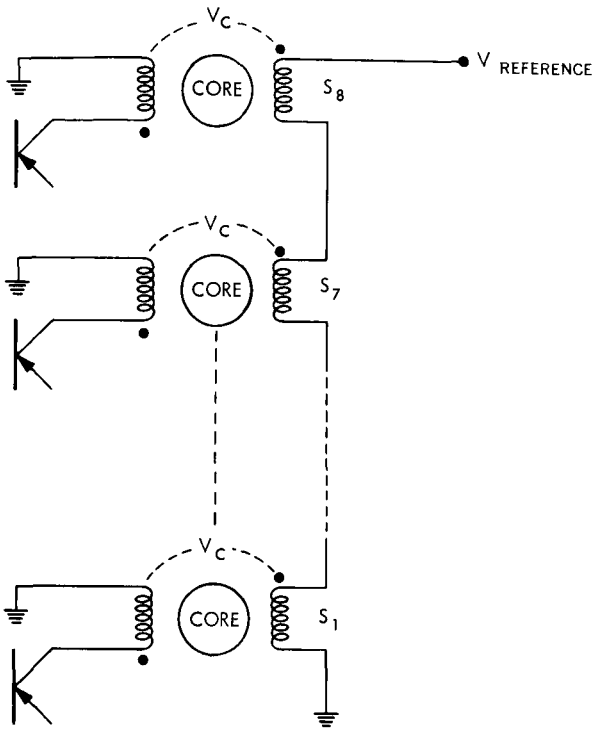


Figure 10—Summing method for reference voltage generators.

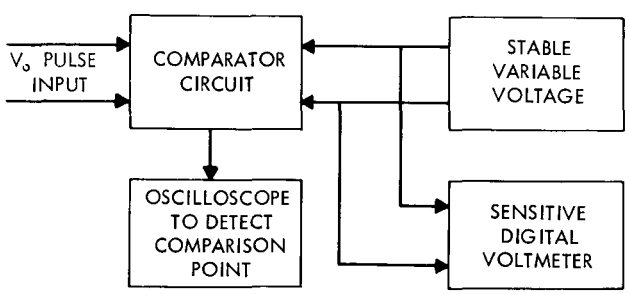


Figure 11—Test setup for measuring V_0.

Figure 10 illustrates the method in which the reference voltage pulses are summed. Any stray capacitive coupling between the primary and secondary winding is not desirable because all of the voltage pulse sources are connected in series. This shunt voltage from capacitive coupling at each source will provide a spurious pulse at the output of the series-connected windings that will cause the desired inductively-coupled pulse to be modified. This spurious pulse was reduced to a negligible value by using a nonlinear core and segmenting the output windings. The only source not affected by this coupling is S_1, because it is at ground potential and is unaffected by shunt capacity; therefore a linear core is used in this source.

The peak pulse voltage output (V_0) was measured in the setup shown in Figure 11. It was possible to measure the amplitude of the 5 volt pulse to an accuracy of ±1 millivolt with this setup.

The number of turns on the feedback winding (N_2) and the type of feedback diode (D_2) were chosen to minimize the change in V_0 with temperature. The total resistance (R_{DB}) of a series-connected diode and base-to-emitter transistor junction may have a positive, zero, or negative slope as a function of temperature, depending on the magnitude of the applied voltage This suggests that there should be an optimum number of turns for N_2, for a given diode and transistor, that will allow the change in R_{DB} to compensate for the temperature changes of the transistor collector-to-emitter saturation resistance and the effective resistance of the core. An optimum number of turns in N_2 was found by experiment and resulted in a maximum change in V_0 of less than 0.2% over the temperature range of -20°C to +60°C.

COMPARISON CIRCUIT

Figure 12 is a circuit diagram of the comparison circuit (Reference 4). This circuit uses two dual N-P-N silicon transistors. Transistors A1 and A4 are in one package; transistors A2 and

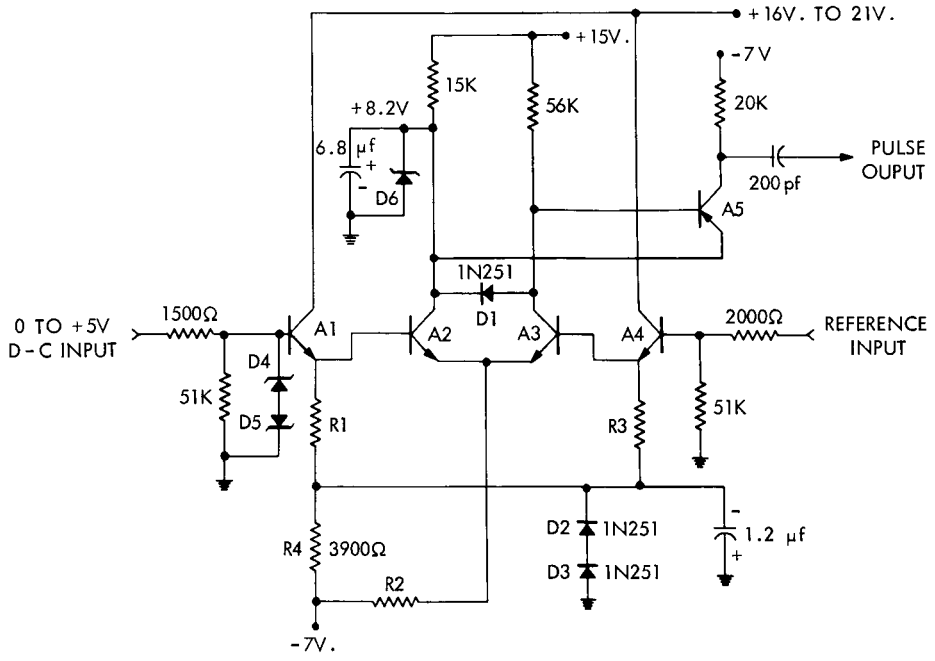


Figure 12—Comparison circuit.

A3 are in another. The type used here is the 2N2642, which has individual characteristics similar to the 2N930. The triode matching characteristics include a forward d-c current gain balance of a minimum of 0.9, a minimum base-to-emitter-voltage differential of 5 millivolts and a base-to-emitter-voltage differential temperature gradient of 10 microvolts/°C. These characteristics are acceptable provided the voltage differential of 5 millivolts and the gain ratio can be balanced out by the circuit.

The circuit operates in the following way. The input to transistor A1 is biased sufficiently positive to insure that transistor A2 is conducting and transistor A3 is cut off. Diode D1 is biased in the forward direction by the current supplied by the +15 volt supply through the 56 kilohm resistor to the collector of transistor A2, which is at a potential of +8.2 volts. The resulting voltage drop across this diode produces a reverse-bias voltage across the base-to-emitter junction of transistor amplifier A5.

Transistor A3 will remain cut off as long as the base-to-emitter voltage is either below the threshold voltage of this junction or is reverse biased by transistor A2. The d-c voltage appearing on the emitter of transistor A3 is a function of the 0 to 5 volt input voltage. If a positive voltage pulse, with an amplitude sufficient to forward-bias A3, is applied to the reference input, A3 will begin to conduct. This will begin to bring diode D1 out of conduction. If the reference input pulse has sufficient amplitude and width the collector of A3 will eventually become more negative than +8.2 volts and A5 will be switched on. The resulting output pulse is further amplified and used to trigger a BO. There is sufficient gain in the system so that a change of less than 1 mv on the d-c input, at a threshold level, will cause the BO to trigger or not trigger. In other words the threshold error is less than 1 mv.

The electrometer output voltage, during range switching and voltage turn-on periods, can approach -15 volts. Also during periods of saturation the output voltage can approach +15 volts. Zener diodes D4 and D5 were placed across the input so that these large positive or negative voltages cannot appear on the base of A1.

Diodes D2 and D3 are biased in the forward direction to provide a voltage to bias "on" transistors A1 and A4. This bias is necessary to eliminate the base-to-emitter junction threshold voltage. This diode voltage also varies with temperature in such a way as to compensate for the changes in the transistor base-to-emitter threshold.

The values of resistors R1, R2, and R3 are adjusted to eliminate the unbalance in the circuit and to set the threshold voltage to zero.

SEQUENCER CIRCUIT

The sequencer and delayed sequencer are shown symbolically in Figure 13 (Pages 115-146 of Reference 3). The sequencer is similar to a ring counter in which a single one is transferred from core to core in response to the 400 cps clock pulses. The sequencer was designed so that up to two cores can be switched by the output of each core. When each core reads out it switches the next core in the sequencer, transferring the one, and at the same time a core is switched in the delayed sequencer. That particular core in the delayed sequencer then produces an output pulse after a time delay. This is a simple way of obtaining delayed pulses, a_7' through a_1', with only a single BO delay.

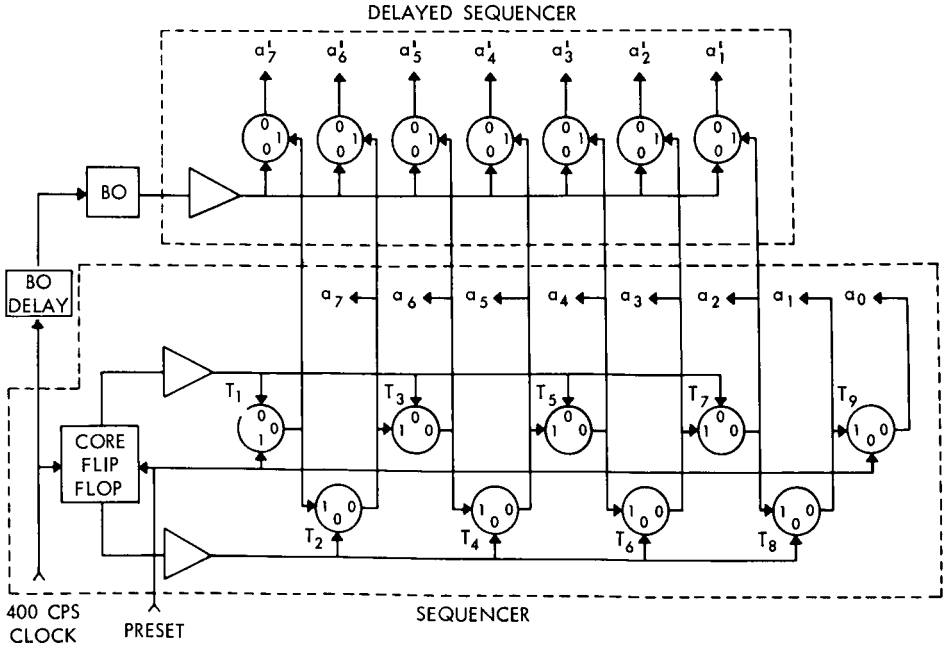


Figure 13—Sequencer and delayed sequencer.

The output of each stage of the sequencer is used to trigger each reference voltage pulse generator. A negative pulse is required for this trigger and is obtained from the output of core T2, in the case of the trigger for S_8, at the time the one is transferred from T1 to T2. A ninth core was added to obtain a total of eight sequential pulses to trigger the eight reference pulse generators. This is required because a one is placed in T1 during preset and T1 does not produce a negative pulse on the first clock pulse of the word. The ninth core is preset at the same time as T1.

The delayed sequencer pulses are required to set up the control circuit elements. The delay allows each sequencer output to trigger a reference voltage generator and to permit the comparison circuit to produce a pulse. The delayed sequencer output pulse sets up the control to hold this reference voltage generator in the active mode. If a pulse appears on the output of the comparator, the delayed sequencer pulse is prevented from enabling the control circuit; and if a pulse does not appear from the comparator, the control circuit is enabled to allow this reference voltage generator to be triggered on the remaining clock pulses.

The preset pulse for the sequencer is applied at the time of the leading edge of the word gate pulse, so that at the time of the first clock pulse, the sequencer is set up to transfer the one in core T1 to core T2; and on the eighth pulse core T9 is set up to produce an output.

BLOCK DIAGRAM DESCRIPTION

Figure 14 is a complete block diagram of the converter and Figure 15 is a timing diagram showing only the pertinent waveforms required in the conversion process.

The word gate input signal is applied to emitter follower EF-1 and amplifier A-21. Emitter follower EF-1 provides a high impedance load to the gate signal. Amplifier A-21 is provided with a source of collector load resistance voltage by the word gate signal during the word gate interval. The circuit was arranged this way so that no matter what kind of failure may occur with the converter there will be no output except during the gating interval. This was felt to be necessary because this converter shares the outputs of other experiments tied to this same point. Any malfunction within the converter could take out all of the experiments. Four diodes, wired in series—parallel, are placed in series with the output signal so that a short to ground will not short out the output signal of all of the other experiments.

The word gate input signal may have a maximum rise time of 50 microseconds. Amplifiers A-1, A-2, and A-3 are used to improve this rise time and invert the signal so that a negative trigger may be applied to BO-1 at the leading edge of the word gate pulse. The output of BO-1 drives A-5 which presets the core flip-flop and sequencer. The overshoot from BO-1 triggers BO-2. Blocking oscillator BO-2 drives A-8 to provide a pulse to disable all of the memory elements, clearing out the information that remained in the memory elements from the preceding conversion.

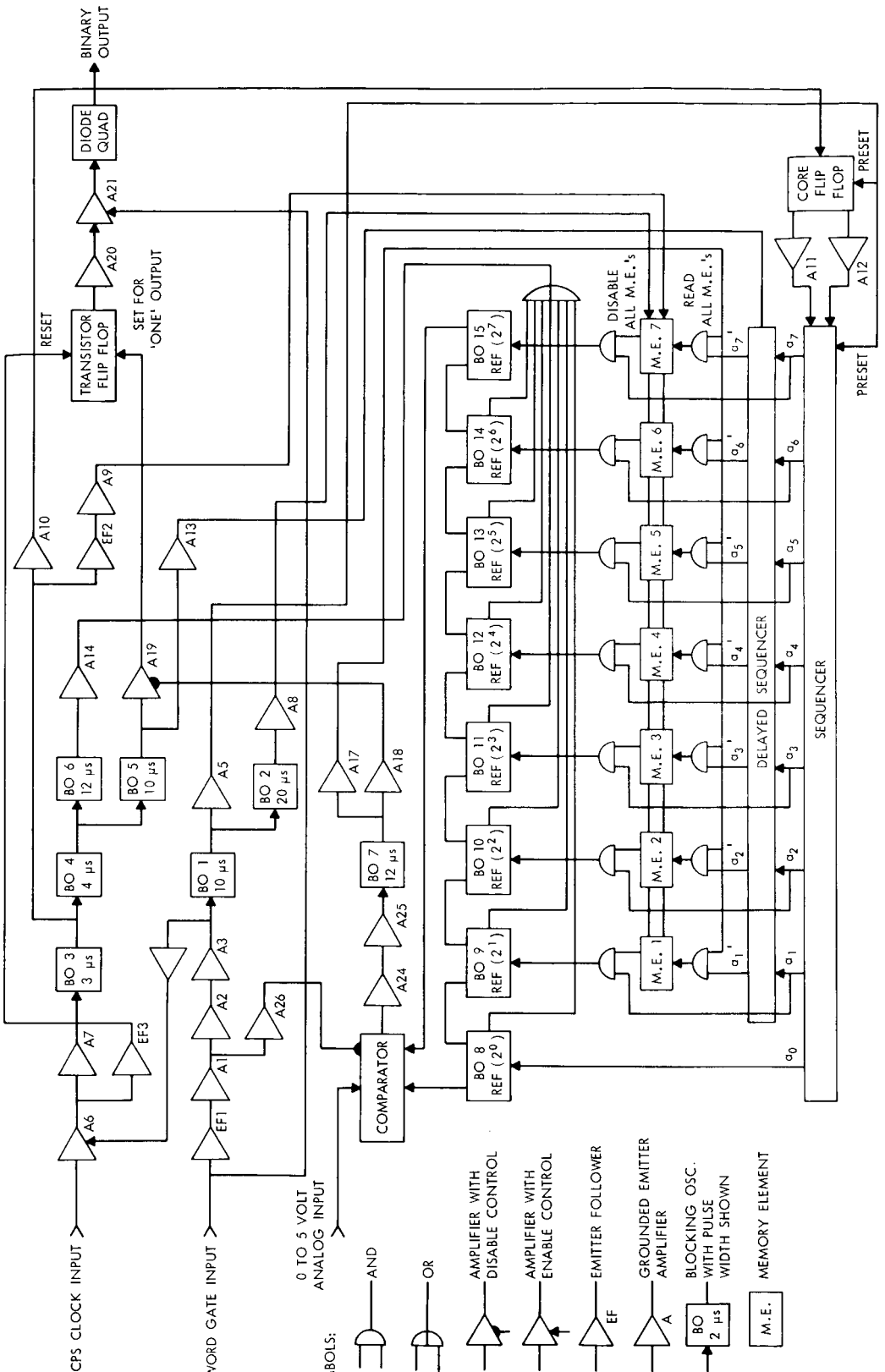


Figure 14—Block diagram of 8-bit analog-to-digital converter.

The 400 cps clock input signal is applied to a high input impedance amplifier, A-6. This amplifier is gated on only during the 20 millisecond word gate pulse interval, so that there will be just 8 clock pulses appearing on the output of A-6 during each gating interval. Amplifier A-6 inverts the clock signal and, on each positive-going swing of the input signal, provides a reset pulse to the transistor flip flop through emitter follower EF-3. This forces the binary output to be in the "zero" state in preparation for the next binary bit to be formed on the negative half cycle of the 400 cps clock input signal.

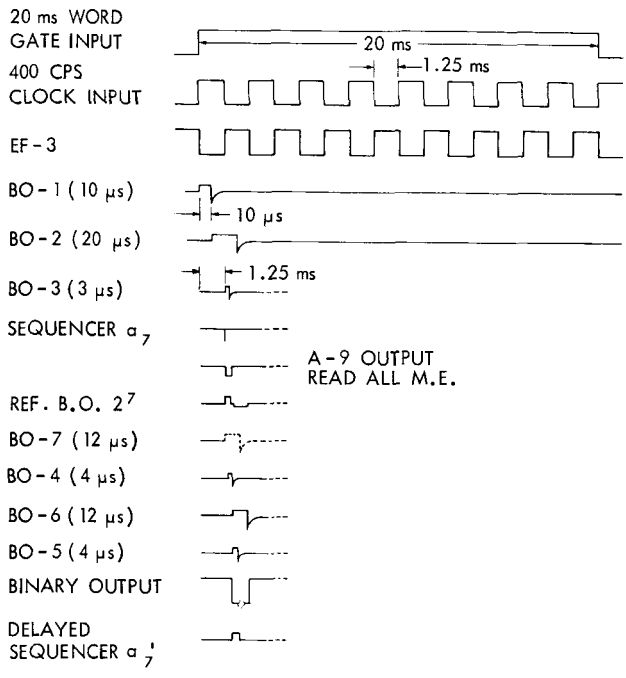


Figure 15—Timing diagram.

The rise and fall time of the clock input may have a maximum value of 5 microseconds. Amplifiers A-6 and A-7 improve this rise and fall time and present a negative trigger pulse to BO-3 at each negative-going half cycle of the clock input signal. This pulse is used to drive A-10, for switching the core flip flop, and A-9, for reading all of the memory elements simultaneously. In the case of the first binary bit, 2^7, there will be no output from any of the memory elements and sequencer output a_7 will trigger reference BO, 2^7. Output a_7 also switches the first core in the delayed sequencer. If we assume the 0 to 5 volts analog input is larger than the 2^7 reference voltage, BO-7 will not be triggered.

The overshoot of BO-3 triggers BO-4. Blocking oscillator BO-4 provides a 4 microsecond delay to give time for the reference BO to apply a pulse to the comparator and for BO-7 to be triggered. The overshoot of BO-4 triggers BO-6 and BO-5. Blocking oscillator BO-5 applies a signal to A-19. In this case, since BO-7 was not triggered, an output will appear on A-19 and the transistor flip flop will cause a "one" to be formed in the binary output. If BO-7 had been triggered A-18 would inhibit A-19 so that there would be no trigger to the flip-flop and a "zero" would be formed in the binary output.

BO-5 also drives A-13. Amplifier A-13 provides a pulse to the delayed sequencer. This pulse causes the first core in the delayed sequencer, previously switched by sequencer output a_7, to provide an output a_7' which in turn is applied to a gate. This gate is controlled by BO-7 and, since BO-7 did not trigger in this case, pulse a_7' enables memory element number 7 so that on subsequent read pulses from A-9, reference BO-7 will continue to be triggered. If BO-7 had been triggered, output a_7' would have been blocked and memory element number 7 would not have been enabled.

Blocking oscillator BO-6, triggered by BO-4, drives A-14. The output of A-14 provides a pulse to reset all of the reference BO's. In this case only reference BO-15 (2^7) will reset; however, the circuit is arranged so that one or all of the reference BO's will be reset if required.

This explains the sequence of operation for the first bit. The remaining 7 bits are formed in exactly the same way; the only difference is that the sequencer output transfers to the next output each time.

Amplifier A-26 blocks the comparator during the interval between word gate pulses. This was necessary since output of the electrometer went negative because of an interface reaction between the electrometer amplifier and the comparator. This reaction occurred only on the most sensitive range with no signal input, and caused a relaxation-type oscillation to be set up that was not corrected until the electrometer output signal was increased to +0.3 volts. This reaction occurred at some time after the binary conversion, therefore by blocking the comparator between word gate pulses it was possible to eliminate the instability and to measure down to the d-c off-set of the electrometer.

SPECIFICATIONS

Mechanical

a) Size: 4-1/2 × 3 × 1 inches excluding connector and mounting flanges (see Figure 1).

b) Weight: 400 grams.

c) Fully encapsulated with commercially available epoxy adhesive.

d) Vibration: 15G, 5 to 2000 cps.

Electrical

a) Analog input voltage: 0 to +5.1 volts d-c.

b) Analog input resistance:

1) 45.5 kilohms at -20°C. and +.04 volt analog input.

2) 52.5 kilohms at +60°C. and +5 volt analog input.

c) Temperature: -20°C to +60°C.

d) Power supply voltages:

1) +16.2 to +21 volts d-c at 2.6 ma. (current measured at 18.5v).

2) -7.000 ±0.1% volts d-c at 1.8 ma.

3) +5.000 ±0.1% volts d-c at 1.1 ma.

e) Power input: Approximately 70 milliwatts total. The converter by itself, including the flip-flop but without amplifiers, requires 20 milliwatts. The pulse logic circuit by itself requires 0.37 milliwatts.

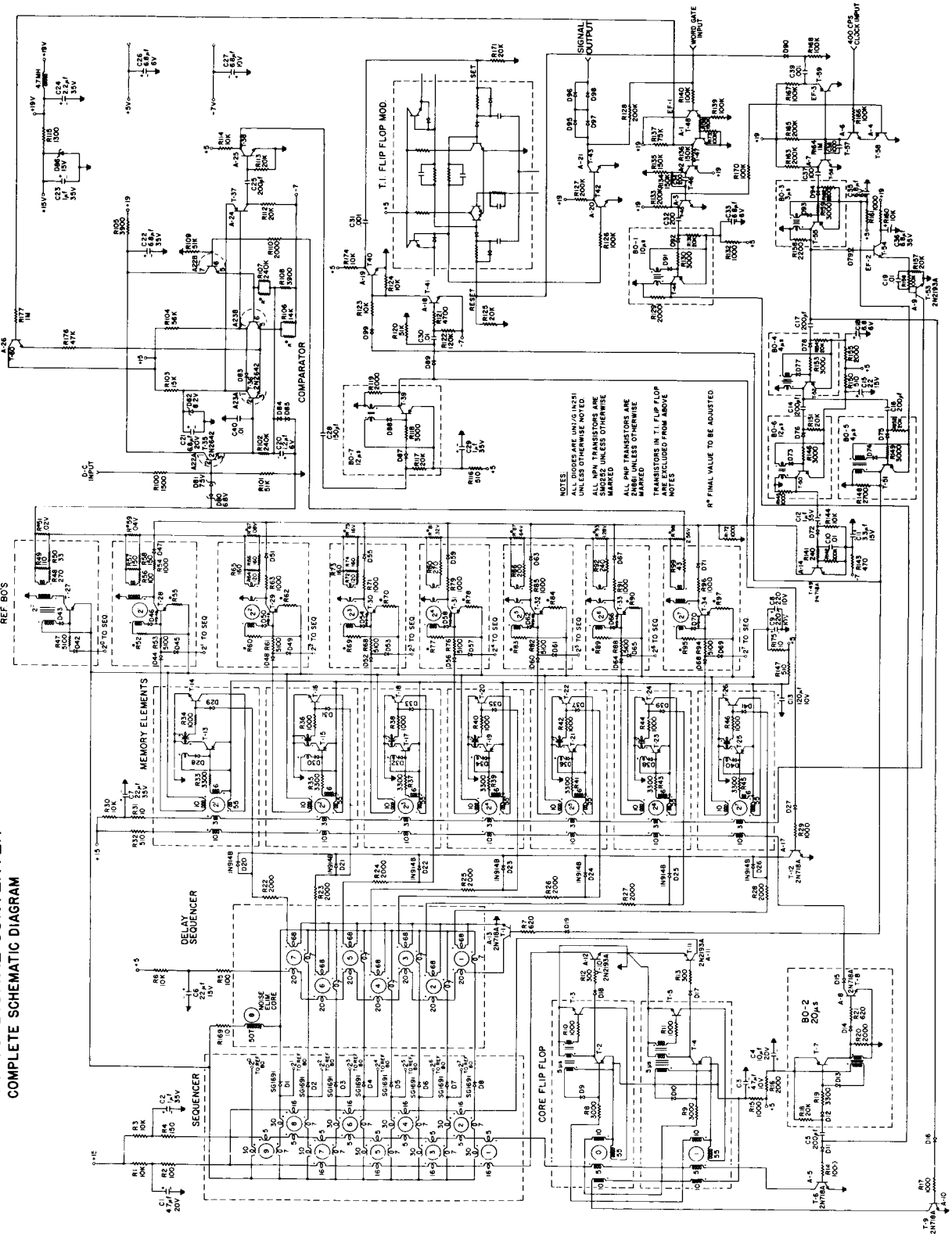


Figure 16—Complete schematic diagram.

f) Accuracy: ±0.5% full scale over the temperature range of -20°C. to +60°C.

g) Binary output: Serial with the most significant bit first. Binary "one" is zero volts and binary "zero" is +16 volts.

h) Binary output impedance: 200 kilohms.

i) Clock input requirements: 0 to +5 volts, 400 cps, square wave with maximum rise and fall time of 5 microseconds. Positive-going half cycle must coincide with the beginning of the word gate.

j) Word gate input requirements: 0 to +16 volts, 20 milliseconds long with a maximum rise time of 50 microseconds. Must be positive during the gating interval.

k) Word rate: Approximately 1.5 per second.

l) Clock input resistance: 100K ohm.

m) Word gate input resistance: 70 kilohms.

CIRCUIT DIAGRAM

The complete circuit diagram is shown in Figure 16. Each of the amplifiers and blocking oscillators are labeled the same as in the block diagram. All of the circuits not already described are straightforward, therefore no detailed circuit description will be made.

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