JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CALIFORNIA

DIGITAL LOGIC FAMILY STUDY

August 1964

Final Report

Document # 64-SD-4331

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Jet Propulsion Laboratory
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Pasadena, California

GENERAL ELECTRIC
SPACECRAFT DEPARTMENT
A Department of the Missile and Space Division
Valley Forge Space Technology Center
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FORWARD

Presented in this report is the work that was completed by the General Electric Company for the six week period beginning June 8, 1964 in accordance with JPL Order # 950930, Req. No. 028-814 of June 22, 1964.

The contract was essentially for the study and design of a digital logic family using a computer.

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INTRODUCTION

This report details the analytical design and testing of a Flip-Flop and Nand gate suitable for use in many spacecraft electronic subsystems. The analysis is shown for a 500 K.C. and 50 K.C. Flip-Flop and a Nand gate. Particular emphasis has been placed on using reliable parts, assuring operation under all worst case assumptions and conditions, and in minimizing the power dissipation of the circuits. The report contains the electrical specifications of the circuits under the environmental and power supply voltage variations they can tolerate, and the logical rules to be applied when using them. Piece part characteristics and tolerances are shown and when critical to circuit operation are specially specified, if not covered in the standard piece part specification. A digital computer (Autonetics - Recomp II) was used in the D.C. analysis to determine, fan-out, input and output currents and critical bias voltages in the circuits. The complete computer analyses, along with descriptions, have been included. A transient analysis using charge techniques has been used to determine circuit delay, rise and fall times. To prove the validity of the analytical D.C. and transient approaches taken in the circuit design, measurements have been made under given operating conditions. The measurement data is compared against the computed values, with a general good agreement existing between data measured and values computed.

DESIGN EVOLUTION

The design evolution of the Flip-Flop and Nand circuits from the first configuration considered to the final design is discussed to give the possible circuit user a better understanding of the how and why of the circuit configurations and the part values used. It may also help the user avoid pitfalls that could occur by his removing or changing parts that might not seem critical.

The performance goals for these circuits were that they be able to operate at a 500K.C. repetition rate with the Nand requiring about 5 mw and the Flip-Flop 10 mw of power. Their operation was to be guaranteed over the temperature range of $-10^{o}C$ to $+80^{o}C$ and with input power supply voltage variations of up to $\pm 15\%$. The complexity of the circuits was to be kept to a minimum and only high reliability parts used throughout the designs to assure maximum reliability. On circuit fan out capability, it was at first specified that the Flip-Flop and Nand outputs should each be able to drive the inputs to 10 other Flip-Flops or Nands. It was found possible within the power limitations to drive 10 Nand inputs. However, when considering Flip-Flop inputs the A.C. triggering current required added to the input current so that only 4 Flip-Flops could be driven by a Nand or Flip-Flop. Rather than increase circuit power dissipation to drive more Flip-Flops, it was agreed that an ability to drive 4 Flip-Flop inputs was satisfactory. In addition to the Flip-Flop and Nand input

loads, the ability to drive stray line capacitance was a requirement. An average capacitance of 50 pf per foot with an average line length of 6 inches seemed a reasonable assumption. In the transient analysis the response versus load is shown graphically so that the response at any given D.C. and capacitive load can easily be determined.

The Nand configuration (Figure 1) initially considered, was the same as the final configuration used throughout the design. To keep the number of different types of parts used to a minimum, the first Nand circuit considered used diodes of one type throughout. The initial rough worst case calculation of the OFF bias on the base of the transistor of the Nand showed that under certain conditions when the transistor was supposed to be biased OFF, it would actually become biased ON. Rather than add a third diode which would reduce the efficiency and reliability, it was decided to investigate using different types of diodes. What was needed was a high conductance diode (D_3) to perform the input gating function and a low conductance diode for the series diodes D_1 and D_2. Of the diodes supplied by Fairchild to JPL, the FD643 was considered for the high conductance requirement and the FD306 as the low conductance diode. Using data supplied by Fairchild, a worst case analysis showed that if the diodes were specified at their operating points, the OFF condition

of the Nand transistor could be guaranteed under all electrical and environmental conditions. This being the case, the use of two types of diodes in the Nand was decided upon. Also early in the design of the Nand, the use of a 60,000 ohm resistor R_2 was considered in place of the 100,000 ohm resistor initially used. The lower value 60,000 ohms was considered since it would result in a larger forward voltage drop across the diodes D_1 and D_2 because of the larger bias current. This would result in an even safer worst case voltage existing on the base of Q_1, when Q_1 is to be in the OFF condition. However, in reducing to 60K, it was found that the required fan-out of 10 Nand loads could not be achieved.* R_2 was then given its original value of 100K and all final analyses in this report are based on the 100K value for R_2. With R_2 having a value of 100K, it has been found that in the worst case, the Nand can have a fan out of 10. Also, when the gate inputs are such as to require Q_1 to be in the OFF condition, Q_1 is guaranteed OFF under the worst operating conditions. In the initial design, R_1 of the Nand had a value of 5.6K ohms. In the computer D.C. analyses, it was found that larger values than 5.6K ohms could be used for R_1 and still meet the fan-out of 10 - requirement. A value of 6.2K ohms was chosen since it resulted in a lower power dissipation as well as adequate transient response of the Nand.

*with reasonable transistor current gains

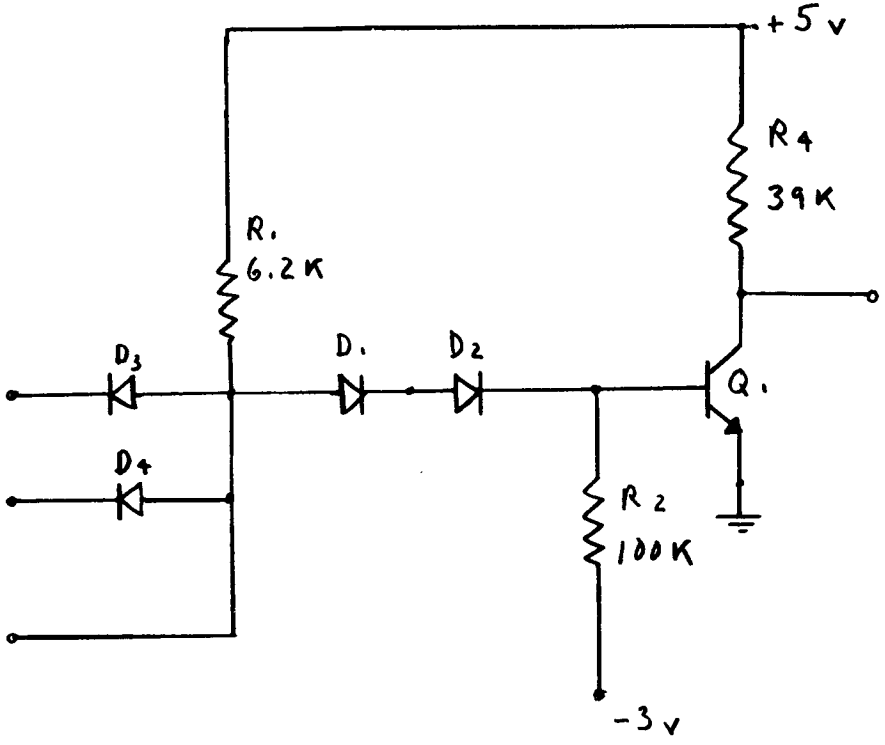


Fig. 1

Q_1 2N914

D_1, D_2 FD306

D_3, D_4 FD643

The initial Flip-Flop design considered was as shown in Figure 2. With the particular arrangement of R_5 and R_9 and considering when the side of the Flip-Flop containing Q_1 is on, there is a forward bias existing across diode D_3 under certain operating conditions. This is especially true for maximum load on Q_1. This means that a very small noise pulse appearing at the input could trigger the Flip-Flop, To avoid this, R_5 and R_9 were rearranged* to provide a voltage, called V_T in the analysis, which results in a back bias appearing across the input diode D_3. The early triggering analysis showed that under given conditions, the 47 micro-micro farad input capacitors were insufficient to guarantee triggering of the Flip-Flop by worst case input signals. The input capacitors were therefore raised to 75 micro-micro farads each, making triggering certain under all conditions. The enabling resistors R_5 and R_9, and R_6 and R_{10} along with the input resistors R_{11} and R_{12} were changed in value to result in 500KC repetition rate of the Flip-Flop with minimum possible dissipated power in these resistors. Referring to resistors R_{13} and R_{14}, it was at first decided to eliminate these resistors since they did not materially enhance the transient response of the internal Flip-Flop. This is true because the turn-off current that does the Flip-Flop switching is supplied through diodes D_3 or D_4. However, in the subsequent computer analyses, it was found that the OFF condition of Q_1 or of Q_4 could not be guaranteed under worst case conditions. Looking at the side of the Flip-Flop containing Q_3 and Q_4 as the OFF side,

*Figure 2-A - Final Flip-Flop Configuration

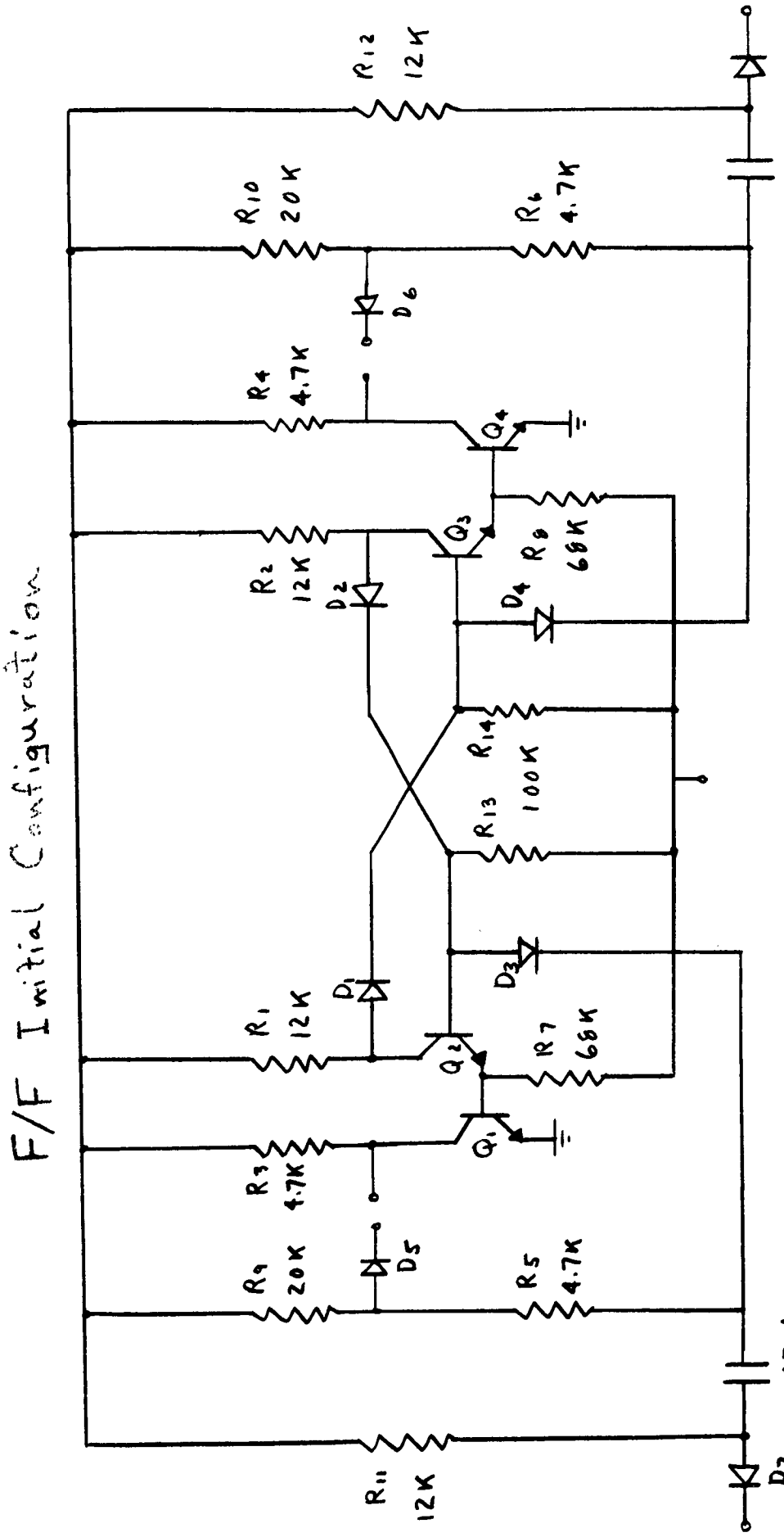

F/F Initial Configuration
R12 12K
R10 20K
R6 4.7K
D6
R4 4.7K
Q4
Q3
R2 12K
D2
R8 68K
D4
R14
R13 100K
D3
D1
R1 12K
Q2
R7 68K
Q1
R3 4.7K
D5
R9 20K
R5 4.7K
47pf
R11 12K
D7

Fig. 2

F/F Final Configuration

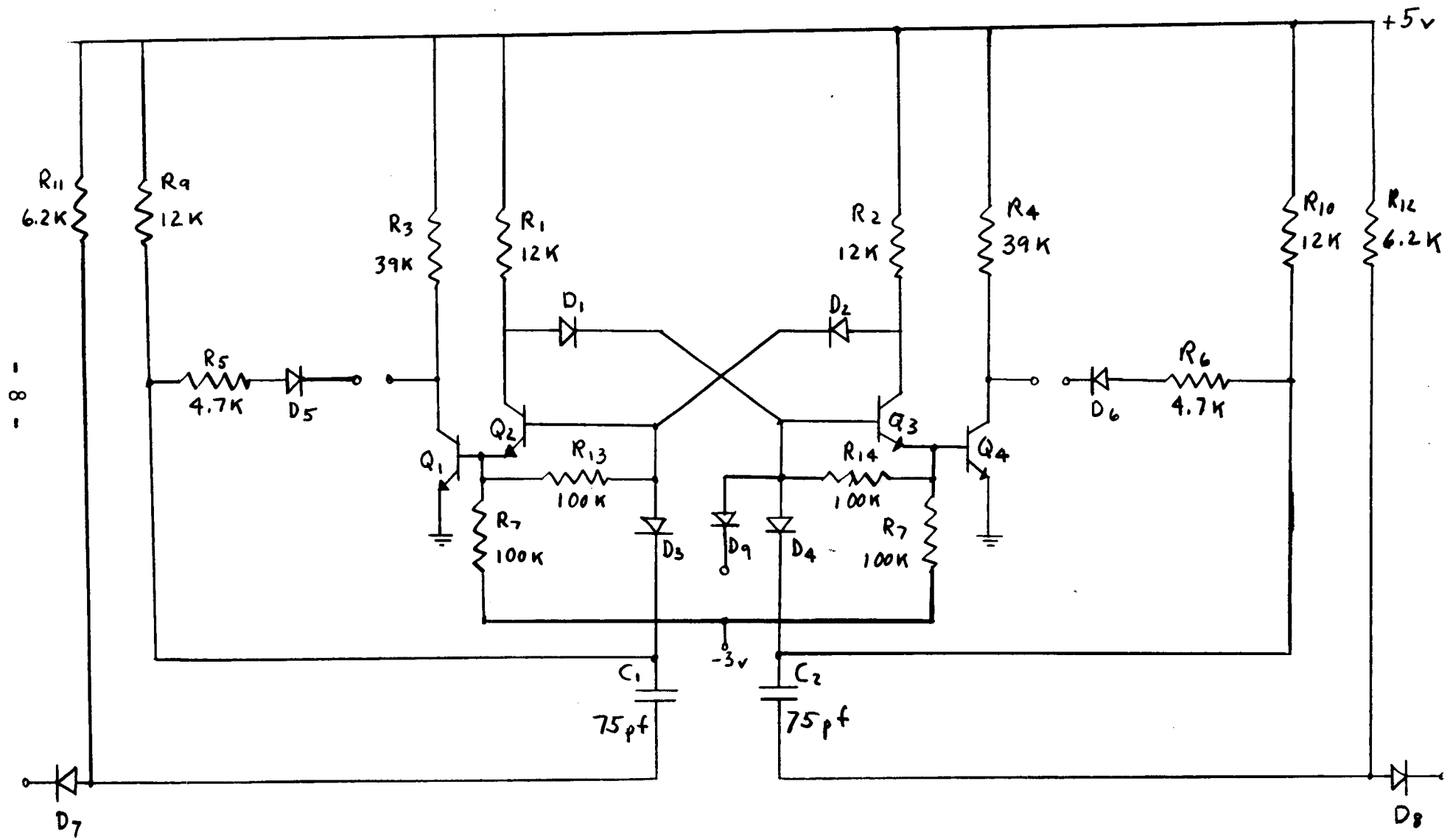


Fig. 2-A

Transistors 2N914
Diodes FD643

the OFF-base voltage on the base of Q_4 would be determined as follows. When Q_4 is in the OFF condition, Q_3 acts as an emitter follower because of the resistor tied to its emitter. This being the case, voltage at the emitter of Q_3 is determined by the sum of the base to emitter voltage of Q_1 plus the collector to emitter saturated voltage of Q_2 minus the forward diode drop of diode D_1 and minus the base to emitter drop of the emitter follower transistor Q_3. Under worst case operating conditions, that is, end of life and high temperature and assuming a very high current gain for transistor Q_3 even though its operating in the low collector current range i.e., $I_c \approx 30$ micro-amps, and assuming the maximum high temperature end of life leakage for diode D_4, it is possible for the leakage current through D_4 to supply all of the required base current for transistor Q_3. Under these conditions, the leakage current through D_4 into the base of the high beta transistor Q_3 causes the base and therefore, the emitter of Q_3 to rise in the positive direction. In the worst case, diode D_1 can actually become back biased and the emitter of Q_3 (also the base of Q_4) sets at a positive voltage significantly above that required to put Q_4 in an undesirable active region of operation. To circumvent this possibility, and to keep the circuit efficiency as high as possible, the possibility of adding a resistor from the base to emitter of Q_2 and one across the base emitter junction of Q_3 was investigated. A value higher than 100K ohms could have been used but since 100K ohms resistors are already used in the

circuit, this value was chosen. With 100K ohms, a forward bias is guaranteed through D_1 or D_2 even considering the maximum end of life leakage current through diode D_3 or D_4. The forward drop across diode D_1 or D_2 is of sufficient magnitude to result in a forward voltage on the base of Q_4 or Q_1 of less than + 0.3 volts. The approach is acceptable because from much past data on the base to emitter voltage of epitaxial transistors at the edge of conduction along with measured data taken on 2N914 transistors during this study period, the + 0.3 volts forward bias for non-conduction is conservative. Putting the 100K resistor across the base to emitter junction had another desirable advantage in that it did not decrease the efficiency of the circuit. By this is meant that the current through the 100K resistor is all delivered to the base of the buffer transistors for driving output load. If they were connected from the base of the in-board flip-flop transistor to V_b, it would result in the loss of about 40 micro-amps of drive current to the inputs of the buffer transistor Q_1 and Q_4. Multiplying this 40 micro-amps by the minimum beta of the outboard transistors of 25 results in a loss of load driving current of about 1 milliamp. Also for a given load that can be driven, triggering of the flip-flop would be more difficult, since for that given load if R_{13} and R_{14} were returned to $-V_b$, more internal current would need to be flowing through resistors R_1 and R_2. This results in more current

being needed to be pulled out during the triggering of the flip-flop which makes triggering more difficult. Although none of these reasons make it absolutely necessary to connect R_{13} and R_{14} as indicated, they do however make it more advantageous to do so. Before leaving this point, one other consideration that was contemplated was the possibility of specifying a maximum low current beta for the 2N914 transistor so that the base current into Q_3 or Q_2 would always exceed the leakage current of diode D_3 or D_4. This was decided against on the basis that if so specified, it would decrease the yield on the 2N914's that could be used, thereby increasing their price. There would also be the possibility of 2N914's somehow getting into modules that were not tested to this specification. The question of yield could become a very serious one, as the manufacturer's of planar epitaxial transistors improve their process to increase the beta hold-up at low collector currents.

All of the computer D.C. analyses and transient analyses were performed on the flip-flop with the final configurations shown in Figure 2A. The only exception to this is the first computer run on the flip-flop which was performed without resistors R_{13} and R_{14} in the circuit. This was used only to determine diode and transistor operating points for the final computer runs.

A. CIRCUIT SPECIFICATION

Power Supplies	+5v ±15%, -3v ±15% or +5v ± 5%, -3v ±5%
Temperature	-10°C to +80°C

Nand	15% P.S.	5% P.S.
Input:		
Zero Level	0.1v to 0.3v	0.1v to 0.3v
One level	2.5v to > 5.75v*	2.5v to > 5.75v*
Current (I_{in})	482 μa to 896 μa	562 μa to 809 μa
Output:		
Zero Level	0.1v to 0.3v	0.1v to 0.3v
One level	4.25v to 5.75v	4.75v to 5.25v
t_r, t_{dr}, t_{od}, t_f, t_s	Function of loading	see curves
Current	Sink for I"o" < 6.3ma	I"o" < 8.2ma
Repetition Rate	500 KC	500 KC
Power		
Zero state	1.38mw to 4.29mw	1.92mw to 3.46mw
One state	2.25mw to 5.24mw	2.88mw to 4.33mw

Flip-Flop (500KC)		
Input:		
Zero level	0.1v to 0.3v	0.1v to 0.3v
One level	4.25v to 5.75v	4.75v to 5.25v
Current	482 μa to 896 μa DC	562 μa to 809 μa DC
Pulse width	2 μ sec. (when conditioning) 1 μ sec. (when used as toggle)	

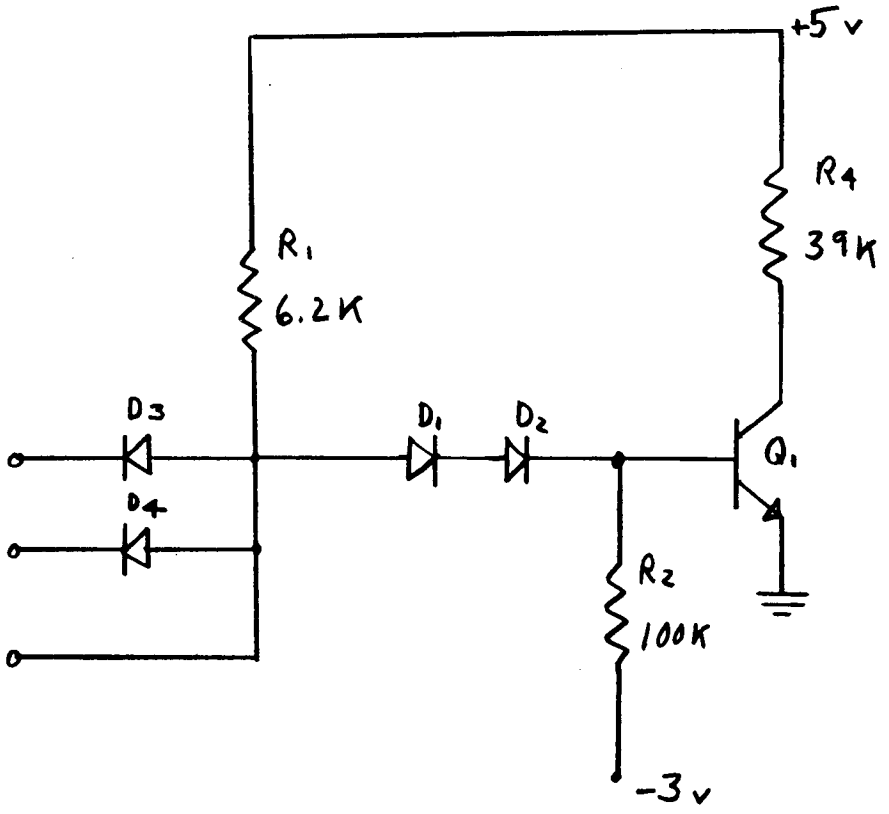
*Upper value limited by input diode breakdown voltage

	15% P.S.	5% P.S.
Repetition Rate	500 KC	500 KC
Noise Immunity	> 0.5v	> 0.5v
Triggering	4.25v at tr 275 nscc (worst case)	
Output:		
Zero Level	0.1v to 0.3v	0.1v to 0.3v
One level	4.25v to 5.75v	4.75v to 5.25v
Current	Sink for I"o" < 6,8ma	I"o" < 8.7 ma.
t_r, t_s, t_f, t_d	see curves	see curves
Power	5.3mw to 12.8mw	6.8mw to 10.6mw

Flip-Flop (65 KC)

Input:		
Zero level	0.1v to 0.3v	0.1v to 0.3v
One level	4.25v to 5.75v	4.75v to 5.25v
Current	77 μa to 141 μa	90 μa to 129 μa
Pulse width	75 μsec.	75 μsec.
Repetition Rate	65 KC	65 KC
Noise Immunity	> 0.5v	> 0.5v
Triggering	4.25v at tr 275 nscc (worst case)	
Output:		
Zero level	0.1v to 0.3v	0.1v to 0.3v
One level	4.25v to 5.75v	4,75v to 5.25v
Current	Sink for 7,0 ma.	I"o" < 8.9ma
t_r, t_s, t_f, t_d	see 500KC curves	see 500KC curves
Power	2,7mw to 6.9mw	3.6mw to 5.7mw

Nand Final Configuration



Q_1	2N914
D_1, D_2	FD 306
D_3, D_4	FD 643

Logical Rules:

Nand Inputs:

a. Up to 9 diode inputs

Nand Drives:

a. 10 Nands

b. 4 F/F (500KC)

c. 20 F/F conditioning inputs (500KC)

d. 10 F/F (50KC)

e. 40 F/F conditioning inputs (50KC)

F/F Drives:

a. 10 Nands

b. 4 F/F (500KC)

c. 20 F/F conditioning inputs (500KC)

d. 10 F/F (50KC)

e. 40 F/F conditioning inputs (50KC)

PARTS LIST

Resistor: JPL hi-reliability part for IRC - CCM, or better.

±4% tolerance, end of life, temperature and initial value

Diode: JPL hi-reliability part for Fairchild diodes.

Additional Specification:

FD306 - specified voltage drop @ 25°C of 0.525v ±50mv at 30 μa; T.C. 2.5mv/°C ±0.2mv/°C from -10°C to +80°C.

FD643 - specified voltage drop @ 25°C of 0.550v ±50mv at 600 μa; T.C. 2.375mv/°C ±0.3mv/°C from -10°C to +80°C.

specified voltage drop of $>$ 0.15v @ I_F = 4 μa, T = 80°C.*

Transistor: JPL hi-reliability part for the 2N914.

Additional Specification:

Specified h_{FE} of greater than 25, end of life at operating current of 6ma and -10°C.

$V_{be} > 0.410v$ @ I_c = 20 μa., T = 80°C.*

$V_{be} < 0.690v$ @ I_c = 6 ma., T = 80°C.*

$V_{ce} < 0.2v$ @ I_c = 0.4 ma., I_b = 0.12ma., T = 80°C.*

Capacitor: JPL hi-reliability part for Corning glass capacitors CY series.

±5% tolerance for temperature, end of life, and initial value.

* See Appendix D, Table VI for explanation.

B. NAND

The Nand configuration is given in Figure 1, Diodes D_1 and D_2 (FD306) were chosen to be of the low conductance type and diodes D_3, D_4 (FD643) were chosen to be high conductance types. This guarantees Q_1 (2N914) is reversed biased when the input is low. The transistor Q_1 was chosen from the JPL high reliability parts list. Resistors R_1 and R_2 were determined based on Fan-out/Fan-in ratio, bias current through diodes D_1 and D_2 and the transient analysis. The extra input lead provides a means for attaching additional inputs (total of nine). The output has a large valued pull up resistor since an effective pull up resistor is provided by the Nand and Flip-flop inputs. This resistor is provided so that the collector is not left floating in the "OFF" state.

1. D.C. Analysis

The equivalent circuits for the Nand in the "ON" and "OFF" states are given in Figures 3 and 4.

Initially, the Nand equations were expressed with $R_1 = 1/g_1$ as one of the unknowns and Fan-out/Fan-in as a known, In this manner, an R_1 could be determined that satisified a Fan-out/Fan-in ratio of ten (JPL requirement). Based on the equivalent circuits of Figure 3 and Figure 4, the following equation can be written. (A glossary of terms is given in Appendix A).

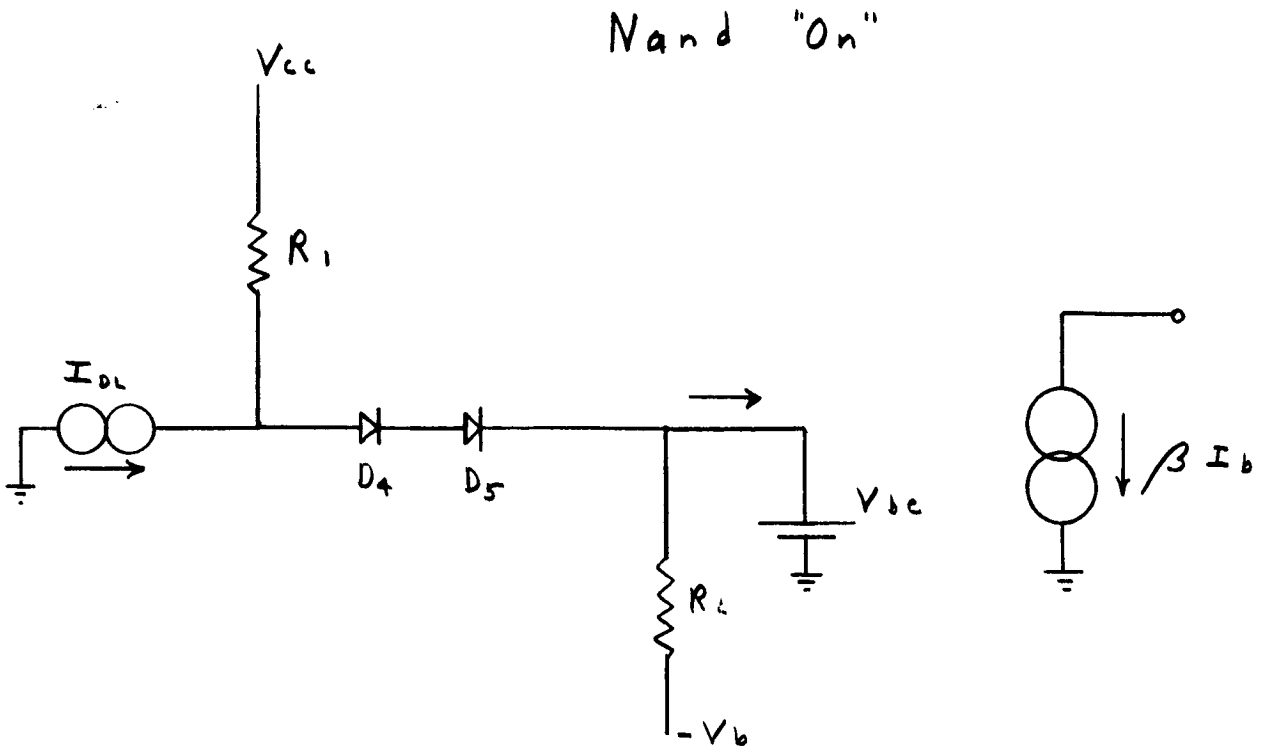

Nand "On"
Vcc
R1
IDL
D4
D5
Vbc
RL
-Vb
β Ib

Fig. 3

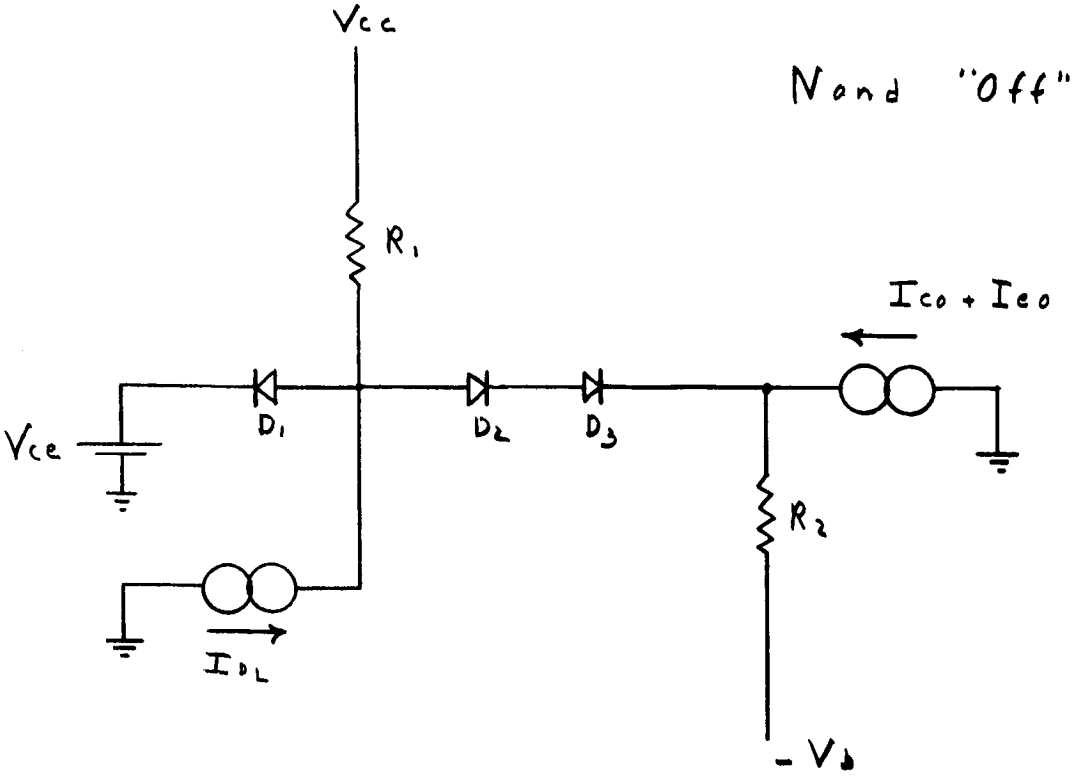

Vcc
Nand "Off"
R1
Ico + Ieo
Vce
D1
D2
D3
R2
IDL
-Vb

Fig. 4

1. $$g_1 (V_{cc} - V_{ce} - V_{D_1}) - I_{in} = -I_{co} - I_{eo} + \frac{V_{ce} + V_{D1} - V_{D2} - V_{D3} + V_b}{R_2} - I_{D_L}$$

2. $$V_{base} = V_{ce} + V_{D_1} - V_{D_2} - V_{D_3}$$

3. $$g_1 (V_{cc} - V_{D_4} - V_{D_5} - V_{be}) - I_b = \frac{V_{be} + V_b}{R_2}$$

4. $$g_1 \left[F \frac{(V_{cc} - V_{ce} - V_{D_1})}{0,97} - h_{FE} \frac{(V_{cc} - V_{D_4} - V_{D_5} - V_{be}}{1.03} \right] - F \left[\frac{(V_{ce} + V_{D_1} - V_{D_2} - V_{D_3} + V_b)}{R_2} - I_{D_L} - I_{co} - I_{eo} \right] - h_{FE} \frac{(V_{be} + V_b)}{R_2}$$

5. $$h_{FE} I_b - I"o" = \frac{V_{cc} - V_{ce}}{R_4}$$

The preceeding equations and the parameter list as given in Computer Run #1 (Appendix C) are first approximations (For explanation of computer format and description of print out, see Appendix B). The answers achieved by using these approximations yield a "ball park" solution for the desired unknowns. The print out of Computer Run #1 yields the partial deriviatives and the solutions for this first cut.

a. Computer Run #1 Conclusions:

1. The equations as written have the following unknowns:

   a. $g_1 = 1/R_1$ - the drive resistor

   b. V_{base} - the voltage appearing on the base emitter junction when the transistor is off.

   c. I_{in} - the amount of current that is pulled out by the input source.

   d. I_b - base drive

   e. I"o" - output current capability

2. From this computer run, it is seen that for a specified F of 10, the value of $R_1 = 1/g_1$ varies from 76K = $1/0.13 \times 10^{-4}$ to 1.98K = $1/0.505 \times 10^{-3}$: the 76K being the best case and the 1.98K being the worst case.

3. From the partials, it is seen that g_1 is quite sensitive to parameter 16 (R_2), $\frac{\Delta g1}{\Delta R2} = -0.415 \times 10^{-9}$. Therefore, R_2 was increased from 60K to 100K. With this change, the value of R_1 varied from 125K = $1/0.797 \times 10^{-5}$ to 15.6K = $1/0,642 \times 10^{-4}$. A substantial increase in the value of R_1 is achieved by going to an R_2 of 100K. Since the larger value of R_1 yields a substantial savings in power, R_2 was left at 100K.

4. With R_2 = 100K, h_{FE} was decreased to result in a h_{FE} of 20 at low temperature. From the print-out, it is seen that in the worst case, a negative resistor is required.

5. h_{FE} was then increased to result in a h_{FE} of 29 at -10°C. The minimum value of R_1 increased from the 15.6K for a h_{FE} of 25 to 15.8K for a h_{FE} of 29. The resultant small increase of R_1 does not seem to warrant an attempt to get a higher h_{FE}.

6. Next, R_2 was reduced back to 60K and h_{FE} was kept at 29 at -10°C. R_1 in the worst case was approximately 10K. However, it was felt that changing R_2 from 100K to 60K did not warrant a requirement for a higher h_{FE}. The 100K would supply approximately 30 μa bias through the diodes D_2 and D_3 while the 60K would supply 50 μa. This difference of 20 μa would result in a $\triangle V_{base}$ of $\approx$ 50 mv, It was felt and verified by later computer runs, that using an FD643 for D_1 and FD306 for D_2 and D_3 and the 100K bias resistor could still guarantee Q_1 off in the worst case.

B. Section A yielded "ball park" values of the desired unknowns. Realizing that the value of R_1 would also be determined by transient considerations and having the upper limit of R_1 (15.6K) from Section A, the equations were written with R_1 a known and F as a unknown. Using the equivalent circuits in Figures 3 and 4, the following equations were written.

Nand Equations (On)

1. $I_b = \frac{(V_{cc} - V_{D4} - V_{D5} - V_{be})}{R_1} + I_{DL} - \frac{(V_{be} + V_b)}{R_3}$

2. $I\text{"o"} = h_{FE}\ I_b - \frac{(V_{cc} - V_{ce})}{R_4}$

3. Power "o" $= V_{cc} \cdot \frac{(V_{cc} - V_{D_4} - V_{D5} - V_{be})}{R_1} + V_b \cdot \frac{(V_{be} + V_b)}{R_3} + V_{cc} \cdot \frac{(V_{cc} - V_{ce})}{R_4}$

Nand Equations (Off)

1. $I_{in} = \frac{(V_{cc} - V_{ce} - V_{D_1})}{R_1} + I_{co} + I_{eo} + I_{DL} - \frac{(V_{ce} + V_{D_1} - V_{D_2} - V_{D_3} + V_b)}{R_3}$

2. $V_{base} = V_{ce} + V_{D_1} - V_{D_2} - V_{D_3}$

3. Power "1" $= V_{cc} \cdot \frac{(V_{cc} - V_{ce} - V_{D1})}{R_1} + V_b \cdot \frac{(V_b + V_{base})}{R_3}$

In addition, one other equation is necessary. This is the ratio of loading current to drive current or Fan-out/Fan-in = F.

Nand Equations

1. Fan-out/Fan-in =

$$\frac{I_b\ h_{FE}}{*g_1\ (V_{cc} - V_{ce} - V_{D_1}) - *g_3\ (V_{ce} + V_{D_1} - V_{D_2} - V_{D_3} + V_b) + I_{co} + I_{eo} + I_{DL}}$$

* g_1 and g_3 were used for ease of putting equation into computer format and to allow the R_1 of the driving stage to vary in the opposite direction than that of the stage being driven.

b. Computer Run #2 Conclusions:

1. The equations as written, have the following unknowns:

a. I_{in} - the amount of current pulled out by the input source.

b. V_{base} - the voltage appearing on the base emitter junction when the transistor is off.

c. I_b - base drive

d. F - Fan-out/Fan-in

e. I"o" - output current capability

f. Power "1" - power being dissipated when the output is high.

g. Power "0" - power being dissipated when the output is saturated.

NOTE: The currents I_{in}, I_b, and I"0" were solved for in order to determine the proper operating points of D_1, D_4, D_5, V_{be} and h_{FE}.

2a. Nominal Solutions

I_{in} = 398 μ a

V_{base} = -0.33v

I_b = 263 μ a

F = 39

I"o" = 15.7 ma.

Pw."1" = 3.1 mw

Pw."o" = 2.49 mw.

b. From the computer run partials the following results are noted:

1. $\frac{\Delta P_w \text{ "1"}}{\Delta V_{cc}}$ = 0.93 mw/volt - a one volt change causes a one milliwatt change in power.

2. $\frac{\Delta F}{\Delta V_{cc}}$ = 5.05/volt - a one volt increase causes an increase of 5 in Fan-out/Fan-in.

3. $\frac{\Delta V_{base}}{\Delta V_{D_1}}$ = 1 volt/volt - V_{base} changes an equal amount with V_{D_1} and $(V_{D_2} + V_{D_3})$.

$\frac{\Delta V_{base}}{\Delta V_{D_2}, V_{D_3}}$ = -2 volt/volt

$\frac{\Delta V_{base}}{\Delta T}$ = 2.43 mv/°C

4. $\frac{\Delta F}{\Delta h_{FE}}$ = 0.66/unit - for an in crease in h_{FE} of 1.5, F increase by 1 (one additional load)

c. V_{base} maximum is negative -0.02. Under worst case condition, the base emitter junction is still reversed biased. A noise pulse of greater than 0.3v would be required to trip the Nand.

d. Fan-out/Fan-in minimum is 10.8. With R_1 = 10K, the Nand can drive 10.8 D.C. loads.

e. I"o" minimum is 3.6 ma. This is low when consideration is given to A.C. loading (one F/F $\approx$ 1.4 ma.). In order to be able to drive at least four flip flops, I"o" minimum will have to be increased to at least 5.6 ma.

f. Power dissipation - the maximum power dissipation occurs when the output is high ("1"). From the computer run, the worst case value is 3.1 mw.

3. In the second print out of computer run #2, R_1 was changed to 6.2K in order to increase I"o" minimum.

a. Nominal Solutions

I_{in} = 659 μ a

V_{base} = -0.33v

I_b = 447 μ a

F = 40.6

I_o = 26 ma.

Pw "1" = 3.4 mw

Pw "o" = 2.5 mw.

b. V_{base} minimum remained -0.02. This is due to the diodes being expressed as voltage sources.

c. Fan-out/Fan-in minimum increased to 11.6.

d. I "o" minimum increased to 6.5 ma. worst case. This drive capability is sufficient for four flip flop loads.

e. Power dissipation - the maximum power dissipation is 5.02 mw worst case.

A third and final computer run was necessary in order to substitute in the correct operating points for D_1, D_2, D_3, D_4, D_5, V_{be} using the bias currents obtained from Computer Run #2. The same equations were used as in Computer Run #2, the difference is in the parameter list, plus some minor terms that had been left out of the previous computer run.

c. Computer Run #3 Conclusions:

1. The equation unknowns are the same as for Computer run #2.

2a. Nominal Solutions

I_{in} = 663 μ a.

V_{base} = -0.32 v

I_b = 465 μ a

F = 38

I"o" = 25 ma.

Pw "1" = 3.5 mw

Pw "0" = 2.6 mw

b. V_{base} maximum is positive 0.01 volts. Therefore, under worst case conditions, Q_1 is still guaranteed off.

c. Fan-out/Fan-in minimum is 11.0. The requirement of at least F = 10 is met.

d. I"0" minimum is 6.3 ma. This remains sufficient to trigger four flip flops.

e. Power Dissipation - the maximum power dissipation is 5.2 mw worst case.

3. In the second print out of Computer Run #3, the power supplies were changed from $\pm$ 15% to $\pm$ 5%.

a. Nominal Solutions

I_{in} = 663 μ a

V_{base} = -0.32 v

I_b = 465 μ a

F = 38

I"o" = 25 ma.

Pw "1" = 3.5 mw

Pw "o" = 2.6 mw

b. V_{base} maximum remains the same +0.01. This is due to the representation of diode drops as voltage sources and not as a function of current. No attempt was made to factor this in for this run since this would lead to an improvement and Q_1 is already guaranteed off.

c. Fan-out/Fan-in minimum increased to 12.5 worst case.

d. I"1" minimum increased to 8.25 ma.

e. Power Dissipation - The maximum power dissipation decreased to 4.3 mw worst case.

D.C. Analysis Conclusion:

The final computer run (Computer Run #3) contains the final circuit values and worst case circuit solutions. Solutions were given for both $\pm$ 15% and $\pm$ 5% power supplies. As can be seen from the results, a large improvement is gained by decreasing the power supply tolerances.

The computer analysis was based on two different type diodes (FD643 and FD306) having the forward voltage drop tightly specified at a particular current level. (See Parts List p. 14).

2. TRANSIENT ANALYSIS NAND

a. Storage Time: the time required to pull out the stored charge is given by:

$$t_s = \tau_b \ln \frac{I_{b1} + I_{B2}}{I_{B2} + I_{bs}}$$ Equation 6 - Appendix E

1. Nominal

Using Computer Run #3 to obtain nominal values -

$I_{b1} = 465\,\mu a$

$I_{in} = 663\,\mu a$

$h_{FE} = 55$ (from specification sheet)

$I_{B2} = 35\,\mu a$

$I_{bs} = \frac{4 \times 663\,\mu a}{55} = 48.2\,\mu a$ assuming four loads

$\tau_b = \tau_s < 13$ nsec. (from spec. sheet)

$t_s < 13 \times 10^{-9} \ln \frac{500}{83.2} = 23.2$ nsec.

2. Worst Case (± 15% Power Supplies)

$$t_s = \frac{\tau_s}{0.69} \ln \frac{I_{b1} + I_{B2}}{I_{bs} + I_{B2}}$$

Worst case occurs at maximum V_{cc}, minimum V_b, and high temperature.

$\tau_s < 20$ nsec. from spec. sheet

$\overline{I_{b1}} = 699\,\mu a$ from best case in Computer Run #3

$\underline{I_{B2}} = 29\,\mu a$

$$\underline{I_{b3}} = \frac{I_o \text{ min. (at above condition)}}{h_{FE}} = \frac{V_{cc} - V_D - V_{ce}}{R_1,\ h_{FE}}$$

since I_{bs} occurs for the case of one D.C. load.

h_{FE} max. = 120 + 120 x 55 x .009 = 120 + 59.5 = 179.5

$$I_{bs} = \frac{5.75 - 0.593 - 55 \times 2.25 \times 10^{-3} - 0.2}{6.45 \times 10^{3} \times 179.5} = 4.4\ \mu a$$

$$t_s < \frac{20 \times 10^{-9}}{0.69} \ln \frac{699 + 29}{4.4 + 29} = 29 \times 10^{-9} \ln 20.8$$

$$t_s < 88 \text{ nsec.}$$

3. Worst Case (±5% Power Supplies)

$\tau s < 20$ nsec.

$\overline{I_{b1}} = 612\ \mu a$

$\underline{I_{B2}} = 30\ \mu a$

$\underline{I_{bs}} = 3.98\ \mu a$

$t_s < 29 \times 10^{-9} \ln 18.9$

$t_s < 85$ nsec.

b. Fall Time (voltage rise time)*- The fall times of interest are:

1. The time the voltage rises driving the flip-flop only.
2. The time the voltage rises until it reaches $V_{be} + V_{D4} + V_{D5} - V_{D1} = V_c$ when driving Nands and flip-flops.
3. The worst case condition of driving the Nands and one F/F input. This is a repetition rate consideration and any F/F input loads greater than one, will decrease the t_f and thus increase possible repetition rate.

The fall time is calculated assuming no help is derived from the diode capacitances. This is a realistic assumption since the FD306 is a fairly low capacitance diode and the diodes "see" a very small ΔV across them.

*Traditionally transistor fall time is transistor turn off time which in this case (NPN transistor) is circuit voltage rise time.

The fall time equation is given by:

$$t_f = \left[\tau_a + \frac{h_{fe}\, R_L\, Q_c}{V_{cc}}\right] \ln \frac{I_{B2} + I_{bs}}{I_{B2}}$$

since $\frac{h_{fe}\, R_L}{V_{cc}} = \frac{1}{I_{bs}}$

$$t_f = \left[\tau_a + \frac{Q_c}{I_{bs}}\right] \ln \frac{I_{B2} + I_{bs}}{I_{B2}}$$

In order to check the validity of the equation for the Nand, the nominal solution was calculated and verified in the laboratory.

1. Nominal

$$\tau_a = \frac{1}{2\pi f_T} = \frac{1}{2\pi\ 500\ MC} = 0.32 \text{ nsec.}$$

$h_{fe} = 55$

$I_{B2} = 35\ \mu a$

$I_{bs} = \frac{4 \times 663\ \mu a}{55} = 48.2\ \mu a$. assuming four loads

$Q_c = 1.2\ C_{ob}\ V_{cb} = 1.2 \times 4.5 \times 10^{-12} \times 5 = 27 \times 10^{-12}$

if a pull up resistor is used

$$t_f = 0.32 \text{ nsec.} + \frac{27 \times 10^{-12}}{48.2 \times 10^{-6}} \ln \frac{35 + 48.2}{48.2}$$

$= 0.56 \times 10^{-6} \ln 1.725$

$= 0.3\ \mu$sec. (0.3 μ sec. x 0.9 for observed value at 90% point)

Measured value in laboratory = 260 nsec. letting collector swing to 90% V_{cc} .

2. Worst Case (± 15% Power Supplies)

Worst case occurs at maximum V_b (-2.55v), minimum V_{cc} (4.25v) low temperature (-10°C), and minimum h_{FE}. Using the worst case solutions when I "o" is minimum (Computer Run #3), the following solutions are obtained:

I_{in} = 524.8 μa (This is the same for either a Nand or a F/F input, since the input circuitry is identical).

F = 11.0

I_o = 6.3 ma.

In order to solve for I_o when V_b is maximum, the partial $\frac{\Delta I_o}{\Delta V_b}$ is used.

$\frac{\Delta I_o}{\Delta V_b} = -0.55 \times 10^{-3}$ from computer run

$\Delta V_b = 2.55 - 3.45 = -0.9v$

$\Delta I_o = 0.55 \times 10^{-3} \times 0.9 = 0.495 \times 10^{-3}$

I_o (at $V_b = 2.55$) = 6.3 ma + 0.495 ma. = 6.8 ma.

$\frac{\Delta I_{in}}{\Delta V_b} = -0.1 \times 10^{-4}$

I_n (at $V_b = 2.55$) = (524.8 + 9) μa = 534 μa.

$Q_c = 1.2 \times 6 \times 10^{-12} \times 4.25 = 30.6 \times 10^{-12}$

$h_{fe} = 25$

f_T = 300 MC

$$I_{B2} = \frac{2.55v + V_{be}}{R_3} = 31\,\mu a.$$

$$I_{bs} = \frac{\text{number of loads} \times I_{in}}{h_{FE}} = \frac{(\# + *) \times 534\,\mu a}{25} =$$

$$(\# + *) \times 21.4\,\mu a$$

\# = number of Nand loads

* = number of F/F inputs.

a. F/F D.C. Loading

Using Equation 9, Appendix E for turn off time and considering D.C. loading only.

$$t_{f(F/F)} = 0.9 \left[0.53 \text{ nsec.} + \frac{30.6 \times 10^{-12}}{* \times 21.4 \times 10^{-16}} \right] \ln \frac{31 + * \times 21.4}{31}$$

Note: Multiplying times 0.9 yields actual measured 90% value.

A plot of worst case turn-off time (t_f) versus the number of F/F inputs is given in Figure 5.

b. D. C. (F/F) and Capacitive Loading

In order to factor in the capacitive loading, the worst case turn-off time is taken as the sum of two times: the D.C. t_f and 2.3 x R_L C_s. The 2.3 term yields the time at which R_L C_s is at 90% of finalvalue.

$$t_{f(F/F)} = 0.9 \left[0.53 \times 10^{-9} + \frac{1.43 \times 10^{-6}}{*} \right] \ln \frac{31 + * \times 21.4}{31} + \frac{14.7 \times 10^3}{*} \times C_s$$

Equation 12

Note: The 14.7×10^3 is arrived at by $2.3 \times 1.04 \times 6.2 \times 10^3 = 14.7 \times 10^3$

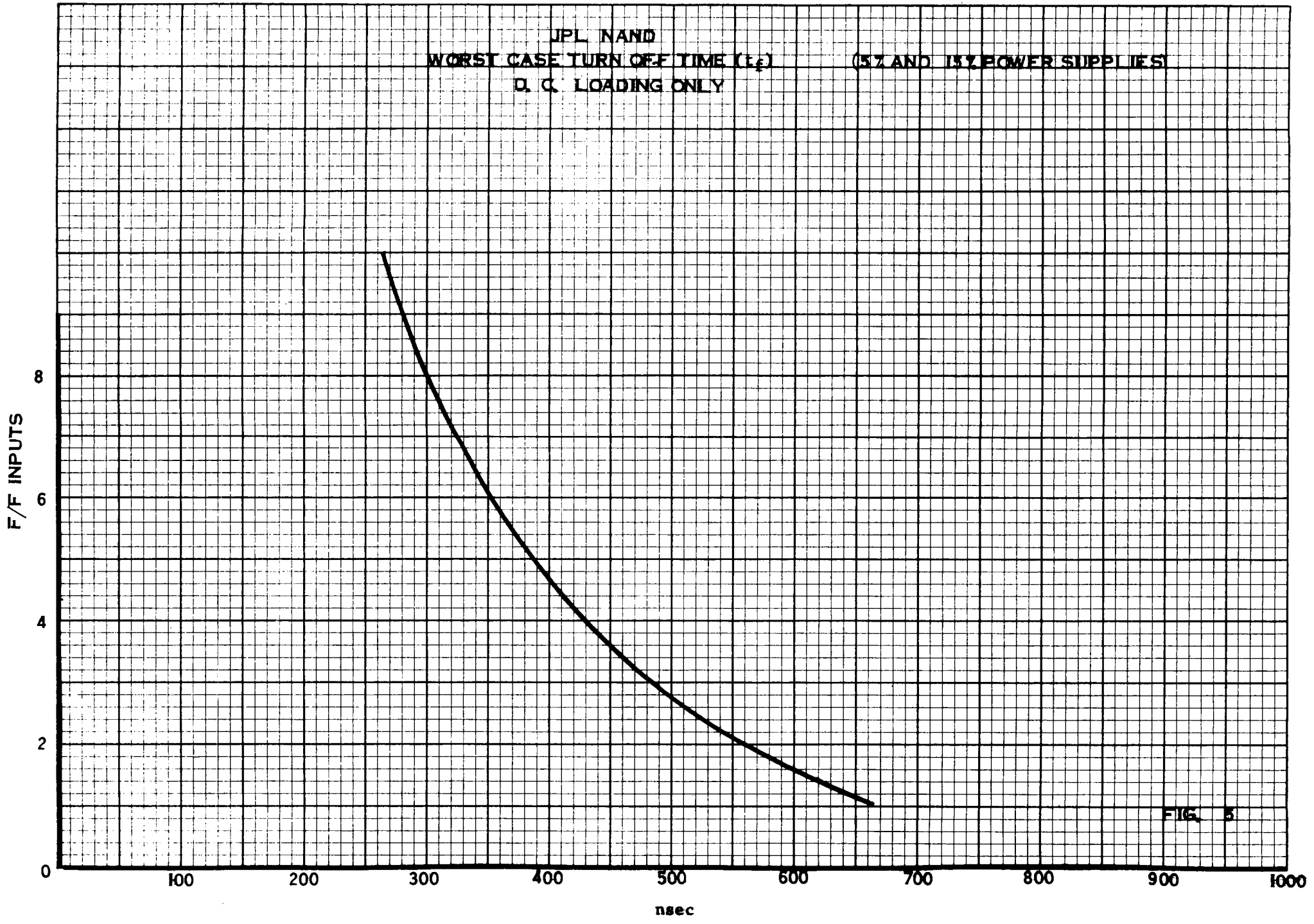

JPL NAND
WORST CASE TURN OFF TIME (t_f)
D. C. LOADING ONLY
(5% AND 15% POWER SUPPLIES)
F/F INPUTS
0
2
4
6
8
100
200
300
400
500
600
700
800
900
1000
nsec

FIG. 5

Example: For the case of eight (8) loads and 100 pf, the worst case turn-off time is given by:

$$t_{f(F/F)} = 0.9 \left[0.53 + \frac{30.6 \times 10^{-12}}{8 \times 21.4 \times 10^{-6}} \right] \ln \frac{31 + 8 \times 21.4}{31} + 1.83 \times 10^{3} \times 100 \times 10^{-12}$$

$$= 0.62 \mu \text{ sec.}$$

A plot of t_f versus D.C. (F/F) and capacitive loading is given in Figure 6.

c. Nand D.C. Loading

Figure 5 is not valid for Nand D.C. loading. In the case of Nand D.C. loading, the loading changes once it reaches $V_{be} + V_{D4} + V_{D5} - V_{D1} = V_c$. If the fall time is assumed to be exponential (realistic since it is essentially an RC charging) then t_{FN} can be solved for as follows:

$$V_c = \underline{V_{cc}} \ (1 - e^{- t_{fN} \times 2.3/t_f})$$

$$V_c = 0.78 + 35 \times 1.7 \times 10^{-3} + 2 \ (0.66 + 35 \times 2.5 \times 10^{-3}) - 0,485 - 35 \times 2.25 \times 10^{-3})$$

$$= 0.78 + 0,0595 + 1.32 + 0.175 - 0.485 - 0.079$$

$$= 1.57v$$

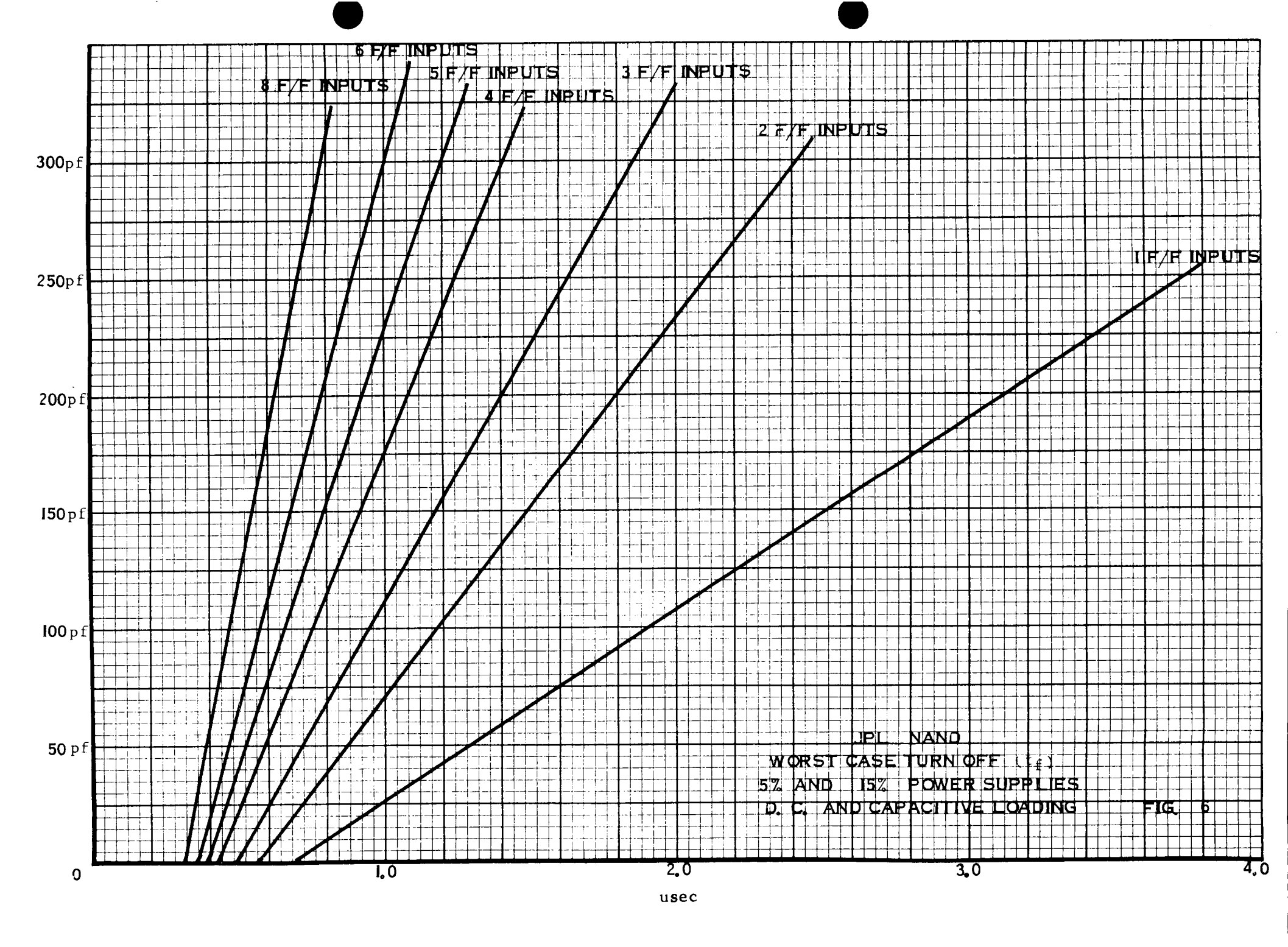
$$1.57 = 4.25 \ (1 - e^{- t_{fN} \ 2.3/t_f})$$

where $\frac{tf}{2.3}$ is the time constant of the driving waveform. The 2.3 is due to t_f being defined as 90% of final value.

$$\log 0.6 = \frac{-2.3 \ t_{fN}}{t_f}$$

$t_{fN} = 0.217 \ t_f$ letting * of Equation 12 equal # + *

Figure 7 is a plot of t_{fN} versus loads.


8 F/F INPUTS
6 F/F INPUTS
5 F/F INPUTS
4 F/F INPUTS
3 F/F INPUTS
2 F/F INPUTS
1 F/F INPUTS
300pf
250pf
200pf
150pf
100pf
50 pf
0
1.0
2.0
3.0
4.0
usec
IPL NAND
WORST CASE TURN OFF (tf)
5% AND 15% POWER SUPPLIES
D. C. AND CAPACITIVE LOADING
FIG. 6

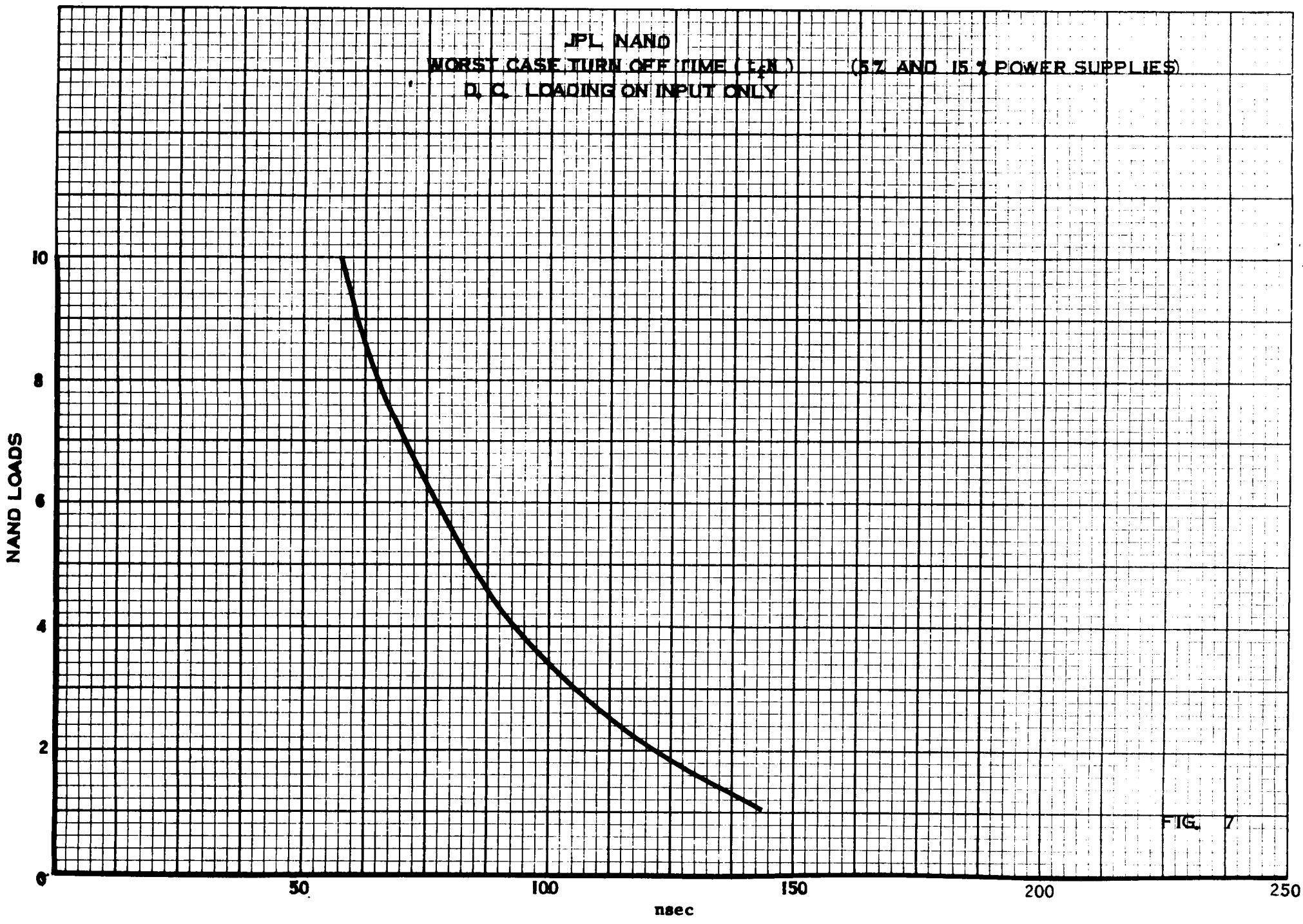

JPL NAND
WORST CASE TURN OFF TIME (t_{pHL})
D. C. LOADING ON INPUT ONLY
(5% AND 15% POWER SUPPLIES)
NAND LOADS
0
2
4
6
8
10
50
100
150
200
250
nsec

FIG. 7

d. D.C. (Nand) and Capacitive Loading

t_{fN} is calculated in the same manner as part c.

$t_{fN} = 0.217\ t_f$

Figure 8 is a plot of t_{fN} versus D.C. and capacitive loading.

e. Nand and F/F Loading

The condition of driving a combination of Nands and F/F's is the combination of two times: t_{fN} and the time required to rise from V_{clamp} to 90% V_{cc}. This time t_f is given by:

$$t_f = 0.217 \left[0.53 \times 10^{-9} + \frac{1.43 \times 10^{-6}}{\# + *} \right] \ln \frac{31 + 21.4\ (\# + *)}{31} +$$

$$0.773 \left[0.53 \times 10^{-9} + \frac{1.43 \times 10^{-6}}{*} \right] \ln \frac{31 + 21.4 \times *}{31} +$$

$$0.217 \times \frac{14.7 \times 10^3}{\# + *} \times C_s + 0.773 \times \frac{14.7 \times 10^3 \times C_s}{*}$$

or

$t_f = t_{fN} + 0.78\ t_f$

Example: For the worst case of no Nands, one F/F input and 30 pf stray capacitance:

$t_f = 1.09\ \mu$ sec. from Figure 6. This is sufficient to guarantee 500 KC operation.

3. Worst Case (±5% power supplies)

Using the ±5% power supply print out of Computer Run #3, the following solutions are obtained:

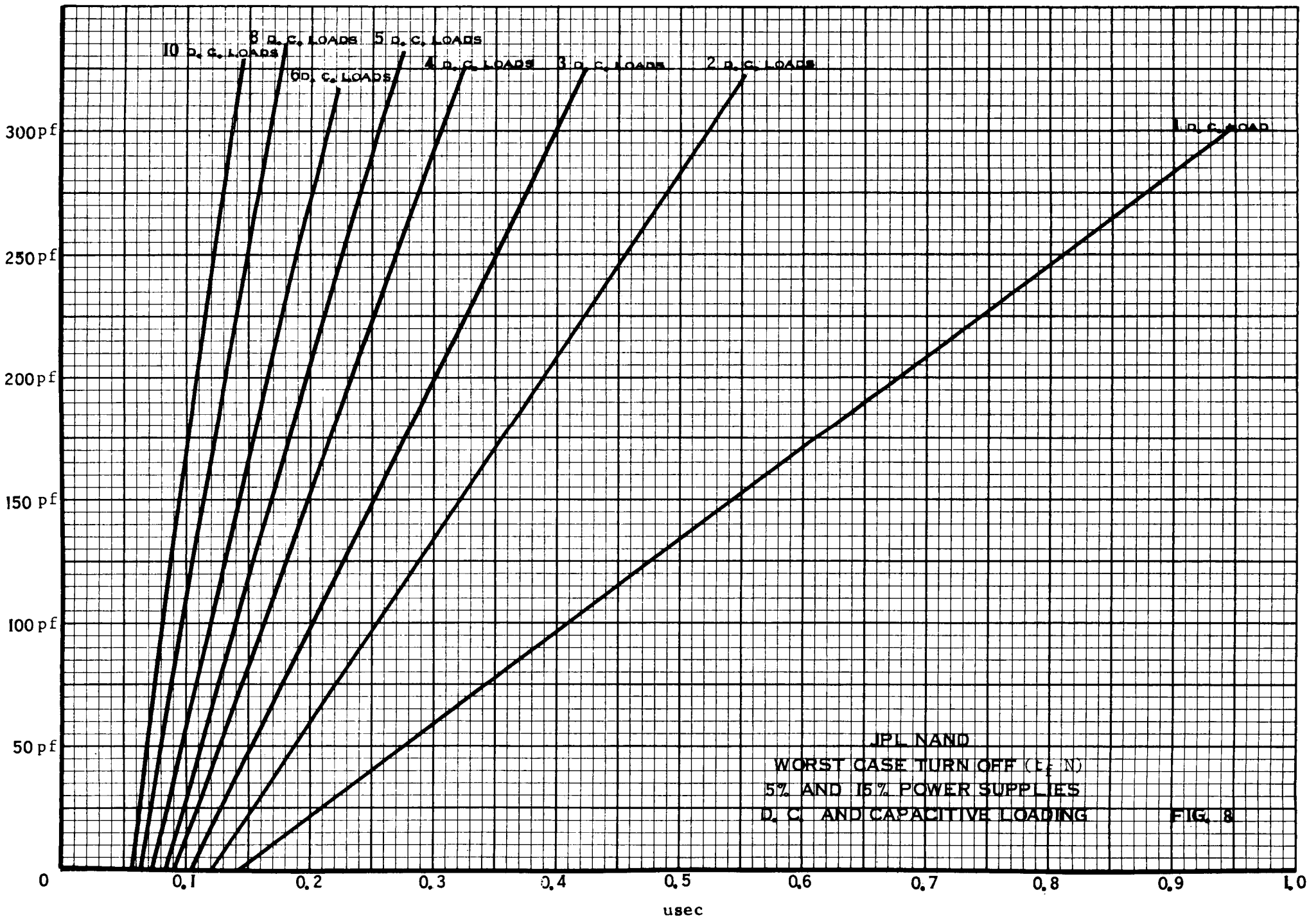

10 D. C. LOADS
8 D. C. LOADS
6 D. C. LOADS
5 D. C. LOADS
4 D. C. LOADS
3 D. C. LOADS
2 D. C. LOADS
1 D. C. LOAD
300 pf
250 pf
200 pf
150 pf
100 pf
50 pf
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
usec
JPL NAND
WORST CASE TURN OFF (E, N)
5% AND 15% POWER SUPPLIES
D. C. AND CAPACITIVE LOADING

FIG. 8

$I_{in} = 605\,\mu a$

$F = 12.5$

$I_o = 8.25$ ma.

$$\frac{\Delta I_o}{\Delta V_b} = -0.55 \times 10^{-3}$$

$\Delta V_b = -0.3$ v

$\Delta I_o = 0.165$ ma

$I_o = 8.415$ ma.

$$\frac{\Delta I_{in}}{\Delta V_b} = -0.1 \times 10^{-4}$$

$\Delta I_{in} = 3\,\mu a$

$\underline{I_{in}} = 608\,\mu a.$

$Q_c = 1.2 \times 6 \times 10^{-12} \times 4.75 = 34.2 \times 10^{-12}$

$$I_{bs} = \frac{(\# + *)\ I_{in}}{h_{FE}} = (* + \#) \times 24.3\,\mu a.$$

a. <u>F/F D. C. Loading</u>

$$t_{f(F/F)} = 0.9 \left[0.53 \text{ nsec.} + \frac{34.2 \times 10^{-12}}{* \times 24.3 \times 10^{-16}} \right] \ln \frac{34 + * \times 24.3}{34}$$

A plot of worst case turn-off time (t_f) versus the number of F/F inputs is given in Figure 5. (Note: the ±5% and ±15% Power Supply curves are approximately the same, therefore, only one curve is shown--this was also verified in the laboratory).

b. <u>D. C. (F/F) and Capacitive Loading</u>

The capacitive loading was factored in the same way as for the ±15% Power Supply case. A plot of t_f versus D.C. and capacitive loading is given in Figure 6.

c. Nand D.C. Loading

This case of the Nand D.C. loading for the ±5% power supply is similar to part c of the ±15% P.S. case. The resulting curve is approximately the same curve as Figure 7.

d. D.C. (Nand) and Capacitive Loading

Since t_{fN} is approximately the same for the ±5% power supply case, the condition of capacitive loading is also the same as given in Figure 8.

c. Delay Time

During the delay, the depletion regions are charged by the driving source. The expression for the delay time is given by:

$$t_{dr} = \left[\frac{2\ t_{ri}}{I_b}\ (Q_e + Q_{cd})\right]^{\frac{1}{2}} \quad \text{if } t_d \ll t_r \quad \text{Equation (1) Appendix E}$$

$$t_{dr} = \frac{Q_e + Q_{cd}}{I_b} + \frac{t_{ri}}{2} \quad \text{if } t_d > t_r \quad \text{Equation (2) Appendix E}$$

Refer to Appendix E for derivation.

1. Nominal

I_b = 465 μ a.

Q_e = 1.67 C_{ib} $V_{be_{off}}$ = 1.67 x 6 x 10^{-12} x 0.32 = 3.2 x 10^{-12}

Q_{cd} = 1.2 C_{ob} ΔV_{cb} = 1.2 x 4.5 x 10^{-12} x 0.32 = 1.73 x 10^{-12}

t_{ri} = t_{fN} of driving source $\approx$100 nsec. for four loads and 50 pf stray capacitance on Nand output

$$t_{d_r} = \left[\frac{200 \times 10^{-9}}{456 \times 10^{-6}}\ (3.2 \times 10^{-12} + 1.73 \times 10^{-12})\right]^{\frac{1}{2}}$$

= 46 nsec.

Observed value in laboratory = 45 nsec.

2. Worst Case (±15% Power Supplies)

Worst case occurs at minimum V_{cc}, V_b, and low temperature.

I_b = 262 μa

$Q_e = 1.67 \times 9 \times 10^{-12} \times 0.65 = 9.8 \times 10^{-12}$

$Q_c = 1.2 \times 6 \times 10^{-12} \times 0.65 = 4.7 \times 10^{-12}$

t_{fN} = 0.225 μ sec. for worst case of 1 load and 30 pf on Nand output

t_{d_r} = 158 nsec.

3. Worst Case (±5% Power Supplies)

I_b = 342 μa.

$Q_e = 9.8 \times 10^{-12}$

$Q_c = 4.7 \times 10^{-12}$

t_{fN} = 0.225

t_{d_r} = 138 nsec.

d. Rise Time (Voltage Fall Time)*

The time required to saturate Q_1 is given by:

$$t_r = \left[\tau a + \frac{Q_c}{I_{bs}}\right] \ln \frac{I_{b1}}{I_{b1} - I_{bs}}$$ Equation (5) Appendix E

$$\tau a = \frac{1}{2 \pi f t}$$

1. Nominal

I_{b1} = 465 μa.

τa = 0.3 nsec.

* Traditionally transistor rise time is transistor turn on time which in this case (NPN transistor) is circuit voltage fall time.

$$Q_c = 1.2 \times 4.5 \times 10^{-12} \times 5 = 27 \times 10^{-12}$$

$$I_{bs} = \frac{I_{in} \times (\# + *)}{h_{fe}} = \frac{663 \times 10^{-6} \times 4}{55} = 48.4\,\mu a \text{ assuming}$$

four loads

$$t_r = \left[0.3 \times 10^{-9} + 0.557 \times 10^{-6}\right] \ln 1.12$$

$$= 61 \text{ nsec.}$$

55 nsec. observed in laboratory

2. Worst Case (±15% Power Supplies)

Since the rise time is of interest in connection with the F/F triggering, the worst case conditions are low power supplies and low temperature.

a. D.C. Loading Only

$$I_{b1} = 261\,\mu a.$$

$$\tau a = 0.53 \text{ nsec.}$$

$$Q_c = 1.2 \times 6 \times 10^{-12} \times 4.25 = 30.6 \times 10^{-12}$$

$$I_{bs} = \frac{I_{in} \times (\# + *)}{h_{fe}} = \frac{525 \times 10^{-6} (\# + *)}{25} = 21 \times 10^{-6} \times (\# + *)$$

$$t_r = \left[0.53 \times 10^{-9} + \frac{1.455 \times 10^{-6}}{(\# + *)}\right] \ln \frac{261}{261 - 21 \times (\# + *)}$$

Figure 9 is a worst case plot of t_r (turn on time) versus number of loads for D.C. loading only.

b. Capacitive Loading

In order to include the effect of capacitive loading, an additional charge must be supplied to the base. The total charge

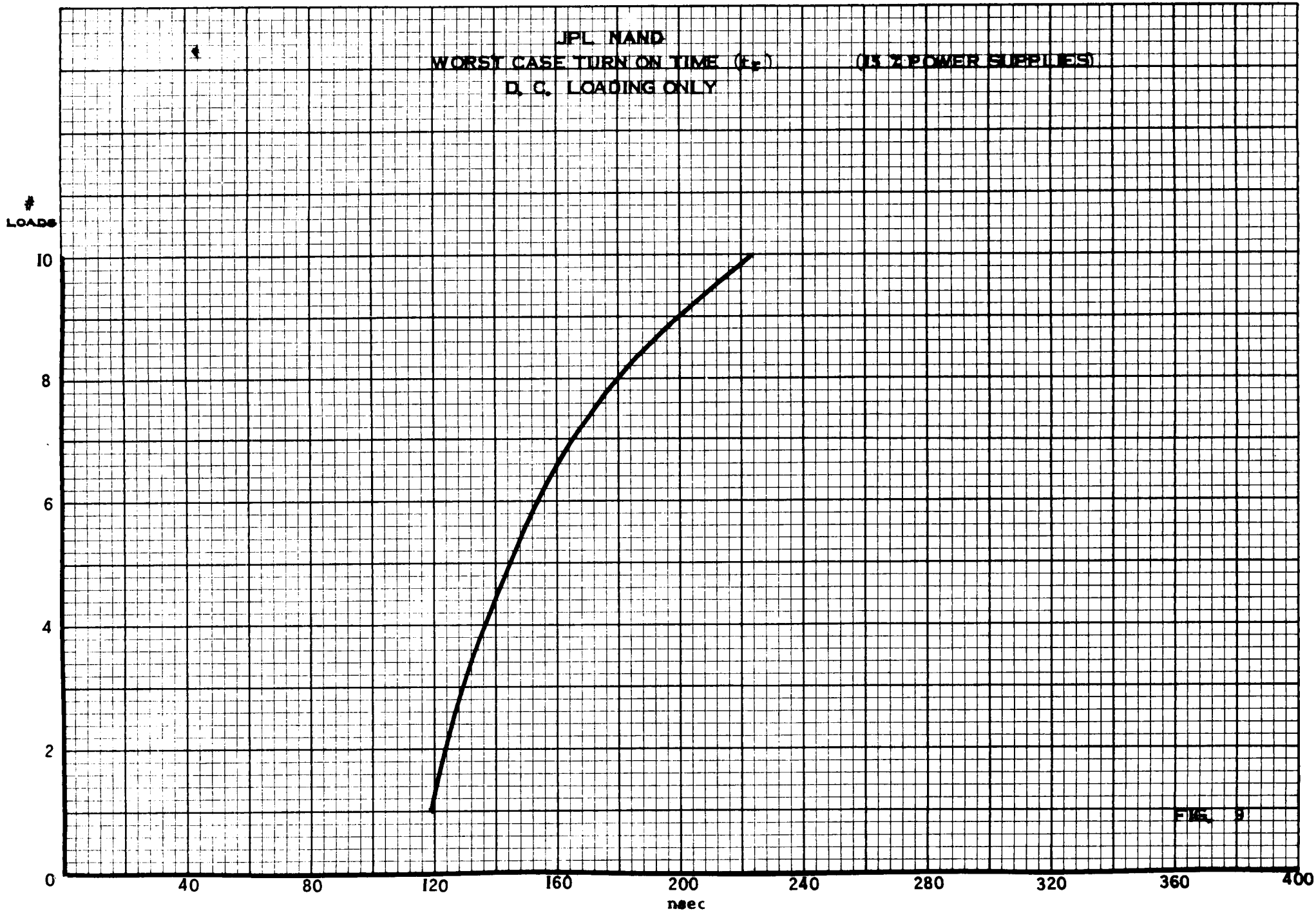

JPL NAND
WORST CASE TURN ON TIME (t_{pd})
D. C. LOADING ONLY
(15 V POWER SUPPLIES)
LOADS
10
8
6
4
2
0
40
80
120
160
200
240
280
320
360
400
nsec

FIG. 9

supplied to the base then will be the sum of Q_c plus Q_s. Q_s is the stray capacitance charge reflected to the base. The rise time equation can be written as:

$$t_r = \left[\tau a + \frac{Q_c + Q_s}{I_{bs}}\right] \ln \frac{I_{b1}}{I_{b1} - I_{bs}}$$

$$Q_s = C_s \frac{(V_{cc} - V_{ce})}{h_{fe}}$$

For the worst case condition being considered:

$$t_r = \left[0.53 \times 10^{-9} + \frac{1.455 \times 10^{-6} + 7.9 \times 10^{3}\ C_s}{\# + *}\right] \ln \frac{261}{261 - 21 \times (\# + *)}$$

Example: Consider the worst case conditions of 4 D.C. loads and 100 pf stray capacitance.

t_r = 562 nsec. ln 1.475

= 218 nsec.

Figure 10 is a plot of t_r versus D.C. and capacitive loading.

3. Worst Case (±5% Power Supplies)

a. D.C. Loading Only

I_{b1} = 342 μ a.

τa = 0.53 nsec.

Q_c = 34.2×10^{-12}

I_{bs} = $24.2 \times 10^{-6} \times (\# + *)$

$$t_r = \left[0.53 \times 10^{-9} + \frac{1.415 \times 10^{-6}}{\# + *}\right] \ln \frac{342}{342 - 24.2 \times (\# + *)}$$

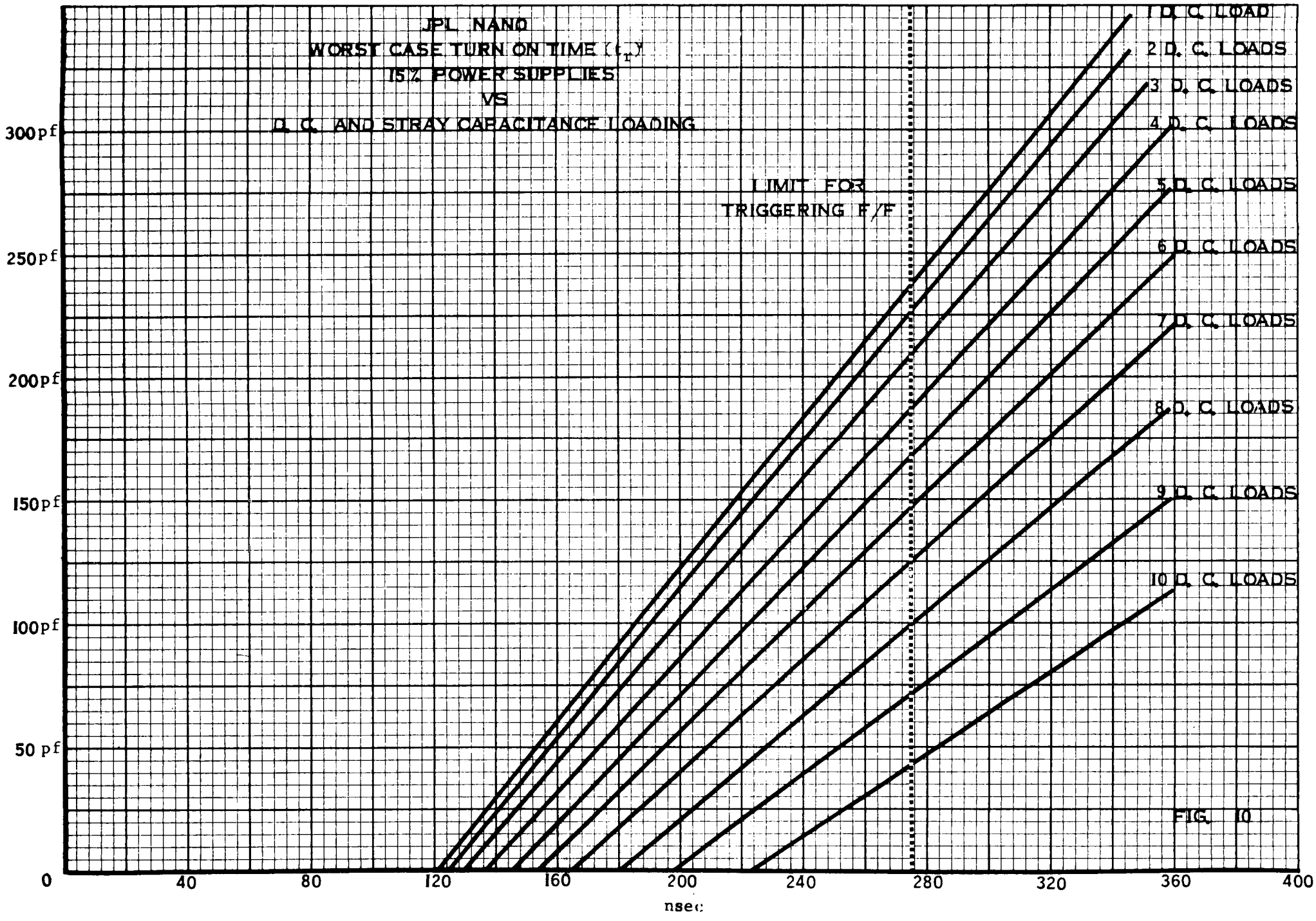

JPL NANO
WORST CASE TURN ON TIME (t_r)
15% POWER SUPPLIES
VS
D. C. AND STRAY CAPACITANCE LOADING
LIMIT FOR
TRIGGERING F/F
1 D. C. LOAD
2 D. C. LOADS
3 D. C. LOADS
4 D. C. LOADS
5 D. C. LOADS
6 D. C. LOADS
7 D. C. LOADS
8 D. C. LOADS
9 D. C. LOADS
10 D. C. LOADS
300pf
250pf
200pf
150pf
100pf
50 pf
0
40
80
120
160
200
240
280
320
360
400
nsec

FIG. 10

Figure 11 is a worst case plot of t_r versus number of loads D.C. loading.

b. Capacitive Loading

$$t_r = \left[0.53 \times 10^{-9} + \frac{1.415 \times 10^{-6} + 7.85 \times 10^{3} \times C_s}{\# + *}\right] \ln \frac{342}{342 - 24.2 \times (\# + *)}$$

Figure 12 is a plot of t_r versus D.C. and capacitive loading.

e. Turn Off Delay

The turn off delay (t_{od}) is the time required to forward bias D_1 and thus, start pulling out base drive. The total turn off delay is the sum of t_{od} plus t_s. Assuming t_r of the driving stage to be an exponential, the turn off delay is given by

$$t_{od} = -\frac{t_r}{2.3} \ln \frac{V_Q}{V_{cc}}$$

V_Q = voltage at which time base current is pulled out.

$V_Q = V_{be} + V_{D4} + V_{D5} - V_{D1}$

2.3 - this term comes from the assumption that t_r is measured at the 90% point.

1. Nominal

$$V_Q = 0.68 + 0.605 + 0.605 - 0.530 = 1.36v$$

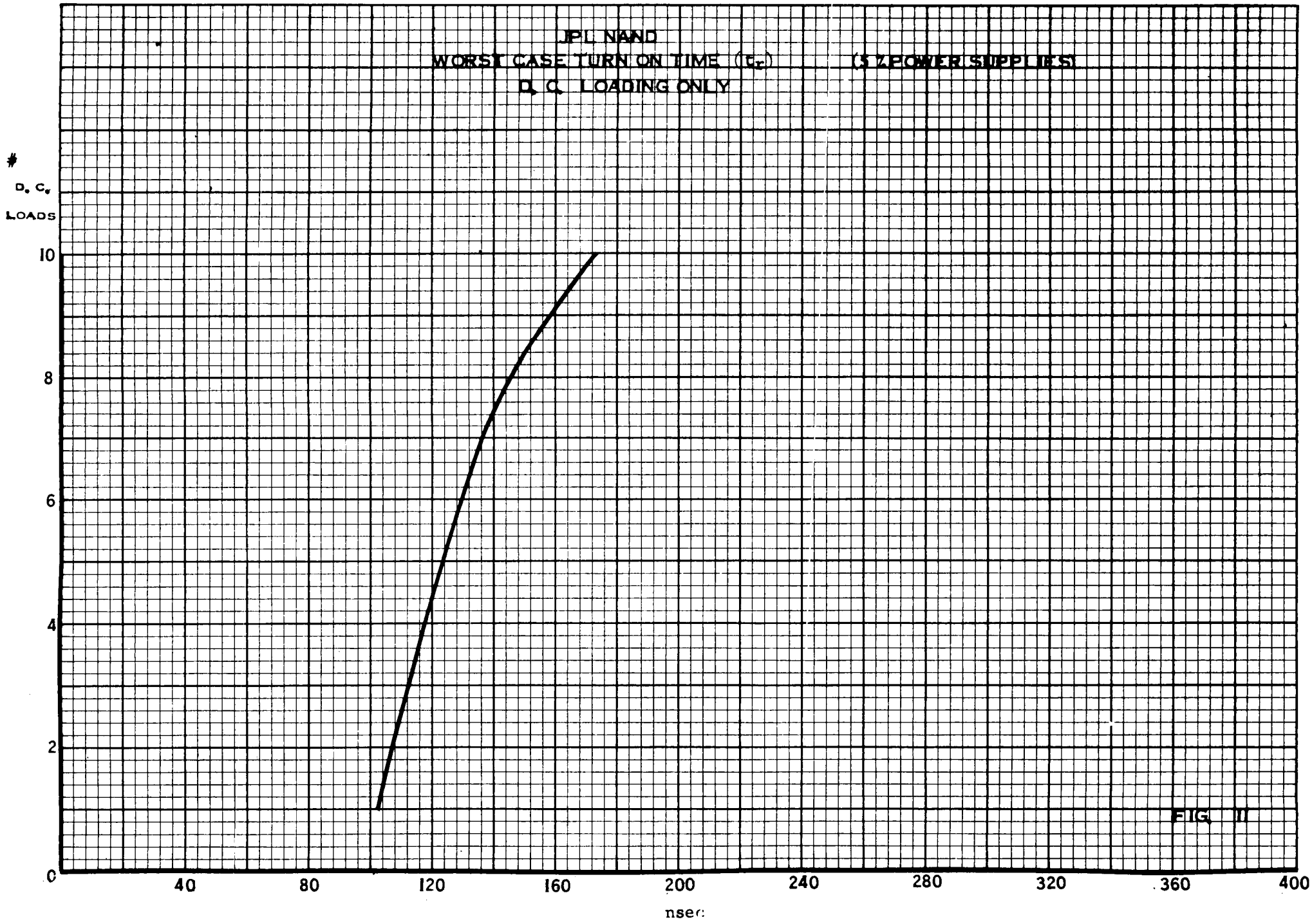

JPL NAND
WORST CASE TURN ON TIME (t_r)
D. C. LOADING ONLY
(3 Z POWER SUPPLIES)
D. C. LOADS
0
2
4
6
8
10
40
80
120
160
200
240
280
320
360
400
nsec

FIG. 11

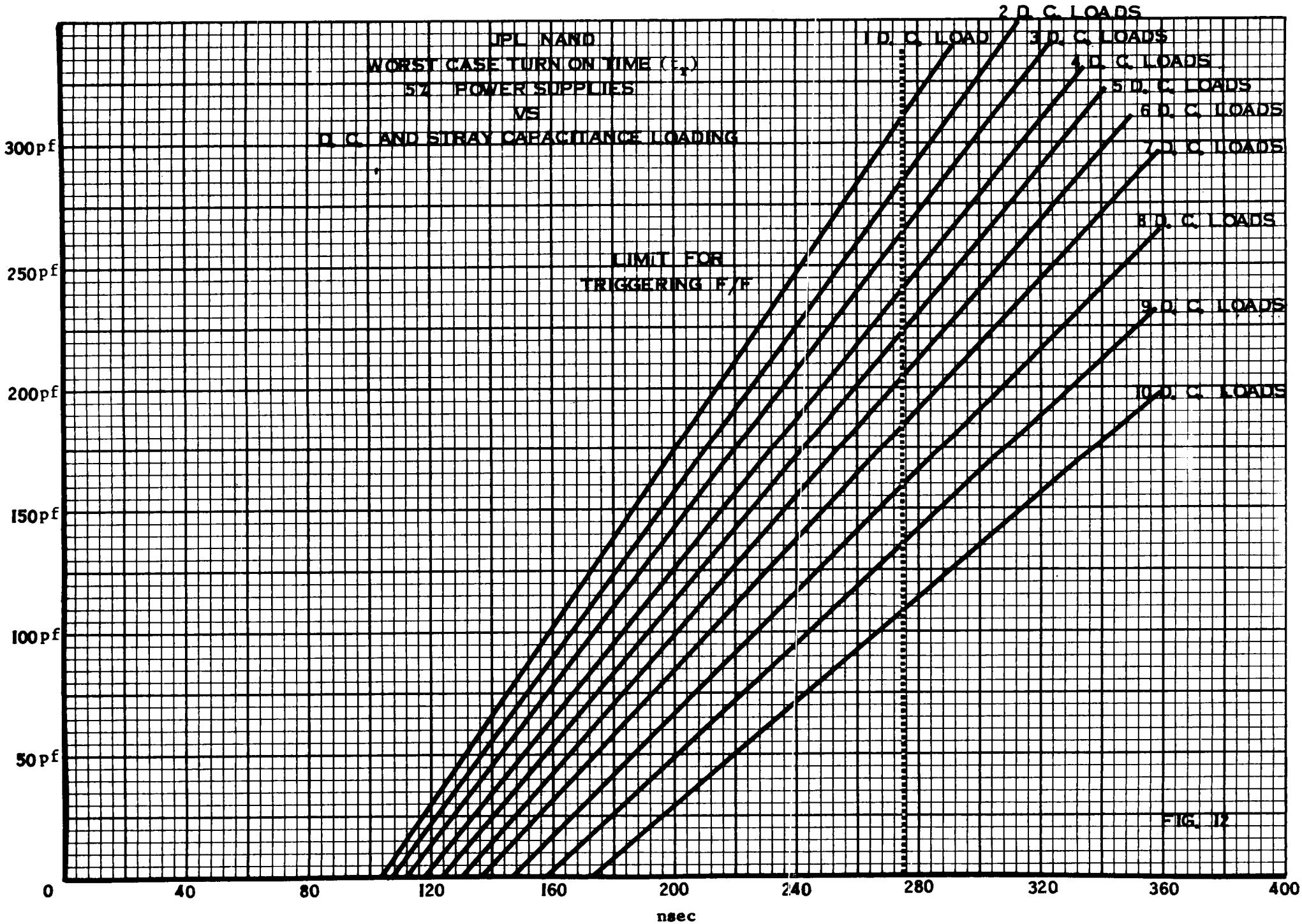

JPL NAND
WORST CASE TURN ON TIME (T_1)
5% POWER SUPPLIES
VS
D. C. AND STRAY CAPACITANCE LOADING
LIMIT FOR
TRIGGERING F/F
1 D. C. LOAD
2 D. C. LOADS
3 D. C. LOADS
4 D. C. LOADS
5 D. C. LOADS
6 D. C. LOADS
7 D. C. LOADS
8 D. C. LOADS
9 D. C. LOADS
10 D. C. LOADS
300pf
250pf
200pf
150pf
100pf
50pf
0
40
80
120
160
200
240
280
320
360
400
nsec

FIG. 12

t_r = 55 nsec. for four D.C. loads as calculated previously

$t_{od} = -23.9 \times 10^{-9} \ln 0.272$

$= 31.1$ nsec.

2. Worst Case (±15% Power Supplies)

Worst case occurs at low power supplies and low temperature.

$V_Q = 0.63 + 1.3 \times 10^{-3} \times 35 + 2 \times 0.55 + 2 \times 35 \times 2.0 \times 10^{-3} - 0.593$

$-35 \times 2.6 \times 10^{-3}$

$= 1.23v$

$$t_{od} = \frac{-t_r}{2.3} \ln 0.29 = 0.54\, t_r$$

$$t_{od} = \frac{0.785 \times 10^{-6} + 4.27 \times 10^{3}\, C_s}{\# + *} \ln \frac{261}{261 - 21 \times (\# + *)}$$

Figure 13 is a plot of worst case t_{od} versus D.C. and capacitive loading.

Note: t_s can be assumed negligible for total turn-off delay time since worst case occurs at minimum power supply voltages and low temperature.

3. Worst Case (±5% Power Supplies)

$V_Q = 1.23v$

$$t_{od} = \frac{-t_r}{2.3} \ln 0.259 = 0.587\, t_r$$

$$t_{od} = \frac{0.83 \times 10^{-6} + 4.6 \times 10^{3} \times C_s}{\# + *} \ln \frac{342}{342 - 24.2 \times (\# + *)}$$

Figure 14 is a plot of worst case D.C. and capacitive loading.

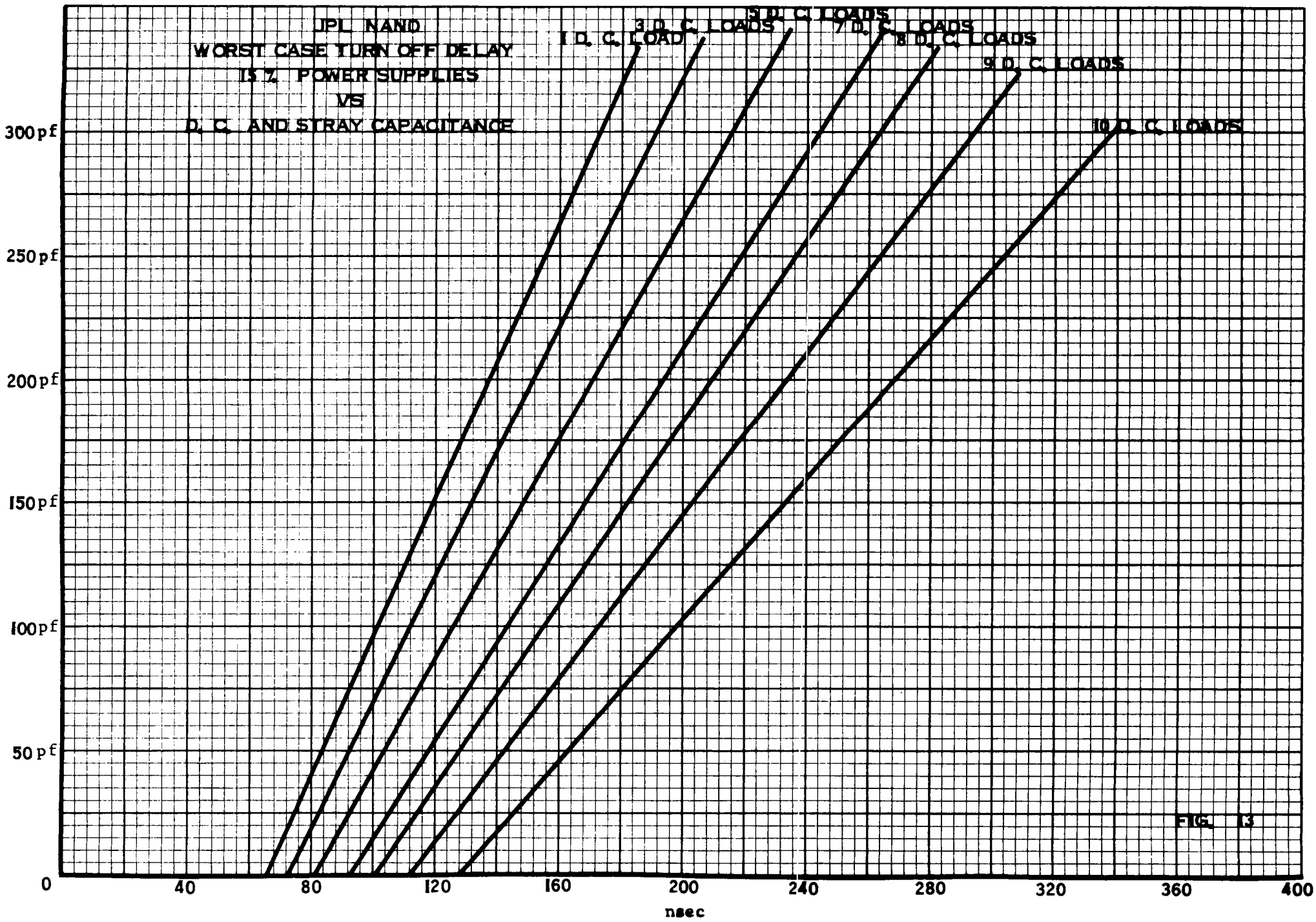

JPL NAND
WORST CASE TURN OFF DELAY
15 % POWER SUPPLIES
VS
D. C. AND STRAY CAPACITANCE
1 D. C. LOAD
3 D. C. LOADS
5 D. C. LOADS
7 D. C. LOADS
8 D. C. LOADS
9 D. C. LOADS
10 D. C. LOADS
300 pf
250 pf
200 pf
150 pf
100 pf
50 pf
0
40
80
120
160
200
240
280
320
360
400
nsec

FIG. 13

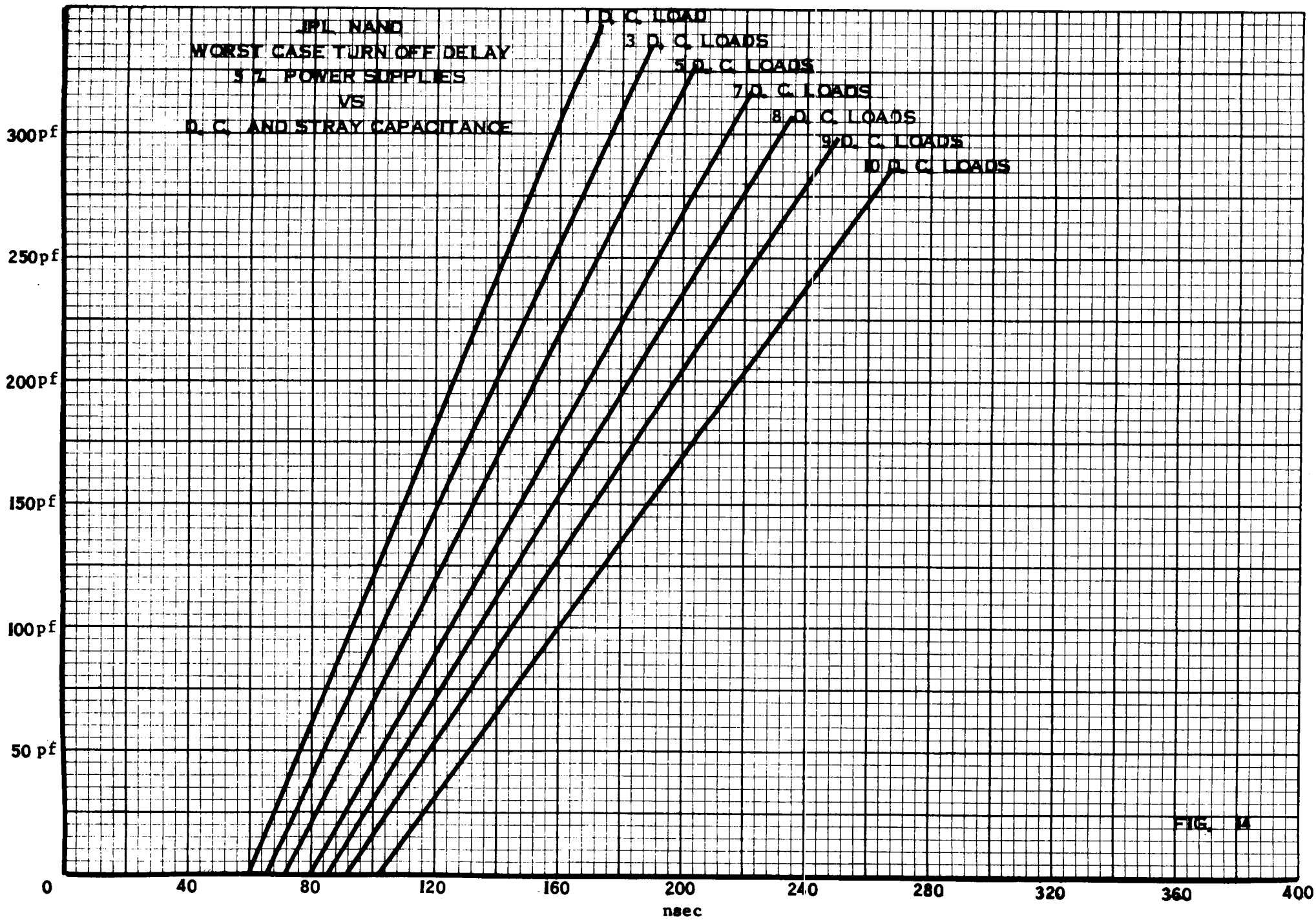

JPL NAND
WORST CASE TURN OFF DELAY
5 V. POWER SUPPLIES
VS
D. C. AND STRAY CAPACITANCE
1 D. C. LOAD
3 D. C. LOADS
5 D. C. LOADS
7 D. C. LOADS
8 D. C. LOADS
9 D. C. LOADS
10 D. C. LOADS
300pf
250pf
200pf
150pf
100pf
50 pf
0
40
80
120
160
200
240
280
320
360
400
nsec

FIG. 14

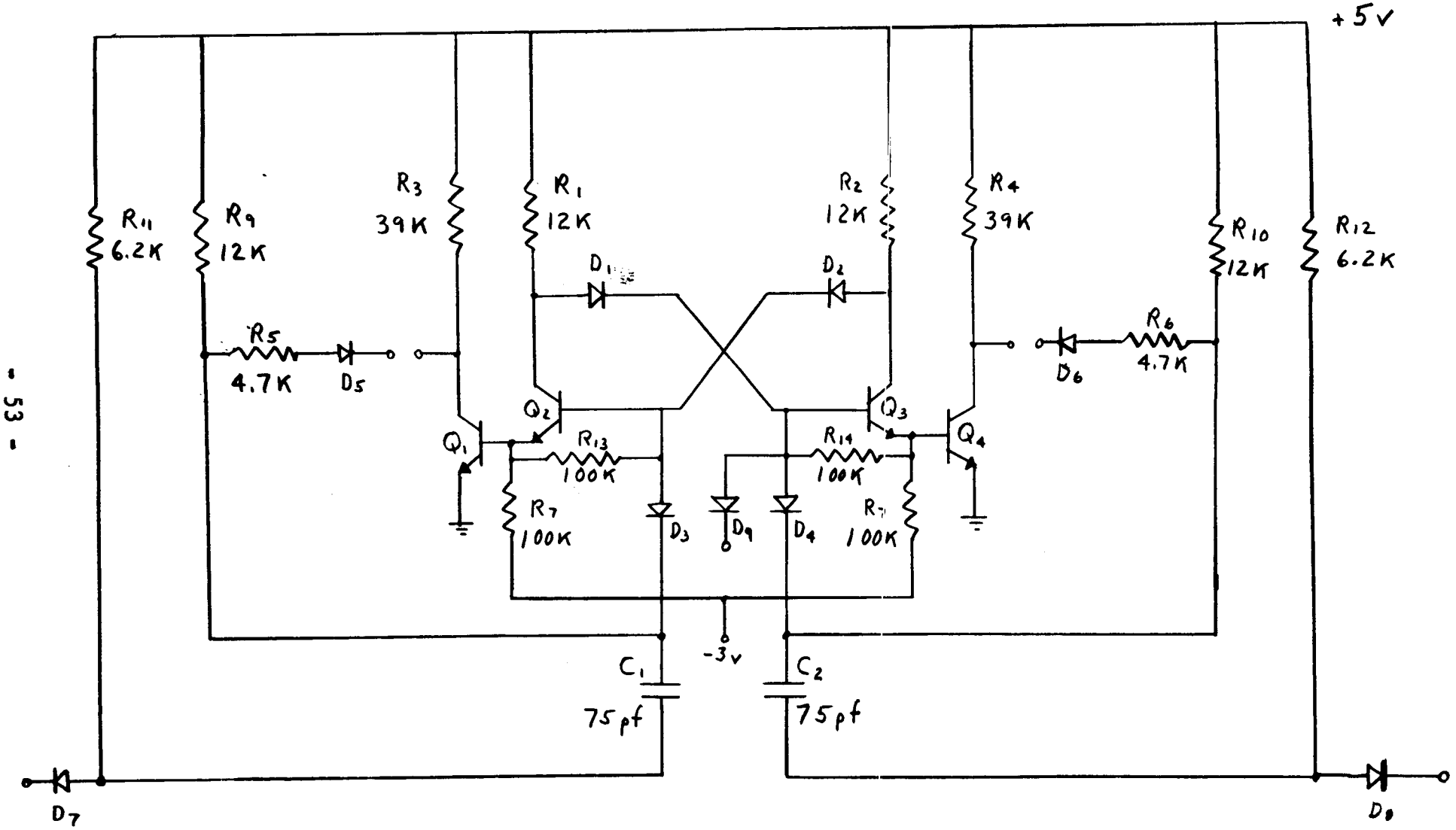
C. FLIP FLOP

General

The flip flop configuration is shown in Figure 15. Transistors Q_2 and Q_3 perform the flip flop memory function while transistors Q_1 and Q_4 buffer the internal flip flop from the output load. Cross coupling diodes D_1 and D_2 provide more efficient cross coupling than resistors. Diodes D_1 and D_2 could be eliminated except for the fact that the OFF condition of Q_1 or Q_4 could not be guaranteed under all operating conditions. For example, when Q_4 is OFF the bias on the base of Q_4, V_1 is determined by the difference

$$V_1 = (V_{be_1} + V_{ce_2}) - (V_{D_1} + V_{be_3}) \qquad \text{(Equation 10)}$$

V_{be_1} and V_{ce_2} are for the ON condition of Q_1 and Q_2, and V_{D_1} and V_{be_3} are for the simultaneous OFF condition at Q_4. At this time Q_3 operates as an emitter follower with R_8 performing the emitter current sink function. R_{14} guarantees a forward current through diode D_1 even for the worst case leakage current through D_4 at the highest operating temperature (+80°C), and a very high beta transistor for Q_3, i.e., $I_{b_3} \simeq 0 \mu a$. This forward current through D_1 guarantees a value for V_{D_1} which when entered in Equation 10 yields a value for V_1 less than +0.3 volts. If D_1 did cut off, the base of Q_3 could go more positive depending upon the leakage of D_4 and the beta of Q_3. The emitter of



Transistors 2N914
Diodes FD 643

Fig. 15

Q_3 would then follow and forward bias Q_4 to the point of conducting significant collector current.

A maximum of +0.3 volts on the base of Q_4 in the OFF condition was chosen on the basis of past experience with transistor V_{be} voltages and the measurements on the 2N914 transistor at very low collector currents shown in Table I. This table shows that at +80°C. V_{be} must be around +0.34 volts to support even 1 μ amps of collector current.

Triggering of the flip flop is accomplished by the negative edge of signals applied to the cathodes of D_7 and D_8 and D. C. resetting through diode D_9. Resistors R_6, R_{10} and R_5, R_9 provide voltage dividers so that if an enable signal exists at the cathode of D_5 or D_6, a threshold voltage exists at the cathode of D_3 of D_4. This threshold voltage provides a back bias across D_3 or D_4 which must be exceeded along with the diode forward drop before the input signal can trigger the base of Q_2 or Q_3. This provides noise immunity to spurious noise pulses existing on the input lines. Except when the D. C. reset signal is present, D_9 is back biased resulting in less than 1.5 pf for coupling noise from the reset line to the input of Q_3.

Resistors R_{11} and R_{12} pull up the anodes of D_7 or D_8 when the transistor supplying the input signal turns off.

1. F/F D. C. ANALYSIS

In the D. C. analysis it is assumed that the flip flop half containing Q_1 and Q_2 is ON and the half containing Q_3 and Q_4 is OFF. Figure 16 is the equivalent circuit for the flip flop with this assumption. The circuit elements along with the unknowns are shown on this diagram.

R_{13} and R_{14} were added later to the design when it was found that V_1 could be unpredictable, when considering the worst case of end of life, high temperature leakage of diode D_4, and high temperature high beta for transistor Q_3, i.e., I_{DL_4} could exceed I_{b_3} and therefore D_1 would not be biased on. The first computer run, whose main purpose was to obtain the bias currents of the transistors and diodes, was without these resistors. However, this has little or no effect on most of the unknowns. Its primary effect is that in the high temperature worst case it makes I_5 positive.

a. Computer Run #4 - 500 K. C. Flip Flop

The equations for the first flip flop computer solution are as follows:

$$I_1 = \frac{V_{cc} - V_{be1} - V_{ce_2}}{R_1} \tag{1}$$

$$I_2 = \frac{V_{cc} - V_{D_2} - V_{be_2} - V_{be_1}}{R_2} \tag{2}$$

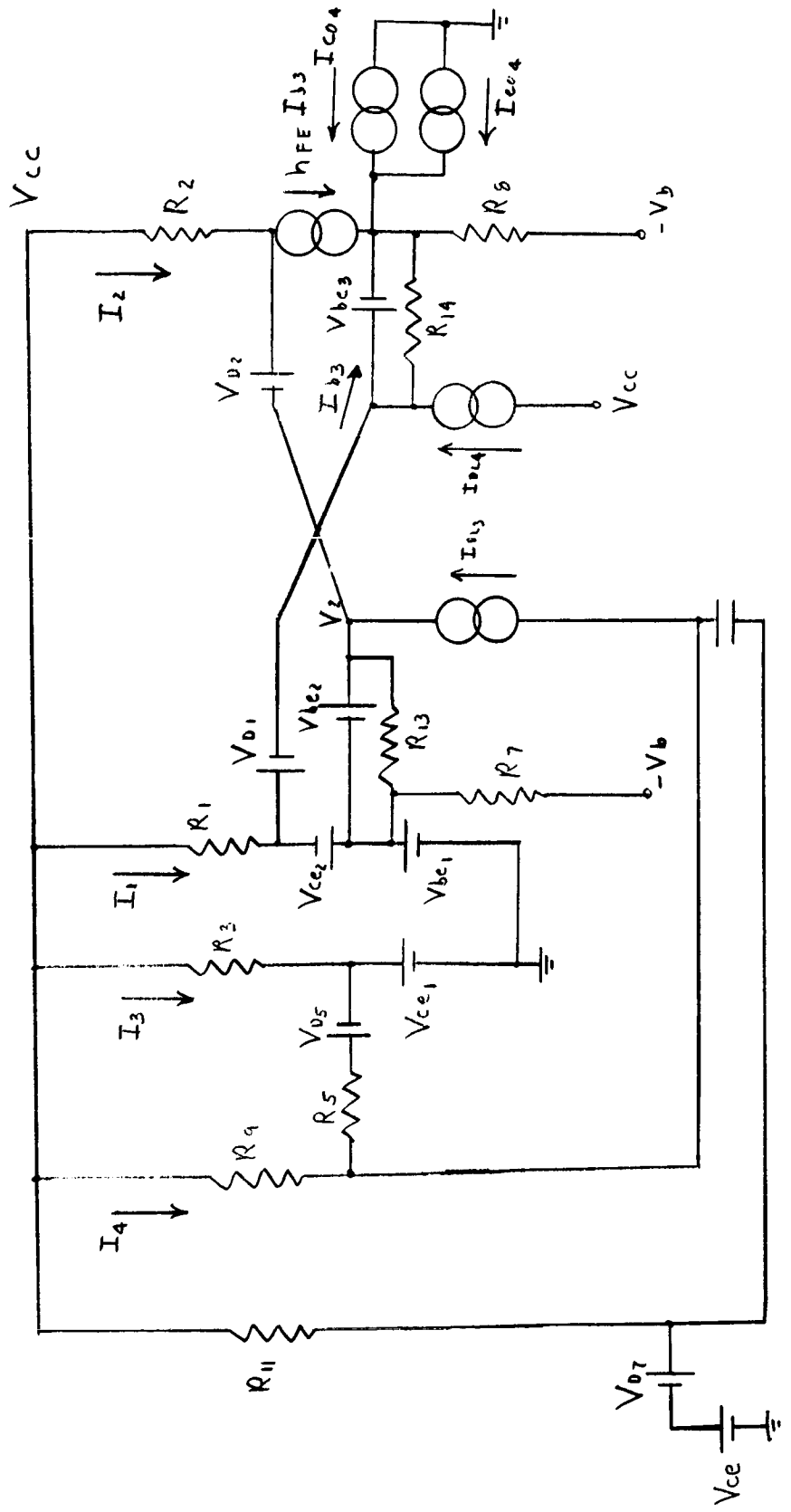

Vcc
R2
I2
hFE Ib3
Ico4
Ieo4
R6
-Vb
Vbc3
R14
VD2
Ib3
Vcc
IB4
IEb3
V2
VD1
Vbe2
R13
R7
-Vb
R1
I1
Vce2
Vbe1
R3
I3
VD5
Vce1
R5
R9
I4
R11
VD7
Vce

Figure 16

$$I_3 = \frac{V_{cc} - V_{ce_1}}{R_3} \tag{3}$$

$$I_4 = \frac{V_{cc} - V_{D_5} - V_{ce_1} + I_{DL_3} R_5}{R_5 + R_9} \tag{4}$$

$$I_5 = I_{b_3} - I_{DL_4} \tag{5}$$

$$I_{b_2} - I_2 = I_{DL_3} - h_{FE_3} I_{b_3} \tag{6}$$

$$I_{b_1} = I_1 - I_5 + I_{b_2} - \frac{V_b + V_{be_1}}{R_7} \tag{7}$$

$$V_2 = V_{be_1} + V_{be_2} \tag{8}$$

$$V_T = -I_{DL_3} R_5 + V_{D_5} + V_{ce_1} + R_5 I_4 \tag{9}$$

$$V_1 = V_{be_1} + V_{ce_2} - V_{D_1} - V_{be_3} \tag{10}$$

$$I_o = h_{FE_1} I_{b_1} - I_3 - I_4 + I_{DL_3} \tag{11}$$

$$P = V_{cc} (I_1 + I_2 + I_3 + I_4 + I_{co_4} + I_{DL_4}) + \frac{V_{cc} (V_{cc} - V_{ce_1} - V_{D_7})}{R_{11}} + \frac{V_b (V_1 + V_b)}{R_8} + \frac{V_b (V_{be_1} + V_b)}{R_7} \tag{12}$$

$$I_{b_3} = \frac{1}{h_{FE_3} + 1} \left[\frac{V_b + V_{be_1} + V_{ce\ 2} - V_{D_1}}{R_8} - V_{be_3} - I_{co_4} - I_{eo_4} \right] \tag{13}$$

The unknown currents in the solution were needed for determining the deliverable output current at the output of the flip flop, the total dissipated power, and the flip flop transient response. The voltages solved for were used for determining the bias, V_1 on Q_4, the triggering threshold voltages, V_T, and V_2.

The part assumptions and first computer run are shown in Appendix C - Computer Run #4. The part parameters are given a Nominal value, Minimum value and Maximum value at 25°C which is largely a function of part manufacturing tolerance and end of life degradation. Also where there is a strong part temperature dependence as for transistor V_{be}, betas and diode forward voltages, a term is added to the parameter to take this into account. For instance, V_{D_1}, the forward voltage across diode D_1 is expressed in the computer equations as:

$$V_{D_1} = V_{D_{1N}} - T.\ C._1\ (T - 35)$$

$V_{D_{1N}}$ is the forward diode drop for that particular diode at its bias current at 25°C. It is inserted into the computer with a maximum, minimum and nominal value. $T.\ C._1$ is the temperature coefficient of diode D_1 at its bias current. It is also given a minimum, maximum and nominal value. T is temperature plus ten degrees centigrade. From the formula it can be seen that at 25°C, $V_{D_1} = V_{D_{1N}}$.

This first computer run was for a ±15% power supply, and ±3% resistors. The assumptions for the betas of the output transistors

Q_1 and Q_4 were the same as for the Nand since the transistor operating points are about the same for both circuits.

Nominal Solutions

I_o = 28.6 ma.

P = 8.7 mw.

V_1 = +0.05 volts

V_T = 1.96 volts

V_2 = 1.48 volts

$I_{c_2} \simeq I_1$ = 0.34 ma.

I_{b_2} = 0.22 ma.

I_{b_1} = 0.53 ma.

I_{b_3} = 1.8 μa.

The first computer run besides giving the operating currents for the transistors and diodes, showed that in the worst case I_5 could be negative as mentioned previously. It also showed that the nominal flip flop dissipated power would be about 8.7 mw with a maximum of 12.9 mw and a minimum of 5.5 mw. The wide range in power being mostly a function of the wide power supply tolerances assumed, i.e., $\pm$15%.

b. Final Computer Analyses - Flip Flop

The equations from the first computer analysis were modified to include R_{13} and R_{14} and in a few cases modified to make the terms in the equations shorter. Some difficulty encountered with the computer

was traced to overloading the computer memory with too many items per term in one or two of the equations. All computer analysis except for the first, use ±4% resistor tolerances. The ±4% includes initial temperature and end of life tolerance.

The final equations are as follows:

$$I_1 = \frac{V_{cc} - V_{be_1} - V_{ce_2}}{R_1} \tag{1}$$

$$I_2 = \frac{V_{cc} - V_{D_2} - V_{be_2} - V_{b1}}{R_1^*} \tag{2}$$

$$I_3 = \frac{V_{cc} - V_{ce_1}}{R_3} \tag{3}$$

$$I_4 = \frac{V_{cc} - V_{D_5} - V_{ce_1} + I_{DL_3} R_5}{R_5 + R_9} \tag{4}$$

$$I_5 = I_{b_3} - I_{DL_4} + \frac{V_{be_3}}{R_{14}} \tag{5}$$

$$I_{b_2} = I_2 + I_{DL_3} - h_{FE_3} I_{b_3} - \frac{V_{be_2}}{R_{13}} \tag{6}$$

$$I_{b_1} = I_1 - I_5 + I_{b_2} + \frac{V_{be_2}}{R_{13}} - \frac{V_b + V_{be_1}}{R_7} \tag{7}$$

$$V_2 = V_{be_1} + V_{be_2} \tag{8}$$

$$V_T = -I_{DL_3} R_5 + V_{D_5} + V_{ce_1} + R_5 I_4 \tag{9}$$

$$V_1 = V_{be_1} + V_{ce_2} - V_{D_1} - V_{be_3} \tag{10}$$

---

*Actually R_2.

$$I_o = h_{FE_1} I_{b_1} - I_3 - I_4 + I_{DL_3} \tag{11}$$

$$P = V_{cc} (I_1 + I_2 + I_3 + I_4 + I_{co_4} + I_{DL_4}) +$$

$$\frac{V_{cc} (V_{cc} - V_{ce_1} - V_{D_7})}{R_{11}} + \frac{V_b (V_1 + V_b)}{R_8} + \frac{V_b (V_{be_1} + V_b)}{R_{8\ (7)*}}$$

$$I_{b_3} = \frac{1}{h_{FE_3} + 1} \left[\frac{V_b + V_{be_1} + V_{ce_2} - V_{D_1} - V_{be_3}}{R_8} - \right. \tag{12}$$

$$\left. I_{co_4} - I_{eo_4} - I_{R14} \right] \tag{13}$$

i. Computer Run #5 - 500 K. C. ±15% Power Supplies - Conclusions

Appendix C - Computer Run #5 contains the determination of diode and transistor parameters. The bias currents in general were taken from the first computer analysis and the actual values for the parameters at these bias points either from measured data Tables I through IV, Appendix D, the plotted transistor saturation characteristics, Appendix D, Fairchild specifications and application curves, or special specifications that will be placed on the device, such as the beta of the 2N914 transistor. All resistors were given a ±4% tolerance including initial, temperature, and end of life drift tolerance. Appendix C - Computer Run #5 is the computer analysis using these part parameters

*Actually R_7.

and ±15% power supplies.

1. Nominal Solutions

I_o = 29.3 ma.

P = 8.5 mw.

V_1 = 0.07 volts

V_T = 1.92 volts

V_2 = 1.42 volts

2. Minimum I_o is 6.8 ma.

3. I_{in} of the Nand under the same condition is <600 μa. Therefore the F/F can drive ten Nand loads.

4. Maximum power is computed as 12.8 mw, an increase of about 50% over the nominal power. This is understandable since maximum power is at maximum power supply voltages. A 15% increase in power supply voltage will result in over a 30% increase in power dissipation.

5. V_1 maximum, the OFF bias on the base of Q_4 computed as a maximum of 0.294 volts. The data Table I - Appendix D shows this to be adequate to guarantee that Q_4 will be in the OFF condition.

6. V_T - V_2 plus the forward voltage drop across D_3 must be exceeded to pull most of the I_{b_2} current (since Q_2 is so heavily saturated) through D_3. This gives the flip flop noise immunity voltage to noise pulses on the input lines. The maximum computed V_T would occur under the same conditions as that for the maximum V_2, i.e., minimum temperature, maximum I_{b_1}, I_{b_2}, V_{ce_1}, V_{cc}, and I_o. Conversely the minimums would

occur at maximum temperature, minimum I_{b1}, I_{b2}, V_{ce}, V_{cc} and I_o. Therefore, noise immunity voltage, V_{NI}, using the maximum values for V_T and V_2 is:

$$V_{NI} = V_{T_{max}} - V_{2max} + V_{D3}$$

$$= 2.3 \text{ volts} - 1.7 \text{ volts} + 0.6^* = 1.2 \text{ volts}$$

Noise immunity voltage using the minimum V_T and V_2 voltages is

$$V_{NI} = 1.5 \text{ volts} - 1.2 \text{ volts} + 0.3 \text{ volts}^{**} = 0.6 \text{ volts}$$

Since V_2 is a function of two diode drops versus only one diode drop for V_T, and V_T is mostly a function of V_{cc} and the divider R_5 and R_9, the above two values for V_{NI} are not the worst case. Worst case would occur at minimum, temperature, V_{cc}, I_o, R_5 and maximum R_9. Under these conditions V_T would be calculated as follows: Minimum I_4 from computer run is 0.2 ma. Then at 0.2 ma,

$$V_{D5} = 0.46 \text{ volts} + 2.5 \text{ mv/}^\circ\text{C} \times 35^\circ = 0.6 \text{ volts}$$

V_{ce_1} = 0.1 volts @ I_o of one load (normal offset voltage of 2N914 is about 80 mv)

$\underline{R_5} = 4.7 \text{ K} \times 0.96 = 4.5 \text{ K}$

$V_T = V_{D5} + \underline{V_{ce1}} + \underline{I_4}\ \underline{R_5}$

$= 0.6 \text{ volts} + 0.1 \text{ volts} + 0.2 \text{ ma} \times 4.5 \text{ K}$

$= +1.6 \text{ volts}$

---

*$I_{D_3} \approx \overline{I_{b_2}} = 0.37$ ma. From Fairchild curves $V_{D3} = 0.5$ volts + 2.3 mv/°C x 35.

**$I_{D_3} \approx I_{b_2} = 0.12$ ma and @ +80°C. From Fairchild curves, $V_{D_3} = 0.44$ v - 2.8 mv/°C x 55.

Under the same conditions V_2 is as follows. The minimum value of V_2 is the value required here except for the fact that it occurs at maximum temperature. Multiplying the maximum temperature coefficient for V_{be1} and V_{be2} times the difference in temperature from +80°C to -10°C and adding this to the minimum V_2 from the computer runs results in the sought for value of V_2. Then V_2 = 1.2 volts + 2 x 2.5 mv/°C x 90° = 1.6 volts. The minimum I_{b2} from the computer run is 0.12 ma. At low temperature then V_{D_3} is 0.44 v + 2.55 mv/°C x 35°C = 0.53 volts at a current of 0.12 ma. The worst case V_{NI} is then

$$V_{NI} = 1.6 \text{ volts} - 1.6 \text{ volts} + 0.5 \text{ volts}$$

$$= 0.5 \text{ volts}$$

To trigger the flip flop it will actually take a larger noise voltage at the input when it is considered that a noise pulse will not have a 0.0 μ sec rise time and will therefore be attenuated through the capacitor C_1.*

ii. Computer Run #6 - 500 K. C. ±5% Power Supplies - Conclusions

Appendix C - Computer Run # contains the 500 K. C. flip flop analysis with a ±5% tolerance on the +5 volt and -3 volt power supplies.

1. The nominal solution will be the same as the previously discussed computer analysis since none of the nominal parameters were changed.

*Table V contains laboratory measurements of V_2 and V_T over the temperature range (-10°C to +80°C), the power supply voltage range (±15%) and minimum and maximum output load conditions. The measurements show at least a 0.2 volt back bias across the diodes (D_3 or D_4) under all conditions. This results in a V_{NI} of about 0.7 volts (measured worst case) at the flip flop side of the input capacitors.

2. Minimum I_o is 8.7 ma.

3. Maximum power in this case is 10.6 mw. This is 2 mw above the nominal power dissipation (8.5 mw).

4. V_1 the OFF bias on the base of Q_4 computes as in the previous computer analysis since the diode operating points were not changed from the previous run. Actually the limits on V_1 for a $\pm$5% power supply will be narrower than for the $\pm$15% analysis is since the current range through the bases of transistors Q_1 and Q_2 will be narrower. This will result in an even safer worst case V_1, i.e., V_1 will be somewhat less positive than the previously computed +0.294 volts.

5. $V_{NI} = V_{T_{max}} - V_{2_{max}} + V_{D3}$ (using maximum values)

$= 2.1$ volts $- 1.7$ volts $+ 0.6$ volts

$= 0.7$ volts

$V_{NI} = V_{T_{min}} - V_{2_{min}} + V_{D3}$

$= 1.6$ volts $- 1.2$ volts $+ 0.3$ volts

$= 0.7$ volts

The worst V_{NI} for a $\pm$5% power supply will be close to the 0.7 volts value computed above, therefore the calculation will not be performed as it was in i. Even in i for a $\pm$15% power supply the V_{NI} computed for minimum V_T and V_2 was within 0.1 volt of the worst case minimum.

65 K. C. Flip Flop

To save power in applications not requiring a 500 K. C. repetition rate in a flip flop, the conditioning resistors R_5, R_9, R_{11} and R_6, R_{10}, R_{12} were increased in value. The ratio of R_5 to R_9 and R_6 to R_{10} were kept the same as before so that the triggering analysis performed for the 500 K. C. flip flop would change very little. Actually since the equivalent resistance on the flip flop input side of C_1 and C_2 has increased substantially triggering is even more certain.

R_9 and R_{10} were set equal to 100 K (since 100 K resistors are already used in the Flip Flop and Nand). Then for the same ratio as before between R_9 and R_5, $R_5 = \frac{100}{120} \times 47\ K = 39.2\ K = R_6$, R_{11} and R_{12} were set at 39 K, since 39 K resistors are used elsewhere and the saving in power in going from 39 K to 62 K is only about 0.2 mw.

iii. Computer Run #7 - 65 K. C. Flip Flop ±15% Power Supplies - Conclusions

The equations and part parameters except for changes in the values of the conditioning resistors were the same as used for the 500 K. C. computer analyses.

1. Nominal Solutions

I_o = 29.5 ma

P = 4.5 mw (Compared to 8.5 mw for 500 K. C. flip flop)

V_1 = 0.07 volts (Same as previous analyses nothing changed to alter V_1)

V_T = 1.9 volts (Same as previous ratio of R_5 to R_9 was not changed)

V_2 = 1.4 volts (Same as previous ratio of R_5 to R_9 was not changed)

2. Minimum I_o is 7.0 ma. As expected this is only slightly above 500 K. C. value of 6.8 ma (increasing conditioning resistors requires less current from buffers Q_1 and Q_4).

3. Maximum power is 6.9 mw compared to 12.8 mw for 500 K. C. flip flop. Minimum power at minimum power supply voltages is 2.8 mw.

4. V_1, computed at 0.29 volts as before since no internal changes were made to the flip flop.

5. The values for the noise immunity voltages, V_{NI} will be the same as for the 500 K. C. computation with ±15% power supply.

iv. Computer Run #8 - 65 K. C. Flip Flop ±5% Power Supplies

The equations and part parameters except for the values of the conditioning resistors were the same as used for the 500 K. C. computer analyses.

Nominal Solutions

The nominal solutions will be the same as the nominal solutions for the 65 K. C. computer analysis ±15% power shown in iv.

Minimum I_o is 8.9 ma.

Maximum power dissipation is 5.7 mw.

2. FLIP FLOP TRANSIENT ANALYSIS

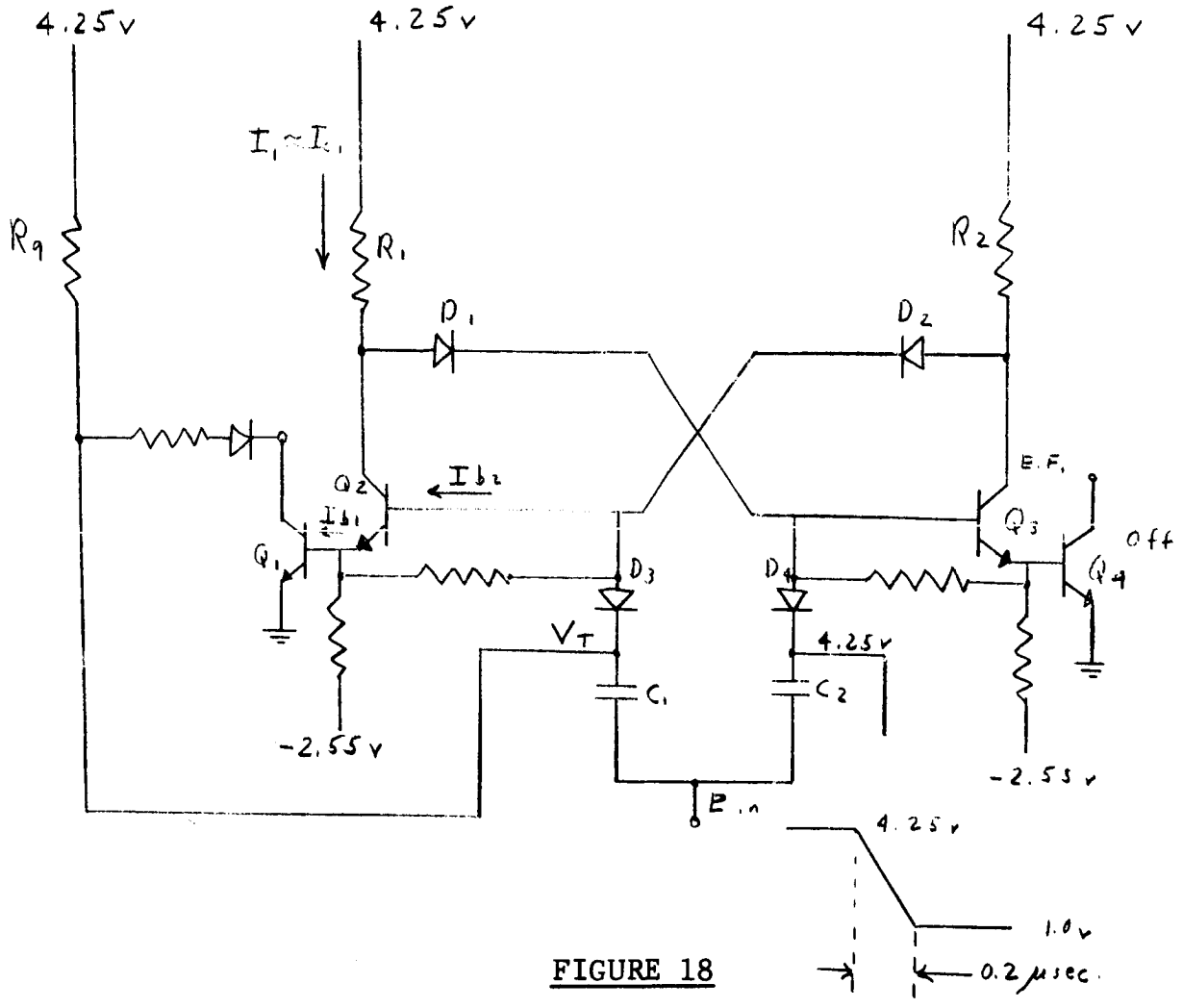


FIGURE 18

General

The transient analysis of the flip flop is divided into two parts, a determination of the loop time* of the flip flop containing

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*Loop Time - is defined as the time interval between the start of a triggering signal (turn off) at the base of the flip flop ON transistor to a point in time where the input signal could end and the opposite transistor of the internal flip flop would be guaranteed to go from the active to the saturated state.

Loop time is of importance because it gives the minimum amount of time the input signal must pull down the input of the transistor being turned off if the flip flop is to change state.

transistors Q_2 and Q_3; and the delay, rise, storage and fall times of the output buffer stages Q_1 and Q_4.

a. Inner F/F

i. Calculation of I_{B_2}

The maximum flip flop loop time analysis starts by assuming transistors Q_1 and Q_2 are saturated (ON), Q_3 is acting as an emitter follower and Q_4 is in the OFF state. The power supplies are assumed to be at their low values, i.e., 5 volt supply, at 4.25 volts and the ambient temperature at -10°C. The reasons for these choices are that transistor currents are smallest at low power supply voltages, therefore, in general, circuit speeds decrease and at the low temperature, beta is lowest and V_{be} drops are highest, both tending to decrease circuit transient response. As the input swings from +4.25 v to +1.0 v, D_4 does not conduct, it remains reverse biased because the steering voltage is at its high level. D_3 becomes forward biased and conducts. It diverts the base current, I_{b_2} from Q_2 and supplies a reverse turn off current (I_{B_2}) to Q_2. Besides just diverting I_{b_2} from Q_2, E_{in} also pulls down the collector of Q_3 through diode D_2. The importance of this point will become more evident when the turn on time of Q_3 is determined. To calculate the minimum value of I_{B_2}, it will be necessary to determine the minimum current through C_1, I_{c_1}, and subtract the maximum I_{b_2} and the maximum current through the steering resistor R_9 at low power supply

voltages and low temperature. The minimum current through C_1 for a ramp E_{in} voltage with a 0.2 μsec fall time is

$$I_{C1} = \frac{\Delta Q}{\Delta t} = C_1 \cdot \frac{\Delta V}{\Delta t} = 71.2 \times 10^{-12} \times \frac{3.25 \text{ v}}{0.2 \times 10^{-6} \text{ sec}}$$

$$= 1.16 \text{ ma}$$

(Note: This is true when a voltage source drives the capacitor and a low impedance sink exists on the other side.)

The maximum current through R_9 during storage time is

$$I_{R9} = \frac{4.25 \text{ v} - (1.7 \text{ v} - 0.7 \text{ v})}{11.5 \text{ K}}$$

$$= 0.283 \text{ ma}$$

From the $\pm$15% power supply computer run (7/10/64)

$$I_{b2} = 0.12 \text{ ma}$$

This minimum occurs at low power supply voltages, low temperature (V_{be}, V_{D2} and V_{be2} maximum) and R_2 maximum. To get I_{b2} maximum at low temperature and low power supply, R_2 should be minimum. If I_{b2} is multiplied x 1.08, this is accomplished. Also initial tolerances on V_{be1}, V_{D2} and V_{be2} should be minimum rather than maximum in the computer solution. This results in an additional voltage across R_2 of 0.16 v for V_{be1}, 0.05 v for V_{be2}, and 0.16 v for V_{D2}. The resultant increase in I_{b2} is $\frac{0.37 \text{ v}}{11.6 \text{ K}} = 0.03$ ma.

Maximum I_{b2} at low temperature and low power supply voltage is then,

$$I_{b_2} = 0.12 \times 1.08 + 0.03 \text{ ma}$$

$$= 0.16 \text{ ma}$$

The turn off current I_{B_2} is then

$$I_{B_2} = I_{C_1} - I_{R9} - I_{b_2}$$

$$= 1.16 \text{ ma} - 0.28 \text{ ma} - 0.16 \text{ ma}$$

$$= 0.72 \text{ ma}$$

ii. Storage Time Calculation for Q_2

$$t_s = \frac{\tau_s}{0.69} \ln \frac{I_{b_1} + I_{B_2}}{I_{bs} + I_{B_2}} \quad \text{(from Appendix E)} \quad I_{b_1} = I_{b_2}$$

$$= \frac{20}{0.69} \ln \frac{0.16 + 0.72}{0.0 + 0.72} \qquad I_{B_2} = I_{B_2}$$

$$= \frac{20}{0.69} \ln \frac{0.88}{0.72} \qquad I_{bs} = \frac{I_{c2}}{h_{FE}} = \frac{I_1}{h_{FE}}$$

$$= \frac{0.26}{100} = .003$$

$$= 5.8 \text{ n sec}$$

$$\approx 0.0$$

The value for t_s, 5.8 n sec, was calculated on the basis of a constant reverse current I_{B_2}. However, as was shown in the flip flop triggering analysis for a 0.2 μsec, input at low temperature and low power supply, the time required in the worst case, from the start of pulling current away from the base of Q_2 until all of the current through R_2 is diverted through D_3 is approximately 42 n sec. Since during this 42 n sec, V_2 is decreasing as I_{b_2} is decreasing to zero fairly uniformly,

and 42 n sec is considerably longer than the computed 5.8 n sec for t_s, then t_s can be neglected as a factor in determining flip flop loop time. Looking at it from the standpoint of worst than worst case, since at the end of the 42 n sec, (if there were a stored base charge V_2 would remain practically constant), close to the full I_{B_2} i.e., 0.72 ma would be applied and the 5.8 n sec t_s would apply. It is felt that the worst than worst case just cited should not be applied here.

iii. Turn Off Time Calculation for Q_2

Q_2 is heavily saturated $I_{b_2} \approx \frac{2}{3} I_{c2}$ ($I_{c_2} = I_1$ from computer run). Therefore, during the 42 n sec period in which I_{b_2} is diverted, little turn OFF charge can be assumed to be taken from the base of Q_2.

This is true because the 42 n sec is practically over before Q_2 starts to come out of saturation i.e., it takes very little base current to saturate Q_2, $I_{bs_2} \ll I_{b_2}$. Therefore, the current pulled through D_3 must practically equal the initial I_{b_2} before Q_2 begins to turn OFF. Furthermore, at the end of the 42 n sec, V_2 is at +1.4 v which is sufficiently low to guarantee no base current through Q_2 at $-10^{o}C$ as shown by part data Appendix D. This means that at the end of this 42 n sec for all practical purposes, the only thing determining fall time is the response of the collector and collector circuit. The following will discuss in more detail, the reasons for this last statement.

Initially, when Q_2 is fully biased on, Q_2 is driven well into saturation as stated previously. This being the case, the equation

for fall time would be $t_f = \frac{Q_b + Q_c}{I_{B_2} + 0.5\ I_{bs}}$, assuming a constant I_{B_2}.

If it is assumed in the worst case that the charge Q_b is not removed until after the 42 n sec have elapsed, then the time, t_{fQb}, to clear out Q_b is calculated as follows:

$$Q_b = \frac{1.2\ I_c}{2\ \pi\ f_t} = \frac{1.2\ (0.3)\ (10^{-3})}{(2)\ (3.14)\ (25)\ (10^6)}$$

$$= 2.3 \times 10^{-12} \text{ coulombs}$$

$$t_{fQb} = \frac{Q_b}{I_{B_2}} = \frac{2.3 \times 10^{-12}}{0.85 \times 10^{-3}} = 2.7 \text{ n sec}$$

This term is quite small compared to the collector circuit component of t_f as will be shown and can therefore be omitted.

Considering the collector circuit as it affects t_f, the equivalent circuit would be as follows:

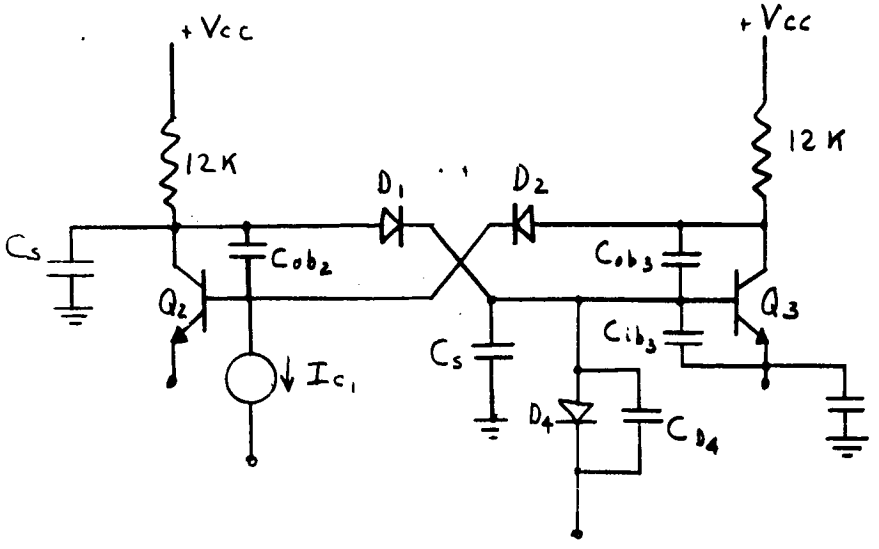


FIGURE 19

Since the base of Q_3 is initially forward biased (emitter follower), the voltage across the base to emitter junction changes only a couple tenths of a volt when Q_3 is brought into saturation. This being the case, the effect of C_{ib_3} can be neglected. Also, capacitance on the emitter of Q_3 can be neglected since it is attenuated by h_{FE_3}. C_{ob_2} is approximately 8 pf which is the average capacitance as V_{C_2} goes from the ON condition to about +2 volts in the OFF condition, (from the Fairchild 2N914 data sheet curves, Input and Output Capacitance vs. Reverse Bias Voltage). For C_{ob_3}, if we assume in the worst case that the input signal remains at the base of Q_2 for the full turn off time of Q_2 then C_{ob_3} must be charged. Since D_2 is forward biased by the trigger signal, this makes the collector of Q_3 look like a low impedance, i.e., the input signal is from a low impedance source. From the Fairchild 2N914 data sheet curves for C_{ob}, C_{ob_3} @ 0.4 v is about 9 pf. A V_{cb} of 0.4 v was chosen since the 0.2 sec voltage fall time input pulls the collector of Q_3 down to about +1.3 volts while the base of Q_3 is at about +0.5 volts. The initial difference, V_{cb_3}, is then about 1.3 - 0.5 = 0.8 v. As V_{c_2} increases, V_{cb_3} decreases to 0 volts after which the collector becomes forward biased. The average V_{cb_3} during this interval is then about 0.4 volts. Diode D_4 has a back bias of approximately 1 volt. From the FDS-6 curves from Fairchild the maximum diode capacitance is approximately 2 pf. If it is assumed that the packaging results in a stray capacitance, C_s, of 5 pf then the total

capacitance $C_T = C_S + C_{ob_2} + C_{ob_3} + C_{D_4}$

$= 5 \text{ pf} + 8 \text{ pf} + 9 \text{ pf} + 2 \text{ pf}$

$= 24 \text{ pf}$

The time constant of the collector circuit for turn off is then

$$\text{T. C.} = R\, C_T = 12.5 \times 10^3 \times 24 \times 10^{-12}$$

$$= 300 \times 10^{-9} \text{ sec}$$

At low temperature (-10°C), the collector of Q_2 rises from +1.0 volt to +2.0 volts before being clamped, i.e., from 20% to 40% of the applied 5 volts. Referring to a standard time constant chart, it can be seen that this requires 0.3 T, C. The time required for the collector of Q_2 to reach its final 2 volt value is then,

$$t_f = 0.3 \times 300 \times 10^{-9} \text{ sec} = 90 \text{ n sec}$$

Good correlation was obtained in laboratory measurements between this number and the measures t_f. Subtracting out the effect of the scope probe capacitance the laboratory measurement indicated a t_f on the breadboard of 100 n sec.

Returning again to consideration of how long an input trigger signal must hold the triggered base off for a guaranteed change in state of the flip flop, if the input signal at Q_2 base should vanish after the 42 n sec time discussed previously with reference to triggering, the collectors of both transistors would be down and would both rise with a time constant as determined in the t_f calculations. The transistor

with the best combination of smallest collector voltage, lower V_{eb}, lower beta, etc., would charge up fastest to the point of supplying base current to its opposite which would then regenerate and cause the flip flop to set, with the transistor being in the OFF conditions having the best combination of parameters just listed. It can now be seen that the end of the 42 n sec period is the flip flop uncertainty point. If the input signal were to end there, the state of the flip flop would be unpredictable in the worst case. It was shown that the worst case fall time of Q_2 was 90 n sec. If we allow a mismatch of up to 30% in collector and stray capacitance, 8% in resistor mismatch and mismatch of 0.2 v in initial V_c voltage ($\frac{0.2\ v}{5\ v}$ = .04 $\cong$ .04 T. C.), the time to charge fully (assuming that one side, Q_2 has a T. C. of 188 n sec ie, C_{ob_3} drops out) is for Q_3; t_f = 0.3 x 188 n sec x .62 = 35 n sec for Q_2; t_f = 0.3 x 188 n sec x 1.04 = 59 n sec.

Δt_f = 59 n sec. - 35 n sec = 24 n sec.

This says that in the worst case the trigger should hold down the previously ON base for at least 24 n sec past the 42 n sec previously discussed, to guarantee triggering the flip flop.

b. Transient Analysis Flip Flop Buffer Stages

i. Storage Time

The time required to pull out the stored charge is given by,

$$t_s = t_b \ln \frac{I_{b_1} + I_{b_2}}{I_{b_2} + I_{bs}}$$

Nominal Case

Using the flip flop computer analysis, Appendix C - Computer Run #5, for the nominal values of all parameters,

$$I_{b_1} = 0.54 \text{ ma}$$

$$I_{B_2} = \frac{3.7 \text{ v}}{100 \text{ K}\Omega} = 37 \ \mu\text{a} \approx 0.04 \text{ ma}$$

$$h_{FE} = 55$$

$$I_{bs} = \frac{I_3 + I_4 + 4 \text{ Nand Loads}}{h_{FE}} = \frac{.12 \text{ ma} + .26 \text{ ma} + 4 \times .66 \text{ ma}}{55}$$

$$= 55 \text{ ma} \approx 0.05 \text{ ma}$$

$$t_b = T_s < 13 \text{ n sec (from 2N914 specification sheet)}$$

$$t_s = 13 \times 10^{-9} \ln \frac{0.54 + 0.04}{0.04 + 0.05} = 24 \text{ n sec}$$

Observed value in the laboratory = 35 n sec.

Worst Case (±15% Power Supplied)

$$t_s = \frac{\tau_s}{0.69} \ln \frac{I_{b_1} + I_{B_2}}{I_{bs} + I_{B_2}}$$

Worst case occurs at maximum V_{cc}, minimum V_b and high temperature. (Parameter values from Appendix C - F/F Computer Analysis.)

τ_s = 20 n sec (from 2N914 specification sheet)

I_{b_1} = 0.78 ma

$I_{B_2} = \frac{2.55\ v + 0.51\ v}{104\ K} = 29 \mu a$

$\overline{h_{FE_1}} = 120 + 120 \times 55 \times 0.009 = 179.5$

$I_{\underline{bs}} \approx \frac{I_3 + I_4 + 1\ \text{Nand Load}}{\overline{h_{FE}}} = \frac{0.15 + 0.34 + 0.79}{179.5}$

$= 7.1 \mu a$

$t_s < \frac{20 \times 10^{-9}}{0.69} \ln \frac{0.78 + .029}{0.007 + .029} = 29 \times 10^{-9} \ln 22.4$

$t_s < 87$ n sec

Worst Case (±5% Power Supplies)

τ_s = 20 n sec

$\overline{I_{b_1}}$ = 0.68 ma

I_{B_2} = 32 μa

$I_{\underline{bs}} = \frac{0.14\ ma + 0.29\ ma + 0.71\ ma}{179.5} = 6 \mu a$

$t_s = 29 \times 10^{-9} \ln \frac{0.68 + 0.032}{0.006 + 0.032}$

t_s = 84 n sec

ii. Fall Time (Voltage Rise Time)

The fall times of interest are:

The time the voltage rises, driving another flip flop.

The time the voltage rises until it reaches $V_{be} + V_{D_4} + V_{D_5} - V_{D_1}$

(Nand parameters) when driving Nands only. This time is of interest in determining the turn on time of the Nand. The worst case condition of driving the Nands and one F/F input. This is a repetition rate consideration and any F/F input loads greater than one, will decrease the t_f and thus increase possible repetition rate.

The fall time equation for the lightly saturated case, i.e., worst case solutions, is given by:

$$t_f = \left[\tau_a + \frac{h_{fe} R_L Q_c}{V_{cc}}\right] \ln \frac{I_{B_2} + I_{bs}}{I_{B_2}}$$

since $$\frac{h_{fe} R_L}{V_{cc}} = \frac{1}{I_{bs}}$$

$$t_f = \left[\tau_a + \frac{Q_c}{I_{bs}}\right] \ln \frac{I_{B_2} + I_{bs}}{I_{B_2}}$$

For the case where the buffer stages are fairly heavily saturated,

$$t_f = \frac{Q_b + Q_c}{I_{B_2} + 0.5\ I_{bs}}$$

$$Q_B = \frac{1.2\ I_c}{2\pi f_t}$$

Nominal

For purposes of checking the validity of the charge equation approach to calculating t_f, a nominal solution is calculated and measurements made in the laboratory.

$$Q_b = \frac{1.2 \times 3.0 \times 10^{-3}}{6.2 \times 300 \times 10^{-12}} = 1.9 \times 10^{-12} \text{ coulombs}$$

$$Q_c = 1.2\ C_{ob}\ V_{cb} = 1.2 \times 4.5 \times 10^{-12} \times 5$$

$$= 27 \times 10^{-12} \text{ coulombs}$$

$$h_{fe} = 25$$

$$I_{B_2} = 35\ \mu a$$

$$I_{bs} = \frac{I\ \text{"o"} + I_3 + I_4}{h_{fe}} = 55\ \mu a \text{ for } I\ \text{"o"} + I_3 + I_4 = 3 \text{ ma}$$

(For these calculations and measurements, a resistor to +5 volts simulates Nand loads).

C_s = 2 pf = stray capacitance across emitter to base of circuit including transistor loads.

$$Q_s' = C_s \times 5 \text{ v} = 1.0 \times 10^{-12} \times 5 \text{ volts} = 5 \times 10^{-12} \text{ coulombs}$$

then,
$$t_f = \frac{Q_b + Q_c + Q_{sb\text{-}e}}{I_{B_2} + 0.5\ I_{bs}}$$

$$= \frac{1.9 \times 10^{-12} + 27 \times 10^{-12} + 5.0 \times 10^{-12}}{35 \times 10^{-6} + 27.5 \times 10^{-6}}$$

$$= 0.55\ \mu\text{sec}^*$$

Worst Case (±15% Power Supplies)

Worst case occurs at maximum Vb (-2.55 v), minimum V_{cc} (4.25 v) low temperature (-10°C), on minimum h_{fe}. For worst case, Equation 9, Appendix E, is used.

*Measurements in the laboratory with the above operating conditions, showed a t_f of 0.5 μsec which is in good agreement with the calculated value. Also, laboratory results show that in some cases, the C_{ib} of the inner transistor assists in turn off of the outer transistor.

$$t_f = \left[\tau_a + \frac{Q_c}{I_{bs}}\right] \ln \frac{I_{B_2} + I_{bs}}{I_{B_2}}$$

$\underline{h_{fe}} = 25$

$I_{in} = 534\,\mu a$ (from Nand t_f calculations)

$Q_c = 1.2 \times 6 \times 10^{-12} \times 4.25 = 30.6 \times 10^{-12}$

$I_4 = 0$ (conditioned by another F/F or Nand)

$$I_{B_2}{}_{-10^oC} = \frac{V_{be_1} + V_b}{R_8} \geq 25\,\mu a$$

$I_3 = 102\,\mu a$

$\tau_a = 0.53$ n sec

$$I_{bs} = \frac{\text{number of loads} \times I_{in} + I_3}{\underline{h_{fe}}} = \frac{(\# + *) \times 534\,\mu a + 102\,\mu a}{25}$$

$$= (\# + *) \times 21.4\,\mu a + 4.1\,\mu a$$

$\#$ = number of Nand loads

$*$ = number of F/F inputs

F/F D. C. Loading

F/F loading only. Using Equation 9 for turn off time,

$$t_f = 0.9 \left[0.53 \text{ n sec} + \frac{30.6 \times 10^{-12}}{* \times 21.4 \times 10^{-6} + 4.1 \times 10^{-6}}\right] \ln \frac{29.1 + * 21.4}{25}$$

Note: Multiplying time 0.9 yields actual measured 90% value.

A plot of worst case turn off time (t_f) versus number of F/F inputs is given in Figure 20.

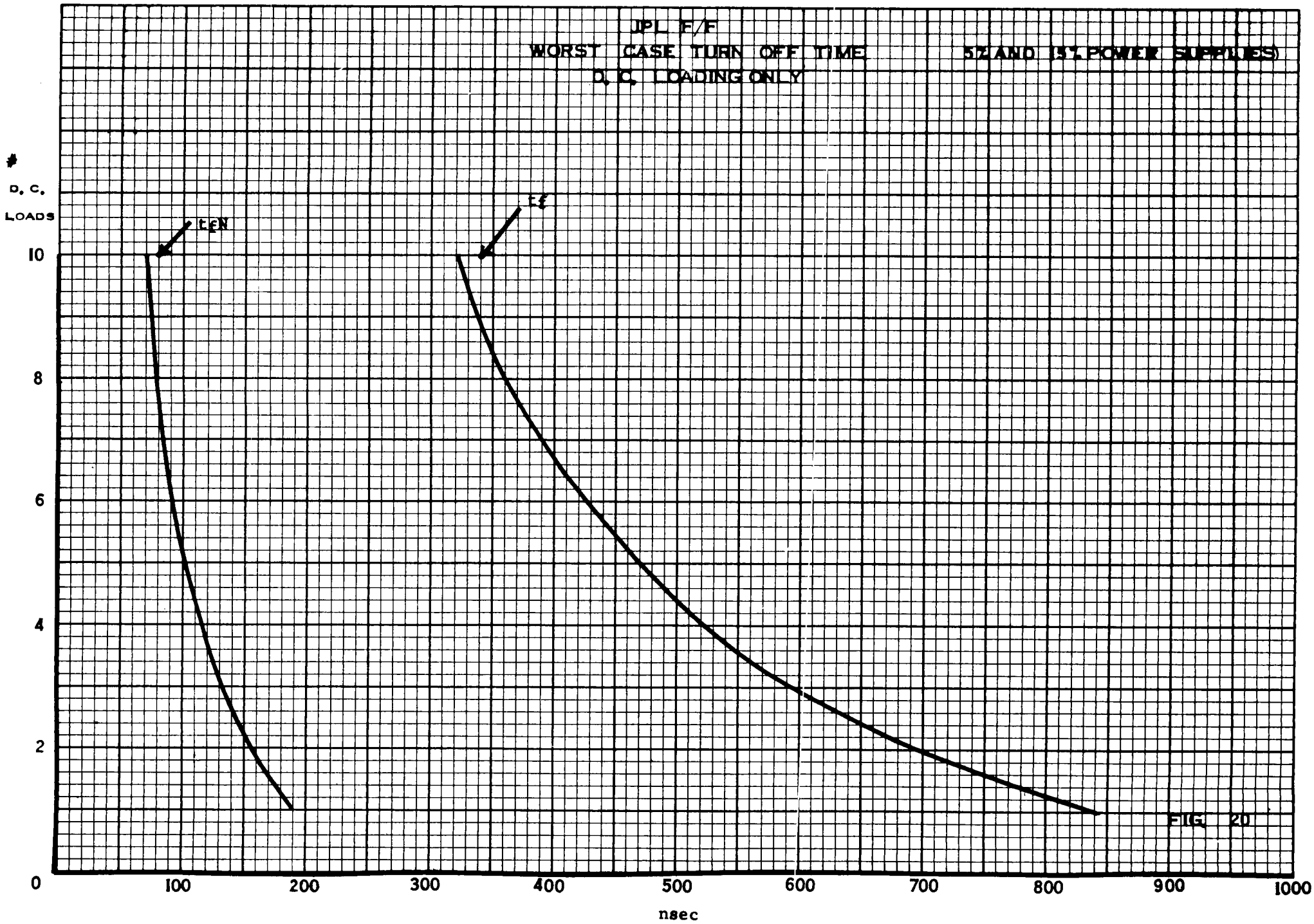

JPL F/F
WORST CASE TURN OFF TIME
D. C. LOADING ONLY
5% AND 15% POWER SUPPLIES)
D. C. LOADS
tfN
tf
10
8
6
4
2
0
100
200
300
400
500
600
700
800
900
1000
nsec

FIG. 20

D. C. (F/F) and Capacitive Loading

In order to factor in the capacitive loading, the worst case turn off time is taken as the sum of two times: the D. C. t_f and 2.3 x R_L C_s. The 2.3 term yields the time at which R_L C_s is at 90% of final value.

$$t_f = 0.9\left[0.53 \times 10^{-9} + \frac{30.6 \times 10^{-6}}{* \times 21.4 + 4.1}\right] \ln \frac{29.1 + * \times 21.4}{25} + \frac{14.7 \times 10^{3} C_s}{*}$$

A plot of D. C. (F/F) and capactivie loading is given in Figure 21.

Nand D. C. Loading

Figure 20 is not valid for Nand D. C. loading. In the case of Nand D. C. loading, the output rises in the same manner as for F/F loading until it reaches $V_{be} + V_{D_4} + V_{D_5} - V_{D1} \equiv V_c$ of the Nand. From this time until it reaches the final value the turn off is determined by R_3. The time required to reach V_c of the Nand can be found solving the following equation. Assuming the fall time to be an exponential

$$V_c = V_{cc} (1 - e - t_{fN} \times 2.3/t_f)$$

For the worst case as solved in the Nand t_f analysis:

$$t_{fN} = 0.217\ t_f$$

Figure 20 also contains a plot of t_{fN}. t_{fN} is only of interest in determining the turn on delay of the Nand, since the F/F output will rise to V_{cc}. This case is covered under combination loads of F/F and Nands.

D.C. (Nand) and Capacitive Loading

t_{fN} is calculated in the same manner as part C.

$t_{fN} = 0.27\ t_f$

Figure 22 is a plot of t_{fN} versus D.C. (Nand) and capacitive loading.

F/F and Nand Loading

The condition of driving a combination of Nands and F/F's is the combination of two times: t_{fN} and the time required to rise from V_c to 90% V_{cc}. This time t_{ff} is given by:

$$t_{ff} = 0.217 \left[0.53 \times 10^{-9} + \frac{30.6 \times 10^{-6}}{(* + \#) \times 21.4 + 4.1} \right] \ln \frac{29.1 + (\# + *)\ 21.4}{25} + 0.773 \left[0.53 \times 10^{-9} + \frac{30.6 \times 10^{-6}}{* \times 21.4 + 4.1} \right] \ln \frac{29.1 + * \times 21.4}{25} + \frac{0.217 \times 14.7 \times 10^3\ C_s}{\# + *} + \frac{0.773 \times 14.7 \times 10^3 \times C_s}{*}$$

or $t_f = t_{fN} + 0.78\ t_f$

Example: For the worst case of no Nands; one F/F input and 30 pf stray capacitance:

$t_f = 1.28\ \mu$sec - this is sufficient to guarantee 500KC operation.

Worst Case (±5% Power Supplies)

Worst case parameters are:

$h_{FE} = 25$

$I_{in} = 608\ \mu$a (from Nand t_f calculation)

$Q_c = 34.2 \times 10^{-12}$

$I_4 = 0$

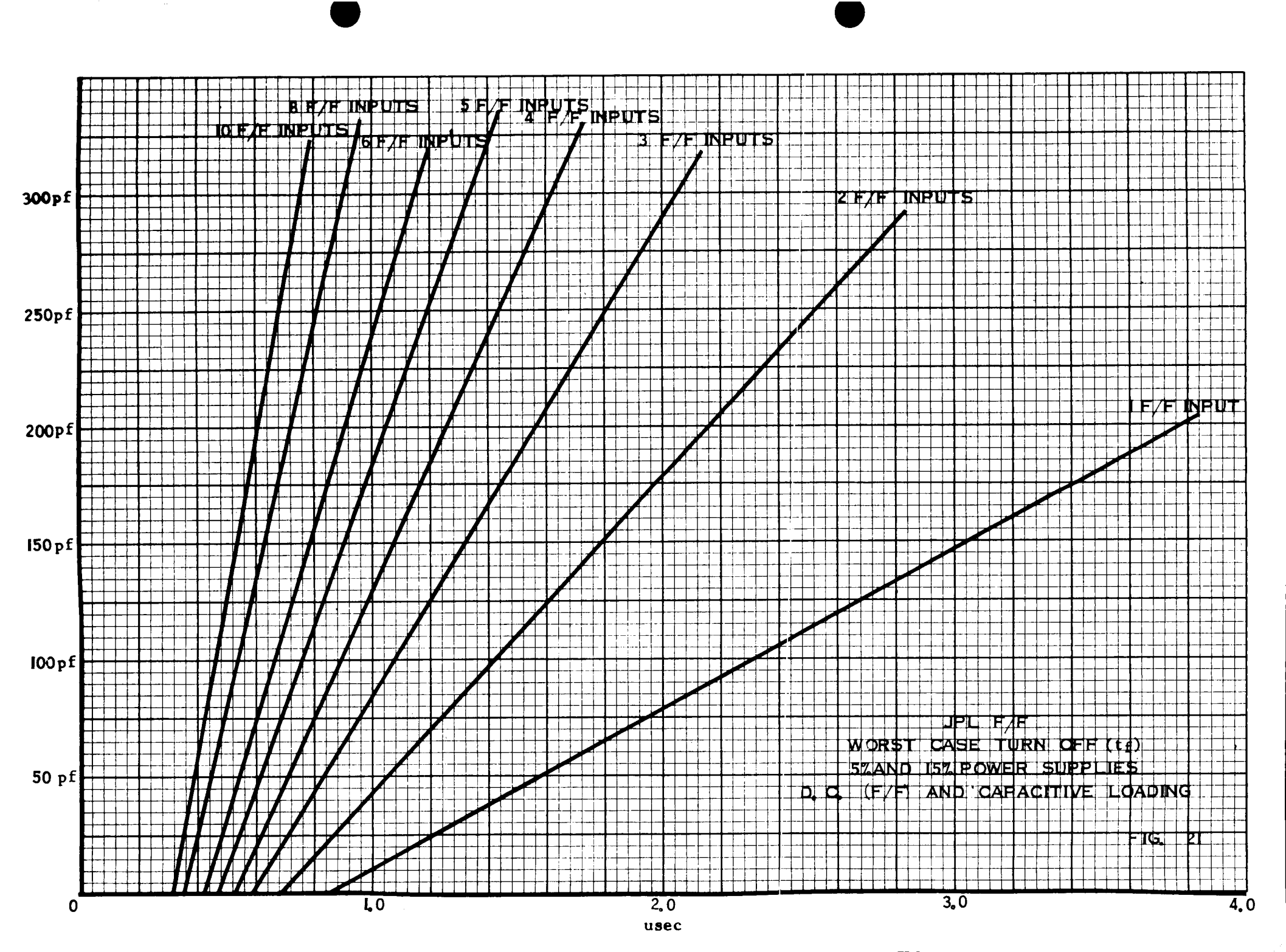
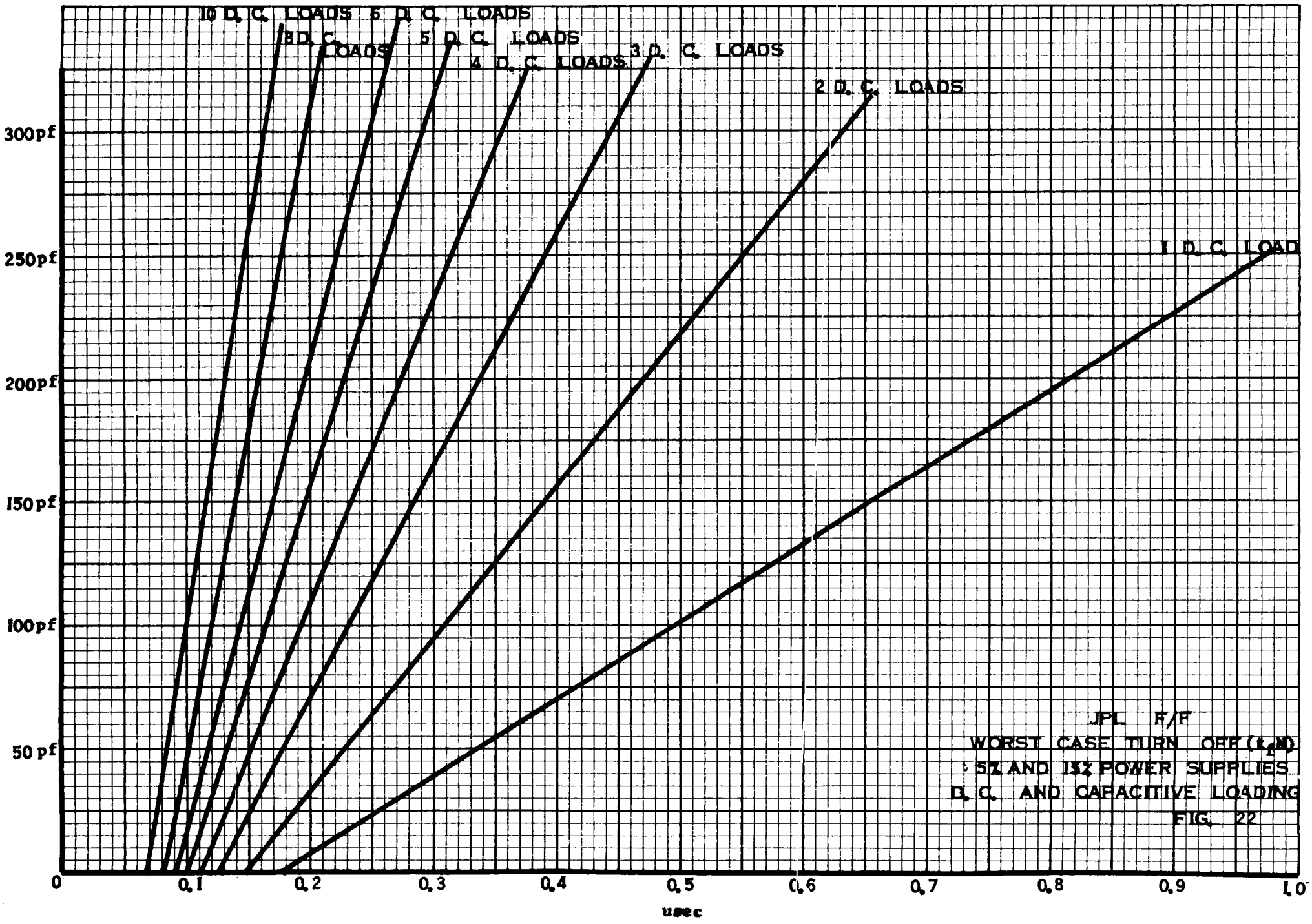

10 F/F INPUTS
8 F/F INPUTS
6 F/F INPUTS
5 F/F INPUTS
4 F/F INPUTS
3 F/F INPUTS
2 F/F INPUTS
1 F/F INPUT
300pf
250pf
200pf
150pf
100pf
50 pf
0
1.0
2.0
3.0
4.0
usec
JPL F/F
WORST CASE TURN OFF (tf)
5% AND 15% POWER SUPPLIES
D. C. (F/F) AND CAPACITIVE LOADING

FIG. 21


10 D. C. LOADS
8 D. C. LOADS
6 D. C. LOADS
5 D. C. LOADS
4 D. C. LOADS
3 D. C. LOADS
2 D. C. LOADS
1 D. C. LOAD
300pf
250pf
200pf
150pf
100pf
50 pf
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
usec
JPL F/F
WORST CASE TURN OFF (t_{pHL})
5% AND 15% POWER SUPPLIES
D. C. AND CAPACITIVE LOADING
FIG. 22

$$I_{B_2} \geq 26\mu a$$

$$I_3 = 115\mu a$$

$$\tau_a = 0.53 \text{ n sec}$$

$$I_{bs} = \frac{(\# + *) \times 608\mu a + 115\mu a}{25} = (\# + *) \times 24.3\mu a + 4.6\mu a$$

F/F D. C. Loading

$$t_{f\ F/F} = 0.9 \left[0.53 \times 10^{-9} + \frac{34.2 \times 10^6}{* \times 24.3 + 4.6} \right] \ln \frac{30.6 + * \times 24.3}{26}$$

A plot of worst case turn off time (t_f) versus the number of F/F inputs is given in Figure 20. (Note: The ±5% and ±15% power supply curves are approximately the same therefore only one curve is shown).

D. C. (F/F) and Capacitive Loading

The capactivie loading was factored in the same way as for the ±15% P. S. case. A plot of D. C. and capacitive loading is given in Figure 21.

Nand D. C. Loading

The case of the Nand D. C. loading is similar to part c of the ±15% P. S. case. The resulting curve is approximately the same curve as Figure 20.

D. C. Nand and Capacitive Loading

Since t_{fN} is approximately the same for the ±5% P. S. case, the condition of capacitive loading is also the same as given in Figure 22.

iii. Rise Time (Voltage Fall Time)

The time required to saturate Q_1 or Q_4 in the nominal case is given by:

$$t_r = \frac{Q_b + Q_c + Q_{sbe}}{I_{b1} - 0.5\ I_{bs}}$$

Nominal

From the previous t_f calculations and under the same load conditions.

$Q_b = 1.9 \times 10^{-12}$ coulombs

$Q_c = 27 \times 10^{-12}$ coulombs

$Q_{sbe} \approx 5 \times 10^{-12}$ coulombs

$I_{bs} = 0.055$ ma

$I_{b1} = 0.54$ ma (Nominal solution for I_{b1} computer run Appendix III)

$$t_r = \frac{1.9 \times 10^{-12} + 27 \times 10^{-12} + 5 \times 10^{-12}}{0.54 \times 10^{-3} - 0.5 \times 0.055 \times 10^{-3}} = 65 \text{ nsec.}$$

Observed value in the laboratory 70 n sec.

Worst Case (±15% Power Supplies)

Since the rise time is of prime interest in connection with the F/F triggering, the worst case conditions are low power supplies and low temperature.

D. C. Loading Only

$I_{b1} = 325 \mu a$

$\tau_a = 0.53$ n sec

$$Q_c = 30.6 \times 10^{-12}$$

$$I_{bs} = \frac{I_{in} \times (\# + *)}{h_{fe}} = \frac{525 \times 10^{-6} \ (\# + *)}{25}$$

$$= 21 \times 10^{-6} \times (\# + *)$$

$$t_r = \boxed{0.53 \times 10^{-9} + \frac{1.455 \times 10^{-6}}{(\# + *)}} \ln \frac{325}{325 - 21 \times (\# + *)}$$

Figure 23 is a worst case plot of t_r versus number of D. D. loads.

Capacitive Loading

In order to include the effect of capacitive loading, an additional charge must be supplied to the base. The total charge supplied to the base is then given by the sum of Q_c plus Q_s. Q_s is the stray capacitive charge reflected to the base. The rise time equation can be written as:

$$t_r = \boxed{\tau_a + \frac{Q_c + Q_s}{I_{bs}}} \ln \frac{I_{b1}}{I_{b1} - I_{bs}}$$

$$Q_s = \frac{C_s \ (V_{cc} - V_{ce})}{h_{fe}}$$

For the worst case condition being considered:

$$t_r = \boxed{0.53 \times 10^{-9} + \frac{1.455 \times 10^{-6} + 7.9 \times 10^{3} \ C_s}{\# + *}} \ln$$

$$\frac{325}{325 - 21 \times (\# + *)}$$

Figure 24 is a worst case plot of t_r versus number of loads for D. C. loading.

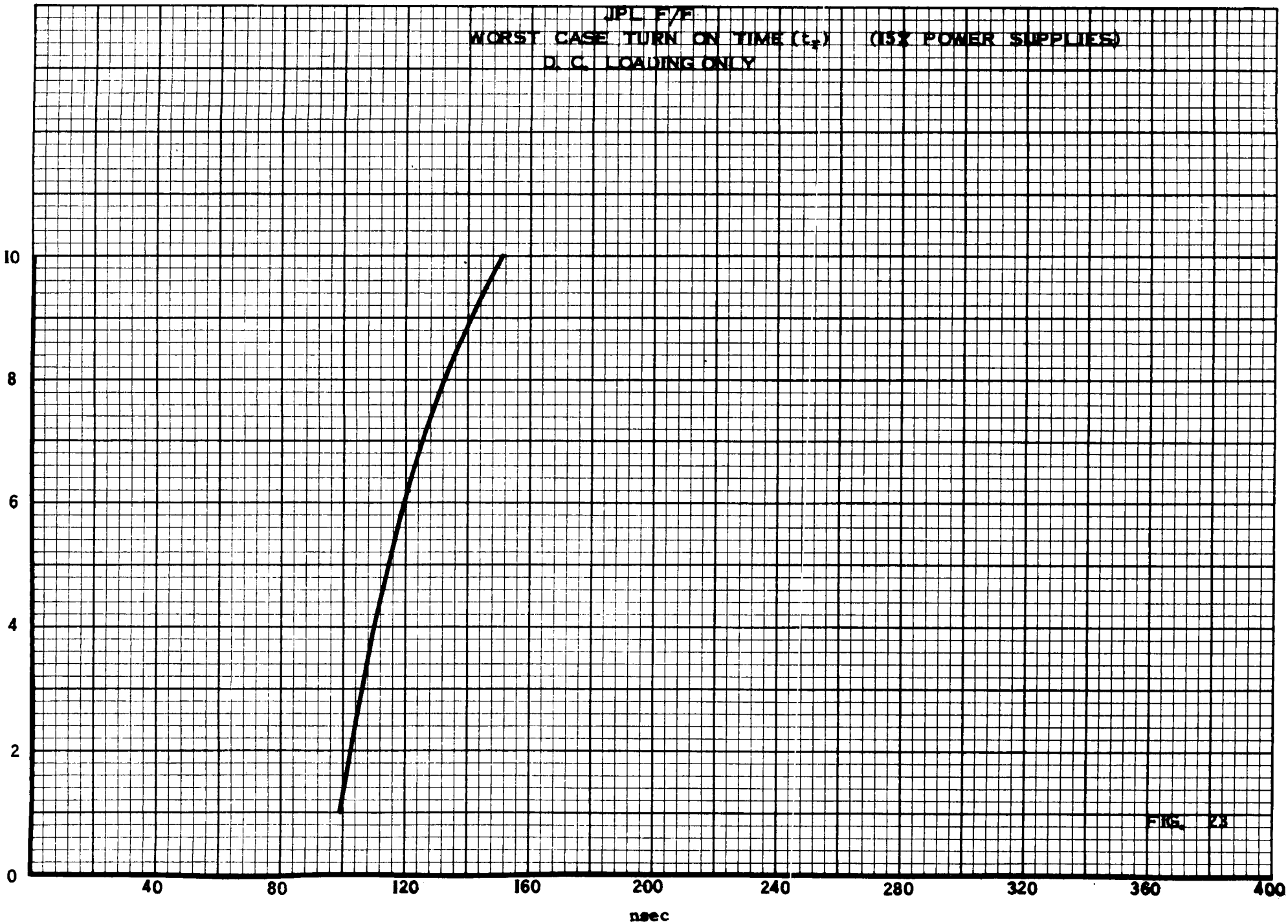

JPL F/F
WORST CASE TURN ON TIME (t_4) (15% POWER SUPPLIES)
D. C. LOADING ONLY
10
8
6
4
2
0
40
80
120
160
200
240
280
320
360
400
nsec

FIG. 23

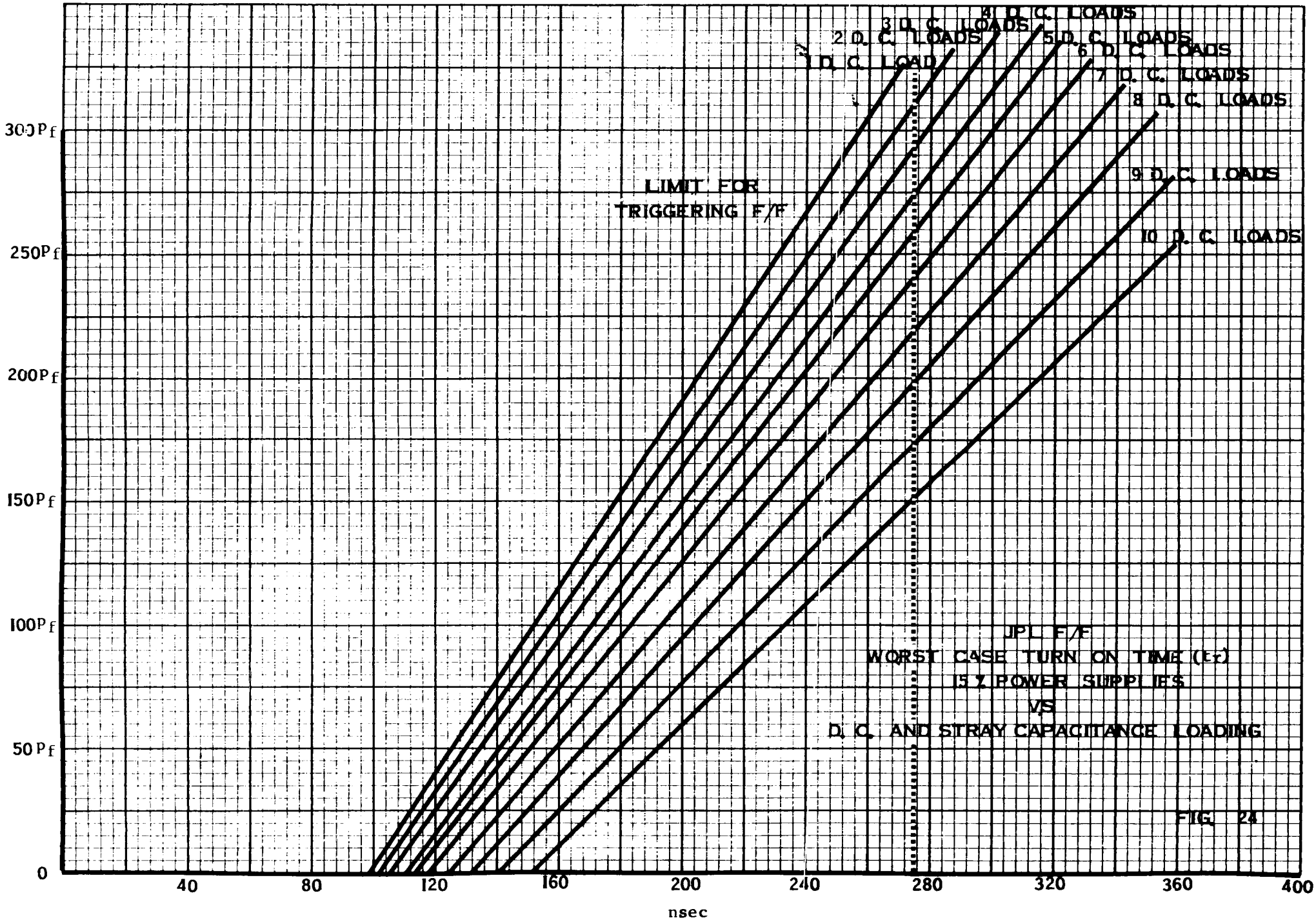

1 D. C. LOAD
2 D. C. LOADS
3 D. C. LOADS
4 D. C. LOADS
5 D. C. LOADS
6 D. C. LOADS
7 D. C. LOADS
8 D. C. LOADS
9 D. C. LOADS
10 D. C. LOADS
LIMIT FOR TRIGGERING F/F
300Pf
250Pf
200Pf
150Pf
100Pf
50Pf
0
40
80
120
160
200
240
280
320
360
400
nsec
JPL F/F
WORST CASE TURN ON TIME (Et)
15% POWER SUPPLIES
VS
D. C. AND STRAY CAPACITANCE LOADING

FIG. 24

Worst Case (±5% Power Supplies)

D. C. Loading Only

$$I_{b1} = 411\mu a$$

$$\tau_a = 0.53 \text{ n sec}$$

$$Q_c = 34.2 \times 10^{-12}$$

$$I_{bs} = 24.2 \times 10^{-6} \times (\# + *)$$

$$t_r = \left[0.53 \times 10^{-9} + \frac{1.415 \times 10^{-6}}{\# + *} \right] \ln \frac{411}{411 - 24.2 \times (\# + *)}$$

Figure 25 is a worst case plot of t_r versus number of loads for D. C. loading.

Capacitive Loading

$$t_r = \left[0.53 \times 10^{-9} + \frac{1.415 \times 10^{-6} + 7.85 \times 10^{3} \times C_s}{\# + *} \right] \ln \frac{411}{411 - 24.2 \times (\# + *)}$$

Figure 26 is a plot of t_r versus D. C. and capacitive loading.

4. Delay Time

The delay time as defined as starting from the time the input waveform has decreased 10% to the time the output waveform has decreased 10% is the sum of the following items:

t_{VT} - time required to exceed the threshold voltage

t_s - storage time of inner transistor

t_f - rise time of the collector of the inner transistor

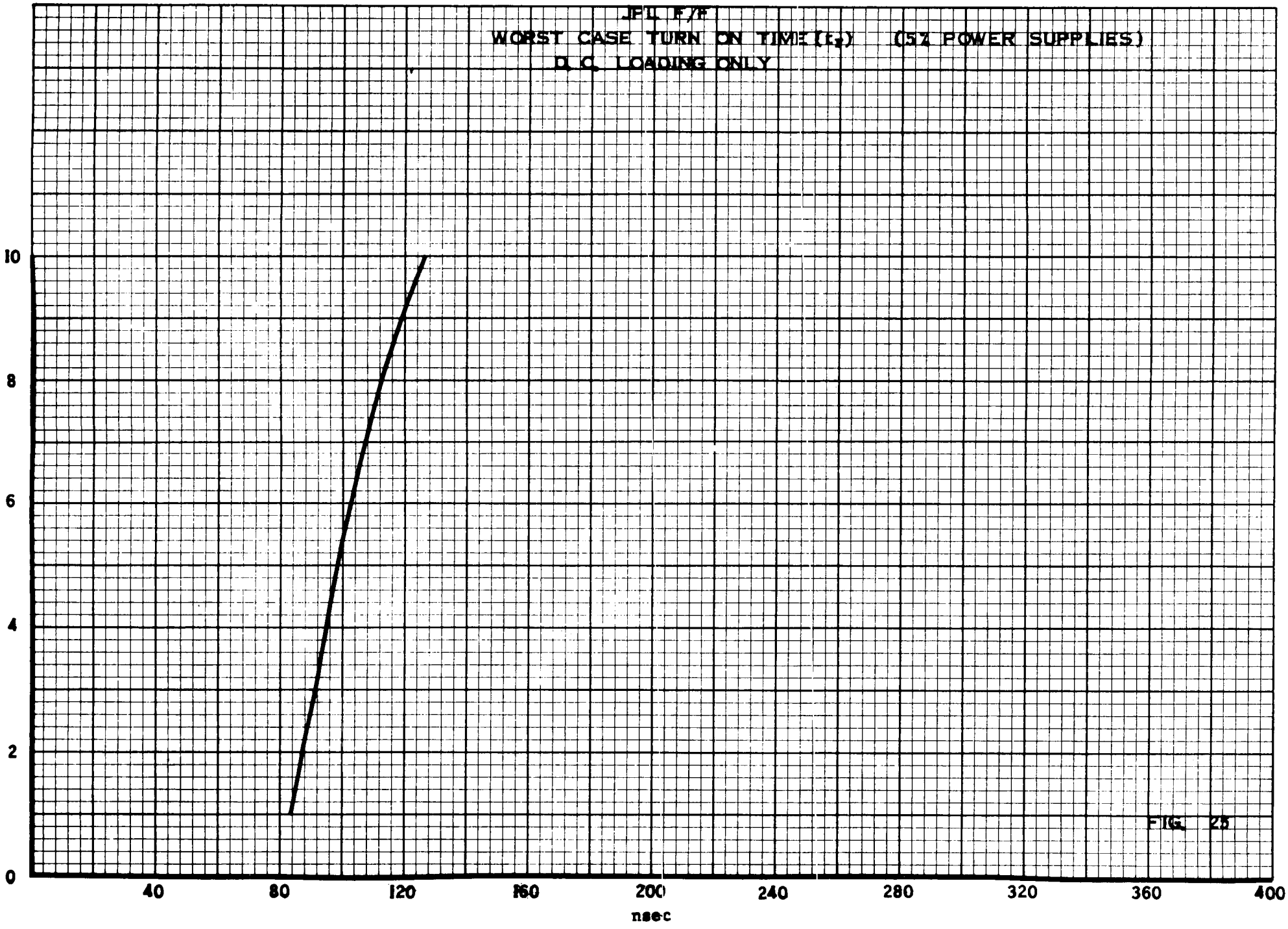

JFL F/F
WORST CASE TURN ON TIME (t_2) (5% POWER SUPPLIES)
D.C. LOADING ONLY
10
8
6
4
2
0
40
80
120
160
200
240
280
320
360
400
nsec

FIG. 25

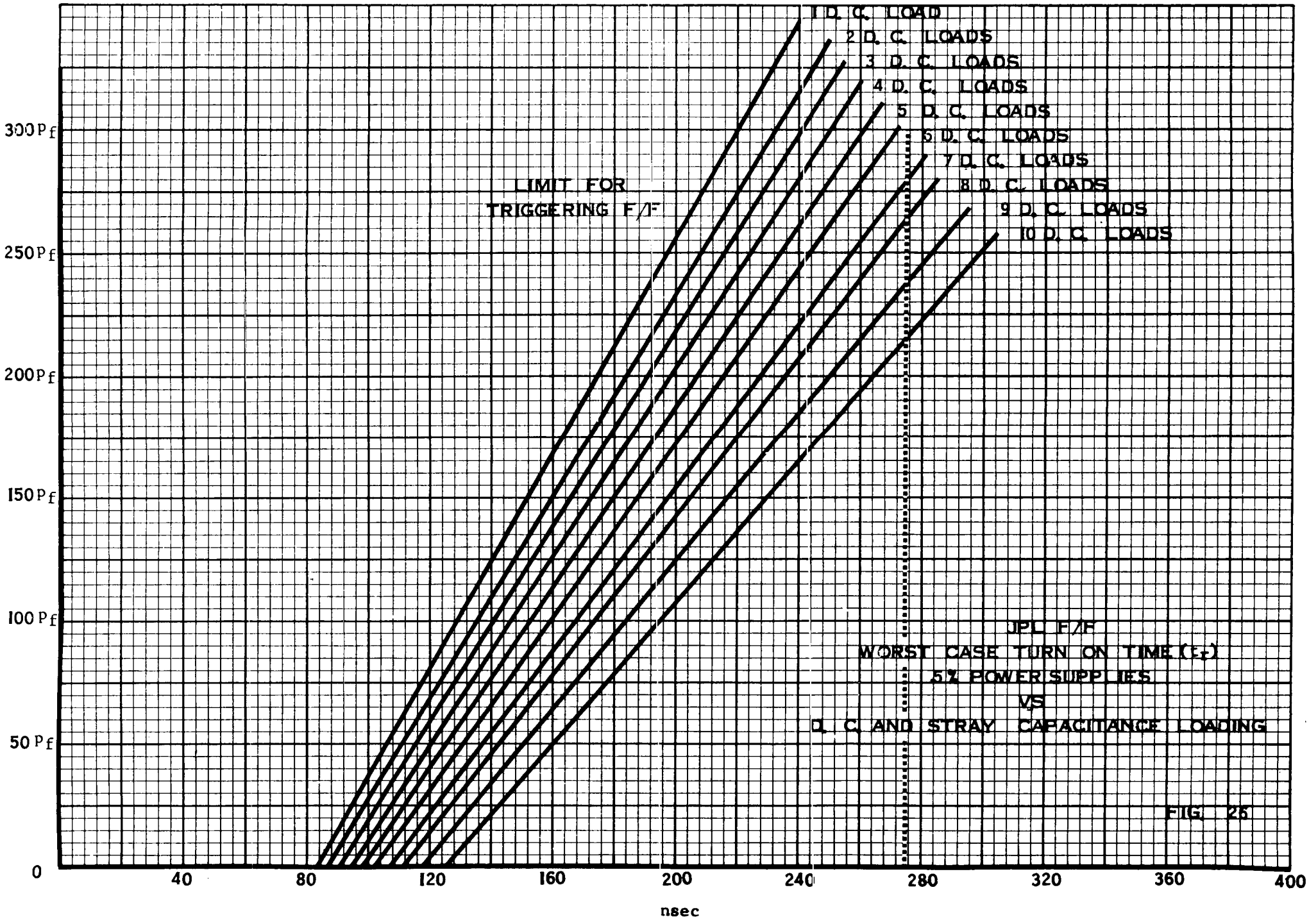

1 D. C. LOAD
2 D. C. LOADS
3 D. C. LOADS
4 D. C. LOADS
5 D. C. LOADS
6 D. C. LOADS
7 D. C. LOADS
8 D. C. LOADS
9 D. C. LOADS
10 D. C. LOADS
LIMIT FOR TRIGGERING F/F
300 Pf
250 Pf
200 Pf
150 Pf
100 Pf
50 Pf
0
40
80
120
160
200
240
280
320
360
400
nsec
JPL F/F
WORST CASE TURN ON TIME (t_r)
5% POWER SUPPLIES
VS
D. C. AND STRAY CAPACITANCE LOADING

FIG. 25

t_{dr} - delay time of outer transistor that is being turned on

t_r - 10% of rise time of outer transistor

As discussed in the transient analysis of the inner transistor, t_s is negligible. In addition, since the rise time of the outer transient is approximately an exponential, the initial 10% decrease of the output can also be assumed negligible. Therefore, the delay time is very nearly given by

$$t_d = t_{VT} + t_f \text{ (inner transistor)} + t_{dr}$$

The worst case t_{VT} can be obtained from the triggering analysis. The t_f of the inner transistor is given in the transient analysis of the inner transistor. t_{dr} can be calculated as follows:

Nominal

$I_{b_1} = 0.54$ ma

$Q_e = 1.67\ C_{ib}\ V_{be_{off}} = 1.67 \times 6 \times 10^{-12} \times 0.5 = 5.0 \times 10^{-12}$

$Q_{cd} = 1.2\ C_{ob}\ V_{cb} = 1.2 \times 4.5 \times 10^{-12} \times 0.5 = 2.70 \times 10^{-12}$

$t_{ri} = 30$ nsec.

The 30 nsec. number for t_{ri} is an estimate. It is based on the fact that the internal Flip-Flop has a t_f of 90 nsec. (which actually is what turns on the opposite side of the Flip-Flop and when t_d occurs). This results from a time constant of 300 nsec, (see transient analysis of internal F/F). Considering that during the t_d time of the output buffer (Q_4), the collector of Q_2 need only rise about 0.5v once the emitter of Q_3 begins to pull up the base of Q_1 from its nominally OFF condition of about -0.1v to +0.4 volts. The 0.4 volt value is where

appreciable base current begins to flow through Q_1. Since the time constant of the circuit driving the base of Q_1 is 300 n sec and the circuit must swing $\frac{0.5\ v}{5\ v} \times 100\% = 10\%$ of the applied voltage during t_d, then the t_{ri} of the input signal during time t_d is 10% x 300 = 30 n sec. Then

$$t_{dr} = \frac{2 \times 30 \times 10^{-9}}{0.54 \times 10^{-3}} (5.0 \times 10^{-12} + 2.7 \times 10^{-12})^{\frac{1}{2}}$$

$$= 29.3 \text{ n sec}$$

Observed value in the laboratory was 32 n sec.

Worst Case (±15% Power Supplies)

Worst case occurs at minimum V_{cc}, V_b, and low temperature.

$I_{b1} = 325 \mu a$

$Q_e = 1.67 \times 9 \times 10^{-12} \times (V_{be1} - V_1) = 10.5 \times 10^{-12}$

$Q_c = 1.2 \times 6 \times 10^{-12} \times (V_{be1} - V_1) = 5.1 \times 10^{-12}$

$t_{ri} = 45$ n sec (assuming 15% of worst case time constant)

$t_{dr} = 66$ n sec

Worst Case (±5% Power Supplies)

$I_{b1} = 411 \mu a$

$Q_e = 10.5 \times 10^{-12}$

$Q_c = 5.1 \times 10^{-12}$

$t_{ri} \leq 45$ n sec

$t_{dr} = 59$ n sec

The nominal case delay time of the F/F is then equal to

$$t_d = t_{VT} + t_f + t_{dr}$$

$$= 40 \text{ n sec} + 30 \text{ n sec} + 29.3 \text{ n sec}$$

$$= 110 \text{n sec}$$

Observed value = 170 n sec.

The worst case delay time (15% P. S.) is equal to

$$t_d = 110 \text{ n sec} + 45 \text{ n sec} + 66 \text{ n sec}$$

$$= 221 \text{ n sec}$$

3. Flip Flop Triggering:

In analyzing the triggering of the F/F, three time constants and equivalent circuits must be considered.

1. Initially, the inside of the capacitor, on the side that is conditioned, sets at V_T (threshold voltage). The A.C. equivalent circuit is given in Figure 27. From time zero, with reference to the start of the triggering edge, until D_3 is forward biased, R_{eq} is R_5 paralleled by R_9.

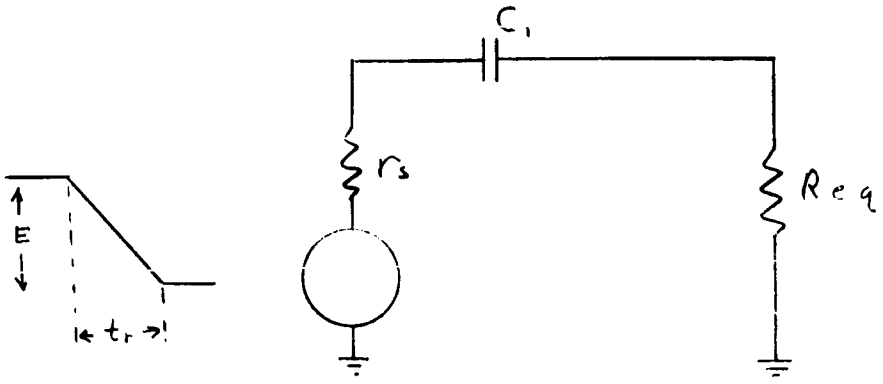


Figure 27

2. After D_3 is forward biased, but before diode D_5 is cut off, R_{eq} is R_5, R_9 and R_2 in parallel. By assuming R_2 is switched in as soon as D_3 is forward biased, a condition slightly worse than worst case is guaranteed. This is offset by the assumption that ts is negligible.

3. After D_5 is cut off, R_{eq} is R_9 and R_2 parallel.

The analysis for a ramp input driving the input networks is given in Appendix F.

A. Nominal

The voltage threshold is given by

$$V_T = \frac{R_9 R_5}{R_9 + R_5} \left(\frac{V_{cc}}{R_9} + I_{DL3} + \frac{V_{D5} + V_{ce}}{R_5} \right)$$

$$= 1.96 \text{ v}$$

The voltage at the base of Q2 is given by

$$V_2 = V_{be_{Q_1}} + V_{be_{Q_2}} = 1.4 \text{ v}$$

The voltage on the inside of the capacitor as a function of time is given by (see Appendix F for derivation).

$$v(t) = V_i - \frac{R_{eq} E C_1}{t_r} \left[1 - e^{-t/R_{eq} C_1} \right] + \frac{It}{C_1}$$

1. Until D_3 is forward biased

$V_i = V_T$

E = driving potential

I = D.C. current (I_4)

R_{eq} = R_9 and R_5 in parallel

Substituting in the following nominal values:

$V_T = 1.96$ v

$R_{eq} = 3.38$ K

$E = V_{cc} - V_{ce} - V_{D_7} = 4.25$

$C = 75$ pf

$I_4 = 250 \mu a$

$$v(t) = 1.96 - \frac{10.7 \times 10^{-7}}{t_r} (1 - e^{-t/254 \times 10^{-9}}) + 3.33 \times 10^6 t$$

2. After D_3 is forward biased and before D_5 is cut off

$V_i = V_{t_1}$ (the voltage at the time the noise immunity is exceeded.)

$R_{eq} = 2.64K$

$I = I_{b2} + I_4 = 225\mu a + 250\mu a = 475\mu a$

$$v(t) = V_{t1} - \frac{8.4 \times 10^{-7}}{t_r} \left(1 - e^{-(t - t_1)/198 \times 10^{-9}}\right) + 6.33 \times 10^6 (t-t_1)$$

3, After D_5 is cut off

$V_i = V_{t2}$ (the voltage at the time D_5 is cut off)

$R_{eq} = 6K$

$I = I_{b2} + I_4 = 475\mu a$

$$v(t) = V_{t2} - \frac{19.1 \times 10^{-7}}{t_r} \left(1 - e^{-(t-t2)/450 \times 10^{-9}}\right) + 6.33 \times 10^6 (t-t_2)$$

4. After the edge of the input pulse has passed,

$$v(t) = (V_{cc} - V_i) \left(1 - e^{-t/R_{eq}C}\right) + V_i$$

From Appendix F

$V_i = V_{tr}$ the voltage a time t_r.

$$v(t) = (5 - V_{tr}) \left(1 - e^{-(t-t_r)/450 \times 10^{-9}}\right) + V_{tr}$$

Figure 29 is a plot of the voltage on the inside of the capacitor as a function of time for t_r of input = 100 nsec.

Figure 29 also contains a plot of the voltage on the base of Q_2. The effect of D_3 is included in the base voltage plot. In order to guarantee triggering, Q_2 must be kept "off" for a particular length

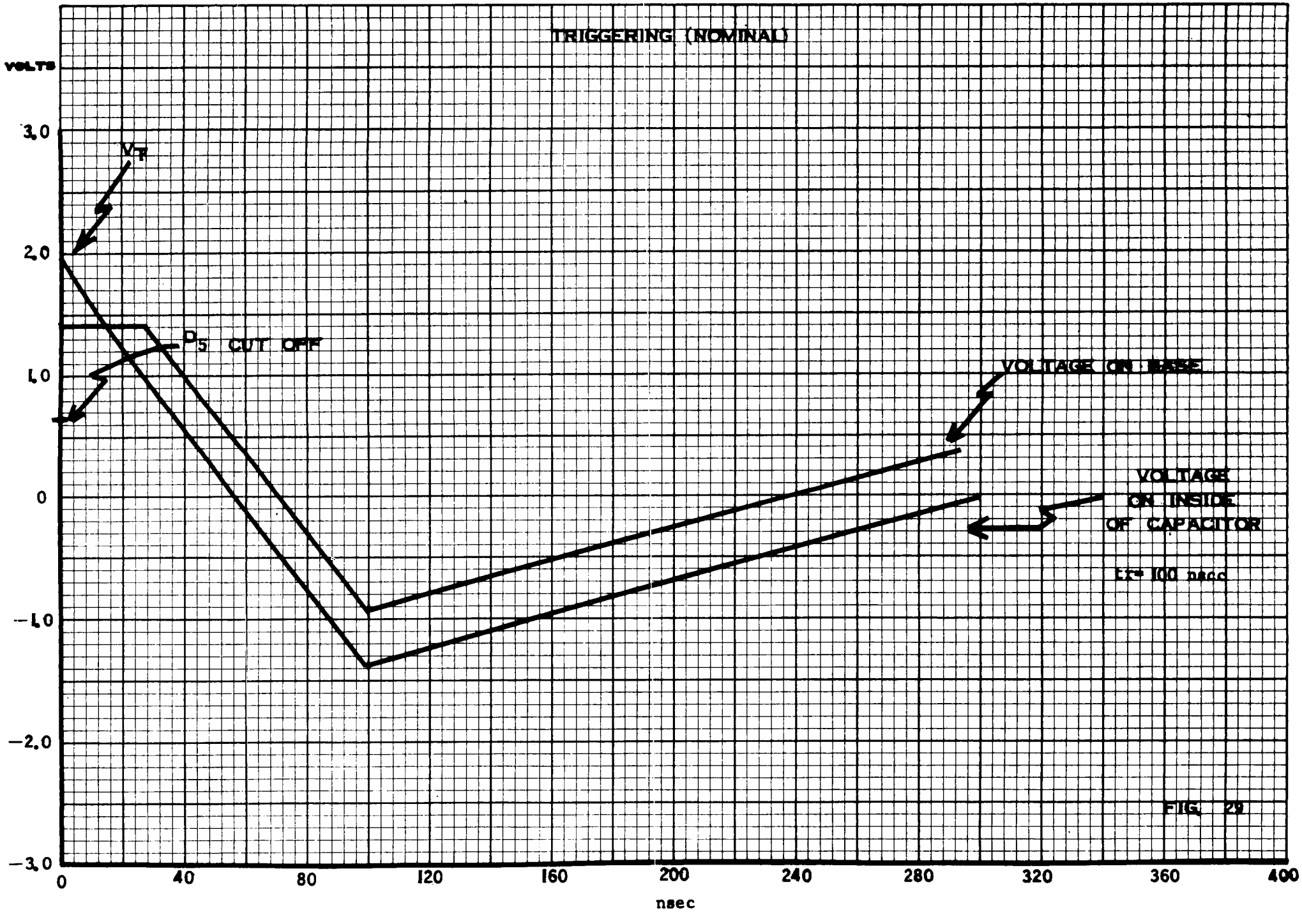

TRIGGERING (NOMINAL)
VOLTS
3.0
2.0
1.0
0
-1.0
-2.0
-3.0
V_T
D_5 CUT OFF
VOLTAGE ON BASE
VOLTAGE ON INSIDE OF CAPACITOR
t_f = 100 nsec
0
40
80
120
160
200
240
280
320
360
400
nsec

FIG. 29

of time. If the F/F has not flipped and reach a steady state by the time the voltage on the base rises to a turn on value, the F/F won't flip. For a turn on voltage of 1.1v nominal, the guaranteed off time is seen to be $>$300 nsec.

B. Worst Case ($\pm$15% Power Supplies)

The worst case triggering occurs at low power supplies, low temperature, maximum V_t, and minimum V_2.

$V_T = 1.96v$

$V_2 = V_{b1} + 35 \times \underline{I_{C_{b1}}} + \underline{V_{b2}} + 35 \times \underline{TC_{b2}} = 1.58v$

$V_{NI}(-10^{oC}) = 1.96 - 1.58 + V_{D3} = 0.91v$

The voltage on the inside of the capacitor as a function of time using equation 10 Appendix F is given by

1. Until D_3 is forward biased.

$V_i = V_T = 1.96v$

$R_{eq} = 3.24K$

$E = 3.28v$

$C = 71.2$ pf

$I_4 = 200\mu a$

$I_{b2} = 150\mu a$

$$v(t) = 1.96 - \frac{7.58 \times 10^{-7}}{t_r} (1 - e^{-t/241 \times 10^{-9}}) + 2.81 \times 10^6 t$$

2 After D_3 is forward biased and before D_5 is cut off

$V_i = V_{t_1}$

$R_{eq} = 2.54K$

$I = 350\mu a$

$$v(t) = V_{t1} - \frac{5.92 \times 10^{-7}}{t_r} \left(1 - e^{-(t-t_1)/181 \times 10^{-4}}\right) + 4.9 \times 10^{6}(t-t1)$$

3. After D_5 is cut off

$V_{ce}+V_{D5} = 0.44 + 2.3 \times 10^{-3} \times 35 + 0.1 = 0.62$

$V_i = V_{t2}$

Req = 5.76K

I = 350 μ a

$$v(t) = V_{t2} - \frac{13.46 \times 10^{-7}}{t_r} \left(1 - e^{-(t-t_2)/400 \times 10^{-9}}\right) + 4.91 \times 10^{6}(t-t_2)$$

4. After the edge of the input pulse has passed

$$v(t) = (4.25 - V_{tr}) \left(1 - e^{-(t-t_r)/400 \times 10^{-4}}\right) + V_{tr}$$

using Equation 11 Appendix F

Figures 30 and 31 are plots of the voltage on the inside of the capacitor and the base for t_r = 200 nsec. and 275 nsec. respectively. In Figure 30 if it is assumed that a minimum change of 180 mv is sufficient to guarantee regeneration in the F/F, then the base is kept below this for 98 nsec.

C. Worst Case (±5% Power Supplies)

$V_T = 2.10v$

$V_2 = 1.58v$

$V_{NI} = 1.08v$

The voltage on the inside of the capacitor as a function of time using equation 10 is given by

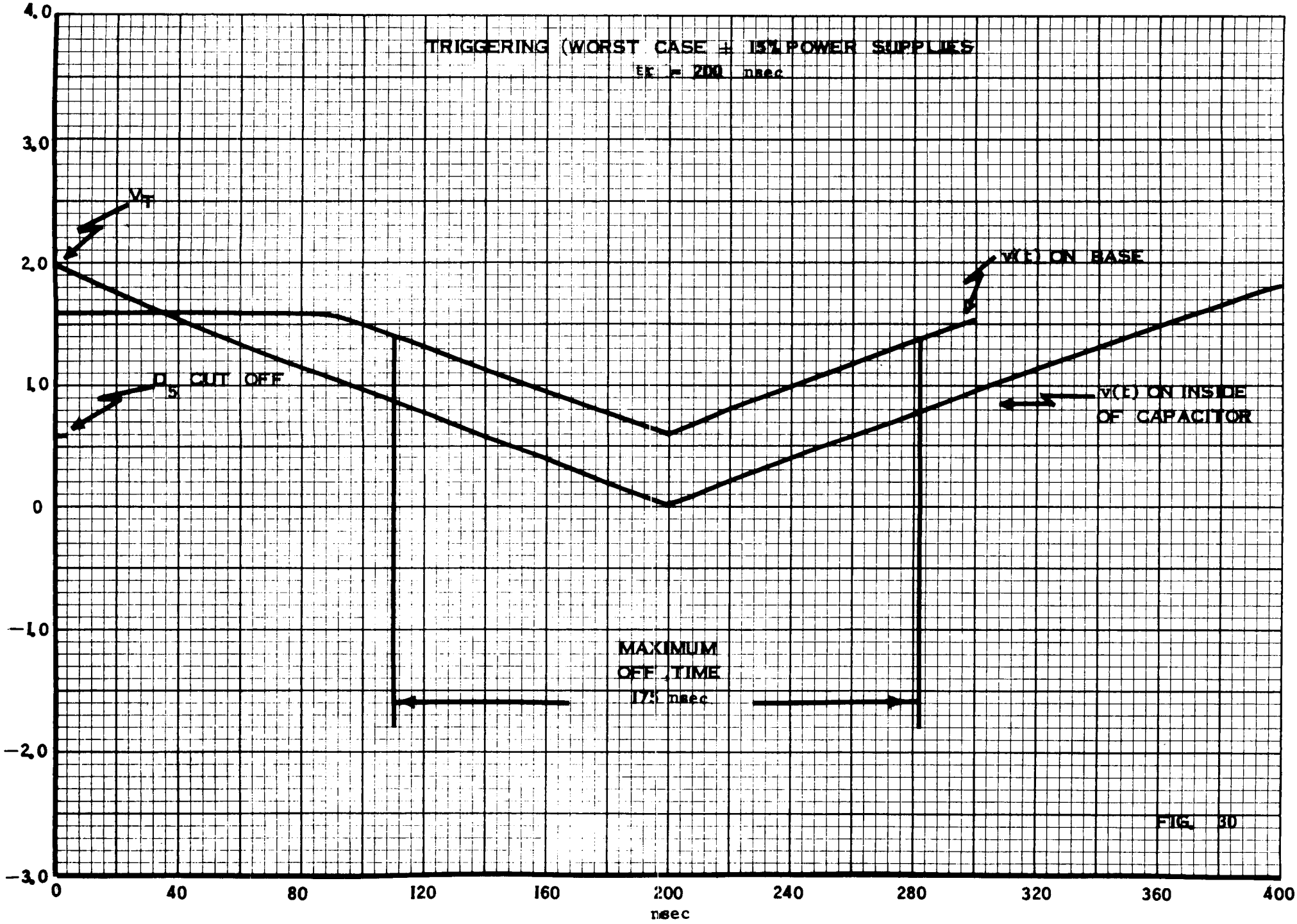

TRIGGERING (WORST CASE ± 15% POWER SUPPLIES
t_F = 200 nsec
V_{TT}
D_5 CUT OFF
v(E) ON BASE
v(E) ON INSIDE OF CAPACITOR
MAXIMUM OFF TIME 175 nsec
4.0
3.0
2.0
1.0
0
-1.0
-2.0
-3.0
0
40
80
120
160
200
240
280
320
360
400
nsec

FIG. 30

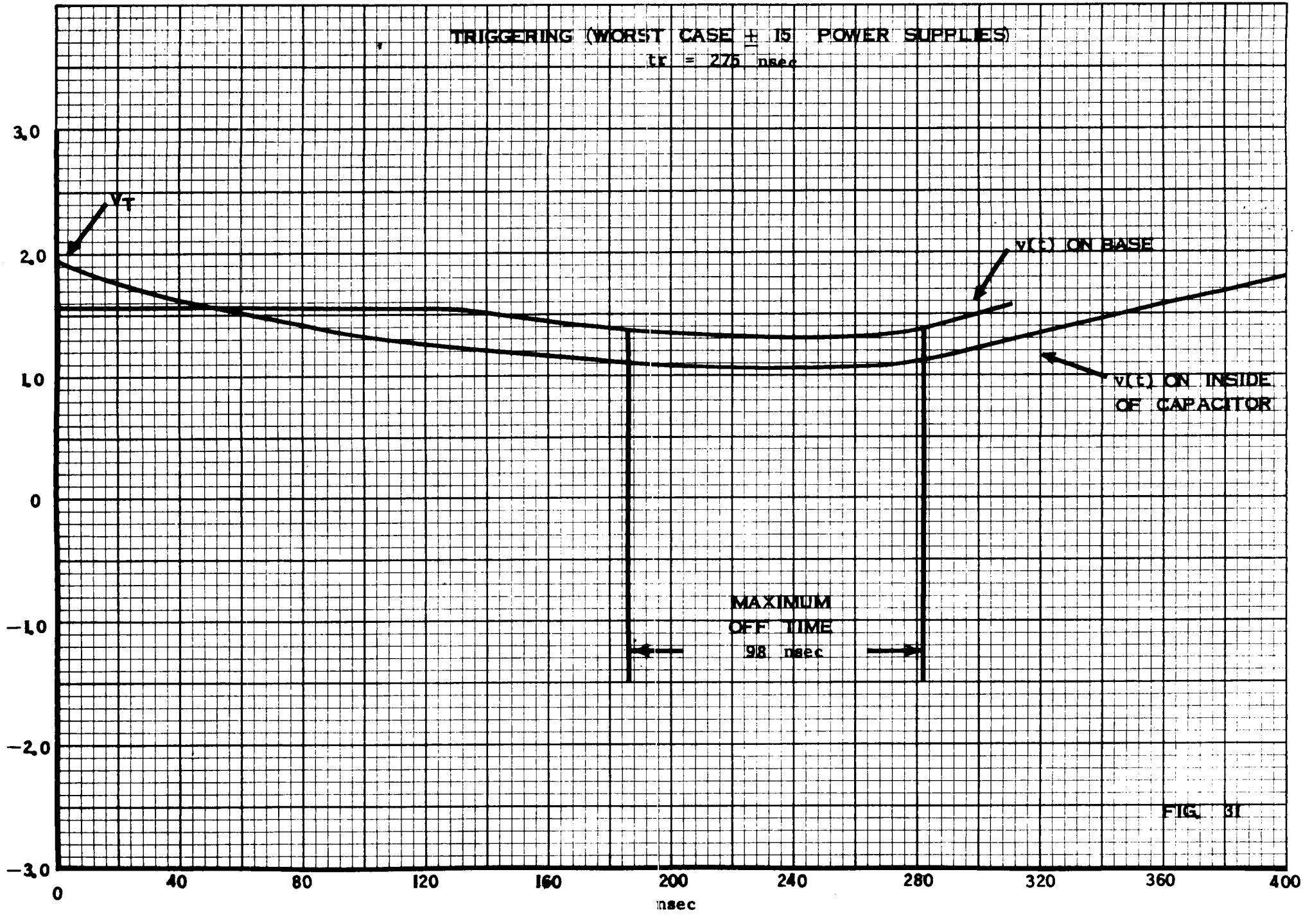

TRIGGERING (WORST CASE ± 15 POWER SUPPLIES)
tr = 275 nsec
3.0
2.0
1.0
0
-1.0
-2.0
-3.0
V_T
v(t) ON BASE
v(t) ON INSIDE OF CAPACITOR
MAXIMUM OFF TIME 98 nsec
0
40
80
120
160
200
240
280
320
360
400
nsec

FIG. 31

1. Until D_3 is forward biased

$V_i = V_T = 2.10v$

$R_{eq} = 3.24K$

$E = 3.78v$

$C = 71.2$ pf

$I_4 = 230 \mu a$

$I_{b2} = 200 \mu a$

$$v(t) = 2.1 - \frac{8.72 \times 10^{-7}}{t_r} (1 - e^{-t/241 \times 10^{-4}}) + 3.23 \times 10^6 t$$

2. After D_3 is forward biased and before D_5 is cut off

$V_i = V_{ti}$

$R_eq = 2.54K$

$I = 430 \mu a$

$$v(t) = V_{t1} - \frac{6.82 \times 10^{-7}}{t_r} (1 - e^{-(t-t_1)/181 \times 10^{-9}}) + 6.04 \times 10^{6}_{(t-t1)}$$

3. After D_5 is cut off

$V_{cc} + V_{D5} = 0.62$

$V_i = V_{t2}$

$R_{eq} = 5.76K$

$I = 430 \mu a$

$$v(t) = V_{t2} - \frac{15.50 \times 10^{-7}}{tr} (1 - e^{-(t-t_2)/400 \times 10^{-9}}) -6.04 \times 10^{6}_{(t-t_2)}$$

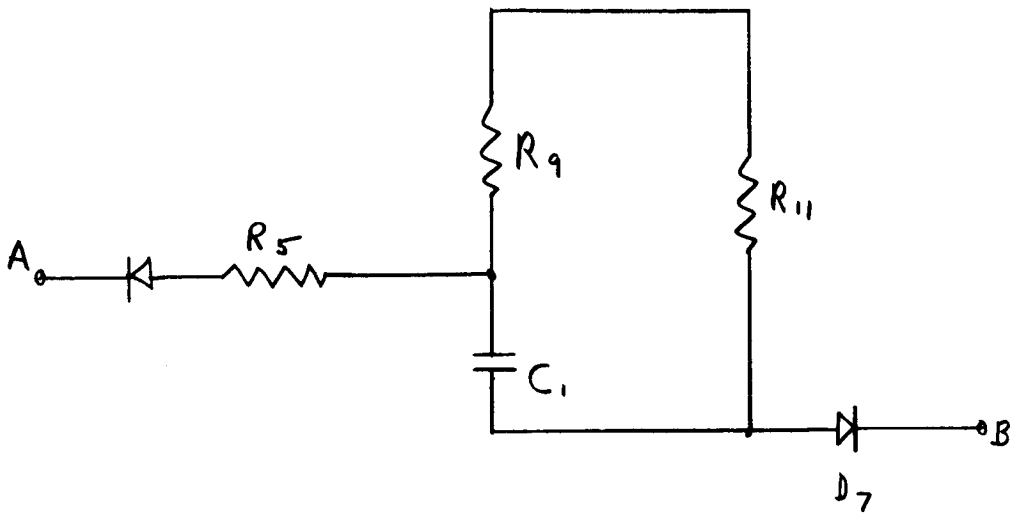
4. After the edge of the input pulse has passed

$$v(t) = (4.75 - V_{tr}) (1 - e^{-(t-t)/400 \times 10^{-9}}) + V_{tr}$$

Figure 32 and 33 are plots of the voltage on the inside of the capacitor and the base for t_r = 200 nsec and 275 nsec. respectively.

4. Repetition Rate

1. In analyzing the repetition rate of the F/F, its use as a counter (toggle) shift register, and conditioned by a gate must be considered. The input circuitry which determines the repetition rate is shown below.



Defining the conditioning terminal as A and the triggering terminal as B, a table of all possible input and triggering conditions can be made. In this way the time constants and total ΔV on the capacitor can be determined and the limiting condition on the repetition rate can be found.

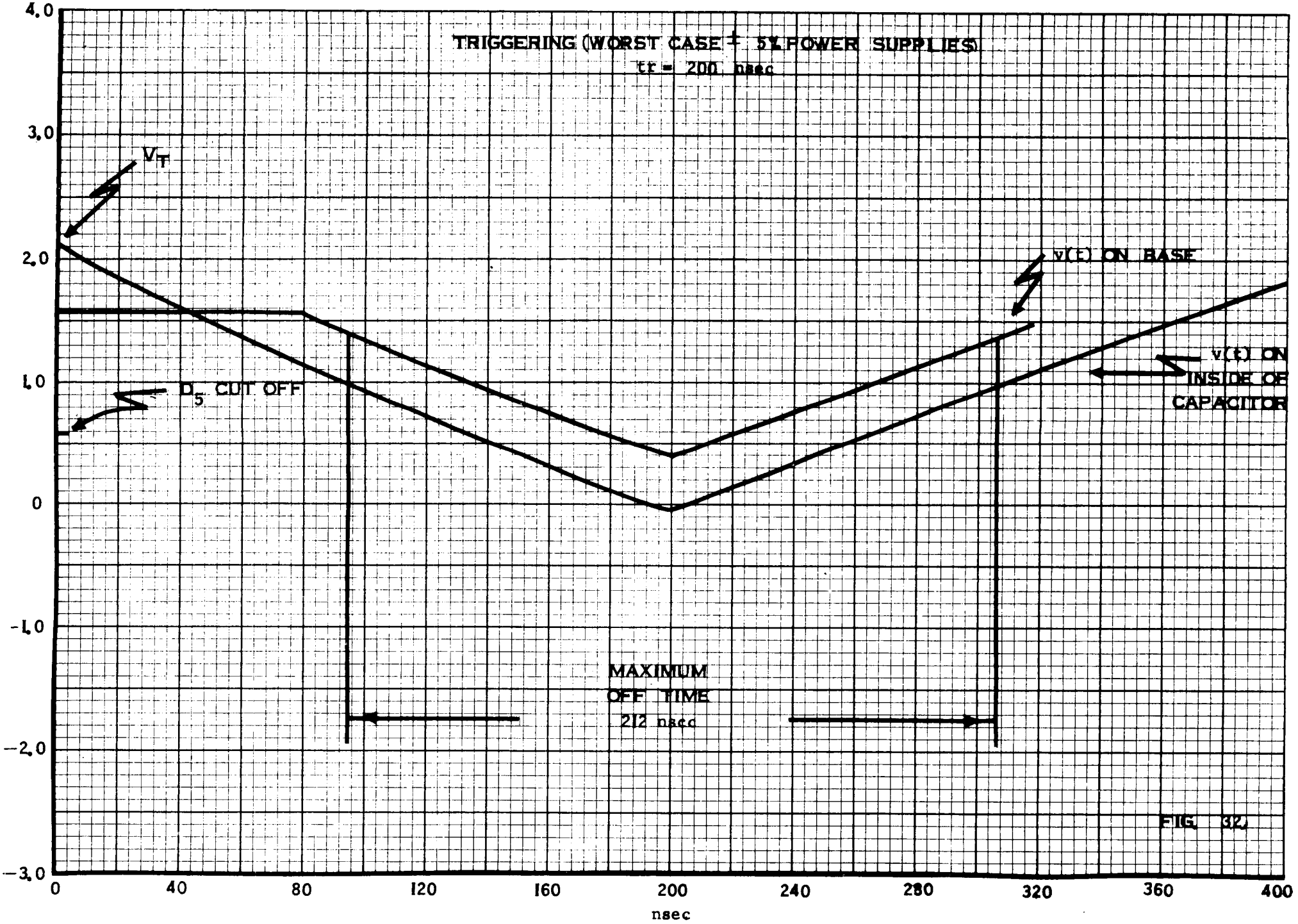

TRIGGERING (WORST CASE ± 5% POWER SUPPLIES)
tr = 200 nsec
V_T
v(t) ON BASE
D_5 CUT OFF
v(t) ON
INSIDE OF
CAPACITOR
MAXIMUM
OFF TIME
212 nsec
4.0
3.0
2.0
1.0
0
-1.0
-2.0
-3.0
0
40
80
120
160
200
240
280
320
360
400
nsec

FIG. 32

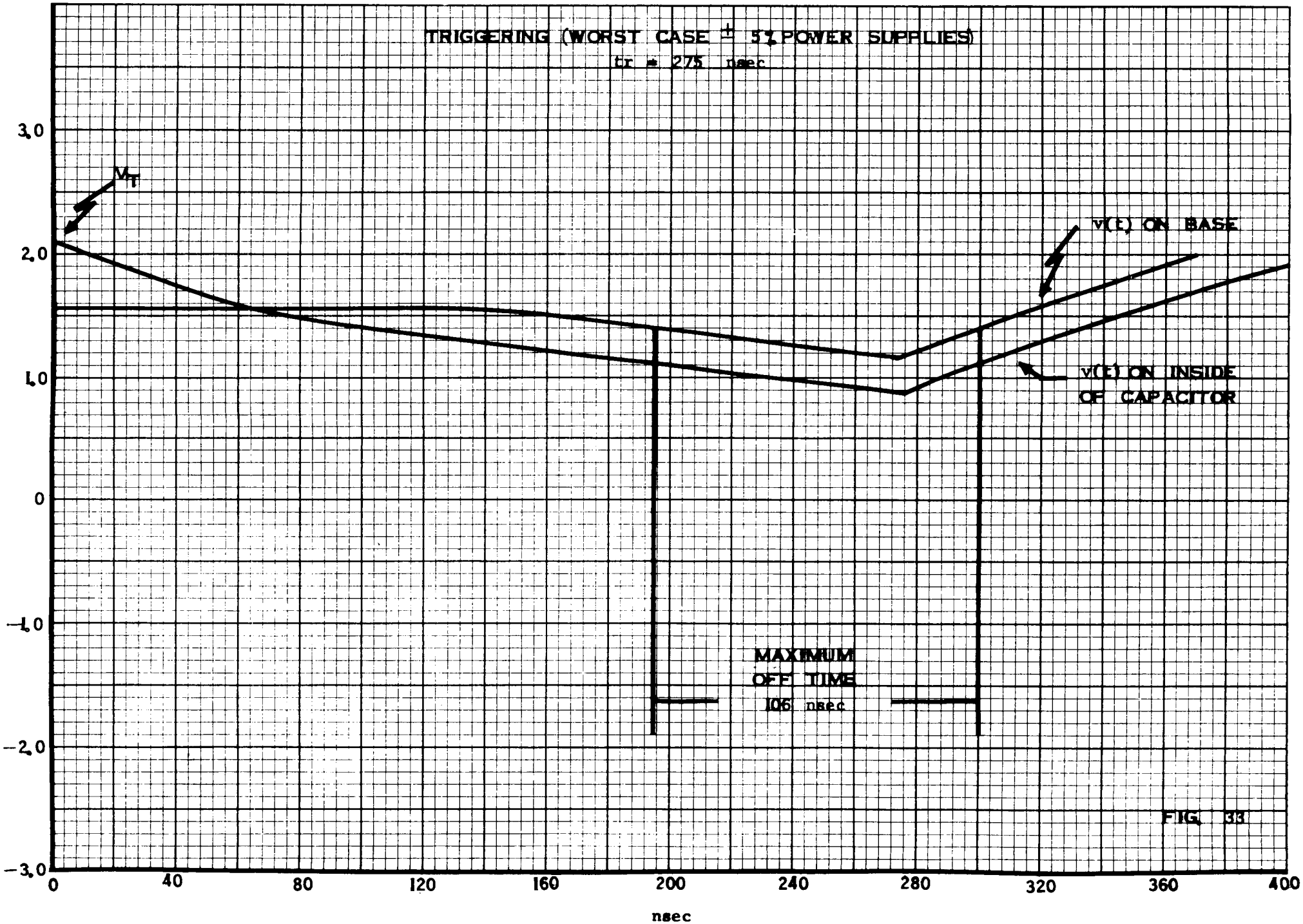

TRIGGERING (WORST CASE ± 5% POWER SUPPLIES)
tr = 275 nsec
3.0
2.0
1.0
0
-1.0
-2.0
-3.0
V_T
v(t) ON BASE
v(t) ON INSIDE OF CAPACITOR
MAXIMUM OFF TIME 106 nsec
0
40
80
120
160
200
240
280
320
360
400
nsec

FIG. 33

	A initial	A final	B initial	B final	R in time constant	ΔV	
1	1	0	1	1	$\approx R_5 + R_{11}$	-3	Getting set to be triggered.
2	0	1	1	1	$R_9 + R_{11}$	+3	Conditioning gate.
3	1	0	0	0	R_5	-3	No action.
4	0	1	0	0	R_9	+3	Conditioning gate.
5	1	1	1	0	R_9	4.2	Gating out.
6	1	1	0	1	$R_9 + R_{11}$	-4.2	No action.
7	0	0	1	0			Triggering
8	0	0	0	1	$\approx R_5 + R_{11}$	-3	Charging capacitor for triggering.
9	1	0	1	0	$\approx R_2$	-1.2	The RC delay prevents triggering.
10	0	1	0	1	$R_9 + R_{11}$	+1.2	Conditioning gate.
11	1	0	0	1	$R_5 + R_{11}$	-1.2	Charging capacitor for triggering.
12	0	1	1	0			Triggering.

The longest time constant is $R_9 + R_{11}$ which occurs for cases 2, 6, and 10. Case 6 doesn't matter since nothing is happening. Case 2 is the worst case since it has the largest ΔV. This case can occur when the F/F is connected in a shift register or when it is conditioned by any logic element. When it is connected as a shift register the difference in charge on the two capacitors will guarantee no false triggering.

2. 500K.C. Flip Flop

The worst case to be considered is when a single input is conditioned.

R_9 = 12K

R_{11} = 6.2K

C = 75 pf

The worst case time constant is equal to:

$= 1.04\ (12 \times 10^3 + 6.2 \times 10^3) \times 1.05 \times 75 \times 10^{-12}$

= 1.49 usec.

In two microseconds the voltage on the inside of the capacitor has charged to

$= Vt + (Vcc - Vt)\ (1-e^{-t/\tau})$

From Computer Run #5

Vcc = 5.75

Vt = 2.15

$= 2.5 + (3.6)\ (1-e^{-1.34})$

= 4.81

Before triggering would occur the voltage on the inside of the capacitor would have to be decreased 4.81 - 2.15 + V_{NI} volts.

$V_{NI} = Vt - VbeQ_1 - VbeQ_2 + VD_3$

$= 2.15 - 0.81 - 2.5 \times 10^{-3} \times 35 - 0.7 - 2.5 \times 10^{-3} \times 35 + 0.5$

= 0.975

A total change of 3.6von the inside of the capacitor is then required to trigger the F/F. As can be seen by the plots for nominal and worst case triggering an attenuation of the input pulse of approximately

72% results. For a Vcc of 5.75 an input pulse of $Vcc-Vce-VD_7 = 5.0$ results - attenuated by 72% yields 3.6 v. Therefore 500 KC operation is guaranteed under the worst case conditions.

3. 65K.C. Flip Flop - As explained previously, R_5, R_9, and R_{11} were increased in value by almost ten times to result in a flip flop that would operate to at least 50K.C. The values chosen were

R_5 = 39K ohm

R_9 = 100K ohm

R_{11} = 39K ohm

The worst case time constant as shown in the previous 500K.C. repetition rate analysis is:

$$= \overline{R9} + \overline{R_{11}} \times \overline{C} = 1.49\,\mu \text{ sec.}$$

Then for the higher values for R_5 and R_9 the time constant is

$$= 1.04\ (100 \times 10^3 + 39 \times 10^3) \times 1.05 \times 75 \times 10^{-12}$$

$$= 11.4 \text{ sec.}$$

The maximum repetition rate is then

$$= \frac{1.49 \text{ sec.}}{11.4 \text{ sec.}} \times 500\text{K.C.}$$

$$= 65\text{K.C.}$$

This is based on the triggering and repetition rate analysis performed previously for the 500K.C. flip flop. Actually the repetition rate will be slightly greater than 65K.C. The reason for this is that during triggering less charging current will be applied to

the capacitor,(R_5, R_9 and R_{11} are larger). Therefore less voltage swing is required at the flip flop side of the capacitor for guaranteed triggering.

References:

1. G.E. Transistor Manual - Sixth Edition 1962

2. "Using Charge Concepts in Transient Analysis of Transistor Switching Circuits" Electronic Design, August 16, 1963, August 30, 1963.

3. Transistor Engineering - Phillips - McGraw-Hill 1962

4. Transient Response In Transistors - Kvammi - G.E. TIS R61EGP8

APPENDIX A

Glossary

Cib	emitter to base capacitance
Cob	collector to base capacitance
Cs	stray capacitance
E	driving potential
F	fan out/fan in
ft	gain bandwidth product
h_{FE}	beta
I_{B2}	reverse current
Ibs	current required to saturate transistor
Ico	collector to base leakage
I_{DL}	diode leakage
Ieo	emitter to base leakage
Iin	current being pulled out of Nand input
I"o"	output current capability
Power "o"	power dissipated when output of Nand is in the zero state
Power "1"	power dissipated when output of Nand is in the one state
Qb	active base charge required to permit a given collector current to flow
Qc	charge needed to charge collector depletion region
Qe	charge necessary to charge emitter depletion region
Qs	charge due to stray capacitance reflected to the base
s	Laplace domain operator

t_d	total delay time
t_{d_r}	turn on delay time
t_f	voltage rise time; turn off time
t_{fN}	turn off time required to reach Vc
tod	turn off delay
tr	rise time (voltage fall time)
tri	rise time of input
ts	storage time
Bv	negative power supply
Vc	Vbe + V_{D4} + V_{D5} - V_{D1} of Nand
V_{base}	"off" voltage on the base emitter junction of the Nand
Vcc	positive power supply
Vi	initial voltage
V_{NI}	noise immunity voltage
V_Q	voltage at which time base current is pulled out of Nand by driving source.
V_T	threshold voltage
V_{t1}	voltage on inside of tirggering capacitor at time the noise immunity is exceeded.
V_{t2}	voltage on inside of triggering capacitor at the time D5 is cut off.
V_{tr}	voltage on inside of triggering capacitor at the time the input ramp has ceased.
V_1	voltage on the base of the outer "off" transistor in the F/F analysis.
V_2	Vbe_1 + Vbe_2 in F/F analysis.

τ_a	active region time constant
τ_s	stored charge time constant
#	number of Nand loads
*	number of F/F input loads

APPENDIX B

Explanation of Computer Format and Runs

The purpose of this section will be to work completely through a computer run - from compiling of the linear equation in the computer language (actually an intermediate language) to analyzing the computer print-out.

A. The first step is to write the linear circuit equations in matrix form i.e., the unknowns on the left with their coefficients, and equal to a constant on the right.

$$a_{11}\, x_1 + a_{12}\, x_2 + a_{13}\, x_3 = K_1$$
$$a_{21}\, x_1 + a_{22}\, x_2 + a_{23}\, x_3 = K_2$$
$$a_{31}\, x_1 + a_{32}\, x_2 + a_{33}\, x_3 = K_3$$

In some cases, the coefficients are zero.

Consider the first set of Nand equations.

1. $$g_1 \; F\left(\frac{V_{cc} - V_{ce} - V_{D1}}{0.97}\right) - h_{FE}\left(\frac{V_{cc} - V_{D4} - V_{D5} - V_{be}}{1.03}\right)$$
$$F\left(\frac{V_{ce} + V_{D1} - V_{D2} - V_{D3} - V_b}{R_2}\right) - I_{DL} - I_{co} - I_{eo} - h_{FE}\left(\frac{V_{be} + V_b}{R_2}\right)$$

2. $$g_1 \; (V_{cc} - V_{ce} - V_{D1}) - I_{in} = -I_{co} - I_{eo} - I_{DL} + \frac{V_{ce} + V_{D1} - V_{D2} - V_{D3} - V_b}{R_2}$$

3. $V_{base} = V_{ce} + V_{D1} - V_{D2} - V_{D3}$

4. $g1 \quad (V_{cc} - VD4 - VD5 - V_{be}) - I_b = \frac{V_{be} + V_b}{R_2}$

5. $h_{FE} \quad I_b - I''o'' = \frac{V_{cc} - V_{ce}}{R_4}$

In this particular case for a 5 x 5 martix and for the second equation,

$a_{21} = (V_{cc} - V_{ce} - V_{D1})$

$a_{22} = -1$

$a_{23}, a_{24}, a_{25} = 0$

$K_2 = -(I_{co} + I_{eo} + I_{DL}) + \frac{V_{ce} + V_{D1} - V_{D2} - V_{D3} + V_b}{R_2}$

$x_1 = g_1$

$x_2 = I_{in}$

$x_3 = V_{base}$

$x_4 = I_b$

$x_5 = I'o''$

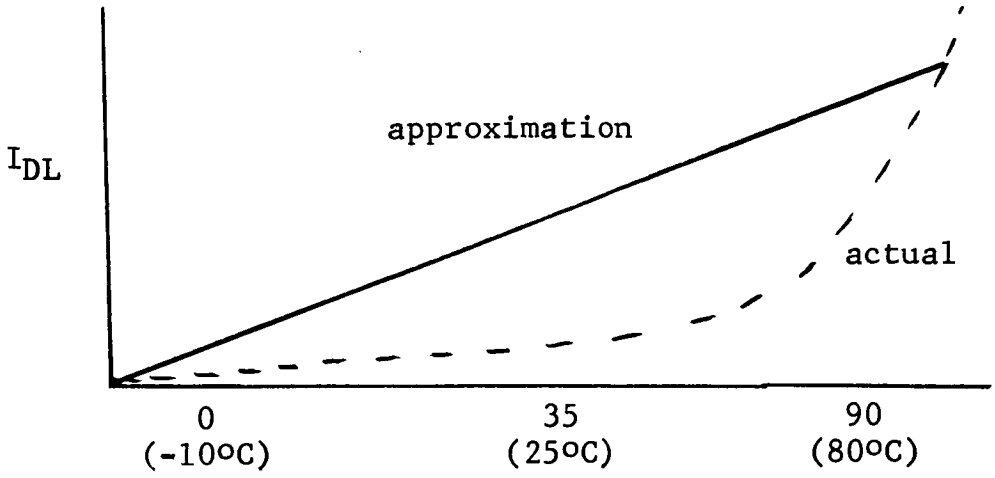
B. These equations must be expanded further in order to express their temperature dependence. The temperature varying parameters are expressed as follows:

a. I_{co}, I_{eo}, and I_{D_L} - collector to base, emitter to base and diode leakages.

$$I_{DL} = \frac{128\ I_{DLn}\ T}{90} = 1.42\ I_{DLn}\ T$$

90 - the total temperature swing
T - temperature (^oC) but shifted $+10^o$ for ease of computer handling.

128 - a forcing function, when divided by 90, forces the leakage at the high temperature to be worst case. The forcing function is derived from the rule of thumb of leakage doubling every 8°C.



b. V_D and V_{be} - diode voltage drops, and saturated base emitter voltage drops.

$$V_D = V_{Dn} - TC_D \ (T - 35)$$

V_{Dn} - nominal voltage drop at 25°C

TC_D - temperature coefficient of diode at its operating point.

The diode voltage drop is the difference between the nominal voltage drop and the resultant voltage due to its temperature coefficient. The equation will cause the temperature varying term to subtract from the nominal for an increase in temperatrue and to add for a decrease in temperature.

h_{FE} (β) - transistor current gain

$h_{FE} = h_{FE_n} + h_{FE_n} TC_{h_{FE}} (T - 35)$

h_{FE_n} - nominal h_{FE}; the minimum nominal h_{FE} and the maximum temperature coefficient yield a minimum h_{FE} of 25 at $-10^{o}C$.

The above expression for h_{FE} assumes a linear relationship with temperature.

All temperature dependent terms are then substituted into the equation. The matrix elements and the constant for the second equation becomes

$$a_{21} = (V_{cc} - V_{ce} - V_{D_{in}} + TC_{D_1} (T - 35)$$

$$a_{22} = -1$$

$$a_{23}, a_{24}, a_{25} = 0$$

$$K_2 = -142\ T\ (I_{con} + I_{eon} + I_{DLn}) + \frac{V_{ce} + V_{D_{in}} - TC_{D1} (T - 35) - V_{D2n} + TC_{D_2} (T - 35) - V_{D3n} + TC_{D3}(T-35)+V_b}{R_2}$$

This procedure is continued until all equations contain the temperature dependent terms.

The next step is to write a parameter list containing the nominal, minimum and maximum values of a parameter at $25^{o}C$. Each parameter is assigned a number (See Computer Run #1).

The numbers corresponding to a parameter are then substituted in the equations. The matrix elements and the constant for the second

equation becomes,

$$a_{21} = 02 - 03 - 04 + 05 \ \&(06 - 07)$$

$$a_{22} = -01$$

$$a_{23},\ a_{24},\ a_{25} = 0$$

$$K_2 = -08 \ \& \ -06 \ \& \ (09 + 10 + 11) + (03 + 04 - 05 \ \&(06 - 07)$$
$$- 12 \ \& 13 + 12 \ \& 14 \ \& \ (06 - 07) + 15) \ /16$$

This procedure is continued until all equation matrix elements and constants are written in this number notation. The entire set is shown in Computer Run #1.

The parameter list, matrix elements and constants in the number notation are then typed into the computer and the equations are solved.

Computer Print-Out

Refer to Computer Run #1.

Page 1 - This page contains the matrix size and the parameter list. The parameters are assigned numbers and the nominal, minimum, and maximum values of the parameter at 25°C are listed.

Page 2 - This page contains the matrix elements and constants for each equation.

Page 3 - At the top of page 3 is the nominal solutions for the unknowns. The unknowns are typed out horizontally in the same order as they are listed in the matrix.

The partials are then solved for with respect to each parameter. If it is not desired to have the partials of the unknowns with

respect to a particular parameter, then a minus sign must be entered in the maximum column of the parameter list for that parameter. As a further explanation of the partials, the first block of partials is expanded.

Page 4 - This page contains additional partials. At the bottom of the page is the first extreme case solution. The solutions given are for the maximum g_1 and the solution for all the other unknowns when g_1 is a maximum.

Page 5 - The extreme case solutions are continued in maximum, minimum order. The maximum solution for the unknown is given first, followed by the minimum solution. This is continued until all extreme cases have solved. The last set of solutions is meangingless and in later Recomp II programs, it will be deleted.

At the bottom of the page and the top of page 6, parameters have been changed.

Pages 6 - 10 - These pages contain nominal and extreme solutions when various parameters are changed.

APPENDIX C

COMPUTER RUNS

Computer Run #1 (Nand)

Part Assumptions and Their Temperature Dependence

The operating points used for the first run were first approximations.

A. $V_{D_{in}}$ = forward voltage drop @ 25°C and I_f = 0.8 ma - from Fairchild curves (FD643)

	Nom.	Min.	Max.
$V_{D_{in}}$	= 0.550	0.528	0.593
T. C. D_1	= 2.35×10^{-3}	2.2×10^{-3}	2.43×10^{-3}

B. V_{D_2} and $V_{D_{3n}}$ = forward voltage drop @ 25°C and I_f = 60 μa - from Fairchild curves (FD306)

	Nom.	Min.	Max.
$V_{D_{2n}} = V_{D_{3n}}$	= 0.540	0.522	0.560
T. C. D_2 or D_3	= 2.39×10^{-3}	2.3×10^{-3}	2.48×10^{-3}

C. $V_{D_{4n}}$ and $V_{D_{5n}}$ = forward voltage drop @ 25°C and I_f = 0.5 ma - from Fairchild curves (FD306)

	Nom.	Min.	Max.
$V_{D_{4n}} = V_{D_{5n}}$	= 0.625	0.610	0.640
T. C. D_4 or D_5	= 2.11×10^{-3}	2.00×10^{-3}	2.22×10^{-3}

D. V_{ben} at 25°C and I_f = 0.5 ma - from Fairchild specification

	Nom.	Min.	Max.
V_{ben}	0.745	0.730	0.760
TC_{be}	2.0×10^{-3}	1.8×10^{-3}	2.2×10^{-3}

E. I_{con} at 25°C and 5 v reverse bias - from Fairchild specification

	Nom.	Min.	Max.
I_{co}	4×10^{-9}	1×10^{-9}	25×10^{-9}

F. I_{eon} at 25°C and 5 v reverse bias - from Fairchild specification

	Nom.	Min.	Max.
I_{eo}	7×10^{-9}	1×10^{-9}	100×10^{-9}

G. I_{DLn} at 25°C and 5 v reverse bias - from Fairchild curves

	Nom.	Min.	Max.
I_{DLn}	0.1×10^{-9}	0.05×10^{-9}	0.15×10^{-9}

H. h_{FE} - same as for F/F.

6/17/64

J.P.L. Nand

Computer Run #1

MATRIX SIZE : 5

PARAMETERS :		NOM	MIN	MAX
1 :	I	1	1	-1
2 :	V_{cc}	5.0	4.25	5.75
3 :	V_{ce}	0.2	0.1	0.3
4 :	V_{D1n}	0.550	0.528	0.593
5 :	T_{cD_1}	2.35-3	2.22-3	2.43-3
6 :	T	35	1-10	90
7 :	35	35	35	-35
8 :	1.42	1.42	1.42	-1.42
9 :	I_{con}	4-9	1-9	25-9
10 :	I_{con}	7-9	1-9	100-9
11 :	I_{BLn}	0.1-9	.05-9	.15-9
12 :	2	2	2	-2
13 :	$V_{D2n} = V_{D3n}$	.540	.522	.560
14 :	$T_{cD_2} = T_{cD_3}$	2.39-3	2.3-3	2.48-3
15 :	V_b	3.0	2.55	3.45
16 :	R_2	60+3	58.2+3	61.8+3
17 :	$V_{D4n} = V_{D5n}$	.625	.610	.640
18 :	$T_{cD_4} = T_{cD_5}$	2.11-3	2.00-3	2.22-3
19 :	V_{ben}	.745	.730	.760
20 :	$T_{c\,be}$	2.0-3	1.8-3	2.2-3
21 :	F	10	10	10
? :	0.97	.97	.97	-.97
23 :	β_n	60	29.2	80
24 :	$T_c\beta$	.007	.005	.009
25 :	1.03	1.03	1.03	-1.03
26		1.0	1.0	1.0

```
20 :      R4      1+0                1+0                1+0

27 :

MATRIX ELMTS

A  1,  1 (21&02-21&03-21&04+21&05&(06-07))/22-(23+23&24&06-07&23&24)&
         (02-12&17+12&18&06-12&18&07-19+20&06-20&07)/25

A  1,  2

A  1,  3

A  1,  4

A  1,  5

C  1      21&(03+04-05&06+05&07-12&13+12&14&06-12&14&07+15)/16
         -21&08&06&(09+10+11)-(23+23&24&06-23&24&07)&(19-20&06+20&07+15)/16

A  2,  1 02-03-04+05&(06-07)

A  2,  2 -01

A  2,  3

A  2,  4

A  2,  5

C  2     -08&06&(09+10+11)+(03+04-05&(06-07)-12&13+12&14&(06-07)+15)/16

A  3,  1

A  3,  2

A  3,  3 01

A  3,  4

A  3,  5

C  3      03+04-05&(06-07)-12&13+12&14&(06-07)

A  4,  1 02-12&17+12&18&(06-07)-19+20&(06-07)

A  4,  2

A  4,  3

A  4,  4 -01

A  4,  5

C  4      (19-20&(06-07)+15)/16

A  5,  1

A  5,  2

A  5,  3

A  5,  4 -23-23&24&(06-07)

A  5,  5 01
```

C 5 -(02-03)/20

g_1	I_{in}	V_{base}	I_b	I_o	Nominal Solutions
+.25105 - 4	+.61653 - 4	-.33000 + 0	+.13023 - 4	+.78132 - 3	3

-.9007 - 5	
.1362 - 4	
-.0000 + 0	$\frac{\Delta(\text{unknown})}{\Delta V_{cc}}$
-.2411 - 5	
-.1447 - 3	
-.3242 - 5	
-.5554 - 4	
+.1000 + 1	$\frac{\Delta}{\Delta V_{cc}}$
-.9741 - 5	
-.5845 - 3	
-.3241 - 5	
-.5553 - 4	
+.1000 + 1	$\frac{\Delta}{\Delta V_{D_1}}$
-.9738 - 5	
-.5843 - 3	
+.0000 + 0	
+.0000 + 0	
-.0000 + 0	$\frac{\Delta}{\Delta T_{cD_1}}$
+.0000 + 0	
+.0000 + 0	
-.1185 - 6	
-.5009 - 6	
+.2430 - 2	$\frac{\Delta}{\Delta T}$
.1670 - 6	
-.4575 - 5	
-.3787 + 1	
-.6580 + 2	
-.0000 + 0	$\frac{\Delta}{\Delta I_{co}}$
-.1138 + 2	
-.6828 + 3	
-.3787 + 1	
-.6580 + 2	
-.0000 + 0	$\frac{\Delta}{\Delta I_{eo}}$
-.1138 + 2	
-.6828 + 3	
+.3787 + 1	
+.6580 + 2	
-.0000 + 0	$\frac{\Delta}{\Delta I_{D_L}}$
+.1138 + 2	
+.6828 + 3	
+.2540 - 5	
+.4413 - 4	
-.2000 + 1	$\frac{\Delta}{\Delta V_{D_2}}$
+.7633 - 5	
.1580 - 3	
+.0000 + 0	
+.0000 + 0	
-.0000 + 0	$\frac{\Delta}{\Delta T_{cD_2}}$
+.0000 + 0	
+.0000 + 0	

$\frac{\Delta g_1}{\Delta V_{cc}} = -0.9007 \times 10^{-5}$ mhos/volt

$\frac{\Delta I_{in}}{\Delta V_{cc}} = +0.1362 \times 10^{-4}$ amps/volt

$\frac{\Delta V_{base}}{\Delta V_{cc}} = 0.0$ volts/volt

$\frac{\Delta I_b}{\Delta V_{cc}} = -0.2411 \times 10^{-5}$ amps/volt

$\frac{\Delta I_o}{\Delta V_{cc}} = -0.1447 \times 10^{-3}$ amps/volt

+.6350 - 5
+.1032 - 4 $\frac{\Delta}{\Delta V_b}$
-.0000 + 0
+.2415 - 5
+.1449 - 3

-.4149 - 9
1029 - 8 $\frac{\Delta}{\Delta R_2}$
.0000 + 0
-.2169 - 9
-.1302 - 7

+.2241 - 4
+.9525 - 4 $\frac{\Delta}{\Delta V_{b4}}$
-.0000 + 0
+.1686 - 4
+.1011 - 2

+.0000 + 0
+.0000 + 0 $\frac{\Delta}{\Delta T_{cb4}}$
-.0000 + 0
+.0000 + 0
+.0000 + 0

+.1883 - 4
+.8001 - 4 $\frac{\Delta}{\Delta V_{be}}$
-.0000 + 0
+.1466 - 4
+.8796 - 3

+.0000 + 0
+.0000 + 0 $\frac{\Delta}{\Delta T_{cbc}}$
- 0000 + 0
0000 + 0
+.0000 + 0

+.4966 - 6
+.2111 - 5 $\frac{\Delta}{\Delta F}$
-.0000 + 0
+.1492 - 5
+.8954 - 4

-.8140 - 7
-.3460 - 6 $\frac{\Delta}{\Delta \beta}$
-.0000 + 0
-.2446 - 6
-.1801 - 5

+.0000 + 0
+.0000 + 0 $\frac{\Delta}{\Delta T_{c\beta}}$
-.0000 + 0
+.0000 + 0
+.0000 + 0

+.0000 + 0
+.0000 + 0 $\frac{\Delta}{\Delta R_4}$
-.0000 + 0
+.0000 + 0
.1752 -15

Max g_1
+.50520 - 3 +.17376 - 2 -.58055 + 0 +.92543 - 3 +.18510 - 1 Solutions when g_1 is maximum

Min g_1

+.13128 - 4 +.84613 - 5 -.20100 - 1 +.26028 - 5 +.26543 - 3 Solutions when g_1 is min.

Max I_{in}

50520 - 3 +.17376 - 2 -.58055 + 0 +.92543 - 3 +.18510 - 1

Min I_{in}

+.13128 - 4 +.84613 - 5 -.20100 - 1 +.26028 - 5 +.26543 - 3

Max V_{base}

+.27172 - 4 +.50816 - 4 -.20100 - 1 +.16507 - 4 +.61453 - 3

Min V_{base}

+.25073 - 4 +.79861 - 4 -.58055 + 0 +.17826 - 4 +.97679 - 3

Max I_b

+.50520 - 3 +.17376 - 2 -.58055 + 0 +.92543 - 3 +.18510 - 1

Min I_b

+ 13128 - 4 +.84613 - 5 -.20100 - 1 +.26028 - 5 +.26543 - 3

Max I_o

+.50520 - 3 +.17376 - 2 -.58055 + 0 +.92543 - 3 +.18510 - 1

Min I_o

+.13128 - 4 +.84613 - 5 -.20100 - 1 +.26028 - 5 +.26543 - 3

+.82469 - 4 +.25706 - 3 -.49930 + 0 +.11550 - 3 +.27823 - 2

PARAMETER

16

1.)

Changed 60K (R_2) to 100K -

.97+5

1.03+5

PARAMETER

13

.525

.+90

.560

Changed value and temperature coefficient of V_{B2} since R_3 is being increased to 100K.

14

2.5-3

2.38-3

2.6-3

16

1+5

.97+5

1.03+5

g_1	I_{in}	V_{base}	I_b	I_o	
15023 - 4	+.36308 - 4	-.30000 + 0	+.76953 - 5	+.46167 - 3	Nominal
Max g_1					
+.64192 - 4	+.19755 - 3	-.58895 + 0	+.82750 - 4	+.19272 - 2	
Min g_1					
+.79797 - 5	+.11147 - 4	+.52700 - 1	+.19851 - 5	+.21508 - 3	
	Max I_{in}				
+.64192 - 4	+.19755 - 3	-.58895 + 0	+.82750 - 4	+.19272 - 2	
	Min I_{in}				
+.79797 - 5	+.11147 - 4	+.52700 - 1	+.19851 - 5	+.21508 - 3	
		Max V_{base}			
15111 - 4	+.25493 - 4	+.52700 - 1	+.67829 - 5	+.29400 - 3	
		Min V_{base}			
+.14504 - 4	+.45278 - 4	-.58895 + 0	+.88170 - 5	+.51331 - 3	

Max I_b

+.64192 - 4 +.19755 - 3 -.58895 + 0 +.82750 - 4 +.19272 - 2

Min I_b

79797 - 5 +.11147 - 4 +.52700 - 1 +.19851 - 5 +.21508 - 3

Max I_o

+.64192 - 4 +.19755 - 3 -.58895 + 0 +.82750 - 4 +.19272 - 2

Min I_o

+.79797 - 5 +.11147 - 4 +.52700 - 1 +.19851 - 5 +.21508 - 3

PARAMETER

23

60

24.2

80

Decreased β to 20 at -10°C

g_1 I_{in} V_{base} I_b I_o

+.15023 - 4 +.36308 - 4 -.30000 + 0 +.76953 - 5 +.46167 - 3 } Nominal

Max g_1

-.47227 - 3 -.16999 - 2 -.58895 + 0 -.97815 - 3 -.16215 - 1

Min g_1

+.79979 - 5 +.11237 - 4 +.52700 - 1 +.20597 - 5 +.21003 - 3

Max I_{in}

-.47227 - 3 -.16999 - 2 -.58895 + 0 -.97815 - 3 -.16215 - 1

Min I_{in}

+.79979 - 5 +.11237 - 4 +.52700 - 1 +.20597 - 5 +.21003 - 3

Max V_{base}

+.16635 - 4 +.30793 - 4 +.52700 - 1 +.10773 - 4 +.33236 - 3

Min Vbase

+.14686 - 4 +.46194 - 4 -.58895 + 0 +.94499 - 5 +.51780 - 3

Max Ib

-.47227 - 3 -.16999 - 2 -.58895 + 0 -.97815 - 3 -.16215 - 1

Min Ib

+.79979 - 5 +.11237 - 4 +.52700 - 1 +.20597 - 5 +.21003 - 3

Max I0

-.47227 - 3 -.16999 - 2 -.58895 + 0 -.97815 - 3 -.16215 - 1

Min I0

+.79979 - 5 +.11237 - 4 +.52700 - 1 +.20597 - 5 +.21003 - 3

PARAMETER

23

0

34.2

80

Raised β to 29 at -10°C

g1 Iin V base Ib I0

+.15023 - 4 +.36308 - 4 -.30000 + 0 +.76953 - 5 +.46167 - 3 } Nominal

Max g1

+.63301 - 4 +.19440 - 3 -.58895 + 0 +.80989 - 4 +.18973 - 2

Min g1

+.79979 - 5 +.11237 - 4 +.52700 - 1 +.20597 - 5 +.21003 - 3

Max Iin

..63301 - 4 +.19440 - 3 -.58895 + 0 +.80989 - 4 +.18973 - 2

Min Iin

+.79979 - 5 +.11237 - 4 +.52700 - 1 +.20597 - 5 +.21003 - 3

Max V_{base}

+.15093 - 4 +.25429 - 4 +.52700 - 1 +.67351 - 5 +.29364 - 3

Min V_{base}

+.14686 - 4 +.46194 - 4 -.58895 + 0 +.94499 - 5 +.51780 - 3

Max I_b

+.63301 - 4 +.19440 - 3 -.58895 + 0 +.80989 - 4 +.18973 - 2

Min I_b

+.79979 - 5 +.11237 - 4 +.52700 - 1 +.20597 - 5 +.21003 - 3

Max I_o

+.63301 - 4 +.19440 - 3 -.58895 + 0 +.80989 - 4 +.18973 - 2

Min I_o

+.79979 - 5 +.11237 - 4 +.52700 - 1 +.20597 - 5 +.21003 - 3

PARAMETER

16

60+3

58.2+3

61.8+3

23

60

34.2

80

Reduced R_2 back to 60K, but increased β to 29 at -10°C,

g_1	I_{in}	V_{base}	I_b	I_o	
+.25067 - 4	+.60991 - 4	-.30000 + 0	+.12908 - 4	+.77445 - 3	} Nominal
Max g_1					
+.10550 - 3	+.32400 - 3	-.58895 + 0	+.13498 - 3	+.31622 - 2	

Min g_m

+.13385 - 4 +.21213 - 4 +.52700 - 1 +.36594 - 5 +.37320 - 3

Max I_{in}

+.10550 - 3 +.32400 - 3 -.58895 + 0 +.13498 - 3 +.31622 - 2

Min I_{in}

+.13385 - 4 +.21213 - 4 +.52700 - 1 +.36594 - 5 +.37320 - 3

Max V_{bias}

+.25174 - 4 +.42615 - 4 +.52700 - 1 +.11275 - 4 +.49161 - 3

Min V_{bias}

+.24476 - 4 +.76991 - 4 -.58895 + 0 +.15750 - 4 +.86303 - 3

Max I_b

+.10550 - 3 +.32400 - 3 -.58895 + 0 +.13498 - 3 +.31622 - 2

Min I_b

+.13385 - 4 +.21213 - 4 +.52700 - 1 +.36594 - 5 +.37320 - 3

Max I_o

+.10550 - 3 +.32400 - 3 -.58895 + 0 +.13498 - 3 +.31622 - 2

Min I_o

+.13385 - 4 +.21213 - 4 +.52700 - 1 +.36594 - 5 +.37320 - 3

J.P.L NAND

Computer Run #2

MATRIX SIZE : 7

PARAMETERS :		NOM	MIN	MAX
1 :	I	1	1	-1
2 :	V_{cc}	5.0	4.25	5.75
3 :	V_{ce}	0.2	0.1	0.3
4 :	$V_{D_{in}}$	0.550	0.528	0.593
5 :	$T_{c\ D_1}$	2.35-3	2.22-3	2.43-3
6 :	T	35	1-9	90
7 :	35	35	35	-35
8 :	1.42	1.42	1.42	1.42
9 :	$I_{co\ nom}$	4-9	1-9	25-9
10 :	$I_{eo\ nom}$	7-9	1-9	100-9
11 :	$I_{D_L\ nom}$	0.1-9	0.05-9	0.15-9
12 :	2	2	2	-2
13 :	$V_{D_{Lnor}} V_{D_{3n}}$	0.540	0.522	0.560
14 :	$T_{c\ D_2 \& D_3}$	2.39-3	2.3-3	2.48-3
15 :	V_b	3.0	2.55	3.45
16 :	R_3	100+3	97+3	103+3
17 :	$V_{D_4 nor}$ $V_{D_5 n}$	0.625	0.610	0.640
18 :	$T_{c\ D_4 \& D_5}$	2.11-3	2.00-3	2.22-3
19 :	$V_{be\,n}$	0.745	0.730	0.760
20 :	$T_{c\ b\text{-}e}$	2.0-3	1.8-3	2.2-3
21 :	R_1	10+3	9.7+3	10.3+3
22 :	0.97	0.97	0.97	-0.97
23 :	β_{nom}	60	29.2	80

24 :	T_c/β	0.007	0.005	0.009
25 :	1.03	1.03	1.03	-1.03
26 :	R_4	1+δ	1+δ	1+δ
27 :		2	2	-
27 :	# of diode inputs	2	2	6
28 :	g_1	1-4	1.03-4	0.97-4
29 :	g_3	1-5	1.03-5	0.97-5
30 :				

MATRIX ELMTS

A 1, 1 01 I_{in}

A 1, 2

A 1, 3

A 1, 4

A 1, 5

A 1, 6

A 1, 7

C 1 (02-03-04+05&(06-07))/21+08&06&(09+10+11&27)-(03+04-05&(06-07)
-12&13+12&14&(06-07)÷15)/16

A 2, 1

A 2, 2 01 V_{base}

A 2, 3

A 2, 4

A 2, 5

A 2, 6

A 2, 7

C 2 03+04-05&(06-07)-12&13+12&14&(06-07)

A 3, 1

A 3, 2

A 3, 3 01 I_b
01

A 3, 4

A 3, 5

A 3, 6

A 3, 7

```
C  3     (02-12&17+12&18&(06-07)-19+20&(06-07))/21-(19-20&(06-07)+15)/16
          +27&08&06&11
A  4,  1
A  4,  2
A  4,  3 -(23+23&24&06-07&23&24)/(28&(02-03-04+05&06-05&07)+08&06&(09+10+11&27)
         -29&(03+04-05&(06-07)-12&13+12&14&(06-07)+15))
A  4,  4 01
A  4,  5                                  F = Fo/Fi
A  4,  6
A  4,  7
C  4
A  5,  1
A  5,  2
A  5,  3 -23-23&24&(06-07)
A  5,  4                                  I"o"
A  5,  5 01
A  5,  6
A  5,  7
C  5     -(02-03)/26
A  6,  1
A  6,  2
A  6,  3
A  6,  4                                  P w "1"
A  6,  5
A  6,  6 01
A  6,  7
C  6     02&(02-03-04+05&06-05&07)/21
A  7,  1
A  7,  2
A  7,  3
A  7,  4                                  P w "0"
A  7,  5
A  7,  6
A  7,  7 01
```

```
C  7     02&(02-12&17+12&18&06-12&18&07-19+20&06-20&07)/21+15&(19-20&06
          +20&07+15)/16
```

I in	V base	I b	F	I "0"	
+.39886 - 3	-.33000 + 0	+.26306 - 3	+.39572 + 2	+.15784 - 1	} nominal solution
+.21250 - 2	+.16148 - 2				
+.1000 - 3	Pw "0"				
-.0000 + 0	Pw "1"	$\frac{\Delta}{\Delta V_{cc}}$			
+.1000 - 3					
+.5058 + 1					
+.6000 - 2					
+.9300 - 3					
+.8055 - 3					
-.1100 - 3					
+.1000 + 1					
+.0000 + 0		$\frac{\Delta}{\Delta V_{ee}}$			
+.1092 + 2					
+.1000 - 7					
-.5000 - 3					
+.0000 + 0					
-.1100 - 3					
+.1000 + 1					
+.0000 + 0		$\frac{\Delta}{\Delta V_{D_1}}$			
+.1093 + 2					
+.0000 + 0					
-.5000 - 3					
+.0000 + 0					
+.0000 + 0					
-.0000 + 0		$\frac{\Delta}{\Delta T_{cD_1}}$			
+.0000 + 0					
+.0000 + 0					
+.0000 + 0					
+.0000 + 0					
+.0000 + 0					
+.2266 - 6					
+.2430 - 2		$\frac{\Delta}{\Delta T}$			
+.6423 - 6					
+.3513 + 0					
+.1491 - 3					
+.1175 - 5					
+.3050 - 5					
+.3920 - 6					
-.0000 + 0		$\frac{\Delta}{\Delta 1.42}$			
+.7000 - 8					
-.3784 - 1					
+.4200 - 6					
+.0000 + 0					
+.0000 + 0					
+.4970 + 2					
-.0000 + 0		$\frac{\Delta}{\Delta T_{co\,nom}}$			
+.0000 + 0					
-.4931 + 7					
+.0000 + 0					
+.0000 + 0					
+.0000 + 0					
+.4970 + 2					
-.0000 + 0					
+.0000 + 0					

-.4931 + 7 +.0000 + 0 +.0000 + 0 +.0000 + 0	$\frac{\Delta}{\Delta I_{C_0\,nom}}$
+.9940 + 2 -.0000 + 0 +.9940 + 2 +.5091 + 7 +.5964 + 4 +.0000 + 0 +.0000 + 0	$\frac{\Delta}{\Delta I_{D_1\,nom}}$
+.2000 - 4 -.2000 + 1 +.0000 + 0 -.1984 + 1 +.0000 + 0 +.0000 + 0 +.0000 + 0	$\frac{\Delta}{\Delta (V_{D_2})_{or}\,\Delta (V_{D_3})}$
+.0000 + 0 -.0000 + 0 +.0000 + 0 +.0000 + 0 +.0000 + 0 +.0000 + 0 +.0000 + 0	$\frac{\Delta}{\Delta T_{c\ D_2\ or\ D_3}}$
-.1000 - 4 -.0000 + 0 -.1000 - 4 -.5125 + 0 -.6000 - 3 +.0000 + 0 +.6775 - 4	$\frac{\Delta}{\Delta V_b}$
+.2644 - 9 -.0000 + 0 +.3700 - 9 +.5578 - 4 +.2225 - 7 +.0000 + 0 -.1112 - 8	$\frac{\Delta}{\Delta R_2}$
+.0000 + 0 -.0000 + 0 -.2000 - 3 -.3009 + 2 -.1200 - 1 +.0000 + 0 -.1000 - 2	$\frac{\Delta}{\Delta (V_{D_4}\ or\ \Delta\ V_{D_5})}$
+.0000 + 0 -.0000 + 0 +.0000 + 0 +.0000 + 0 +.0000 + 0 +.0000 + 0 +.0000 + 0	$\frac{\Delta}{\Delta T_{c\ D_4\ or\ D_5}}$
+.0000 + 0 -.0000 + 0 -.1100 - 3 -.1655 + 2 -.6600 - 2	$\frac{\Delta}{\Delta V_{b\,c}}$

+.0000 + 0
-.4700 - 3

+.0000 + 0
-.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.7105 - 9

$\frac{\Delta}{\Delta T_c V_{bc}}$

-.4208 - 7
-.0000 + 0
-.2975 - 7
-.4476 - 2
-.1785 - 5
-.2104 - 6
-.1486 - 6

$\frac{\Delta}{\Delta R_1}$

+.0000 + 0
-.0000 + 0
+.0000 + 0
+.6595 + 0
+.2631 - 3
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta \beta_{nom}}$

+.0000 + 0
-.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta T_c \beta_{nom}}$

+.0000 + 0
-.0000 + 0
+.0000 + 0
+.0000 + 0
+.4752 -15
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta R_t}$

+.4970 - 8
-.0000 + 0
+.4970 - 8
+.2546 - 3
+.2982 - 6
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta(\text{\# of diode inputs})}$

+.0000 + 0
-.0000 + 0
+.0000 + 0
-.4172 + 6
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta g_1}$

+.0000 + 0
-.0000 + 0
+.0000 + 0
+.2651 + 6
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta g_3}$

Worst Case Solutions for $R_1 = 10K$ ①

I_{in}	V_{base}	I_b	$\frac{\text{Fan Out}}{\text{Fan In}}$	$I_{"0"}$	
I_{in} max					
+.53662 - 3	-.35285 + 0	+.38932 - 3	+.92273 + 2	+.46562 - 1	
+.31155 - 2	+.24947 - 2				
$P_{w("1")}$	$P_{w("0")}$				
I_{in} min					
+.28523 - 3	-.23430 + 0	+.15985 - 3	+.12640 + 2	+.38507 - 2	
+.13531 - 2	+.10162 - 2				
+.33286 - 3	V_{base} max				
+.15243 - 2	-.20100 - 1	+.23722 - 3	+.26557 + 2	+.88316 - 2	
	+.12311 - 2				
+.46117 - 3	V_{base} min				
+.28119 - 2	-.58055 + 0	+.29601 - 3	+.35206 + 2	+.16221 - 1	
	+.20850 - 2				
+.50672 - 3	-.87850 - 1	I_b max			
+.29584 - 2	+.25473 - 2	+.39889 - 3	+.10015 + 3	+.47707 - 1	
+.31369 - 3	-.49930 + 0	I_b min			
+.14625 - 2	+.98011 - 3	+.15080 - 3	+.10855 + 2	+.36328 - 2	
+.49027 - 3	-.11650 - 1	+.39889 - 3	F max		
[illegible]	[illegible]		+.97385 + 2	[illegible]	
[illegible]	[illegible]		F min		
+.14625 - 2	+.98011 - 3	[illegible]	+.11563 + 2	+.36328 - 2	
+.50672 - 3	-.87850 - 1	+.39889 - 3	+.10015 + 3	$I_{"0"}$ max	
+.29584 - 2	+.25473 - 2			+.47707 - 1	
+.31369 - 3	-.49930 + 0	+.15080 - 3	+.10855 + 2	$I_{"0"}$ min	
+.14625 - 2	+.98011 - 3			+.36328 - 2	
+.52788 - 3	-.35285 + 0	+.38058 - 3	+.91790 + 2	+.45517 - 1	
+.31155 - 2	+.25527 - 2				
$P_{w"1"}$ max					
+.24451 - 3	-.23430 + 0	+.16013 - 3	+.12979 + 2	+.40743 - 2	
+.13531 - 2	+.95315 - 3				
$P_{w"1"}$ min					
+.49597 - 3	-.87850 - 1	+.38522 - 3	+.98526 + 2	+.46072 - 1	
+.29584 - 2	+.26012 - 2				

Pw"0" max

+.32420 - 3 -.49930 + 0 +.16061 - 3 +.11249 + 2 +.38691 - 2
+.14625 - 2 +.90621 - 3

Pw"0" min

+.34425 - 3 -.49930 + 0 +.18172 - 3 +.12728 + 2 +.43776 - 2
+.15529 - 2 +.10067 - 2

PARAMETER

21

6.2+3
6.014+3
6.386+3

} Changed R_1 to 6.2 K

26

0.1613-3
0.16614-3
0.1564-3

} Changed $g_1 = 1/R_1$ to $0.1613 \times 10^{-3} = 1/6.2$ K

I in	V base	Ib	F: Fan-out / Fan-In	I "0"
+.65934 - 3 +.34274 - 2 Pw ("1")	-.33000 + 0 +.25357 - 2 Pw ("0")	+.44724 - 3	+.40696 + 2	+.26834 - 1
I in Max. +.86670 - 3 +.50249 - 2	-.35285 + 0 +.39753 - 2	+.64681 - 3	+.94709 + 2	+.77359 - 1
I in min +.46036 - 3 +.21824 - 2	-.23430 + 0 +.15465 - 2	+.28463 - 3	+.13400 + 2	+.68568 - 2
	V base Max -.20100 - 1 +.19344 - 2	+.40270 - 3	+.27149 + 2	+.14993 - 1
	V base min -.58055 + 0 +.32748 - 2	+.50294 - 3	+.36268 + 2	+.27561 - 1
		Ib max +.66207 - 3	+.10247 + 3	+.79183 - 1
		Ib Min +.27023 - 3	+.11657 + 2	+.65098 - 2
			F max +.98372 + 2	+.79183 - 1

+.80561 - 3 -.11850 - 1
+.47716 - 2 +.40606 - 2

(11)

+.52537 - 3 -.57530 + 0 +.27023 - 3 +.12406 + 2 +.65098 - 2
+.23588 - 2 +.14877 - 2
Pw "0" min

+.82206 - 3 -.87850 - 1 +.66207 - 3 +.10247 + 3 +.79183 - 1
+.47716 - 2 +.40606 - 2
I "0" max

+.52459 - 3 -.49930 + 0 +.27023 - 3 +.11657 + 2 +.65098 - 2
+.23588 - 2 +.14877 - 2
I "0" min

+.85996 - 3 -.35285 + 0 +.63807 - 3 +.94439 + 2 +.76314 - 1
+.50249 - 2 +.40333 - 2
Pw "1" max

+.48964 - 3 -.23430 + 0 +.29391 - 3 +.13591 + 2 +.70803 - 2
+.21824 - 2 +.14835 - 2
Pw "1" min

+.81131 - 3 -.[illegible] - 1 +.64701 - 3 +.[illegible] + 3 +.[illegible] - 1
+.[illegible] - 2 +.[illegible] -
Pw "0" max

+.[illegible] - 3 -.[illegible] + 0 +.27921 - 3 +.11847 + 2 +.67260 - 2
+.23588 - 2 +.14102 - 2
Pw "1" min

Transistor and Diode Bias Points for Final Computer Run
±15% Power Supply

	From Computer Run #2	T. C. D_1	V_{Din} (From Fairchild curves)
	I_{in} = 659 μa Nom.	2.41×10^{-3}	0.530
V_{D1}	= 868 μa Max.	2.60×10^{-3}	0.593
	= 480 μa Min.	2.25×10^{-3}	0.485

	From Computer Run #2	T. C. D_4	$V_{D4} = V_{D5}$ (From Fairchild curves)
	I_{b1} = 447 μa Nom.	2.25×10^{-3}	0.605
V_{D4}	= 662 μa Max.	2.5×10^{-3}	0.660
	= 270 μa Min.	2.0×10^{-3}	0.550

	From Computer Run #3	T. C. V_{be}	V_{be} (From spec sheet and part data)
	I_{b1} = 447 μa Nom.	1.4×10^{-3}	0.68
V_{be}	= 662 μa Max.	1.7×10^{-3}	0.78
	= 270 μa Min.	1.0×10^{-3}	0.63

Computer Run #3

MATRIX SIZE : 7

PARAMETERS :		NOM	MIN	MAX
1 :	I	1	1	-1
2 :	V_{cc}	5	4.25	5.75
3 :	V_{ce}	.2	.1	.25
4 :	$V_{D_1 n}$	.530	.485	.593
5 :	T_{cD_1}	2.41-3	2.25-3	2.6-3
6 :	T	35	1-9	90
7 :	35	35	35	-35
8 :	1.42	1.42	1.42	1.42
9 :	I_{con}	4-9	1-9	25-9
10 :	I_{eon}	7-9	1-9	100-9
11 :	I_{DLn}	6-9	2-9	8-9
12 :	2	2	2	-2
13 :	$V_{D_2 n} = V_{D_3 n}$	.525	.480	.570
14 :	$T_{cD_2} = T_{cD_3}$	2.39-3	2.3-3	2.62-3
15 :	V_b	3	2.55	3.45
16 :	R_2	100+3	96+3	104+3
17 :	$V_{D_4 n} = V_{D_5 n}$	.605	.55	.66
18 :	$T_{cD_4} = T_{cD_5}$	2.25-3	2-3	2.5-3
19 :	V_{ben}	.68	.63	.78
20 :	T_{cbe}	1.4-3	1-3	1.7-3
21 :	R_1	6.2+3	5.95+3	6.45+3
22 :	0.97	.97	.97	-.97

23 :	β_n	55	29.2	80
24 :	$T_{c\beta}$	.007	.005	.009
25 :	1.03	1.03	1.03	-1.03
26 :	R_4	1+8	1+8	1+8
27 :	# input diodes	2	2	9
28 :	g_1	~~1-4~~	~~1.04-4~~	~~.96-4~~ } in error corrected later.
29 :	g_2	1-5	1.04-5	.96-5
30 :				

MATRIX ELMTS

A 1, 1 01

A 1, 2

A 1, 3

A 1, 4

A 1, 5

A 1, 6

A 1, 7

C 1 (02-03-04+05&(06-07))/21+08&06&(09+10+11&27)-(03+04-05&(06-07)
-12&13+12&14&(06-07)+15)/16

A 2, 1

A 2, 2 01

A 2, 3

A 2, 4

A 2, 5

A 2, 6

A 2, 7

C 2 03+04-05&(06-07)-12&13+12&14&(06-07)

A 3, 1

A 3, 2

A 3, 3 01

A 3, 4

A 3, 5

A 3, 6

A 3, 7

C 3 (02-12&17+12&18&(06-07)-19+20&(06-07))/21-(19-20&(06-07)+15)/16+27

```
        &08&06&11
A  4,  1                                                          - 149 -
A  4,  2
A  4,  3 -(23+23&24&06-07&23&24)/(28&(02-03-04+05&06-05&07)+08&06&(09+10
           +11&27)-29&(03+04-05&(06-07)-12&13+12&14&(06-07)+15))
A  4,  4 01
A  4,  5
A  4,  6
A  4,  7
C  4
A  5,  1
A  5,  2
A  5,  3 -23-23&24&(06-07)
A  5,  4
A  5,  5 01
A  5,  6
A  5,  7
C  5      -(02-03)/26
A  6,  1
A  6,  2 -15/16
A  6,  3
A  6,  4
A  6,  5
A  6,  6 01
A  6,  7
C  6      02&(02-03-04+05&06-05&07)/21+15&15/16
A  7,  1
A  7,  2
A  7,  3
A  7,  4
A  7,  5
A  7,  6
A  7,  7 01
C  7      02&(02-12&17+12&18&06-12&18&07-19+20&06-20&07)/21+15&(19-20&06
```

```
+20&07+15)/16+02&(02-03)/26
```

I_{in}	V_{base}	I_b	$\frac{\text{Fan Out}}{\text{Fan In}}$	$I_{"o"}$	
+.66305 - 3	-.32000 + 0	+.46541 - 3	+.63780 + 2	+.25597 - 1	} Nominal solution
+.35239 - 2	+.26187 - 2				
+.1613 - 3	P_{w}"0"				
-.0000 + 0					
+.1613 - 3	P_{w}"1"				
+.6135 + 1		$\frac{\Delta}{\Delta V_{cc}}$			
+.8871 - 2					
+.1503 - 2					
+.1316 - 2					
-.1713 - 3					
+.1000 + 1					
+.0000 + 0		$\frac{\Delta}{\Delta V_{cc}}$			
+.1749 + 2					
+.1000 - 7					
-.7765 - 3					
-.5000 - 7					
-.1713 - 3					
+.1000 + 1					
+.0000 + 0		$\frac{\Delta}{\Delta V_{D_1}}$			
+.1751 + 2					
+.0000 + 0					
-.7765 - 3					
+.0000 + 0					
+.0000 + 0					
-.0000 + 0					
+.0000 + 0		$\frac{\Delta}{\Delta T_{co_1}}$			
-.3864 - 4					
+.0000 + 0					
+.1769 - 8					
+.0000 + 0					
+.3977 - 6					
+.2370 - 2					
+.9827 - 6		$\frac{\Delta}{\Delta T}$			
+.5416 + 0					
+.2334 - 3					
+.2015 - 5					
+.4716 - 5					
+.8050 - 6					
-.0000 + 0		$\frac{\Delta}{\Delta 1.42}$			
+.4200 - 6					
-.7037 - 1					
+.2310 - 4					
+.0000 + 0					
+.0000 + 0					
+.4970 + 2					
-.0000 + 0					
+.0000 + 0		$\frac{\Delta}{\Delta I_{co}}$			
-.7898 + 7					
+.0000 + 0					
+.0000 + 0					
+.0000 + 0					
+.4970 + 2					
-.0000 + 0					
+.0000 + 0		$\frac{\Delta}{\Delta I_{eo}}$			
-.7898 + 7					
+.0000 + 0					

+.0000 + 0
+.0000 + 0

+.9940 + 2
-.0000 + 0
+.9940 + 2
-.2174 + 7
+.5467 + 4
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta I_{DL}}$

+.2000 - 4
-.2000 + 1
+.0000 + 0
-.3177 + 1
+.0000 + 0
-.6000 - 4
+.0000 + 0

$\frac{\Delta}{\Delta V_{D2} \text{ or } V_{D3}}$

+.0000 + 0
-.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta T_{C\,D2 \text{ or } D3}}$

-.1000 - 4
-.0000 + 0
-.1000 - 4
+.2189 + 0
-.5500 - 3
+.5710 - 4
+.6710 - 4

$\frac{\Delta}{\Delta V_b}$

+.2653 - 9
-.0000 + 0
+.3644 - 9
+.4993 - 4
+.2004 - 7
-.7960 - 9
-.1093 - 8

$\frac{\Delta}{\Delta R_2}$

+.0000 + 0
-.0000 + 0
-.3226 - 3
-.4421 + 2
-.1774 - 1
+.0000 + 0
-.1613 - 2

$\frac{\Delta}{\Delta V_{D4} \text{ or } V_{D5}}$

+.0000 + 0
-.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta T_{C\,D4 \text{ or } D5}}$

+.0000 + 0
-.0000 + 0
-.1713 - 3
-.2347 + 2
-.9421 - 2
+.0000 + 0
-.7765 - 3

$\frac{\Delta}{\Delta V_{bc}}$

+.0000 + 0
-.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta T_{cbe}}$

-.1100 - 6
-.0000 + 0
-.8010 - 7
-.1098 - 1
-.4406 - 5
-.5499 - 6
-.4005 - 6

$\frac{\Delta}{\Delta R_1}$

+.0000 + 0
-.0000 + 0
+.0000 + 0
+.1160 + 1
+.4654 - 3
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta \beta}$

+.0000 + 0
-.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta T_{c\beta}}$

+.0000 + 0
-.0000 + 0
+.0000 + 0
+.0000 + 0
+.4752 -15
+.0000 + 0
-.2376 -14

$\frac{\Delta}{\Delta R_4}$

+.2982 - 6
-.0000 + 0
+.2982 - 6
-.6523 - 2
+.1640 - 4
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta(\#\text{ diode inputs})}$

+.0000 + 0
-.0000 + 0
+.0000 + 0
-.6714 + 6
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta g_1}$

+.0000 + 0
-.0000 + 0
+.0000 + 0
+.4262 + 6
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta}{\Delta g_3}$

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15 Volt Power Supply

PARAMETER

28

.1613-3
.1681-3
.1550-3

} Correction to initial parameter list

	Vbase Pw "1" / Pw "0"	Ib	Fan out / Fan in	Iout	
+.66305 - 3 +.35239 - 2	-.32000 + 0 +.26187 - 2	+.46541 - 3	+.38603 + 2	+.25597 - 1	} Nominal Solutions
(+.89670 - 3) Iin max. +.1821 - 2	-.40980 + 0 +.39631 - 2	+.65346 - 3	+.94460 + 2	+.78154 - 1	
(+.48215 - 3) Iin min. +.23099 - 2	-.19925 + 0 +.16309 - 2	+.30416 - 3	+.13939 + 2	+.73271 - 2	
+.56748 - 3 +.25900 - 2	(+.12250 - 1) Vbase max. +.20108 - 2	+.41986 - 3	+.27537 + 2	+.15631 - 1	
+.75972 - 3 +.46163 - 2	(-.64740 + 0) Vbase min. +.31074 - 2	+.48829 - 3	+.35228 + 2	+.26758 - 1	
+.85086 - 3 +.49391 - 2	-.15180 + 0 +.42228 - 2	(+.69932 - 3) Ib max.	+.10656 + 3	+.83638 - 1	
+.52483 - 3 +.24706 - 2	-.45725 + 0 +.14548 - 2	(+.26177 - 3) Ib min.	+.11030 + 2	+.63061 - 2	
+.81264 - 3 +.49777 - 2	+.47450 - 1 +.42802 - 2	+.68197 - 3	(+.10034 + 3) F max	+.81564 - 1	

+.53406 - 3 -.62500 + 0 +.27115 - 3 +.12233 + 2 +.65319 - 2
+.24061 - 2 +.13909 - 2

Fan out min
Fan in

I'o" max

+.85086 - 3 -.15180 + 0 +.69932 - 3 +.10656 + 3 +.83638 - 1
+.49391 - 2 +.42228 - 2

I'o' min.

+.52483 - 3 -.45725 + 0 +.26177 - 3 +.11030 + 2 +.63061 - 2
+.24706 - 2 +.14548 - 2

+.88373 - 3 -.22980 + 0 +.64149 - 3 +.93907 + 2 +.76722 - 1
+.52453 - 2 +.40324 - 2
Pw"1" max

+.49514 - 3 -.37925 + 0 +.31619 - 3 +.14187 + 2 +.76169 - 2
+.22463 - 2 +.15607 - 2
Pw'1' min

+.86633 - 3 -.30180 + 0 +.68739 - 3 +.10264 + 3 +.82212 - 1
+.51303 - 2 +.42915 - 2
Pw'0" max

+.51119 - 3 -.30725 + 0 +.27385 - 3 +.11901 + 2 +.65969 - 2
+.23192 - 2 +.13840 - 2
Pw'0" min.

~~PARAMETER~~

~~5~~

~~4.75~~

~~5.25~~

~~15~~

~~3~~

~~2.85~~

~~3.15~~

PARAMETER

28

.1613-3

..081-3

.1550 3

02

5

4.75

5.25

15

3

2.85

3.15

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5 to Power Supply

	I_{in}	V_{base}	I_b	$\frac{Fan\ out}{Fan\ in}$	I_o	
b						
+	6305 - 3	-.32000 + 0	+.46541 - 3	+.38603 + 2	+.25597 - 1	} Nominal
	+.35239 - 2	+.26187 - 2				
	Pw "1"	Pw "0"				
	$I_{in\ max.}$					
	+.80978 - 3	-.40980 + 0	+.56654 - 3	+.90708 + 2	+.67758 - 1	
	+.43092 - 2	+.32017 - 2				

I in min

+.56279 - 3 -.19925 + 0 +.38480 - 3 +.15126 + 2 +.92698 - 2
+.29161 - 2 +.21502 - 2

V base max

4839 - 3 +.12250 - 1 +.50077 - 3 +.28746 + 2 +.18644 - 1
+.33028 - 2 +.26555 - 2

V base min

+.68508 - 3 -.64740 + 0 +.41365 - 3 +.33095 + 2 +.22668 - 1
+.37988 - 2 +.24942 - 2

I b max

+.76394 - 3 -.15180 + 0 +.61240 - 3 +.10396 + 3 +.73243 - 1
+.40886 - 2 +.34386 - 2

I b min

+.60548 - 3 -.45725 + 0 +.34242 - 3 +.12519 + 2 +.82488 - 2
+.30976 - 2 +.19530 - 2

F max

+.73149 - 3 +.47450 - 1 +.60083 - 3 +.98209 + 2 +.71859 - 1
+.40946 - 2 +.34577 - 2

Fan out / Fan in min

0845 - 3 -.62500 + 0 +.34554 - 3 +.13684 + 2 +.83241 - 2
+.30663 - 2 +.19317 - 2

I o max

+.76394 - 3 -.15180 + 0 +.61240 - 3 +.10396 + 3 +.73243 - 1
+.40886 - 2 +.34386 - 2

I o min

+.60548 - 3 -.45725 + 0 +.34242 - 3 +.12519 + 2 +.82488 - 2
+.30976 - 2 +.19530 - 2

+.80283 - 3 -.22980 + 0 +.56056 - 3 +.90311 + 2 +.67046 - 1
+.43302 - 2 +.32307 - 2

+.56977 - 3 -.37925 + 0 +.39082 - 3 +.15239 + 2 +.94149 - 2
+.28870 - 2 +.21208 - 2

+.78542 - 3 -.30180 + 0 +.60648 - 3 +.99865 + 2 +.72535 - 1
2405 - 2 +.34673 - 2

Pw'o max

+.58582 - 3 -.30725 + 0 +.34848 - 3 +.13215 + 2 +.83949 - 2
+.29685 - 2 +.19233 - 2

Pw'o min

COMPUTER RUN #4

Part Assumptions and Their Temperature Dependence

The operating points used for the first run were first approximations.

A. $V_{D_{1n}}$ = Forward voltage diode D_1 @25°C at an I_f of 2 ma from Fairchild curves.

	Nom.	Min.	Max.
$V_{D_{1n}}$ =	0.30 v	0.27 v	0.33 v
$T.C.D_1$ =	3.25×10^{-3}v/°C	3.1×10^{-3}v/°C	3.45×10^{-3}v/°C

Then for computer equation $V_{D1} = V_{D_{1n}} - T.\ C._1\ (T - 35)$.

B. $V_{D_{2n}}$ = Forward voltage D_2 @ 25°C at an I_f of 0.3 ma.

	Nom.	Min.	Max.	
$V_{D_{2n}}$ =	0.51 v	0.48 v	0.55 v	From Fairchild
$T.C._2$ =	2.5×10^{-3}v/°C	2.4×10^{-3}v/°C	2.6×10^{-3}/°C	curves

Then for the computer equation $V_{D_2} = V_{D_{2n}} - T.\ C._2\ (T - 35)$.

C. $V_{D_{5n}}$ = Forward voltage diode D_5 @ 25°C at an I_f ~ 1 ma.

(For the final computer run, the value for $V_{D_{5n}}$ will be chosen at closer to 0.25 ma rather than the original 1 ma value).

	Nom.	Min.	Max.	
$V_{D_{5n}}$ =	0.57 v	0.54 v	0.61 v	From Fairchild
$T.C._5$ =	2.3×10^{-3}v/°C	2.2×10^{-3}v/°C	2.4×10^{-3}v/°C	curves

Then for the computer equation, $V_{D_5} = V_{D_{5n}} - T.\ C._5\ (T - 35)$.

D. V_{be1n} = Forward base to emitter voltage Q_1 @ 25°C and $I_b \approx 0.6$ ma, $I_c \approx 5$ ma.

	Nom.	Min.	Max.	
V_{be1n}	= 0.745 v	0.730 v	0.760 v	From a few measured units
$T.C._{be1}$	= 2.0×10^{-3}v/°C	1.8×10^{-3}v/°C	2.2×10^{-3}v/°C	Estimated

Then for the computer equation, $V_{be1} = V_{be1n} - T.\ C._{be_1}\ (T - 35)$.

E. V_{be2n} = Forward base to emitter voltage Q_2 @ 25°C and $I_b \approx 0.3$ ma, $I_c = 0.6$ ma.

	Nom.	Min.	Max.	
V_{be2n}	= 0.74 v	0.72 v	0.76 v	Few measured units.
$T.C._{be2}$	= 2×10^{-3}v/°C	1.8×10^{-3}v/°C	2.2×10^{-3}v/°C	Estimated

F. V_{be3n} = Forward base to emitter voltage Q_3 @ 25°C and $I_b \approx 2$ ma, $I_c = 30$ ua (non-saturated)

	Nom.	Min.	Max.	
V_{be3n}	= 0.54 v	0.50 v	0.58 v	Few units measured
$T.C._{be3}$	= 2.0×10^{-3}v/°C	1.8×10^{-3}/°C	2.2×10^{-3}v/°C	Estimated

Computer equation $V_{be3} = V_{be3n} - T.\ C._{be3}\ (T - 35)$.

G. I_{co} - See Nand (1.42T) I_{con}

H. I_{co} - See Nand (1.42T) I_{eon}

I. I_{DL} - See Nand (1.42T) I_{DL}

J. β_{1n} - Beta of Q_1 @ 25°C and $I_c \approx 5$ ma

	Nom.	Min.	Max.	
β_{1n} =	55	29.2	120	From Specs.
KT_1 =	0.07	.005	.009	From Data Sheet 2N914.

For computer then, $\beta_1 = \beta_{1n} + KT_1 (T - 35) \beta_{1n}$.

K. β_{3n} = Beta of Q_3 @ 25°C and $I_c \approx 30$ ua

	Nom.	Min.	Max.	
β_{3n} =	15	5.5	35	From data sheet 2N914
KT_1 =	.0083	.0063	.0103	

All diodes - FD643.

All transistors - 2N914.

500K.C. Flip-Flop - Computer Run
R_1 Fixed - Equations July 1, 1964
±15% Power Supply ±3% Resistors
Before R_{13} and R_{14} were added

Computer Run #4

TRIX SIZE : 13

PARAMETERS :	NOM	MIN	MAX
1 : α_1	1	1	1
2 : T.C.1	3.25-3	3.1-3	3.45-3
3 : T°	35	1-9	90
4 : V_{D1n} or V_{D7n}	.3	.27	.33
5 : 35	35	35	35
6 : T.C.2	2.5-3	2.4-3	2.6-3
7 : V_{D2n}	.51	.48	.55
8 : β_{1n}	55	29.2	120
9 : KT_1	.007	.005	.009
10 : V_{D5n}	.57	.54	.61
11 :	2.3-3	2.2-2	
11 : T.C.5	2.3-3	2.2-3	2.4-3
12 : V_{cc1}	.2	.1	.3
13 : V_{be1n}	.745	.73	.76
14 : T.C. b_{1-2-3}	2-3	1.8-3	2.2-3
15 : V_{cc2n}	.14	.08	.2
16 : V_{be2n}	.74	.72	.76
17 : V_{be3n}	.54	.50	.58
18 : β_{3n}	15	5.5	35
19 : KT_3	.0083	.0063	.0103
20 : I_{con}	4-9	.01-9	25-9
21 : C	1.42	1.42	1.42
22 : I_{DLn}	5.5-9	.01-9	8-9
23 : I_{con}	7-9	.01-9	100-9
24 : R_3	39+3	37.8+3	40.2+3
25 : R_5	4.7+3	4.55+3	4.85+3
26 : R_9	12.0+3	11.6+3	12.44+3

27 : R_8	100+3	97+3	103+3
28 : R_7	100+3	97+3	103+3
29 : R_1	12+3	11.64+3	12.4+3
) : o_1	1	1	1
31 : R_{11}	6.2+3	6.0+3	6.4+3
32 : V_{cc}	5	4.25	5.75
33 : V_L	3	2.55	3.45
34 :			

MATRIX ELMTS

```
A  1,  1 01
A  1,  2
A  1,  3
A  1,  4
A  1,  5
A  1,  6
A  1,  7
   1,  8
A  1,  9
A  1, 10
A  1, 11
A  1, 12
A  1, 13
C  1      (32-13+14&(03-05)-15)/29
A  2,  1
A  2,  2 01
A  2,  3
A  2,  4
A  2,  5
A  2,  6
A  WN  U
A  2,  8
A  2,  9
A  2, 10
```

A 2, 11

A 2, 12

A 2, 13

Q 2 ~~(32+06&(03-05)-07+14&(03-05)-13-16+14&03~~ (typing error)

~~-05~~

(32+06&(03-05)-07+14&(03-05)-13-16+14&03-14&05)/29

A 3, 1

A 3, 2

A 3, 3 01

A 3, 4

A 3, 5

A 3, 6

A 3, 7

A 3, 8

A 3, 9

A 3, 10

A 3, 11

A 3, 12

A 3, 13

C 3 (32-12)/24

A 4, 1

A 4, 2

A 4, 3

A 4, 4 01

A 4, 5

A 4, 6

A 4, 7

A 4, 8

A 4, 9

A 4, 10

A 4, 11

A 4, 12

A 4, 13

```
C  4      (32-10+11&03-11&05-12+22&21&03&25)/(25+26)
A  5,  1
A  5,  2
A  5,  3
A  5,  4
A  5,  5 01
A  5,  6
A  5,  7
A  5,  8
A  5,  9
A  5, 10
A  5, 11
A  5, 12
A  5, 13 -01
C  5      -22&21&03
A  6,  1
A  6,  2 -01
A  6,  3
A  6,  4
A  6,  5
A  6,  6 01
A  6,  7
A  6,  8
A  6,  9
A  6, 10
A  6, 11
A  6, 12
A  6, 13 18+18&19&(03-05)
C  6      22&21&03
A  7,  1 01
A  7,  2
A  7,  3
A  7,  4
```

```
A  7,  5 -01
A  7,  6 01
A  7,  7 -01
A  7,  8
A  7,  9
A  7, 10
A  7, 11
A  7, 12
A  7, 13
C  7     (33-14&(03-05)+13)/28
A  8,  1
A  8,  2
A  8,  3
A  8,  4
A  8,  5
A  8,  6
A  8,  7
A  8,  8 01
A  8,  9
A  8, 10
A  8, 11
A  8, 12
A  8, 13
C  8     13-14&(03-05)+16-14&(03-05)
A  9,  1
A  9,  2
A  9,  3
A  9,  4 -25
A  9,  5
A  9,  6
A  9,  7
A  9,  8
A  9,  9 01
```

```
A  9, 10
A  9, 11
A  9, 12
A  9, 13
C  9      -25&21&03&22-11&(03-05)+10+12
A 10,  1
A 10,  2
A 10,  3
A 10,  4
A 10,  5
A 10,  6
A 10,  7
A 10,  8
A 10,  9
A 10, 10 01
A 10, 11
A 10, 12
A 10, 13
C 10      13-14&(03-05)+15-04+02&(03-05)-17+14&(03-05)
A 11,  1
A 11,  2
A 11,  3 01
A 11,  4 01
A 11,  5
A 11,  6
A 11,  7 -08-08&09&(03-05)
A 11,  8
A 11,  9
A 11, 10
A  1, 11 01
A 11, 12
A 11, 13
C 11      21&03&22
```

A 12, 1 -32

A 12, 2 -32

A 12, 3 -32

A 12, 4 -32

A 12, 5

A 12, 6

A 12, 7

A 12, 8

A 12, 9

A 12, 10 -33/27

A 12, 11

A 12, 12 01

A 12, 13

C 12 ~~32&21&03&20+32&21&03&22+(32&32-32&12-04&32+32&02&03-32&02&06~~
~~32&21&03&20+32&21&03&22+(32&32-32&12-04&32+32&02&03-32&02&06~~
~~32~~
~~32&21&03&20+32&21&03&22+(32&32-32&12-14~~ } typing error

32&21&03&20+32&21&03&22+(32&32-32&12-04&32+32&02&03-32&02&05)/31+(33&33)
/27+(13&33-14&33&(03-05)+33&33)/27

A 13, 1

A 13, 2

A 13, 3

A 13, 4

A 13, 5

A 13, 6

A 13, 7

A 13, 8

A 13, 9

A 13, 10

A 13, 11

A 13, 12

A 13, 13 27

C 13 (33+13-14&03+14&05+15-04+02&03-02&05-17+14&03-14&05-21&03&23&27-21&03
&20&27)/(18+18&19&03-18&19&05+01)

I_1	I_2	I_3	I_4	I_5	
.34292 - 3	+.25042 - 3	+.12308 - 3	+.25337 - 3	+.15956 - 5	} Nominal Solution
+.22266 I_{b2} 3	+.52653 I_{b1} 3	+.14850 V_2 1	+.19596 + 1	+.45000 - 1	
+.28583 - 1	+.86840 - 2	+.18690 - 5	V_4	V_1	
I_0	P	I_{b3}			

Meaning less

-.3395 - 3	$\frac{\Delta u^*}{\Delta 01}$
-.2479 - 3	
-.1219 - 3	
-.2509 - 3	
+.1539 - 6	
-.2187 - 3	
-.5218 - 3	
-.1470 + 1	
-.3108 + 1	
-.4455 - 1	
-.5669 - 1	
-.1335 - 1	
+.1167 - 6	

* unknown
ie. I_1, I_2, I_3 etc.

+.0000 + 0	$\frac{\Delta u}{\Delta T.C._1}$
+.0000 + 0	
+.0000 + 0	
+.0000 + 0	
+.0000 + 0	
+.0000 + 0	
+.0000 + 0	
+.0000 + 0	
.0000 + 0	
.0000 + 0	
+.0000 + 0	
+.0000 + 0	
+.0000 + 0	

+.1667 - 6	$\frac{\Delta u}{\Delta T^0}$
+.5417 - 6	
+.0000 + 0	
+.1399 - 6	
-.2126 - 7	
+.5191 - 6	
+.7271 - 6	
-.4000 - 2	
-.1679 - 2	
+.3250 - 2	
+.2427 - 3	
+.6967 - 5	
-.1345 - 7	

+.0000 + 0	$\frac{\Delta u}{\Delta(V_{01n} \& V_{02n})}$
+.0000 + 0	
+.0000 + 0	
+.0000 + 0	
-.6250 - 6	
+.9375 - 5	
.1000 - 4	
+.0000 + 0	
+.0000 + 0	
-.1.000 + 1	
+.5500 - 3	
-.8365 - 3	
-.6250 - 6	

-.1667 - 6
-.5417 - 6
+.0000 + 0
-.1377 - 6
+.1255 - 7
-.4966 - 6
-.6958 - 6
.4000 - 2
+.1653 - 2
-.3250 - 2
-.2408 - 3
-.6889 - 5
+.1255 - 7

$\frac{\Delta u}{\Delta 35}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta u}{\Delta T.C.2}$

+.0000 + 0
-.8333 - 4
+.0000 + 0
+.0000 + 0
.0000 + 0
.8333 - 4
-.8333 - 4
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.4583 - 2
-.4167 - 3
+.0000 + 0

$\frac{\Delta u}{\Delta V_{DZN}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.5265 - 3
+.0000 + 0
+.0000 + 0

$\frac{\Delta u}{\Delta B_{IN}}$

+.0000 + 0
+.0000 + 0
.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta u}{\Delta KT_1}$

+.0000 + 0
+.0000 + 0
+.0000 + 0

+.0000 + 0
+.0000 + 0
+.0000 + 0
.5988 - 4
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.7186 + 0
+.0000 + 0
+.5988 - 4
-.2994 - 3
+.0000 + 0

$\frac{\Delta U}{\Delta V_{05n}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta U}{\Delta T.C.5}$

+.0000 + 0
+.0000 + 0
-.2564 - 4
-.5988 - 4
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.7186 + 0
+.0000 + 0
+.8552 - 4
-.1234 - 2
+.0000 + 0

$\frac{\Delta U}{\Delta V_{ce1}}$

-.8333 - 4
-.8333 - 4
+.0000 + 0
+.0000 + 0
+.6250 - 6
-.9271 - 4
-.1867 - 3
+.1000 + 1
+.0000 + 0
+.1000 + 1
-.1027 - 1
-.7733 - 3
+.6250 - 6

$\frac{\Delta U}{\Delta V_{be1n}}$

+.0000 + 0
-.8882 -10
+.0000 + 0
+.0000 + 0
+.6939 -12
+.0000 + 0

$\frac{\Delta U}{\Delta T.C._{bc1,2,3}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.3469 -12

$\frac{\Delta u}{\Delta T.C._{be_{1,2,3}}}$

-.8333 - 4
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.6250 - 6
-.9375 - 5
-.9333 - 4
+.0000 + 0
+.0000 + 0
+.1000 + 1
-.5133 - 2
-.3867 - 3
+.6250 - 6

$\frac{\Delta u}{\Delta V_{ce_{2n}}}$

+.0000 + 0
-.8333 - 4
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.8333 - 4
-.8333 - 4
+.1000 + 1
+.0000 + 0
+.0000 + 0
-.4583 - 2
-.4167 - 3
+.0000 + 0

$\frac{\Delta u}{\Delta V_{be_{2n}}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.6250 - 6
+.9375 - 5
+.1000 - 4
+.0000 + 0
+.0000 + 0
-.1000 + 1
+.5500 - 3
-.3000 - 4
-.6250 - 6

$\frac{\Delta u}{\Delta V_{be_{3n}}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.1157 - 6
-.1157 - 6
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.7579 -12
+.0000 + 0
-.1157 - 6

$\frac{\Delta u}{\Delta B_{3n}}$

+.0000 + 0
+.0000 + 0

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta u}{\Delta KT_3}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.3106 + 1
+.4659 + 2
+.4970 + 2
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.2734 + 4
+.2485 + 3
-.3106 + 1

$\frac{\Delta u}{\Delta I_{con}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.5418 - 7
-.2166 - 6
+.5534 - 6
+.7700 - 6
+.0000 + 0
-.6501 - 3
+.0000 + 0
+.4249 - 4
+.1933 - 5
-.2406 - 7

$\frac{\Delta u}{\Delta C}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.1399 + 2
-.4970 + 2
+.4970 + 2
+.9940 + 2
+.0000 + 0
-.1678 + 6
+.0000 + 0
+.5503 + 4
+.3184 + 3
+.0000 + 0

$\frac{\Delta u}{\Delta I_{DLn}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.3106 + 1
+.4659 + 2
+.4970 + 2
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.2734 + 4
+.0000 + 0

$\frac{\Delta u}{\Delta I_{con}}$

-.3106 + 1

+.0000 + 0
+.0000 + 0
-.3125 - 8
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.3125 - 8
-.1562 - 7
+.0000 + 0

$\frac{L}{LR_2}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
-.1511 - 7
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.1814 - 3
+.0000 + 0
+.1511 - 7
-.7556 - 7
+.0000 + 0

$\frac{L_1}{LR_5}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
-.1506 - 7
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.7080 - 4
+.0000 + 0
+.1506 - 7
-.7532 - 7
+.0000 + 0

$\frac{\Delta u}{\Delta R_9}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.1884 -10
+.2826 - 9
+.3015 - 9
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.1658 - 7
-.2017 - 8
-.1884 -10

$\frac{\Delta u}{\Delta R_8}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.3708 - 9
+.0000 + 0

$\frac{\Delta u}{\Delta R_7}$

+.0000 + 0
+.0000 + 0
+.2039 - 7
+.0000 + 0
+.0000 + 0

$\frac{\Delta u}{\Delta R_1}$

-.2829 - 7
-.2066 - 7
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.2066 - 7
-.4895 - 7
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.2693 - 5
-.2448 - 6
+.0000 + 0

Meaning less

$\frac{\Delta u}{\Delta o_1}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta u}{\Delta R_{11}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.5795 - 6
+.0000 + 0

$\frac{\Delta u}{\Delta V_{cc}}$

+.8333 - 4
+.8333 - 4
+.2564 - 4
+.5988 - 4
+.0000 + 0
+.8333 - 4
+.1667 - 3
+.0000 + 0
+.2814 + 0
+.0000 + 0
+.9081 - 2
+.3784 - 2
+.0000 + 0

$\frac{\Delta u}{\Delta V_b}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0

+.6250 - 6
-.9375 - 5
-.2000 - 4
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.1100 - 2
+.1285 - 3
+.6250 - 6

$\frac{\Delta u}{\Delta V_b}$

$I_{1\ max.}$

+.43479 - 3 +.35180 - 3 +.13557 - 3 +.28785 - 3 -.69297 - 6
+.33476 - 3 +.73084 - 3 +.12480 + 1 +.21691 + 1 +.89750 - 1
+.13069 + 0 +.12007 - 1 +.32943 - 6

} Solutions when I_1 is maximum

$I_{1\ min.}$

+.26024 - 3 +.16774 - 3 +.10979 - 3 +.21876 - 3 +.51310 - 5
+.14574 - 3 +.36608 - 3 +.16060 + 1 +.17124 + 1 +.81500 - 1
+.84904 - 2 +.60446 - 2 +.51310 - 5

} Solutions when I_1 is minimum

$I_{2\ max.}$

+.42259 - 3 +.35747 - 3 +.13557 - 3 +.28785 - 3 -.67210 - 6
+.33929 - 3 +.72294 - 3 +.12520 + 1 +.21691 + 1 +.20975 + 0
+.12927 + 0 +.11974 - 1 +.35030 - 6

$I_{2\ min.}$

+.26879 - 3 +.15661 - 3 +.10979 - 3 +.21876 - 3 +.48970 - 5
+.13562 - 3 +.36459 - 3 +.16740 + 1 +.17124 + 1 -.38500 - 1
+.84545 - 2 +.60308 - 2 +.48970 - 5

$I_{3\ max.}$

+.39605 - 3 +.32782 - 3 +.14947 - 3 +.29942 - 3 -.66688 - 6
+.30935 - 3 +.66637 - 3 +.12780 + 1 +.20252 + 1 +.23975 + 0
+.11910 + 0 +.11978 - 1 +.35552 - 6

$I_{3\ min.}$

+.29012 - 3 +.18127 - 3 +.98259 - 4 +.20638 - 3 +.48385 - 5
+.16053 - 3 +.41135 - 3 +.15760 + 1 +.18560 + 1 -.68500 - 1
+.96047 - 2 +.59811 - 2 +.48385 - 5

$I_{4\ max.}$

+.39605 - 3 +.32782 - 3 +.14055 - 3 +.32487 - 3 -.66688 - 6
+.30935 - 3 +.66637 - 3 +.12780 + 1 +.19815 + 1 +.23975 + 0
+.11908 + 0 +.12073 - 1 +.35552 - 6

$I_{4\ min.}$

+.29012 - 3 +.18127 - 3 +.10450 - 3 +.18872 - 3 +.48385 - 5
+.16053 - 3 +.41135 - 3 +.15760 + 1 +.19023 + 1 -.68500 - 1
+.96161 - 2 +.59325 - 2 +.48385 - 5

$I_{5\ max}$

+.38008 - 3 +.27702 - 3 +.13557 - 3 +.27507 - 3 +.80316 - 5
+.24877 - 3 +.57919 - 3 +.16740 + 1 +.23281 + 1 +.69250 - 1
+.47199 - 1 +.10963 - 1 +.80316 - 5

$I_{5\ min.}$

+.30404 - 3 +.22766 - 3 +.10979 - 3 +.23131 - 3 (-.82570 - 6)
+.21942 - 3 +.49149 - 3 +.12520 + 1 +.15668 + 1 +.70500 - 1
+.17958 - 1 +.66976 - 2 +.19670 - 6

$I_{b_2\ max}$

+.43479 - 3 +.36125 - 3 +.13557 - 3 +.28785 - 3 -.18460 - 7
(+.35363 - 3) +.75777 - 3 +.12080 + 1 +.21691 + 1 +.89750 - 1
+.13552 + 0 +.11950 - 1 +.10039 - 5

$I_{b_2\ min.}$

+.26024 - 3 +.15887 - 3 +.10979 - 3 +.21876 - 3 +.12873 - 5
(+.12375 - 3) +.33865 - 3 +.16460 + 1 +.17124 + 1 +.81500 - 1
+.78296 - 2 +.61266 - 2 +.12873 - 5

+.43479 - 3 +.36125 - 3 +.13557 - 3 +.28785 - 3 -.84946 - 6
+.35280 - 3 (+.75777 - 3) +.12080 + 1 +.21691 + 1 +.89750 - 1
+.13552 + 0 +.11950 - 1 +.17292 - 6
$I_{b_1 max.}$

+.26024 - 3 +.15887 - 3 +.10979 - 3 +.21876 - 3 +.68859 - 5
+.12935 - 3 (+.33865 - 3) +.16460 + 1 +.17124 + 1 +.81500 - 1
+.78296 - 2 +.61266 - 2 +.68859 - 5
$I_{b_1 min.}$

+.38008 - 3 +.27702 - 3 +.13557 - 3 +.27507 - 3 +.14031 - 5
+.24561 - 3 +.58267 - 3 (+.16740 + 1) +.23281 + 1 -.70750 - 1
+.47485 - 1 +.10888 - 1 +.14031 - 5
$V_{2\ max.}$

+.30404 - 3 +.22766 - 3 +.10979 - 3 +.23102 - 3 +.33840 - 5
+.20259 - 3 +.47045 - 3 (+.12520 + 1) +.15701 + 1 +.21050 + 0
+.17174 - 1 +.67335 - 2 +.33853 - 5
$V_{2\ min.}$

+.38008 - 3 +.27702 - 3 +.13557 - 3 +.28912 - 3 +.14031 - 5
+.24561 - 3 +.58267 - 3 +.16740 + 1 (+.23962 + 1) -.70750 - 1
+.47471 - 1 +.10969 - 1 +.14031 - 5
$V_{T max}$

+.30404 - 3 +.22766 - 3 +.10979 - 3 +.21987 - 3 +.23629 - 5
+.20361 - 3 +.47250 - 3 +.12520 + 1 (+.15148 + 1) +.21050 + 0
+.17262 - 1 +.66904 - 2 +.33853 - 5
$V_{T min.}$

+.39605 - 3 +.32782 - 3 +.13557 - 3 +.28785 - 3 -.64253 - 6
+.30802 - 3 +.66501 - 3 +.12780 + 1 +.21691 + 1 (+.37975 + 0)
+.11888 + 0 +.11711 - 1 +.37987 - 6
$V_{1 max.}$

+.29012 - 3 +.18127 - 3 +.10979 - 3 +.21876 - 3 +.45655 - 5
+.16170 - 3 +.41279 - 3 +.15760 + 1 +.17124 + 1 (-.20850 + 0)
+.96155 - 2 +.61782 - 2 +.45655 - 5
$V_{1 min.}$

+.43479 - 3 +.36125 - 3 +.13557 - 3 +.28785 - 3 -.84948 - 6
+.35280 - 3 +.75777 - 3 +.12080 + 1 +.21691 + 1 +.89750 - 1
+.13552 + 0 +.11950 - 1 +.17292 - 6

$I_{o\,max.}$

+.26024 - 3 +.15887 - 3 +.10979 - 3 +.21876 - 3 +.68859 - 5
+.12935 - 3 +.33865 - 3 +.16460 + 1 +.17124 + 1 +.81500 - 1
+.78296 - 2 +.61266 - 2 +.68859 - 5

$I_{o\,min.}$

+.43479 - 3 +.36125 - 3 +.14947 - 3 +.32487 - 3 -.62904 - 6
+.34071 - 3 +.73672 - 3 +.12080 + 1 +.19815 + 1 +.22975 + 0
+.13170 + 0 +.12942 - 1 +.39336 - 6

$P_{max.}$

+.26024 - 3 +.15887 - 3 +.98259 - 4 +.18872 - 3 +.45750 - 5
+.13926 - 3 +.36015 - 3 +.16460 + 1 +.19023 + 1 -.58500 - 1
+.83690 - 2 +.54779 - 2 +.45750 - 5

$P_{min.}$

+.38008 - 3 +.27702 - 3 +.13557 - 3 +.27507 - 3 +.80316 - 5
+.24877 - 3 +.57919 - 3 +.16740 + 1 +.23281 + 1 +.69250 - 1
+.47199 - 1 +.10963 - 1 +.80316 - 5

$I_{b_3\,max.}$

+.30404 - 3 +.22766 - 3 +.10979 - 3 +.23102 - 3 +.19542 - 6
+.21839 - 3 +.48944 - 3 +.12520 + 1 +.15701 + 1 +.70500 - 1
+.17881 - 1 +.66920 - 2 +.19670 - 6

$I_{b_3\,min.}$

+.29012 - 3 +.18127 - 3 +.10979 - 3 +.21876 - 3 +.48385 - 5
+.16053 - 3 +.41135 - 3 +.15760 + 1 +.17124 + 1 -.68500 - 1
+.95808 - 2 +.62243 - 2 +.48385 - 5

TRANSISTOR AND DIODE BIAS POINTS FOR FINAL COMPUTER RUNS

500 K.C. ±15% POWER SUPPLY

All transistors 2N914
All diodes FD 643

(Current Values from Computer Run #4)			$T.C._2$*	V_{D2}*	Tolerance	V_{D2n}
I_{D2}	=	0.22ma Nom.	2.5mv/°C	0.505v		
	=	0.35ma Max.	2.3mv/°C	0.555v	+25mv =	0.580v
	=	0.12ma Min.	2.8mv/°C	0.445v	-25mv =	0.420v

(Current Values from Computer Run #4)			$T.C._5$*	V_{D5n}*	Tolerance	V_{D5n}
I_4	=	.25ma Nom.	2.5mv/°C	0.510v		
	=	.32ma Max.	2.3mv/°C	0.552v	+25mv =	0.577v
	=	.19ma Min.	2.8mv/°C	0.465v	-25mv =	0.440v

(Currents Calculated) (Not Computer)			$T.C._7$*	V_{D7n}*	Tolerance	V_{D7n}
I_{D7}	=	0.645ma Mon.	2.3mv/°C	0.560v		
	=	0.83ma Max.	2.2mv/°C	0.595v	+25mv =	0.620
	=	0.51ma Min.	2.5mv/°C	0.508	-25mv =	.483v

I_{c1}	I_{b1}	V_{ce_1} @25°C	V_{ce1} @+80°C	V_{ce1} @-10°C	V_{ce1} Nom. 0.2 Min. 0.1 Max. 0.3
6ma	.53ma	nom. 0.18			
		TR#7		@.37ma	
10ma	.34ma	max. 0.26v	0.21v	0.30v	Note: Currents from Computer Run #4
		TR#10			V_{ce} from plots V_{ce} vs I_b, Appendix D
1ma	.75ma	min. 0.11v	0.11v	0.10v	

*From Fairchild Curves for FD363 Diode

TRANSISTOR AND DIODE BIAS POINTS FOR FINAL COMPUTER RUNS

-continued-

I_{c1}	I_{b1}	V_{be1} @25°C	V_{be1} @80°C	V_{be1} @-10°C	T.C.$_{be1}$ (+25° to +80°)	T.C.$_{be1}$ (+25° to -10°)
	(Nom #2)					
6ma	0.53ma	0.76v				
	(Min #6)					
1ma	0.34ma	0.68v	0.585v	0.75v	1.8mv/°C	2.0mv/°C
	(Max #2)					
10ma	0.75ma	0.78v	0.68v	0.815v	1.8mv/°C	1.0mv/°C

Note: I_{b1} from Computer Run #4

T.C.$_{be1}$ = Nom 1.5mv/°C
Min 1.0mv/°C
Max 2.0mv/°C

V_{be1n} = Nom .75v Added
Min .65v 30mv to
Max .81v 25°C data

Extrapolated from V_{ce} Versus I_b Plots, Appendix D

I_{c2}	V_{ce2} @25°C	V_{ce2} @80°C	V_{ce2} @-10°C	I_{b2}
0.43	0.16v	0.18v	0.14v	0.12v
0.26	0.10v	0.12v	0.09v	0.35v

Nom V_{ce2} = 0.14v
Min V_{ce2} = 0.08v
Max V_{ce2} = 0.20v

Note: I_{c2} from Computer Run #4, $I_1 \approx I_{c2}$

I_{c2}	I_{b2}	V_{be2} @25°C	V_{be2} @80°C	V_{be2} @-10°C	T.C.$_{be2}$ (25° to +80°)	T.C.$_{be2}$ (25° to -10°)
	(Max TR#2)				(Note: I_{c2} from)	
0.43ma	0.35ma		0.57v	0.745v	(Computer Run #4)	
	(Min TR#6)				(I_1 I_{c2})	
0.26ma	0.12ma	0.66v	0.54v	0.71v	2.2mv/°C	1.2mv/°C
	(Nom TR#6)					
0.34ma	0.22ma	0.69v	0.55v	0.72v	2.5mv/°C	0.9mv/°C

T.C.$_{be2}$ = Min = 1.0mv/°C
Max = 2.5mv/°C
Nom = 2.0mv/°C

V_{be2_n} = Min 0.65v
Max 0.75v
Nom 0.67v

Determination of $V_{be_{3n}}$

Maximum $V_{be_{3n}}$

$$\bar{I}_{c3} = \frac{\bar{V}_{R8}}{R8} = \frac{3.75v.}{96K\ ohm} = 39\mu a.$$

where $\bar{V}_{R_8}$ = Max. Fwd. OFF bias, base Q_4 + $\bar{V}_b$

= +0.3v. + 3.45v. = 3.75v.

$\bar{V}_{be_3}$ @ 30 μ a. and 25°C = 0.596v. (Fr. Table I)

Also from Table I, $\frac{\Delta V_{be_3}}{\Delta I_{c_3}} = \frac{17\ mv.}{20\mu a.} = 0.85\ mv./\mu a.$

$\approx 1.0\ mv./\mu a.$

Then for I_{c_3} = 39 μ a.,

$\bar{V}_{be_3}$ = 0.596v. + 1.0 mv./μ a. x 9μ a.

= 0.605 mv.

Minimum V_{be_3}

$$I_{c3} = \frac{V_{R8}}{\bar{R}_8} = \frac{2.35v.}{104K\ ohm} = 22.6\mu a.$$

where V_{R_8} = Max. Rev. OFF bias, base Q_4 + V_b

= -0,2v. + 2.55v. = 2.35v.

V_{be_3} @ 20 μa. and 25°C = 0.570v. (FR. Table I)

V_{be_3} @ 22.6μa. = 0.570v. + 1 mv/μa. x 2.6μa

= 0.573v.

Nominal V_{be_3}

$$= \frac{0.605 - 0.573}{2} + 0.573 = 0.589v.$$

Determination of $T.C._{be_3}$

From Table I @ I_c = 30 μ a.

TR	V_{be_3} @ 25°C.	V_{be_3} @ -10°C.	$T.C._{be_3}$ (Calculated)
# 2	0.592v.	0.653v.	1.74mv./°C
# 6	0.581v.	0.646v.	1.86mv./°C
# 7	0.596v.	0.653v.	1.63mv./°C
#10	0.584v.	0.642v.	1.66mv./°C
	@ 25°C	@ +80°C	
# 2	0.592v.	0.460v.	2.4mv./°C
# 6	0.581v.	0.450v.	2.39mv./°C
# 7	0.596v.	0.460v.	2.47mv./°C
#10	0.584v.	0.448v.	2.47mv./°C

Therefore, $T.C._{be_3}$ is;

Nominal = 2.0 mv./°C.

Minimum = 1.6 mv./°C.

Maximum = 2.5 mv./°C.

Determination of $h_{FE_{3n}}$ (Q_3)

From Appendix D, Table I

@ 25°C. and I_c = 30 μa.

TR#	2	6	7	10
h_{FE}	18.7	20	9.4	50

@ 80°C. and I_c = 30 μa.

TR#	2	6	7	10
h_{FE}	50	60	25	100

@-10°C. and I_c = 30 μa.

TR#	2	6	7	10
h_{FE}	12.5	14.3	6.0	27.3

Therefore, $h_{FE_{3n}}$ or β_{3n} is,

20 = Nominal

6.0 = Minimum

60 = Maximum

The change in h_{FE} from +25 C to -10 C is,

for transistor #2, $(1 - \frac{12}{19}) \times \frac{100}{35} = 1.05\%/°C.$

#6, $(1 - \frac{14.3}{20}) \times \frac{100}{35} = 0.86\%/°C.$

#7, $(1 - \frac{6}{9.4}) \times \frac{100}{35} = 1.03\%/^{o}C.$

#10, $(1 - \frac{27.3}{50}) \times \frac{100}{35} = 1.3\%/^{o}C.$

K_{T_3} is then, 0.01 Nominal

0.007 Minimum

0.02 Maximum

Note: Absolute maximum h_{FE} @ 80°C is then 126

Absolute minimum h_{FE} @ -10°C is then 2

Determination of V_{D1_n}

I_{F1} is maximum when h_{FE_3} is minimum, $I_{DL_4} = 0$ and V_{be_3} is maximum.

Therefore, $\bar{I}_{F1} = \frac{\bar{I}_{c3}}{h_{FE_3}} + \bar{I}_{R8}$

$= \frac{30}{2}\mu a + 7\mu a = 22\mu a.$

$V_{D1_n} = 0.435$ (Fr. Fairchild FD643 curves @ 25°C.)

I_{F1} is minimum when h_{FE_3} is maximum, I_{DL_4} is maximum and V_{be_3} is minimum.

Therefore, $I_{F1} = I_{R_8} - I_{DL4}$ assuming h_{FE_3} 100

$= 4.7\mu$ a. $- 1\mu$ a. $I_{DL_4} = 0.4\mu$ a. @ 80°C Fairchild curves

$= 3.7\mu$ a. $\simeq 4\mu$ a

V_{D1_n} = 0.333v. - 25mv. Tol. (Diode #3 fr. meas. Table IV)

= 0.308v.

Determination of T.C.,

From Table IV worst unit, ie. #3

$$\overline{T.C.} = \frac{0.159v.}{55°C} = 3.2 \text{ mv./°C}$$

From Fairchild curves $T.C._1$ = 2.8 mv./°C

Determination of I_{R14}

Nominal $I_{R_{14}} = \frac{V_{be3n}}{R_{14}} = \frac{0.59v.}{100K \text{ ohm}} = 5.9\mu$ a.

Minimum $I_{R14} = \frac{V_{be3}}{\overline{R_{14}}} = \frac{0.44v.}{104K \text{ ohm}} = 4.2\mu$ a.

Maximum $\overline{I_{R_{14}}} = \frac{\overline{V_{be3}}}{R_{14}} = \frac{0.69}{96K \text{ ohm}} = 7.2\mu$ a.

Note: $\overline{V_{be3}}$ @ -10°C

V_{be3} @ 80°C

Computer Run #5

JPL Flip-Flop - 500K.C.
R_{13} and R_{14} added
$\pm$15% Power Supplies
$\pm$ 4% Resistors
Transistor and Diode parameters as measured and bias points from first Computer Run

Matrix Size: 13

	Parameter	Nom.	Min.	Max.
1 :	01	1	1	-1
2 :	$T.C._1$	3-3	2.8-3	-3.2-3
3 :	T^o	35	1-9	90
4:	V_{Din}	.37	.308	.435
5 :	35	35	35	-35
6 :	T.C. 2	2.55-3	2.35-3	-2.76-3
7 :	$V_{D_{2n}}$	.505	.445	.605
8 :	$h_{FE_{in}}$	55	29.2	120
9 :	KT_1	.007	.005	-.009
10 :	V_{D5_n}	.510	.44	.577
11 :	T.C. 5	2.5-3	2.3-3	-2.8-3
12 :	V_{ce_1}	.2	.1	.3
13 :	$V_{be_{in}}$	.75	.65	.81
14 :	T.C. be 1,2,3	2-3	1-3	2.5-3
15 :	$V_{ce_{2n}}$	.14	.08	.2
16 :	$V_{be_{2n}}$	.67	.65	.7
17 :	$V_{be_{3n}}$	.589	.573	.605
18 :	h_{FE3n}	20	6	60
19 :	KT_3	.01	0.007	-.02
20 :	I_{con}	4-9	.01-9	25-9
21 :	C	1.42	1.42	1.42
22 :	I_{DLn}	5.5-9	.01-9	8-9
23 :	I_{eon}	7-9	.01-9	100-9
24 :	R_3	39 +3	37.4+3	40.5+3

25 :	R_5	4.7+3	4.5+3	4.9+3
26 :	R_9	12+3	11.5+3	12.5+3
27 :	R_8	100+3	96+3	104+3
28 :	R_7	100+3	96+3	104+3
29 :	R_1	12+3	11.6+3	12.5+3
30 :	V_{D7n}	.56	.508	.595
31 :	R_{11}	6.2+3	5.95+3	6.45+3
32 :	V_{cc}	5	4.25	5.75
33 :	V_b	3	2.55	3.45
34 :	T.C . 7	2.3-3	2.2-3	2.5-3
35 :	R_{13}	100+3	96+3	104+3
36 :	R_{14}	100+3	96+3	104+3
37 :	$I_{R_{14}}$	5.9-6	4.2-6	7.2-6
38 :				

MATRIX ELMTS

548/ 3).5s

- 1, 1 01

- 1, 2

0 1, 3

```
- 1,  4
- 1,  5
- 1,  6
- 1,  7
- 1,  8
- 1,  9
- 1, 10
- 1, 11
- 1, 12
- 1, 13
C 1      (32-13+14&(03-05)-15)/29
- 2,  1
- 2,  2 01
- 2,  3
- 2,  4
- 2,  5
- 2,  6
- 2,  7
- 2,  8
- 2,  9
- 2, 10
- 2, 11
- 2, 12
- 2, 13
: 2      (32+06&(03-05)-07+14&(03-05)-13-16+14&03-14&05)/29
- 3,  1
- 3,  2
- 3,  3 01
- 3,  4
- 3,  5
- 3,  6
- 3,  7
- 3,  8
```

```
- 3, 9
- 3, 10
- 3, 11
- 3, 12
- 3, 13
: 3     (32-12)/24
- 4, 1
- 4, 2
- 4, 3
- 4, 4 01
- 4, 5
- 4, 6
- 4, 7
- 4, 8
- 4, 9
- 4, 10
- 4, 11
- 4, 12
- 4, 13
: 4     (32-10+11&03-11&05-12+22&21&03&25)/(25+26)
- 5, 1
- 5, 2
- 5, 3
- 5, 4
- 5, 5 01
- 5, 6
- 5, 7
- 5, 8
- 5, 9
- 5, 10
- 5, 11
- 5, 12
- 5, 13 -01
```

```
: 5      -22&21&03+(17-14&03+14&05)/36                    6     16-7-64
- 6,  1
- 6,  2 -01
- 6,  3
- 6,  4
- 6,  5
- 6,  6 01
- 6,  7
- 6,  8
- 6,  9
- 6, 10
- 6, 11
- 6, 12
- 6, 13 18+18&19&(03-05)-(16-14&03+14&05)/35
: 6      22&21&03
- 7,  1 01
- 7,  2
- 7,  3
- 7,  4
- 7,  5 -01
- 7,  6 01
- 7,  7 -01
- 7,  8
- 7,  9
- 7, 10
- 7, 11
- 7, 12
- 7, 13
: 7      (33-14&(03-05)+13)/28-(16-14&03+14&05)/35
- 8,  1
- 8,  2
- 8,  3
- 8,  4
```

```
- 8,  5
- 8,  6
- 8,  7
- 8,  8 01
- 8,  9
- 8, 10
- 8, 11
- 8, 12
- 8, 13
: 8     13-14&(03-05)+16-14&(03-05)
- 9,  1
- 9,  2
- 9,  3
- 9,  4 -25
- 9,  5
- 9,  6
- 9,  7
- 9,  8
- 9,  9 01
- 9, 10
- 9, 11
- 9, 12
- 9, 13
: 9     -25&21&03&22-11&(03-05)+10+12
- 10,  1
- 10,  2
- 10,  3
- 10,  4
- 10,  5
.  0,  6
- 10,  7
- 10,  8
- 10,  9
```

```
- 10, 10 01
- 10, 11
- 10, 12
- 10, 13
: 10      13-13
13-14&(03-05)+15-04+02&(03-05)-17+14&(03-05)
- 11,  1
- 11,  2
- 11,  3 01
- 11,  4 01
- 11,  5
- 11,  6
- 11,  7 -08-08&09&(03-05)
- 11,  8
- 11,  9
- 11, 10
- 11, 11 01
- .1, 12
- 11, 13
: 11      21&03&22
- 12,  1 -32
- 12,  2 -32
- 12,  3 -32
- 12,  4 -32
- 12,  5
- 12,  6
- 12,  7
- 12,  8
- 12,  9
- 12, 10 -33/27
- 12, 11
- 12, 12 01
- 12, 13
: 12      32&21&03&20+32&21&03&22+(32&32-32&12-30&32+32&34&03-32&34&05)/31+(33
```

```
&33)/27+(13&33-14&33&(03-05)+33&33)/27
- 13,  1
- 13,  2
- 13,  3
- 13,  4
- 13,  5
- 13,  6
- 13,  7
- 13,  8
- 13,  9
- 13, 10
- 13, 11
- 13, 12
- 13, 13 27
: 13      (33+13-14&03+14&05+15-04+02&03-02&05-17+14&03-14&05-21&03&23&27-21&03
          &20&27-27&37)/(18+18&19&03-18&19&05+01)
```

7-10-64

10 July 1964 - P.M.
J.P.L. Flip Flop Run
R_{13} R_{14} added
± 15% power supplies
± 4% Resistors
Transistor & Diode
Parameters Measured

I_1	I_2	I_3	I_4	I_5	
+.34250 - 3	+.25625 - 3	+.12308 - 3	+.25696 - 3	+.67054 - 5	Nominal
+.23475 - 3	+.53974 - 3	+.14200 + 1	+.19164 + 1	-.69000 - 1	Solution
+.29306 - 1	+.85161 - 2	+.10887 - 5	V_T	V_1	
I_{b_2}	P	I_{b_3}			
I_{b_1}					

$\frac{\Delta u}{\Delta T^\circ}$ *
+.1667 - 6
+.5458 - 6
+.0000 + 0
+.1519 - 6
-.3746 - 7
+.5296 - 6
+.7337 - 6
-.4000 - 2
-.1823 - 2
+.3000 - 2
+.2481 - 3
+.6274 - 5
-.9652 - 8

u = unknown
ie. I_1, I_2, I_3, etc.

$\frac{\Delta u}{\Delta V_{D1n}}$
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
- 4762 - 6
9524 - 5
+.1000 - 4
+.0000 + 0
+.0000 + 0
-.1000 + 1
+.5500 - 3
-.3000 - 4
-.4762 - 6

$\frac{\Delta u}{\Delta V_{D2n}}$
+.0000 + 0
-.8333 - 4
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.8333 - 4
-.8333 - 4
+.0000 + 0
+.0000 + 0
-.0000 + 0
-.4583 - 2
-.4167 - 3
+.0000 + 0

$\frac{\Delta u}{\Delta B_{1n}}$
+.0000 + 0
+.0000 + 0
0000 + 0
.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.0000 + 0

+.5397 - 3
+.0000 + 0
+.0000 + 0

+.0000 + 0
+.0000 + 0
+.0000 + 0
5988 - 4
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.7186 + 0
-.0000 + 0
+.5988 - 4
-.2994 - 3
+.0000 + 0

$\frac{\Delta U}{\Delta V_{DSn}}$

+.0000 + 0
+.0000 + 0
-.2564 - 4
-.5988 - 4
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.7186 + 0
-.0000 + 0
+.8552 - 4
-.1234 - 2
+.0000 + 0

$\frac{\Delta U}{\Delta V_{ce_1}}$

8333 - 4
8333 - 4
+.0000 + 0
+.0000 + 0
+.4762 - 6
-.9286 - 4
-.1867 - 3
+.1000 + 1
+.0000 + 0
+.1000 + 1
-.1027 - 1
-.7733 - 3
+.4762 - 6

$\frac{\Delta U}{\Delta V_{be_{1n}}}$

+.0000 + 0
-.1776 - 9
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.1776 - 9
-.1776 - 9
+.0000 + 0
+.0000 + 0
-.0000 + 0
-.1705 - 7
+.0000 + 0
3469 -12

$\frac{\Delta U}{\Delta T, C, be_{1,2,3}}$

-.8333 - 4
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.4762 - 6
-.9524 - 5

$\frac{\Delta U}{\Delta V_{ce_{2n}}}$

-.9333 - 4
+.0000 + 0
+.0000 + 0
+.1000 + 1
-.5133 - 2
-.3867 - 3
+.4762 - 6

+.0000 + 0
-.8333 - 4
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.8333 - 4
-.7333 - 4
+.1000 + 1
+.0000 + 0
-.0000 + 0
-.4033 - 2
-.4167 - 3
+.0000 + 0

$\frac{\Delta u}{\Delta V_{be2n}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.9524 - 5
+.9524 - 5
-.4222 -11
+.0000 + 0
+.0000 + 0
-.1000 + 1
1930 - 9
.3000 - 4
-.4762 - 6

$\frac{\Delta u}{\Delta V_{be3n}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.5136 - 7
-.5136 - 7
-.3553 -12
+.0000 + 0
+.0000 + 0
-.0000 + 0
-.1933 -10
+.0000 + 0
-.5136 - 7

$\frac{\Delta u}{\Delta \beta_{3n}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.2367 + 1
+.4733 + 2
+.4970 + 2
+.0000 + 0
0000 + 0
-.0000 + 0
+.2733 + 4
+.2485 + 3
-.2367 + 1

$\frac{\Delta u}{\Delta I_{con}}$

+.0000 + 0
+.0000 + 0

+.0000 + 0
+.5418 - 7
-.2108 - 6
+.5592 - 6
+.7700 - 6
+.0000 + 0
-.6501 - 3
.0000 + 0
+.4249 - 4
+.1933 - 5
-.1833 - 7

$\frac{\Delta u}{\Delta C}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.1399 + 2
-.4970 + 2
+.4970 + 2
+.9940 + 2
+.0000 + 0
-.1678 + 6
-.0000 + 0
+.5503 + 4
+.3184 + 3
+.0000 + 0

$\frac{\Delta u}{\Delta I_{DLn}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.2367 + 1
+.4733 + 2
.4970 + 2
.0000 + 0
+.0000 + 0
-.0000 + 0
+.2733 + 4
+.0000 + 0
-.2367 + 1

$\frac{\Delta u}{\Delta I_{eon}}$

+.0000 + 0
+.0000 + 0
-.3125 - 8
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.0000 + 0
+.3125 - 8
-.1562 - 7
+.0000 + 0

$\frac{\Delta u}{\Delta R_3}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
-.1533 - 7
.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.1839 - 3
-.0000 + 0
+.1533 - 7
-.7664 - 7

$\frac{\Delta u}{\Delta R_5}$

+.0000 + 0

$\frac{\Delta u}{\Delta R_9}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
-.1528 - 7
+.0000 + 0
.0000 + 0
+.0000 + 0
+.0000 + 0
-.7180 - 4
-.0000 + 0
+.1528 - 7
-.7639 - 7
+.0000 + 0

$\frac{\Delta u}{\Delta R_8}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.1382 -10
+.2764 - 9
+.2902 - 9
+.0000 + 0
+.0000 + 0
-.0000 + 0
+.1596 - 7
-.1984 - 8
-.1382 -10

$\frac{\Delta u}{\Delta R_7}$

+.0000 + 0
+.0000 + 0
.0000 + 0
.0000 + 0
+.0000 + 0
+.0000 + 0
+.3713 - 9
+.0000 + 0
+.0000 + 0
-.0000 + 0
+.2042 - 7
+.0000 + 0
+.0000 + 0

$\frac{\Delta u}{\Delta R_1}$

-.2826 - 7
-.2114 - 7
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.2114 - 7
-.4940 - 7
+.0000 + 0
+.0000 + 0
-.0000 + 0
-.2717 - 5
-.2470 - 6
+.0000 + 0

$\frac{\Delta u}{\Delta V_{DTN}}$

.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0

+.0000 + 0
-.0000 + 0
+.0000 + 0
-.8065 - 3
+.0000 + 0

+.0000 + 0
.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.0000 + 0
+.0000 + 0
-.5460 - 6
+.0000 + 0

$\frac{\Delta U}{\Delta R_{11}}$

+.8333 - 4
+.8333 - 4
+.2564 - 4
+.5988 - 4
+.0000 + 0
+.8333 - 4
+.1667 - 3
+.0000 + 0
+.2814 + 0
-.0000 + 0
+.9081 - 2
+.3751 - 2
.0000 + 0

$\frac{\Delta U}{\Delta V_{cc}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.4762 - 6
-.9524 - 5
-.2000 - 4
+.0000 + 0
+.0000 + 0
-.0000 + 0
-.1100 - 2
+.1274 - 3
+.4762 - 6

$\frac{\Delta U}{\Delta V_b}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.0000 + 0
.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta U}{\Delta T.C.7}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0

$\frac{\Delta u}{\Delta R_{13}}$

+.0000 + 0
-.7105 -16
-.6634 -10
+.0000 + 0
+.0000 + 0
-.0000 + 0
-.3649 - 8
+.0000 + 0
+.0000 + 0

$\frac{\Delta u}{\Delta R_{14}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.5832 -10
+.0000 + 0
+.5832 -10
+.0000 + 0
+.0000 + 0
-.0000 + 0
+.3207 - 8
+.0000 + 0
+.0000 + 0

$\frac{\Delta u}{\Delta I_{R14}}$

+.0000 + 0
+.0000 + 0
+.0000 + 0
+.0000 + 0
-.4762 - 1
+.9524 + 0
+.1000 + 1
+.0000 + 0
+.0000 + 0
-.0000 + 0
+.5500 + 2
+.0000 + 0
-.4762 - 1

I_1 max

+.44461 - 3 +.36295 - 3 +.13457 - 3 +.29612 - 3 +.35643 - 5 } Solutions when I_1 is maximum
+.35546 - 3 +.76382 - 3 +.10750 + 1 +.20485 + 1 -.14500 + 0
+.12652 + 0 +.11836 - 1 +.91530 - 7

I_1 min

+.25640 - 3 +.17486 - 3 +.11096 - 3 +.21784 - 3 +.10948 - 4 } Solutions when I_1 is minimum
+.15686 - 3 +.37409 - 3 +.15300 + 1 +.17448 + 1 +.24000 - 1
+.79183 - 2 +.59353 - 2 +.46148 - 5

I_2 max

+.42716 - 3 +.36683 - 3 +.13457 - 3 +.29612 - 3 +.43699 - 5
+.35820 - 3 +.74781 - 3 +.11900 + 1 +.20485 + 1 -.25000 - 1
+.12386 + 0 +.11765 - 1 +.10381 - 6

I_2 min

+.26180 - 3 +.14966 - 3 +.11096 - 3 +.21784 - 3 +.11240 - 4
+.13266 - 3 +.35551 - 3 +.16850 + 1 +.17448 + 1 -.96000 - 1
+.75087 - 2 +.58493 - 2 +.43597 - 5

I_3 max

+.39020 - 3 +.32402 - 3 +.15107 - 3 +.30762 - 3 +.35930 - 5

+.31387 - 3 +.66624 - 3 +.12350 + 1 +.19048 + 1 +.13500 + 0
+.11027 + 0 +.11653 - 1 +.12017 - 6

$I_{3\,min}$

+.30043 - 3 +.20222 - 3 (+.97531 - 4) +.20534 - 3 +.10353 - 4
+.18654 - 3 +.45006 - 3 +.13700 + 1 +.18885 + 1 -.25600 + 0
+.96191 - 2 +.59739 - 2 +.40196 - 5

$I_{4\,max}$

+.39020 - 3 +.32402 - 3 +.13951 - 3 (+.32594 - 3) +.35930 - 5
+.31387 - 3 +.66624 - 3 +.12350 + 1 +.20016 + 1 +.13500 + 0
+.11027 + 0 +.11692 - 1 +.12017 - 6

$I_{4\,min}$

+.30043 - 3 +.20222 - 3 +.10561 - 3 (+.19670 - 3) +.10353 - 4
+.18654 - 3 +.45006 - 3 +.13700 + 1 +.17913 + 1 -.25600 + 0
+.96197 - 2 +.59715 - 2 +.40196 - 5

$I_{5\,max}$

+.37220 - 3 +.26966 - 3 +.13457 - 3 +.28290 - 3 (+.13674 - 4)
+.24447 - 3 +.56876 - 3 +.16850 + 1 +.22137 + 1 -.80000 - 2
+.51112 - 1 +.10621 - 1 +.64600 - 5

$I_{5\,min}$

+.30819 - 3 +.23752 - 3 +.11096 - 3 +.23219 - 3 (+.39611 - 5)
+.23829 - 3 +.51596 - 3 +.11900 + 1 +.15798 + 1 -.11300 + 0
+.20524 - 1 +.66203 - 2 +.27414 - 8

$I_{b2\,max}$

+.43750 - 3 +.36683 - 3 +.13457 - 3 +.29612 - 3 +.42612 - 5
(+.36790 - 3) +.77710 - 3 +.11900 + 1 +.20485 + 1 -.14500 + 0
+.12872 + 0 +.11712 - 1 -.48544 - 8

$I_{b2\,min}$

+.25220 - 3 +.14966 - 3 +.11096 - 3 +.21784 - 3 +.76799 - 5
(+.11847 - 3) +.32528 - 3 +.16850 + 1 +.17448 + 1 +.24000 - 1
+.68423 - 2 +.59328 - 2 +.79969 - 6

$I_{b1\,max}$

+.43750 - 3 +.36683 - 3 +.13457 - 3 +.29612 - 3 +.39834 - 5
+.36762 - 3 (+.77710 - 3) +.11900 + 1 +.20485 + 1 -.11300 + 0
+.12872 + 0 +.11713 - 1 +.25019 - 7

$I_{b1\,min}$

+.25220 - 3 +.14966 - 3 +.11096 - 3 +.21784 - 3 +.80049 - 5
+.11880 - 3 (+.32528 - 3) +.16850 + 1 +.17448 + 1 -.80000 - 2
+.68423 - 2 +.59317 - 2 +.79135 - 6

$V_{2\,max}$

+.37220 - 3 +.26966 - 3 +.13457 - 3 +.28290 - 3 +.72755 - 5
+.24560 - 3 +.57630 - 3 (+.16850 + 1) +.22137 + 1 -.13500 + 0
+.51795 - 1 +.10595 - 1 +.61687 - 6

+.30819 - 3 +.23752 - 3 +.11096 - 3 +.23191 - 3 +.75796 - 5

+.21720 - 3 +.49125 - 3 +.11900 + 1 +.15831 + 1 +.14000 - 1
+.19524 - 1 +.66160 - 2 +.21850 - 5
$V_{2\,min}$

+.37220 - 3 +.26966 - 3 +.13457 - 3 +.30015 - 3 +.72755 - 5
+.24560 - 3 +.57630 - 3 +.16850 + 1 +.22982 + 1 -.13500 + 0
+.51778 - 1 +.10695 - 1 +.61687 - 6
$V_{T\,max}$

+.30819 - 3 +.23752 - 3 +.11096 - 3 +.21854 - 3 +.65585 - 5
+.21822 - 3 +.49329 - 3 +.11900 + 1 +.15183 + 1 +.14000 - 1
+.19621 - 1 +.65635 - 2 +.21850 - 5
$V_{T\,min}$

+.28405 - 3 +.22373 - 3 +.11096 - 3 +.23191 - 3 +.78628 - 5
+.20078 - 3 +.44874 - 3 +.13500 + 1 +.15831 + 1 +.29400 + 0
+.17805 - 1 +.64665 - 2 +.24682 - 5
$V_{1\,max}$

+.39460 - 3 +.28246 - 3 +.13457 - 3 +.28290 - 3 +.72082 - 5
+.26103 - 3 +.61573 - 3 +.15250 + 1 +.22137 + 1 -.41500 + 0
+.55367 - 1 +.10783 - 1 +.54957 - 6
$V_{1\,min}$

+.43750 - 3 +.36683 - 3 +.13457 - 3 +.29612 - 3 +.39834 - 5
+.36762 - 3 +.77710 - 3 +.11900 + 1 +.20485 + 1 -.11300 + 0
+.12872 + 0 +.11713 - 1 +.25019 - 7
$I_{o\,max}$

+.25220 - 3 +.14966 - 3 +.11096 - 3 +.21784 - 3 +.80049 - 5
+.11880 - 3 +.32528 - 3 +.16850 + 1 +.17448 + 1 -.80000 - 2
+.68423 - 2 +.59317 - 2 +.79135 - 6
$I_{o\,min}$

+.44461 - 3 +.38106 - 3 +.15107 - 3 +.32594 - 3 +.33024 - 5
+.36931 - 3 +.77744 - 3 +.10250 + 1 +.20016 + 1 +.14000 - 1
+.12874 + 0 +.12884 - 1 +.13732 - 6
P_{max}

+.25640 - 3 +.15806 - 3 +.97531 - 4 +.19670 - 3 +.10549 - 4
+.14292 - 3 +.36106 - 3 +.15800 + 1 +.17913 + 1 -.13500 + 0
+.76658 - 2 +.53143 - 2 +.38819 - 5
P_{min}

+.37220 - 3 +.26966 - 3 +.13457 - 3 +.28290 - 3 +.12879 - 4
+.24420 - 3 +.56929 - 3 +.16850 + 1 +.22137 + 1 +.24000 - 1
+.51160 - 1 +.10622 - 1 +.65281 - 5
$I_{b_3\,max}$

+.30819 - 3 +.23752 - 3 +.11096 - 3 +.23191 - 3 +.57274 - 5
+.23757 - 3 +.51347 - 3 +.11900 + 1 +.15831 + 1 -.14500 + 0
+.20423 - 1 +.66140 - 2 -.53191 - 9
$I_{b_3\,min}$

+.30043 - 3 +.20222 - 3 +.11096 - 3 +.21784 - 3 +.10353 - 4

+.18654 - 3 +.45006 - 3 +.13700 - 1 +.17448 + 1 -.25600 + 0 7-10-64
+.95932 - 2 +.62270 - 2 +.40196 - 5

Computer Run #6

J.P.L. Flip-Flop 7/13/64
±5% Power Supplies
±4% Resistors
500KC Resistor Values

Parameter

32

5

4.75

5.25

33

3

2.85

3.15

I_1	I2	I_3	I_4	I_5	
+.34250 - 3	+.25625 - 3	+.12308 - 3	+.25696 - 3	+.67054 - 5	
I_{b2}	I_{b1}	V_2	V_T	V_1	Nominal
+.23475 - 3	+.53974 - 3	+.14200 + 1	+.19164 + 1	-.69000 - 1	Solution
I_o	P	I_{b3}			
+.29306 - 1	+.85161 - 2	+.10887 - 5			

I_{1max}

+.40151 - 3 +.31985 - 3 +.12222 - 3 +.26739 - 3 +.35336 - 5
+.31521 - 3 +.68338 - 3 +.10750 + 1 +.19077 + 1 -.14500 + 0
+.11319 + 0 +.97133 - 2 +.60843 - 7

I_{1min}

+.29640 - 3 +.21486 - 3 +.12433 - 3 +.24909 - 3 +.11586 - 4
+.19438 - 3 +.44784 - 3 +.15300 + 1 +.18854 + 1 +.24000 - 1
+.94995 - 2 +.76424 - 2 +.52526 - 5

I_{2max}

+.38405 - 3 +.32373 - 3 +.12222 - 3 +.26739 - 3 +.43392 - 5
+.31795 - 3 +.66737 - 3 +.11900 + 1 +.19077 + 1 -.25000 - 1
+.11053 + 0 +.96482 - 2 +.73118 - 7

I_{2min}

+.30180 - 3 +.18966 - 3 +.12433 - 3 +.24909 - 3 +.11878 - 4
+.17017 - 3 +.42926 - 3 +.16850 + 1 +.18854 + 1 -.96000 - 1
+.90900 - 2 +.75464 - 2 +.49974 - 5

I_{3max}

+.35020 - 3 +.28402 - 3 +.13770 - 3 +.27888 - 3 +.35623 - 5
+.27672 - 3 +.59201 - 3 +.12350 + 1 +.17640 + 1 +.13500 + 0
+.97977 - 1 +.95736 - 2 +.89484 - 7

I_{3min}

+.34353 - 3 +.24532 - 3 +.10988 - 3 +.23659 - 3 +.10991 - 4
+.22716 - 3 +.53002 - 3 +.13700 + 1 +.20292 + 1 -.25600 + 0
+.11338 - 1 +.77103 - 2 +.46573 - 5

I_{4max}

+.35020 - 3 +.28402 - 3 +.12716 - 3 +.29469 - 3 +.35623 - 5
+.27672 - 3 +.59201 - 3 +.12350 + 1 +.18610 + 1 +.13500 + 0
+.97972 - 1 +.96013 - 2 +.89484 - 7

I_{4min}

+.34353 - 3 +.24532 - 3 +.11898 - 3 +.22543 - 3 +.10991 - 4
+.22716 - 3 +.53002 - 3 +.13700 + 1 +.19321 + 1 -.25600 + 0
+.11340 - 1 +.77005 - 2 +.46573 - 5

I_{5max}

+.33220 - 3 +.22966 - 3 +.12222 - 3 +.25417 - 3 +.13036 - 4
+.20695 - 3 +.49477 - 3 +.16850 + 1 +.20729 + 1 -.80000 - 2
+.44450 - 1 +.86353 - 2 +.58223 - 5

I_{5min}

+.35129 - 3 +.28063 - 3 +.12433 - 3 +.26344 - 3 +.39918 - 5
+.27854 - 3 +.59615 - 3 +.11900 + 1 +.17204 + 1 -.11300 + 0
+.23723 - 1 +.84362 - 2 +.33429 - 7

I_{bzmax}

+.39440 - 3 +.32373 - 3 +.12222 - 3 +.26739 - 3 +.45413 - 5
+.32219 - 3 +.68512 - 3 +.11900 + 1 +.19077 + 1 -.14500 + 0
+.11348 + 0 +.96630 - 2 +.27521 - 6

$I_{bz\,min}$

+.29220 - 3 +.18966 - 3 +.12433 - 3 +.24909 - 3 +.76018 - 5
+.16152 - 3 +.41153 - 3 +.16850 + 1 +.18854 + 1 +.24000 - 1
+.86991 - 2 +.75447 - 2 +.72156 - 6

$I_{b,max}$

+.39440 - 3 +.32373 - 3 +.12222 - 3 +.26739 - 3 +.42634 - 5
+.32191 - 3 +.68512 - 3 +.11900 + 1 +.19077 + 1 -.11300 + 0
+.11348 + 0 +.96638 - 2 +.30508 - 6

$I_{b,min}$

+.29220 - 3 +.18966 - 3 +.12433 - 3 +.24909 - 3 +.79268 - 5
+.16184 - 3 +.41153 - 3 +.16850 + 1 +.18854 + 1 -.80000 - 2
+.86991 - 2 +.75437 - 2 +.71323 - 6

$V_{2\,max}$

+.33220 - 3 +.22966 - 3 +.12222 - 3 +.25417 - 3 +.72034 - 5
+.20841 - 3 +.50206 - 3 +.16850 + 1 +.20729 + 1 -.13500 + 0
+.45111 - 1 +.86133 - 2 +.54476 - 6

$V_{2\,min}$

+.35129 - 3 +.28063 - 3 +.12433 - 3 +.26316 - 3 +.78830 - 5
+.25748 - 3 +.57121 - 3 +.11900 + 1 +.17237 + 1 +.14000 - 1
+.22713 - 1 +.84327 - 2 +.24884 - 5

$V_{T\,max}$

+.33220 - 3 +.22966 - 3 +.12222 - 3 +.26966 - 3 +.72034 - 5
+.20841 - 3 +.50206 - 3 +.16850 + 1 +.21489 + 1 -.13500 + 0
+.45095 - 1 +.86946 - 2 +.54476 - 6

$V_{T\,min}$

+.35129 - 3 +.28063 - 3 +.12433 - 3 +.24795 - 3 +.68619 - 5
+.25851 - 3 +.57325 - 3 +.11900 + 1 +.16507 + 1 +.14000 - 1
+.22812 - 1 +.83653 - 2 +.24884 - 5

V_{max}

+.32716 - 3 +.26683 - 3 +.12433 - 3 +.26316 - 3 +.81662 - 5
+.24106 - 3 +.52869 - 3 +.13500 + 1 +.17237 + 1 +.29400 + 0
+.20994 - 1 +.82656 - 2 +.27716 - 5

V_{min}

+.35460 - 3 +.24246 - 3 +.12222 - 3 +.25417 - 3 +.71361 - 5
+.22384 - 3 +.54150 - 3 +.15250 + 1 +.20729 + 1 -.41500 + 0
+.48683 - 1 +.87847 - 2 +.47745 - 6

$I_{b\,max}$

+.39440 - 3 +.32373 - 3 +.12222 - 3 +.26739 - 3 +.42634 - 5
+.32191 - 3 +.68512 - 3 +.11900 + 1 +.19077 + 1 -.11300 + 0
+.11348 + 0 +.96638 - 2 +.30508 - 6

$I_{b\,min}$

+.29220 - 3 +.18966 - 3 +.12433 - 3 +.24909 - 3 +.79268 - 5
+.16184 - 3 +.41153 - 3 +.16850 + 1 +.18854 + 1 -.80000 - 2
+.86991 - 2 +.75437 - 2 +.71323 - 6

+.40151 - 3 +.33795 - 3 +.13770 - 3 +.29469 - 3 +.32692 - 5
+.32930 - 3 +.69725 - 3 +.10250 + 1 +.18610 + 1 +.14000 - 1
+.11545 + 0 +.10616 - 1 +.10408 - 6

q_{max} 2-13-64 4

+.29640 - 3 +.19806 - 3 +.10988 - 3 +.22543 - 3 +.11137 - 4
+.18062 - 3 +.43505 - 3 +.15800 + 1 +.19321 + 1 -.13500 + 0
+.92559 - 2 +.68993 - 2 +.44706 - 5

q_{min}

+.33220 - 3 +.22966 - 3 +.12222 - 3 +.25417 - 3 +.12241 - 4
+.20669 - 3 +.49530 - 3 +.16850 + 1 +.20729 + 1 +.24000 - 1
+.44498 - 1 +.86363 - 2 +.58903 - 5

$I_{bs\,max}$

+.35129 - 3 +.28063 - 3 +.12433 - 3 +.26316 - 3 +.57580 - 5
+.27782 - 3 +.59367 - 3 +.11900 + 1 +.17237 + 1 -.14500 + 0
+.23622 - 1 +.84291 - 2 +.30155 - 7

$I_{bs\,min}$

13/7/64

Computer Run #7

J.P.L. Flip-Flop
65 K.C.
±15% Power Supply
±4% Resistors

PARAMETER

25

39+3

37.4+3

40.5+3

26

100+3

96+3

104+3

31

39+3

37.4+3

40.5+3

7/13/64
±15%

I_0	P	I_{L3}	V_T	V_1
+.34250 − 3	+.25625 − 3	+.12308 − 3	+.30940 − 4	+.67054 − 5
+.23475 − 3	+.53974 − 3	+.14200 + 1	+.19060 + 1	−.69000 − 1
+.29532 − 1	+.45102 − 2	+.10887 − 5		

Nominal Solutions

I_{1max}

+.44461 − 3	+.36295 − 3	+.13457 − 3	+.35909 − 4	+.35643 − 5
+.35546 − 3	+.76382 − 3	+.10750 + 1	+.20154 + 1	−.14500 + 0
+.12678 + 0	+.65979 − 2	+.91530 − 7		

I_{1min}

+.25640 − 3	+.17486 − 3	+.11096 − 3	+.26128 − 4	+.10948 − 4
+.15686 − 3	+.37409 − 3	+.15300 + 1	+.17417 + 1	+.24000 − 1
+.81100 − 2	+.29792 − 2	+.46148 − 5		

I_{2max}

+.42716 − 3	+.36683 − 3	+.13457 − 3	+.35909 − 4	+.43699 − 5
+.35820 − 3	+.74781 − 3	+.11900 + 1	+.20154 + 1	−.25000 − 1
+.12412 + 0	+.65265 − 2	+.10381 − 6		

I_{2min}

+.26180 − 3	+.14966 − 3	+.11096 − 3	+.26128 − 4	+.11240 − 4
+.13266 − 3	+.35551 − 3	+.16850 + 1	+.17417 + 1	−.96000 − 1
+.77005 − 2	+.28932 − 2	+.43597 − 5		

I_{3max}

+.39020 − 3	+.32402 − 3	+.15107 − 3	+.37293 − 4	+.35930 − 5
+.31387 − 3	+.66624 − 3	+.12350 + 1	+.18715 + 1	+.13500 + 0
+.11054 + 0	+.62070 − 2	+.12017 − 6		

I_{3min}

+.30043 − 3	+.20222 − 3	+.97531 − 4	+.24629 − 4	+.10353 − 4
+.18654 − 3	+.45006 − 3	+.13700 + 1	+.18856 + 1	−.25600 + 0
+.97998 − 2	+.31847 − 2	+.40196 − 5		

I_{4max}

+.39020 − 3	+.32402 − 3	+.13951 − 3	+.39346 − 4	+.35930 − 5
+.31387 − 3	+.66624 − 3	+.12350 + 1	+.19728 + 1	+.13500 + 0
+.11055 + 0	+.61523 − 2	+.12017 − 6		

I_{4min}

+.30043 − 3	+.20222 − 3	+.10561 − 3	+.23685 − 4	+.10353 − 4
+.18654 − 3	+.45006 − 3	+.13700 + 1	+.17867 + 1	−.25600 + 0
+.97927 − 2	+.32150 − 2	+.40196 − 5		

I_{5max}

+.37220 − 3	+.26966 − 3	+.13457 − 3	+.34066 − 4	+.13674 − 4
+.24447 − 3	+.56876 − 3	+.16850 + 1	+.22072 + 1	−.80000 − 2
+.51361 − 1	+.56171 − 2	+.64600 − 5		

I_{5min}

+.30819 − 3	+.23752 − 3	+.11096 − 3	+.28101 − 4	+.39611 − 5
+.23829 − 3	+.51596 − 3	+.11900 + 1	+.15523 + 1	−.11300 + 0
+.20728 − 1	+.34927 − 2	+.27414 − 8		

3 of 4

7/13/64
±15%

	+.43750 - 3	+.36683 - 3	+.13457 - 3	+.35909 - 4	+.42612 - 5
	+.36790 - 3	+.77710 - 3	+.11900 + 1	+.20154 + 1	-.14500 + 0
$I_{bz\,max}$	+.12898 + 0	+.64743 - 2	-.48544 - 8		
	+.25220 - 3	+.14966 - 3	+.11096 - 3	+.26128 - 4	+.76799 - 5
	+.11847 - 3	+.32528 - 3	+.16850 + 1	+.17417 + 1	+.24000 - 1
$I_{bz\,min}$	+.70340 - 2	+.29767 - 2	+.79969 - 6		
	+.43750 - 3	+.36683 - 3	+.13457 - 3	+.35909 - 4	+.39834 - 5
$I_{bi\,max}$	+.36762 - 3	+.77710 - 3	+.11900 + 1	+.20154 + 1	-.11300 + 0
	+.12898 + 0	+.64751 - 2	+.25019 - 7		
	+.25220 - 3	+.14966 - 3	+.11096 - 3	+.26128 - 4	+.80049 - 5
$I_{Li\,min}$	+.11880 - 3	+.32528 - 3	+.16850 + 1	+.17417 + 1	-.80000 - 2
	+.70340 - 2	+.29756 - 2	+.79135 - 6		
	+.37220 - 3	+.26966 - 3	+.13457 - 3	+.34066 - 4	+.72755 - 5
$V_{z\,max}$	+.24560 - 3	+.57630 - 3	+.16850 + 1	+.22072 + 1	-.13500 + 0
	+.52044 - 1	+.55914 - 2	+.61687 - 6		
	+.30819 - 3	+.23752 - 3	+.11096 - 3	+.27815 - 4	+.75796 - 5
$V_{z\,min}$	+.21720 - 3	+.49125 - 3	+.11900 + 1	+.15797 + 1	+.14000 - 1
	+.19728 - 1	+.34883 - 2	+.21850 - 5		
	+.37220 - 3	+.26966 - 3	+.13457 - 3	+.36062 - 4	+.72755 - 5
$V_{T\,max}$	+.24560 - 3	+.57630 - 3	+.16850 + 1	+.22880 + 1	-.13500 + 0
	+.52042 - 1	+.56029 - 2	+.61687 - 6		
	+.30819 - 3	+.23752 - 3	+.11096 - 3	+.26512 - 4	+.65585 - 5
$V_{T\,min}$	+.21822 - 3	+.49329 - 3	+.11900 + 1	+.14928 + 1	+.14000 - 1
	+.19813 - 1	+.34871 - 2	+.21850 - 5		
	+.28405 - 3	+.22373 - 3	+.11096 - 3	+.27815 - 4	+.78628 - 5
$V_{i\,max}$	+.20078 - 3	+.44874 - 3	+.13500 + 1	+.15797 + 1	+.29400 + 0
	+.18009 - 1	+.33388 - 2	+.24682 - 5		
	+.39460 - 3	+.28246 - 3	+.13457 - 3	+.34066 - 4	+.72082 - 5
$V_{i\,min}$	+.26103 - 3	+.61573 - 3	+.15250 + 1	+.22072 + 1	-.41500 + 0
	+.55616 - 1	+.57792 - 2	+.54957 - 6		
	+.43750 - 3	+.36683 - 3	+.13457 - 3	+.35909 - 4	+.39834 - 5
$I_{o\,max}$	+.36762 - 3	+.77710 - 3	+.11900 + 1	+.20154 + 1	-.11300 + 0
	+.12898 + 0	+.64751 - 2	+.25019 - 7		

4 of 4

7/13/64
±15%

+.25220 - 3 +.14966 - 3 +.11096 - 3 +.26128 - 4 +.80049 - 5
+.11880 - 3 +.32528 - 3 +.16850 + 1 +.17417 + 1 -.80000 - 2
for +.70340 - 2 +.29756 - 2 +.79135 - 6

+.44461 - 3 +.38106 - 3 +.15107 - 3 +.39346 - 4 +.33024 - 5
+.36931 - 3 +.77744 - 3 +.10250 + 1 +.19728 + 1 +.14000 - 1
+.12902 + 0 +.69453 - 2 +.13732 - 6
F_{max}

+.25640 - 3 +.15806 - 3 +.97531 - 4 +.23685 - 4 +.10549 - 4
+.14292 - 3 +.36106 - 3 +.15800 + 1 +.17867 + 1 -.13500 + 0
+.78388 - 2 +.27631 - 2 +.38819 - 5
P_{min}

+.37220 - 3 +.26966 - 3 +.13457 - 3 +.34066 - 4 +.12879 - 4
+.24420 - 3 +.56929 - 3 +.16850 + 1 +.22072 + 1 +.24000 - 1
+.51409 - 1 +.56183 - 2 +.65281 - 5
$I_{b_2\,max}$

+.30819 - 3 +.23752 - 3 +.11096 - 3 +.27815 - 4 +.57274 - 5
+.23757 - 3 +.51347 - 3 +.11900 + 1 +.15797 + 1 -.14500 + 0
+.20627 - 1 +.34864 - 2 -.53191 - 9
$I_{b_3\,min}$

RUN # 8

7/13/64
JPL Flip Flop
65 K.C.
± 5% Power Supply
± 4% Resistors

PARAMETER
25
39+3
37.4+3
40.5+3
26
100+3
96+3
104+3
31
39+3
37.4+3
40.5+3
32
5
4.75
5.25
33
3

I_1	I_2	I_3	I_4	I_5	
+.34250 - 3	+.25625 - 3	+.12308 - 3	+.30940 - 4	+.67054 - 5	Nominal
+.23475 - 3	+.53974 - 3	+.14200 + 1	+.19060 + 1	-.69000 - 1	
+.29532 - 1	+.45102 - 2	+.10887 - 5	V_T	V_1	
I_0	$P_{nom.}$	I_{b3}			
I_{1max}					
+.40151 - 3	+.31985 - 3	+.12222 - 3	+.32449 - 4	+.35336 - 5	
+.31521 - 3	+.68338 - 3	+.10750 + 1	+.18753 + 1	-.14500 + 0	
+.11342 + 0	+.54056 - 2	+.60843 - 7			
I_{1min}					
+.29640 - 3	+.21486 - 3	+.12433 - 3	+.29876 - 4	+.11586 - 4	
+.19438 - 3	+.44784 - 3	+.15300 + 1	+.18819 + 1	+.24000 - 1	
+.97188 - 2	+.38723 - 2	+.52526 - 5			
	I_{2max}				
+.38405 - 3	+.32373 - 3	+.12222 - 3	+.32449 - 4	+.43392 - 5	
+.31795 - 3	+.66737 - 3	+.11900 + 1	+.18753 + 1	-.25000 - 1	
+.11076 + 0	+.53405 - 2	+.73118 - 7			
	I_{2min}				
+.30180 - 3	+.18966 - 3	+.12433 - 3	+.29876 - 4	+.11878 - 4	
+.17017 - 3	+.42926 - 3	+.16850 + 1	+.18819 + 1	-.96000 - 1	
+.93092 - 2	+.37762 - 2	+.49974 - 5			
		I_{3max}			
+.35020 - 3	+.28402 - 3	+.13770 - 3	+.33833 - 4	+.35623 - 5	
+.27672 - 3	+.59201 - 3	+.12350 + 1	+.17313 + 1	+.13500 + 0	
+.98222 - 1	+.50759 - 2	+.89484 - 7			
		I_{3min}			
+.34353 - 3	+.24532 - 3	+.10988 - 3	+.28377 - 4	+.10991 - 4	
+.22716 - 3	+.53002 - 3	+.13700 + 1	+.20258 + 1	-.25600 + 0	
+.11546 - 1	+.41266 - 2	+.46573 - 5			
			I_{4max}		
+.35020 - 3	+.28402 - 3	+.12716 - 3	+.35598 - 4	+.35623 - 5	
+.27672 - 3	+.59201 - 3	+.12350 + 1	+.18326 + 1	+.13500 + 0	
+.98231 - 1	+.50298 - 2	+.89484 - 7			
			I_{4min}		
+.34353 - 3	+.24532 - 3	+.11898 - 3	+.27145 - 4	+.10991 - 4	
+.22716 - 3	+.53002 - 3	+.13700 + 1	+.19269 + 1	-.25600 + 0	
+.11539 - 1	+.41640 - 2	+.46573 - 5			
				I_{5max}	
+.33220 - 3	+.22966 - 3	+.12222 - 3	+.30606 - 4	+.13036 - 4	
+.20695 - 3	+.49477 - 3	+.16850 + 1	+.20670 + 1	-.80000 - 2	

3 of 4 +.44673 - 1 +.45412 - 2 +.58223 - 5

Is min

+.35129 - 3 +.28063 - 3 +.12433 - 3 +.31850 - 4 +.39918 - 5
+.27854 - 3 +.59615 - 3 +.11900 + 1 +.16924 + 1 -.11300 + 0
+.23954 - 1 +.44743 - 2 +.33429 - 7

Ib max

+.39440 - 3 +.32373 - 3 +.12222 - 3 +.32449 - 4 +.45413 - 5
+.32219 - 3 +.68512 - 3 +.11900 + 1 +.18753 + 1 -.14500 + 0
+.11371 + 0 +.53552 - 2 +.27521 - 6

Ib min

+.29220 - 3 +.18966 - 3 +.12433 - 3 +.29876 - 4 +.76018 - 5
+.16152 - 3 +.41153 - 3 +.16850 + 1 +.18819 + 1 +.24000 - 1
+.89183 - 2 +.37746 - 2 +.72156 - 6

Ib max

+.39440 - 3 +.32373 - 3 +.12222 - 3 +.32449 - 4 +.42634 - 5
+.32191 - 3 +.68512 - 3 +.11900 + 1 +.18753 + 1 -.11300 + 0
+.11371 + 0 +.53561 - 2 +.30508 - 6

Ib min

+.29220 - 3 +.18966 - 3 +.12433 - 3 +.29876 - 4 +.79268 - 5
+.16184 - 3 +.41153 - 3 +.16850 + 1 +.18819 + 1 -.80000 - 2
+.89183 - 2 +.37735 - 2 +.71323 - 6

Ib max

+.33220 - 3 +.22966 - 3 +.12222 - 3 +.30606 - 4 +.72034 - 5
+.20841 - 3 +.50206 - 3 +.16850 + 1 +.20670 + 1 -.13500 + 0
+.45334 - 1 +.45192 - 2 +.54476 - 6

Ib min

+.35129 - 3 +.28063 - 3 +.12433 - 3 +.31563 - 4 +.78830 - 5
+.25748 - 3 +.57121 - 3 +.11900 + 1 +.17199 + 1 +.14000 - 1
+.22945 - 1 +.44708 - 2 +.24884 - 5

Ib max

+.33220 - 3 +.22966 - 3 +.12222 - 3 +.32399 - 4 +.72034 - 5
+.20841 - 3 +.50206 - 3 +.16850 + 1 +.21397 + 1 -.13500 + 0
+.45332 - 1 +.45286 - 2 +.54476 - 6

Ib min

+.35129 - 3 +.28063 - 3 +.12433 - 3 +.30048 - 4 +.68619 - 5
+.25851 - 3 +.57325 - 3 +.11900 + 1 +.16250 + 1 +.14000 - 1
+.23030 - 1 +.44685 - 2 +.24884 - 5

Ib max

+.32716 - 3 +.26683 - 3 +.12433 - 3 +.31563 - 4 +.81662 - 5
+.24106 - 3 +.52869 - 3 +.13500 + 1 +.17199 + 1 +.29400 + 0
+.21225 - 1 +.43037 - 2 +.27716 - 5

Ib min

+.35460 - 3 +.24246 - 3 +.12222 - 3 +.30606 - 4 +.71361 - 5
+.22384 - 3 +.54150 - 3 +.15250 + 1 +.20670 + 1 -.41500 + 0

4 of 4 +.48907 - 1 +.46907 - 2 +.47745 - 6

$I_{o_{max}}$ +.39440 - 3 +.32373 - 3 +.12222 - 3 +.32449 - 4 +.42634 - 5
+.32191 - 3 +.68512 - 3 +.11900 + 1 +.18753 + 1 -.11300 + 0
+.11371 + 0 +.53561 - 2 +.30508 - 6

$I_{o_{min}}$ +.29220 - 3 +.18966 - 3 +.12433 - 3 +.29876 - 4 +.79268 - 5
+.16184 - 3 +.41153 - 3 +.16850 + 1 +.18819 + 1 -.80000 - 2
+.89183 - 2 +.37735 - 2 +.71323 - 6

P_{max} +.40151 - 3 +.33795 - 3 +.13770 - 3 +.35598 - 4 +.32692 - 5
+.32930 - 3 +.69725 - 3 +.10250 + 1 +.18326 + 1 +.14000 - 1
+.11571 + 0 +.57090 - 2 +.10408 - 6

P_{min} +.29640 - 3 +.19806 - 3 +.10988 - 3 +.27145 - 4 +.11137 - 4
+.18062 - 3 +.43505 - 3 +.15800 + 1 +.19269 + 1 -.13500 + 0
+.94542 - 2 +.36183 - 2 +.44706 - 5

$I_{b_{3max}}$ +.33220 - 3 +.22966 - 3 +.12222 - 3 +.30606 - 4 +.12241 - 4
+.20669 - 3 +.49530 - 3 +.16850 + 1 +.20670 + 1 +.24000 - 1
+.44721 - 1 +.45423 - 2 +.58903 - 5

$I_{b_{3min}}$ +.35129 - 3 +.28063 - 3 +.12433 - 3 +.31563 - 4 +.57580 - 5
+.27782 - 3 +.59367 - 3 +.11900 + 1 +.17199 + 1 -.14500 + 0
+.23853 - 1 +.44673 - 2 +.30155 - 7

APPENDIX D
TABLE I

2N914 (Q3) LOW CURRENT V_{be} AND I_b MEASUREMENTS

V_{ce} = 2v

TR #	I_C	25°C I_b	25°C V_{be}	+80°C I_b	+80°C V_{be}	-10°C I_b	-10°C V_{be}
	μa.	μa.	mv	μa.	mv.	μa.	mv.
2	1.0	0.2	503	---	344	---	579
	10	0.8	566	0.2	420	1.3	632
	20	1.2	582	0.4	444	1.9	644
	30	1.6	592	0.6	460	2.4	653
	50	2.4	603	1.0	475	3.4	665
	100	3.8	621	1.9	497	5.4	582
6	1.0	0.3	489	---	343	0.2	563
	10	0.8	551	0.2	419	1.1	619
	20	1.1	570	0.4	437	1.7	638
	30	1.5	581	0.5	450	2.1	646
	50	2.0	595	0.8	465	3.0	659
	100	3.3	614	1.6	489	4.8	676
7	1.0	0.2	502	---	354	.35	568
	10	1.7	570	0.5	427	2.5	624
	20	2.4	585	0.85	446	4.0	644
	30	3.2	596	1.2	460	5.0	653
	50	4.4	606	1.9	477	6.8	667
	100	7.1	624	3.4	499	10.8	684
10	1.0	---	452	---	337	0.4	561
	10	0.3	560	---	410	0.6	610
	20	0.4	574	0.2	438	0.9	633
	30	0.6	584	0.3	448	1.1	642
	50	0.9	597	0.5	465	1.5	654
	100	1.6	614	1.0	487	2.5	673

Conclusions:

1. +0.3v seems to be quite safe as an upper limit on the forward bias of an OFF transistor, ie. $I_c < 1\ \mu a.$
2. V_{be} and h_{FE} data (Q3) used in subsequent computer runs.

Meters Used

I_c - TM - 0064
I_b - TP - 0101
V_{be} - ND - 0163
V_{ce} - TP - 0001

TABLE II

Tabulation of I_b, at fixed Collector currents and at V_{ce} = 0.3v from data plotted on the 2N914.

TR#	I_c Ma.	I_b Ma.	B_{10} I_c/I_b	T °C	I_c Ma.	I_b Ma.	B_6 I_c/bI
1	10	0.18	55.5	25	6	0.11	54.5
2	10	0.215	46.5		6	0.13	46.2
3	10	.195	51.3		6	.117	51.3
4	10	.100	100		6	.060	100
5	10	.120	83.4		6	.072	83.5
6	10	.155	69.5		6	.096	62.4
7	10	.284	35.2		6	.185	32.5
8	10	.140	71.4		6	.086	69.8
9	10	.160	62.5		6	.100	60.0
10	10	.118	84.7		6	.070	85.8
		+80°C		+80°C		+80°C	
TR#							
7	10	.255	39.2		6	.160	37.5
10	10	.130	77.0		6	.078	76.9
		-10°C		-10°C		-10°C	
7	10	.370	27.0		6	.234	25.6
10	10	.310	32.3		6	.142	42.2

TABLE III

2N914 Nonsaturated and Saturated Beta Measurements @ -10°C

	I_b (ma)									
I_c V_{ce}	TR # 1	TR # 2	TR # 3	TR # 4	TR # 5	TR # 6	TR # 7	TR # 8	TR # 9	TR # 10
6ma .2V	.210	.300	.260	.160	.160	.200	.320		.210	.150
Beta	28.6	20	23.1	37.5	37.5	30	18.8		28.6	40
6ma .3V	.130	.180	.150	.080	.100	.140	.240		.108	.077
Beta	46	33.4	40	75	60	42.8	25		55.6	78
6ma 2.0V	.110	.135	.120	.060	.078	.110	.200		.110	.080
Beta	54.5	44.5	50	100	77	54.5	30		54.5	75
6ma 5.0V	.100	.120	.110	.050	.060	.090	.170		.090	.060
Beta	60	50	54.5	120	100	66.6	35.2		66.6	100
10ma .2V	.380	.460	.410	.220	.270	.320	.460		.360	.235
Beta	26.4	21.7	24.4	45.5	37.0	31.3	21.7		27.8	42.5
10ma .3V	.200	.260	.240	.120	.135	.200	.350		.200	.135
Beta	50	38.5	41.7	83.4	74.0	50	28.6		50	74.0
10ma 2.0V	.175	.225	.215	.090	.110	.165	.320		.170	.120
Beta	57.2	44.5	46.5	111	91.0	60.5	31.3		58.8	83.4
10ma 5.0V	.160	.200	.190	.085	.100	.150	.160		.145	.100
Beta	62.5	50	52.6	118	100	66.6	62.5		69.0	100

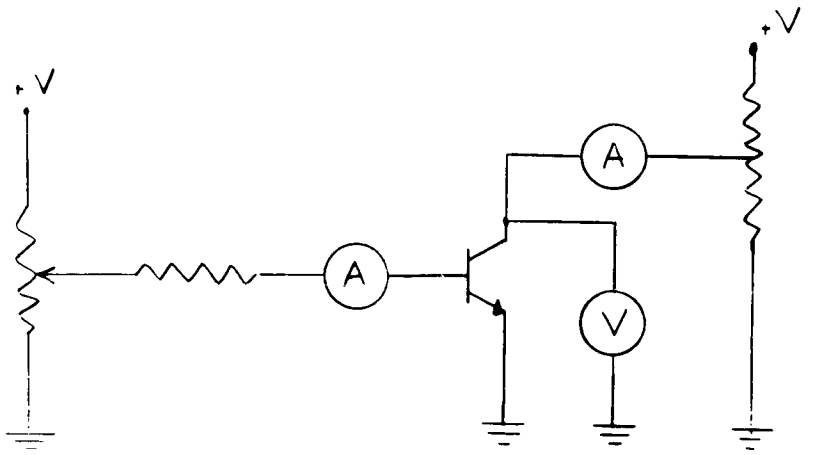


TABLE IV

V_F MEASUREMENTS FDS 643 DIODES

Diode #	I_F μa	25°C V_F mv.	+80°C V_F mv.	-10°C V_F mv.
1.	0.1	153	20.3	265
	0.5	239	63	338
	1.0	275	89	364
D_1 minimum operating point	2.0	299	138	401
→	4.0	340	169	426
	10.0	384	223	466
2.	0.1	157	20.3	268
	0.5	233	63	346
	1.0	276	89	364
	2.0	299	136	399
	4.0	341	173	425
	10.0	387	224	468
3.	0.1	149	20.5	268
	0.5	227	64	343
	1.0	264	91	365
	2.0	300	134	397
	4.0	333	174	426
	10.0	379	224	468

Ammeter - Keithley Instr.
IC# TP 0004
Due Date Next Cal. - 11/13/64

Voltmeter - J. Fluke
IC ND-0163
Due Date Next Cal. - 8/22/64

Power Supply - Power Design
IC# TG 0002

Diode Data used to get Fwd. voltage of D_1 and T.C., for computer run of Flip-Flop

TABLE V

D.C. Bias Measurements - J.P.L. Flip-Flop
500 D.C., ±1% resistors
R_{13} and R_{14} added
All diodes FDS-643
All transistors 2N914

				Flip-Flop "o" side ON			Flip-Flop "1" side ON		
T°	Vcc + volts	Vb - volts	R_L ohms	V_{11} volts	V_{2o} volts	V_{To} volts	V_{1o} volts	V_{21} volts	V_{T1}*
25°C	5	3	----	-.140	1.260	1.880	-.100	1.350	1.500
	5	3	500	-.060	1.435	1.920	-.030	1.435	1.600
	4.25	2.55	----	-.140	1.340	1.58	-.100	1.250	1.220
	4.25	2.55	500	-.060	1.410	1.65	-.030	1.415	1.300
	5.75	3.45	----	-.140	1.360	2.00	-.110	1.36	1.620
	5.75	3.45	500	-.060	1.440	2.10	-.030	1.44	1.700
	5	3	----	+.080	1.120	1.720	+.140	1.12	1.450
	5	3	500	+.170	1.200	1.780	+.225	1.205	1.500
+80°C	4.25	2.55	----	±.080	1.110	1.500	+.140	1.110	1.300
	4.25	2.55	500	±.162	1.195	1.580	+.240	1.180	1.382
	5.75	3.45	----	+.081	1.130	1.940	+.142	1.120	1.650
	5.75	3.45	500	+.172	1.215	2.000	+.240	1.200	1.740
	5	3	----	-.240	1.490	1.890	-.220	1.470	1.450
	5	3	500	-.170	1.499	1.910	-.135	1.490	1.510
	4.25	2.55	----	-.220	1.460	1.650	-.205	1.460	1.305
	4.25	2.55	500	-.160	1.480	1.700	-.140	1.480	1.380
-10°C	5.75	3.45	----	±.222	1.470	2.090	-.215	1.480	1.650
	5.75	3.45	500	-.158	1.500	2.150	-.142	1.500	1.720

Power Supplies - Power Design IC# TG-0002 - IC# TG-0021

Voltmeter - RCA - Voltohmist ±3% TG-0026

* Shorted diode (D_6), nullified the V_{T1} values measured. Considering that D_6 should have resulted in at least 0.4 volts at the highest temperature it can be seen that for all cases tested, V_T V_2 is positive, ie., the input diodes are back biased by at least 0.2 volts.

TABLE VI

Tabulation of 2N914 Flip-Flop Operating Voltages*

Data Source	Parameter	Suggested Spec. Operating Point @80°C	Suggested Spec. Limits
From Plots Appendix D	V_{be_3} =	0.437v. @ I_c = 20 μ a.	0.410
From Table IV	V_{D_1} =	0.169v. @ 4.0 μ a.	0.150
			0.560
From Plots Appendix D	V_{ce_2} =	0.180v. @ I_c = 0.4ma. I_b = 0.12ma.	0.20
From Plots Appendix D	V_{be_1} =	0.650v. @ I_c = 6ma. I_b = 0.3 ma.	0.69
			0.89

$$V_1 = 0.89v. - 0.56v. = 0.33v.^*$$

The data table I shows that at 0.33v. maximum, the collector current of Q_4 will be less than 1 μ a. To increase I_c of Q_4 to even 20 μ a will take an additional 0.1 volts.

* Purpose of this table is to show the worst values for diode and transistor voltages measured along with a suggested specification limit on these voltages (which includes a tolerance added to the measured values). These specification limits will guarantee that when either Q_1 or Q_4, F/F are to be OFF, they will be OFF.

TABLE VII

Measurement of Noise Immunity - Flip Flop

Temp.	V_T (Set) volts	V_2 (Meas.) volts	V_T-V_2 (Calc.) volts	V_1 (Meas.) volts	Noise Pulse t_f usec.	Va. c. peak to peak
-10^0C	1.5	1.5	0.0*	-0.2	0.1	2.3
	1.5	1.5	0.0	-0.2	0.2	2.6
	1.5	1,5	0.0	-0.2	0.4	3.2
	1.5	1.5	0.0	-0.2	1.0	4.75 (would not trigger)
$+80^0$C	1.6**	1,35	+0.25	+0.17	0.1	2.2
	1.6	1.35	+0.25	+0.17	0.2	2.6
	1.6	1.35	+0.25	+0.17	0.4	3.6
	1.6	1.35	+0.25	+0.17	1.0	4.75 (would not tiggger)

Purpose: The computer Runs show the D.C. voltage that must be exceeded to begin triggering the F/F. Because of the transient response of the F/F and the attenuation due to the charging of the input capacitors it will take larger noise pulses than indicated by the D.C. values to trigger the F/F. These measurements give an indication of the overall noise immunity of the F/F.

* Computer Run #5, P. , worst case V_T-V_2 = 0v. @ -10^0C.
** Computer Run #5, worst case minimum value for V_T = +1.6v.

TABLE VII (Cont'd.)

Test Conditions

1. R9 returned to separate power supply for independent adjustment of V_T. So that worst case computed V_T-V_2 could be simulated.

2. Vcc = +4.25v. Condition for which V_T is minimum value set in test. Also I_{b_2} = min., therefore current that must be pulled through D_3 to trigger F/F is minimum.

3. Q_2 = Low gain transistor, TR #7

4. Q_3 = High gain transistor, TR #10

5. Q_1 and Q_2 in ON state.

6. Output load is $\frac{4.5v.}{750 \text{ ohms}} \approx$ 6ma. (only on Q_1 Q_2 unloaded)

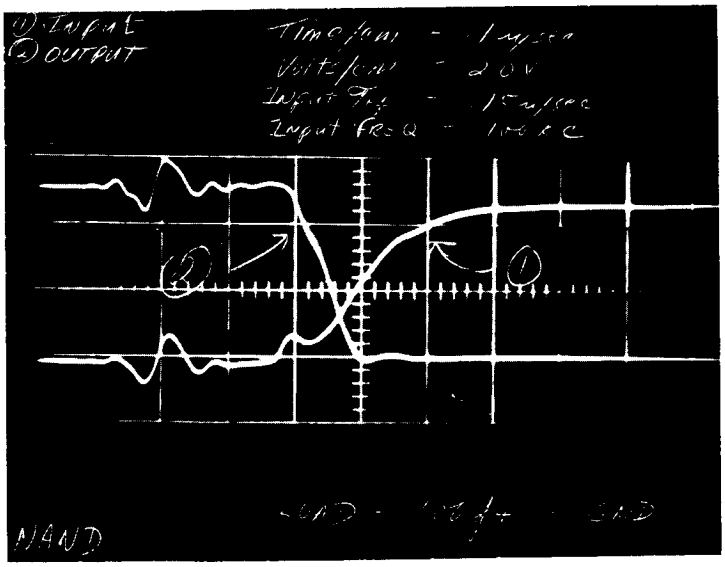
7. Noise wave form amplitude adjusted until occasional random triggering of F/F takes place. Then noise amplitude reduced until no triggering takes place. Amplitude at which no triggering takes place is recorded value.

8. Noise Pulse - t_f - fall time negative edge
   Pw - pulse width
   F - noise pulse repetition rate
   Va.c. - amplitude of negative edge

9. Q_1 = TR #2 Q_4 = TR #6

10. Noise pulse width set at 10usec., repetition rate of Noise signal 50K.C.

At 25°C., Vcc = 5.75v., V_T = max. = +2.3 volts, the input signals required for solid triggering versus input t_f were measured as: t_f = 0.1usec. Va.c. $\geq$2.7v., t_f = 0.2usec. Va.c. $\geq$3.1v. t_f = 0.4usec. Va.c. = 3.9v. (Note: Input signal @Vcc = 5.75v. will be about 5.5 volts. At 25°C, Vcc = 4.25v., V_T = 1.75v., t_f = 0.1usec. Va.c. $\geq$2.8v., t_f = 0.2usec. Va.c. $\geq$3.0v., t_f = 0.4usec Va.c. $\geq$3.6v.

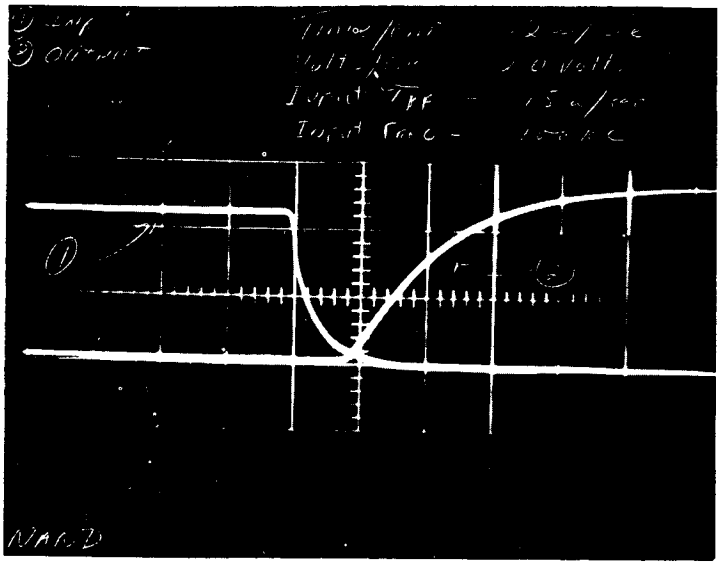


Nand

I_o = 200 μ a

C_s = 100 pf

Output t_r = 0.09 μ sec.



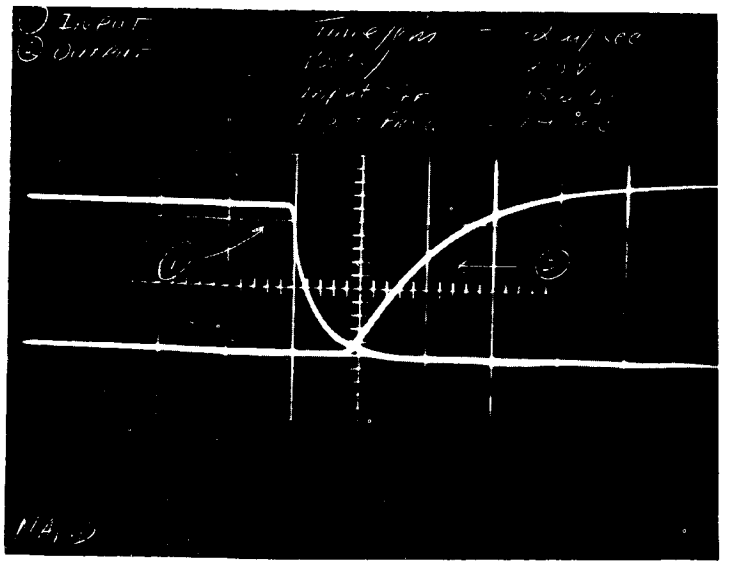
Nand

I"o" = 200 μa

Input t_r = 0.2 μ sec.

Output t_f = 0.5 μ sec.

t_{od} = 0.16 μ sec.



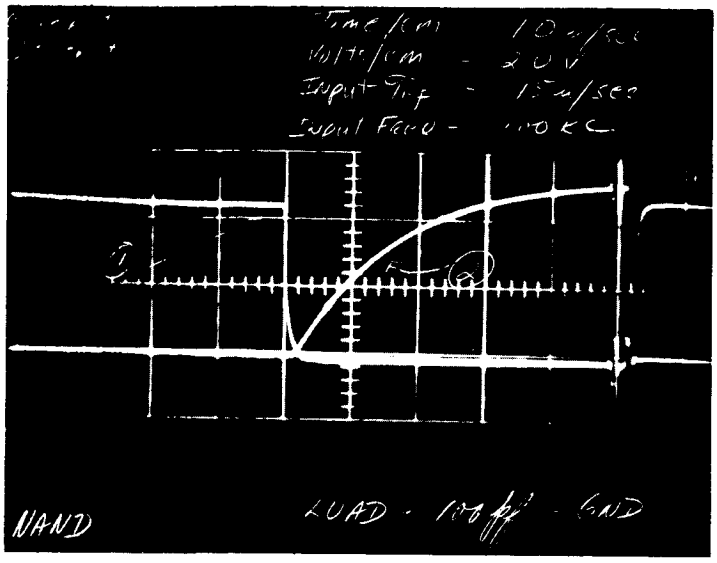
Nand

I"o" = 200 μa

Input t_r = 0.2 μ sec.

Output t_f = 0.5 μ sec.

t_{od} = 0.16 μ sec.

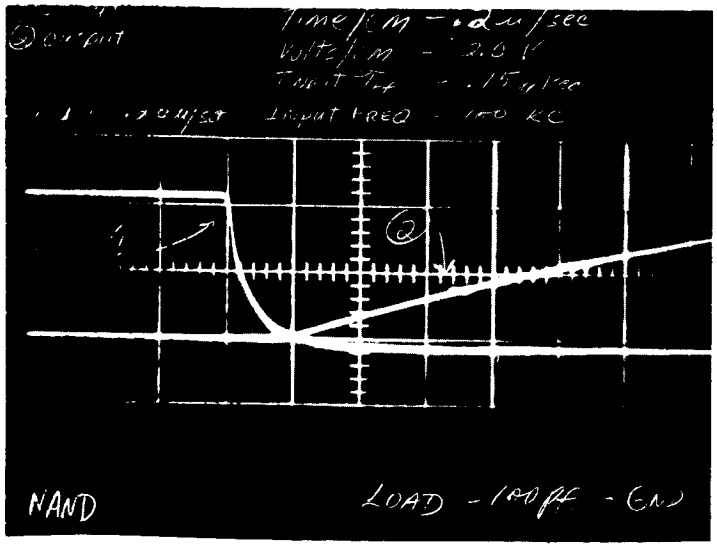


Nand

I"o" = 200 μ a

C_s = 100 pf

Output t_f = 3 μ sec.

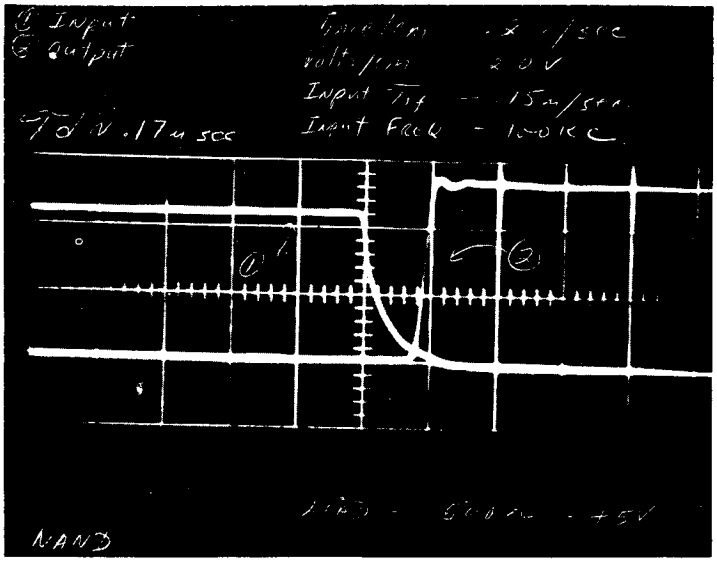


Nand

I"o" = 200 μ a

C_s = 100 pf

Output t_{od} = 0.18 μ sec.



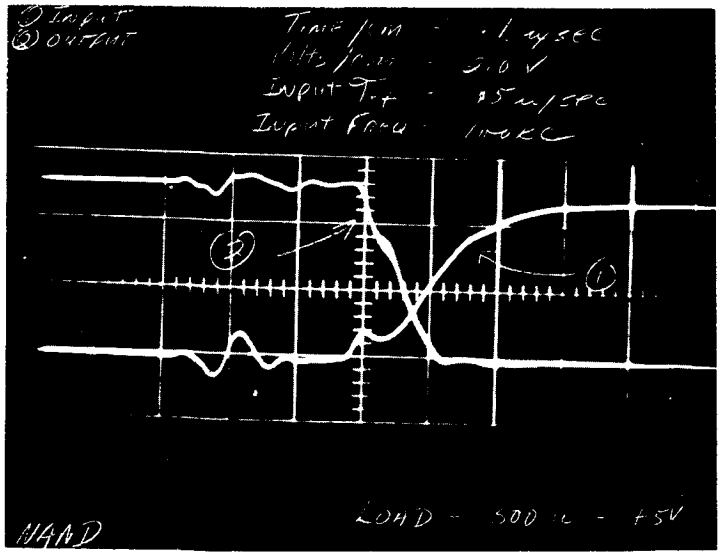
Nand

I"o" = 10 ma.

Input t_r = 0.16 μ sec.

Output t_f = 0.05 μ sec.

t_{od} = 0.18 μ sec.



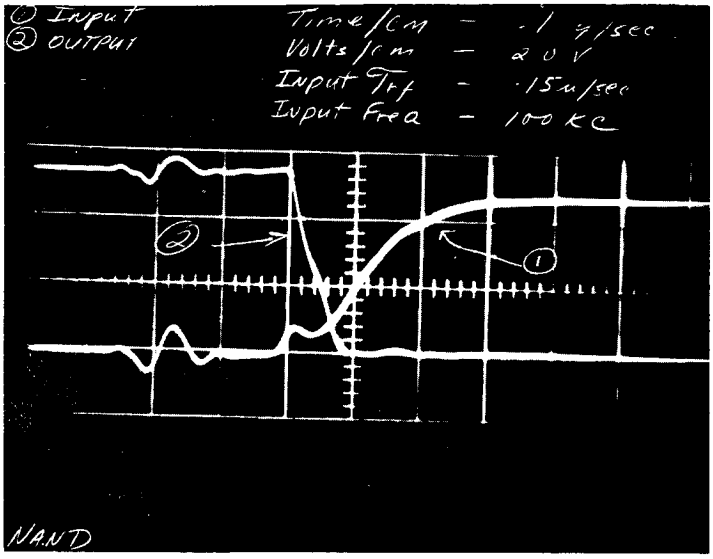
Nand

I"o" = 10 ma.

Input t_r = 0.25 μ sec.

Output t_r = 0.12 μ sec.

t_{dr} = 15 nsec.



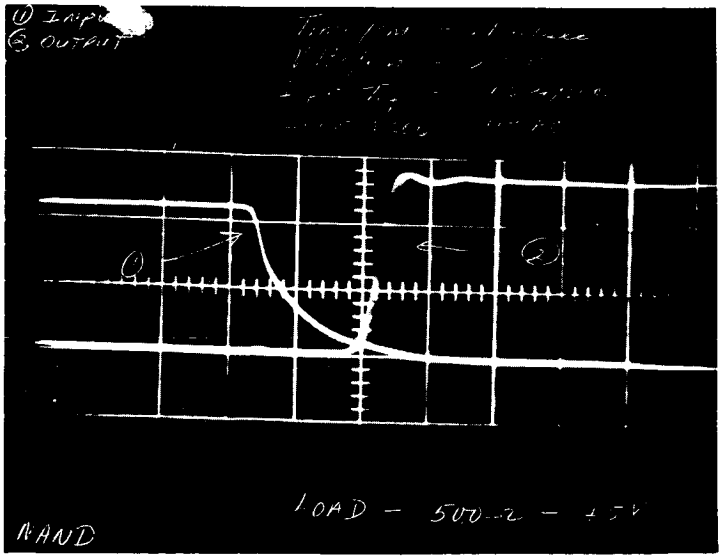
Nand

I"o" = 200 μ a

Input t_r = 0.25 μ sec.

Output t_f = 0.08 μ sec.

t_{d_r} = 15 nsec.



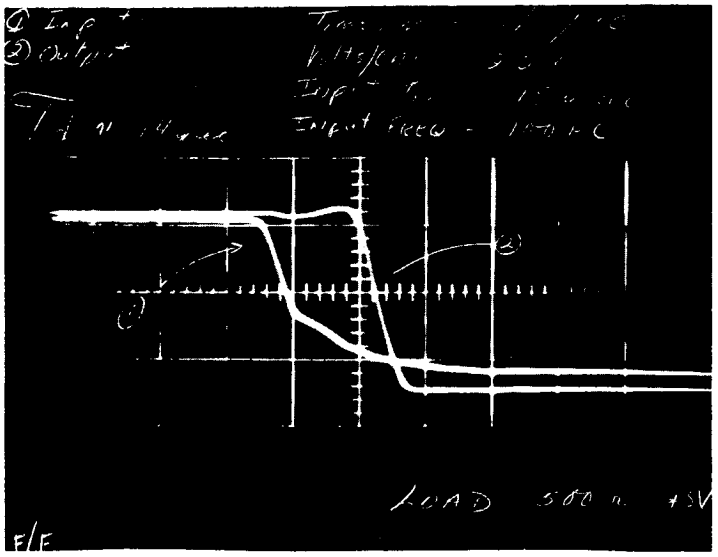
Nand

I"o" = 10 ma.

Input t_r = 0.16 μ sec.

Output t_f = 0.05 μ sec.

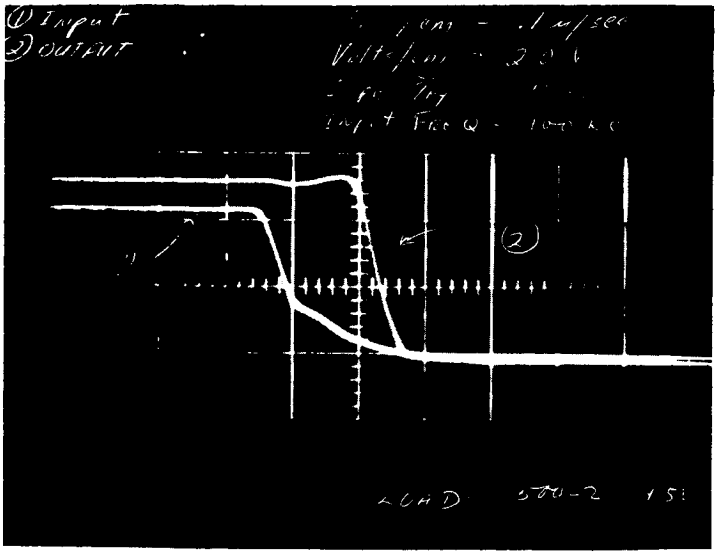
t_{od} = 0.18 μ sec.



F/F

I"o" = 10 ma.

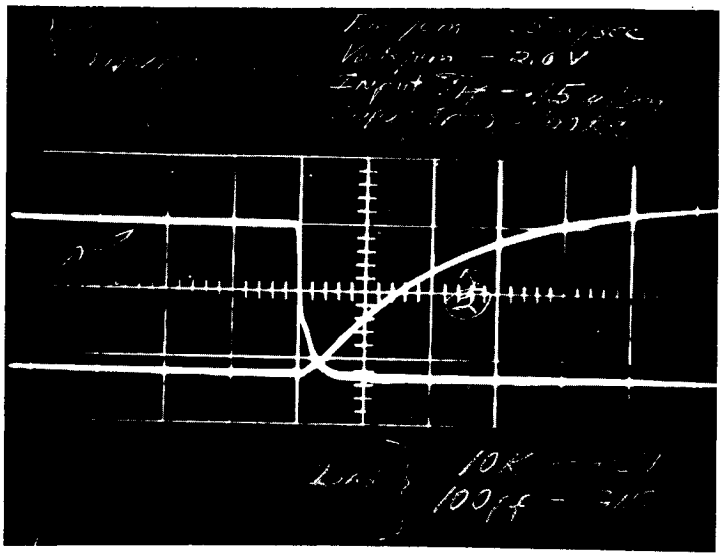
Output t_d = 0.15 μ sec.



F/F

I"o" = 10 ma.

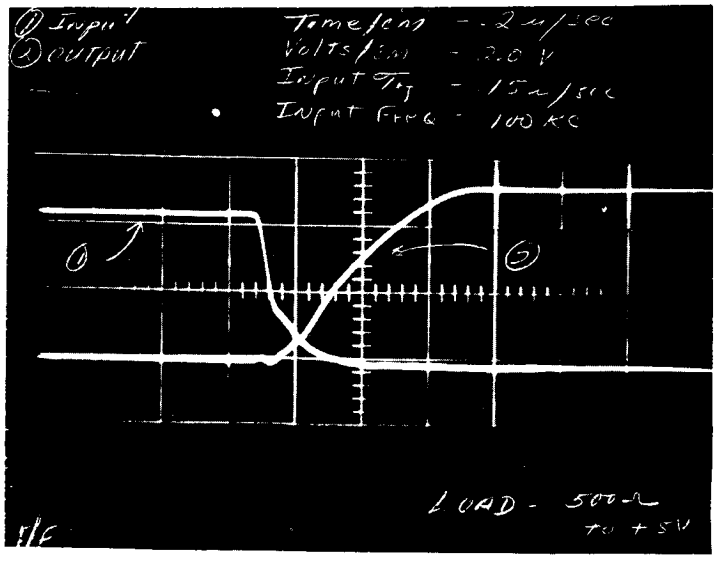
Output t_r = 60 nsec.



F/F

I"o" = 500 μ a

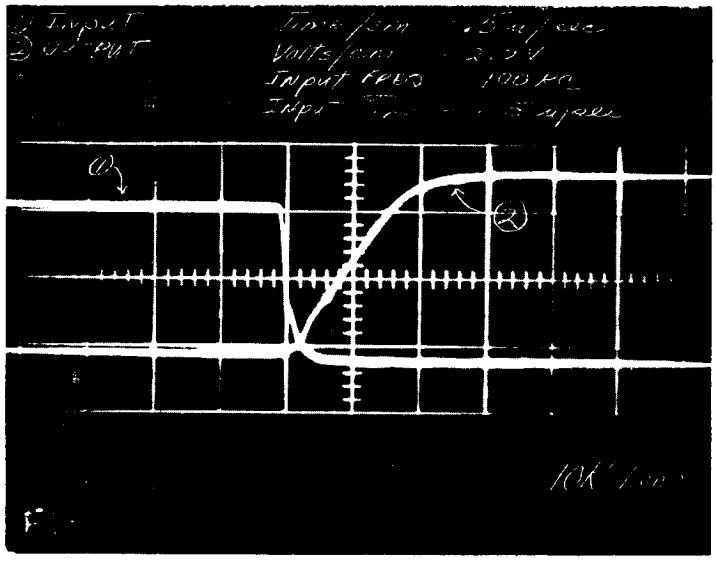
Output t_f = 2 μ sec.



F/F

I"o" = 10 ma.

Output t_r = 0.5 μ sec.

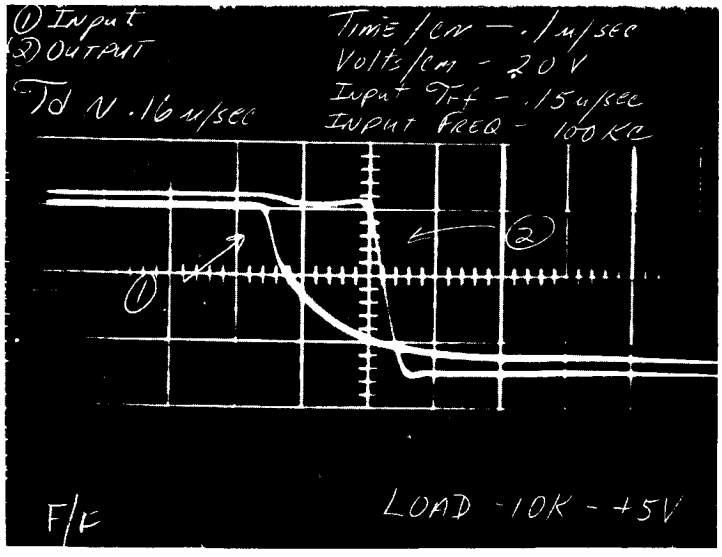


F/F

I"o" = 500 μa

Input t_r = 100 nsec.

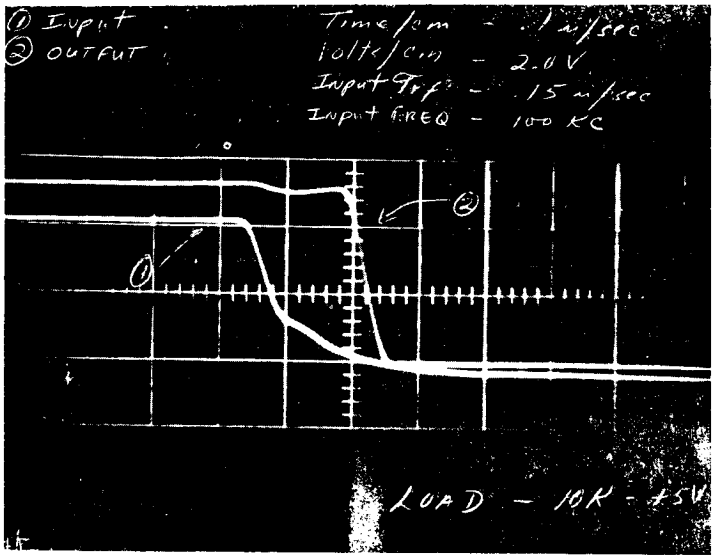
Output t_f = 1 μ sec.



F/F

I"o" = 500 μ a

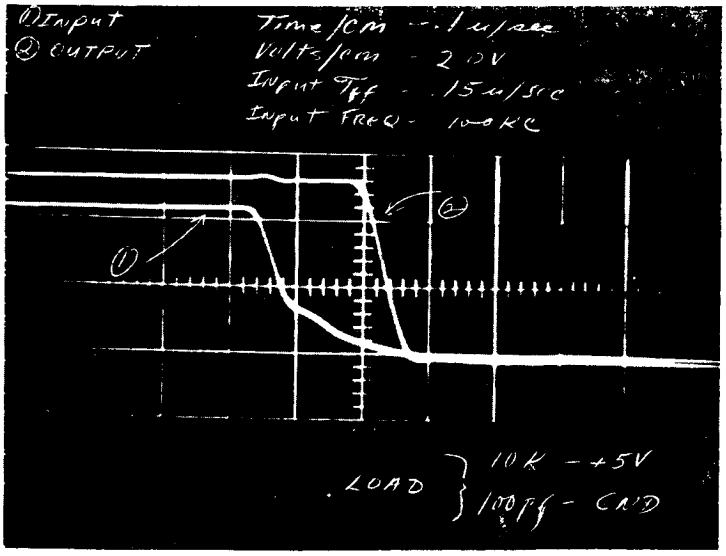
t_d = 0.16 μ sec.



F/F

I"o" = 500 μa

Output t_r = 50 nsec.

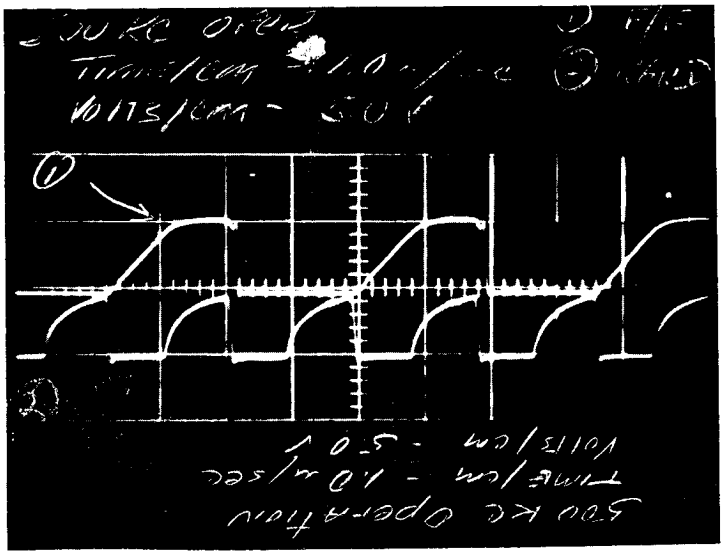


F/F

I"o" = 500 μa

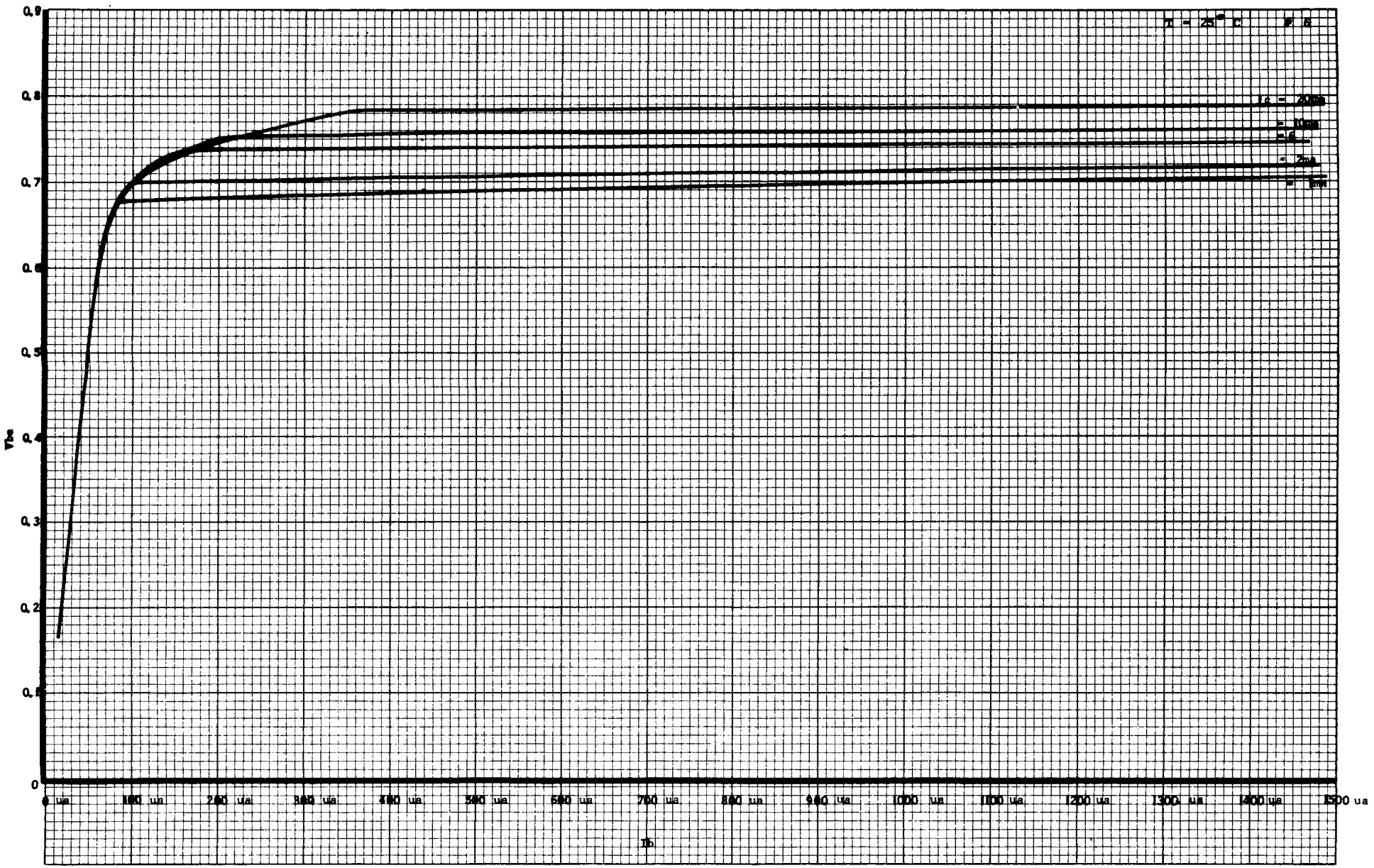
C_s = 100 pf

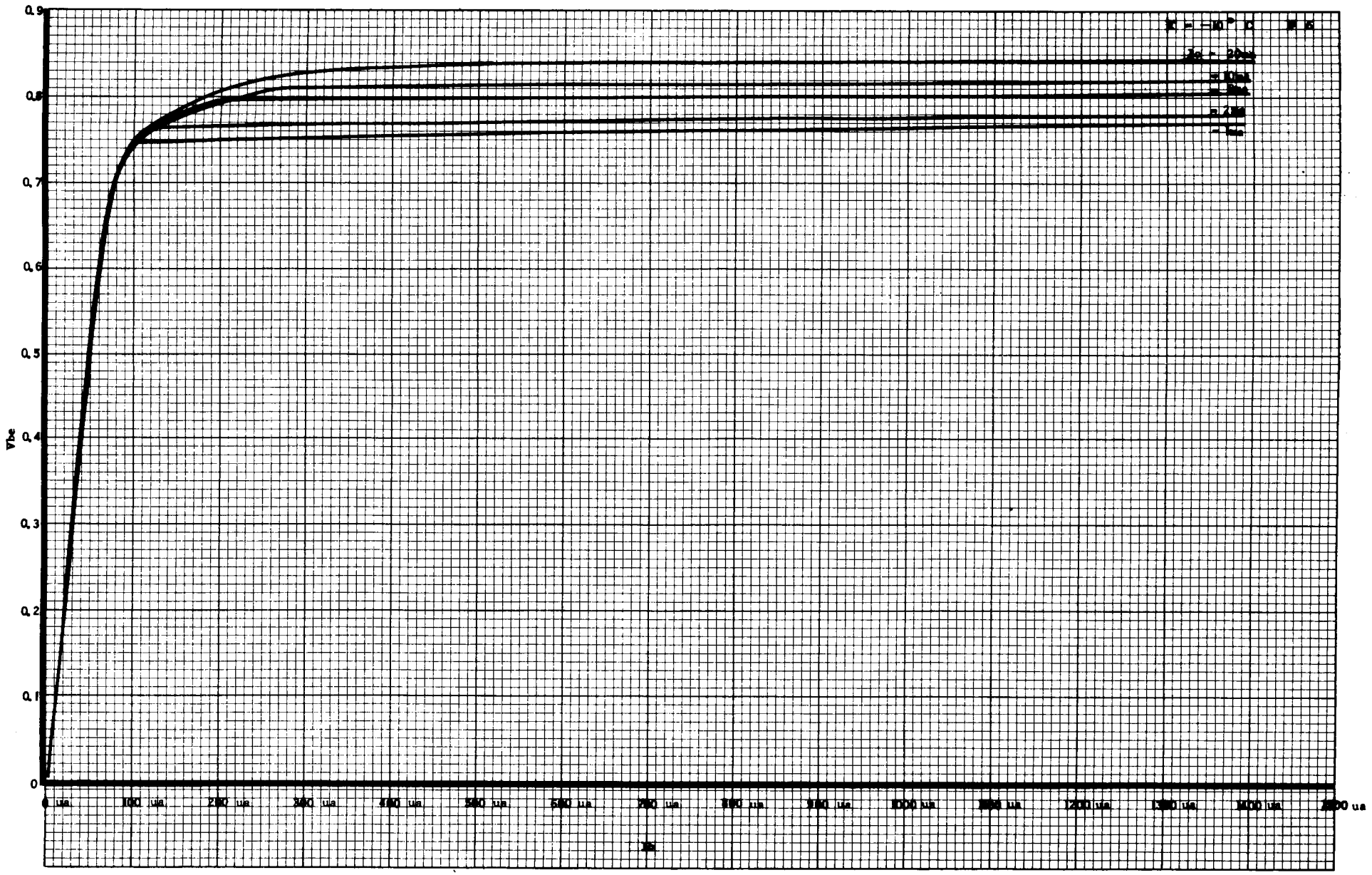
Output t_r = 60 nsec.



F/F

500 KC Operation


Tj = 25° C
Ic = 20mA
= 10mA
= 5
= 2mA
= 1mA
Vce
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0 ua
100 ua
200 ua
300 ua
400 ua
500 ua
600 ua
700 ua
800 ua
900 ua
1000 ua
1100 ua
1200 ua
1300 ua
1400 ua
1500 ua
Ib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0.5
0.4
0.3
0.2
0.1
0
Vbe
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300 ua
400 ua
500 ua
600 ua
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800 ua
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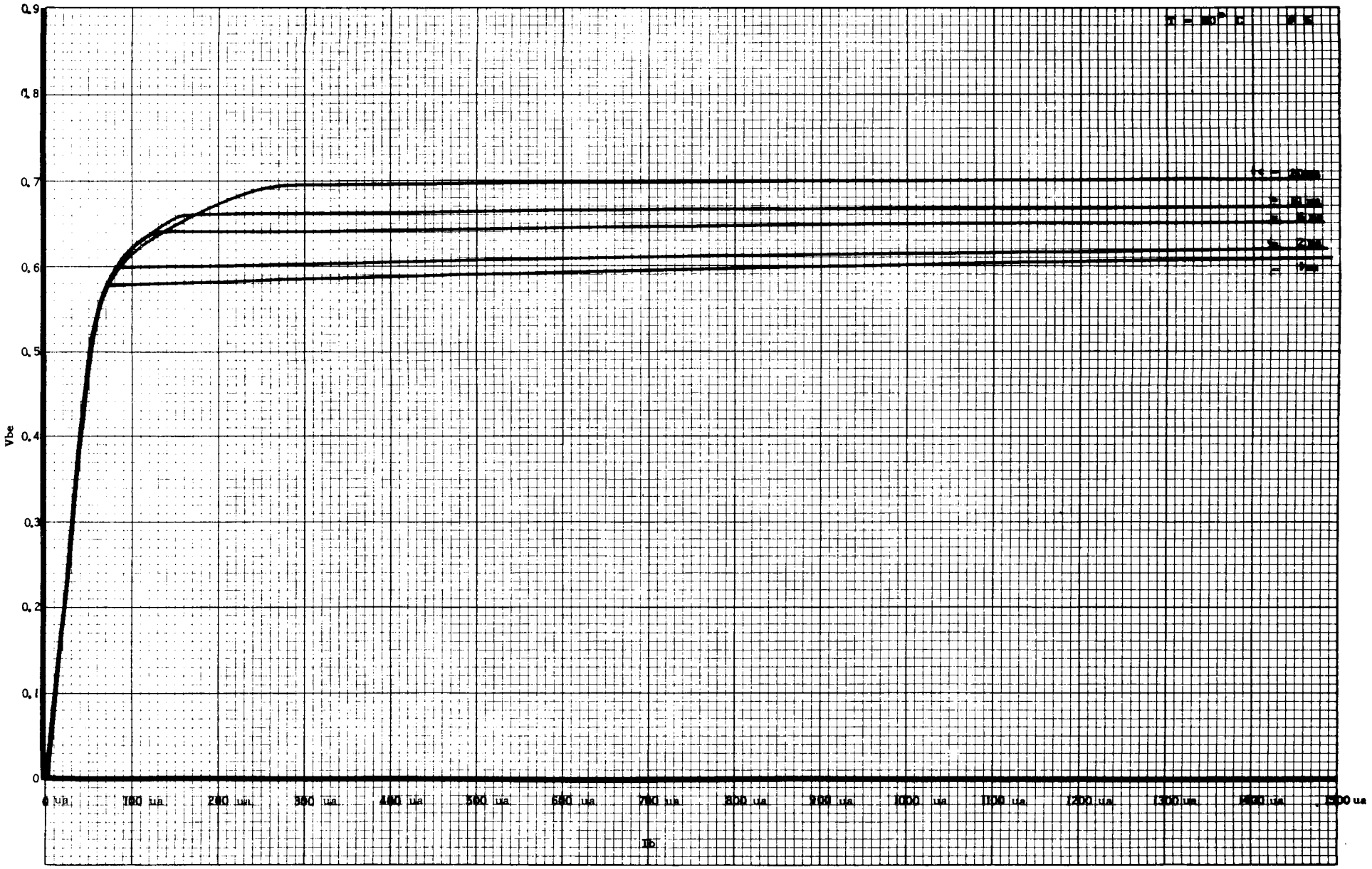
1000 ua
1100 ua
1200 ua
1300 ua
1400 ua
1500 ua
Ib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300 ua
400 ua
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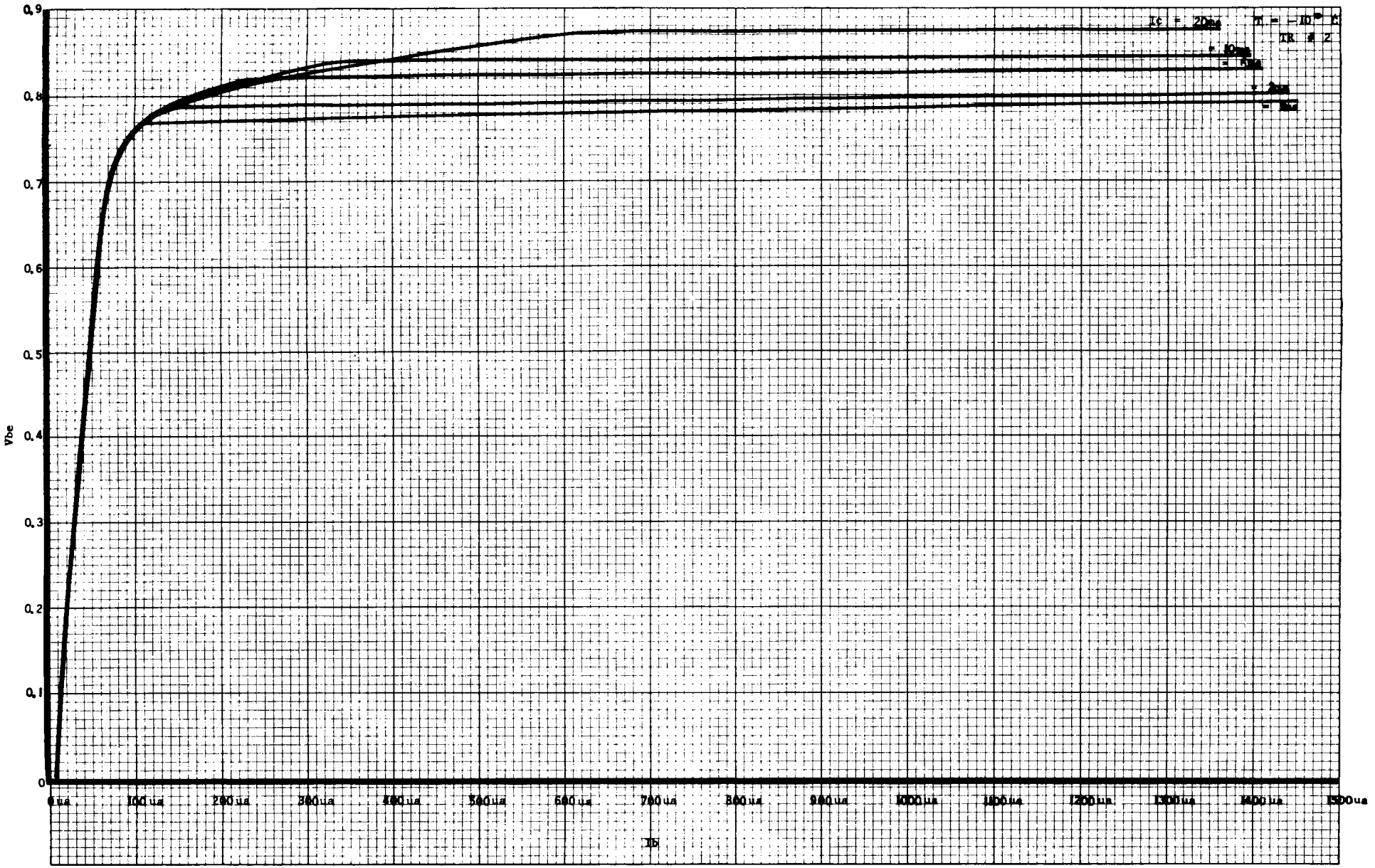
1000 ua
1100 ua
1200 ua
1300 ua
1400 ua
1500 ua
Ib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0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Vbe
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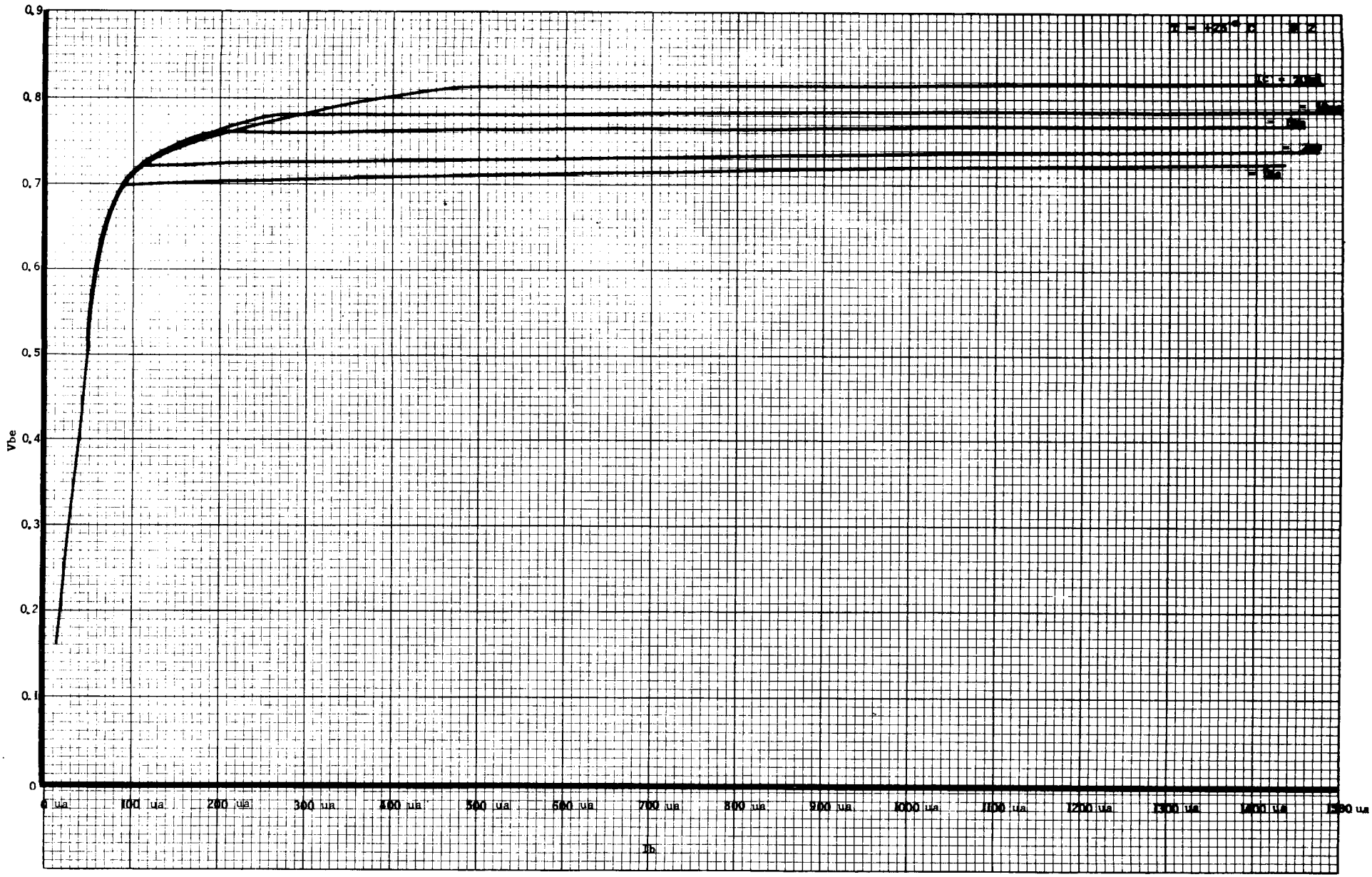
200ua
300ua
400ua
500ua
600ua
700ua
800ua
900ua
1000ua
1100ua
1200ua
1300ua
1400ua
1500ua
Ib


0.9
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0.6
0.5
0.4
0.3
0.2
0.1
0
Vbe
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400 ua
500 ua
600 ua
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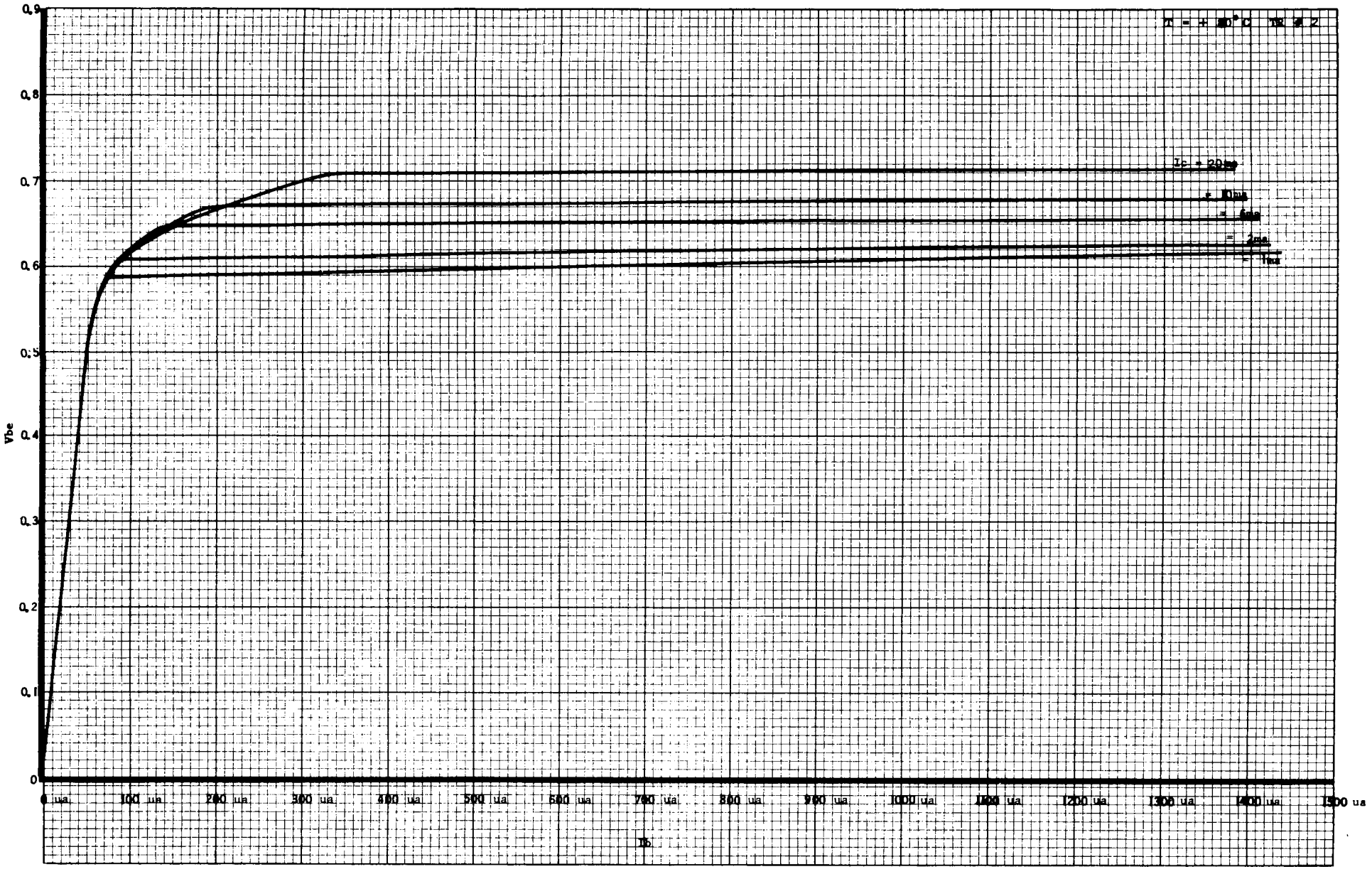
900 ua
1000 ua
1100 ua
1200 ua
1300 ua
1400 ua
1500 ua
Ib


Vbe
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0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0 ua
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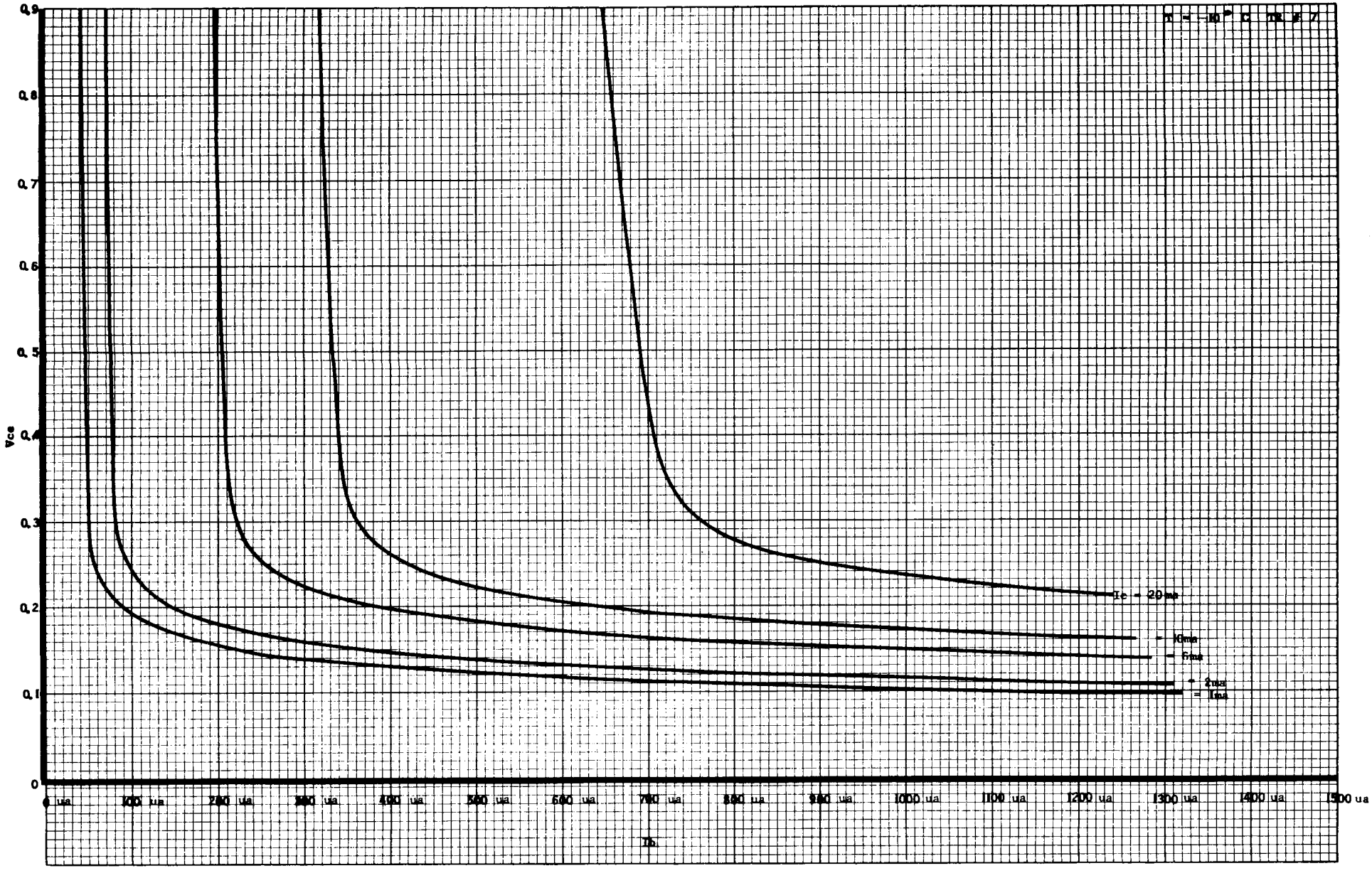
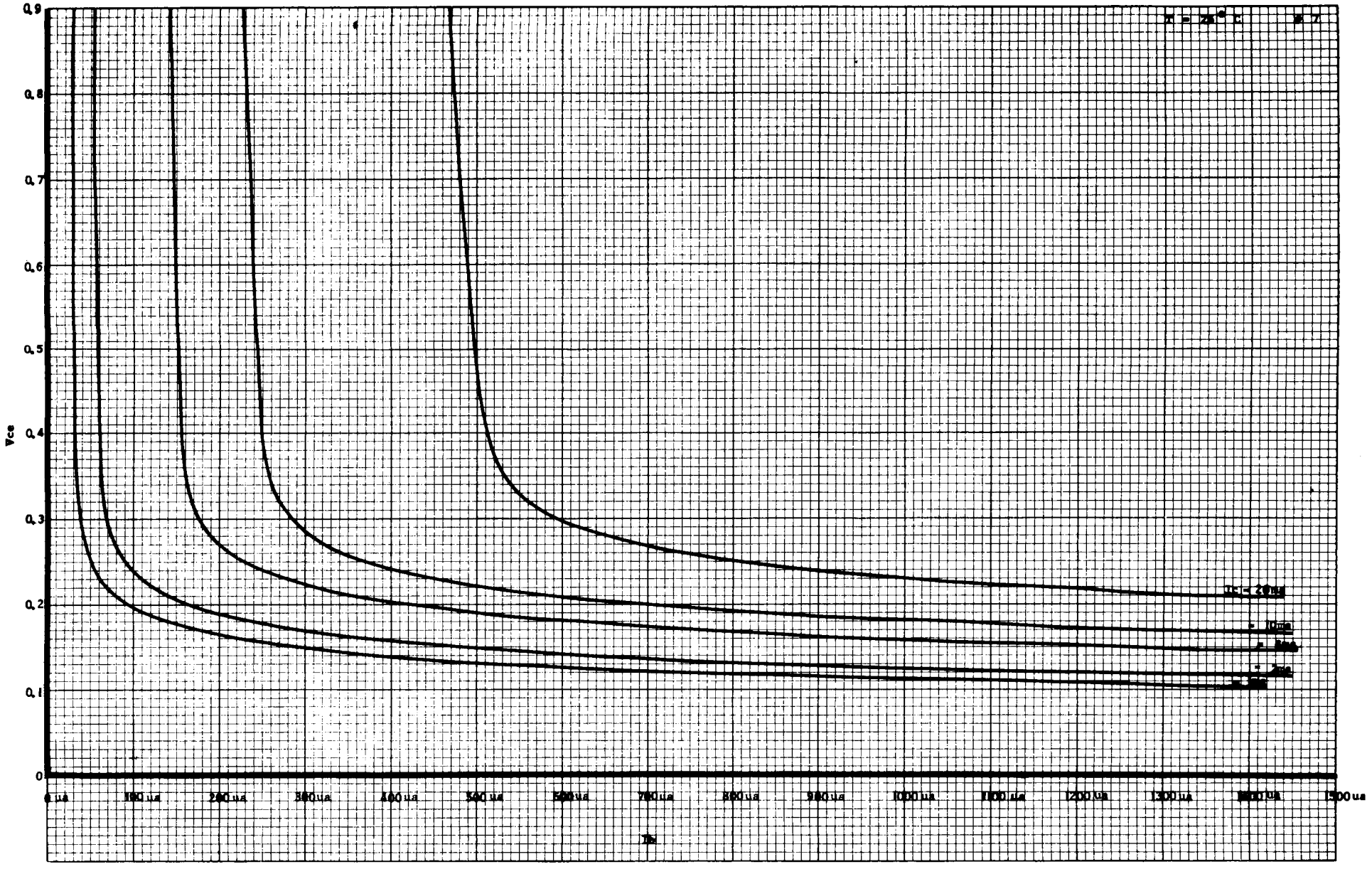
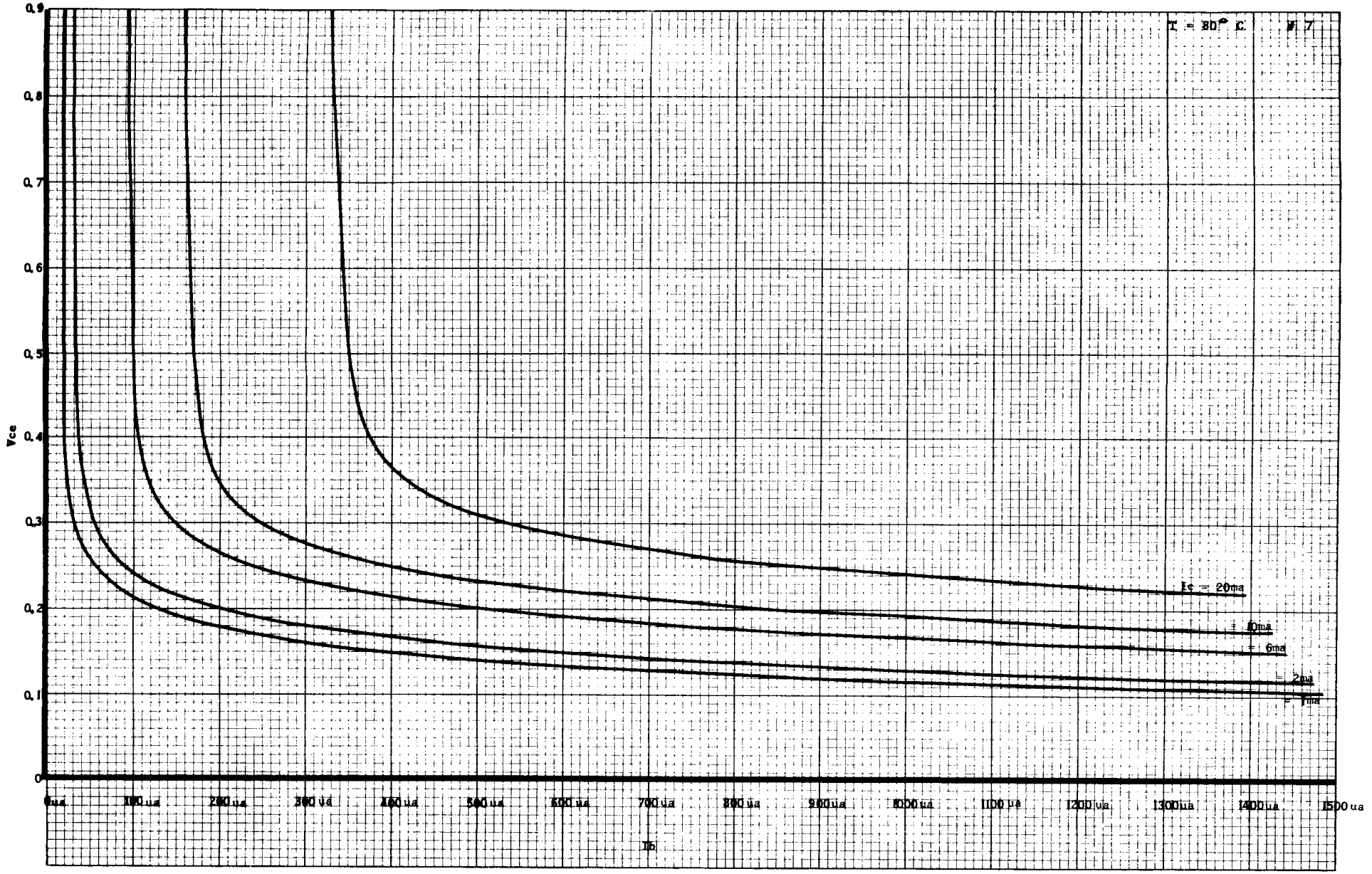
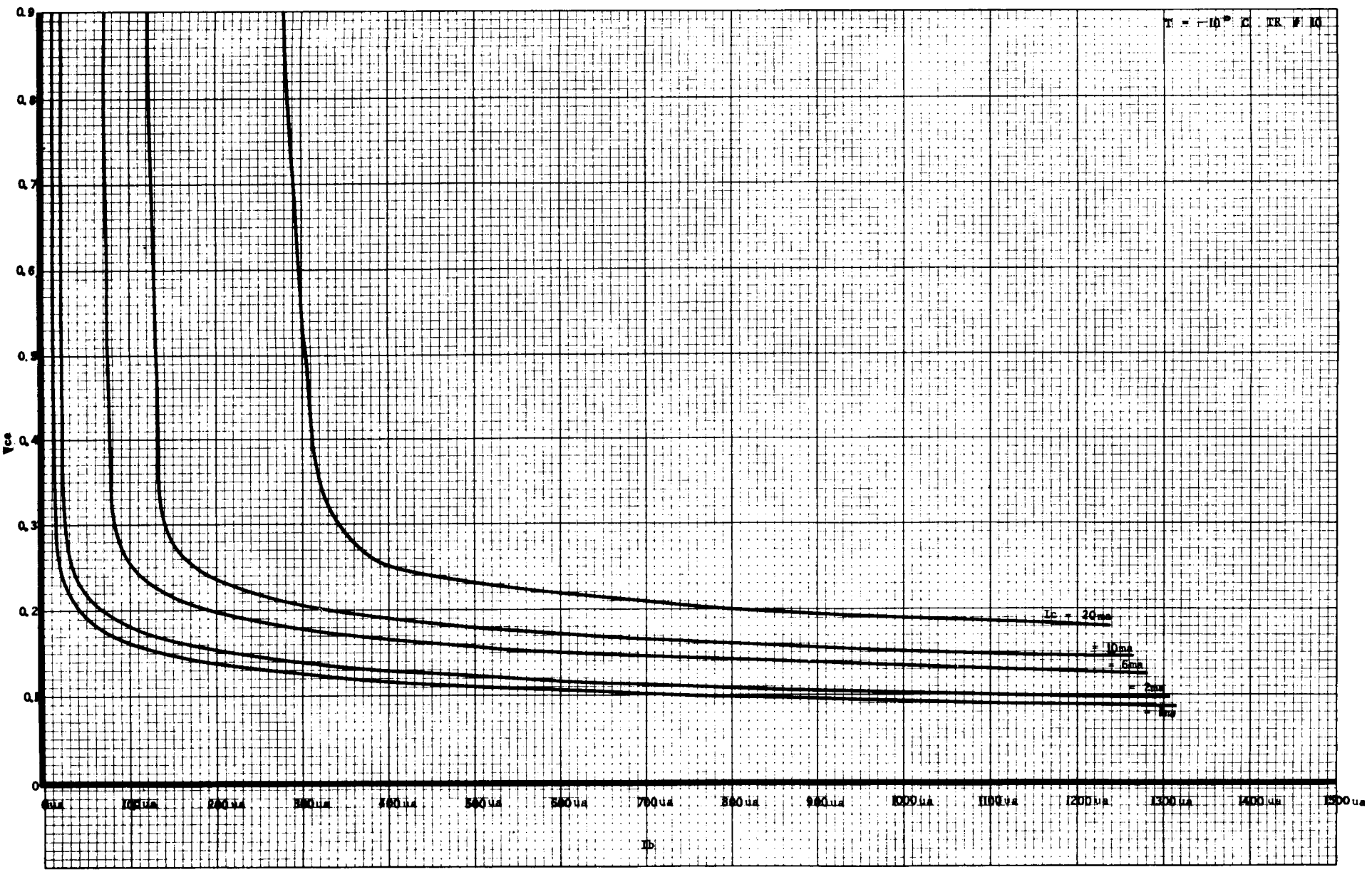
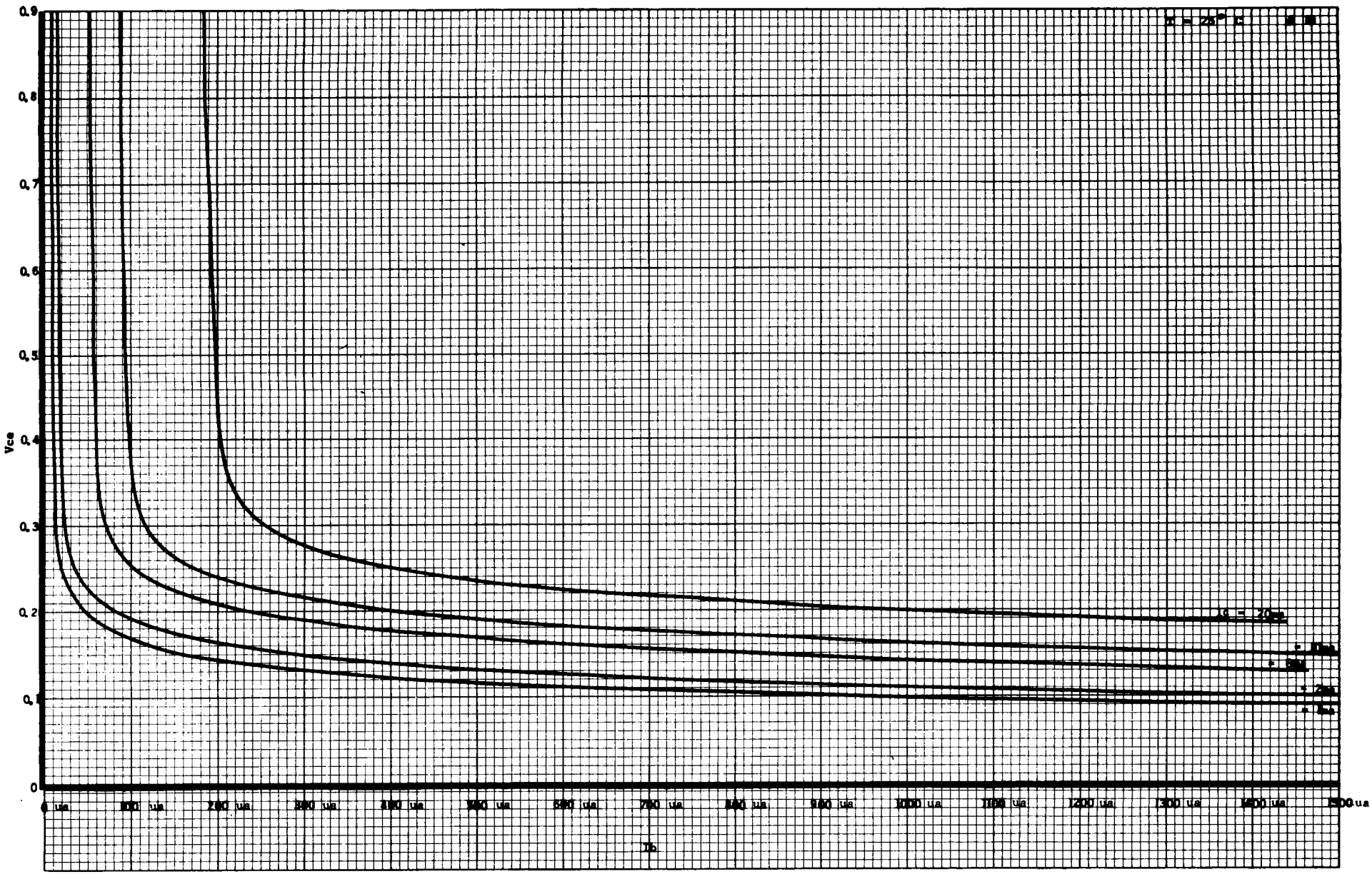
300 ua
400 ua
500 ua
600 ua
700 ua
800 ua
900 ua
1000 ua
1100 ua
1200 ua
1300 ua
1400 ua
1500 ua
Ib

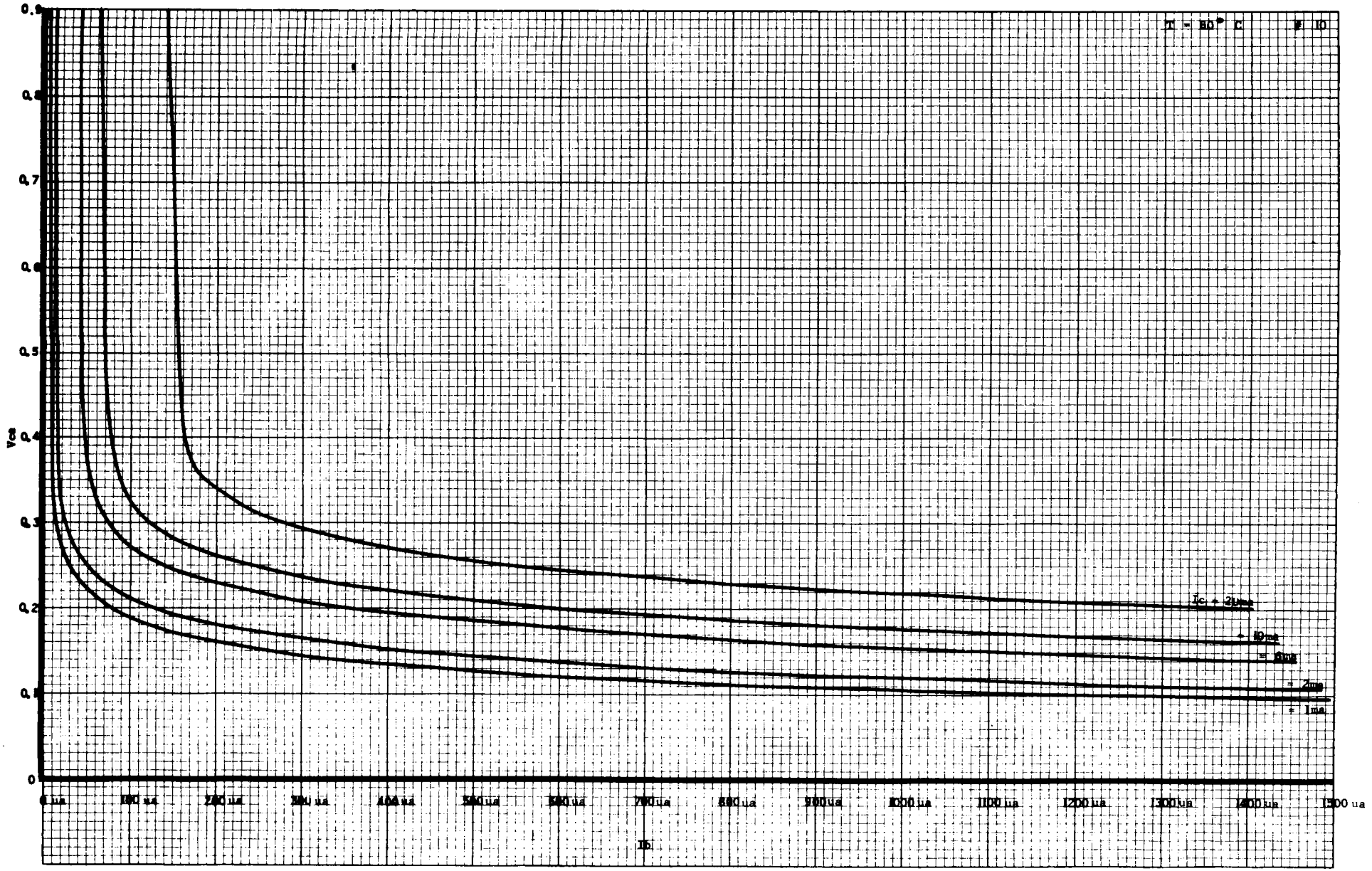

0.9
0.8
0.7
0.6
0.5
0.4
Vce
0.3
0.2
0.1
0
0 ua
100 ua
200 ua
300 ua
400 ua
500 ua
600 ua
700 ua
800 ua
900 ua
1000 ua
1100 ua
1200 ua
1300 ua
1400 ua
1500 ua
Ib
Ic = 20 ma
= 10ma
= 6ma
= 2ma
= 1ma


Vce
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0 ua
100 ua
200 ua
300 ua
400 ua
500 ua
600 ua
700 ua
800 ua
900 ua
1000 ua
1100 ua
1200 ua
1300 ua
1400 ua
1500 ua
Ib


T = 80° C.
Vce
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Ic = 20ma
= 10ma
= 6ma
= 2ma
= 1ma
0ua
100ua
200ua
300ua
400ua
500ua
600ua
700ua
800ua
900ua
1000ua
1100ua
1200ua
1300ua
1400ua
1500ua
Ib


T = -10° C TR F 10
Vce
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Ic = 20ma
= 10ma
= 6ma
= 2ma
= 0ma
700 us
1000 us
1100 us
1200 us
1300 us
1400 us
1500 us
Ib
k


0,9
0,8
0,7
0,6
0,5
0,4
0,3
0,2
0,1
0
Vce
0 ua
100 ua
200 ua
300 ua
400 ua
500 ua
600 ua
700 ua
800 ua
900 ua
1000 ua
1100 ua
1200 ua
1300 ua
1400 ua
1500 ua
Ib


Tc = 80° C
β 10
Vce
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Ic = 3ma
= 2ma
= 1ma
0 ua
100 ua
200 ua
300 ua
400 ua
500 ua
600 ua
700 ua
800 ua
900 ua
1000 ua
1100 ua
1200 ua
1300 ua
1400 ua
1500 ua
Ib

APPENDIX E

GENERAL TRANSIENT

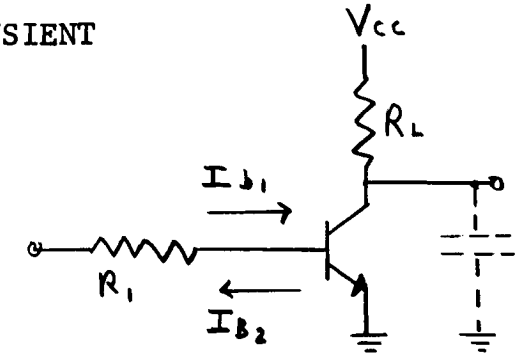


Figure 34

1. Turn ON Delay

Delay caused by:

1. Emitter and collector depletion layers are partially discharged. Emitter base was charged to $-V_{in}$; Collector base was charged $V_{cc} + V_{in}$.

a. A charge Q_E is supplied to the emitter junction capacitance $\longrightarrow f(V_{beo})$.

b. A charge Q_{cd} is supplied to the collector junction. This charge supplied, reduces the voltage across junction from $V_{cc} - (-V_{in})$ V_{cc}.

Total charge Q_{in} supplied to the transistor during delay time.

$$Q_{in} = Q_e + Q_{cd}$$

Assuming the input waveform is a current ramp driving the circuit in Figure 34, then

$$i = \frac{I_b}{t_r} t \quad \text{for } t_r \geq t > 0$$

$$Q_{in} = I_b \int_0^t \frac{t}{t_r} \, dt = \frac{I_b \, t^2}{2 \, t_r}$$

The output delay time may be either less than or greater than the input rise time.

For $t_{dr} \quad t_{ri}$

$$Q_{in} = \frac{I_b \, t^2}{2 \, t_r} = Q_e + Q_{cd}$$

$$t_{dr} = \frac{2 \, t_r}{I_b} \, (Q_e + Q_{cd})^{\frac{1}{2}} \qquad \text{Equation 1}$$

For $t_{dr} \quad t_{ri}$

$$Q_{in} = I_b \int_0^{t_r} \frac{t}{t_r} \, dt + I_b \int_{t_{ri}}^{t} dt = \frac{I_b \, t_r}{2} + I_b \, (t - t_{ri})$$

$$= I_b \, (t - \frac{t_r}{2}) = Q_e + Q_{cd}$$

$$t_{dr} = \frac{Q_e + Q_{cd}}{I_b} + \frac{t_{ri}}{2} \qquad \text{Equation 2}$$

$$Q_e = \int_{V_{be\ off}}^{V_{be\ on}} C_{ib}(v) \, dv \qquad C_{ib}(v) = C_{IB} + K_e \, V^{-1/n}$$

For a diffused junction device

$$Q_e = 1.67 \, K_e \, (V_{be_{off}} + 0.7)^{0.6}$$

$$K_e = C_{ib} \ (\text{meas}) \ (V_{eb} \ (\text{meas}) + 0.7)^{0.4}$$

If V_{eb} (meas) and $V_{bc_{off}}$ of circuit are made the same, then

$$Q_e = 1.67\ C_{ib}\ (meas)\quad V_{be_{off}}$$

$$Q_c = \int_{V_{cb}}^{V_{be\ on}} C_{ob}\ (v)\ dv \qquad C_{ob}(v) = C_{OB} + K_e\ v^{-1/n}$$

The linear term C_{OB} must be considered if the transistor is epitaxial.

For epitaxial transistors

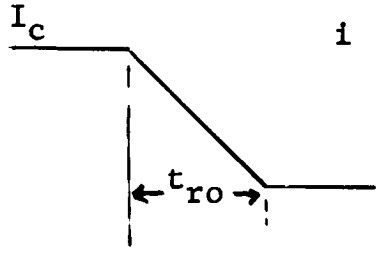
$$C_{ob}\ V_{cb} \leq Q_c \leq 1.67\ C_{ob}\ V_{cb}$$

$Q_c \approx 1.2\ C_{ob}\ V_{cb}$ if C_{ob} is measured near the point of operation

2. <u>Output Rise Time</u> (turn on time = t_r):

1. Collector swings from V_{cc} to V_{ce}
2. Stray output capacitance is discharged.
3. A charge Q_c is supplied to the collector junction during rise time
4. A charge Q_B is supplied to the base sufficient to switch the output current.
5. The collector time constant τ_c limits speed.

$$Q_{out}\ req. = \tfrac{1}{2}\ \Delta I_c\ t_{ro} + C_s\ V_{cc}$$



$$i = \int_0^{t_{ro}} \frac{\Delta I_c}{t_{ro}}\ t = \frac{I_c\ t^2}{2\ t_{ro}}\Bigg|_0^{t_{ro}} = \tfrac{1}{2}\Delta I_c\ t_{ro}$$

$$Q_{out} = \frac{i_c\ t}{2}$$

$$Q_B = \tau_c\ i_c$$

$$Q_B = \frac{2\ \tau_c\ Q_{out}}{t}$$

$$Q_{B\ available} = Q_{in} - Q_c$$

$$Q_{in} - Q_c = \frac{2\ \tau_c}{t}\ Q_{out\ available}$$

$$Q_{out\ available} = \frac{t}{2\ \tau_c}\ (Q_{in} - Q_c)$$

The time required then is that which satisfies

$$Q_{out\ available} = Q_{out\ req.}$$

$$\frac{t}{2\ \tau_c}\ (Q_{in} - Q_c) = \frac{I_c\ t}{2} + C_s\ V_{cc}$$

If we assume that Q_{in} is a constant current source, i.e., input signal instantaneously reaches a steady state, then $Q_{in} = I_b\ t$

$$\frac{t}{2\ \tau_c}\ (I_b\ t - Q_c) = \frac{I_c\ t}{2} + C_s\ V_{cc}$$

$$t = t_{ro} = \frac{Q_c + \tau_c\ I_c}{2\ I_b} + \sqrt{\left(\frac{Q_c + \tau_c\ I_c}{2\ I_b}\right)^2 + \frac{2\tau_c\ C_s\ V_{cc}}{I_b}} \qquad \text{Eq. 3}$$

If there is no stray capacitance

$$t_{ro} = \frac{Q_c + \tau_c\ I_c}{I_b}$$

The previous equation is good only for forced beta $<$ 1/3 of normal beta. Also above did not include recombination. To include this term, let

$I_b = I_b - 0.5\ I_{bs}$ $\quad$ I_{b_s}: the base current just at saturation

$$t_r = \frac{Q_c + \tau_c I_c}{I_{b_1} - 0.5\ I_{bs}} = \frac{Q_c + Q_b}{I_{b_1} - 0.5\ I_{bs}} \qquad \text{Equation 4}$$

For a forced beta of greater than one-third of transistor beta

$$t_r = \left[\frac{\tau_a + h_{FE}\ R_L\ Q_c}{V_{cc}}\right] \ln \frac{I_{b1}}{I_{b1} - I_{b_s}} \qquad \text{Equation 5}$$

REFERENCE 2

3. Storage Time (t_s)

During storage time, the stored charges in the base and collector regions are removed.

For planar epitaxial transistors, the following equations have proven most valid:

$$t_s = \tau_s \ln \left(\frac{I_{b1} + I_{B2}}{I_{b_s} + I_{B2}}\right) \qquad \text{Equation 6}$$

REFERENCE 1

Valid for $I_{B_2} < 2\ I_{b_1}$

For conditions $I_{B_2} > 2\ I_{b_1}$

$$t_s = \frac{\tau_s}{0.69} \ln \frac{I_{b1} + I_{B2}}{I_{b_s} + I_{B2}} \qquad \text{Equation 7}$$

4. Turn Off (t_f):

Turn off in a function of

a. Q_b = active base charge

b. Q_c = collector depletion region charge

c. I_{B_2} = pull out current

d. I_{b_s} = saturation current

$$t_f = \frac{Q_b + Q_c}{I_{B2} + 0.5\ I_{bs}}$$ Equation 8

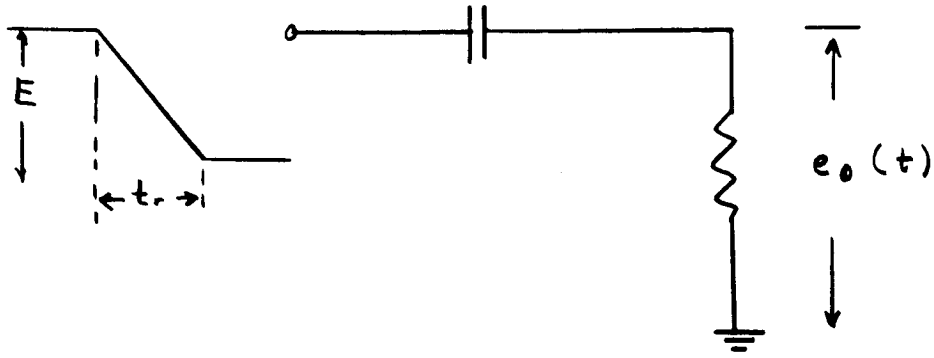
valid for $I_{B2} \leq 0.1\ I_c$

$$t_f = \left[\frac{\tau_a + h_{FE}\ R_L\ Q_c}{V_{cc}}\right] \ln \frac{I_{B2} + I_{bs}}{I_{B2}}$$

for $I_{B2} > 0.1\ I_c$

APPENDIX F

For the case of a series RC with a ramp applied, the following

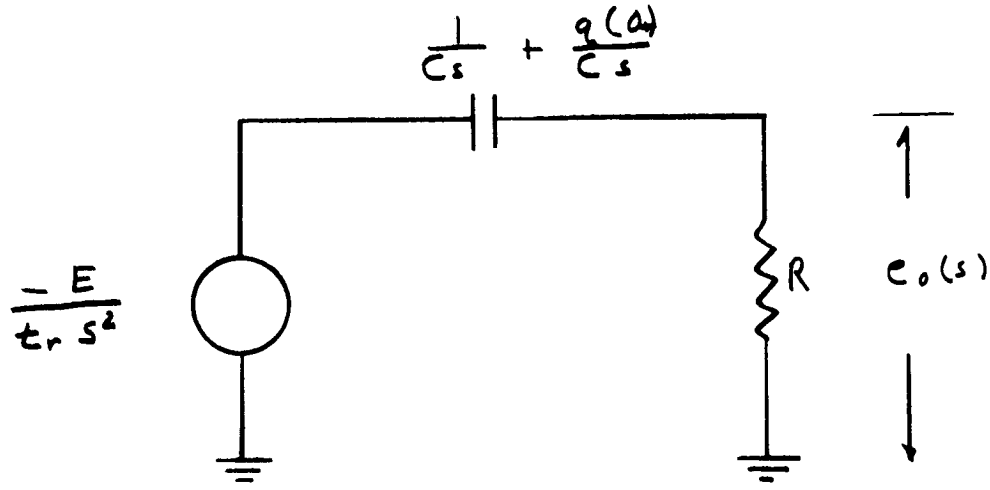


equations can be written.

(Note: The ramp approximation was made in order to guarantee a worst case solution. If an exponential was assumed, more triggering voltage is available)

$f(t) = -\frac{Et}{t_r}$ for $t_r \geqslant t > 0 \longrightarrow -\frac{E}{t_r s^2}$ in the Laplace domain

$f(t) = 0$ for $t > t_r$



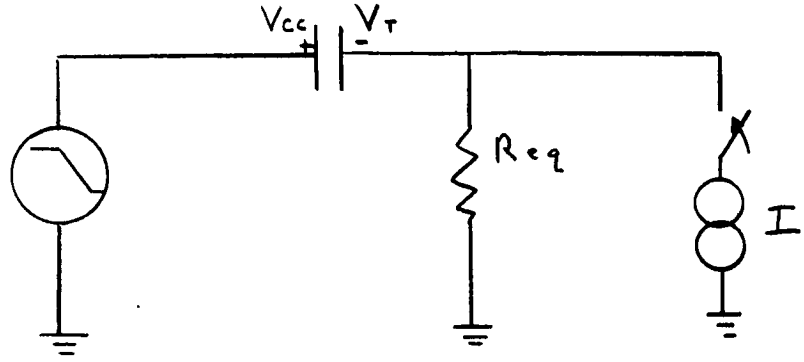
Assuming no initial change on capacitor

$$e_o(s) = -\frac{(E/trS^2)\,R}{R + 1/CS} = \frac{E}{t_r S\,(S + 1/RC)}$$

Therefore:

$$e(t) = -\frac{REC}{t_r}\,(1 - e^{-t/RC})$$

In the particular application where this equation finds use, an approximate equivalent circuit is given by



The voltage on the inside of the capacitor is a function of the A.C. current through R_{eq}, and I which is either/or the D.C. base current and steering current.

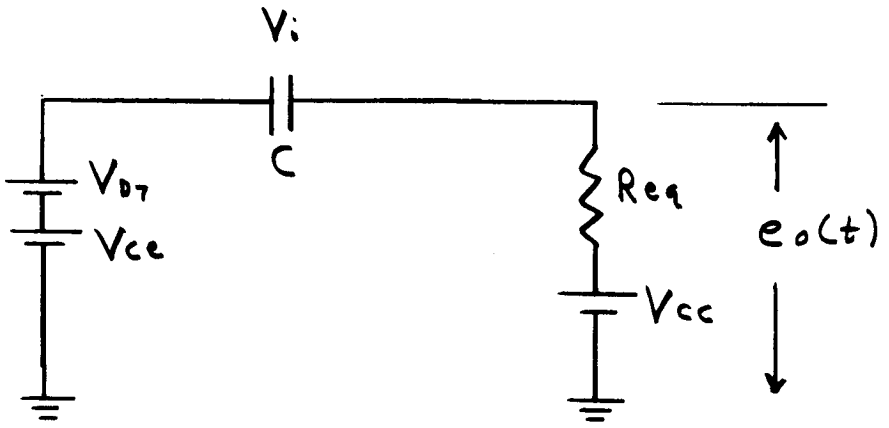
The voltage on the inside of the capacitor is then given by

$$e(t) = f\,(A.C.\ voltage) + f\,(D.C.\ voltage)$$

$$= -\frac{REC}{t_r}\,(1 - e^{-t/RC}) + \frac{I_t}{C} \qquad \text{Equation 10}$$

$$\text{for } t_r \gg t > 0$$

After the input edge has passed, the equivalent circuit is that of a series RC charging



$$e_o(t) = V_{tr} + (V_{cc} - V_{tr})\ (1 - e^{-t/RC}) \qquad \text{Equation 11}$$

V_{tr} = voltage on inside of capacitor at time t_r