APPENDIX G

PHASE NOISE INSTRUMENTATION

Submitted as part of the Final Report

for RF Test Console on JPL

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WESTINGHOUSE DEFENSE AND SPACE CENTER

SURFACE DIVISION

ADVANCED DEVELOPMENT ENGINEERING

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LIST OF ILLUSTRATIONS

1.0 Statement of Work

Paragraph (7) of the Statement of Work, Article 1 in [illegible] 36542, reads as follows:

> "Conduct experimentation to determine the most promising method of achieving short term stable frequency division".

The primary purpose of the frequency division is to make possible the accurate measurement of phase noise under conditions where the instantaneous phase deviation might be as great as four radians. The following paragraphs describe the experimentation conducted and the conclusions reached.

2.0 Experimental Work on Frequency Division

A block diagram showing the application of the frequency division is shown in figure 2.1. The 10 MC signal containing phase noise with instantaneous deviation up 4 radians is compared in a phase detector with a noise free 10 MC signal from the reference oscillator. Since the linear range of operation of a phase detector is inherently limited to approximately one radian, frequency division must be accomplished to prevent the noise from exceeding the linear range of the phase detector. Division by a factor of 2, 4, or 8 is desired. The stability of the frequency dividers should be such that negligible error is introduced into the final measurement.

2.1 Methods of Accomplishing Frequency Division

Two methods of frequency division were considered as suitable for this application:

(1) Division by bistable multivibrators, and (2) Division by phase locked loop.

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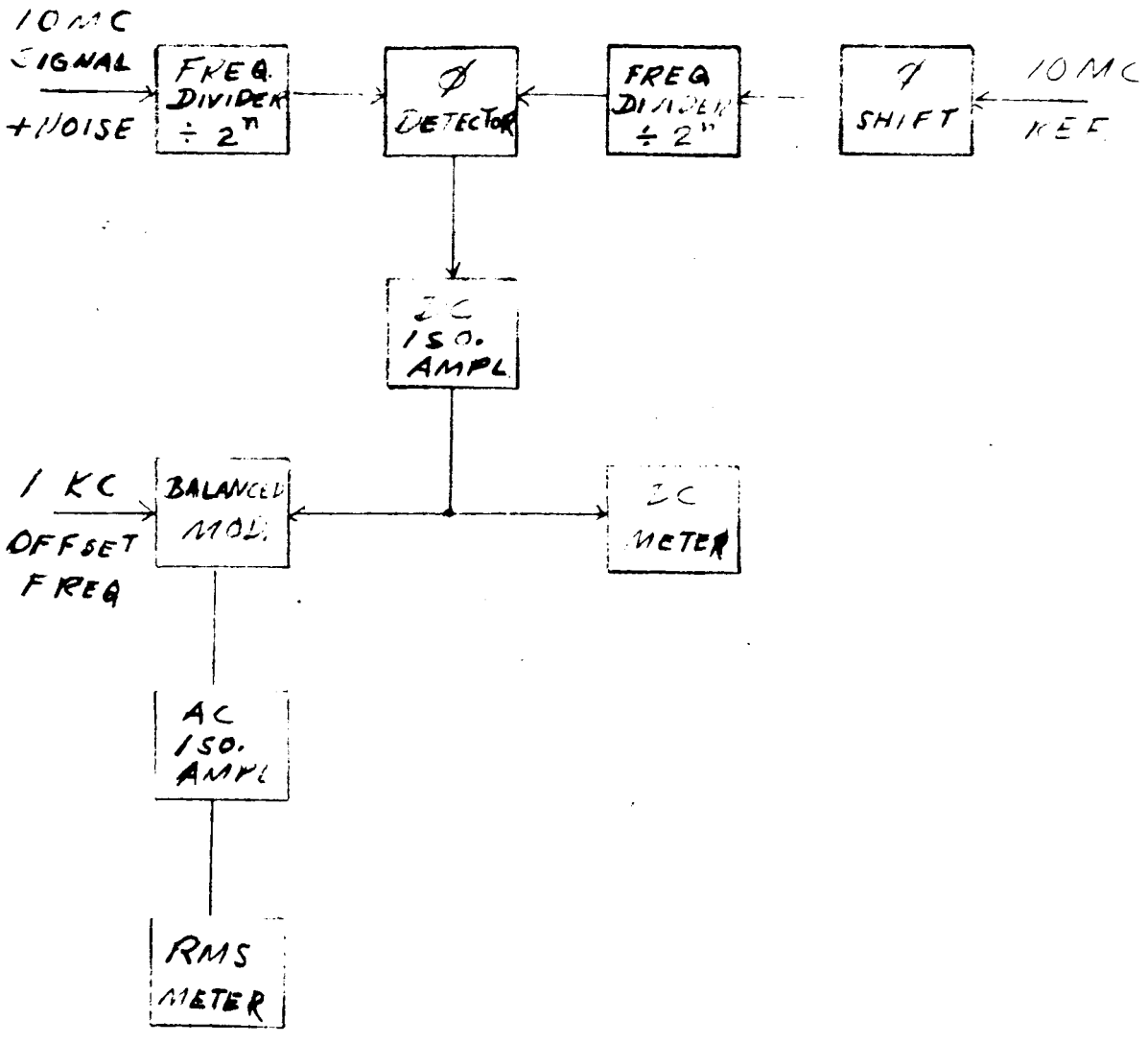

PHASE NOISE MEASUREMENT USING FREQUENCY DIVIDERS

FIG. 2.1

The bistable multivibrators method is shown in block form in figure 2.2. A squaring amplifier is used to provide a suitable drive to a series of bistable multivibrators which are connected in one of several configurations which will accomplish binary division. The outputs from this method are square waves at the desired frequencies.

A block diagram showing a method of division by phase locked loop is shown in figure 2.3. In this method, a voltage controlled oscillator is used to produce the desired frequency. The oscillator is phase locked to the input signal by comparison in a phase detector of the multiplied output of the VCO, the filtered output of the phase detector controlling the frequency of the VCO. Division factor can be changed by shifting from the VCO to the appropriate multiplier output.

Experimentation to determine which of the two methods is most promising is described in the following paragraphs.

2. Experimentation of Division Using Bistable Multivibrators

As seen in figure 1, two identical frequency dividers are used, one in the reference path and one in the signal path. Therefore, the problem in this case was to determine the relative jitter between two identical binary dividers dividing by 2, 4, or 8 from 10 MC. The only type logic readily available for this experimentation was the Solomon breadboard logic, capable of 10 MC operation and having rise times in the order of 10 n sec.

Two identical binary divider circuits were connected as shown in figure 2.4. Gates were used in interconnecting the flip-flops to

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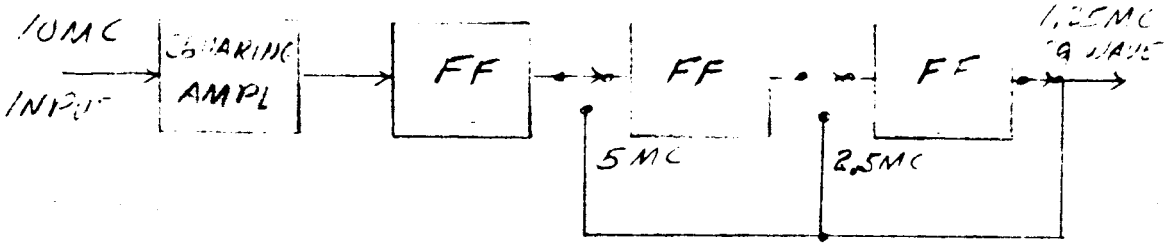
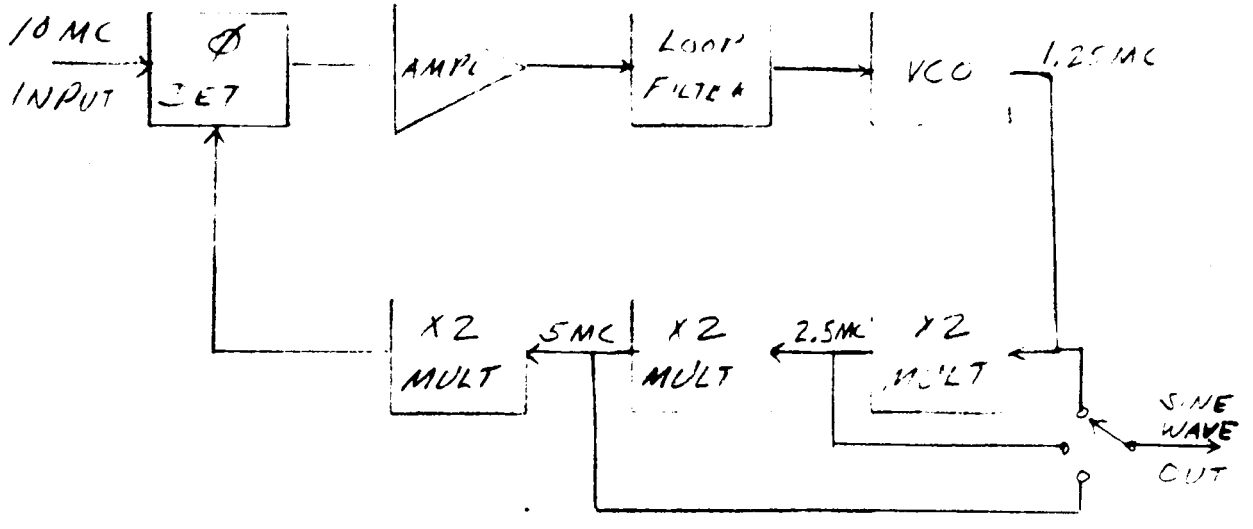


FREQUENCY DIVISION WITH BISTABLE MULTIVIBRATOR.

FIG 2.2



FREQUENCY DIVISION WITH PHASE LOCKED LOOP

FIG. 2.3

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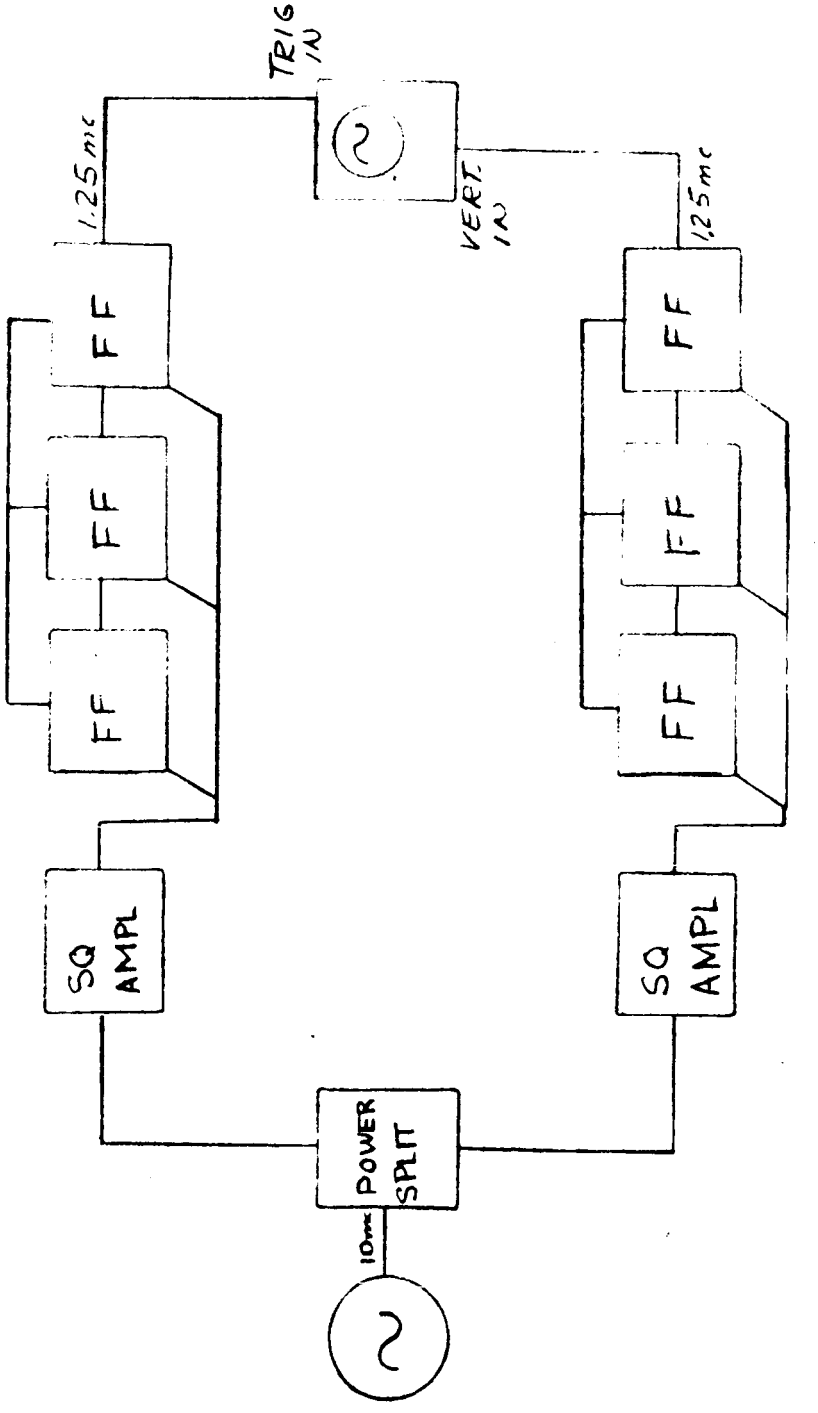

JITTER MEASUREMENT
FIG. 2.4

produce a grey code counter configuration, the most desirable method of dividing by 8 since only one flip-flop changes state at a time. In order to determine the relative jitter between the two dividers, the output of one was applied to the vertical input to a Tektronix 521 scope, while the output of the other was applied to the trigger. As shown in the photographs in figure 2.5, no jitter could be observed. For comparison purposes, the upper view in each photograph was made with the scope synchronized internally. If the resolution of the scope is taken as 1/10 of the smallest division (.2 cm), The maximum jitter which would not be detectable is .1 x .2 x 10 n sec/cm = 0.2 nanoseconds. This figure includes any jitter in the scope trigger circuits as well as the sum of the jitter in the two binary circuits.

It was noted that the fall time of the flip-flop output is approximately 10 nanoseconds, but the rise time is in excess of 50 nanoseconds. This results in asymetry which would certainly show up as a reduction in the linearity when used to drive a digital phase detector.

As a further check, the outputs of the two dividers were connected to an elementary digital phase detector as shown in Figure 2.6. The digital phase detector is shown in Figure 2.7. Use of this type phase detector is desirable if the rise and fall times of the flip-flop outputs can be made equal and sufficiently fast. The output of the digital phase detector was examined carefully for evidence of 60 cycle ripple; none was observed. Since the sensitivity of the phase detector was 1 mv/degree, and the maximum sensitivity of the scope 50 mv/cm, the 60 cycles in order to be unobserved must have been less than $\frac{.1 \times .2 \times 50}{8}$

65-5[illegible]

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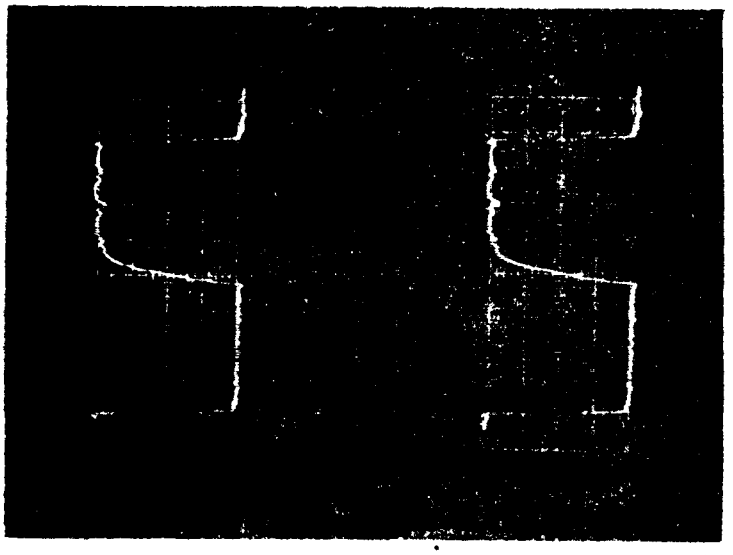

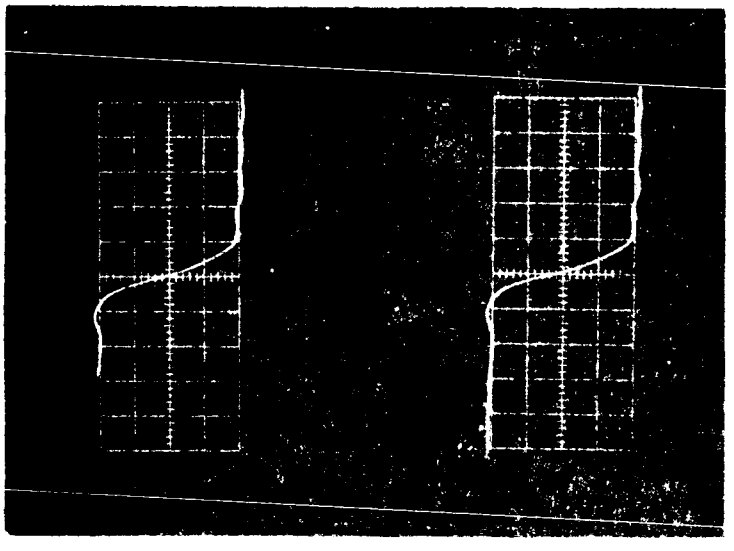

@ 100 nanosec/cm

@ 10 nanosec/cm

BINARY DIVIDER OUTPUT WAVEFORMS

FIG. 2.5

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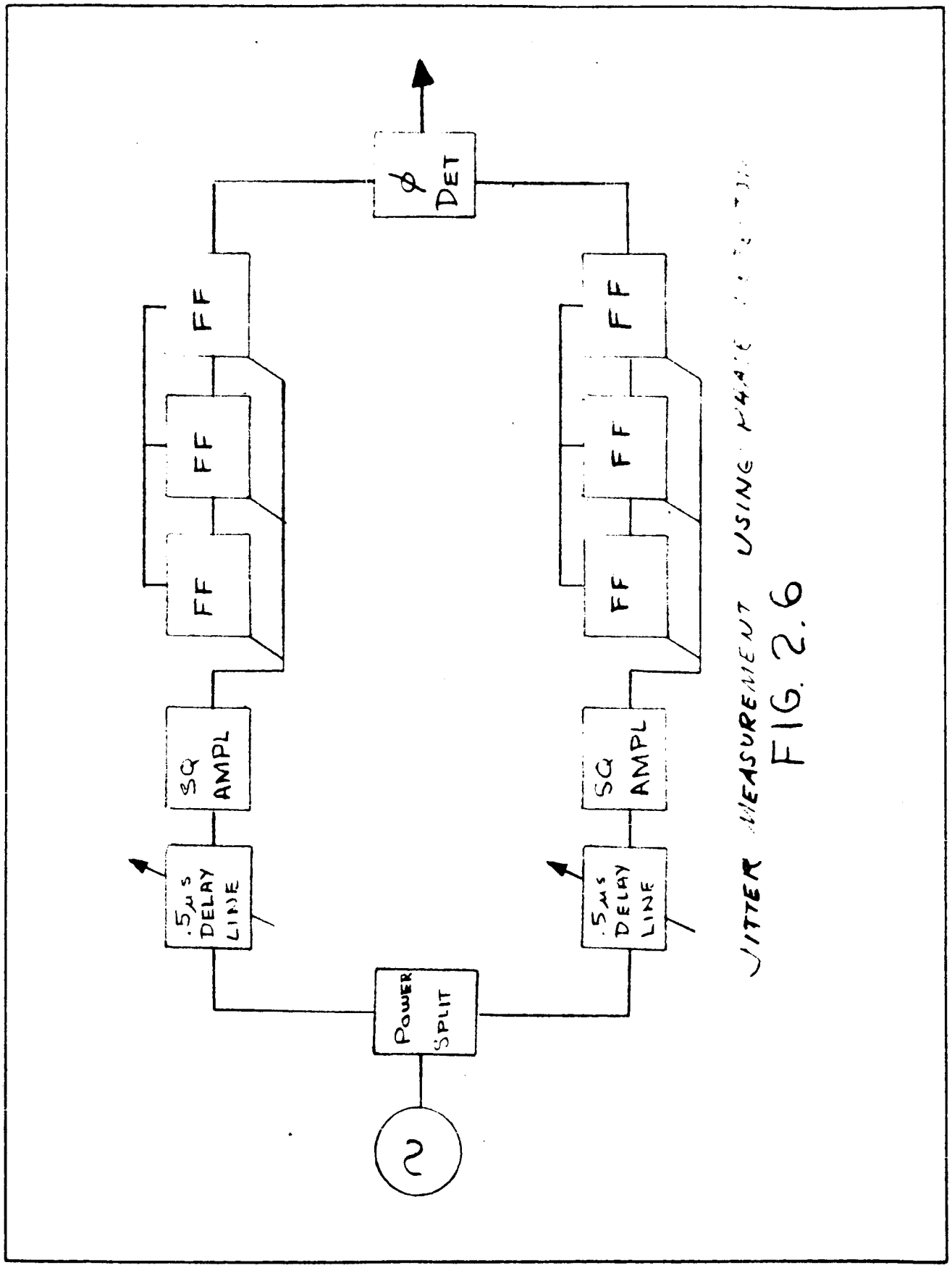

JITTER MEASUREMENT USING [illegible]

FIG. 2.6

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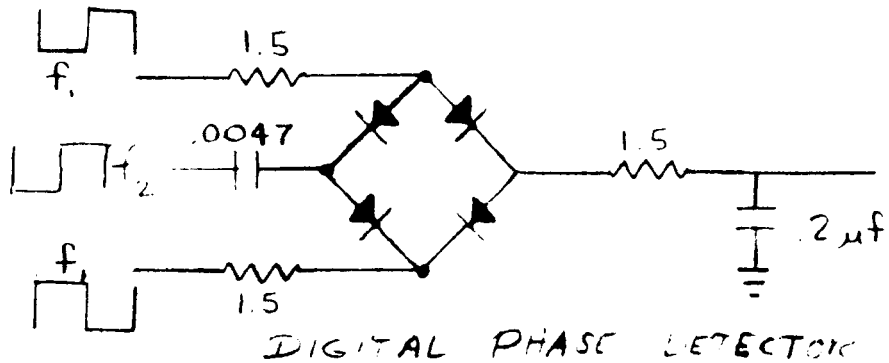
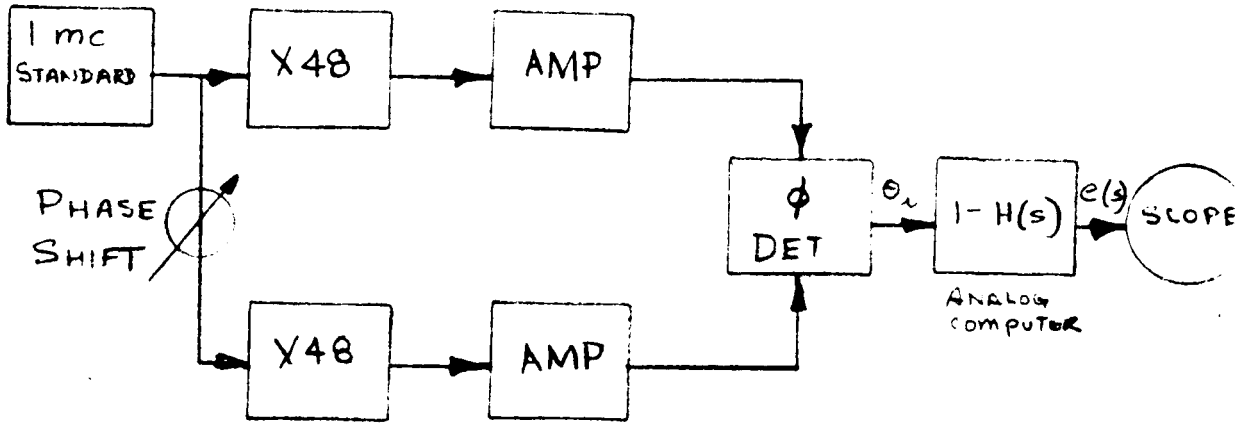


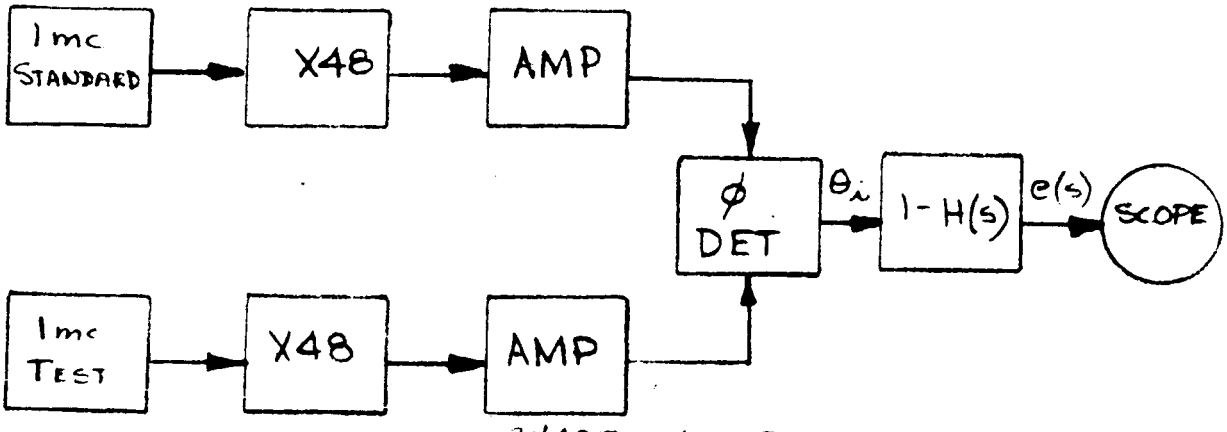
DIGITAL PHASE DETECTOR

FIG 2.7



INTERNAL PHASE NOISE MEASUREMENT

FIG. 2.8



OSCILLATOR PHASE NOISE MEASUREMENT

FIG. 2.9

approximately .125 degrees at 1.25 MC or .2 nanoseconds.

Difficulty was encountered in attempting to check the linearity of the phase detector. Movement of the wiper arm of the variable delay lines used as phase shifters invariably resulted in erratic counting action, causing jump in phase angle in 45° multiples. It is assumed, however, that the linearity of this circuit is degraded considerably by the asymetric output of the flip-flop.

2.3 Implementation of Division Using Phase Locked Loop

Upon examination of the circuitry required to accomplish frequency division using a phase locked loop (figure2.3), it was decided that the most likely sources of jitter would be the multipliers and the VCO. It was decided to determine, by experimentation with existing hardware of the type that would be used in a phase locked loop, what order magnitude of jitter would be introduced.

Two identical harmonic multiplier chains were available having a total multiplication factor of 48 (1 MC to 48 MC). These were arranged in the configuration shown in figure 2.9. The phase shifter was used to calibrate the phase detector in volts/radian, and the noise level or "grass level" as measured on the scope was an indication of the total phase noise introduced by the multipliers, amplifiers, and phase detectors. The phase noise in 2 BW_0 of 3 cps was measured as 0.7 degrees peak at 48 MC.

To get an indication of the noise which might be introduced by the VCO, the multipliers were driven by separate oscillators as shown in figure 2.9; both oscillators are precision standards, one

oscillator is arranged as a VCO. Following the same procedure, the noise was measured on the scope and found to be 1.43 degrees peak. It should be pointed out that "peak" is meaningless in a statistical sense; However, it is an indication of the order of magnitude of the noise level.

2.4 Comparison of Results of Experimentation

Difficulties are encountered in attempting to compare directly the results of experimentation of the two methods because of the different frequencies involved. The bistable multivibrator method was performed at the frequency required, 10 MC divided to 1.25 MC; the error was found to be too small to measure, and in any event smaller than .125 degrees at 1.25 MC. The experimentation with components similar to those which would be used in phase locked loop yielded a phase error of 1.43 degrees at 48 MC. To determine what the effect of this amount of noise on a phase locked loop whose output is 1 MC, it is necessary to divide the error by the multiplication factor involved. This yields an answer of $\frac{1.43}{48}$ = .03 degrees. This would represent .0375 degrees at 1.25 MC (.03 x $\frac{1.25\text{MC}}{1\text{MC}}$). This is based on the assumption that the jitter in the multipliers is directly proportional to the multiplication factor. It is likely, however, that the noise would be greater than .0375 since the same numbers of multiplier stages would be used. (The X43 multiplication consists of two X4 stages and one X3 stage). This figure is smaller than that obtained for the binary division; however, it is an actual measurement whereas the figure for the binary case is a maximum figure, since no noise was detected.

It is concluded that division by bistable multivibrators is the preferable method for the following reasons:

(1) Simplicity

(2) Economy

(3) Outputs are compatible with use of a digital phase detector, preferable for simplicity and linearity, and required by the specification. The sine wave outputs from the phase locked loop method require a squaring amplifier.

3.0 RF Test Console Instrumentation

The specific purpose of the phase noise instrumentation is to make accurate phase noise density function, variance, and spectrum measurements during FM system tests. A block diagram of the equipment for accomplishing these measurements, using a binary divider system of frequency division, is shown in figure 3.1. The following paragraphs describe the essential characteristics of the components which would be a part of the instrumentation.

3.1 Balanced Modulators

The balanced modulators will be identical to those used in the FM Receiver and described in that section of the report. Figure 3.2 is a schematic diagram of the basic circuit.

3.2 I.F. Amplifiers

The IF Amplifiers are identical to those used in the FM Receiver. Each amplifier will consist of three stages of the basic feedback pair circuit shown in schematic form in figure 3.3.

3.3 Phase Shifter

It is anticipated that a type R resolver made by Merrimac Research and Development Inc. will be used in this application. This model gives a continuous phase shift from 0 to 360° with an accuracy of ± 0.2 degrees. Insertion loss of 33 db is compensated by placing an IF amplifier immediately after the phase shifter.

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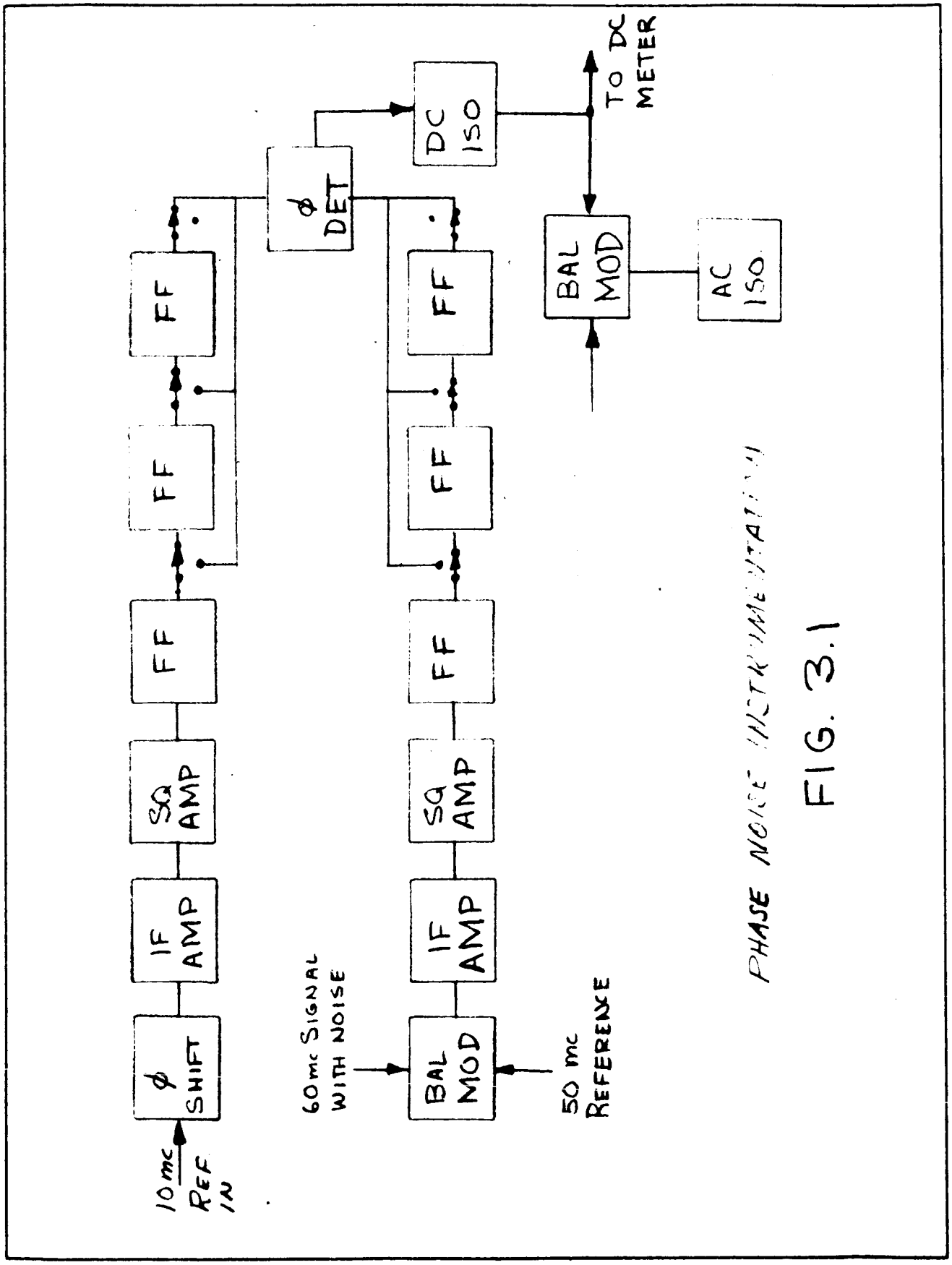

PHASE NOISE MEASUREMENT

FIG. 3.1

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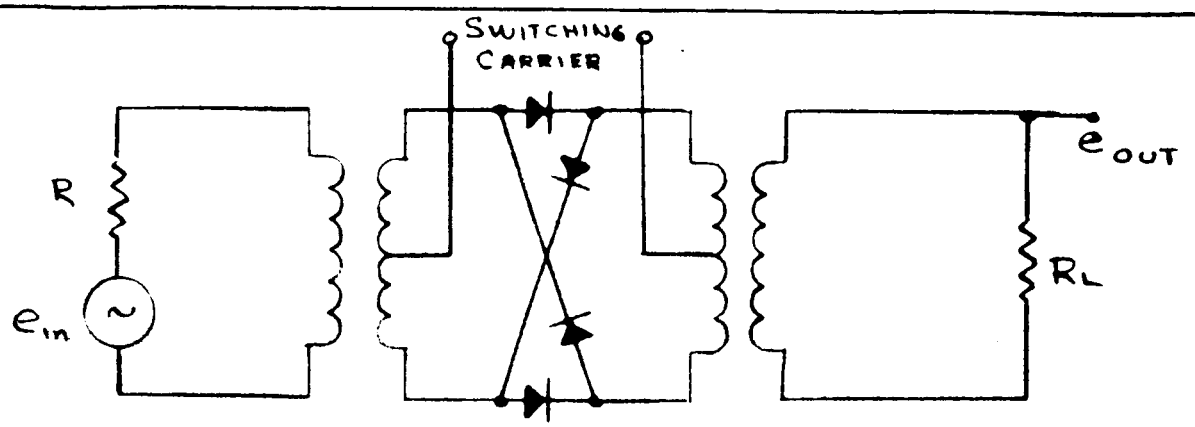

FIG. 3.2 BALANCED MIXER

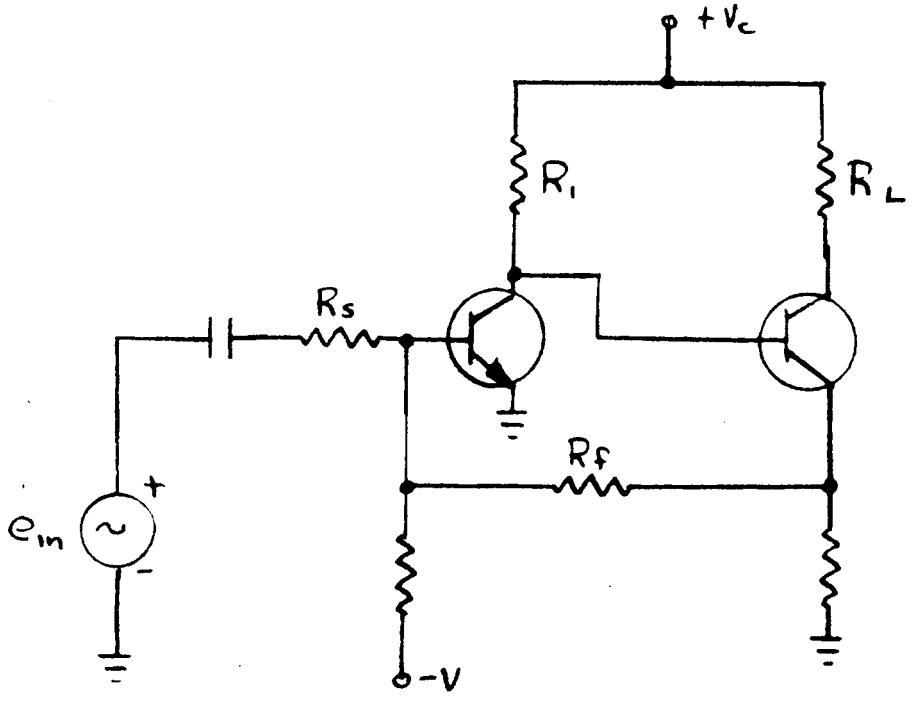

FIG. 3.3 FEEDBACK PAIR

3.4 Limiters

The limiters in this case will actually be high frequency squaring amplifiers. The best approach to this circuit appears to be a modification of a family of digital packages developed by Westinghouse to improve the delay and rise time. The present circuit has a delay of approximately 15 nanoseconds and a rise time of approximately 10 nanoseconds. It is felt that the use of transistors of higher power now available will result in an improvement sufficient to meet the specification of 5 nanoseconds delay and 4 nanoseconds rise time. Symmetry is presently acceptable.

3.5 Binary Dividers

The binary dividers will also be developed by modification of an existing bistable multivibrator. Experimentation has shown that the noise contributed by a binary divider system using circuits with rise times of approximately 10 nanoseconds would be negligible. Reduction of the rise time would result in a reduction of any noise. The microcircuit group has developed a family of packages constructed in thin film which can be operated as high as 50 MC. Modifications will be made to make these packages suitable for this application. The modifications to be made to the circuit will accomplish two things:

(1) Reduce the rise time to 4 nanoseconds

(2) Develop a symmetric output

3.6 Phase Detector

The phase detector will be digital, and will be similar to the phase detector used in the PM/FM transmitter. A schematic diagram of the basic circuit was shown in figure 2.7. This type phase detector has a response characteristics which is linear almost to $\pm$ 90°, the

principal limitation being; the rise time and symmetry of the square wave inputs.

3.7 Isolation Amplifiers

The DC isolation amplifier will be same are used in several other applications in the console, Philbrick type PP45L. The AC isolation amplifier will consist of two stages of the feedback pair similar to those used in the IF amplifiers.