GENERAL DYNAMICS | ELECTRONICS
SAN DIEGO OPERATIONS

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FINAL REPORT

INFRARED DETECTOR MICROELECTRONIC AMPLIFIERS

Submitted to

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1.0 MECHANICAL DESIGN

1.1 PREAMPLIFIER

Physical characteristics of the preamplifiers satisfied the requirements of JPL Statement of Work, SW 3478, as modified by JPL Interoffice Memorandum, A. Eisenman to D. LaPorte, dated 3 November 1964. Maximum body dimensions were 0.125 in. × 1.0 in. × 1.94 in., exclusive of header.

Details of the physical construction are contained in GD/E Drawings 3005603, 3005605, 3005606, and 3005607, which were previously delivered to JPL. Figure 1 shows the component layout conforming to GD/E Drawing 3005603. This layout was made for use with the Fairchild FET 2N3277 in the 0.125 in. × 0.250 in. flatpack case as shown in Figure 1. Preamplifiers Serial No. 1 through 6 were built according to this layout.

When the Siliconix 2N3578 on the 0.10 in. × 0.10 in. ceramic chip was substituted for the 2N3277, the layout was revised as shown in Figure 2 and on GD/E Drawing 3005603, revised 21 April 1965. Copies of the revised GD/E Drawing 3005603 and schematic diagram, GD/E Drawing No. 3005601, revised 21 April 1965 are included with this report. This layout was used for all amplifiers subsequent to Serial No. 6. Other changes made on this same revision were:

1) Addition of 82-pf ceramic capacitor C5
2) Elimination of 21.5 K ohm resistor R9
3) Substitution of microballoon filled epoxy resin, Type P-37A for polyurethane foam, Type CPR349-4, as the encapsulation material

The C5 and R9 changes became effective with preamplifiers, Serial No. 7 and on. The encapsulation change became effective with Serial No. 40 and on.

The two different encapsulants are visually distinguishable by their color; Type P-37A is blue, and Type CPR 349-4 is green. Type P-37A provides more uniform density with

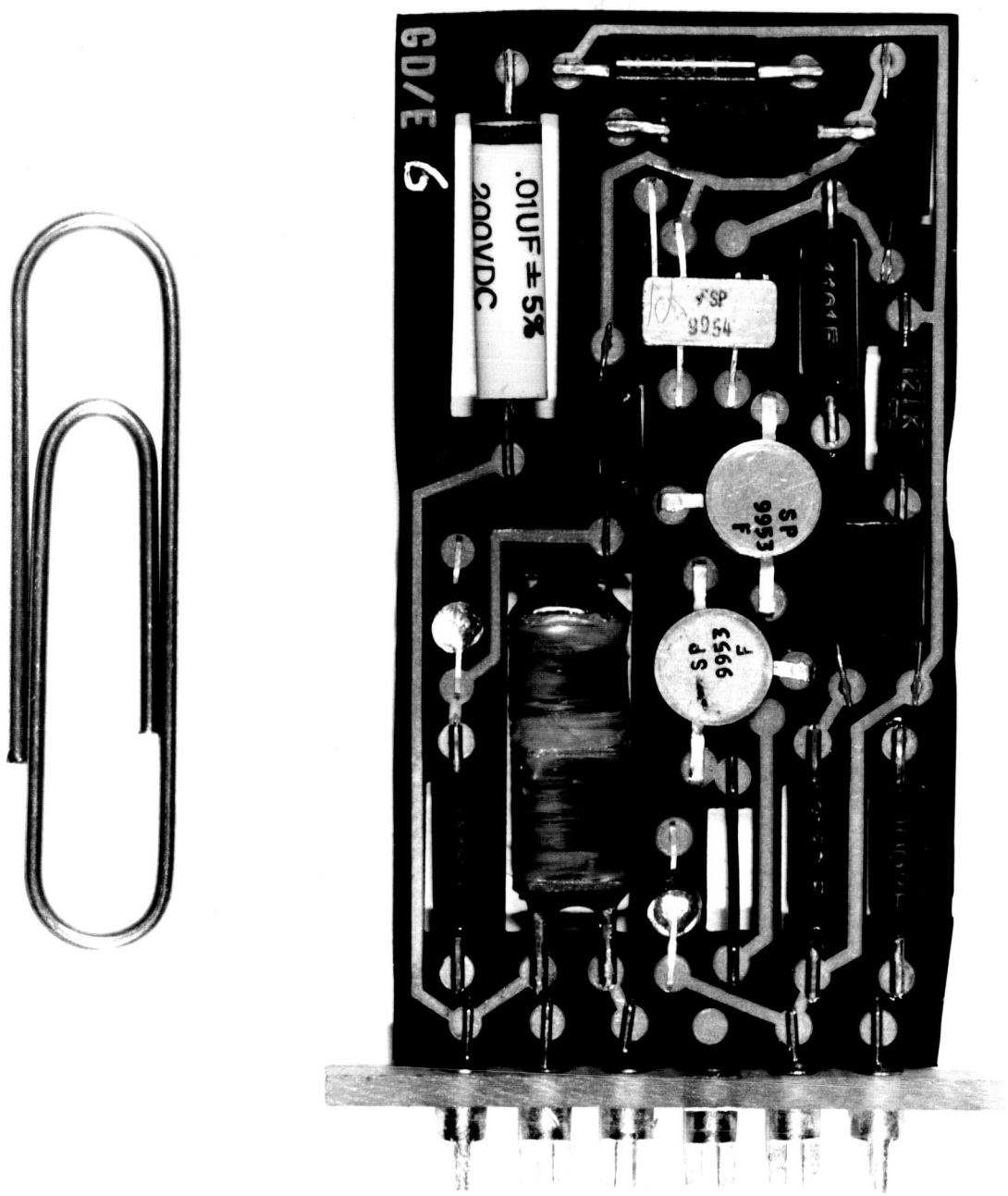


Figure 1. Component Layout Conforming to GD/E Drawing 3005603

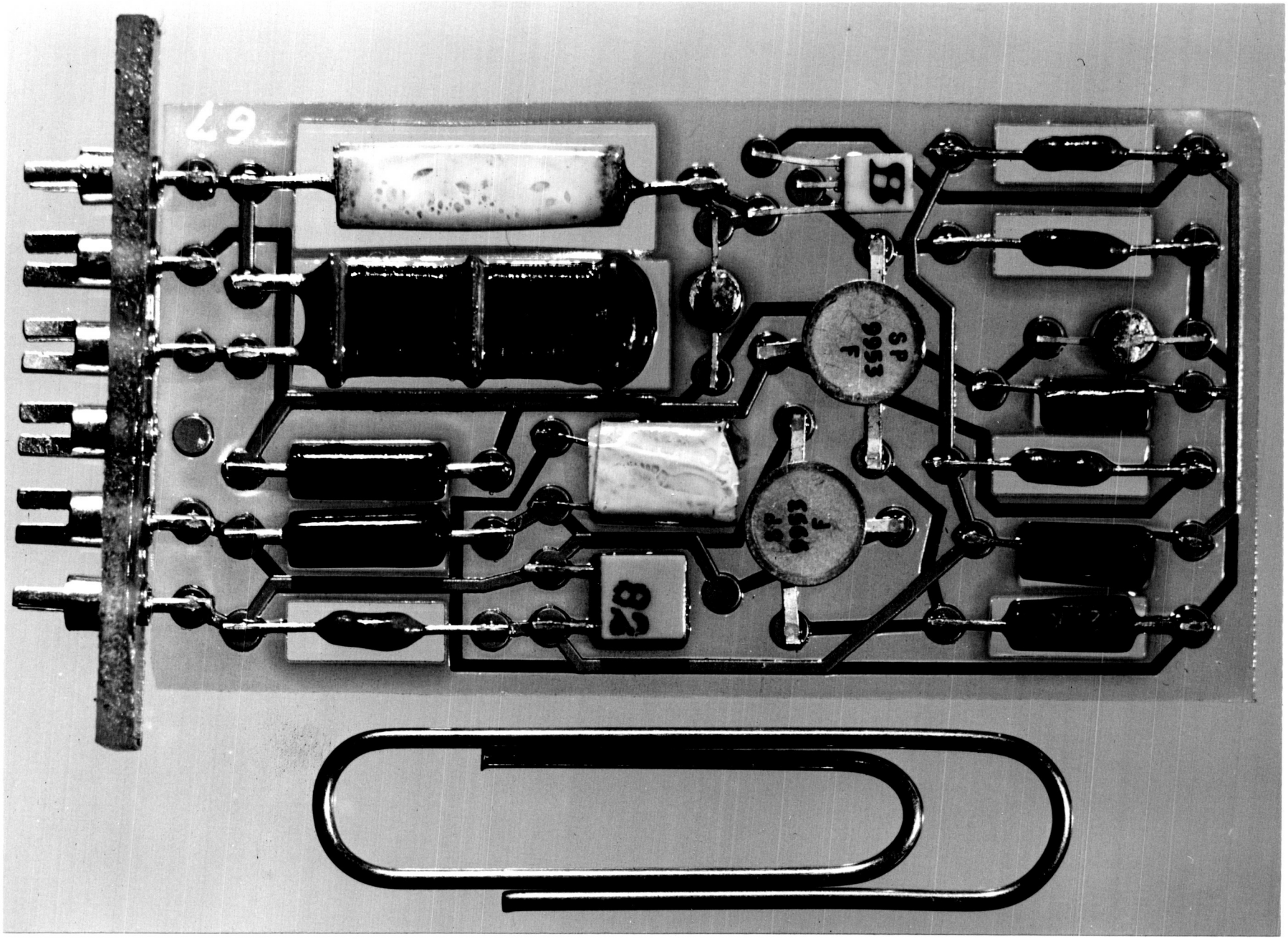


Figure 2. Component Layout Conforming to GD/E Drawing 3005603, Revised 21 April 1965

voids than Type CPR 349-4 foam polyurethane; however, both materials performed satisfactorily over the temperature range. No failures were experienced as a result of the thermal or mechanical properties of either.

On preamplifiers Serial No. 1 through 6, pin connections from terminals to the printed circuit board were made by soldering the pin into a hollow terminal. Subsequent amplifiers used one piece pin-terminal combination.

Total weight of a completed preamplifier (Figure 3) is 6.2 grams. It is distinguishable from the intermediate amplifier both by its color (gray) and by Part No. 3005603-1 stenciled on the thin edge (not visible in Figure 3).

1.2 INTERMEDIATE AMPLIFIER

Details of the physical construction of the intermediate amplifiers are contained in GD/E Drawings 3005602, 3005604, 3005605, and 3005607, which were previously delivered to JPL.

Figure 4 shows the component layout used for all intermediate amplifiers. Shown also are the three separate steps in the assembly process:

1) The weldable double-sided circuit board
2) The board with components installed
3) The encapsulated module with nickel electrostatic shield

Completing the module requires only a spray coat of insulating enamel (blue for the intermediate amplifier) and identification stencils.

Maximum body dimensions are the same as for the preamplifier, 0.125 in. × 1.0 in. × 1.94 in., exclusive of header. Type CPR 349-4 foam polyurethane was used for encapsulation of all intermediate amplifiers because these were all built before the changeover to microballoon Type P-37A epoxy resin.

Approximately half of all intermediate amplifiers made used solder pins in hollow terminals. The remainder used one piece pin-terminal combination.

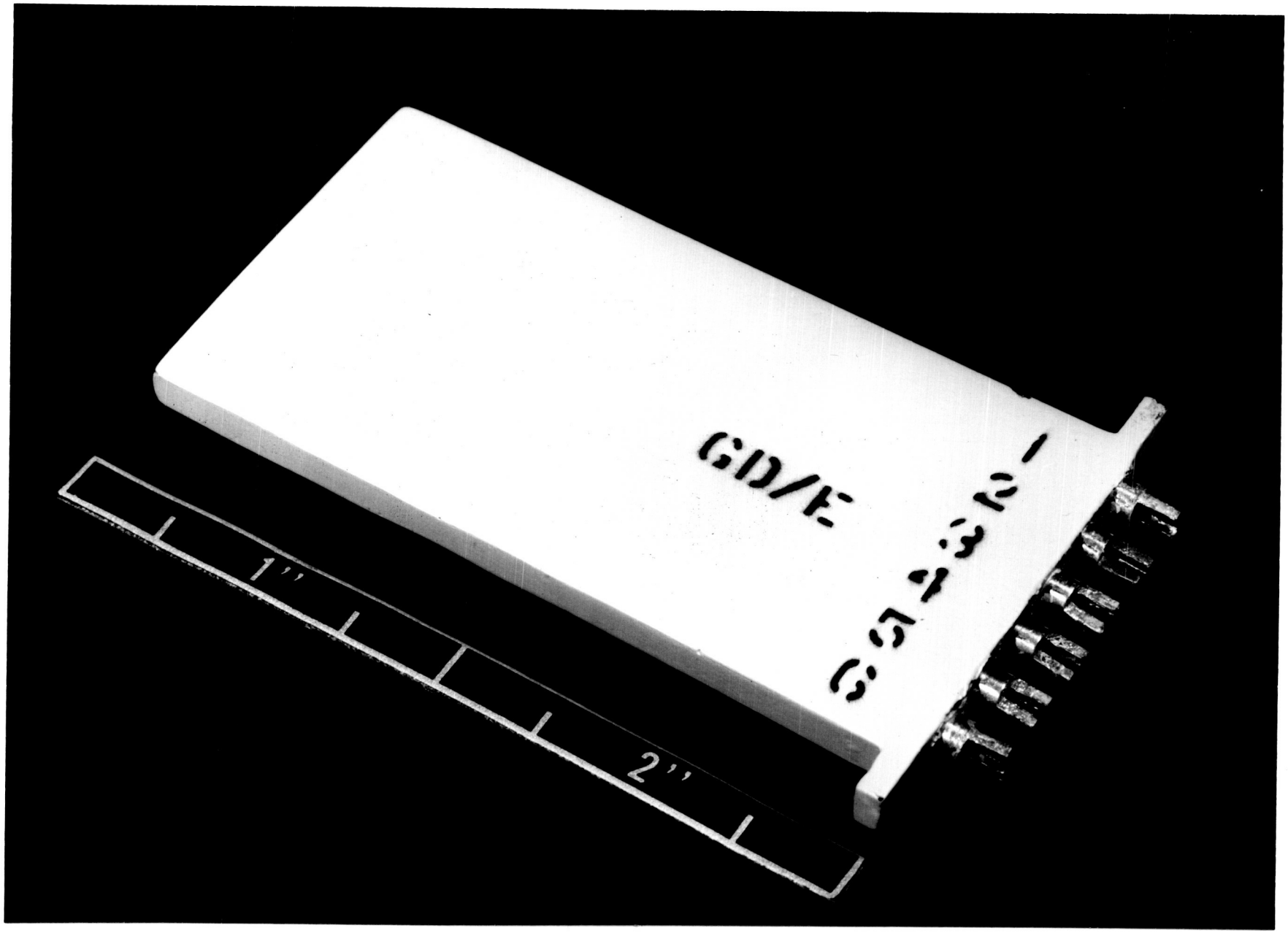


Figure 3. Completed Preamplifier

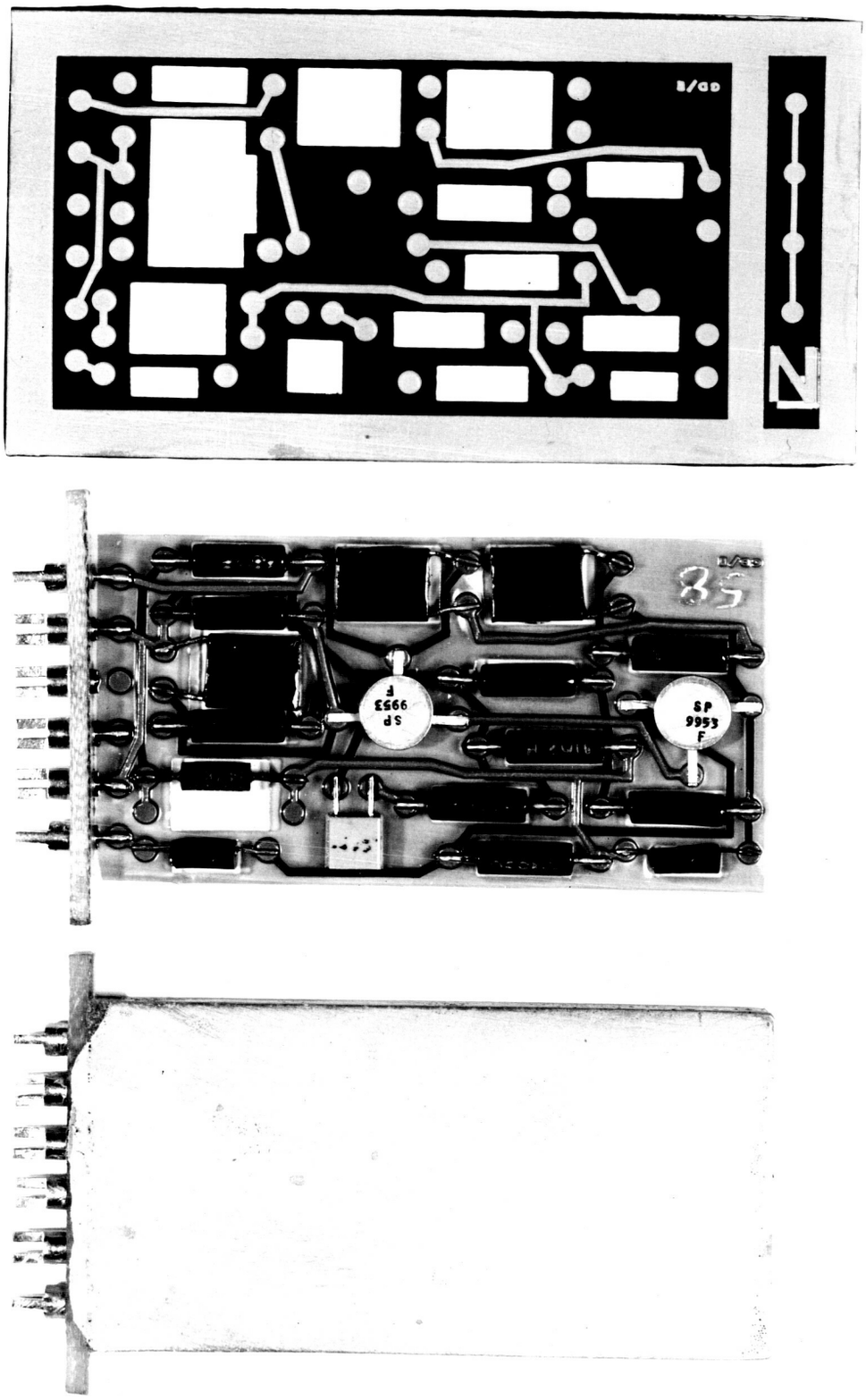


Figure 4. Component Layout of Intermediate Amplifier

2.0 COMPONENT SELECTION AND EVALUATION

2.1 PREAMPLIFIER

All components originally selected for the preamplifier proved to be acceptable except the input stage FET. The Fairchild 2N3277 in a TO-5 can, used for breadboarding, demonstrated suitable characteristics including noise figure. In the 0.125 in. × 0.250 in. × 0.035 in. flat package, however, the ambient temperature 330-cps noise figure for the transistor alone had increased to approximately 7.0 db from about 1.0 db in the TO-5 can. Further tests showed that the problem was associated with the noise-versus-frequency characteristic; in the flat package the characteristic low frequency 1/f rise began at a higher frequency than in the TO-5 container.

Tests were performed by Fairchild Semiconductor on two dice from the same wafer; these dice exhibited different characteristics in the two different packages. Because Fairchild Semiconductor was unable to isolate the cause of the problem, a replacement transistor had to be found.

The Siliconix 2N3578 on a 0.10 in. × 0.10 in. ceramic chip, epoxy coated, proved very satisfactory. Of 42 transistors measured for 330-cps ambient temperature noise figure, none exceeded 0.6 db; the average was about 0.3 db.

Table 1 summarizes failures and rejections in the preamplifier components.

The wirewound, 1-megohm resistor presented a major handling problem. Fine wire winding breakage occurred during all stages of assembly, encapsulation, and plating because the thickness dimension of the resistor was only 0.025 in. less than the maximum module thickness. Substituting an in-house polyurethane coating for the relatively thick and soft silicon rubber coating originally applied by the vendor provided some relief for the problem late in the program. Temperature performance, however, was suprisingly good for this type component; only two failures were directly attributable to temperature cycling.

Table 1. Preamplifier Component Failures and Rejections

QUANTITY	SYMBOL	TYPE AND VALUE	FAILURE MODE	CAUSE
23	R_1	Wirewound, 1 Megohm	Open	Physical damage
2	R_1	Wirewound, 1 Megohm	Open	Temperature cycle
3	R_2, R_4	Film pellet, 2.87 Megohm	Below tolerance	Temperature cycle
7	Q_2, Q_3	2N3117 Transistor	High noise	Factory processes
2	Q_2, Q_3	2N3117 Transistor	No output	Temperature cycle

Experience with the 2N3117 transistors during fabrication of intermediate amplifiers dictated that they be screened for noise figure before installation in the second and third stages of the preamplifier because of their wide noise figure distribution. Seven 2N3117 transistors were outside an acceptable limit; two had no output after the Receiving Inspection, -125° C soak.

Three 2.87-megohm pellet resistors were slightly below the 5% tolerance after the Receiving Inspection, -125° C soak. No component failures occurred after installation in the module except the wirewound bias resistor.

Note (Figure 2) that four resistors are considerably smaller than the mylar cutout in which they are installed. These are Caddock Electronics metal film, Type MM112, 1/20-watt resistors without molded epoxy case, 0.061 in. in diameter and 0.165 in. long. The Mepco, 1/10-watt, Type FE10 resistor, for which the layout was designed, has a 0.098-in. diameter and is 0.270 in. long. Considerable space could have been saved in the original layout had it been known at the time that the MM112 resistors were available.

2.2 INTERMEDIATE AMPLIFIER

The noise figure of the 2N3117 transistor presented the only component problem in the intermediate amplifier. The transistors in the 63 intermediate amplifiers that were assembled had been cold soaked and given a beta check, but not a noise-figure measurement,

before being installed. Of these 63 amplifiers, 16 had noise figures greater than 12.5 db, ranging as high as 60 db. Replacing first stage transistors in 13 of the 16 amplifiers with transistors that had been screened for a good noise-figure measurement resulted in 13 acceptable amplifiers.

No component failures occurred after installation. One metal film resistor (Mepco) was rejected after cold soak for being slightly below tolerance.

3.0 ELECTRICAL PERFORMANCE

3.1 PREAMPLIFIER

Table 2 summarizes "worst case" performance of those characteristics measured on the five amplifiers subjected to Design Assurance Tests. All requirements have been satisfied; however, performance was considerably better than specification limits for input impedance, output impedance, dynamic range, and independent linearity.

Table 2. Preamplifier Electrical Performance

PARAMETER	SPECIFICATION VALUE		"WORST CASE" * MEASURED VALUE
	MIN	MAX	
Input Impedance	5 megohms		20.2 megohms
Noise Figure**		5 db	4.68 db
Phase Shift		±25 deg	19.5 deg
Phase Shift Variation		±8 deg	4.75 deg
Voltage Gain	9	11	9.55 (min) 9.78 (max)
Output Impedance		2 K ohms	108.5 ohms
Input Dynamic Range	2.5 mv		180 mv
Input Capacitance		50 pf	49.8 pf
Power Consumption		5 mw	3.78 mw
Independent Linearity		8%	0.79%
Transfer Stability		2%	1.9%

* Lowest (or highest) value obtained at any test temperature on any of the five amplifiers subjected to Design Assurance Tests.

** Combined amplifier and bias resistor noise.

Figure 5 shows voltage-gain distribution as a function of temperature on all preamplifiers. Voltage-gain distribution shifts verylittle over the operating-temperature range. Individual amplifier gain remains stable (within about 1 percent) over the temperature range; the average was about 0. 5 percent.

Figure 6 shows noise-figure distribution as a function of temperature for preamplifiers. The distribution broadens at -125° C with a higher average value than at 0° C and at +30° C. The individual test data sheets previously delivered to JPL show, however, that the actual noise voltage output of the amplifiers decreased with temperature down to -125° C for those 55 amplifiers which met the combined 5 db noise identification. For the five amplifiers,temperature-limited to -80° C, the noise-voltage output decreased from +30° C to 0° C but increased as temperature was lowered to -80° C and to -125° C. What causes this condition is not known with certainty but the 2N3117 transistors of the second or third stage are suspected; for example, defects in surface passivation or imperfect bonds of the fine wire connections to the dice or the case tabs. In fact, replacement of the second stage 2N3117 in one case did correct an out-of-specification noise condition.

3.2 INTERMEDIATE AMPLIFIER

Table 3 summarizes "worst case" performance for those characteristics which were measured on the five intermediate amplifiers subjected to Design Assurance Tests. All requirements were satisfied, most of them with a comfortable margin.

Figure 7 show voltage-gain distribution as a function of temperature on intermediate amplifiers. The average drift with temperature was about 1 percent negative over the range +30° C to -50° C.

Figure 8 shows noise-figure distribution with temperature for the intermediate amplifiers. The broadening and general increase of noise-figure distribution with decreasing temperature is even more evident then for the preamplifier. The 2N3117 transistor is the only active device in the intermediate amplifier; therefore, it is most likely the

component responsible for this changing characteristic. Of the 60 intermediate amplifiers delivered to JPL, the -50° C noise figure of 46 was 10 db or less and of 14 was between 10 and 12.5 db.

Table 3. Intermediate Amplifier Electrical Performance

PARAMETER	SPECIFICATION VALUE		"WORST CASE" * MEASURED VALUE
	MIN	MAX	
Input Impedance	50 K ohms		208.3 K ohms
Noise Figure		10 db	9.72 db
Phase Shift		±10 deg	1.5 deg
Phase Shift Variation		±4 deg	0.8 deg
Voltage Gain	95	205	95.42 (min) 102 (max)
Output Impedance		500 ohms	213 ohms
Input Dynamic Range	25 mv		31.5 mv
Input Capacitance		150 pf	149 pf
Power Consumption		20 mw	14.7 mw
Independent Linearity		5%	1.05%
Transfer Stability		1%	0.41%

* Lowest (or highest) value obtained at any test temperature on any of the five amplifiers subjected to Design Assurance Tests.

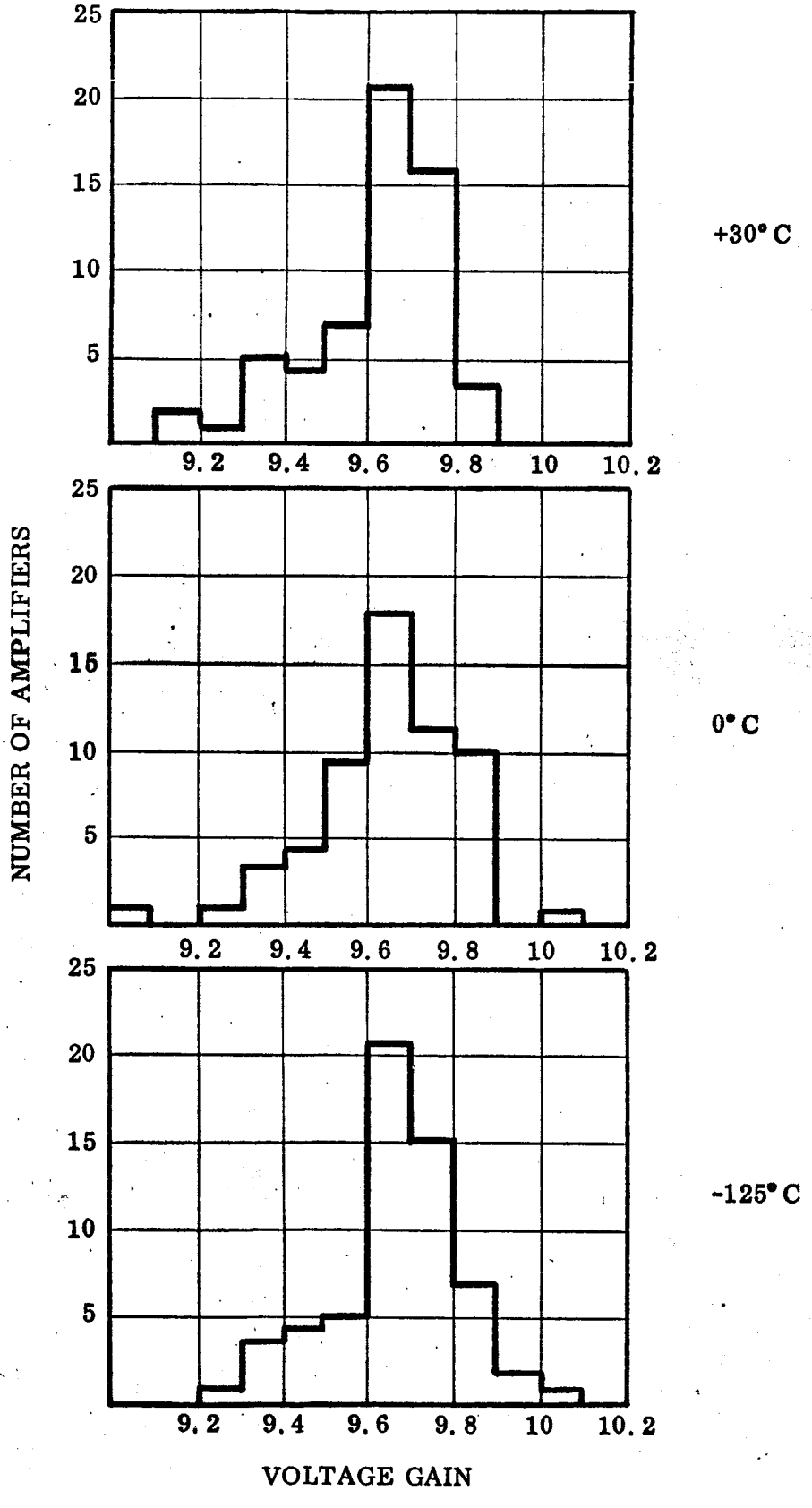


Figure 5. Preamplifier Voltage-Gain Distribution

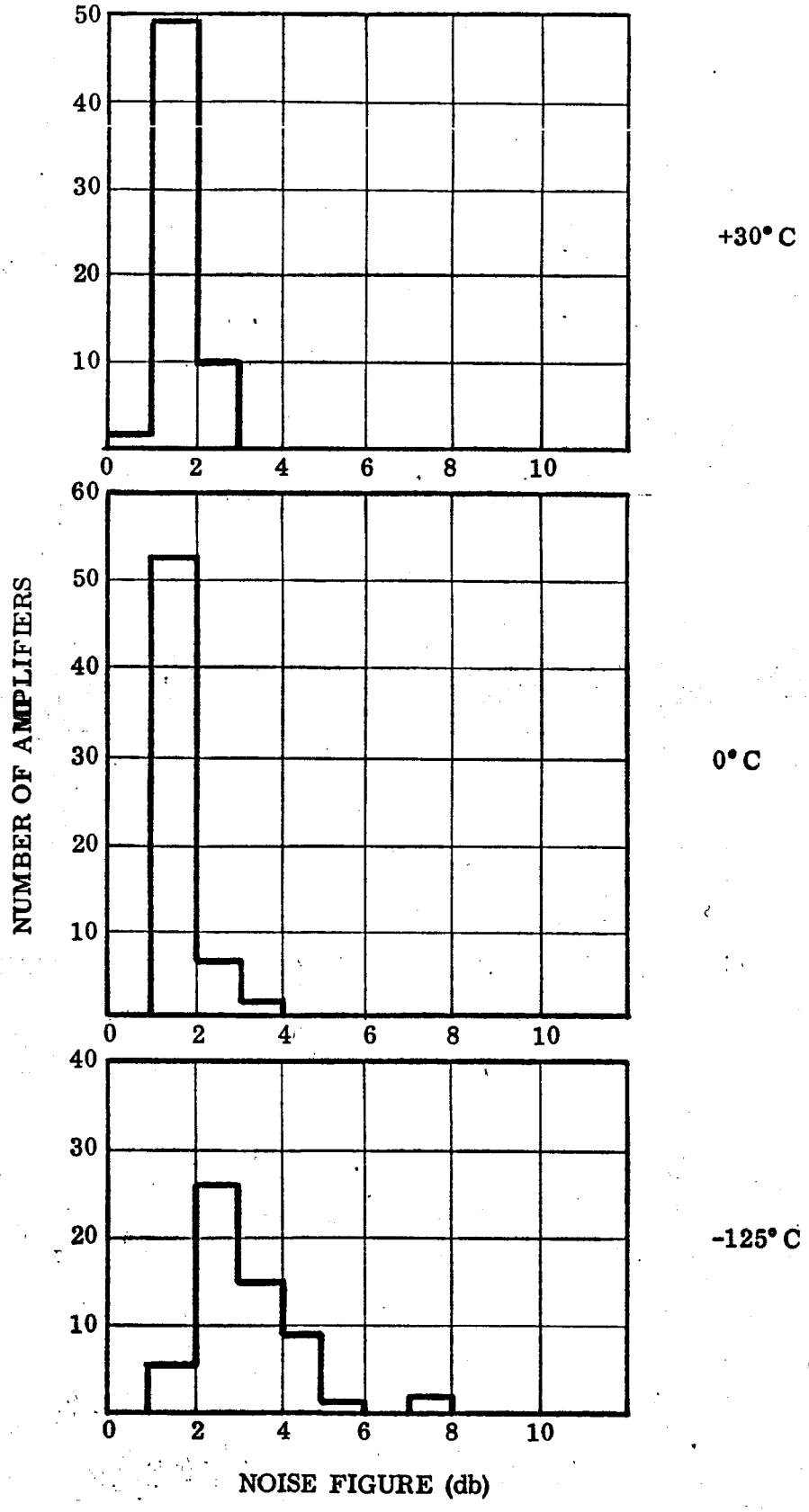


Figure 6. Preamplifier Noise-Figure Distribution

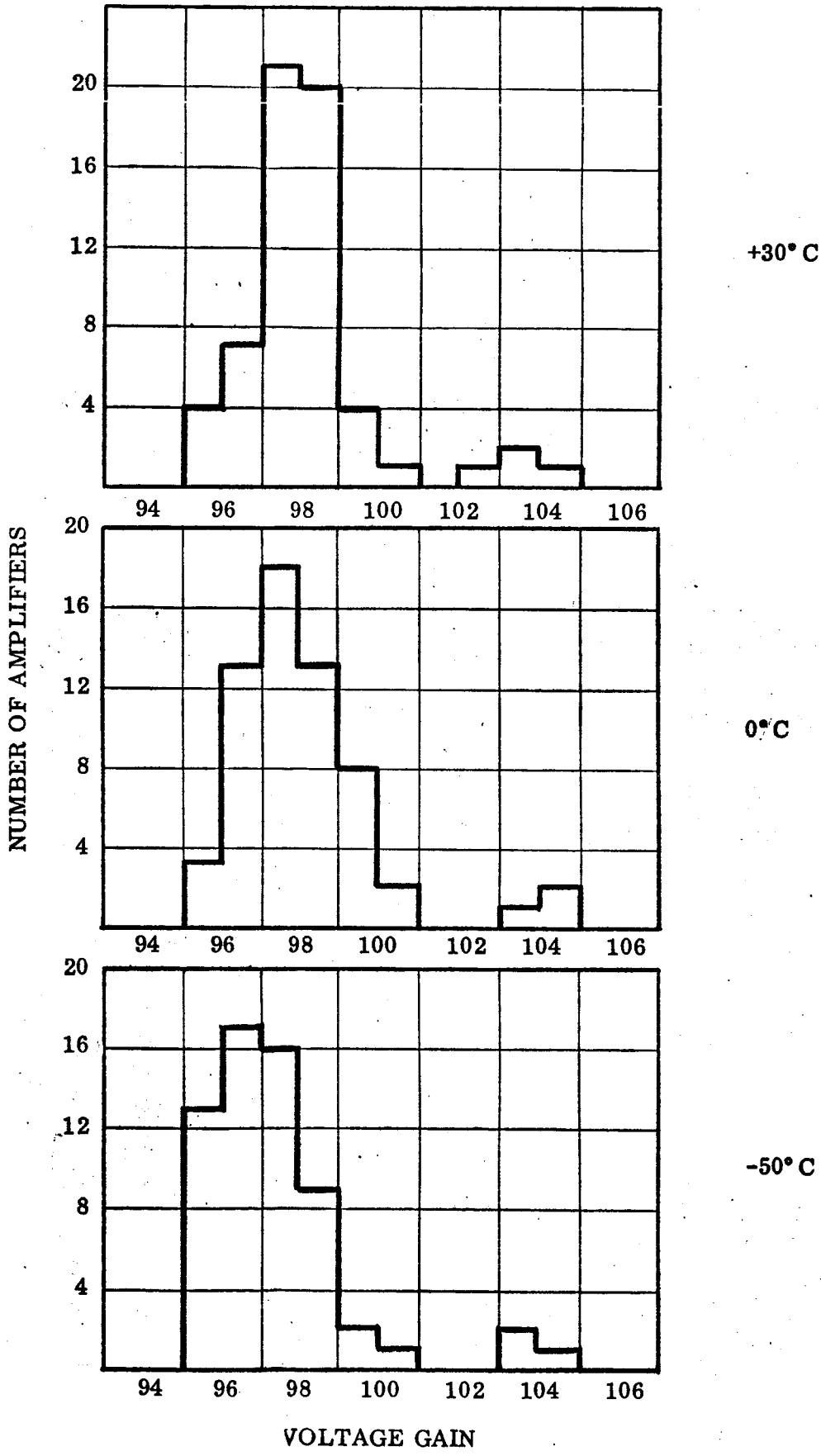


Figure 7. Intermediate Amplifier Voltage-Gain Distribution

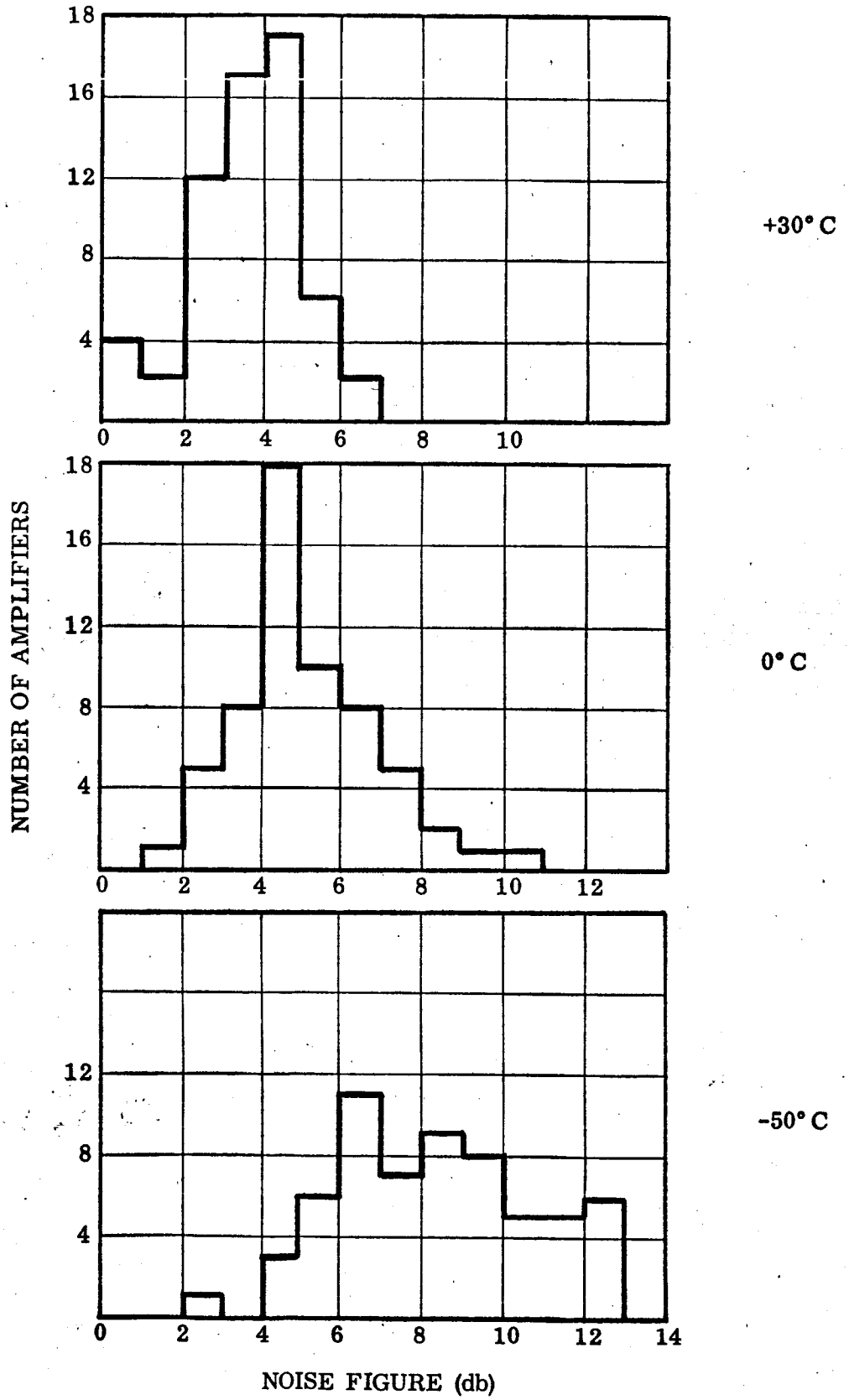


Figure 8. Intermediate Amplifier Noise-Figure Distribution

4.0 COMPONENT REPLACEMENT

Situations that dictated replacement of components in the welded assemblies before and after encapsulation were:

1) Replacement of FET 2N3277 by 2N3578 in Preamplifiers Serial No. 1 through 6
2) Replacement of Resistor R7 to match the 2N3578 characteristics
3) Replacement of Q1 in 13 intermediate amplifiers to improve noise figure
4) Replacement of Q2 in one preamplifier to improve noise figure
5) Replacement of 23 wirewound resistors (R1) in preamplifiers

The paint and electroformed shield were completely stripped from modules that had been encapsulated. The encapsulation was then removed in the area of the part to be replaced by use of a scalpel and dental pick. The weld pad and component leads were then cleaned with an epoxy stripper. The leads of the defective component were clipped adjacent to the weld pad, but the weld nugget and a small section of the lead component were left intact. The new component was then installed by Pulse-Dot soldering, a process which uses a minimum amount of controlled heat. Finally, after the void in the encapsulation was filled with Type P-37A epoxy resin, the plating and paint were applied.

In subsequent testing to the temperature extremes, no failure occurred at the connection of any of the replaced components. As a check on future performance, the amplifiers in which these repairs have been made are listed below:

Item 1)	1 through 6
Item 2)	1 through 6
Item 3)	20, 49, 23, 42, 31, 50, 27, 15, 32, 26, 29, 63, 24
Item 4)	26
Item 5)	9 (twice), 10, 16, 19 (twice) 22 (twice), 23, 25 (twice), 26, 37, 38, 39, 43, 47, 51, 55, 58, 59, 61, 62

5.0 WELDABLE PRINTED CIRCUIT BOARD FABRICATION AND WELDING CHARACTERISTICS

The details of design and manufacturing processes used to make the weldable printed circuit boards are contained in GD/E Report 3005015, previously supplied to JPL. Figure 9 illustrates the manner in which five boards were formed on a single sheet by step-and-repeat at the photo-reduction stage.

For both types of amplifiers, 0.060-in. diameter weld pads and 0.016-in. conductors were used on both sides of the board. Experimentation has been continued on improving the weld strength and strength distribution. A recently developed change in pad configuration shows promise. Eliminating the circular section on the side of the board to which the component lead is attached, improves the heat balance. In preliminary testing, this has resulted in greater strength with less dispersion. Present data indicates that strengths will exceed the requirements of JPL Specification GPO-30995-GEN by 15 to 20 percent. Detailed test results will be forwarded when available.

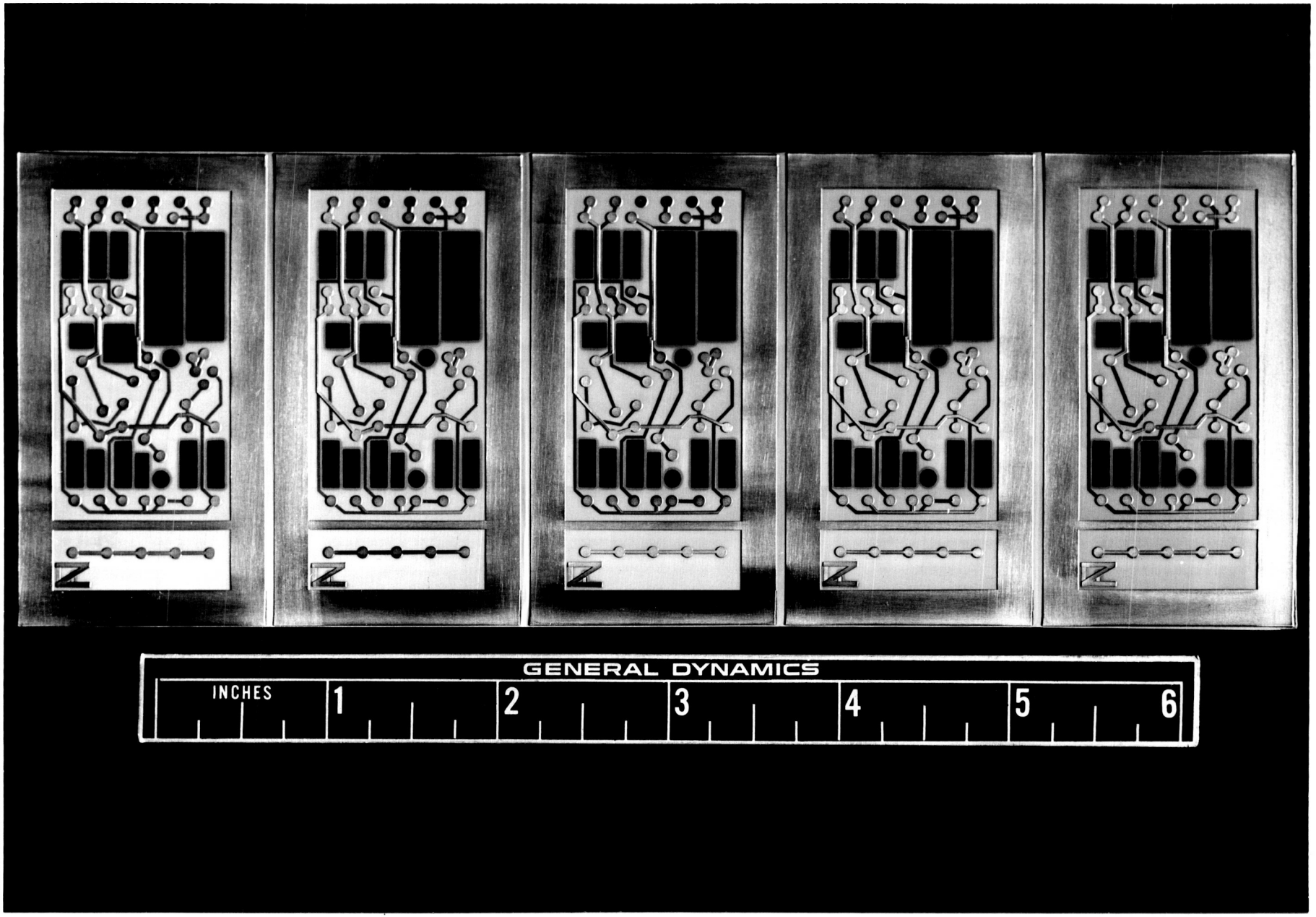


Figure 9. Multiple Printed Circuit Boards

6.0 TESTING PROCEDURES AND TECHNIQUES

All testing for the intermediate amplifiers was done in accordance with Test Procedures 1, 4, 6, 8, 10, 12, and 16, previously delivered to JPL, with the exception of noise figure measurement, Part III, 3B of TP-1. In this case, the measurement of e_{so} was eliminated and noise figure was calculated by

$$NF = 20 \log \frac{1.13\, e_{no}}{e_{th}\, K_v}$$

where

e_{no} = output noise voltage, with input terminated in R_s

K_v = amplifier voltage gain as measured in TP-1, Part III, 2

e_{th} = thermal noise of source resistance

The same change was made in measurement of preamplifier noise figure, TP-2, Part III, 3B.

The Quiet Amplifier was eliminated from the instrumentation for making preamplifier gain measurements. With the same inputs specified in TP-2, Part III, 2, the amplifier output was terminated as specified and read directly on the Model 600, Tunable Microvoltmeter. For the low-level input, the gain of the amplifier is equal to the output in microvolts divided by 10. For the high-level input, the gain is equal to the output in millivolts. The high signal level gain figure was used for noise figure calculations.

In TP-9, Preamplifier Independent Linearity, Part III, 1(b)(1), the formula should read

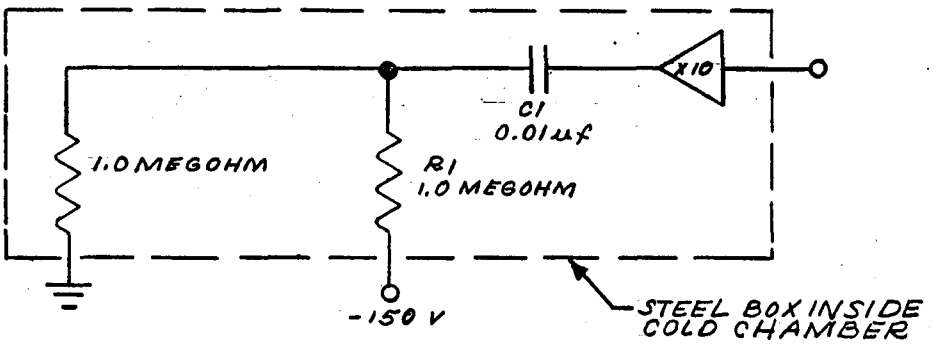
$$G_x = \frac{e_o}{e_i} \times 10$$

In TP-11, Preamplifier Transfer Stability, Part III, 1(e), the formula should read

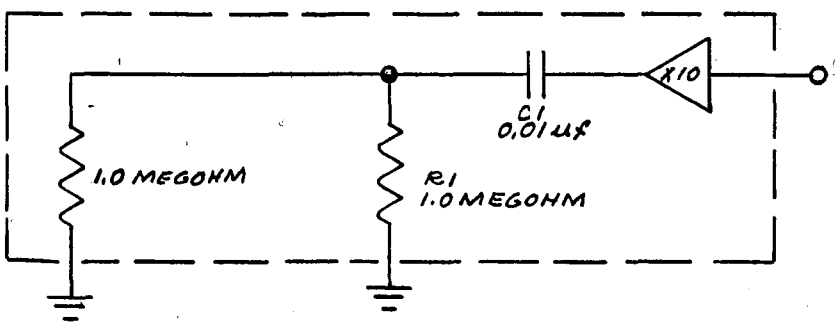
$$G = \frac{e_o}{e_i} \times 10$$

In TP-5, Preamplifier Phase Shift Measurement, Part III, 1(a), the test oscillator output was set to 300 millivolts rather than to 100 millivolts. The higher signal level was necessary to obtain reliable operation of the phase meter.

Test Procedure 14, Preamplifier Bias Resistor Noise, was eliminated entirely. To replace this procedure, noise-figure measurements were made by the procedure of TP-2 with R_s = 500 K ohms, 150 volts bias applied (NF_2) and with R_s = 500 K ohms, no bias applied (NF_3). The 500 K ohm resistance was obtained by connecting a 1.0-megohm wirewound resistor in parallel with R_1, the 1.0-megohm bias resistor as shown schematically in Figure 10.



A. NF_2 Measurement



B. NF_3 Measurement

Figure 10. Connection for Noise-Figure Measurement

Bias resistor current noise was assumed to be $NF_2 - NF_3$ where NF_2 and NF_3 were computed with R_s = 500 K ohms.

The following steps were taken to minimize the effect of external noise during noise-figure and low-level gain measurements:

1) Amplifier and source resistance were placed in steel box inside chamber
2) Inputs and outputs were on coaxial cable, including power and bias
3) Chamber power was turned off during measurement period
4) Batteries were used to supply the -150 volt bias voltage

A test jig with spring-loaded contacts to the amplifier terminals proved satisfactory for these measurements, which made soldering to the terminals unnecessary. Repeated use of the jig, however, required careful attention to the condition of the contact surfaces and to the spring tension.

Another necessary precaution is for the bias voltage to be removed when the test temperature cycle causes heavy condensation on the amplifier and test jig; i.e., when returning to ambient from the -125° C soak. Repeated failure to do so resulted in a carbonized current path on the jig terminal block and finally in severe damage to the jig and one preamplifier.

Noise-voltage measurements were made using a 30-second integration period. Several preamplifiers were observed to have higher noise figures without bias than with bias ($NF_3 > NF_2$). When this occurred, measurements were repeated to verify the condition actually existed. One explanation may be that the bias voltage stresses the input capacitor, C1, in addition to generating current through the bias and source resistors. For the unusual cases where NF_3 was greater than NF_2, the noise components of capacitor stress and resistor current may have had a canceling effect in the narrow band around 330 cps. If these few unusual cases are neglected, average bias resistor noise measured about 0.7 db, 0.4 db, and, 0.3 db at +30° C, 0° C, and -125° C, respectively.

7.0 RECOMMENDATIONS

The following changes are recommended for improved performance and reliability and for decreased size and cost if circuits of this type are to be utilized on space missions:

a. Decrease bobbin thickness of the 1.0-megohm wirewound resistor. Discussion with Kelvin Electric indicates that this can be done and the overall thickness reduced by about one-half.

b. Replace the 2N3117 transistor to provide a lower figure with less dispersion. It is felt that this can be obtained on a 0.10 in. × 0.10 in. ceramic substrate similar to the 2N3578 FET.

c. Use Caddock Type MM112 resistors without molded case. If used throughout, considerable saving in volume without loss in reliability would result.

d. Encapsulate by transfer molding using one part epoxy powder to provide a denser, more uniform coating. Application of this process to circuits of this type is being investigated at GD/E.

e. The new weld pad configuration described in Section 5.0 should provide improvement in weld strength and distribution characteristics. Test data will be furnished to JPL.

f. All resistors, with the exception of 1 megohm and 2.87 megohms, could be replaced with silk-screened Ceramet resistors, preconnected on a single wafer if further reduction in volume is of sufficient importance to justify a major redesign.

PREAMPLIFIER PARTS LIST

Resistors

Symbol	Value	Tolerance (%)	Power (watts)	Construction	Mfgr Type	Manufacturer
R_1	1.0 M	0.5	1/4	wirewound	1258P	Kelvin
* R_2, R_4	2.87 M	5	1/10	pellet	6928-RP	Mallory
* R_3	51.1 K	1	1/10	metal film	FE10	Mepco
* R_5	1.1 K	1	1/10	metal film	FE10	Mepco
* R_6	100 K	1	1/10	metal film	FE10	Mepco
* R_7	23.7 K	1	1/10	metal film	FE10	Mepco
* R_8	121 K	1	1/20	metal film	FE5	Mepco
* R_{10}	10 K	1	1/10	metal film	FE10	Mepco
* R_{11}	21.5 K	1	1/10	metal film	FE10	Mepco

* Preferred replacement; Caddock, 1/20 watt, metal film, Type MM112

Capacitors

Symbol	Value	% Tolerance	Voltage	Construction	Mfgr Type	Manufacturer
C_1	0.01 μf	10	200	metallized polycarbonate	EP34938	Electron Products
C_2	1 μf	10	20	solid tantalum	B105	Components Inc.
C_3	3.3 μf	10	20	solid tantalum	A335	Components Inc.
C_4	10 μf	10	6	solid tantalum	M10	Components Inc.
C_5	82 pf	10	200	ceramic	RH04CX820K	San Fernando Electric

Transistors

Symbol	Type	Mfgr Designation	Case Style	Manufacturer
Q_1	2N3578	SU501	0.1 in. × 0.1 in. chip	Siliconix
Q_2	2N3117	SP9953	TO-51	Fairchild
Q_3	2N3117	SP9953	TO-51	Fairchild

INTERMEDIATE AMPLIFIER PARTS LIST

Resistors

Symbol	Value	Tolerance (%)	Power (watts)	Construction	Mfgr Type	Manufacturer
R_1	147 K	1	1/10	metal film	FE10	Mepco
R_2	31.6 K	1	1/10	metal film	FE10	Mepco
R_3	12.1 K	1	1/10	metal film	FE10	Mepco
R_4	51.1 Ω	1	1/10	metal film	FE10	Mepco
R_5	68.1 K	1	1/10	metal film	FE10	Mepco
R_6	13.3 K	1	1/10	metal film	FE10	Mepco
R_7	1.0 K	1	1/10	metal film	FE10	Mepco
R_8	5.11 K	1	1/10	metal film	FE10	Mepco
R_9	6.81 K	1	1/10	metal film	FE10	Mepco
R_{10}	5.62 K	1	1/10	metal film	FE10	Mepco

Caddock, 1/20 watt, metal film, Type MM112 are a preferred replacement for all resistors.

Capacitors

Symbol	Value	% Tolerance	Voltage	Construction	Mfgr Type	Manufacturer
C_1	1 μf	10	20	solid tantalum	B105	Components Inc.
C_2	1 μf	10	20	solid tantalum	B105	Components Inc.
C_3	10 μf	10	20	solid tantalum	L10	Components Inc.
C_4	3900 pf	10	50	ceramic	G504X392K	San Fernando Electric
C_5	10 μf	10	20	solid tantalum	L10	Components Inc.
C_6	10 μf	10	20	solid tantalum	L10	Components Inc.

Transistors

Symbol	Type	Designation	Case Style	Manufacturer
Q_1	2N3117	SP9953	TO-51	Fairchild
Q_2	2N3117	SP9953	TO-51	Fairchild

LOW NOISE MICROELECTRONIC AMPLIFIER FOR OPERATION DOWN TO CRYOGENIC TEMPERATURES

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Abstract

This report describes the design and fabrication of a low level preamplifier for use in applications requiring very low noise and highly gain stable amplification over large temperature ranges with particular emphasis on temperatures of -125°C and colder. The circuit utilizes single plane, flat pack construction with microdiscrete passive components and semiconductors which are resistance welded to a mylar based printed circuit board. The over all dimensions of 1.0" by 1.8" and 0.12" in thickness include an electroplated and insulated electrostatic shield and signal/power terminals along one of the narrow edges of the package.

Summary

In many applications, when minimum size, weight, and power consumption are important considerations, the high degree of miniaturization afforded by single chip integrated circuits is unnecessary and often even impractical. In these circumstances, the utilization of microdiscrete components and microcircuit techniques can be applied to provide a degree of design flexibility, components availability, and precision performance that cannot be approached by thin film or diffused, fully integrated methods. In addition, this method of microminiaturization permits the use of fabrication techniques which are more economically suited to small production quantities as well as adaptable to large, fully automated production runs.

The method of microminiaturization to be described utilizes the flat pack type of construction in which all components are in a single plane and which results in a package shape that has one of its dimensions reduced to a practical minimum. Some advantages of this configuration are adaptability to stacking when many similar units are required, high packing density, good electrical isolation and heat sinking due to the metal shield, and repairability due to the single plane construction. Microdiscrete metal film and pellet type resistors are used along with miniature solid tantalum, ceramic, and metallized polycarbonate capacitors as the passive elements. The semiconductors include Kotab type field effect and flat pack type bipolar transistors. Components are mounted either on the printed circuit or in holes through the board to hold package thickness to less than 1/8 inch. Component leads are resistance welded to pads on the printed board and the assembly is held in place by polyurethane potting. An insulating spray coat of paint completes the module.

The electrical circuit characteristics of the amplifier are optimized for use with a high impedance, liquid nitrogen cooled, IR detector. However, the unit is useful in many other applications when low level signals from high impedance sources must be amplified by an accurately known and temperature stable scale factor, with a minimum of additional noise, by an amplifier capable of operation down to extremely low temperatures. Furthermore, due to the space and weight limitations in the vicinity of the IR detectors, particularly when multiple arrays of amplifiers are required, the size of the discrete components must be the smallest obtainable and the number of circuit components must be minimized.

Circuit Design

The electrical circuit design was based on the following list of requirements:

1. Input resistance, in the order of 50 megohms
2. Input capacitance, less than 20pf
3. Voltage gain, 20db
4. Gain stability, ± 0.5 percent
5. Output amplitude, up to 1 volt pp
6. Frequency response, ± 1db from 10 cps to 100 kc
7. Output resistance, less than 500 ohms
8. Spot noise figure, less than 2db for source resistances between 0.2 megohm and 2.0 megohm and frequencies down to 300 cps
9. Temperature range, -125°C to +30°C specified, -175°C to +100°C objective
10. Total power consumption, less than .005 watts

Additional requirements restricting the design were protection against transients on the signal input terminal due to power supply turn on and the necessity for a minimum parts count due to severe space and weight limitations.

The specified performance was achieved by the use of the three stage feedback amplifier shown in Figure 1. The utilization of complementary transistors permitted dc coupling which resulted in a high degree of dc feedback and consequently good operating point stability as

well as a minimization of the parts count. High open loop gain was obtained by the elimination of local signal feedback and isolation of the two gain stages. Over all negative feedback was facilitated by the use of only two phase inversions while closed loop gain was made dependent upon only the ratio of the values of two precision film resistors.

Input Impedance and Noise Figure

In order to obtain the high input resistance and low noise figure in the range of source resistances specified, it was necessary to employ a field effect device for the input stage. The FET used has a maximum gate leakage current of only a few nanoamperes at the upper end of the specified temperature range which indicated that the input resistance would be limited to about 1000 megohms. However, due to bias stability requirements, a much lower gate source circuit resistance was necessary. Using a high degree of negative feedback and gate to source boot-strapping provided both a high dynamic input resistance of 50 megohms and a practical, low dc gate circuit resistance of less than 3 megohms.

An additional advantage of boot-strapping in the input circuit is the effective decrease in the capacity, particularly when the amplifier operates with high impedance sources and moderately fast response is required. The input capacitance is determined by the sum of the stray shunt capacities and the FET dynamic input capacity. The latter is given by

$$C_i = C_{gs}(1 - K_{gs}) + C_{gd}(1 + K_{gd}) \qquad (1)$$

where C_{gs} and C_{gd} are the device terminal to terminal capacities and K_{gs} and K_{gd} are the absolute voltage gains between the indicated terminals. The first term on the right side of the equation indicates that C_{gs} will be virtually eliminated since the feedback will tend to make K_{gs} equal to unity. The second term shows that C_{gd} will tend to increase due to the Miller effect; however, as shown in the appendix and because the drain of the FET is within the feedback loop, K_{gd} will be much smaller than unity. Thus, since C_{gs} is in the order of 12-20 pf and C_{gd} is 3-6 pf, the effective input capacity will be only a few picofarads. However, due to the thinness of the package, the stray capacities result in an input terminal capacitance of 15-20 pf.

In addition to the advantage of considerably higher input impedance, when compared with practical input impedances available with bipolar transistors using similar feedback techniques, the FET also has an advantage with respect to noise figure when used with high resistance sources. Since its output current does not pass through any p-n junctions, the only source of shot noise is the extremely small gate leakage current. This results in a low noise figure with much larger source resistances and over much larger ranges of source resistance than are available from bipolar transistors. A further advantage of the FET, when it must be operated at low frequencies, is the position in the frequency spectrum of its flicker noise or 1/f region. The 1/f corner for bipolar transistors occurs near 1 kc, while for an FET, the corner occurs near 100 cps for source resistances in the order of 1 megohm.

For the frequency range in which this amplifier operates, the output impedance of the first stage is in the same order as or is higher than the load resistance. Under these conditions, the noise generated by the load resistance must be considered and the resulting noise figure equation for the amplifier becomes

$$F = F_1 + \frac{F_2}{P_1} + \frac{F_3}{P_1 P_2} \qquad (2)$$

where F is the over all noise factor and F_1, F_2, F_3, P_1, and P_2 are the corresponding noise factors and power gains of the three individual stages. As indicated, the over all noise factor will be very nearly the noise factor of the input transistor if the power gain of the first stage is sufficiently high. A further condition for low noise requires an optimum source resistance of about 20k for the second stage and 4k for the third. In this amplifier, however, the gain stability, low power, and low temperature specifications necessitate a compromise of the above conditions resulting in a slightly greater noise figure and the requirement for low noise transistors in the third as well as the second stages. The power gain from the input terminal to the drain of the FET is approximately 10db indicating the second stage noise cannot be neglected. The source resistance required by the second stage, however, has a relatively broad optimum region centered around 20k ohms so that the actual source resistance of about 100k ohms produces a sufficiently low noise figure. The emitter follower provides power gain and approximately the correct source impedance for the output stage; however, due to the impedance transformation, the output stage also influences the over all noise figure. Although all stages influence the noise figure, the contributions from each are small, and as shown in the performance table, over all noise figures between 1db and 2db can be obtained.

Gain Stability

In order to obtain the required gain stability and linearity, a large amount of feedback, high open loop gain, and good operating point stability were necessary. Typical temperature coefficients for the drain current of an FET are approximately -0.6 percent per degree Centigrade while typical collector current drifts in npn transistors are about +0.5 percent per degree C. The dc feedback reduces these temperature coefficients by a factor of 10, and in addition, reverses the transistor's coefficient improving its ac gain characteristics at the lower temperatures. The resulting dc operating point

stability is typically ± 5 percent on FET drain current and ± 3 percent on transistor collector current over the temperature range +75°C to -150°C.

The degree of open loop stability required is indicated by the differential of the basic feedback amplifier equation

$$\%\Delta A_f = \frac{\%\Delta A}{1 + AB} \quad (3)$$

where: ΔA_f = the change in closed loop gain
ΔA = the change in open loop gain
$1 + AB$ = the feedback level

For this circuit, due to the variation in semiconductor parameters with temperature, open loop ac gain varies inversely with temperature down to about -100°C and then reverses. The maximum change in gain is about 75 percent; thus, the amplifier open loop gain of about 63db results in 43db of feedback and the required closed loop gain stability of 0.5 percent.

Low Temperature Operation

Disregarding mechanical failures, passive components, in general, function in a normally predictable way at any temperature from +100°C down to the cryogenic region. For example, all parameters of film resistors except temperature coefficient are normally controlled to -125°C. Information on solid tantalum capacitors shows relatively linear and predictable parameter variation down to -190°C. Since the field effect transistor is a majority carrier device resembling a voltage controlled resistor, it also, in general, functions predictably at lower temperatures. Bipolar semiconductors, however, are not normally rated for low temperatures and published data for operation below -65°C are not usually available.

Published typical operating characteristics for silicon diffused bipolar transistors, at temperatures between -65°C and +100°C indicate a relatively linear variation with temperature. Above and below this range, normal semiconductor properties begin to deteriorate and eventually disappear with the result that transistor action ceases. As shown by the experimentally obtained curves of Figure 4, current gain under constant dc current operating conditions, for example, decreases almost linearly from its +25°C value as temperature decreases. Below -60°C however, the rate of fall decreases and the characteristic curve tends to approach zero gain at 0°K asymptotically. Although the curves show that current gain drops to very low values (about 2% of its +25°C value) at -200°C, the dynamic input impedance also behaves in much the same way thereby making amplification, at least for small signals, possible.

For low frequency FET amplifiers employing large load to source resistance ratios, the voltage gain is given by

$$A_{v1} = gm\, R_L \quad (4)$$

where: gm = small signal transconductance
R_L = drain circuit ac load resistance

Voltage gain for bipolar transistor amplifiers is given approximately by

$$A_{v2} = \frac{h_{fe} R_L}{h_{ie} + R_g} \quad (5)$$

where: h_{fe} = short circuit small signal current gain
h_{ie} = short circuit input impedance
R_L = collector circuit ac load resistance

If the two single stage amplifiers are connected in simple cascade, however, neither optimum over all gain nor satisfactory low temperature operation is obtained due to the mutual loading. The large drain resistance of the FET stage is shunted by the relatively low input impedance of the bipolar stage and the high output impedance of the FET stage appears in series with the input of the bipolar stage. As indicated in Figures 3 and 4, the gain of each unloaded stage increases as temperature decreases toward approximately -100°C; however, the loading on the FET due to h_{ie} increases at a greater rate resulting in a decreasing over all gain characteristic. An additional stage, consisting of a simple emitter follower interposed between the two amplifiers provides the impedance level conversion required to obtain more satisfactory performance from the over all amplifier. As shown in Figure 5, the high input impedance and low output impedance of the emitter follower effectively isolate the FET and bipolar stages giving an over all voltage gain nearly equal to the product of the individual unloaded gains.

Electrical noise due to passive components will generally decrease as temperature decreases. Neglecting resistance changes due to temperature coefficient, resistor noise decreases as temperature decreases since the thermal component of resistor noise is directly proportional to the square root of temperature. Current noise in resistors, however, is independent of resistance and temperature. Noise due to capacitors tends to decrease at low temperatures since leakage decreases.

The two main sources of noise in an FET are the thermal noise of the conducting channel and the shot noise caused by the gate leakage current. Since both sources are increasing functions of temperature, the electrical noise decreases at lower temperatures. Flicker noise is an additional important source of noise in bipolar transistors. Along with shot noise, it contributes to increasing electrical noise at lower temperatures due to increasing junction resistance.

D C Operating Conditions

The noise figure of the FET stage is relatively independent of the operating point, while the noise figure of the bipolar stage is a sensitive function of dc collector current. For this reason, the FET stage biasing is based mainly in obtaining the correct operating conditions in the output stage along with the highest gain at the lowest practical current in the first stage. The FET operates at about 60 ua and the output stage at about 200 ua. The resulting total power requirement is less than 5 milliwatts and the open loop gain is about 1000 at $+25^{o}C$ and $-165^{o}C$.

Packaging Design

Packaging Requirements and Constraints. The packaging design was based on the following list of requirements and constraints: (Figure 1)

1. The maximum package size was to be . 125 x 1. 0 x 2. 0 inches exclusive of terminals and positioning flanges.

2. Six terminals were to be provided at one end of the package. These terminals were . 09 inch diameter, gold plated, bifurcated, and soldered terminals.

3. Operating temperatures were $-125^{o}C$ to $+30^{o}C$ with a design goal of $-175^{o}C$ to $+100^{o}C$.

4. Headers containing the terminals were of . 062 inch epoxy/fiber glass board. This board was to extend beyond the maximum envelope . 12 inch on each side to form position flanges for use during mounting.

5. The package was to be elec trostatically shielded.

Considering the above package requirements and constraints, it is apparent that the package must have a high degree of flexibility, especially in environmental temperatures; it must be small and disproportionately thin, and it still must support solder terminals. With the further considerations of development time and development cost, the decision was made to use microcircuit techniques and microdiscrete components as opposed to integrated circuits. The GD Flat-Pak Module Technique was used. This technique was the only practical method of meeting the . 125 inch package thickness requirement and still use discrete components.

Description of the GD Flat-Pak Module. The Flat-Pak is a welded planar electronic circuit module technique developed by General Dynamics. The planar terminology is derived from its two dimensional weldment configuration on a two sided printed circuit board. It has the advantage of the repeatability of a printed circuit board plus the reliability of a resistance welded module.

The circuit board material is mylar . 001 inch thick laminated on both sides with one-ounce copper (. 0014 inch thick). Holes were etched through the circuit board material to accept the body of each electronic component and in the area of each land to allow the lands to be placed through and therefore be conductors from one side to the other, both for circuit continuity and for opposed electrode welding. The lands are matched pads on both sides of the circuit board connected together through the mylar substrate by electroplated nickel. The hole which is etched through the circuit board material for each land is smaller than the matched pads on each side so that the mylar is sandwiched in a similar way as with an eyelet. The electronic components were dropped into the etched clearance holes in the circuit board material and the leads were welded to the lands with a vertically opposed electrode welder. This eliminated the necessity to bend the leads of all electronic components which have coplanar leads. The leads were pre-cut to a predetermined length and are relatively short since no heat sinking is required during the short weld cycle.

The circuit interconnections are nickel plated copper. The electro-plated nickel serves a dual purpose. It acts as a resist to the copper etchant during final etching and it aids welding due to the low resistance of copper when bare and unplated.

The minimum thickness of the Flat-Pak Module is determined by the dimension of the largest electronic component in the module. Since components lie in the holes in the circuit board, they protrude from both sides of the circuit board, and the thickness of the circuit board is not additive in determining the module thickness. The maximum height of each component as mounted was limited to 0. 11 inch for this 0. 125 inch dimension of the module. The minimum length and minimum width of the module are determined by the cross sectional area of each component plus the conductor area, the welding land area, and necessary spacing between each. It follows, then, that holding line conductor lengths to a minimum and equalizing the number of conductors on each side of the printed circuit board will tend to increase the over all parts density by holding down the area required for conductors.

Packaging Layout of the Module. The packaging layout was made four times scale on mylar drawing format. The choice of scale was made to a large extent by considering conductor widths and welding land sizes versus available tape widths and circle sizes since the masters were made by taping. The layout was made on a drawing format to expedite the task since it became the assembly drawing after the addition of identifications and the parts list. The electronic components were laid out to the maximum size allowed by specification with connection points shown as lands or circles with a cross in the center for matching the art work. A frame

was added all around, external to the circuit area, for handling rigidity and to prevent damage during later fabrication and assembly. This frame also acts as a "thief" during electro-plating to prevent excessive nickel build-up on the conductors. Lands were also added, external to the circuit area, for use during assembly for further proofing of weld schedule and for inspection. As a matter of nomenclature, the side viewed when looking at the layout is considered "near side" and is the side on which all electronic components are mounted. Conductors for interconnection are shown as single lines and conductors on the "far side" of the board to component leads are shown as dotted.

Preparation of the Circuit Photo Masters. The art work for the circuit photo masters (Figure 8) is the conventional black tape and circles on mylar drawing format. The masters were made to match the layout and therefore match each other. Three photo masters are required for the Flat-Pak. These are the near side circuit, the far side circuit, and the hole pattern. The hole pattern master allows holes to be etched for the components and in the welding lands for continuity from one side to the other. For the component holes, the entire component outline was taped solid, but for the welding land holes, only a small circle was placed in the center of the land. The land size is .060 inch diameter on both sides and the hole through the mylar is .040 inch diameter. This, once again, is for the eyelet effect. The conductor lines are .016 inch wide. These were the dimensions before nickel plating. The module size is 1.0 x 2.0 inches exclusive of the frame.

When the masters were photographed to reduce them to the actual size of the module, a number of images were put on a single sheet of film by a step-and-repeat process. This allows several module printed circuit boards to be made at one time on a single sheet of material. Positive transparencies of each of the three masters are used in this process.

Fabrication of the Printed Circuit Board. The Flat-Pak Circuit Board material is copper/mylar laminate. The mylar substrate thickness is .001 inch and the copper is one-ounce on each side. Briefly, the basic steps of fabricating circuit boards are as follow: (Figure 9)

1. The copper/mylar laminate is sensitized with a photo resist and is exposed to light with the hole pattern positive in contact.

2. The copper on one side of the laminate and the mylar are etched away in this hole pattern leaving only the copper on the other side.

3. New photo resist is applied and the laminate is again exposed to light with near side and far side circuit pattern positives in contact.

4. These circuit patterns on each side of the laminate are then electro-plated with nickel to a .004 inch thickness.

5. The photo resist is removed and all copper is etched away leaving only the nickel plated circuit and exposing the mylar substrate containing the etched component holes.

The sheet of circuit boards is now ready for assembly and welding of electronic components in place. Up to this point, these boards were fabricated with only photographic, chemical etching and electro-plating processes and no hand work or machine work was required.

Assembly and Finish of the Modules. The electronic components and the header were resistance welded to the printed circuit board with a vertically opposed electrode welder (Figure 7). When the holes were etched in the welding lands and subsequently plated, a dimple was left on the far side of each land. The bottom electrode was located in this dimple while welding. This combination is an automatic positioning feature. The header was made from .062 inch thick epoxy/fiber glass laminate with swaged-in solder terminals. These terminals contain pins on the circuit side of the header which were resistance welded to the circuit lands.

After the circuit boards were assembled and functionally tested, the frame was cut away from the circuit. They were conformally coated with polyurethane and encapsulated in a rigid polyurethane foam. This foam was used in preference to a solid or filled resin because tests indicated that it would be superior in the extremely low operating temperatures and would least affect the circuit function. Some resins fracture at these low temperatures. After curing, the foam was given a seal coat to insure a smooth surface on which to plate.

The modules were then ready for electrostatic shielding. This was accomplished by nickel plating the entire module except the header. The case common terminal has a piece of copper foil running to the surface of the module such that, when plated, the case was attached to the foil and was electrically common. The modules were first coated over the surface with approximately ten millionths of an inch of electroless copper and were painted, serialized, and identified and were complete and ready for final functional test.

The volume of this module is .25 cubic inch and each module weighs 6 grams and contains 18 electronic components. The parts density, then, is 72 per cubic inch and weighs less than one ounce per cubic inch.

Appendix

1. Derivation of Amplifier Gain

$$V_{gs} = e_i - v_s \tag{1}$$

$$= e_i - (i_d + i_{c2}) R_1 \tag{2}$$

$$= e_i - gm V_{gs} R_1 - i_{c2} R_1 \tag{3}$$

$$i_{c2} = h_{fe2} i_{b2} = (1 + h_{fe1}) h_{fe2} i_{b1} \tag{4}$$

$$i_d = i_{b1} \frac{R_4 + h_{ie1}}{R_4} \tag{5}$$

Then from Eq. (4) and (5)

$$i_{c2} = (1 + h_{fe1}) h_{fe2} i_d \frac{R_4}{R_4 + h_{ie1}} \tag{6}$$

$$= (1 + h_{fe1}) h_{fe2} gm V_{gs} \frac{R_4}{R_4 + h_{ie1}} \tag{7}$$

$$= gm V_{gs} h_{fe}' \tag{8}$$

where

$$h_{fe}' = (1 + h_{fe1}) h_{fe2} \frac{R_4}{R_4 + h_{ie1}}$$

Substituting Eq. (8) in (3)

$$V_{gs} = e_i - gm V_{gs} R_1 - gm V_{gs} R_1 h_{fe}' \tag{9}$$

$$e_i = V_{gs} (1 + gm R_1 h_{fe}') \tag{10}$$

$$e_o = V_s + i_{c2} R_2 \tag{11}$$

$$= e_i - V_{gs} + gm V_{gs} h_{fe}' R_2 \tag{12}$$

From Eq. (10) and (12)

$$e_o = V_{gs} (1 + gm R_1 h_{fe}') - V_{gs} + gm V_{gs} h_{fe}' R_2 \tag{13}$$

$$= gm V_{gs} h_{fe}' (R_1 + R_2) \tag{14}$$

From Eq. (10) and (14)

$$\frac{e_o}{e_i} = \frac{gm h_{fe}' (R_1 + R_2)}{(1 + gm h_{fe}' R_1)} \tag{15}$$

Eq. (15) is in the feedback amplifier form

$$K_f = \frac{K}{1 + KB} \tag{16}$$

where

$$K = gm h_{fe}' (R_1 + R_2) = \text{open loop gain} \tag{17}$$

$$KB = gm h_{fe}' R_1 = \text{feedback factor} \tag{18}$$

$$B = \frac{R_1}{R_1 + R_2 \frac{h_{fe}'}{1 + h_{fe}'}} = \frac{R_1}{R_1 + R_2} \tag{19}$$

Then since the open loop gain is high (i.e. KB >> 1), the closed loop gain is

$$K_f = \frac{1}{B} = \frac{R_1 + R_2}{R_1} \tag{20}$$

2. Input Resistance

$$R_i = \frac{e_i}{i_i} = \frac{e_i R_g}{e_i - V_s} = \frac{e_i R_g}{V_{gs}} \tag{21}$$

$$e_i = V_{gs} + V_s$$

$$= \frac{i_{c2}}{gm h_{fe}'} + i_d R_1 + i_c R_1 \tag{22}$$

$$= \frac{i_{c2}}{gm h_{fe}'} + \frac{i_{c2} R_1}{h_{fe}'} + i_{c2} R_1 \tag{23}$$

$$= i_{c2} \left[\frac{1 + gm R_1 + gm h_{fe}' R_1}{gm h_{fe}'} \right] \tag{24}$$

$$= V_{gs} (1 + gm R_1 h_{fe}') \tag{25}$$

From Eq. (21) and (25)

$$R_i = R_g (1 + gm R_1 h_{fe}') \tag{26}$$

3. Input Capacitance

$$C_i = C_{gs} (1 - K_{gs}) + C_{gd} (1 + K_{gd}) \tag{27}$$

where

C_{gs} and C_{gd} are the FET terminal capacitances

K_{gs} and K_{gd} are the gate to source and gate to drain voltage gains

$$K_{gs} = \frac{V_s}{e_i} = \frac{e_i - V_{gs}}{e_i} = 1 - \frac{V_{gs}}{e_i} \quad (28)$$

$$1-K_{gs} = \frac{V_{gs}}{e_i} \quad (29)$$

From Eq. (10), (27), and (29)

$$C_{gs}' = C_{gs} \frac{1}{1 + gm h_{fe}' R_1} \quad (30)$$

For the C_{gd} term in Eq. (27)

$$K_{gd} = \frac{V_d}{e_i} = \frac{i_d}{e_i} \cdot \frac{R_4 R_e'}{R_4 + R_e'} \quad (31)$$

where

$$R_e' = h_{ie1} + \frac{(h_{fe1} + 1) R_{e1} h_{ie2}}{R_{e1} + h_{ie2}}$$

R_{e1} = the emitter resistor of the emitter follower

From Eq. (10) and (31)

$$\frac{V_d}{e_i} = \frac{R_e'}{(1 + h_{fe1}) h_{fe2} R_1} \quad (32)$$

and from Eq. (27), (31), and (32)

$$C_{gd}' = C_{gd}\left[1 + \frac{R_e'}{h_{fe1} h_{fe2} R_1}\right] \quad (33)$$

4. Noise Figure

The noise factor of an amplifier is defined as

$$F = \frac{\text{Total noise power referred to amplifier input}}{\text{Noise power due to the source resistance}} \quad (34)$$

Since both the input signal and the input noise power have the same generator resistance R_s, and both the output signal and output noise power hav have the same load resistance; the noise figure can be expressed in the more conveniently measured voltage rather than power.

$$NF_{(db)} = 20 \log \frac{E_{no}}{A_v \sqrt{4KTBR_s}} \quad (35)$$

where

E_{no} = total output noise voltage

A_v – amplifier voltage gain

B = noise bandwidth

R_s = source resistance

k = Boltzman's constant

T = absolute temperature

When the amplifier consists of more than one stage the overall power gain is $P_1 \ldots P_n$ and the output noise is

$$N_o = F_n P_n + F_{n-1} P_n P_{n-1} + \ldots + F_1 P_n \ldots P_1 \quad (36)$$

where

F is the per stage noise factor

P is the power gain

n is the number of stages

Dividing each term by the overall power gain gives the overall noise factor

$$= F_1 + \frac{F_2}{P_1} + \ldots \frac{F_n}{P_1 \ldots P_{n-1}} \quad (37)$$

The noise figure for the emitter follower and common emitter amplifier is found as follows:

From the general noise factor equation

$$F = \frac{\left(\frac{S}{N}\right)_i^2}{\left(\frac{S}{N}\right)_o^2} = \frac{\frac{P_s}{kTB}}{\frac{V_s^2}{V_n^2}} \quad (38)$$

If the emitter follower signal output is expressed as

$$V_s^2 = \left[\frac{R_e}{R_e + h_{ib}}\right]^2 4 P_s R_s = 4 G^2 P_s R_s \quad (39)$$

and the noise voltages are expressed as

Thermal noise in R_s = $4kTBR_s G^2$

Shot noise in R_n = $4kTBR_n G^2$

Thermal noise in R_e = $4kTBR_e (1 - \frac{1}{G})^2$

Shot noise in R'_n = $4kTBR'_n$

Then the noise factor is

$$F = \frac{P_s}{kTB} \cdot \frac{4kTB}{4G^2 P_s R_s} \cdot \left[R_s G^2 + R_n G^2 + R'_n + R_e \left(1 - \frac{1}{G}\right)^2 \right] \quad (40)$$

$$= 1 + \frac{R_n}{R_s} + \frac{R_n'}{G^2 R_s} + \frac{R_e}{R_s} \left(1 - \frac{1}{G}\right)^2 \quad (41)$$

Since G will be very nearly unity

$$F = 1 + \frac{R_n}{R_s} + \frac{R_n'}{R_s} \quad (42)$$

where

P_s = signal power

R_s = source resistance

R_n = equivalent noise resistance

R_n' = transformed equivalent noise resistance of next stage

$G = \frac{R_e}{R_e + h_{ib}}$ = voltage gain of emitter follower

5. Output Resistance

$$V_s = (i_d + i_{c2}) R_1 \quad (43)$$

$$= gm\, V_{gs} R_1 + i_{c2} R_1 \quad (44)$$

$$i_{c2} = \frac{V_s}{R_1} - gm\, V_{gs} \quad (45)$$

From Eq. (11) and (45)

$$e_o = V_s + \frac{V_s}{R_1} R_2 - gm\, V_{gs} R_2 \quad (46)$$

The output current is the difference between the feedback and collector currents.

$$i_o = i_{fb} - i_{c2} = \frac{V_s}{R_1} - gm\, V_{gs} - gm\, V_{gs} h_{fe}' \quad (47)$$

Since R_o is measured with e_i equal to zero $V_{gs} = -V_s$, therefore

$$R_o = \frac{e_o}{i_o} = \frac{V_s + V_s R_2/R_1 + gm\, V_s R_2}{V_s/R_1 + gm\, V_s + gm\, V_s h_{fe}'} \quad (48)$$

$$= \frac{1 + \frac{R_2}{R_1}}{gm\, h_{fe}'} \left[1 + \frac{R_1 R_2 gm}{R_1 + R_2} \right] \quad (49)$$

$$\doteq \frac{R_1 + R_2}{KB} \quad (50)$$

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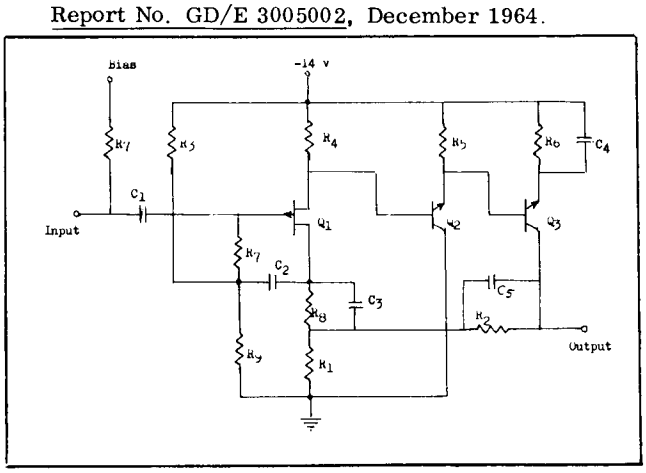
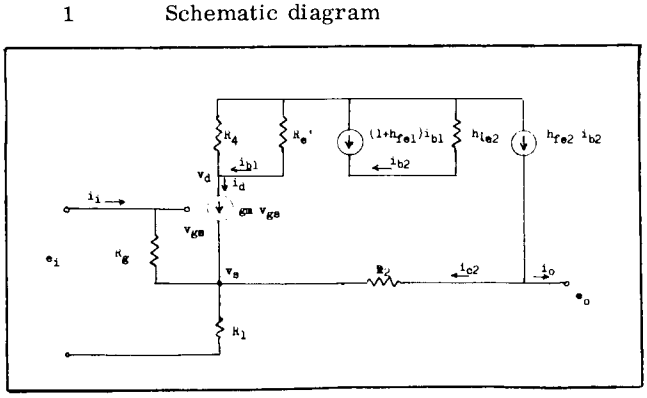
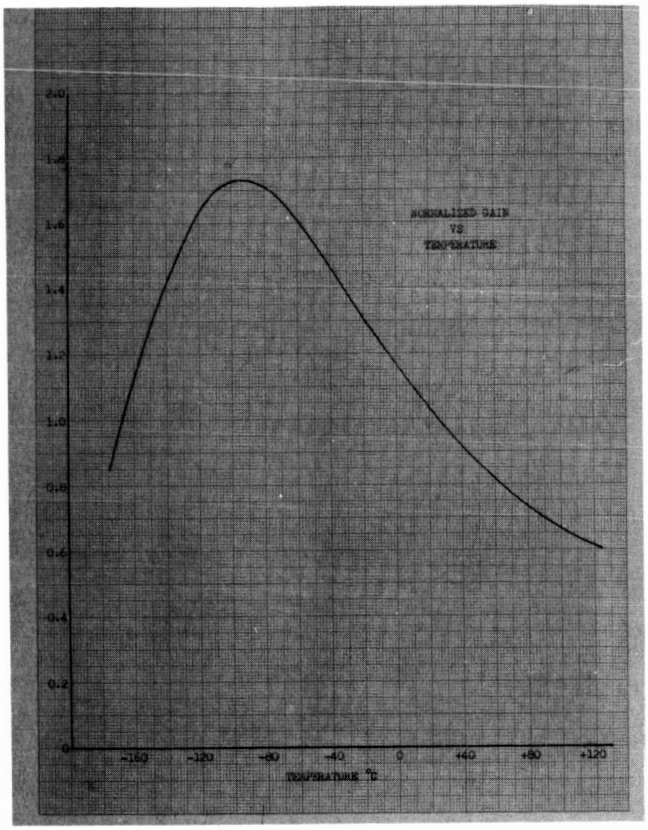


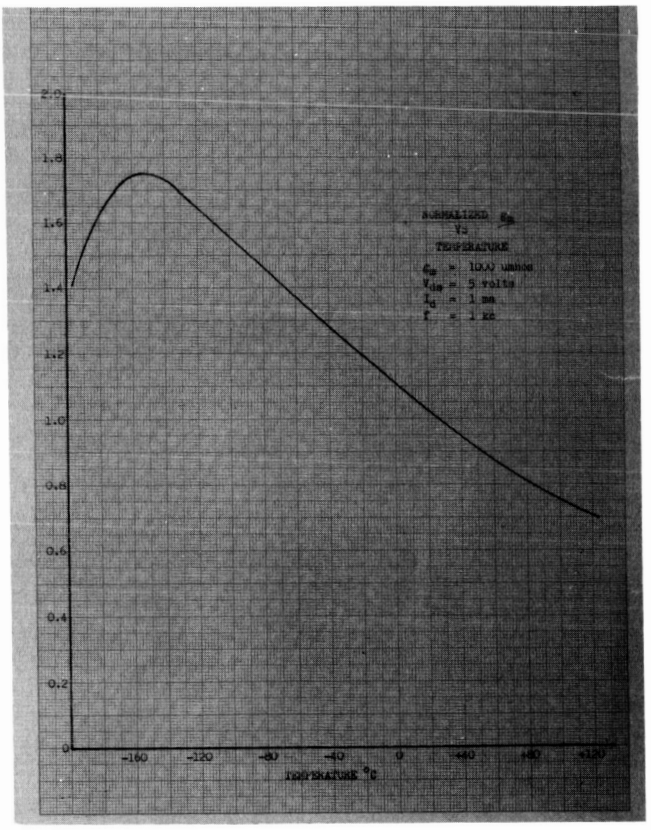
1 Schematic diagram



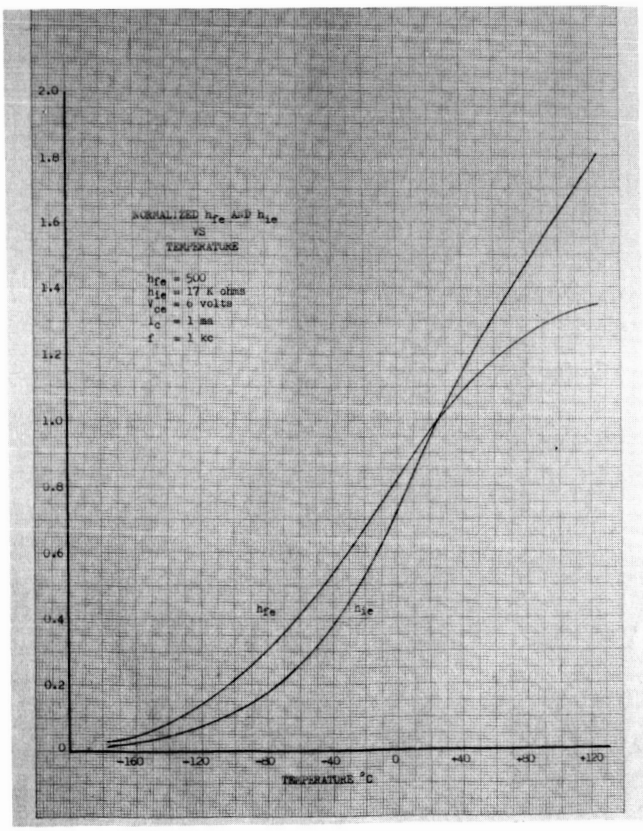
2 Equivalent circuit



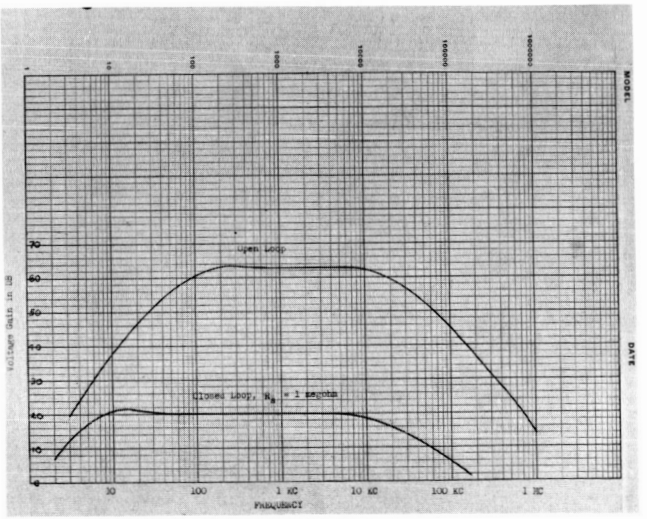
3 FET transconductance versus temperature



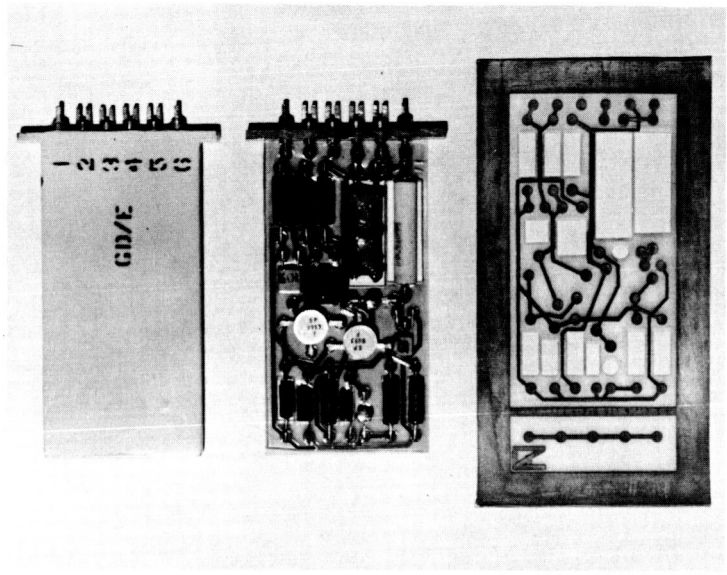
5 Open loop gain versus temperature



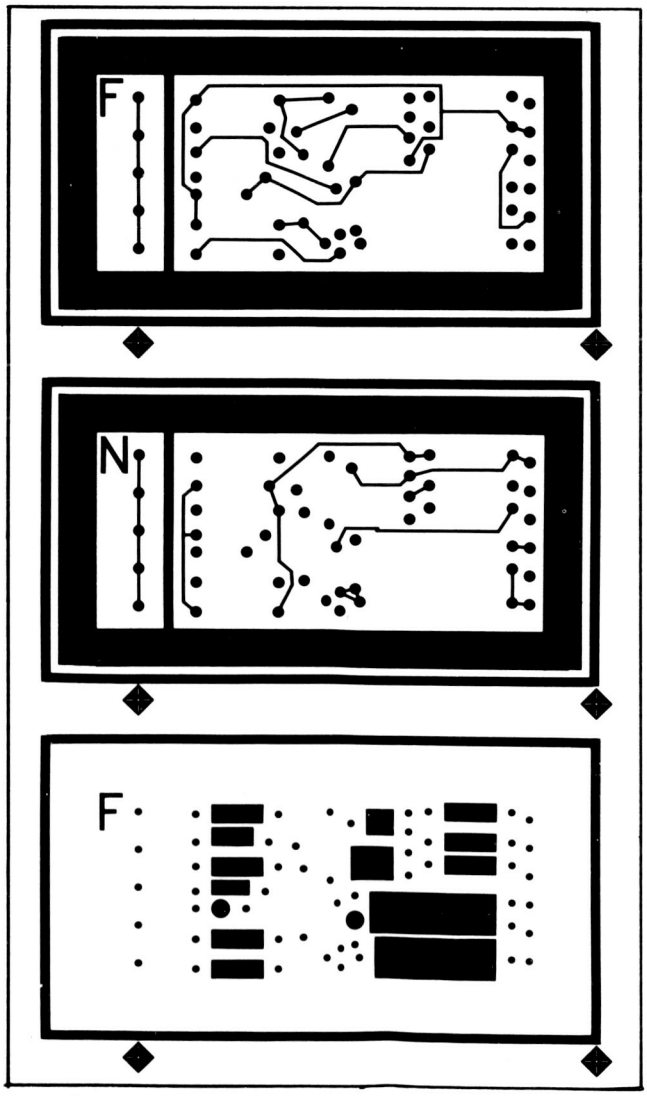
4 Transistor parameters versus temperature



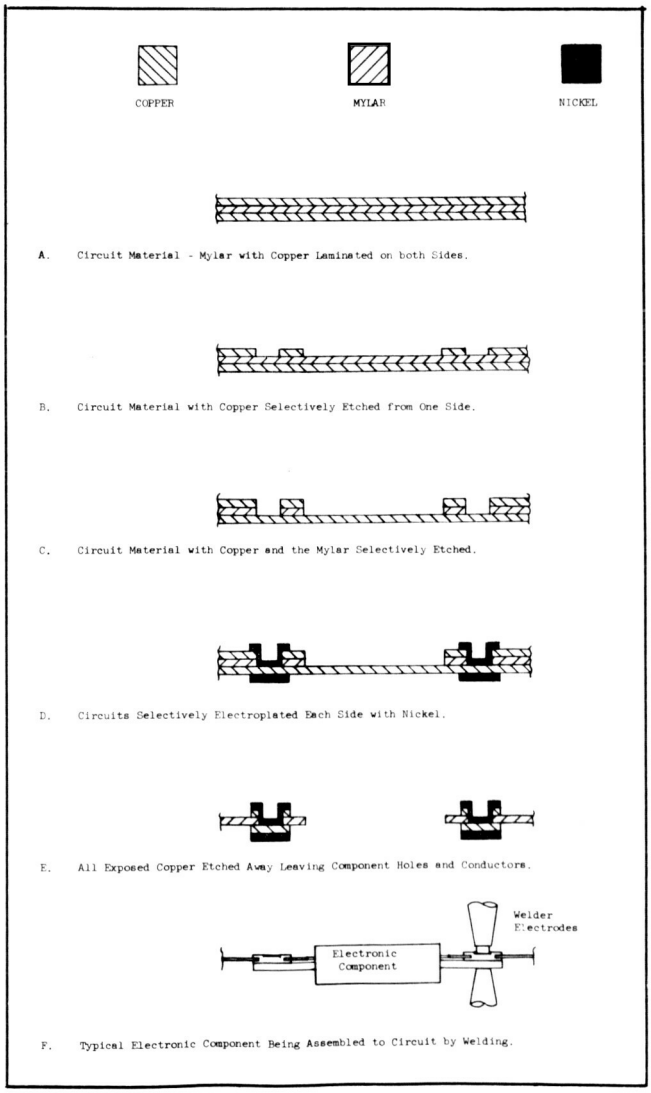
6 Frequency response



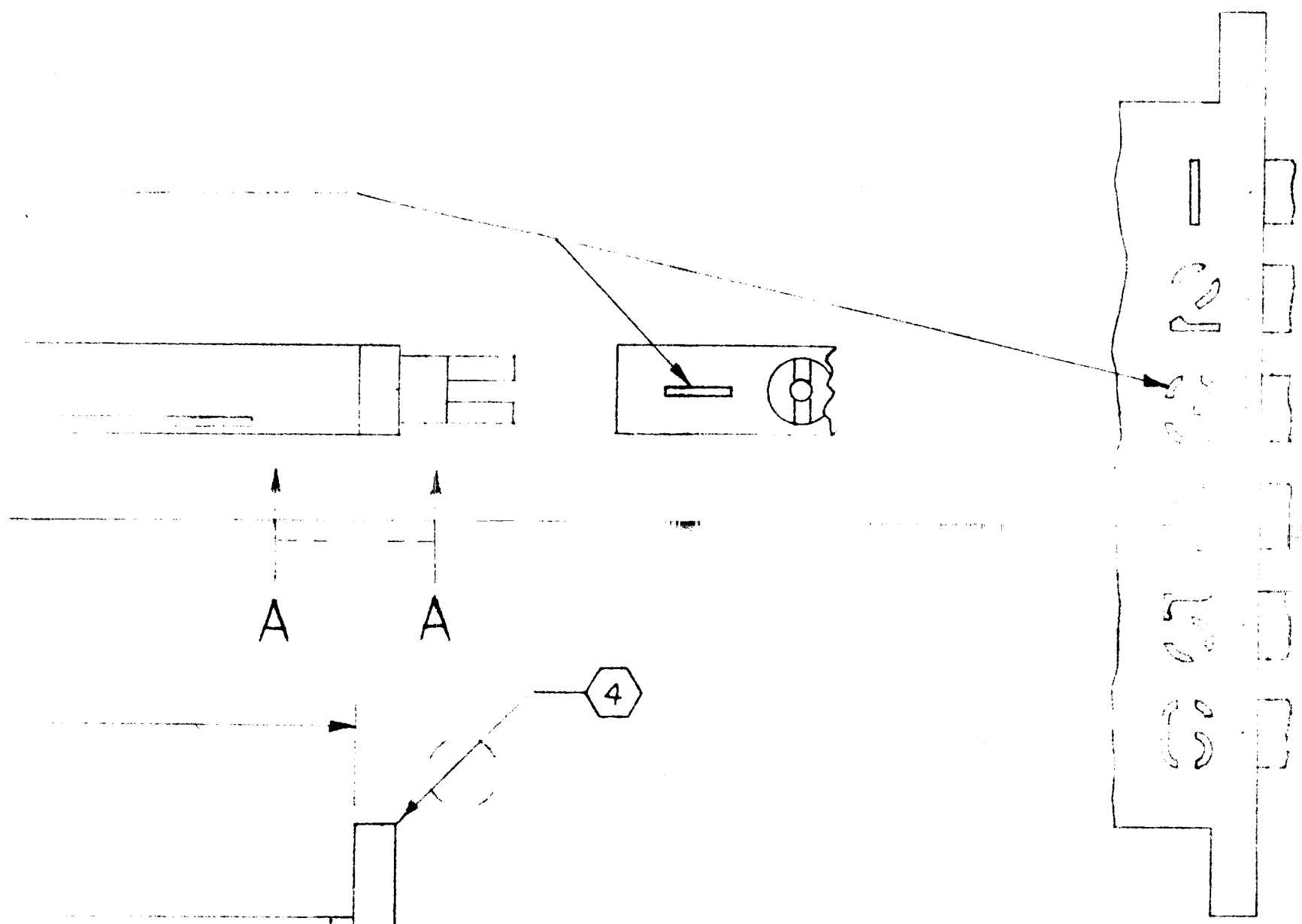
7 Stages in the assembly of the modules

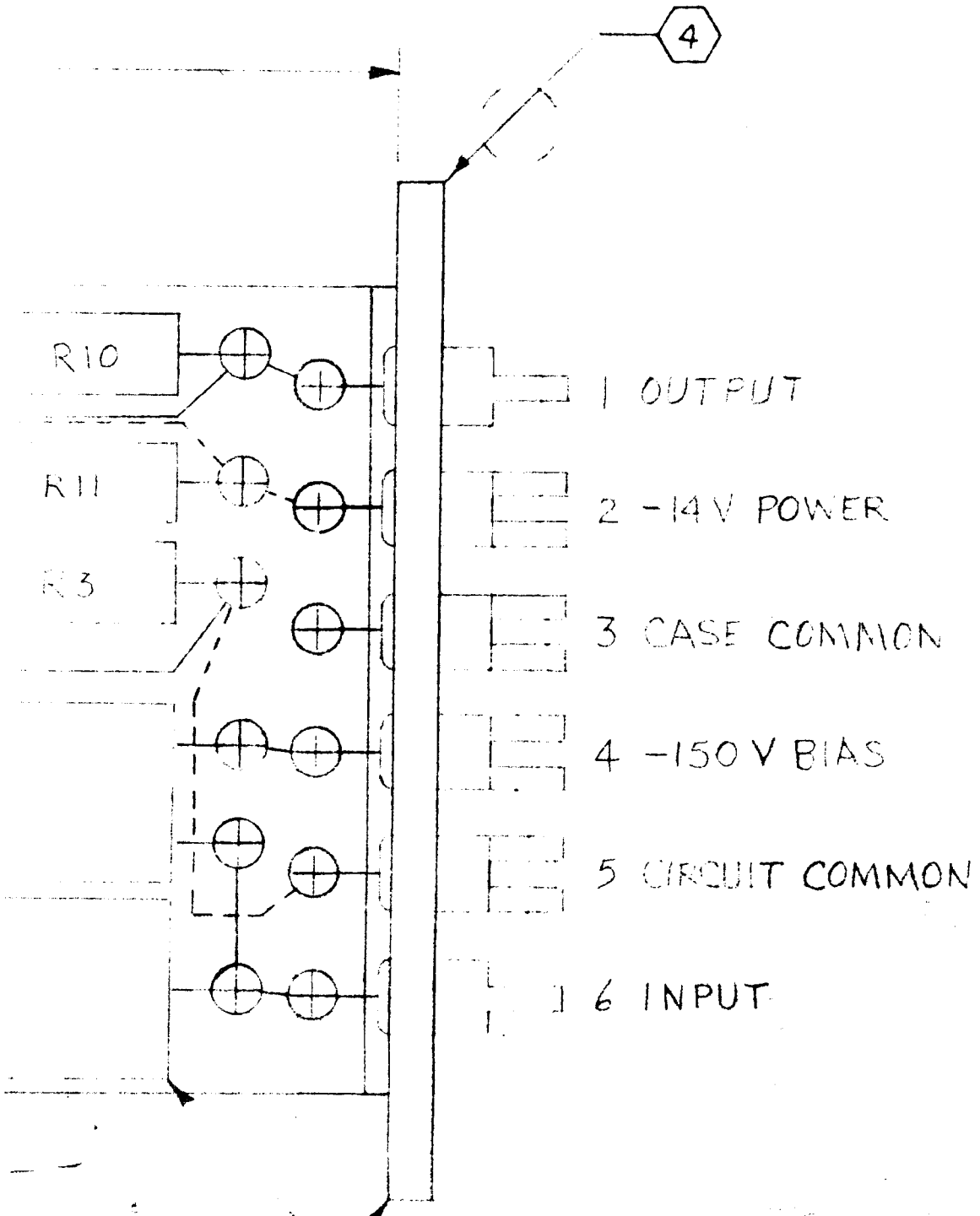


8 Module photo masters

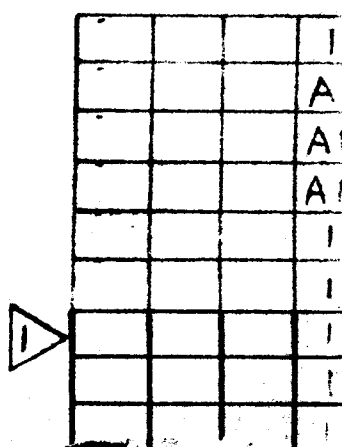


Levels in the fabrication of the printed circuit board


A
A


4
R10
R11
R3
1 OUTPUT
2 -14 V POWER
3 CASE COMMON
4 -150 V BIAS
5 CIRCUIT COMMON
6 INPUT

VIEW A-A


1

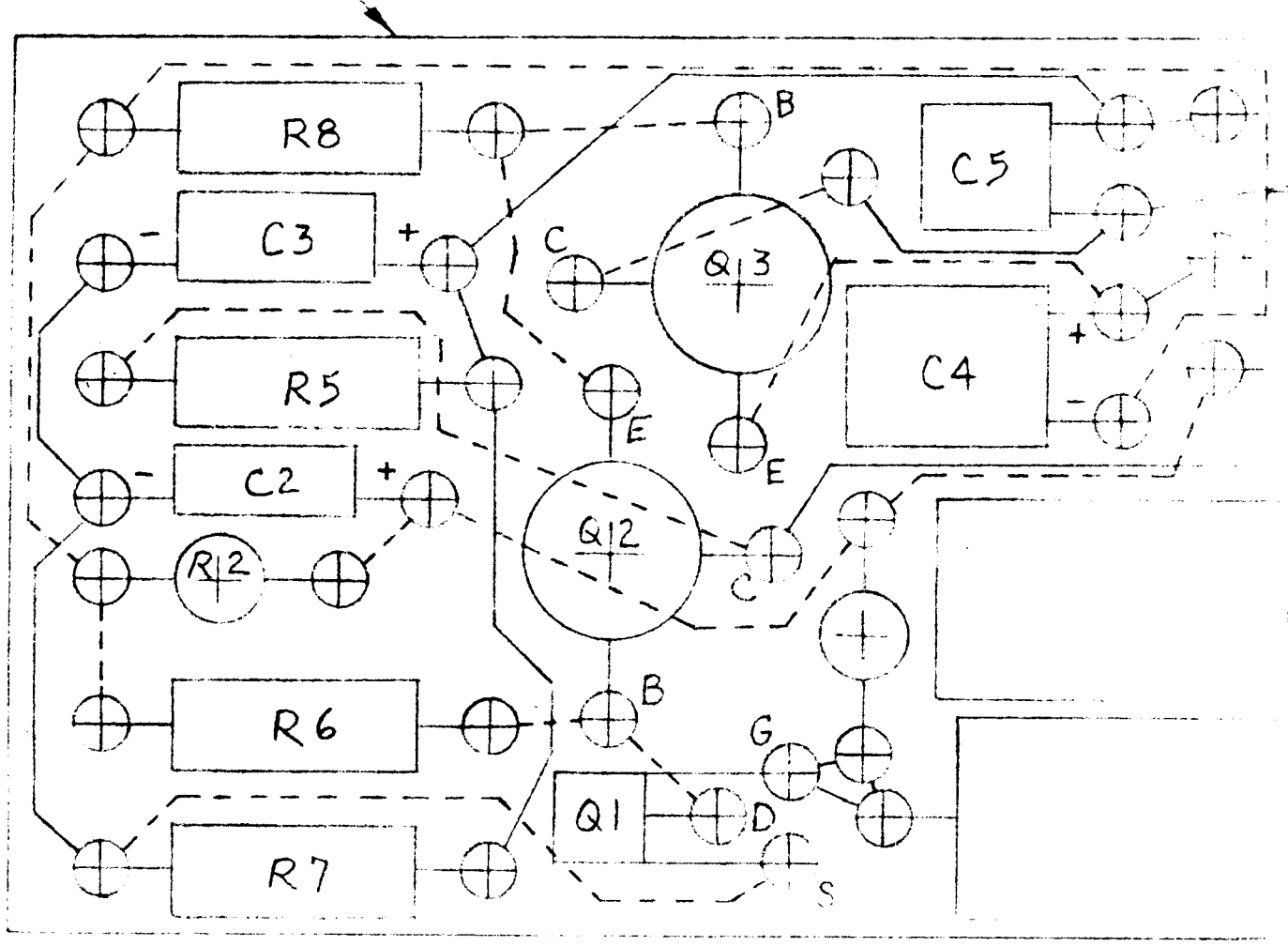
STENCIL APPROX. AS SHOWN .0? HIGH

.118±.002

ENCAPSULATION DIMS.

1.932±.002

.993±.002



REVISIONS

SYM	DESCRIPTION	DATE	APPROVED
A	REMOVED R9 80031 FE 5 21.5 K. ADDED C5. Q1 WAS 07263 SP9954 2N3277. ITEM 5 WAS 18975 CPR349-4 POLYURETHANE FOAM.	4/21/65 4/21/65	[signature] [signature] 4-22-65

	CAPACITOR	96733	RH04CX820K		CERAMIC	82 PF 200 WV
	EPOXY INK	79436	50-700 CAT-L-INK			BLACK
	POLYURETHANE	98795	7-C-23			SPRAY COAT
	EPOXY RESIN	99098	P-37A			MICROBALLOON FILLED
	TRANSISTOR	07263	SP9953		2N3117	
	TRANSISTOR	07263	SP9953		2N3117	
	TRANSISTOR	17856	SU501		2N3578	
	RESISTOR	80031	FE 10 1/10 W		METAL FILM	21.5K
	↓	↓	FE 10 1/10 W		↓	10 K

ORIGINAL NO. 1

			1
			R
			-

QUANTITY

SS.

SS.

ED TO ITEM (3).

SEE ENGINEERING RECORD

TOP DWG

APPLICATION

NOTES: ~

1. ▷1 PARTS TO BE SELECTED DURING ASSY.

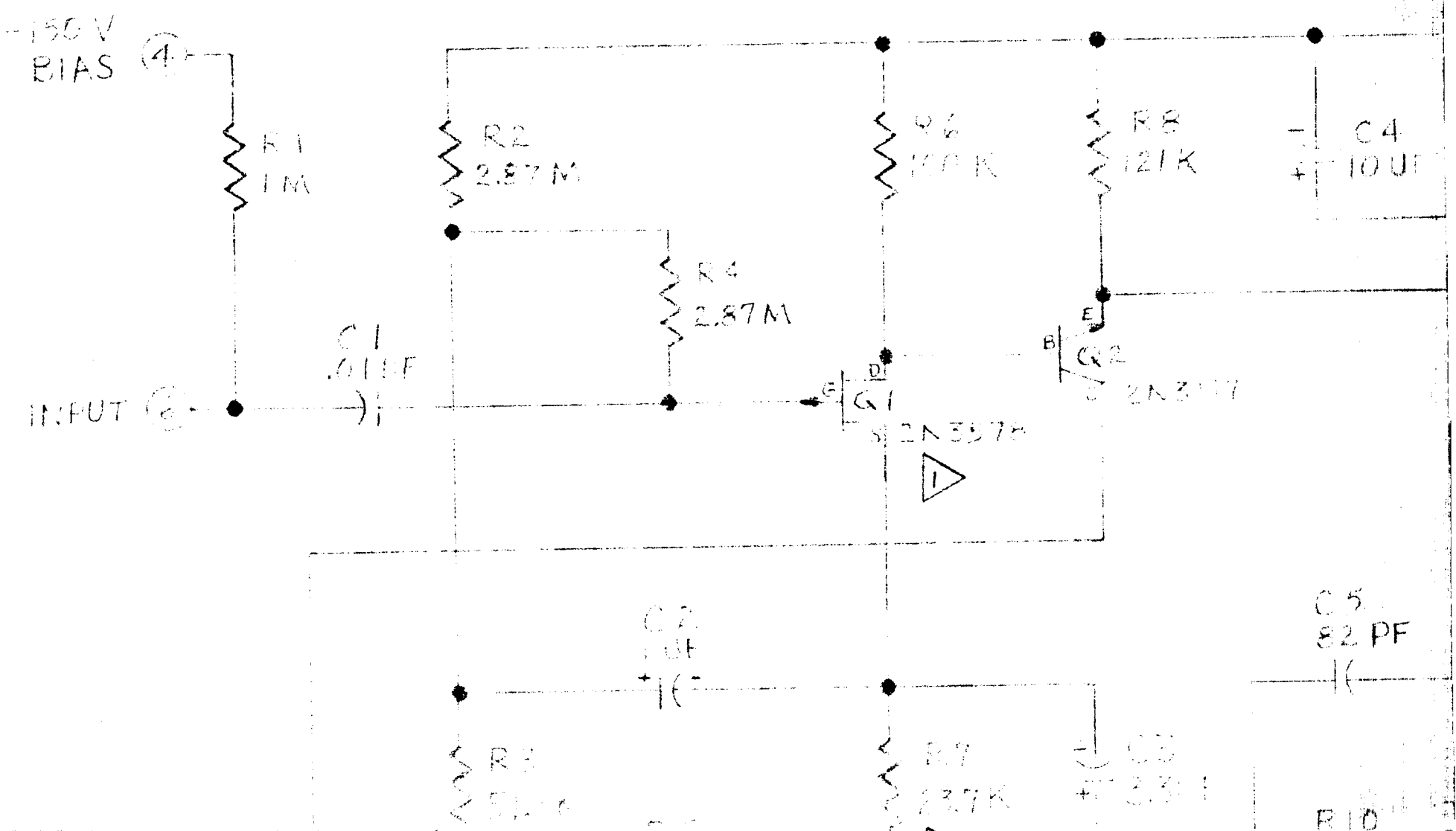
2. ALL COMPONENTS AND LEADS OF ITEM (4) TO BE RESISTANCE

3. EXCEPT TERMINALS, COAT WITH ITEM (6) .001 MAX. THICK

4. ENCAPSULATE TO DIMS. SHOWN WITH ITEM (5).

5. EXCEPT IN TERMINAL AREA, CU/NI PLATE TO .001 THICK

6. STENCIL AS SHOWN USING ITEM (7).


-150 V
BIAS
4
R1
1M
R2
2.87M
R4
2.87M
C1
.01 UF
INPUT
6
G
D
Q1
2N3578
1
R6
R8
121K
C4
10 UF
E
B
Q2
C5
82 PF
R7
C3
R10

QUANTITY

APPLICATION
SEE ENGINEERING RECORD

1. ▷1 PARTS TO BE SELECTED DURING ASSY.

NOTES:

ITEM NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT	PART OR IDENTIFYING NO.	CONTROL NUMBER	SPECIFICATION	REMARKS

LIST OF MATERIAL

MANUFACTURING STD
UNLESS OTHERWISE NOTED
DIMENSIONS IN INCHES
TOLERANCES
.XX = ±.03
.XXX = ±.010

ANGULAR = ± 0° 30'

HEAT TREAT
AL ALY PER MIL-H-6088
STEEL PER MIL-H-6875

MATL SURFACES
✓
PER MIL-STD-10

GOVT		
CHECKER		
PROJ	E. C. Kingsbury	10/16/64
DESIGN		10/16/64
PREP		10/16/64

GENERAL DYNAMICS | ELECTRONICS – SAN DIEGO
P.O. Box 127, San Diego 12, Calif.

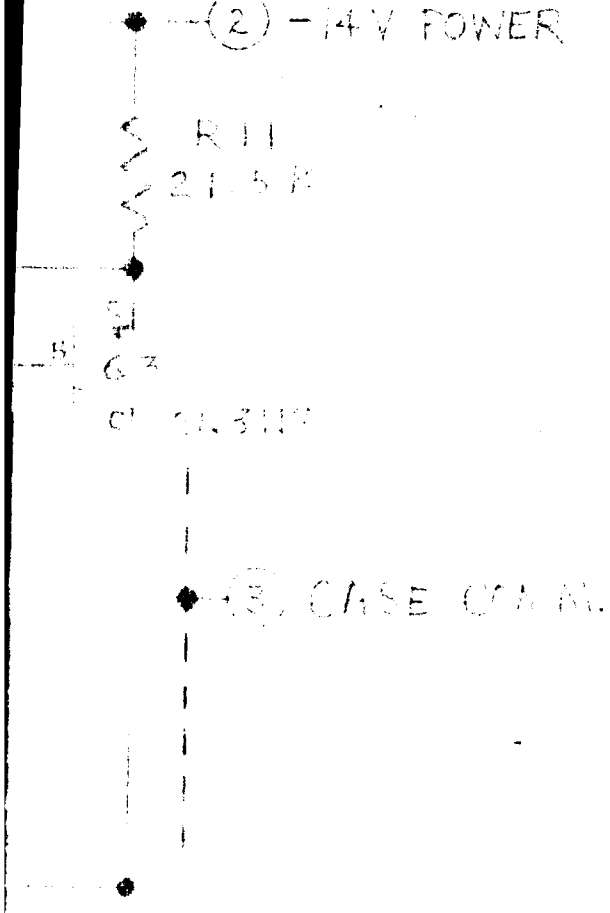
SCHEMATIC DIAGRAM —
PREAMPLIFIER,
INFRARED DETECTOR

CODE IDENT NO.	SIZE	
12436	C	3005601

SCALE — | (R) 11-16-64 | SHEET 1 OF 1

REV SH
A 1
3005601

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
A	REMOVED R9. ADDED C5. Q1 WAS 2N3277.	4/21/65 4/30/65	[illegible]



LAST NO. USED

C 5

R 11 R9 NOT USED

Q 3