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TELEMETRY COMPUTER INTEGRATION SYSTEM

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TELEMETRY COMPUTER INTEGRATION SYSTEM

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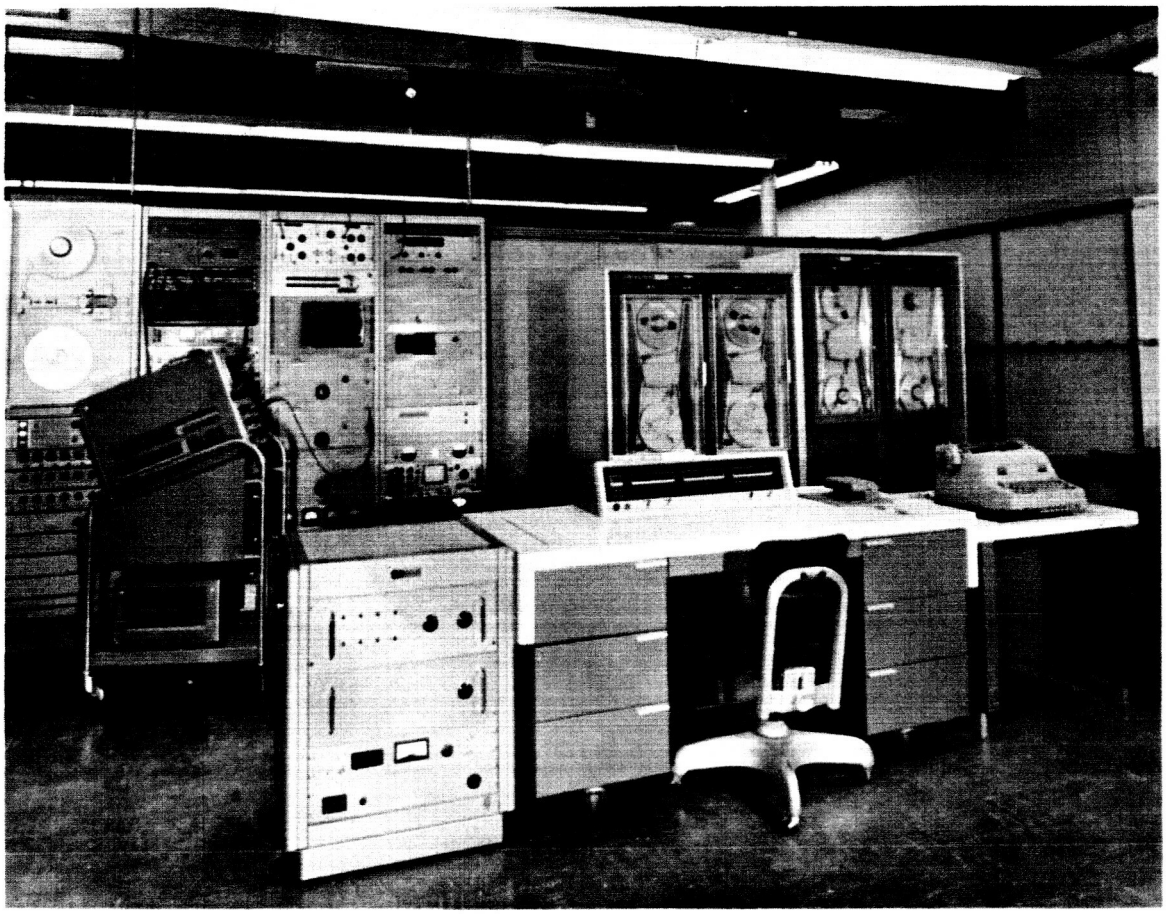
ABSTRACT

The design concept involved in this project considers the feasibility of integrating a high speed, general purpose, small scale, digital computer with a pulse frequency modulation signal reduction and conversion system to obtain the highest quality of intelligence in a minimum period of time.



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SECTION I

INTRODUCTION AND SUMMARY

INTRODUCTION

The Data Processing Branch's Data Systems Engineering Section has completed a design project concerned with the feasibility of integrating a high speed, general purpose, small scale, digital computer with a telemetry signal reduction and conversion system. The computer selected was the Control Data Corporation, CDC 160. The telemetry signal reduction and conversion portion consisted of the Explorer (S-3) Satellite, pulse frequency modulation (PFM), data processor. The time decoder used, converted standard NASA time codes to digital format. The latter two pieces of equipment were constructed at NASA. See Figure 1-1 for graphic illustration of the three parts mentioned.

SUMMARY

In addition to Section I, the background is presented in Section II. The initial and revised design concepts are presented in Section III and Section IV, respectively. Section V contains the details of the technical aspects of the project. The software, or the program integration, is explained in Section VI and Section VII. Finally, Section VIII presents both the specific and general conclusions of the project.

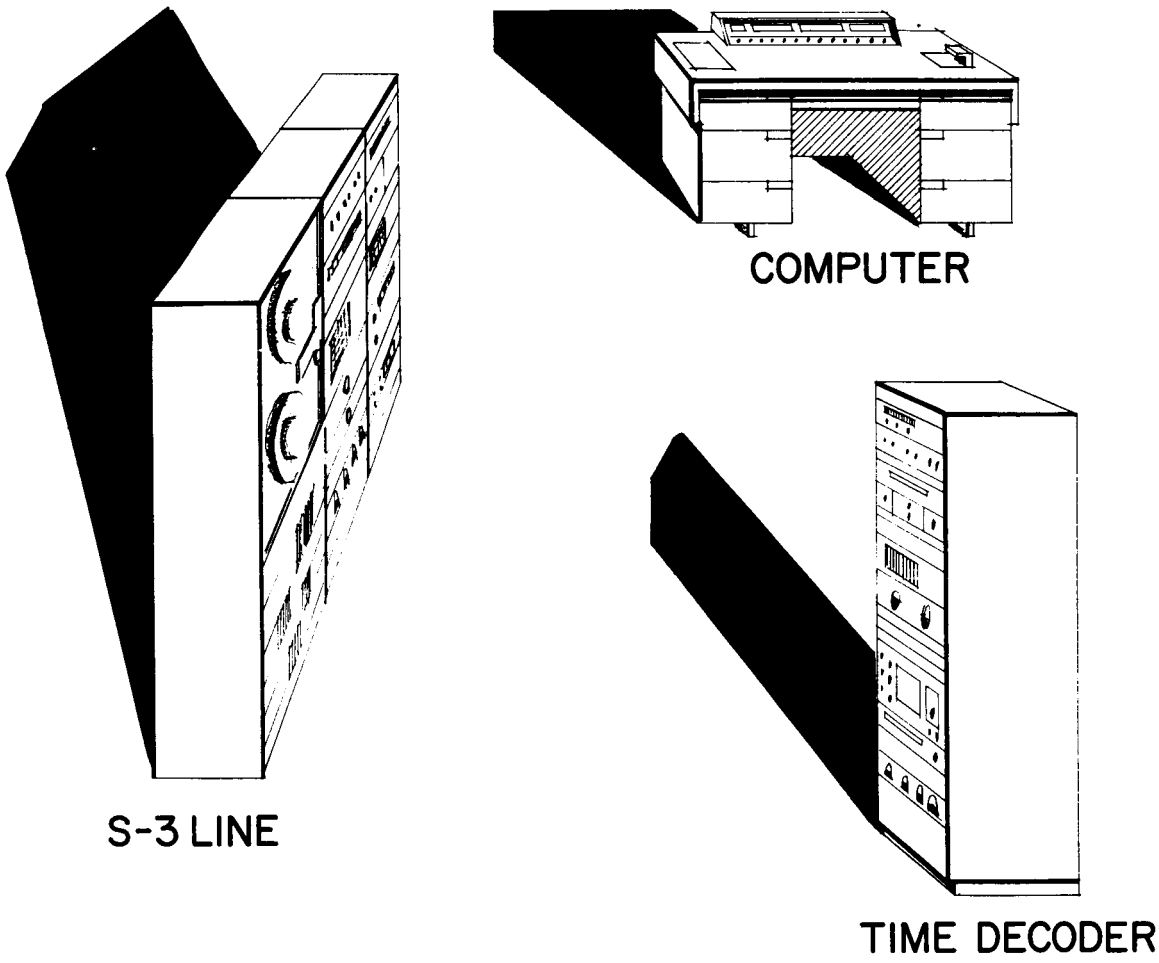


Figure 1-1 — CDC-160, S-3 Line, and Time Decoder

SECTION II

BACKGROUND

The background of the telemetry computer integration project is described below. The basis of the proposed change in design involves the Data Processing Branch's present procedure for processing most of the telemetry information received from NASA's field tracking stations. After a brief description of the procedure, reasons are presented which indicate the need for the enhancement in design of the equipment that is used for current processing of data.

A block diagram of the present data processing procedure is shown in Figure 2-1. The illustration shows the movement of information, i. e., the data flow, as it passes through the signal processing stage to storage and then out of storage for futher data reduction. The dashed lines divide the process into three time periods. The time between the dashed lines is a variable dependent upon scheduling sophistication and the production control of the data processing operation.

The present processing method is as follows. After tape evaluation, the analog tapes received from the satellite data acquisition network are played back and converted from analog to digital information on the telemetry signal reduction line. The digital information is then partially edited and formatted

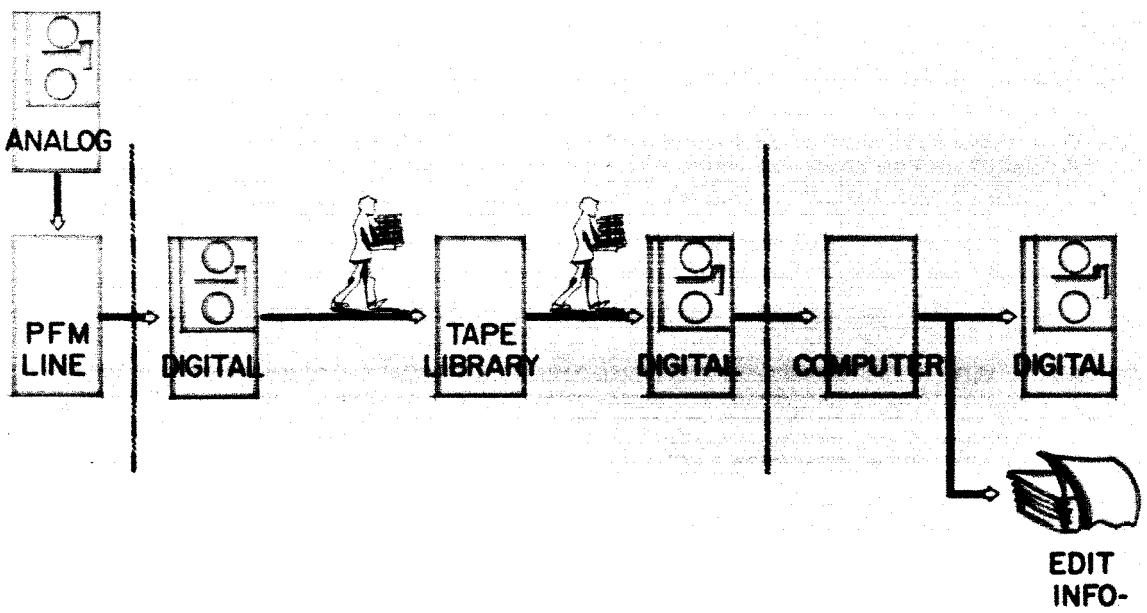


Figure 2-1 — Present Processing Method

by special purpose buffering devices and stored on magnetic tapes. Following this procedure, the tape is further edited and formatted on a medium size, general purpose computer.

It has been observed that the above procedure involves physical handling of data tapes at the times of the analog-to-digital conversion and of computer editing. The procedure requires expenditures of time and manpower that can be saved by taking advantage of the time available during the analog-to-digital conversion periods of reduction. Use of advanced design techniques would accomplish the saving of both time and manpower.

In the procedure for processing current telemetry information, the equipment that performs the digital recording and formatting can be considered as a special purpose computer that has the ability to perform a limited number of functions rapidly. However, the digital information that is recorded by this equipment must be transferred to a high speed, general purpose computer for further editing and formatting. Application of suitable design techniques can therefore introduce an economy of operation in the system. There are many types of general purpose computers that can be integrated into an overall reduction system to accomplish this task. During the time the signal conversion is occurring, other functions can be performed simultaneously. Available time is used and the data processing operation approaches its desired goal of obtaining the highest quality of intelligence in the shortest period of time. The final result is a savings in equipment and in manpower, a considerable reduction in total processing time, and a more expedient and efficient system.

It was with the above-mentioned concept in mind that a program of integrating a computer into a telemetry reduction system was undertaken by the Data Processing Branch. See Figure 2-2 for the proposed equipment relationship for the integrated telemetry computer system.

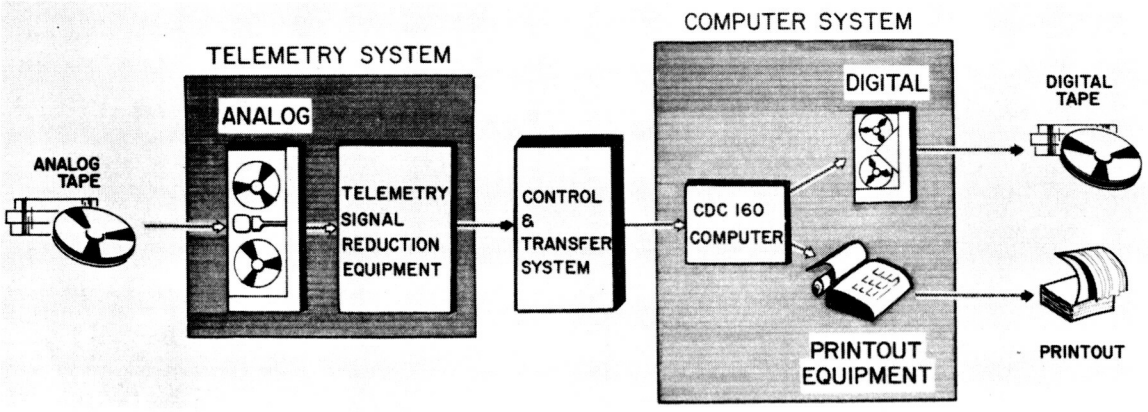


Figure 2-2 — Integrated Telemetry System

SECTION III

INITIAL DESIGN CONCEPT

The initial design concept was based upon economy of construction as a main factor along with the following constraints. No changes would be made to the circuits within the CDC-160 computer proper nor to the external commercial equipment which served as standard input/output devices.

The first prototype was developed around the output storage register of the S-3 PFM telemetry reduction and conversion line. The output storage registers were used as the data transfer elements of the system. A simulator of some complexity was constructed to pass data to the computer at a predetermined data rate. This simulator was designed so that the computer could be used in both a single order progression and in a continuous high-speed operational mode for test purposes.

Various input and editing routines were performed by the computer in periods of several micro-seconds to a few milliseconds. These routines ascertained that the computer was capable of accepting inputs and excuting information checks easily.

The incorporation of an output routine after editing and storing data proved to be unsuccessful. The computer was able to reference and readily dispose of information, but the mechanical and electronic control features of the magnetic tape units were too slow to permit the computer to accept another input word during the time the output routine was occurring. In this case, the use of a single transfer register to transmit information into the computer proved to be inadequate because of a slow tape drive turn-on response. Consequently, the initial design concept had to be reconsidered. The results of continued testing indicated further considerations when using a nonbuffered computer. A computer without simultaneous input-output capability is constricted in its operations by the functions of the external equipment. Even in the initial approach if the desired operations of entering, computing, and passing information had been accomplished successfully, it still would not have been feasible to speed up input data without adding external compensating circuits as well as modifying the program routines.

SECTION IV

REVISED DESIGN CONCEPT

The revised design had to compensate for the limitations imposed by the external equipment in the initial design. To solve this problem, it became apparent that the construction had to be expanded more than originally desired because a different interfacing transfer and control mechanism had to be developed. Since there was no method to temporarily store input data for any time period because the single transfer register had to always be capable timewise, of accepting the next word to be sent to the computer, an interface device that would also accept data for storage was finally decided upon.

The revised design concept provides for less frequent inputs to the computer and thereby increases the time period so that the output of information can be performed with sufficient time left for computation as well as a return to an input mode. This redesign is a more flexible system than the initial design. The sacrifice in the economy of construction and the increased number of information storage circuits that provided more storage was well justified. In the revised design concept, the data input rate can be handled easily and the control arrangements are such that data can be converted at twice the nominal rate. With these improved features, the revised system was more than able to meet the project operation requirements.

The programming was also minimized in the redesign because the program does not have to include routines to compensate for the close timing tolerances that were experienced in initial design. Consequently, it will be easier to test the redesigned system during performance of operational checkouts.

A simulation test instrument was constructed for the initially designed system because of the unavailability of an analog-to-digital reduction line for experimentation. Although the simulation test instrument was satisfactorily developed for its initial application, it was reconstructed to meet the redesign criterion and is far less complex than the initial system. Also, it was reconstructed to contain related computer-simulator control generation circuits. The simulation test circuits are contained with the rest of the interfacing transfer and control circuits in a separate cabinet. It is used as a device to test the system for information, passage, storage register reliability, and control timing.

SECTION V

TECHNICAL DESIGN

INTEGRATED TELEMETRY SYSTEM

Figure 5-1 is a block diagram of the integrated telemetry computer system illustrating how the CDC 160 computer is connected to the telemetry processor. The integrated control and transfer system regulates the data processing flow from the processor to the computer. Its two main functions are to: (1) synchronize the control pulses between the processing equipment and the computer, and to: (2) accept information from the telementry system and hold it until the computer requests it. The integrated control and transfer unit is positioned external to the CDC 160 computer.

The integrated telemetry computer system consists of the S-3 telemetry processing line, the CDC 160 computer with its peripheral equipment, and a binary coded decimal (BCD) time decoder. The main parameters and the essential characteristics of the three subsystems are listed in Tables 5-1 through 5-4.

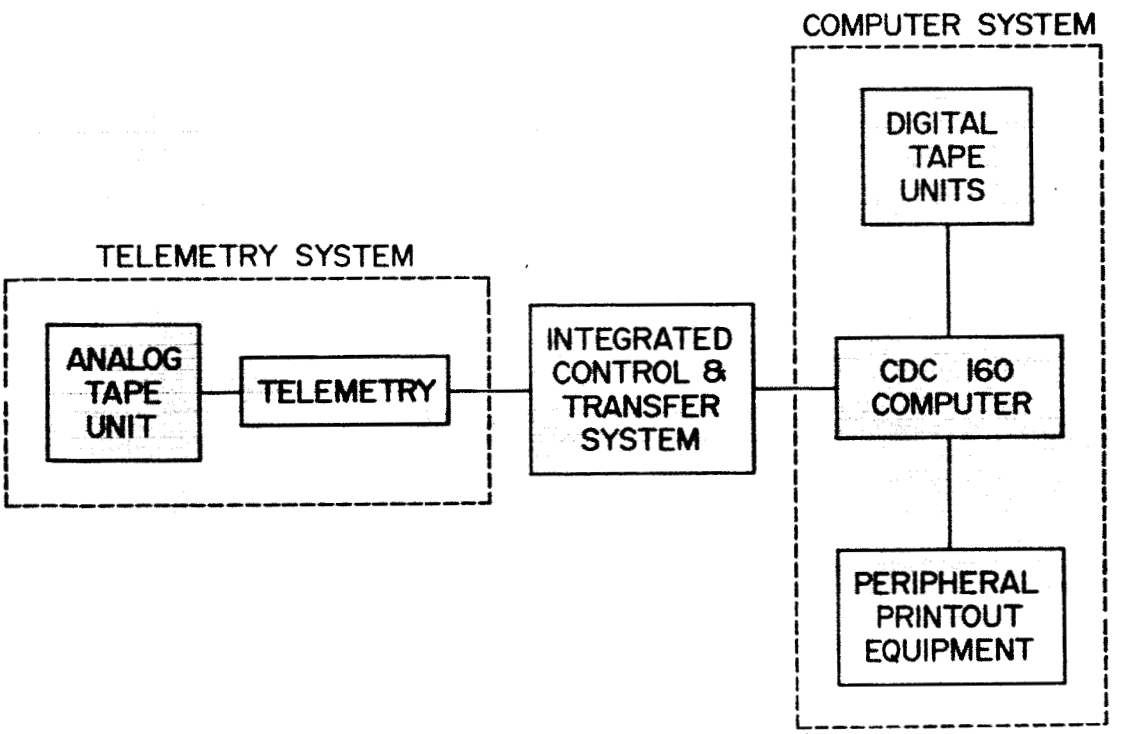


Figure 5-1 — (Block Diagram) Integrated Telemetry System

Table 5-1

S-3 Explorer Satellite Telemetry Processor

1. Processes PFM data, 5kc to 15kc
2. 128 comb filter bank, 114 filters utilized
3. 13 bit digital output register
4. Digital count, 115 maximum
5. Octal count, 700 maximum
6. Most significant bit, bad data flag
7. 16 channel decommutation
8. Data word rate, 20 milliseconds
9. Frame rate, 320 milliseconds
10. Output control signals
    - A. Data present
    - B. Time hold, time statisize
    - C. Time present

Table 5-2

Time Decoder

1. BCD time output used, 4 bits/character
2. 12 time characters
3. 48 bits
4. Time word frozen by time hold signal
5. Time readout initiated by time present signal

Table 5-3

CDC - 160 System

1. General purpose, solid state, computer
2. Run and step modes
3. 6.4 microsecond memory cycle time
4. 12 bit computer word, signed
5. Parallel logic
6. 67 instructions
   - A. Manipulatory
   - B. Arithmetic
   - C. Jumps
   - D. Input/output
   - E. Miscellaneous
7. 4096 word, magnetic core storage
8. Non buffered input/output

Table 5-4

Peripheral Equipment of Telemetry Computer System

1. Four magnetic tape transports - Ampex 163's
   - A. 150 inches per second speed
   - B. 200 lines per inch
   - C. 30 kc character rate
   - D. IBM compatible
2. Soroban, IBM typewriter
3. Ferranti, paper tape reader
4. BRPE, paper tape punch

INTEGRATED TELEMETRY COMPUTER SYSTEM

Figure 5-2 is a general block diagram of the integrated telemetry computer system showing the control and data connection lines between the various subsystems. The main points of consideration for design are presented in Tables 5-5 through 5-9.

The data flow is shown by the heavy black lines in Figure 5-2 and the control functions by the lighter lines. With the exception of the computer which has to communicate bi-directionally, it can be seen that all other data and control paths flow from left to right in the diagram.

The sequence of events up to the interface circuits of the control and transfer subsystem is relatively straight forward. PFM data is reproduced on one channel of the analog tape reproducer and is sent serially, bit by bit, to the S-3 telemetry processing line for conversion to digital form. At the same time, BCD time is read from another channel to the BCD time decoder.

Table 5-5

Timing

1. Input cycle: The computer cycle time is approximately 3000 times faster than the telemetry data rate of 20 milliseconds.
2. A typical, uncomplicated load and store series of instructions can be performed in 28 microseconds. Therefore, information can be moved nearly 700 times between data inputs.
3. No timing constraints are imposed by the computer on the data input.

Table 5-6

Data Input

1. Synchronization pulses are generated every 20 milliseconds for a data word and every 320 milliseconds for frame recognition.
2. Bad data flags are generated.
3. Error possibilities are:
A. Too many data words per frame; seventeen or more. When this occurs the extra words must be locked out.
B. Too few data words per frame; fifteen or less. When this happens, the extra words need to be added to fill out one frame.

Table 5-7

Time Input

1. 12 BCD characters; hundreds of days down to units of milliseconds.
2. Time; transmitted 7.5 milliseconds after the last data point per frame occurs.
3. 48 bits to be transferred each time.
4. Time is transmitted every 320 milliseconds.

Table 5-8

Output From Computer to Magnetic Tape

1. At end of a 960 time and data character input (16 frames), an output is necessary.
2. Timing requirements of magnetic tape transports.
   A. Write time - 33 microseconds per character; total block storage is approximately 33 milliseconds.
   B. Magnetic tape transport turn-on time:
      (1) 20 milliseconds to move off the load point;
      (2) 20 to 35 milliseconds to obtain recording speeds depending on the unit.
   C. Best output time is approximately 54 milliseconds, not considering safety factors or programming extras.

Table 5-9

Computer Constraints

1. The computer places constraints upon the system along with the magnetic tape drives because:
   A. It lacks buffering capability to sequentially interlace input and output cycles at fast data rates.
   B. It must select a piece of external equipment and hold that selection until the input/output process is completed.
   C. No computation can take place when the computer inputs or outputs blocks of data.

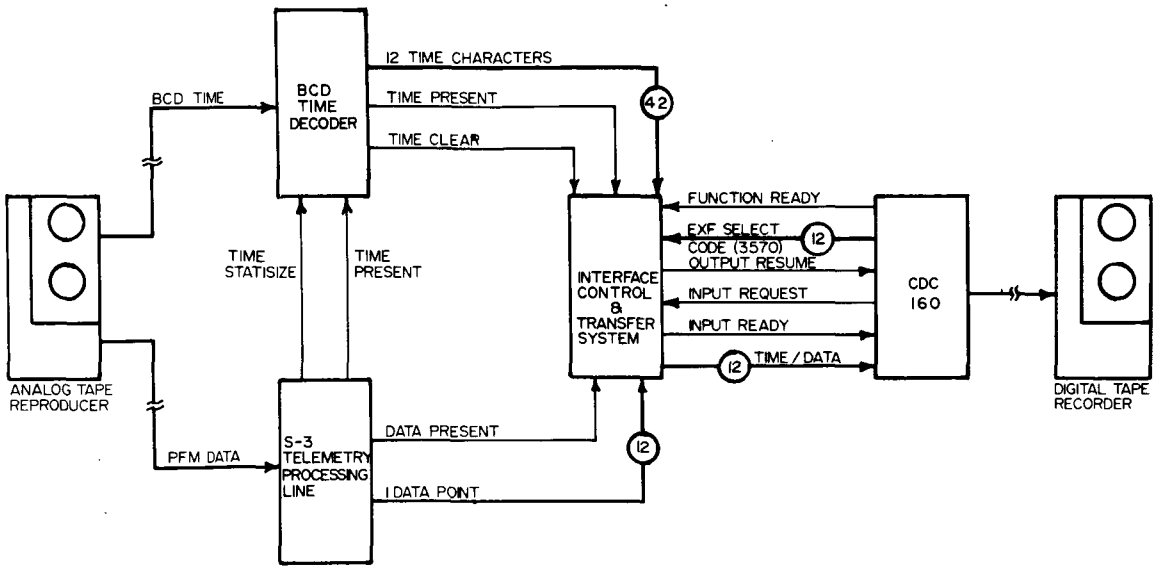


Figure 5-2 — Integrated Telemetry Computer System

Once synchronization is obtained in the processor, the data words are processed by the S-3 telemetry processing line and a digital data word is sent in twelve parallel bits to the interface transfer and control subsystem (ICTS). Each data word is accompanied by a data present pulse to signify its presence in the processor output register. The ICTS does not accept the data words until frame synchronization has occurred.

At sync time the 16th data word of a frame will have been digitized in the telemetry processor. The processor will send a "time statisize" or a "time hold" pulse to the BCD time decoder to "freeze" a time word. Along with it will be a "time present" pulse which is used to generate a "time clear" strobe as well as to pass on through the time decoder to the interface circuits to start a transfer sequence. Forty two bits comprising twelve characters of time are then stored in the ICTS time storage registers for passage to the CDC 160.

The computer takes in the time in four computer words of twelve binary bits. It then takes in four data words which have been stored at 20 millisecond intervals over a total period of 80 milliseconds. The data cycle is repeated a 2nd, 3rd, and 4th time over a frame period of 320 milliseconds. The frame time is the duration it takes for sixteen words to pass through the processor for analog to digital conversion. This insertion of twenty into the computer is the basic cycle and it is repeated sixteen times until 960 time and data characters have been stored and an output cycle is required.

Depending upon the point in time in the processing sequence, either the ICTS or the computer can initiate the transfer between the units. The control sequence

between the ICTS and the computer is started when the computer sends a "function ready" signal plus an "external function select" code of twelve parallel bits (an octal designation). This is the computer's way of isolating the ICTS from other external devices peripheral to the computer.

This prepares the computer input circuits to accept data from the ICTS. The ICTS returns an "output resume" pulse to the computer to notify it that it has acknowledged selection. The computer once again returns a control signal in the form of an "input request." This is examined by the ICTS and if time or data is ready to be transferred, an "input ready" is sent back to the CDC 160 which will then take in twelve bits of information.

The input cycle, once underway, consists of the four time words accepted by the computer with a time limitation dictated only by the amount of program requirements performed by the computer. The time input is followed by the acceptance of sixteen data words in four, 4 data word subcycles. The timing for the loading of the sixteen data words is dependent upon the data rate as well as the internal program considerations. The ICTS collects four data words at a 20 millisecond rate for each input. At the fourth input; i. e., at a total elapsed time of 80 milliseconds the ICTS notifies the computer that data is ready to be sent to it. The computer reads in the four words, performs calculations, and returns to wait for the start of the next data subcycle.

When 960 time and data characters are stored the computer unloads the information in a record of 960 characters on digital magnetic tape. This input-output sequence is continued until processing is ended. Any incompleted block at the end is filled by a program subroutine and is stored on the magnetic tape to complete a record file. The initial control references between the CDC 160 and the ICTS will come from the computer at the start of a processing cycle and after each output record. The ICTS will provide the control enable between input frames while 960 characters are being stored in the computer prior to the output cycle.

Depending upon the mode of the system; that is, whether in the operational or in the run or step mode for the simulator, these signals can appear as both pulse or voltage levels.

INTEGRATED CONTROL AND TRANSFER SUBSYSTEM

Coordination of the data passage between the three major subsystems (discussed in paragraph 5.1) is dependent upon the integrated control and transfer subsystem. Upon development of this subsystem, the S-3 telemetry processor,

the BCD time decoder, and the CDC 160 computer were joined together physically and operationally. A block diagram of the various parts of the integrated control and transfer subsystem is provided in Figure 5-3. The following paragraphs present a general description of the function each part performs.

The ICTS consists of eight important circuit areas. These are designated within the blocks shown in Figure 5-3.

Computer Control Reference Circuits

These circuits serve as the central reference point of communication controls between the ICTS and the CDC 160. All control signals sent from the computer, or received by the computer, pass through these circuits.

Input Clock Gating Circuits

These circuits enable the subsystem control sequence. The circuits generate the clock pulses that initiate the synchronize information flow between the various subsystems and keep count of the correct time and data words that are sent to the computer.

Time/Data Enable Circuits

These circuits provide the proper selection of time and data during an output cycle to the computer to ensure that twelve characters of time are loaded before sixteen data words, or forty eight data characters, are taken by the computer for each telemetry data frame.

Data Input Counter

This device supervises the storage of digital data words sent from the telemetry processor every 20 milliseconds. When four data words have been stored this circuitry notifies the ICTS that it is time for the computer to accept data.

Time Storage Circuits

These circuits accept forty eight bits of time from the BCD time decoder when a time present signal is sent from it. These circuits retain the time until called for by computer. Forty two of the bits are meaningful in the total time

word. The other six bits have no use in the time word structure so they are not sent to the computer. This can be seen at the input and the output of the time storage circuits.

Data Storage Circuits

These circuits store four data words over an 80 millisecond period for transfer to the computer. There are twelve characters consisting of forty eight bits of data.

Time/Data Output Gates

These gates and/or gate combinations transmit time or data to the computer in three character bytes depending on which type of information has been enabled for output.

Simulator Circuits

These circuits provide a duplication of the timing signals used during the operational mode for system testing. A preselected number is duplicated for each data character so bit checks can be made on each stage of the data storage register. The simulator can be controlled for testing at the 20 millisecond data rate or for step testing by computer instruction subcycles.

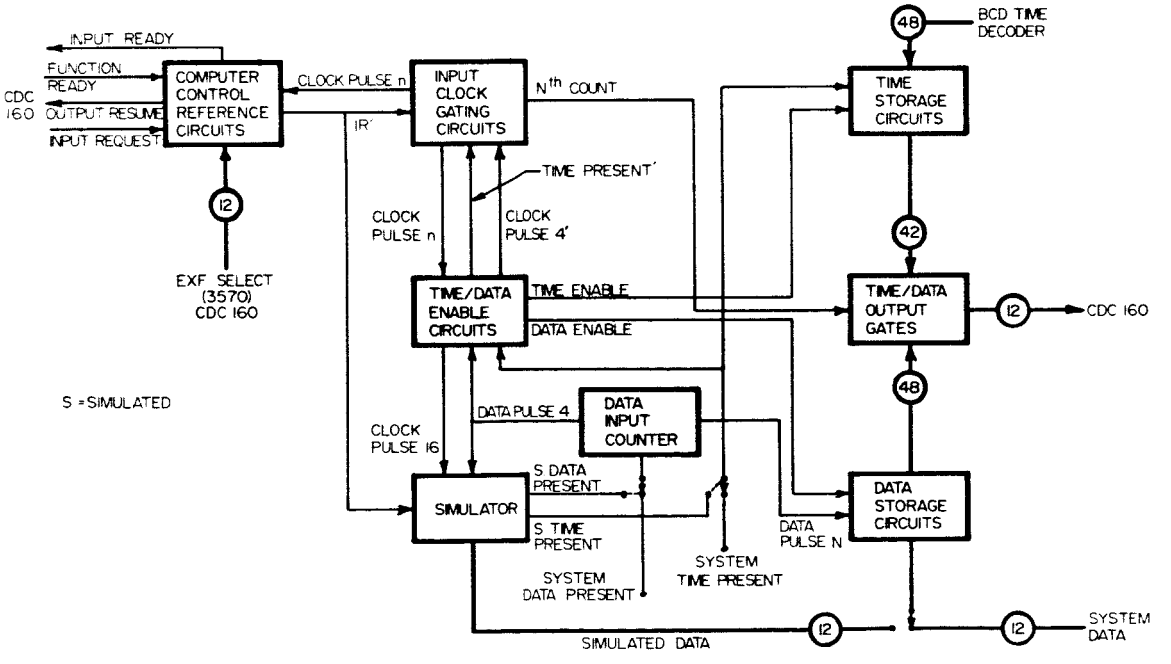


Figure 5-3 — Integrated Control & Transfer Subsystem

DEVELOPMENTAL CONCEPTS

Developmental concepts, including the original data register concept, voltage levels at interfaces, logic levels, computer input and output voltage levels, and other pertinent information is presented in this section. Acceptance and rejection of various concepts are discussed.

A forty two bit time register was designed to hold twelve characters of time and it preserves time until the unload is completed.

To send twelve data bits comprising one data word directly to the computer as soon as it appears on the telemetry processor output lines is not feasible because it takes more than one data word of processing time (20 milliseconds to output). Because of this, incoming data can be loaded over previous data. One extra twelve bit register for storage of a data word increases the time available at output to approximately 40 milliseconds. This concept was rejected because: (1) the output magnetic tape speeds are different between tape units, and (2) the recorder block length would have to be cut in half.

In the data register concept decided upon, a greater storage facility is featured. Four data words are stored in a forty eight bit register during the input cycle. This method of storing at input allows 80 milliseconds for the output cycle. This is sufficient time for a full block output and for a return to the input cycle. The time and data transfer cycles can also be controlled by the same count sequence as follows: (1) Four time words to the computer, and (2) four data words repeated four cycles for a total of sixteen data words.

The S-3 processor, the BCD time decoder, and the interface transfer and control system were constructed with Packard-Bell digital logic circuits. The circuits were 200 kc and/or logic. Voltage references to and from the computer were satisfied by the use of CDC computer logic output cards. The Packard-Bell logic voltage levels are 0 volts for a logical zero and -12 volts for a logical one. The computer input/output logic levels are zero volts for a logical one and -16 volts for a logical zero. The computer output cards perform the necessary inversion for signals moving in both directions. Resistive loading of 2.2 kilohms were placed at the junction of the computer output control lines and the input lines to the interface circuits for voltage attenuation. Diode coupling was used for isolation between the computer input data lines and the output buffer gates from the interface circuits.

The use of sensing and acknowledgement circuits were considered to be unnecessary for the system because there can be no delay in the established throughput rate once the processing cycle starts. This eliminates extra circuits that would only be appropriate for a buffered computer with a multi-flow servicing problem.

No BCD to binary converter circuits were developed for the time or data inputs to the computer because a reconversion process would have been needed for the time and the data did not warrant it.

MODES OF OPERATION

The integrated telemetry computer system has three modes of operation; the system run mode, the simulator run mode, and the simulator step mode. They are discussed in the next three paragraphs.

System Run Mode

This mode is for the system operational process. The computer performs at its optimum cycle speed of 6.4 microseconds as it accepts, processes, and outputs the converted time and data information. The throughput rate of the system is determined by the input data rate, which for this design configuration is 20 milliseconds.

Simulator Run Mode

The simulator run mode is used for dynamic testing. In this mode, the control, timing, and transfer circuits are tested at the same data rate as the system when it is processing information. The data is repetitive for all characters in a frame. Sequencing is initiated by the computer. The simulator isolates the processor as a source of error, and also the time decoder, if desired.

Simulator Step Mode

The simulator step mode is used for static checks. Its primary function is to check the contents of the transfer circuits storage registers. Level setting on the control elements are also tested. The simulator step mode is also used to sequentially step through the computer instructions that are necessary for communication between the computer and the integrated transfer and control system.

SECTION VI

PROGRAMMING REQUIREMENTS

Following are the program requirements for the system while processing S-3A data tapes for basic buffer duplication. The computer is required to accept twelve characters of time at 320-millisecond intervals, constituting four time words. The computer is also required to accept one character of data every 20 milliseconds. Another requirement is that the computer must output a 960 character block approximately every 5.1 seconds. The computer is required to enter a BCD zero as well as bad inputs into three BCD characters.

Following are the operations the computer performs according to or beyond basic requirements.

1. It accepts twelve time characters at 320 millisecond intervals.
2. Performs BCD-binary conversion on the milliseconds of time.
3. Separates time words into twelve characters; program multiplexing is used for this.
4. Corrects for BCD zero on time inputs.
5. Accepts four data words every 80 milliseconds; these are four 12-bit words.
6. Separates data words into three characters; program multiplexing is used for this.
7. Corrects for BCD zero on data inputs.
8. Outputs 960 character blocks of information.

In addition to the performance of the above requirements, the following quality control functions are also performed according to or beyond basic specifications.

1. Performs a time differential check on milliseconds of time.
2. Flags bad time.
3. It stores initial time.
4. Limit tests for bad data words.
5. Flags bad data words.
6. Counts bad data words.
7. Counts frames of data.
8. Performs quasi-clock search-a complex operation.
9. Extracts quasi-clock information.
10. Performs RIDL cycle search-a complex operation.
11. Extracts RIDL cycle information.

APPROXIMATE TIMES OF PROCESSING SUBROUTINES

Time

Input consisting of 12 time characters takes approximately 2 milliseconds (4 time words). The BCD to binary conversion takes 2.8 milliseconds, but can be changed to approximately 300 microseconds. The Δt check takes approximately 220 microseconds. The Ti storage takes approximately 1.7 milliseconds to perform.

Data

1. Input rate for three data characters - 1 data point
   - Bad data point ..... 280 ms
   - Good data point ..... 500 ms

2. Output rates
   - Computer 1 character ..... 12.8 us
   - Magnetic tape write per character ..... 33½ ms
   - Total 960 character write ..... 33 ms
   - Tape turn-on time ..... 20 ms

   Total output time ..... 53 ms

RIDL Cycle

Switches in and out during every frame and tests for values. 40 ms maximum
12 character time transfer ..... 1.2 ms
Quasi-clock, missing data points/RIDL Cycle, missing frames/RIDL Cycle ..... 400 us
Data point 15 ..... 53 us

Total time ..... 2.17 ms

Quasi-Clock Cycle

The composite estimate at maximum number of sequences ..... 1.5 to 2 ms

REMAINING SUBROUTINES

The remaining items of the test that are not performed were previously done on the IBM 1401 and 1410 quality control checks of S-3A but could have been included in the program. They were:

1. The sun aspect routine (channel 0 and channel extractions).
2. The RIDL Cycle Δt could have been changed from a millisecond conversion, which was programmed for S-3 Quality Control Program. This would add a BCD - Binary conversion of (minutes and seconds) and a summation of differences; this runs the binary bits count up to 21; and it has to be converted back to BCD characters after processing ends.
3. Percentage of bad data words/good data words; this is a post-online operation.

PROGRAM ASPECTS

The software or program subroutines performed the following functions during the data flow process:

1. Input and storage of time and data.
2. Data flagging ordinarily performed on special purpose equipment.
3. Quality checks performed during subsequent computer operations.
4. Determination and extraction of sub-commutated data cycles performed during post-processing computer operations.
5. Output editing and formatting of time and data.
6. Output editing of quality control and extraction of super-commutated data for specific experiments.
7. Program "housekeeping" to retain control and organization of the data flow process.

These functions are shown according to their sequence of occurrence in the program flow diagrams.

PROGRAM FLOW CHARTS

The flow charts of the integrated telemetry computer system are presented in the following order: The general data flow, general throughput buffer mode, ID subroutine, time subroutine, data subroutine, RIDL cycle subroutine, quasi-clock subroutine, file stop time and block fill, and printout routines.

Time and Data Processing Sequence

The programming for the computer integration project was carried out as development progressed. There were different stages of program construction that required consideration. First, the basic subroutine called for an input of a twelve character time word followed by sixteen, three character, data words. This arrangement was repeated for sixteen time frames until a storage block

of 960 characters was accumulated. At the completion of the block storage, an output of all 960 characters to magnetic tape was required. This basic throughput mode is shown at the top of Figure 6-1.

Construction of the integrated telemetry computer system was based on a twelve character BCD time word to be read in before data was stored. After reading in the time word, the computer was constrained by the system to accept four groups of four data words at intervals of 80 milliseconds rather than sixteen data words at 20 milliseconds intervals each. The time read-in intervals were spaced at the data frame rate of 320 milliseconds. An output block of information occurred every 5.12 seconds.

The Identification subroutine at the bottom of Figure 6-1 is performed prior to processing of tapes, and the ID information will always be the first block on any digitized tape just as it would be done in the current process.

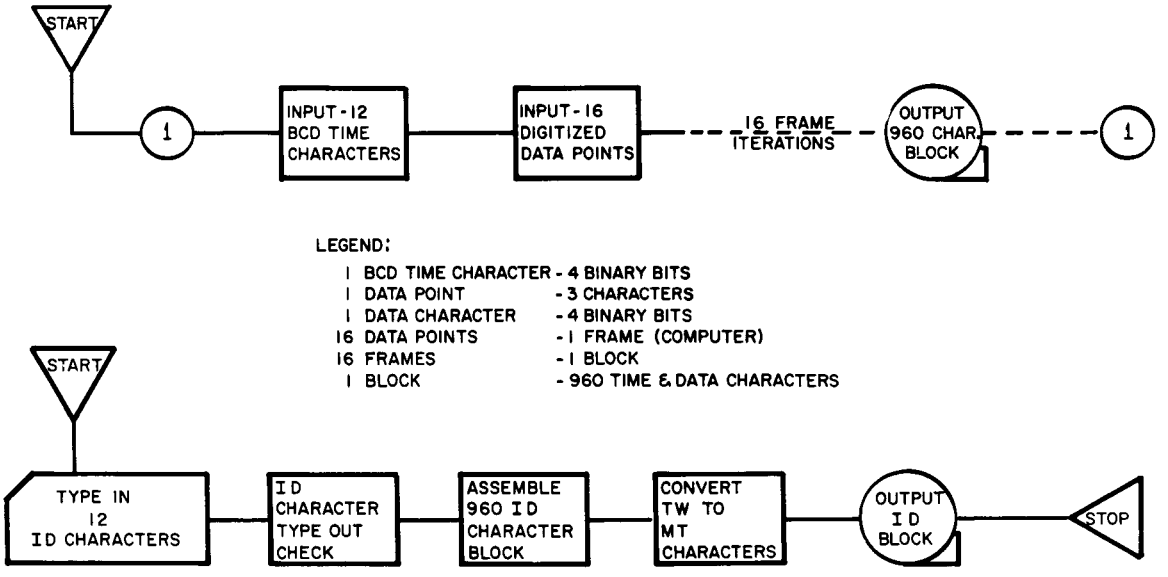


Figure 6-1 – Time & Data Processing Sequence (Buffer Throughput Mode) And ID Subroutine

Time Subroutine Flow Chart

Acceptance from an input source and the checking of time within the CDC 160 computer is performed as shown in the time subroutine flow chart. (Figure 6-2)

Whenever a frame of data is to be inserted into the computer, it is preceded by a twelve character time word. When the time word is stored in the time storage register of the interface control and transfer system storage circuits,

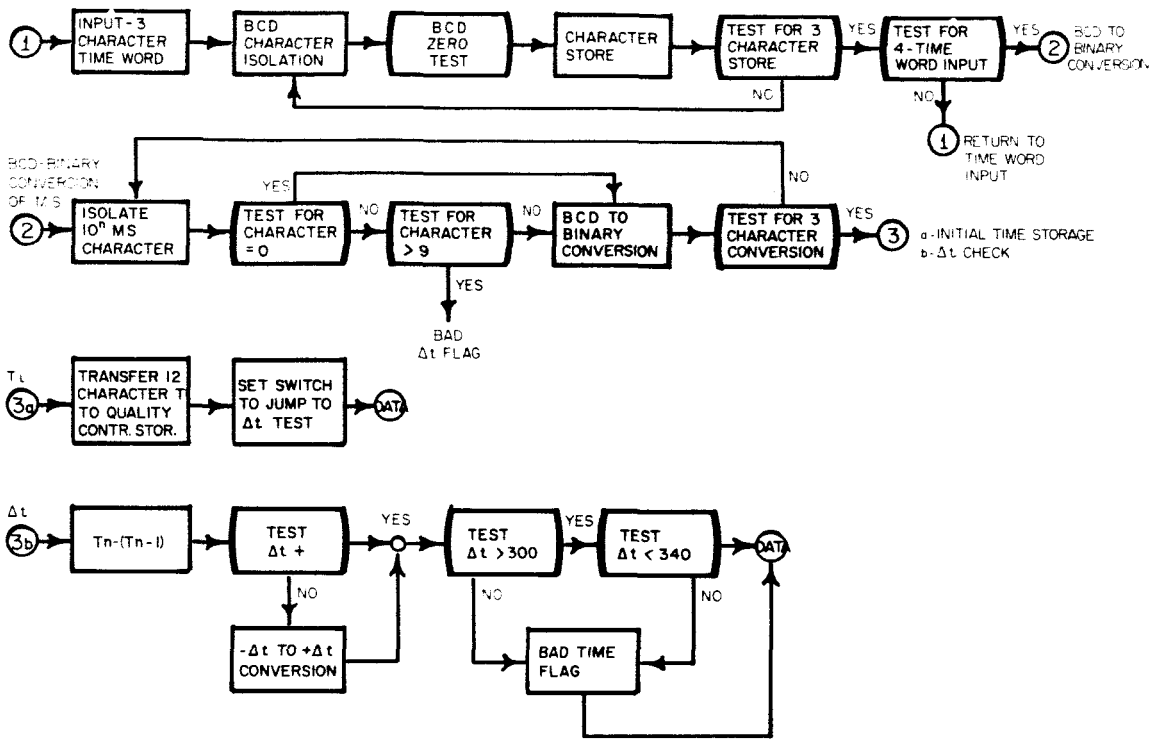


Figure 6-2 — Time Subroutine Flow Chart

a time present signal is generated that notifies the computer to take it. The CDC 160 then accepts the twelve characters in three binary coded decimal character words. Once in the computer, each of the characters is isolated and a test for a binary coded decimal (BCD) zero is made. No provisions were made in the circuits of the system to convert a binary zero to a BCD zero. This was a hard-wire function of the special purpose format buffer used in the processing lines as shown in Figure 2-1, Section II. The computer is called upon to handle this test through it program structure. This provision is necessary for later parity checks and character translations.

The program then stores a character, tests it to find out if three characters have been checked and if not, repeats, the three character strip-out. Afterwards the program tests for four time words; returning to the input until a complete word is loaded.

The next task the computer performs is a conversion of the millisecond portion of the time word from three BCD characters to a twelve bit binary word preparatory to a quality check of the time differential (Δ t) check between two frames of data. The BCD - binary conversion is shown between program connection points 2 and 3 of the time subroutine flow chart. The program first determines the characters by powers of ten. It tests the extreme digits, 0 and 9, of

the decimal radix and converts each BCD character to a binary representation. A three character test follows, and is necessary to provide for a summation of characters for units, tens, and hundreds of milliseconds.

Once the conversion is completed the computer has to ascertain if the time input is the initial time transfer of the production run, or subsequent ones. If it is the initial time (Ti) then no millisecond check can be made since no 320 millisecond interval has passed. The computer program then performs a switch routine to allow Δ t checks for any following time transfers and passes to the beginning of the data input subroutine.

For all other time inputs, the time subroutine jumps into a Δt check. In the test the computer subtracts the previous time input (tn - 1) from the current time input (Tn). A check is made for a positive or negative differential to account for a millisecond update greater than 1000 which will appear as a lesser number, since 999 is the highest possible millisecond count. If this is the case, a program adjustment is made and then a limit check is performed to determine if the time differential is 320 milliseconds plus or minus 20 milliseconds. This is done by testing the lower limit at 300 milliseconds and the upper limit at 340 milliseconds. If the difference exceeds these limits, a bad time flag is placed in the second time word in storage. Housekeeping resets and relocations are performed at the end of each time pass prior to entering into the data subroutine.

Data Subroutine Flow Chart

The subroutine for the collection and storage of data would be a simple one if no interruptions for special experimenter extractions were made. In a strict data input routine (and this was the case for the preliminary program efforts) the data would have been brought in and stored. The program would have tabulated data points for the output cycle and returned to a time input or gone to an output routine when a block of 960 characters had been filled. As can be seen in the data flow chart (Figure 6-3), this was not the case. The data inputs necessitate several checks similar to those performed on each time word. As each data word arrives in the computer, it is tested for an upper limit to determine its worth. If it is not valid, a bad data word flag is placed into character storage, this being repeated three times in a data word. The number of bad data points are accumulated for later editing and quality control features. When the data word is acknowledged to be valid, each data character is masked out, a BCD zero test performed on it, and it is stored into the 960 character block storage. After each character store, a test is made to make certain the characters of the word have been placed in memory. When this is completed the computer then brings in the next data word.

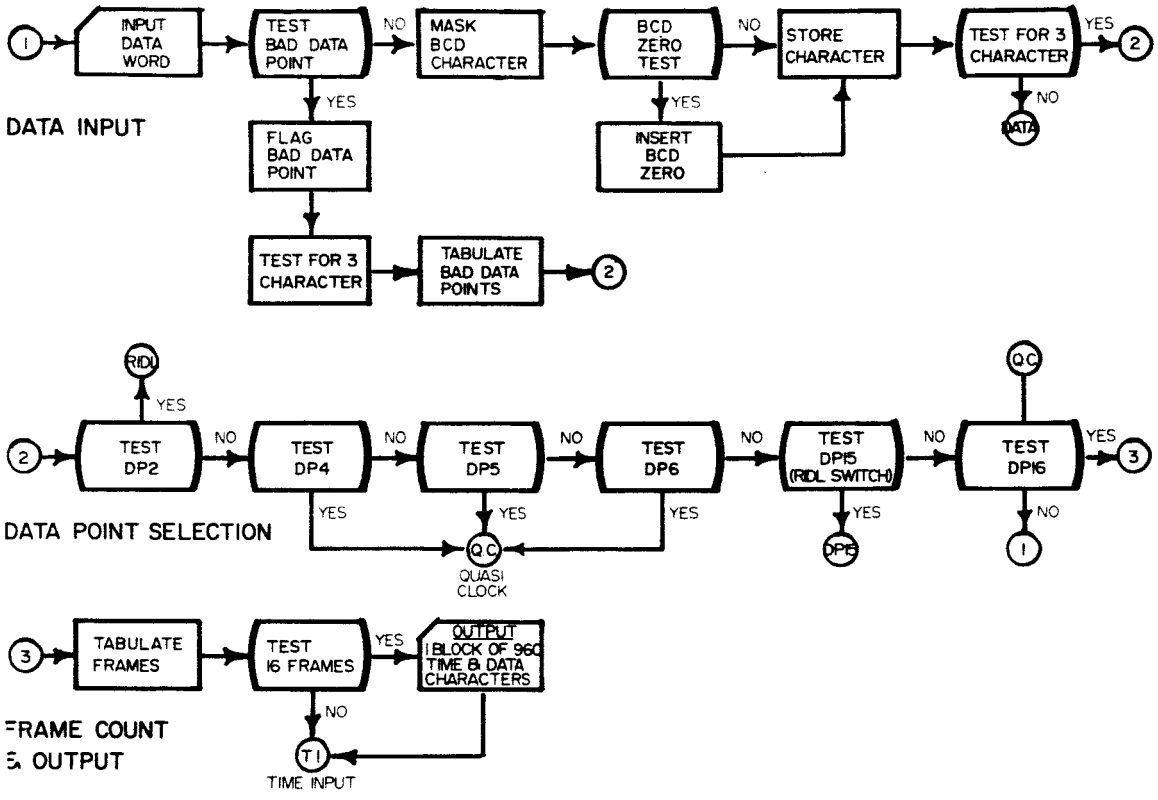


Figure 6-3 — Data Subroutine Flow Chart

Relating the program method of handling each data input to the external storage; it is irrelevant to the computer in this application as to whether or not it takes in sixteen data words in blocks of four from an external register or if it accepts them one data word at a time. The only difference in operation is that the computer can operate more expediently on four data words and consequently wait longer for more data inputs. In either case as was pointed out in the technical considerations involving redesign, because of output limitations, the requirements for checks at input involve very little time compared to the time interval between data words. The programming discussed is blocked out between data entry point 1 and point 2 of the flow chart.

Had no program effort been involved to demonstrate how later computer work could be accomplished during the digitizing phase of production then the data subroutine would have been terminated by the subroutine shown starting at the point 3 of the flow chart. This is the frame count and output program. It tabulates the number of frames accepted by the computer for future reference and tests for storage of sixteen frames, consisting of 960 time and data characters. If less than sixteen frames are stored, an incomplete block is signified and control is switched back for another frame cycle starting with a time input.

When the block is determined to be filled an output commences. A block of information is sent out for recording on digital magnetic tapes. At the completion of the output cycle, the program returns to the time input subroutine.

Moving back to the data subroutine flow chart at the point 2 input for data word selection, it can be seen that a number of auxiliary programs exits have been inserted. This is the method used for extraction of experimental information pertinent to given channels. Provisions have been made to bypass individual experiments if they are not recognized. This causes the program to branch off to an auxiliary path and to continue on through the data flow previously mentioned.

As each data word is loaded into the CDC 160, a test is carried out to determine at what point in a frame it is located. Data word 2 recognition calls for a branching out, to search for supercommutated data used for an experiment designated the RIDL cycle.

Data words 4, 5, and 6 are used together in the determination of another experiment called a Quasi-Clock cycle. The 15th data word is also recognized in conjunction with the RIDL cycle test. Data word 16 is used as the key for determining frame and block counts.

No detail will be spent in explaining the nature of the experimental data in the extraction programs. The emphasis will be placed on what the requirements are and how the computer was programmed to obtain the data.

RIDL (Rearch Industry Defense Laboratory) Cycle

The requirements for obtaining desirable information are as follows:

1. Check each frame for D. P*. 2
2. Test for D. P* 2 = 200
3. Test for 8 D. P. 2's = 200
4. Test for D. P. 2 = 400
5. Obtain RIDL cycle time
6. Count frames per RIDL cycle
7. Count 8 - D. P. 15's
8. Store 8th D. P. 15

In satisfying the above requirements, the computer program is required to perform a number of complex program switches. A number of supplementary functions are also performed. Referencing the RIDL cycle subroutine flow chart, (Figure 6-4) the program first tests for D. P. 2 after branching out from the

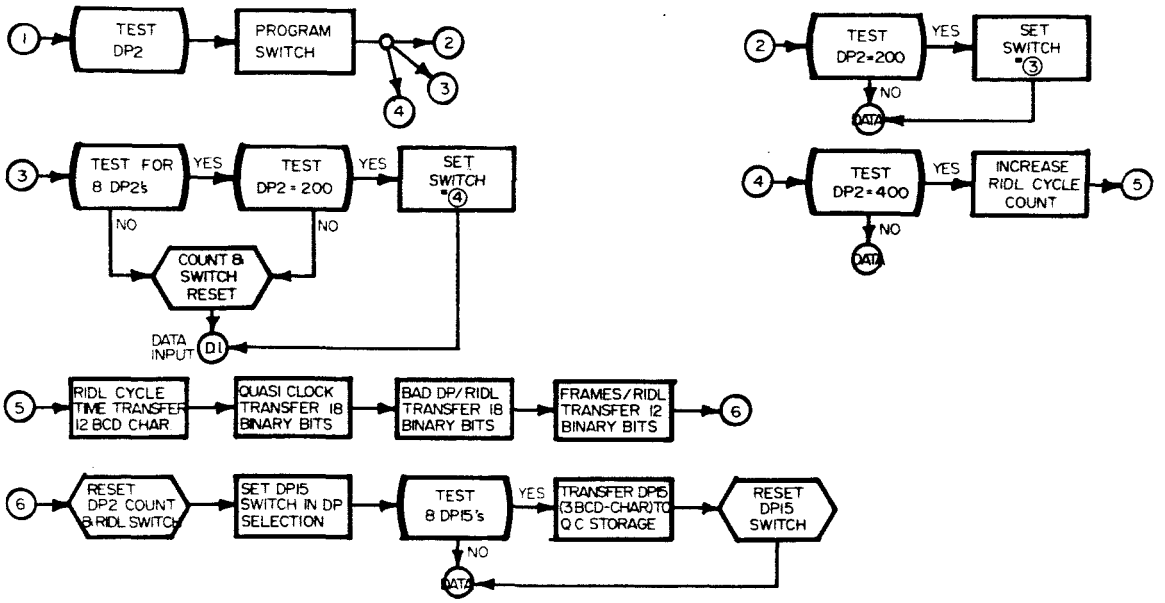


Figure 6-4 — RIDL Cycle Subroutine Flow Chart

data flow path, and then tests the quantity of the data word. If the data point = 200, the RIDL cycle continues by switching the sequence from the test just completed to another subset with entry at point 3 for 8 consecutive D. P. 2's. If not, the program merely returns to the normal data flow path. When 8 data points are counted and another test for 200 is verified then a switch is made to allow the next D. P. 2 occurring to be tested for a quantity of 400. If any of these tests fail, resets of the switch orders are made and the program re-initiates a new search mode. When the value is found to equal 400 then the RIDL cycle is identified and a count made of the cycles. These cycles occur approximately 7½ minutes apart on the Explorer (S-3) Satellite.

Once having determined the RIDL cycle, the program enters point 5 on the flow diagram. It transfers the twelve most recent characters of time stored, to a storage block used for experimental and quality control information. It also transfers eighteen binary bits of quasi-clock information which is temporarily stored by the quasi-clock subroutine; it transfers a count of bad data points and the number of data frames which occur during the RIDL cycle. From this point the computer resets various program switches and arranges for a count of eight D. P. 15's and a transfer of the eighth D. P. 15 to the RIDL storage block. A glance at the sequence entering at point 6 and exiting back to the main data flow chart illustrates these events. Whereas all the other program switches are

*D. P. means data point and is synonymous with data word.

placed in the RIDL cycle subroutine, the D. P. 15 switch is placed in the main data flow chain to eliminate complicating movement back through the flow paths associated with D. P. 2.

Quasi-Clock Cycle Subroutine

The quasi-clock cycle determination is an intricate programming endeavor and is rather difficult when it is associated with a real time or a reproduced real time method of data collection and conversion. The program had to be developed for both super and subcommutation in order to arrive at a decision and extract the required data.

The quasi-clock data was transmitted from telemetry channels 4, 5, and 6 of the S-3 satellite, and an increase of the clock by a count of one took place after 240 frames of data. The format was such that the cycle was composed of four identical 60 frame subcycles with the quasi-clock count appearing twice, or eight times during the main 240 frame cycle.

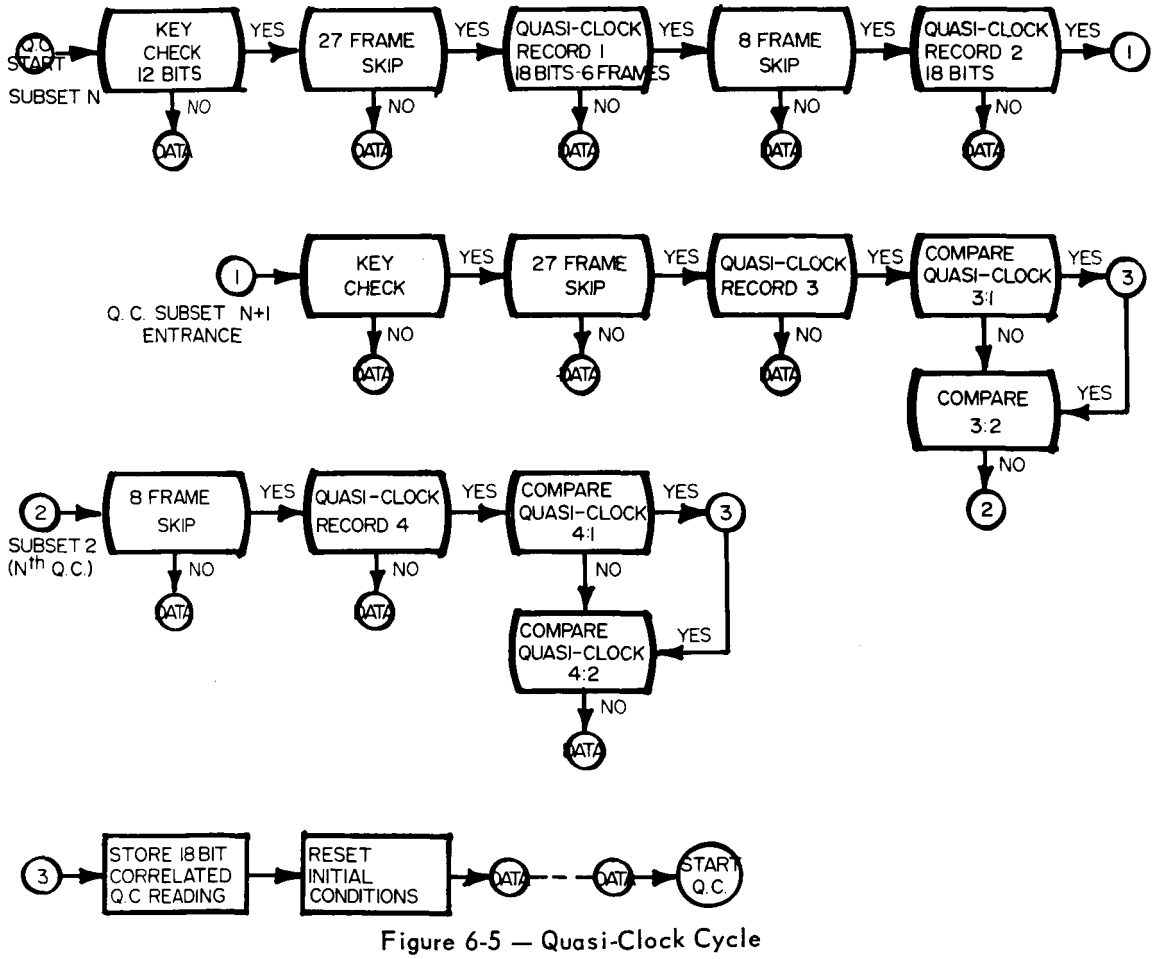


Figure 6-5 — Quasi-Clock Cycle

The program method for extracting the quasi-clock information is shown in Figure 6-5 and is described as follows:

1. The program finds a twelve bit synchronization key consisting of the lower bit in the upper data character of a data word.

   This key is extracted from twelve consecutive frames from channels 4, 5, and 6. These frames are always the first twelve frames of each 60 frame subset. The synchronization key is recognized by a comparison with a known bit pattern stored in the computer. The computer will accept the first valid pattern that appears in one of the three channels.

2. The program then counts through twenty seven consecutive data frames to position it for a second extraction of different data.

3. The program next extracts the first quasi-clock reading of eighteen bits of each 60 frame subset. These consist of six bits from data words 4, 5, and 6 from six consecutive frames. The bits again consist of the lowest order bit of the upper data character in each data word.

4. An eight frame skip is performed and the second eighteen bit quasi-clock record of the 60 frame subset is extracted.

5. A positive identification is made by finding a correlation between two quasi-clock extractions from eight different subsets. This can be seen in the quasi-clock comparisons in the quasi-clock cycle flow diagram which illustrates the conditions for subsets 1 through 4. The routine search through the four subsets, or subcycles of a 240 frame sequence, makes a check for twenty possible correlations.

6. After the quasi-clock is confirmed by a cross correlation, the 18 bit quasi-clock word is stored for future usage. The movement of this clock count to a quality control storage location is performed along with information obtained during the RIDL cycle. Since the quasi-clock occurs every 240 frames of approximately every minute and seventeen seconds, it can be considered as a minor wheel rotation inside of the seven and one half minute RIDL cycle. The quasi-clock will update nearly six times within a RIDL cycle under normal conditions. The quasi-clock program "free wheels" until the larger cycle of the RIDL period is completed and then its most current reading is extracted for storage. The eighteen bit quasi-clock temporary storage is accordingly reset to eliminate the possibility of erroneous data being taken out because the movement of the quasi-clock wheel within the RIDL cycle is asynchronous to it.

File Stop Time Storage and Final Block

When processing of analog data ends, there are a number of statistics that must be accounted for. The final time for the last full frame of data must be recorded and any incomplete block of data must be filled so a proper block length can be maintained when the final block is recorded on magnetic tape. The flow diagram shown in Figure 6-6 illustrates this.

When this is done at the end of a processing run with the integrated telemetry computer system, the computer locates the last storage address used, transfers the final time read-in to a quality control storage area and fills the remaining storage cells of the 960 character block with bad data flags. The final block is loaded on magnetic tape, and an end of file is written to indicate where loading stops. The process run is completed by a rewinding of the magnetic tape and a typewriter printout is performed, stating "End of Run."

This routine is a postprocessing operation but must be completed immediately after a conversion of analog to digital data takes place.

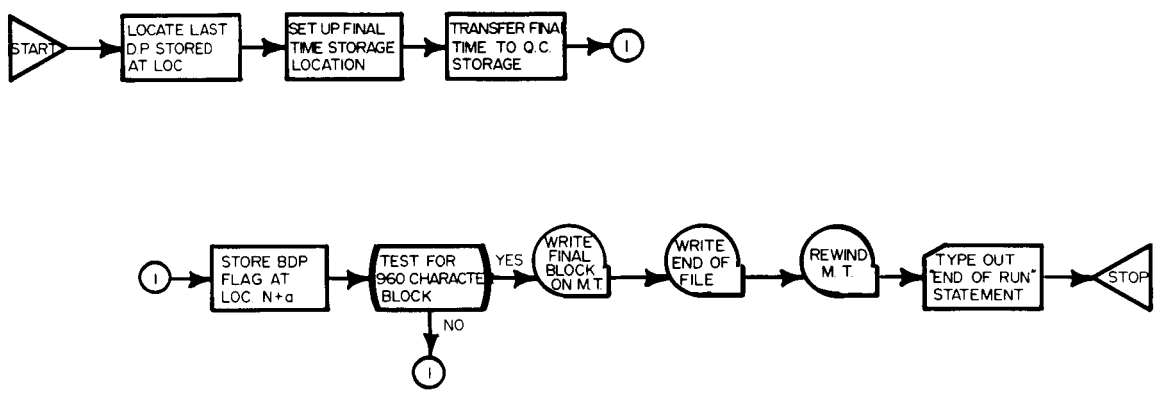


Figure 6-6 — File Stop Time Storage & Final Block Fill

Quality Control Printout

When the production run is completed a digital magnetic tape with a prescribed format is available for decommutation or further analysis. This can be done by immediate insertion of off-line processing programs. This area was not explored in this project because the problem was one of exploiting the time present during the analog to digital conversion process. In any case, the recorded magnetic tape can be used for immediate processing or it can be printed out directly on the typewriter in 960 character block printouts.

SECTION VII

SOFTWARE INTEGRATION

DATA PROCESSING ALTERNATIVES

When a computer is made a part of an overall system, two alternatives are presented for data processing. The first alternative is a two-pass operation. During the first pass of the two-pass operation, the computer can be used in place of the output buffers. The computer can accept data, store it, and transmit the data to a magnetic tape in predetermined quantities. The magnetic tape can then be rewound and played back for quality control calculations and editing by the computer.

The second alternative is a one-pass operation which consists of a simultaneous performance of the buffer process together with the quality control determination. (This comprehensive approach is the desired goal). In the one-pass operation, the time intervals between data inputs can be used for manipulations and calculations for quality control purpose. Thus, the computer is put to work more efficiently during a given time span.

SUPPORT PARAMETERS

A general purpose computer, even of the small scale catagory, can be used for one-pass operations of telemetry data if it has an adequate repertoire and rapid cycle times. A computer with a buffered input/output with interrupt capability can easily accomplish all quality control requirements on data input rates of a slow and medium nature on similar types of problems. In the case of very fast data rates, iterative time consuming functions such as data synchronization, binary coded decimal-to-binary conversions, and limit checks should be handled externally to allow for other computations.

As the project has proven, modification of an external nature can be made in order to use a non-buffered computer for on-line processing, however, this type of system is always output bound if large amounts of data are to be transferred to magnetic tape.

Costs for modifications to meet the problem requirements could be absorbed more easily in the purchase of a buffered computer. Furthermore, data processing "system variability" is difficult to achieve with the type of development program herein described. System variabliity can best be achieved in a buffered system by a greater programming power.

STARS REFERENCE

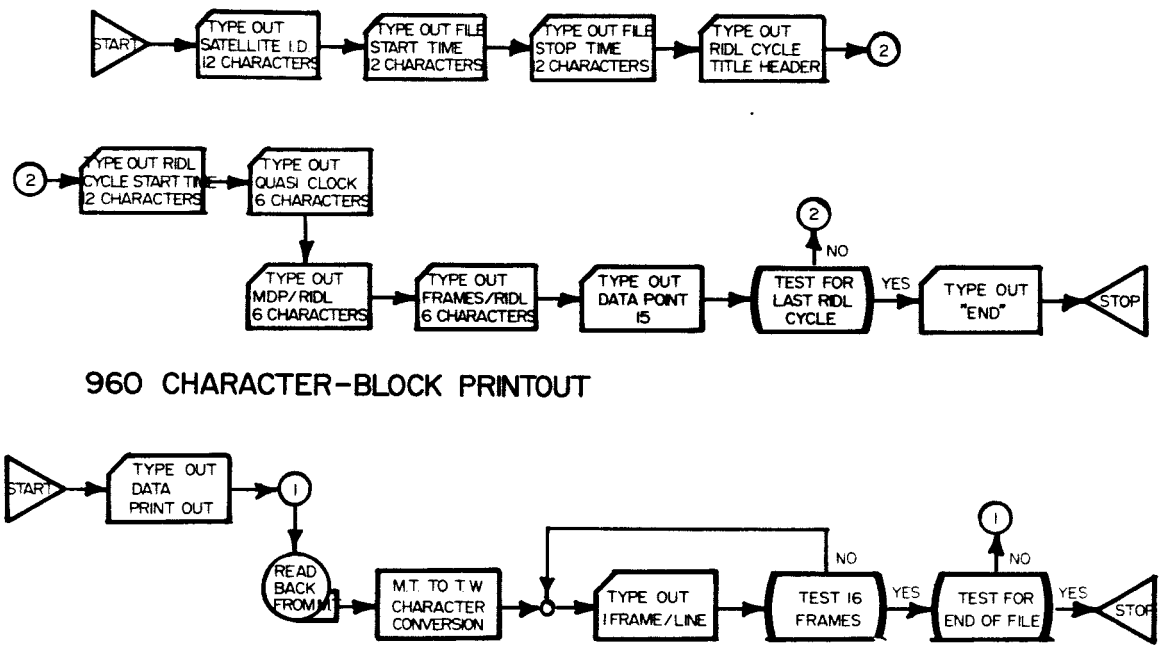
Althrough both systems are alike in performance of data quality control operations, the integrated telemetry computer is a slower and less complicated system than the STARS, Phase II system now under purchase by GSFC, NASA. The integrated telemetry computer is a system that is progressively only a step away from two-way communication.

The STARS, Phase II system readily does what an input/output limited computer cannot do. The STARS system has a closed loop function in a digital sense; that is, it is capable of feedback to the telemetry processor which is supplying it information. Therefore, the format is controlled by the computer "futuristically speaking".

Extending the communication process is the next progressive step to be taken for the integrated telemetry computer system. The computer should be enhanced so that it controls the data rate and format to properly synchronize the data stream. Also, the computer should be capable of providing servo control for better resolution of raw data signals.

Prior to performing the block printouts, the computer program calls for a printout of all the previously stored statistical and quality control information that has been collected. The printout subroutine is shown in Figure 6-7.

Since this information is collected and retained in both BCD and binary number formats during processing and the different input/output routines call for various equipment coding, extensive program effort for character conversion, translation, and information movement was required to effeciently prepare this postoperative portion of the program.



960 CHARACTER-BLOCK PRINTOUT

Figure 6-7 — Quality Control Printout

SECTION VIII

CONCLUSIONS

The conclusions derived from the telemetry computer integration project are as follows: The objectives of the design goal were tested and proven to be feasible. The results obtained from the engineering efforts of the design project led to further overall conclusions, beyond the scope of the design project, that the advantages and disadvantages of various computers can be assessed with regard to present and future telemetry reduction systems. Specifically it has been proven that by coupling a computer to the output of the telemetry signal processing line in place of the currently used buffer devices, to receive the digitized data, immediate savings in time, manpower, and efficiency result. In addition, the following improvements are accomplished by the operational change:

1. The computer replaces the special purpose equipment and eliminates "duplication of function" costs.

2. Storage equipment and space for reels of magnetic tapes containing intermediate processed data is eliminated.

3. Manpower and transportation costs for movement of the magnetic tapes are removed.

4. Time compression in the total data processing cycle is achieved. Analog processing, physical tape movement, and computer analysis are incorporated so that all three functions are performed when the analog processing time ends.