THIRD QUARTERLY REPORT

NONDISSIPATIVE DC to DC REGULATOR-CONVERTER STUDY

15 December 1964 to 15 August 1965

Contract No.: NAS 5-3921

Prepared by

Hamilton Standard DIVISION OF UNITED AIRCRAFT CORPORATION
WINDSOR LOCKS, CONNECTICUT • U.S.A.

for

GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

HSER 3124

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GODDARD SPACE FLIGHT CENTER
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I. ABSTRACT

The effort in the third quarterly period included the following:

1. Initial Breadboard development of the self-stabilizing chopper power Stage.

2. Evaluation of several frequency control stages.

3. Test and evaluation of the frequency-efficiency characteristics of the self-stabilizing chopper.

4. Size and weight analysis of the self-stabilizing chopper.

The results of the effort for this quarterly period are:

1. The final configuration for the power stage is a single-ended self-stabilizing chopper. The basic self-stabilizing concept requires a means of circuit starting for each half cycle; an external gate trigger pulse is utilized for this purpose. A means of current limiting is required to prevent circuit recovery time lag of the self-stabilizing chopper; a degenerative feedback current limit method is utilized for this purpose.

2. A saturating core square wave oscillator has been selected for this phase of the program as the variable frequency source.

3. The frequency-efficiency characteristics of the 10-watt self-stabilizing chopper show relatively small changes in peak efficiency at minimum line voltage but significant changes in efficiency at maximum line voltage.

4. The nominal switching frequency of the 10-watt chopper regulator should be at least 25 KC to insure meeting the design goal component weight of 0.63 pounds. The component volume estimate at 25 KC is approximately 6 cubic inches which is well under the 15 cubic inch design goal.

TABLE OF CONTENTS

LIST OF TABLES AND ILLUSTRATIONS

LIST OF TABLES AND ILLUSTRATIONS (Continued)

II. PURPOSE

The purpose of this program is to provide concepts, techniques, and developed modular circuitry for non-dissipative DC to DC converters in the power range of 0 to 100 watts.

Major program goals are the maximization of efficiency, simplicity, and reliability, along with minimization of size, weight, and response times of the converters.

The circuits are to be modular in concept, so that a minimum of development is required to tailor a circuit to a specific application requirement. The concepts should also allow, inasmuch as practical, for the use of state-of-the-art manufacturing techniques.

The program is multi-phased, including a study, analysis, and design phase, and a breadboard phase during which the concepts are to be verified by construction and test of eight breadboards.

III. INTRODUCTION

The work of the previous quarter included the following:

1. Initial development of the self-stabilizing chopper power stage.
2. Frequency control stages
3. Frequency-efficiency characteristics of the self-stabilizing chopper regulator.
4. Size and weight analysis of the self-stabilizing chopper regulator

Several problem areas with the self-stabilizing scheme were uncovered early in the breadboard development phase which required extensive investigations. The problems were associated with circuit starting, circuit recovery time, and balanced operation. Solutions to each of these problems were determined.

Breadboard investigations of several variable frequency sources were made to determine the most applicable frequency source for this phase of the program. The following circuits were considered; the unijunction transistor relaxation oscillator, the astable multivibrator oscillator, and the saturating core square wave oscillator.

The frequency-efficiency characteristics of the self-stabilizing chopper regulator were obtained. Tests were run at nominal switching frequencies of 5, 10, 20, and 30 KC.

A size and weight analysis of the self-stabilizing chopper regulator was obtained for the above nominal switching frequencies. Results of the frequency-efficiency testing and of the size and the size and weight analysis were used to determine the optimum switching frequency for the chopper regulator.

IV TECHNICAL DISCUSSION

A. INITIAL DEVELOPMENT OF THE SELF STABILIZING CHOPPER

The basic self stabilizing chopper power stage shown in figure 1, consists of two power transistors Q1 and Q2, two driver transistors Q3 and Q4 and a base drive transformer T1. Resistors R2 and R4 control the base current supplied to Q1 and Q2. Self stabilization of the chopper is obtained through the constant volt second product of the saturating core drive transformer. The volt second product of this transformer is capable of sustaining a voltage of E volts for a time of t seconds. If E increases t must decrease to maintain the constant volt second product; hence; automatic stabilization is accomplished for input line variations.

A description of circuit operation follows; assume transistor Q3 is biased in the forward direction. If the leakage current through resistor R3 is sufficient to turn on transistor Q2 slightly, part of voltage E will be applied across transformer T1. Current will flow through transistor Q3 thus driving transistor Q2 into saturation and delivering power to the load. Drive voltage for transistor Q2 is maintained for Et volt-seconds until transformer T1 saturates. Drive voltage for transistor Q2 collapses after saturation of the drive transformer, thus turning transistor Q2 off. The chopper circuit is forced into a cut-off state until transistor Q4 becomes energized. When transistor Q4 becomes energized the cycle repeats itself with transistor Q1 delivering power to the load. Note that starting of the self-stabilizing chopper is required to initiate each half cycle.

Several problem areas with the self stabilizing chopper scheme were uncovered early in the breadboard development phase. One problem was associated with circuit starting. A second problem was associated with insuring rapid turn off of the self stabilizing chopper after the drive transformer T1 had saturated. A third problem was associated with obtaining a balanced output of the push-pull stage consisting of transistors Q1 and Q2.

Circuit Starting Problem

An external means of starting the self-stabilizing chopper is required to initiate each half cycle of operation. This is necessary since the saturation of the drive transformer T1 during the previous half cycle shuts off the main chopper transistors. The circuit shown in figure 1, depends on leakage through resistors R1 and R3 to energize transformer T1.

This method of starting was found to be unsatisfactory during the preliminary breadboard stages. The component resistance values of R1 and R3 had to be set at relatively low values to initiate circuit turn on. However, the resultant values of these resistors produced sufficient base drive from the main supply voltage to keep the chopper transistors switched on independent of the drive voltage provided by the drive transformer T1.

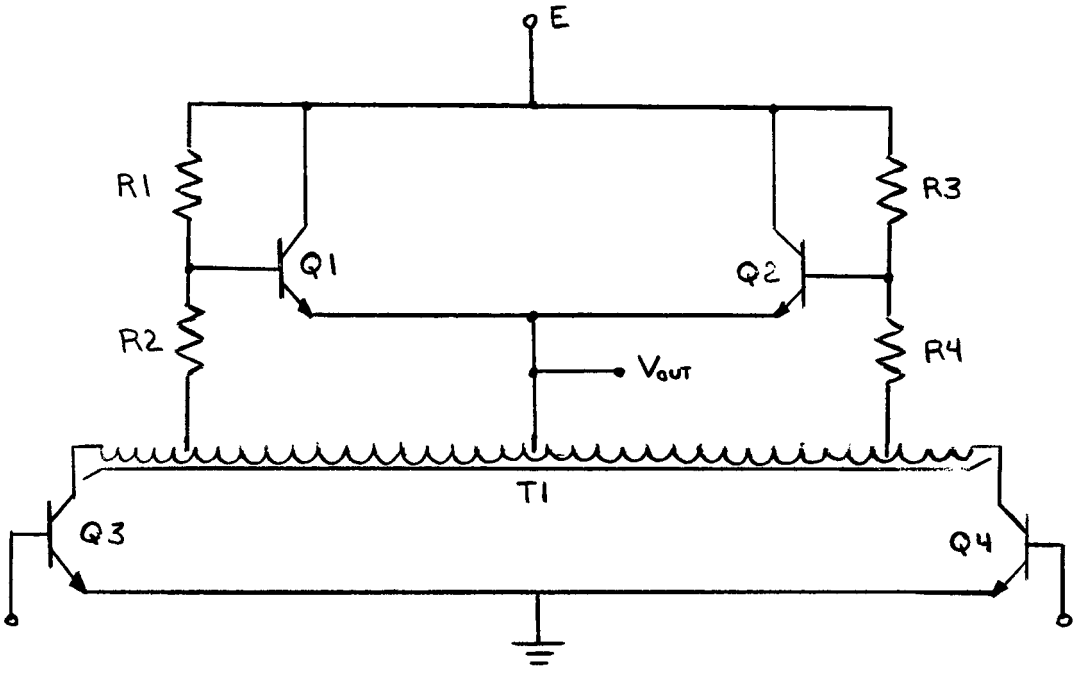


Figure 1 BASIC SELF STABILIZING CHOPPER POWER STAGE

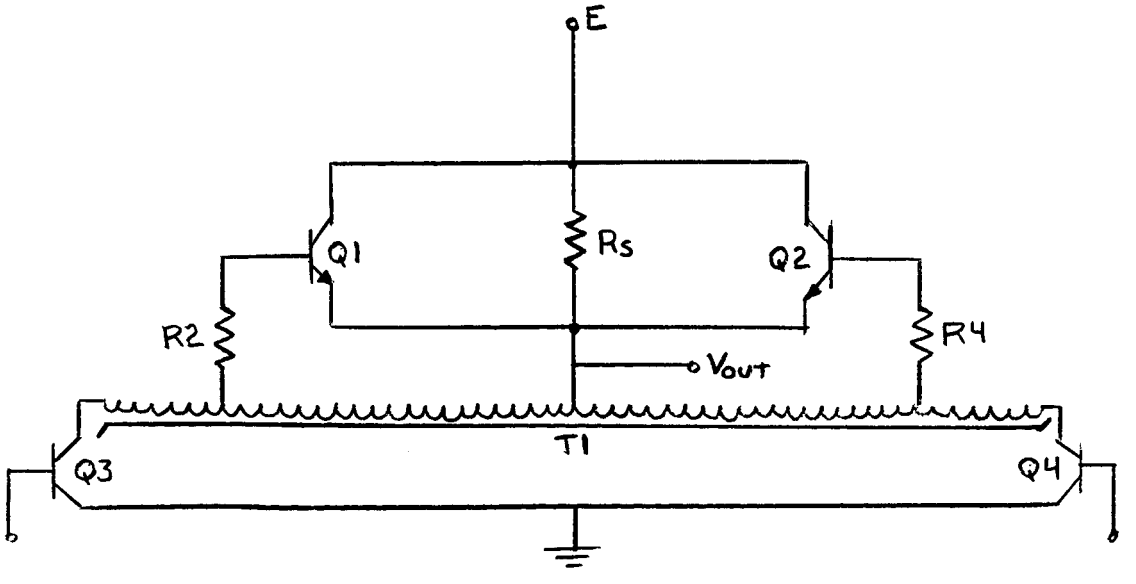


Figure 2 MODIFIED SELF STABILIZING CHOPPER POWER STAGE

The modification shown in figure 2, was tried to solve this starting problem. This modification eliminated resistors R1 and R3 and added an alternate starting resistor RS. Resistor RS was connected directly across transistors Q1 and Q2 to lead the main supply voltage directly to the prima ry of transformer T1. The intended solution was to set resistor RS to a value low enough to provide sufficient leakage around transistors Q1 and Q2 to energize transformer T1. Note, however, that RS has now provided a direct coupling path between input and output.

This method of circuit starting was breadboarded and evaluated. It was determined that the resistance value was dependent on the input voltage. For example, at 10 volts input it was found that RS had to be set as low as 30Ω to provide sufficient turn on drive. This approach was discarded because the requirement for a small value of RS would provide low impedance coupling between the input and output of the circuit.

The modification shown in figure 3, was investigated as another possible solution to the starting problem. This circuit utilized a gate pulse input rather than the fixed leakage coupling previously discussed. The gate pulse, which is coupled through diodes D1 and D2, momentarily connects the supply voltage to the bases of transistors Q1 and Q2. These transistors are momentarily driven on, thus allowing the supply voltage to be impressed across transformer T1. The regeneration process is initiated and the circuit operates as previously described.

The gate pulse is synchronized to the variable frequency square wave source so that the gate pulse is applied at the same instant that either transistor Q3 or Q4 is forward biased.

Satisfactory starting characteristics were obtained with this starting method. All further breadboard testing was done using the gate pulse starting technique.

Circuit Recovery Time Lag Problem

The finite recovery time of the main chopper transistors, after the driver transformer T1 has saturated, results in a transient low impedance condition existing across the input voltage. This causes a large current spike to be drawn through the driver transformer. This current spike introduces an additional time delay in circuit recovery time, thus resulting in significant power losses for the system. Preliminary breadboard testing indicated that if this current pulse could be limited, the recovery time of the chopper circuit could be increased, and the power losses associated with this recovery lag could be minimized.

Investigations were conducted to determine solutions to this problem. The investigations involved studies of both the inherent characteristics of the driver transformer, and of circuit methods for achieving some form of current limiting.

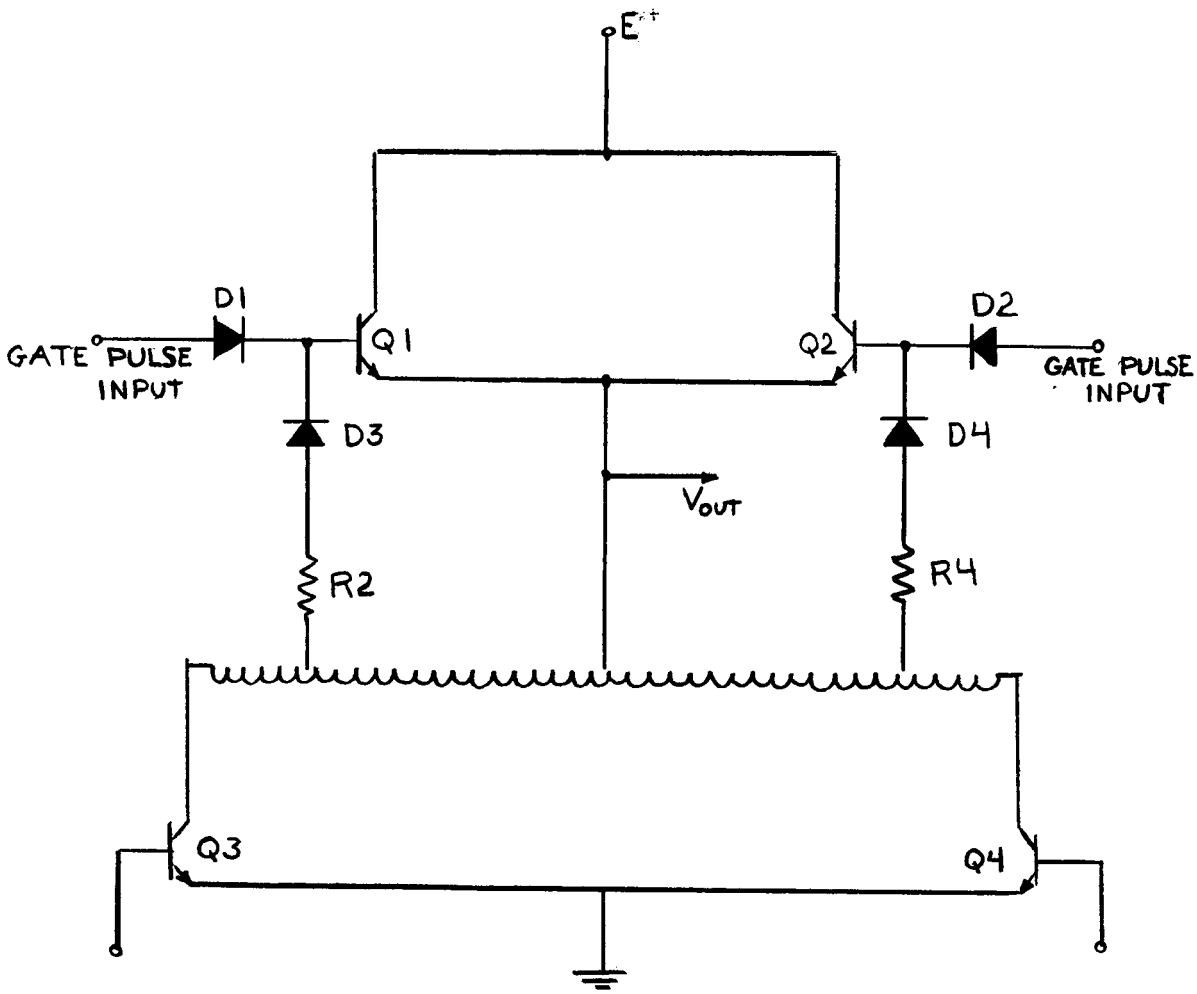


Figure 3 SELF STABILIZING CHOPPER POWER STAGE USING GATE PULSE STARTING

Driver Transformer Investigation

The investigation conducted into the driver transformer was made to determine what effect on the current pulse the inherent characteristics the transformer might have. Studies on the terminal response of switching cores has been reported in detail by Strauss [1]. An approximation up to where saturation occurs, of the current drawn into an open circuited transformer excited by a step voltage of constant amplitude is given by:

$$i(t) = \frac{\sigma l V^2}{8N^3 h^2 B_s} t + \frac{H_c l}{N}$$

After saturation occurs the current drawn is determined by:

$$i(t) = \frac{V}{R}\left(1 - \varepsilon^{-\frac{R}{L}t}\right)$$

where

σ = conductivity of the core
l = length of core
V = applied voltage
N = number of turns
h = width of core
Bs = maximum flux density
Hc = coercive MMF
R = source resistance (including winding resistance)
L = inductance of coil in air

The above equation for current drawn up to saturation has been derived based on the following assumptions:

1. The radius of curvature of the core is large compared to the thickness of the core d.

2. The width of the core h is much greater than the thickness of the core d.

3. The hysteresis loop is perfectly rectangular.

4. The core is initially magnetized at $-B_s$ and switches to $+B_s$.

5. The field penetrates at equal rates from both inside and outside of the core.

Figure 4 shows the terminal current response of the square-loop core to a constant voltage excitation. The current begins rising linearly from Ic, where Ic is the current due the coercive MMF. At t_s saturation occurs and the current rises exponentially to a steady state value determined by the magnitude of the applied voltage and the magnitude of the source resistance. The slope of the linear portion of the curve is determined by the geometry of the core, its conductivity, and the magnitude squared of the applied voltage.

1.) Strauss, Leonard: Wave Generation and Shaping, New York, McGraw-Hill, 1960.

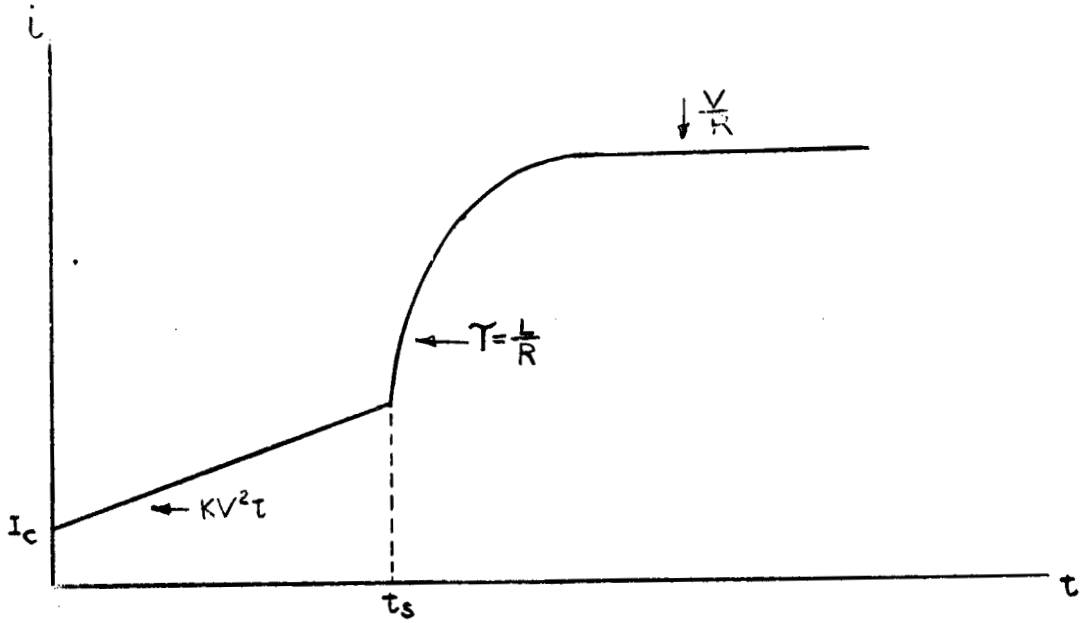


Figure 4 Current Response of a Square Loop Core To A Constant Voltage Excitation

TABLE 1 MAGNETIC PROPERTIES FOR SWITCHING CORES

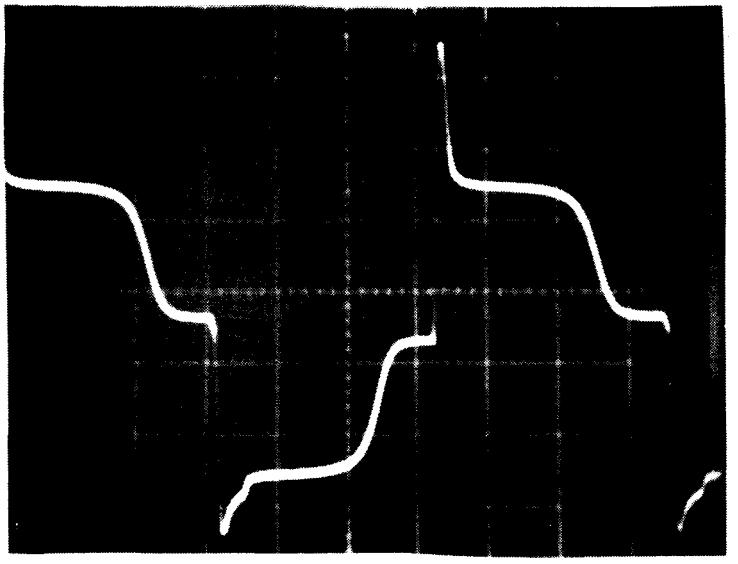
Core Material	Volume Resitivity $1/\sigma$	Saturation Flux Density B	Coercive MMF H	Squareness Ratio
Deltamax	45μΩ-cm	15,500 gauss	0.16 oersteds	0.98 typical
Permalloy	55μΩ-cm	8,000 gauss	0.07 oersteds	0.50-0.90 typical
Ferrite IG C-2	100Ω-cm	2,750 gauss	0.36 oersteds	0.91 typical

The time constant of the exponential rise is determined by the equivalent source resistance and the inductance of the coil in air. This time constant is normally very small, since the air coil inductance of a small toroid is normally in the microhenry range.

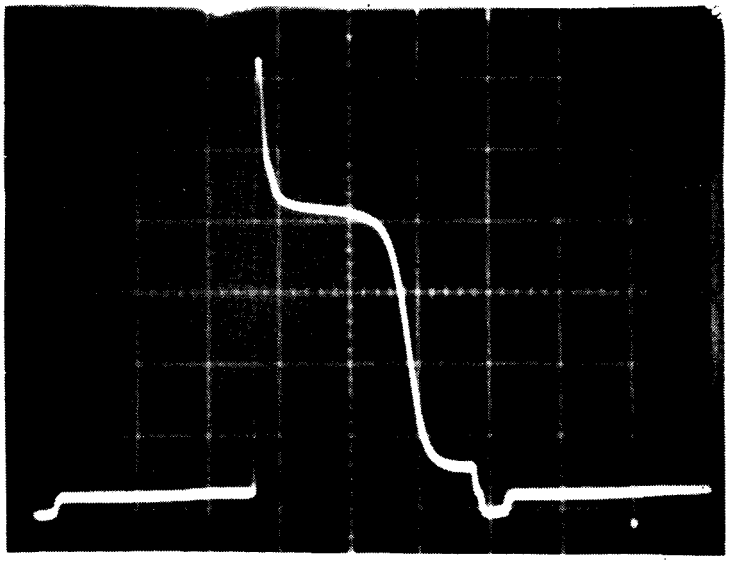
For a given transformer core material (σ = constant), the most predominant term of the above equation for limiting the current is N, the number of turns of the winding. A transformer design requiring a large number of turns would have a two fold effect; reduction of the coercive current constant, since this is inversely proportional to N: and reduction of the slope of the eddy current, since this is inversely proportional to the cube of N. A design criteria for a large number of turns would require a transformer of small core area for a given core material and excitation voltage. However, the reduction of core area would have to be made by making the thickness d very small while keeping the width h large, since the width h is also an important term in reducing the eddy current slope. Investigations of fractional mil bobbin cores have shown this condition difficult to meet, since the width to thickness ratio h/d is normally 4. 5 to 1.

Table 1 shown some typical magnetic properties of several materials that were investigated for this application. Preliminary calculations using the above equation showed that the finite core would require the least current at saturation since its volume resistivity is several orders of magnitude greater than the other magnetic materials. Preliminary calculations also showed that the final steady state current drawn after saturation would be about the same for each core.

Test comparisons were made between a deltamax and ferrite core. The saturation characteristics for a deltamax and a ferrite driver transformer, breadboarded for the 10-watt chopper, are shown in figures 5 and 6. The saturation characteristic of the deltamax core shows a much more rapid turn off time than the ferrite core. This faster turn off time is probably attributed to the higher squareness ratio of the deltamax core. Measurements of the turn off slope showed that the deltamax transformer had a turn off slope of 4 volts per microseconds compared to 2 volts per microsecond for the ferrite transformer. The results of these tests have indicated that deltamax core materials provide the most desirable characteristics for this circuit application. All further efforts made in determining the solution to this problem utilized this core material.

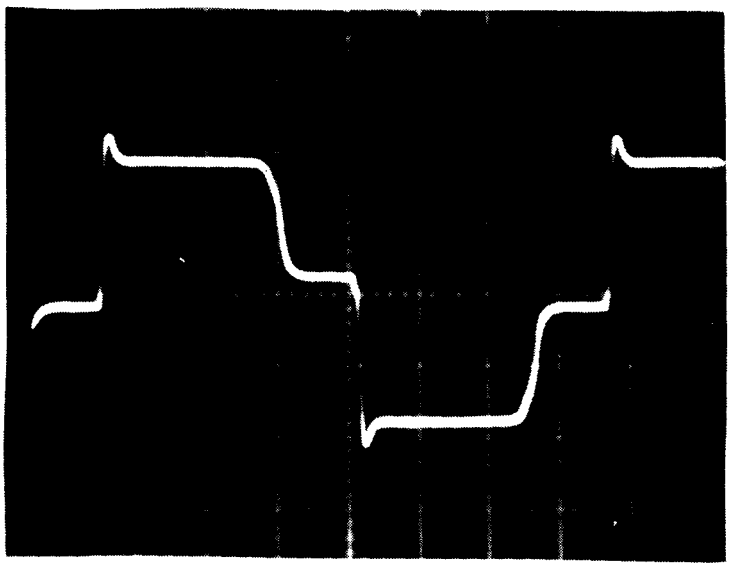


Waveform Across Primary of Transformer
Vertical Scale: 10 volts/cm
Horizontal Scale: 10 μsec/cm

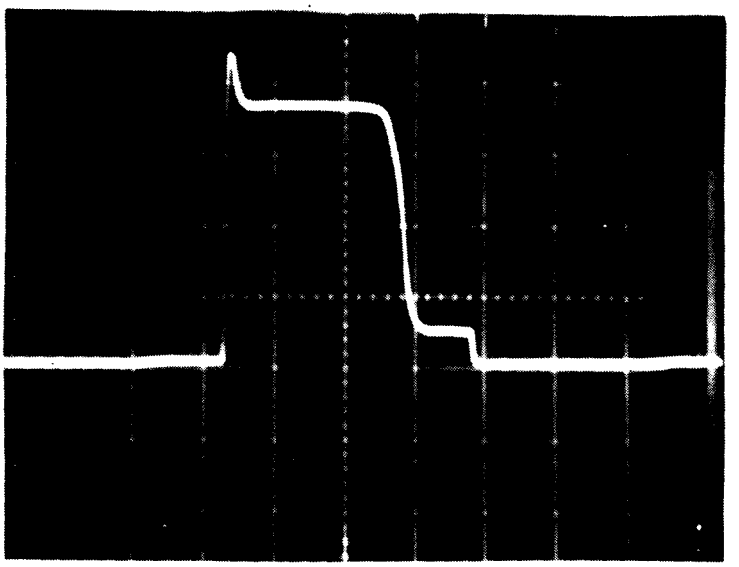


Collector-Emitter Waveform
Vertical Scale: 5 volts/cm
Horizontal Scale; 10 μsec/cm

Figure 5 Saturation Characteristic of Ferrite Driver Transformer



Waveform Across Primary of Transformer
Vertical Scale: 10 volts/cm
Horizontal Scale: 10 μsec./cm



Collector-Emitter Waveform
Vertical Scale: 5 volts/cm
Horizontal Scale: 10 μsec/cm

Figure 6 Saturation Characteristic of Deltamax Driver Transformer

Current Limiting Techniques

Investigations were conducted to determine circuit methods for achieving some form of current limiting. The investigation covered three methods of current limiting, designated as resistive current limiting, degenerative feedback current limiting, and transistor current limiting.

The saturation current spike problem could be described as follows. Referring to the circuit shown in figure 7, assume that transistors Q2 and Q3 are conducting.

When transformer T1 saturates, a large current spike is drawn through T1 and transistor Q3 since this traisistor is still forward biased. Transistor Q3 tries to turn off since its base drive is collapsing. However, transistor Q2 has a finite recovery time because of the saturation characteristics of the driver transformer and the inherent transistor recovery time: The saturation current drawn thus becomes very large, forcing the driver transformer further into saturation. This results in a very slow recovery time for the overall circuit and significant power losses for the driver transformer.

Resistive Current Limiting

This circuit approach is shown in figure 8. Assume transistors Q2 and Q3 are driven into saturation. When transformer T1 saturates, a large current spike is again drawn through transformer T1 and transistor Q3. However, the amplitude of this spike becomes limited to some degree by resistor R5. Thus, the transformer is not driven as deeply into saturation as before. This should result in a slightly faster recovery time and less power losses.

Degenerative Feedback Current Limiting

This circuit is shown in figure 9. Again assuming transistor Q2 and Q3 are driven into saturation, a current spike is drawn through transformer T1 and transistor Q3 when T1 saturates. As the current increases, the voltage drop across resistor R6 also increases, which in turn reduces the base emitter bias of transistor Q3. This causes transistor Q3 to come out of saturation, thus introducing a large resistance, into the line. The result is a current spike whose amplitude should be significantly less than that of either of the two previous schemes because of the high impedance of transistor Q3.

Transistor Current Limiting

This circuit approach is shown in figure 10. Assume transistors Q2 and Q3 are driven into saturation. Under normal operation, transistor Q5 is biased into saturation by the network consisting of resistors R7, R8 and R9 and diode D4. When transformer T1 saturates, a spike of current is drawn

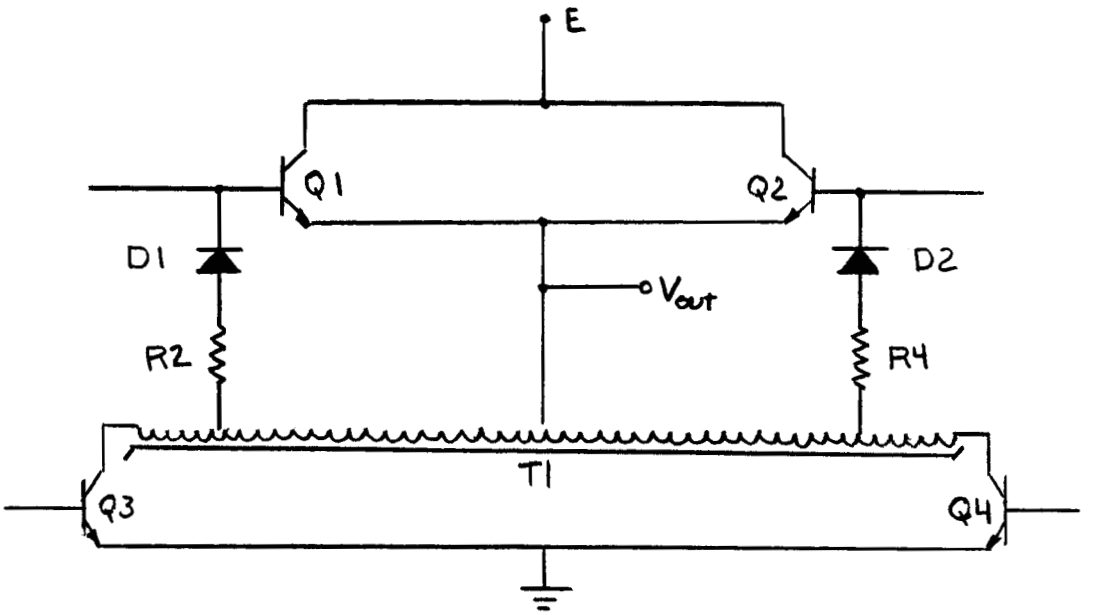


Figure 7 NO CURRENT LIMITING

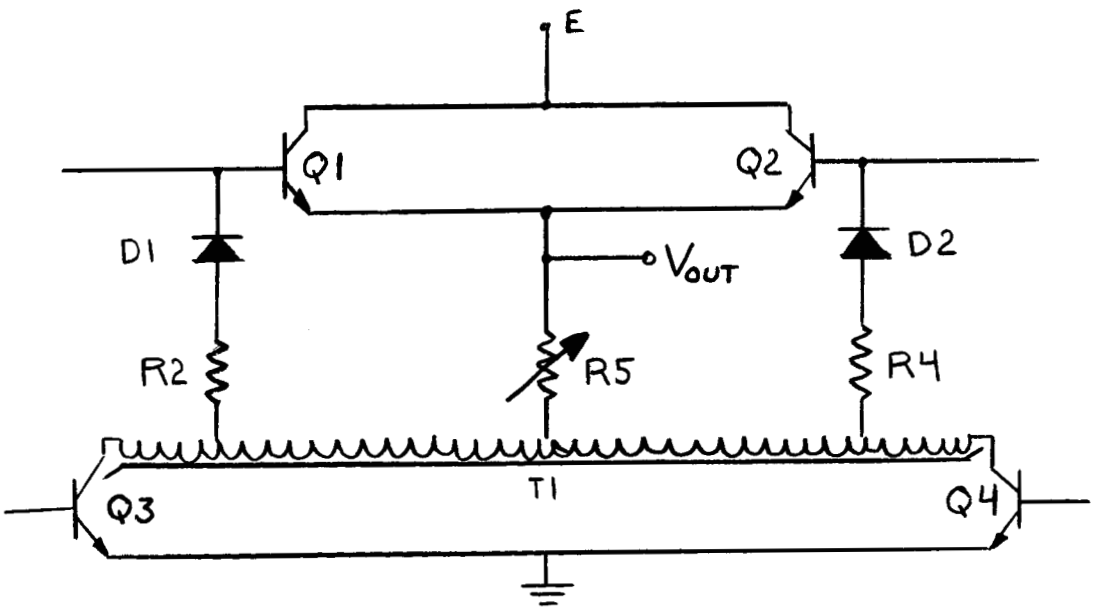


Figure 8 RESISTOR CURRENT LIMITING

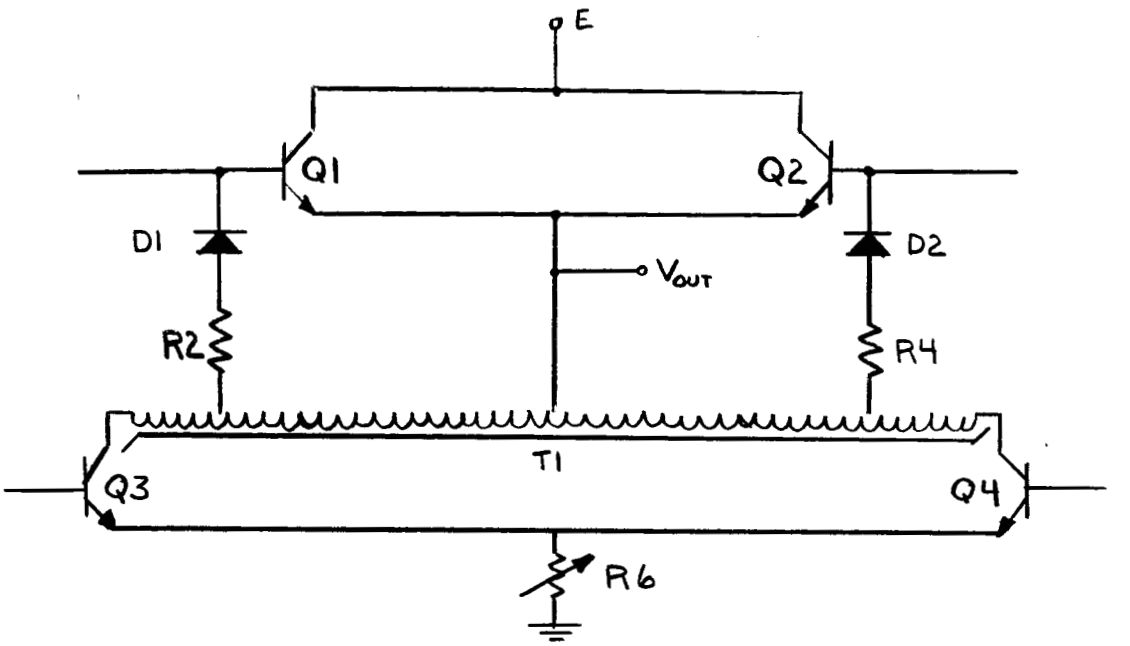


Figure 9 DEGENERATIVE FEEDBACK CURRENT LIMITING

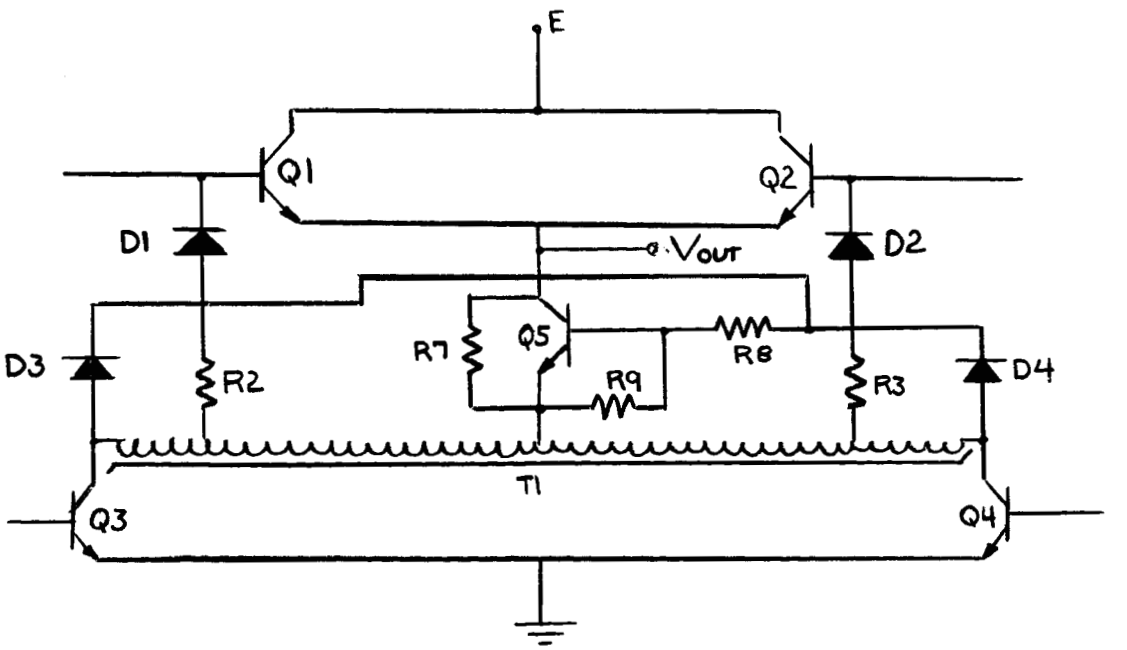


Figure 10 TRANSISTOR CURRENT LIMITING

through T1 and transistor Q3. Since the voltage across T1 collapses, the base drive to transistor Q5 is reduced, forcing it to come out of saturation. Thus, the collector to emitter resistance of transistor Q5 is introduced into the line in parallel with resistor R7, and the resultant resistance should be more effective than the resistive current limit approach, since its limiting resistance cannot be made too large because of the normal steady state drive requirement.

Experimental Tests

Breadboard testing was performed to evaluate the different methods of current limiting previously discussed. A series of driver transformer designs was generated at four different nominal frequencies, 5KC, 10KC, 20KC, and 30KC. Variable core geometries were also evaluated to determine what effect this would have on the saturation current drawn. Small adjustments were made for the driver transformer turns ratio to account for the voltage drop caused by the current limiting resistor. Normal transformer turns ratios were set at 4.5 to 1, whereas those for the resistive current limit tests were set at 4.0 to 1.

Tests were performed at 20 volts input for no load and full load, since these represented worst conditions. A small sensing resistor was connected in series with each driver transistor collector, and a HP model 310A wave analyzer was used to measure the RMS components of the drive current. A minimum of ten harmonics were recorded for each test condition, and the total RMS content was calculated from these readings.

The results of these tests are shown in table 2. The RMS current drawn with no current limiting varied from 135 milliamps at 5KC to 735 milliamps at 30KC. The RMS current drawn with 5Ω resistive current limiting varied from 80 milliamps at 5KC to 269 milliamps at 10KC. No tests were performed with resistive current limiting at 20 and 30 KC. The RMS current drawn with a 10Ω degenerative current feedback varied from 35 milliamps at 5KC to 116 milliamps at 30KC. The average current change from no current limiting to the resistive current limiting was about 3 to 1, whereas the average current change from no current limiting to the degenerative current limiting was about 5 to 1.

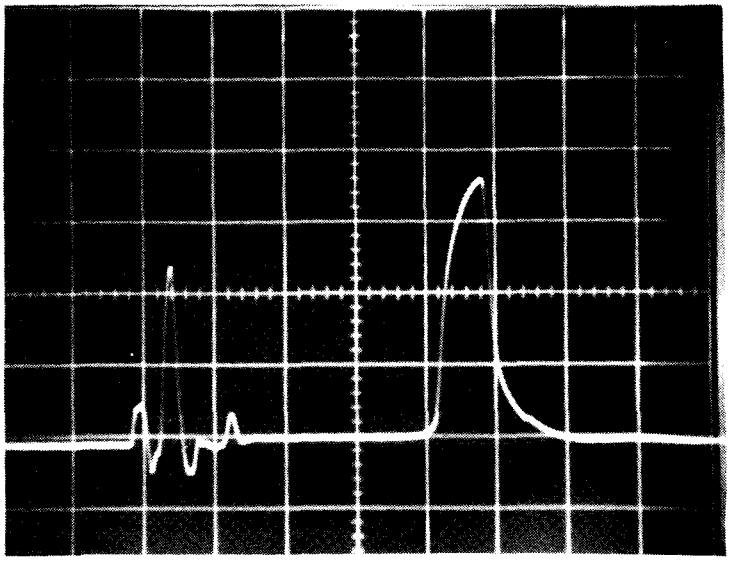
The most significant effect on core geometry was attributed to the number of primary turns. By holding core area constant the primary turns were made proportional to switching frequency. The RMS current was significantly less for the lower frequencies than for the higher frequencies. This was to be expected since the current expression discussed in the previous sections showed the current to be inversely proportional to the cube of the primary turns. The variation in core length showed little change in the current drawn.

Only preliminary testing was done with the transistor current limiting approach. It had been hoped that this approach would be at least as good as the resistive current limiting approach without the normal steady state losses that would be associated with this fixed resistor approach. However, the circuit recovery problems discussed earlier also occurred with this approach. Further detailed investigations with this approach were discontinued.

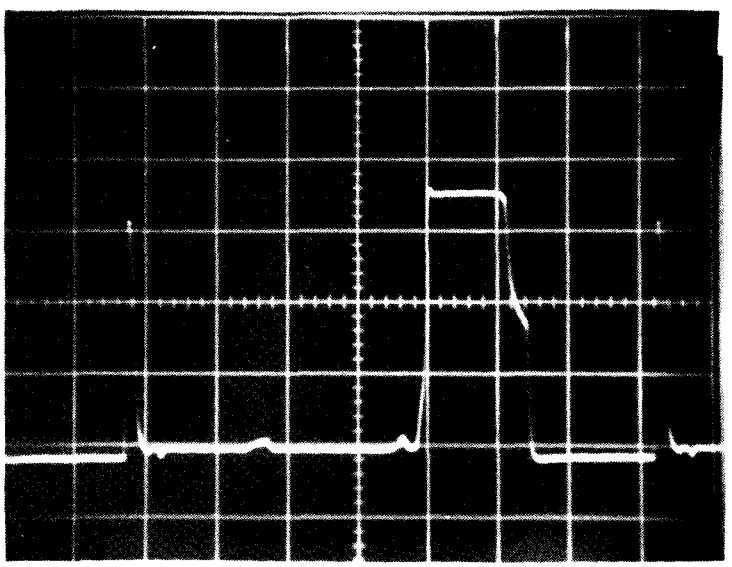
Current and voltage waveshapes for the different methods of current limiting investigated are shown in figures 11 through 13. Figure 11 shows the driver

TABLE 2 RMS DRIVE CURRENT FOR DIFFERENT CURRENT LIMITING APPROACHES

						Current Limiting Approaches	
Transformer	Core Length (Inches)	Core Area ($in^2 \times 10^{-3}$)	Primary Turns	Design Frequency (KC/S)	Load Condition	No Current Limiting (amps rms)	5Ω Resistive Current Limiting (amps-rms)	10Ω Degenerative Feedback Current Limiting (amps-rms)
L	1.28	2.93	170	5	NL		.1370	.0625
L					FL		.0797	.0461
M	1.86	2.93	170	5	NL		.1490	.0638
M					FL		.0915	.420
P	1.86	2.93	170	5	NL	.2120		.0615
P					FL	.1350		.0384
H	2.26	2.93	173	5	NL		.1450	.0610
H					FL		.0895	.0410
O	2.26	2.93	173	5	NL	.2090		.0563
O					FL	.1305		.0369
C	1.28	3.32	160	5	NL	.2230		.0587
C					FL	.1510		.0352
J	1.77	5.86	87	5	NL		.1520	.0603
J					FL		.1065	.0426
B	1.09	1.31	226	10	NL	.2610		.0795
B					FL	.1680		.0557
K	1.28	2.93	87	10	NL		.2060	.0550
K					FL		.1550	.0470
O	1.28	2.93	87	10	NL	.3860		.0815
O					FL	.2740		.0593
N	1.86	2.93	85	10	NL		.2690	.0880
N					FL		.1850	.0680
R	1.09	1.31	97	20	NL	.5500		.1060
R					FL	.4410		.0903
S	1.24	1.31	97	20	NL	.5420		.1050
S					FL	.4060		.0955
A	0.685	1.25	90	30	NL	.5970		.1050
A					FL	.4600		.0882
μ	1.31	1.31	64	30	NL	.7350		.1160
μ					FL	.6050		.1140

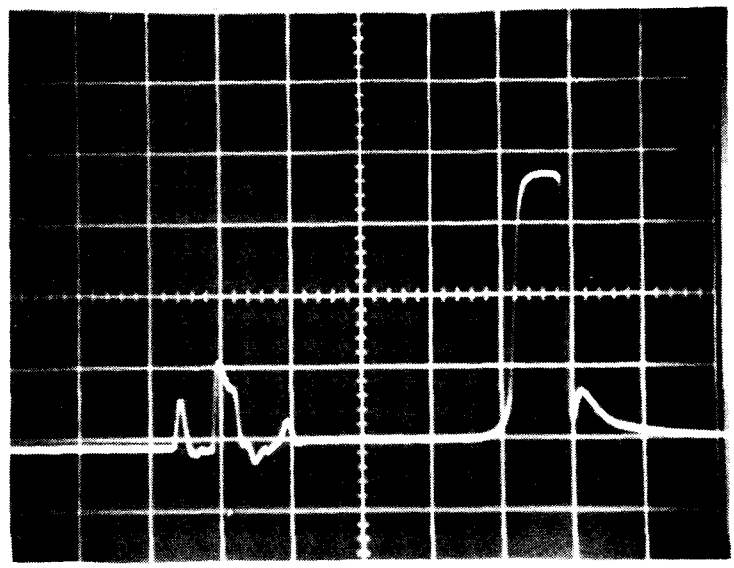


Collector Current
Vertical Scale 1 amp/cm
Horizontal Scale 4μsec/cm

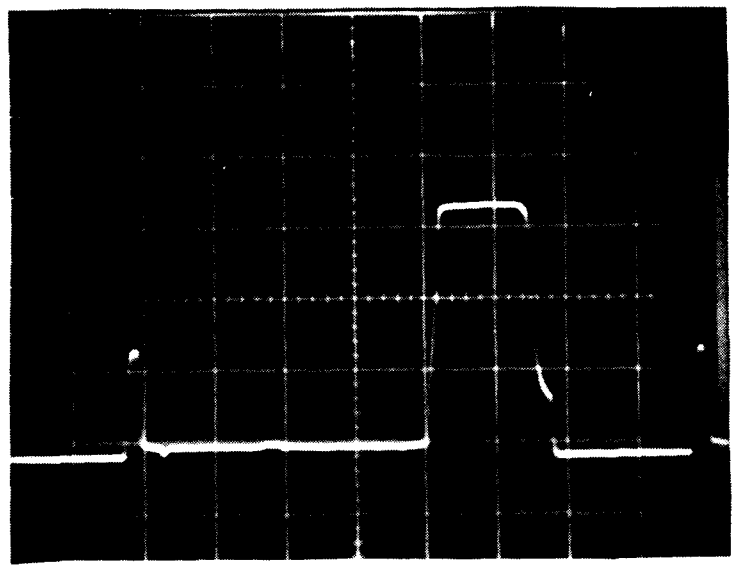


Collector-Emitter Voltage
Vertical Scale: 10 volts/cm
Horizontal Scale: 10μsec/cm

Figure 11 Collector-Emitter Voltage Waveform and Collector Current Waveform of Chopper Driver Stage With No Current Limiting

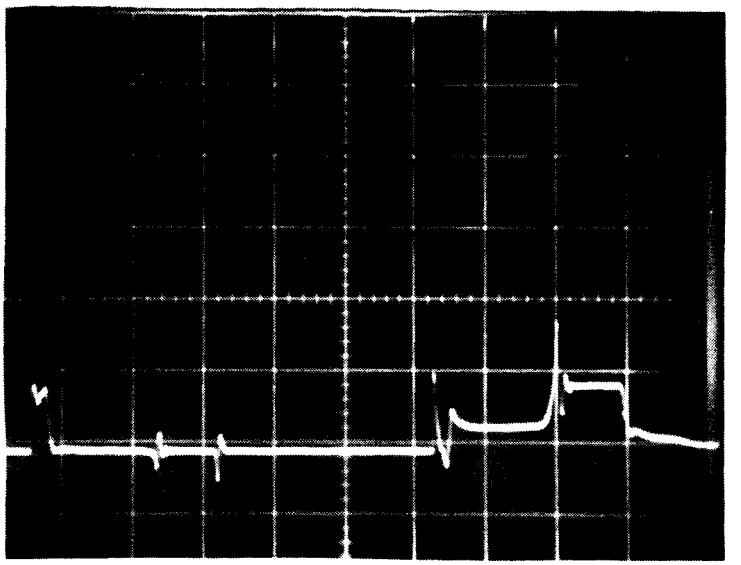


Collector Current
Vertical Scale: 0.5 amps/cm
Horizontal Scale: 4μsec/cm

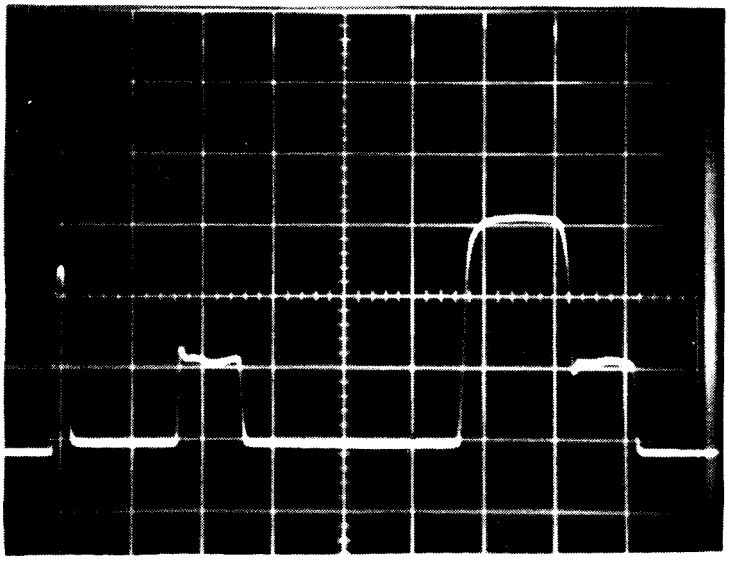


Collector-Emitter Voltage
Vertical Scale: 10 volts/cm
Horizontal Scale : 10μsec/cm

Figure 12 Collector-Emitter Voltage Waveform and Collector Current Waveform of Chopper Driver Stage with 5Ω Current Limiting



Collector Current
Vertical Scale: 0.025 amps/cm
Horizontal Scale: 4μsec/cm

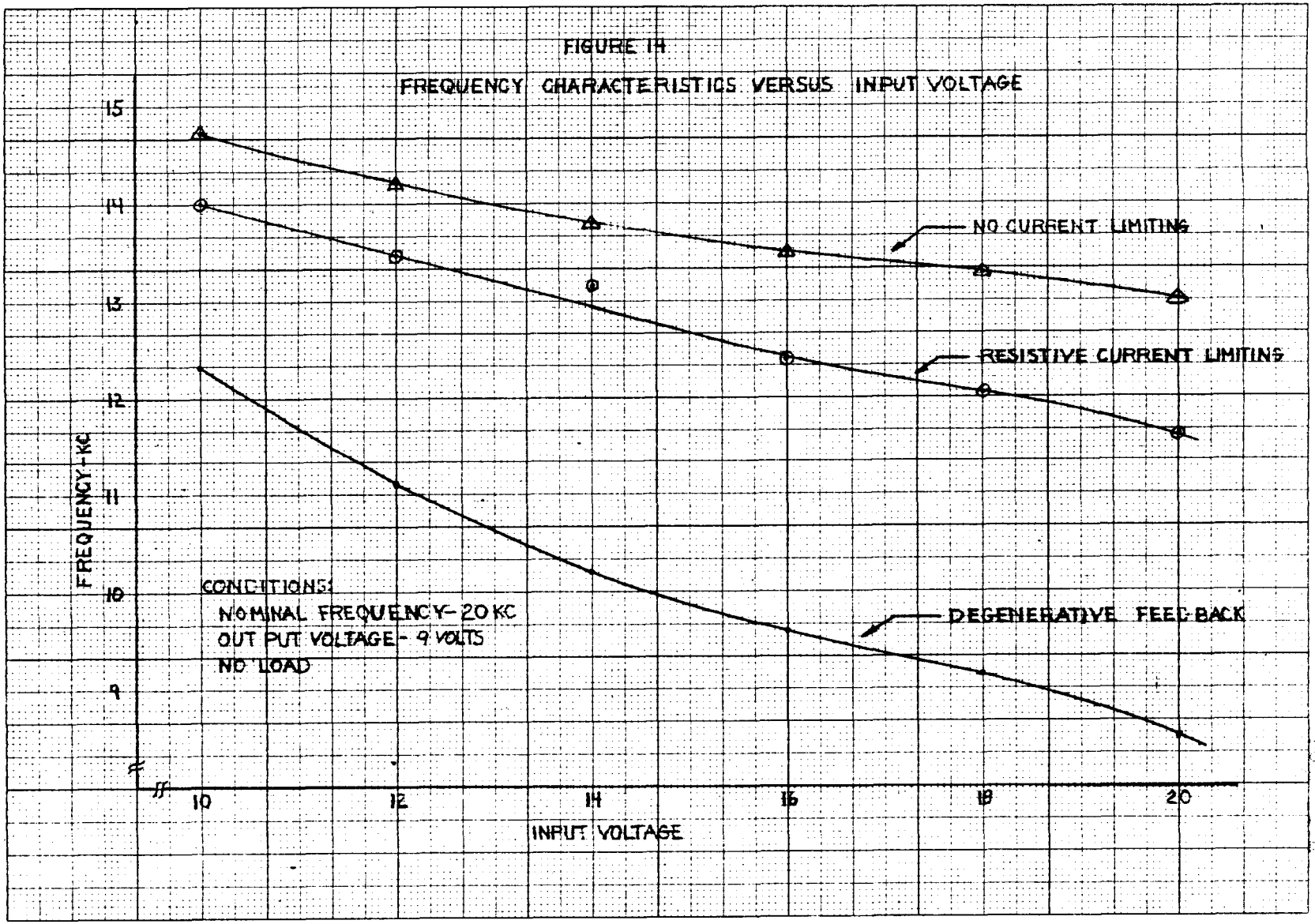


Collector-Emitter Voltage
Vertical Scale: 10 volts/cm
Horizontal Scale: 10μsec/cm

Figure 13 Collector-Emitter Voltage Waveform and Collector Current Waveform of Chopper Driver Stage with 26Ω Emitter Feedback

FIGURE 14

FREQUENCY CHARACTERISTICS VERSUS INPUT VOLTAGE



current and driver collector-emitter voltage with no current limiting applied. The peak current drawn after saturation is in excess of 3.5 amps with a pulse width of approximately 4 microseconds. This pulse width is approximately equal to the recovery time lag of the collector-emitter voltage waveform.

Figure 12 shows the driver current and driver collector-emitter voltage with resistive current limiting applied. The peak current drawn after saturation is approximately 1.3 amps with a pulse width of 3.3 microseconds. This pulse width is approximately equal to the recovery time lag of the collector-emitter voltage waveform. The peak current drawn for this method of current limiting has been reduced to nearly 1/3 of its original value with no current limiting. However, only a slight improvement in recovery time has been produced.

Figure 13 shows the driver current and driver collector-emitter voltage with degenerative feedback current limiting applied. The peak current drawn after saturation is only 0.025 amps with negligible pulse width. The recovery time lag of the collector-emitter voltage is approximately 1.6 microseconds. A significant difference in the collector-emitter waveform of this method of current limiting compared to the previous methods is readily apparent. The additional pulse shown in the collector-emitter waveform is a direct result of the degenerative emitter feedback effect. This additional pulse clearly shows that the driver transistors are no longer saturated during this interval of the cycle. Additional testing has shown that the height and width of this additional pulse are functions of the input voltage.

The experimental testing with the various current limiting techniques investigated have shown that the frequency characteristics of the system are affected by the method of current limiting applied. The curves in figure 14, illustrate this effect. With the no current limiting approach, the peak frequency is 14.7 KC, and a frequency change of approximately 12% is required to maintain a constant output voltage. With the resistive current limiting approach the peak frequency is 14 KC, and a frequency change of approximately 17% is required to maintain a constant output voltage. With the degenerative feedback current limiting approach, the peak frequency drops of 12.3 KC, and a frequency change of 31% is required to maintain a constant output voltage. Investigations are presently being conducted into these effects and will be reported in the next progress report.

Balanced Output Problem

A problem occurred early in the experimental testing with obtaining a balanced output waveform from the push-pull chopper power stage. The asymmetrical output of the push-pull chopper occurred over the entire input voltage range and for all load conditions. The degree of asymmetry was greater at light loads than at full load. This asymmetrical operation of the chopper made operation erratic at low input voltage and heavy load. Conditions were reached where only one side of the push-pull chopper could be pulse width controlled.

Balanced operation of the push-pull chopper could be obtained at specific load and voltage conditions by introducing an imbalance in the driver stage. However, this balanced condition for the chopper existed only over a very limited range of operation.

Preliminary tests indicated that the problem was caused by the input impedance characteristics of the chopper transistors. It appeared that an input impedance mismatch of the chopper transistors reflected an unbalanced load of sufficient magnitude to affect operation of the saturating driver transformer. The chopper transistors used in experimental testing were high frequency switching 2N2880 type devices. These devices have a maximum specified V_{BE} (sat) of 1.2 volts at a collector current of 1 amp and a large signal gain of 10. This results in an input impedance of 12 Ω. However, data for the same conditions result in a typical input impedance of approximately 8 Ω. Further, at light collector currents the input impedance becomes greater than 30 Ω for these devices.

A possible solution to this problem would be to cancel out the impedance variation characteristics of the chopper transistors. To effectively do this would require the series resistors R_2 and R_4 of figure 3 to have values significantly larger than the maximum reflected input impedance characteristics of the chopper transistors. This condition would not be compatible with the high efficiency requirement since significant power losses would now be associated with these resistors. An alternate solution to this problem would be to require matched input impedances for the chopper transistors; this would require both matching of transistor gain and base emitter voltage. In addition, the input characteristics of the transistors would have to be closely matched for all possible voltage and load conditions.

The resultant disadvantages of the solutions discussed above required an investigation for an alternate self-stabilizing chopper scheme. A circuit concept investigated was a single ended version of the basic push-pull chopper. The single ended self-stabilizing chopper power stage is shown in figure 15. Circuit operation is similar to the push-pull chopper except for the output of the driver. The output of the driver is half wave rectified through diodes D3 and D4 and connected in a frequency doubling configuration at the base of transistor Q1. Thus, transistor Q1 operates at twice the

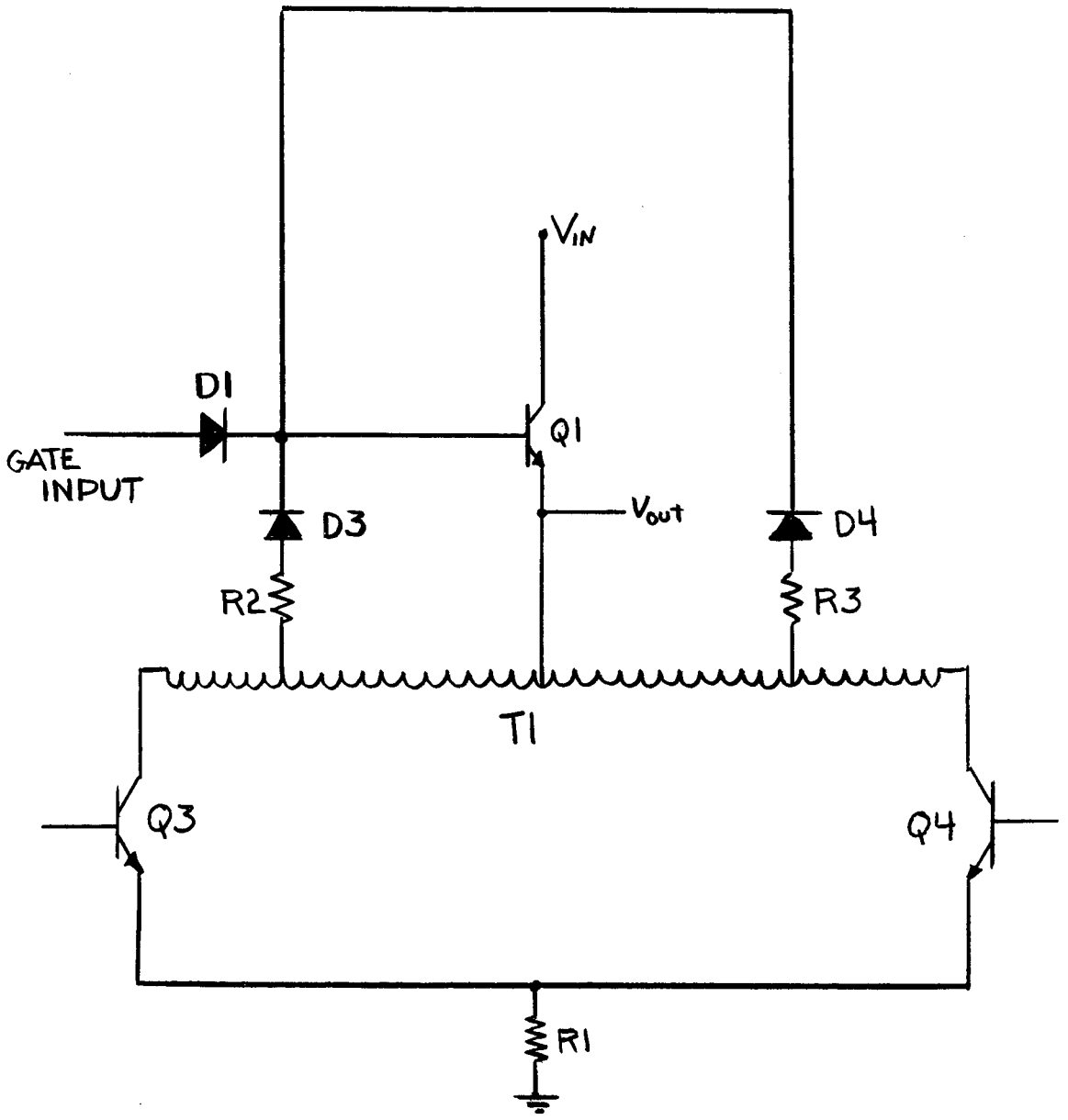


FIGURE 15 SINGLE ENDED SELF-STABILIZING CHOPPER

fundamental frequency of the system. This circuit concept utilizes the full power capability of the driver stage.

The single ended version of the chopper was tested and gave satisfactory performance. All development testing and performance testing discussed in this report was accomplished using the single-ended circuit scheme.

B. FREQUENCY CONTROL STAGES

Investigations were conducted into several methods for obtaining a variable frequency source to be used with the initial development effort of the self stabilizing chopper power stage. These investigations were conducted as a parallel effort with the initial development phase. During the initial development phase frequency sources of varying characteristics were required. The following circuits were breadboarded and evaluated:

1. Unijunction transistor relaxation oscillator
2. Astable multivibrator oscillator
3. Saturable core square wave oscillator

Unijunction Transistor Relaxation Oscillator

The relaxation oscillator circuit is shown in figure 16. This circuit consists of a unijunction transistor oscillator coupled into a bistable multivibrator. The frequency of oscillation is controlled by the R1 C1 time constant and is defined by the equation $f = \frac{1}{R1\ C1\ \ln\left(\frac{1}{1-n}\right)}$ where n is the intrinsic standoff ratio of the unijunction transistor.

Circuit operation can be described as follows: Capacitor C1 charges through resistor R1 towards the supply voltage. The unijunction transistor remains in a high impedance state until a fraction of the supply voltage is developed across the charging capacitor, this voltage being defined by the intrinsic standoff ratio of the device. At this voltage the unijunction fires into a low impedance state. Capacitor C1 discharges into the device thus producing a positive pulse across resistor R3. The height and width of this pulse are determined by the characteristics of the unijunction and the component values of this circuit.

This pulse is inverted and amplified by Q2 and applied to the triggering network of the bistable multivibrator whose operation can be described as follows: Assume Q4 is on and Q3 is off. Resistors R10 and R11 are holding diodes D1 and D2, respectively, reversed biased. The inverted pulse from transistor Q2 is coupled across capacitors C2 and C3 to the cathodes of D1 and D2, forward biasing D2. This decreases Q4 base drive, thus increasing Q3 base drive. This process is regenerative and proceeds until Q3 is on and Q4 is off.

The resulting output is a half cycle of a square wave, the other half cycle being formed when the relaxation oscillator fires again. Thus the frequency of the multivibrator is one-half that of the oscillator.

The unijunction relaxation oscillator has many features of operation. The first feature is circuit simplicity. A second feature is stable frequency response due to the frequency being dependent on only one RC charging network.

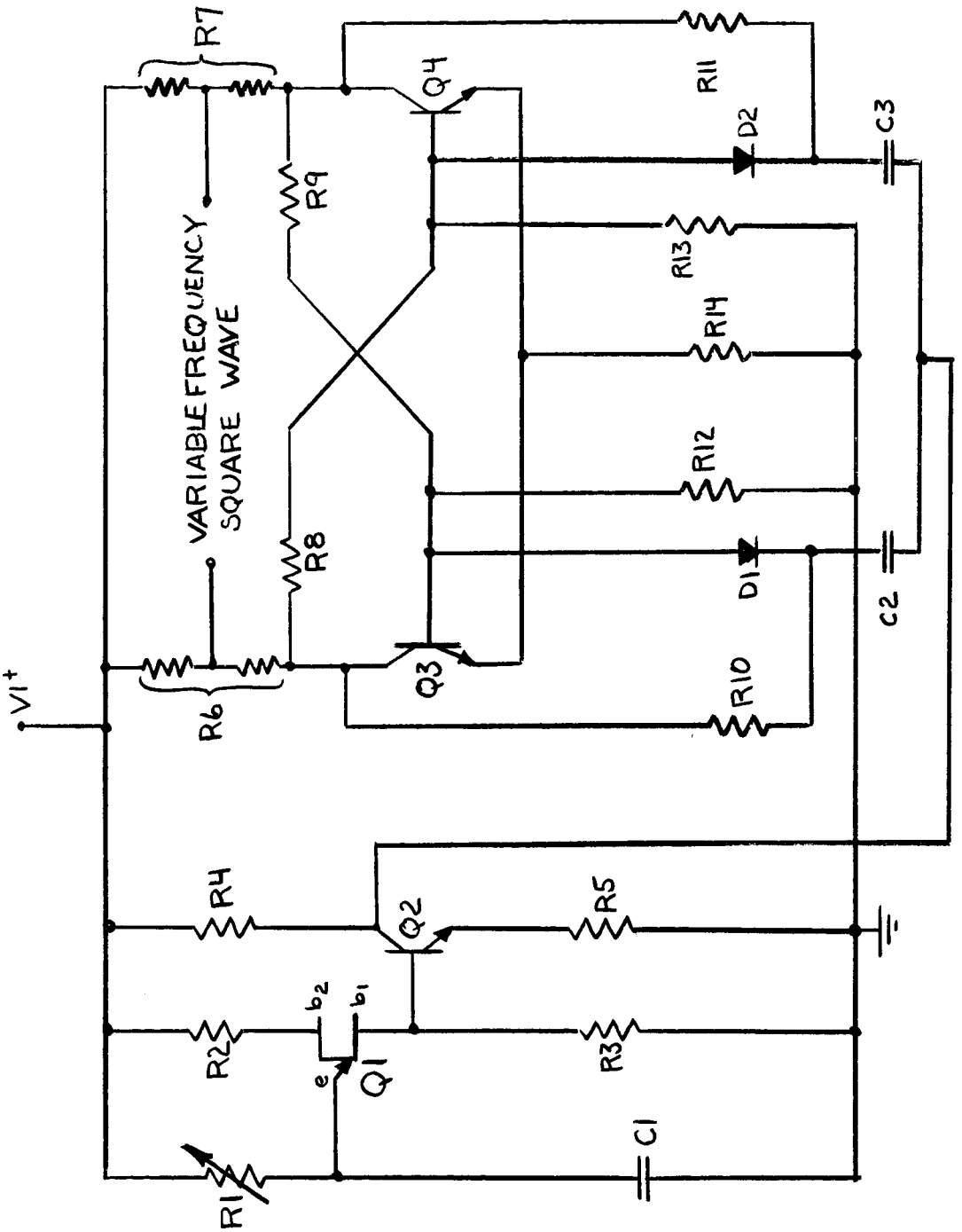


Figure 16 UNIJUNCTION TRANSISTOR OSCILLATOR

A third feature is a simple method of obtaining a range of frequencies by varying only one parameter, the resistance. This is achieved by utilizing the variable resistance characteristics of a transistor. A fourth feature is a frequency range of greater than 3 - 1 which is obtained by variation of this RC time constant.

Although the unijunction relaxation oscillator operates over a wide range of parameters, there are several limiting conditions which must be considered to satisfy operation. The first condition is a maximum limit of R1 as dictated by the minimum emitter current required to fire the unijunction transistor. This, therefore, sets a limit on the minimum frequency obtainable since the frequency is inversely proportional to the resistance. The second condition is a minimum limit for capacitor C1 below which the amplitude of the emitter voltage will decrease. This decreases the frequency stability, the allowable range of R1 and the output voltage developed across R3. The third condition is that the voltage across R3 is always some fraction of the supply voltage, as defined by the base one to emitter resistance and resistor R3. Therefore, if the supply voltage is low, very low output voltage will be developed.

Experimental Results

A unijunction relaxation oscillator was breadboarded, and a supply voltage of 9 volts was used to simulate the output of the 10 watt chopper. A 2N2647 unijunction transistor was used because the minimum emitter current required to fire the device is lower than that of the older 2N489 family by a factor of 10 - 1. A wide range of frequencies at high frequency is, therefore, obtainable but at a low supply voltage of 9 volts. This can be achieved only at a much higher supply voltage with the 2N489 family.

With capacitor C1 equal to .0082μf and R1 variable from about 30 KΩ to 4.8KΩ, a frequency range of 4,000 cps to 24,000 cps or a 6 - 1 range was recorded.

Only preliminary design calculations were made for frequencies up to 60 KC/s, A nine volt supply and a 2N2647 unijunction transistor were used as before. A low capacitance of .002 μf and less was used to satisfy the high frequency requirement. From the results it was concluded that there would not be enough output voltage developed to fire the next stage. This was caused by the low supply voltage of nine volts and by the capacitance being 0. 002 μf and less. The effect of a low capacitance value is described in limiting condition #2.

Astable Multivibrator Oscillator

This circuit is shown in figure 17. It consists of an astable multivibrator coupled into a bistable multivibrator. The frequency of operation is set by the R3-C1 and R4-C2 time constant and is defined by the equation

$$F = \frac{1}{2(R3\ C1)\ \ln\left(1 + \frac{V1}{Vc}\right)}$$

To understand the operation of the astable multivibrator, assume that Q2 is being held on by the current through R4 and that Q1 is being held off by a reverse voltage from C1. C2 charges towards V1. C1 charges towards Vc-Vo. When C1 develops a slightly positive voltage with respect to ground on the base of Q1, the transistor conducts, lowering its collector voltage. This voltage drop is coupled across C2 to Q2 and begins to turn Q2 off. This process proceeds until Q1 is on and Q2 is off. The resultant output is a half cycle of a square wave, the other half cycle being formed when Q1 turns off and Q2 turns on.

Diodes D1 and D2 from emitter to base on Q1 and Q2 clamp the reverse emitter voltage seen by the off transistor. Diodes D3 and D4 prevent C1 and C2 from discharging through diodes D1 and D2.

The output signal from the oscillator gates the bistable multivibrator on and off, producing a square wave output whose frequency is one-half that of the astable multivibrator.

The features of operation of the astable multivibrator are as follows: The first feature is a frequency of oscillation which is independent of supply voltage unlike the unijunction transistor relaxation oscillator. A second feature is a frequency range which is proportional to the natural logarithm of the ratio of voltage Vc to the sum of Vc and the supply voltage, V1. However, this range is limited by the minium value of Vc which will still provide sufficient base drive to turn the transistors on into saturation.

One limitation involved in the operation of the astable multivibrator is its inherent frequency drift. This is due to fluctuations in supply voltage which will vary the charging of the capacitor. Thus, the firing point of the off transistor will not always occur with the same half period of oscillation. A further limitation is the asymmetry of the collector waveform because of component tolerances within the circuit.

Experimental Results

An astable multivibrator was breadboarded, and a 9 volt supply voltage was used to simulate the output of the 10 watt chopper.

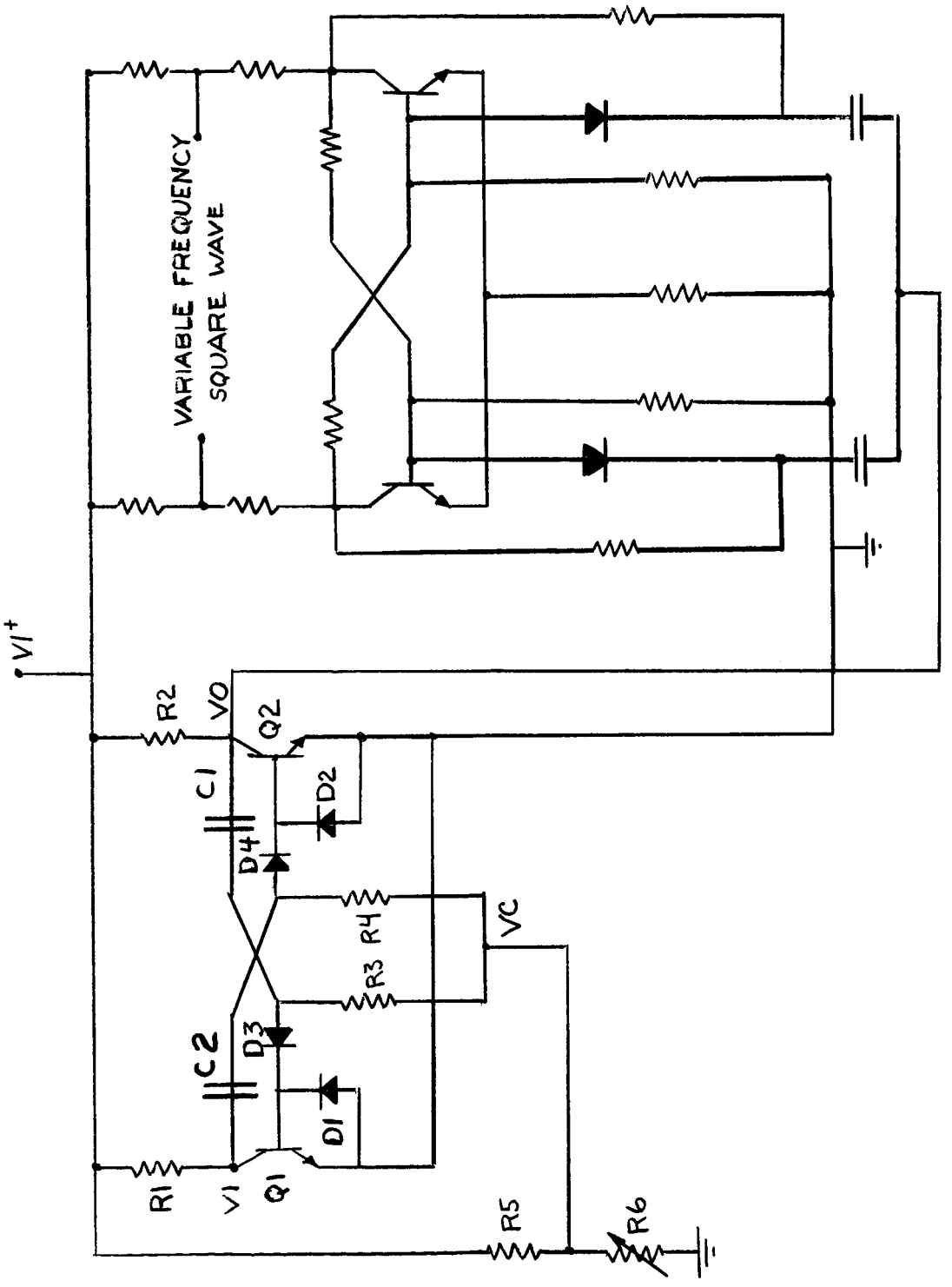


Figure 17 ASTABLE MULTIVIBRATOR OSCILLATOR

Through variation of the R3-C1 and R4-C2 time constant, frequencies up to 80 Kc/s were obtained. However, the maximum frequency range was limited to about 1 1/2 to 1 because the frequency bottomed out when voltage Vc approached four volts or less. This occurred because insufficient base drive was developed to drive the transistors into saturation. The transistors still switched on, but never went into saturation. Thus, the frequency increased nonlinearly as Vc was varied below four volts.

The frequency also tended to drift about 15 cps because of the variation in the firing point of the off transistor.

Saturating Core Square Wave Oscillator

This circuit is shown in figure 18. It consists of a push-pull amplifier, a saturating transformer which supplies base drive to the transistors and an output coupling transformer.

Circuit operation can be described as follows. When voltage is applied, the starting circuit consisting of diode D1, and resistor R4 forward biases either transistor Q1 or Q2 into conduction. Regeneration occurs through the feedback loop consisting of resistor R1 and drive transformer T1.

Transformer T1 is designed to saturate, after a given time, with the available supply voltage. As the core of T1 saturates, it demands more magnetizing current. This increased current causes an increased voltage drop across R1, which causes a decrease in the primary voltage of T1. Degeneration takes place until transistor Q1 no longer conducts and polarity reversal occurs. Transistor Q1 becomes forward biased and the cycle repeats itself.

The frequency of oscillation is defined by the equation $f = \frac{E \times 10^8}{4N B A}$ where N is the number of turns on the primary, B is the flux density in lines/sq. inch, and A is the cross sectional area of core in sq. inches. The voltage, E impressed across the primary of transformer T1, is a square wave with a peak amplitude equal to twice the supply voltage minus the drop across the feedback resistor R1.

This circuit has many features of operation. The first feature is its stable frequency response, since for a fixed applied voltage, the frequency stability is dependent only on the saturation flux density of the driver transformer core. A second feature is that frequency control can be made dependent on only one parameter, the applied voltage E. Variation of the applied voltage E is easily accomplished by varying the feedback resistor R1; variation of R1 can be achieved by utilizing the variable resistance characteristic of a transistor. Another feature of operation of this circuit is that there is no frequency limitation due to the supply voltage magnitude.

The range of frequency of the oscillator is determined by two conditions. The minimum base-emitter voltage required to drive the switching transistors Q1 and Q2 determines the lower limit of operating frequency. The maximum rated reverse bias base-emitter voltage determines the upper limit of operating frequency.

A serious limitation of this circuit, compared to the previous circuits investigated, is that transformers are required.

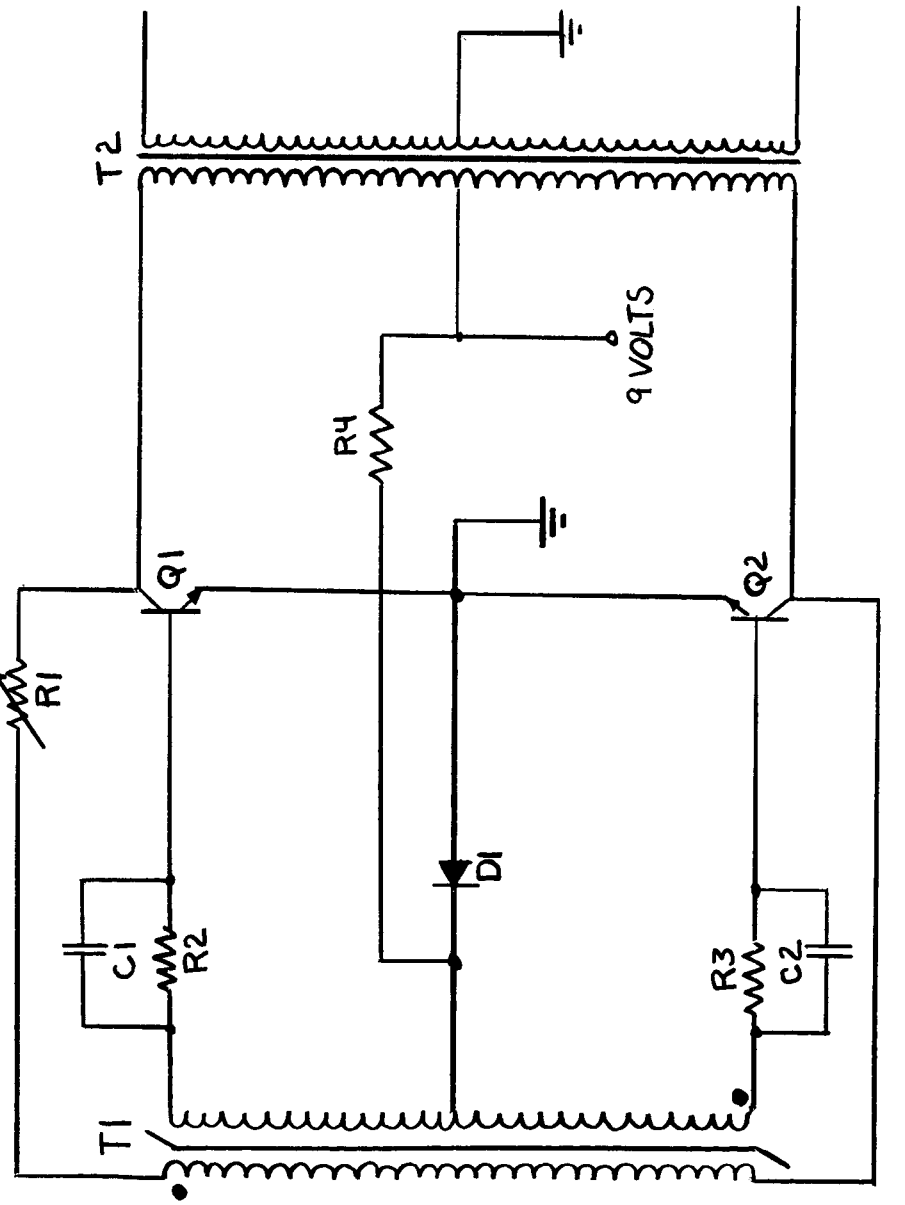


Figure 18 SATURATING CORE SQUARE WAVE OSCILLATOR

Experimental Results

The saturable core square wave oscillator was breadboarded and a supply voltage of 10 volts was used. A 2N1893 type transistor was used for transistors Q1 and Q2, because its maximum reverse bias base-emitter voltage rating of 7 volts would allow for a relatively large range of frequency operation.

Test results showed that a frequency range of about 2.5 to 1 was obtained. The change in frequency was proportional to resistor R1, with frequency decreasing for increasing R1. However, the circuit exhibited a bottoming effect with further increases in resistor R1 resulting in increases in the output frequency of the circuit. This bottoming effect was probably caused by a current limiting condition set by resistor R1 on the feedback network of the oscillator.

C. EFFICIENCY VERSUS FREQUENCY

Efficiency tests were run on the self stabilizing chopper power stage and output filter at several switching frequencies. These tests were performed to determine the frequency-efficiency characteristics of this circuit. The power stage was operated in a single ended configuration, and a constant 470Ω load (approximately 2% load) was maintained across the output terminals to simulate normal control circuit loading. The efficiency measurements were based on power measurements at the input of the chopper power stage and at the output of the filter. The input power measurements included gate drive power but did not include frequency control stage power or buffer driver stage power. Efficiency measurements were made for nominal switching frequency designs of 5, 10, 20, and 30 KC. The degenerative feedback current limiting technique was used in these tests.

The results of the frequency-efficiency tests are shown in tables 3 through 6. Figure 19 shows the full load efficiency versus input voltage for each of the frequencies tested. The curves also show that the drop off of efficiency is more rapid for the higher switching frequencies. The peak efficiency for the 5KC test was 91.5% whereas the peak efficiency for the 30 KC test was 86.3%; both of these points occurred at 10 volts input. At 20 volts input the efficiency for the 5KC test dropped to 79.0% whereas the efficiency for the 30KC test was only 68.6%.

Investigations were conducted to determine the distribution of losses in the circuit. Instrument measurements were made at the input and output of the circuit. Waveform analysis at the input to the filter was performed to determine the input power to the filter. The power losses of the power stage and driver stage were obtained by subtracting the input power to filter from the total input power to the circuit. Measurements were made for the 20 KC test and are summarized below:

Input Voltage	Input Power	Output Power	Drive Losses	Filter Losses
10V	11.0	9.40	0.50	1.10
13V	11.7	9.45	0.40	1.85
15V	12.1	9.45	0.60	2.05
20V	12.8	9.45	0.95	2.40

This data should be interpreted as only indications of the distribution of losses, since errors were introduced in the waveform analysis of the power input to the filter. These errors were a result of the simplifications made to the voltage and current waveforms so that simple graphical methods could be utilized.

The bulk of the power losses were in the filter circuit with the losses

TABLE 3 EFFICIENCY DATA FOR 5KC/S FREQUENCY EFFICIENCY TEST - TRANSFORMER P

E in (Volts)	I in (Amps)	E out (Volts)	I out (Amps)	P in (Watts)	P out (Watts)	Efficiency (%)	Frequency (CPS)
			No Load				
10	.051	9.00		.510			3789
12	.059	9.01		.708			3740
14	.063	9.01		.880			3623
16	.065	9.00		1.04			3507
18	.066	9.00		1.19			3400
20	.0665	8.99		1.33			3300
			1/4 Load				
10	.300	9.01	.287	3.00	2.59	86.3	3935
12	.265	9.01	.287	3.17	2.59	81.8	3879
14	.242	9.01	.287	3.39	2.59	76.5	3834
16	.225	9.00	.287	3.60	2.59	72.0	3764
18	.210	9.01	.286	3.88	2.57	66.9	3690
20	.195	9.01	.286	3.90	2.57	66.0	3631
			1/2 Load				
10	.530	9.00	.535	5.30	4.82	91.0	4036
12	.460	9.00	5.35	5.51	4.82	87.5	3978
14	.415	9.01	.535	5.81	4.82	83.0	3922
16	.380	9.01	.535	6.08	4.82	79.3	3870
18	.350	9.01	.537	6.30	4.84	76.5	3801
20	.325	9.01	.542	6.50	4.87	74.2	3734
			3/4 Load				
10	.780	9.00	.800	7.80	7.20	92.3	4123
12	.680	8.99	8.00	8.15	7.20	88.4	4072
14	.600	9.00	.800	8.40	7.20	85.7	4010
16	.540	9.01	.800	8.64	7.20	83.3	3963
18	.490	9.01	.800	8.80	7.20	81.9	3886
20	.450	9.01	.800	9.00	7.20	80.0	3825
			Full Load				
10	1.030	9.01	1.05	10.30	9.45	91.5	4230
12	.880	9.01	1.05	10.57	9.45	89.5	4158
14	.775	9.00	1.05	10.85	9.45	87.0	4078
16	.710	9.00	1.05	11.35	9.45	83.3	4040
18	.645	9.01	1.06	11.61	9.52	82.0	3970
20	.600	9.00	1.07	12.00	9.63	80.2	3916

TABLE 4 EFFICIENCY DATA FOR 10KC/S FREQUENCY
EFFICIENCY TEST - TRANSFORMER Q

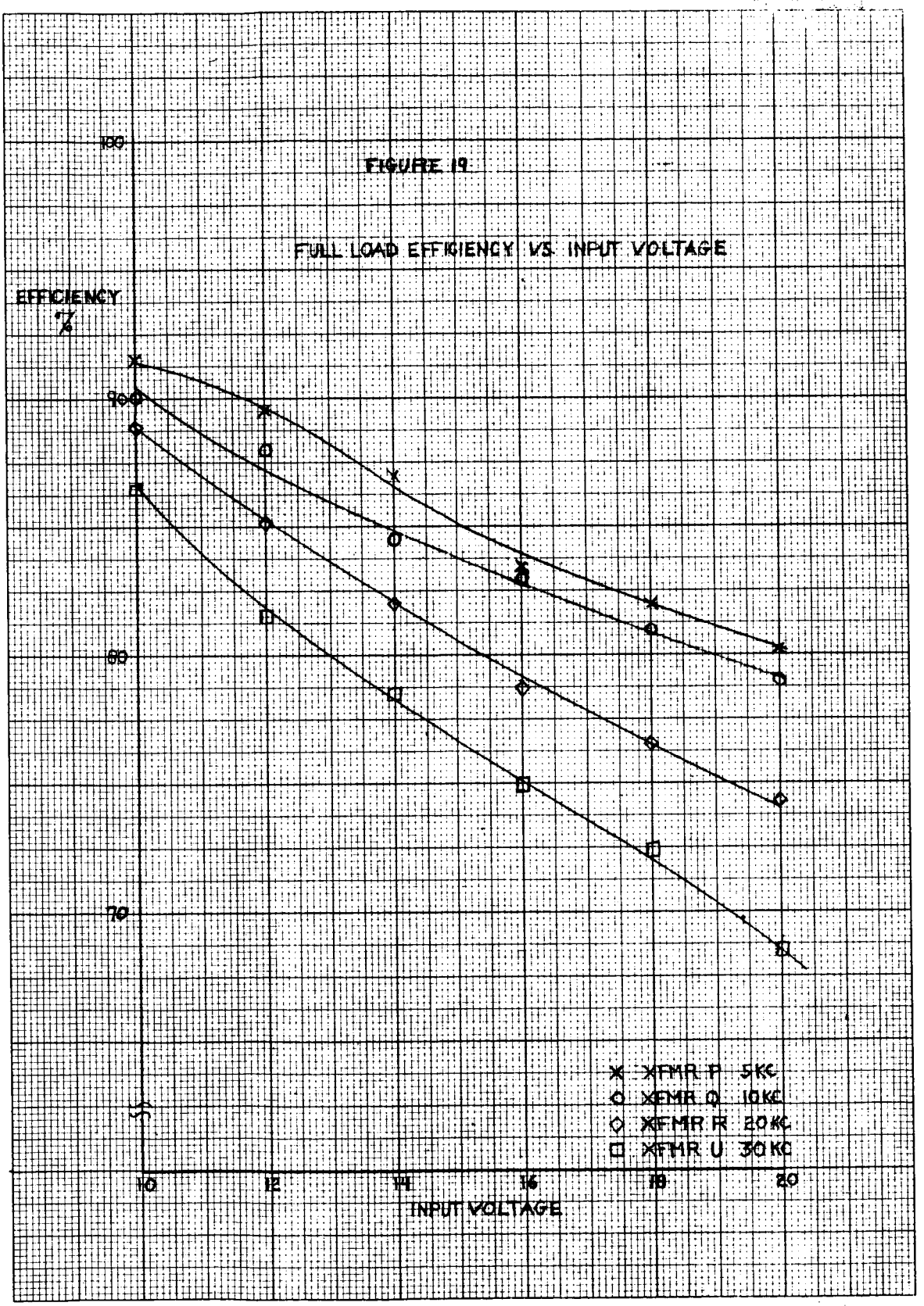
E in (Volts)	I in (Amps)	E out (Volts)	I out (Amps)	P in (Watts)	P out (Watts)	Efficiency (%)	Frequency (CPS)
			No Load				
10	.065	9.00		.65			6608
12	.075	9.00		.90			6405
14	.079	9.00		1,11			6138
16	.0815	9.00		1.30			5935
18	.0815	9.00		1.47			5678
20	.0815	9.00		1.63			5481
			1/4 Load				
10	.310	9.01	.290	3.10	2.61	84.0	6954
12	.282	9.00	.290	3.27	2.61	80.0	6754
14	.260	9.00	.290	3.64	2.61	71.6	6545
16	.242	9.01	.290	3.87	2.61	67.4	6393
18	.228	9.01	.290	4.10	2.61	63.6	6177
20	.215	9.01	.290	5.30	2.61	49.2	6024
			1/2 Load				
10	.555	9.01	.550	5.55	4.95	89.0	7235
12	.485	9.01	.550	5.83	4.95	85.0	7003
14	.435	9.00	.550	6.08	4.95	81.4	6785
16	.400	9.01	.550	6.40	4.95	77.2	6648
18	.370	9.01	.550	6.66	4.95	74.3	6492
20	.345	9.01	.550	6.90	4.95	71.7	6296
			3/4 Load				
10	.810	9.00	.820	8.10	7.38	91.3	7395
12	.705	9.01	.810	8.46	7.29	86.0	7211
14	.620	9.00	.805	8.68	7.23	83.3	6985
16	.570	9.01	.810	9.12	7.29	80.0	6868
18	.520	9.01	.810	9.36	7.29	78.9	6699
20	.475	9.01	.805	9.50	7.23	76.2	6522
			Full Load				
10	1.060	9.01	1.06	10.60	9.55	90.0	7619
12	.905	9.00	1.06	10.85	9.55	88.0	7369
14	.810	9.01	1.06	11.34	9.55	84.5	7227
16	.720	9.00	1.06	11.50	9.55	83.0	6996
18	.655	9.00	1.06	11.80	9.55	81.0	6839
20	.610	9.01	1.07	12.20	9.63	79.0	6714

TABLE 5 EFFICIENCY DATA FOR 20KC/S FREQUENCY
EFFICIENCY TEST - TRANSFORMER

E in (Volts)	I in (Amps)	E out (Volts)	I out (Amps)	P in (Watts)	P out (Watts)	Efficiency (%)	Frequency (CPS)
			No Load				
10	.096	9.01		.96			12522
12	.106	9.00		1.27			11885
14	.113	9.00		1.58			11087
16	.112	8.99		1.79			10371
18	.114	9.00		2.05			9.817
20	.113	9.00		2.26			9.288
			1/4 Load				
10	.335	9.00	.290	3.35	2.61	78.0	13660
12	.318	9.01	.289	3.82	2.61	68.3	12670
14	.290	9.00	.290	4.06	2.61	64.3	12017
16	.275	9.00	.290	4.40	2.61	59.4	11446
18	.255	8.99	.290	4.60	2.61	56.8	10818
20	.245	9.00	.290	4.90	2.61	53.3	10353
			1/2 Load				
10	.570	9.01	.550	5.70	4.95	86.9	14261
12	.510	9.00	.545	6.11	4.90	80.3	13405
14	.470	8.99	.545	6.58	4.90	74.5	12522
16	.425	9.00	.545	6.80	4.90	72.1	12035
18	.393	9.00	.545	7.07	4.90	69.4	11390
20	.370	9.02	.545	7.40	4.90	66.3	10932
			3/4 Load				
10	.835	9.01	.815	8.35	7.33	87.9	14967
12	.735	9.01	.815	8.83	7.33	83.0	14048
14	.655	9.01	.815	9.16	7.33	80.0	13304
16	.595	9.01	.805	9.50	7.25	76.4	12468
18	.542	9.01	.805	9.75	7.25	74.5	12087
20	.500	9.00	.805	10.00	7.25	72.5	11475
			Full Load				
10	1.075	9.00	1.06	10.75	9.54	88.7	15342
12	.935	9.00	1.06	11.20	9.54	85.1	14502
14	.825	9.00	1.05	11.50	9.45	82.0	13613
16	.750	9.01	1.05	12.00	9.45	78.6	13196
18	.680	9.01	1.05	12.30	9.45	76.6	12470
20	.630	9.00	1.04	12.60	9.36	74.3	12367

TABLE 6 EFFICIENCY DATA FOR 30KC/S FREQUENCY EFFICIENCY TEST-TRANSFORMER

E in (Volts)	I in (Amps)	E out (Volts)	I out (Amps)	P in (Watts)	P out (Watts)	Efficiency (%)	Frequency (CPS)
			NO LOAD				
10	.120	9.00		1.20			17409
12							
14	.155	9.01		2.17			15243
16	.155	9.01		2.48			13866
18	.153	9.01		2.76			12925
20	.150	9.01		3.00			12229
			1/4 Load				
10	.360	9.00	.290	3.60	2.61	72.4	18934
12	.342	8.99	.290	4.10	2.61	63.6	17447
14	.325	9.00	.290	4.55	2.61	57.3	16487
16	.312	9.01	.290	5.00	2.61	52.2	15442
18	.295	9.00	.290	5.31	2.61	49.1	14265
20	.280	9.01	.290	5.60	2.61	46.6	13840
			1/2 Load				
10	.595	9.00	.550	5.95	4.95	83.2	19788
12	.540	9.00	.550	6.48	4.95	76.4	18495
14	.490	9.00	.540	6.86	4.86	71.0	17248
16	.465	9.02	.545	7.44	4.90	65.9	16278
18	.430	9.00	.545	7.74	4.90	63.4	15324
20	.405	9.00	.545	8.10	4.90	60.5	14305
			3/4 Load				
10	.865	9.01	.810	8.65	7.29	84.2	20965
12	.760	9.00	.810	9.13	7.29	79.7	19241
14	.680	9.00	.810	9.50	7.29	76.8	18132
16	.635	9.00	.810	10.15	7.29	71.7	17161
18	.590	9.03	.810	10.62	7.29	68.5	16061
20	.545	9.00	.810	10.90	7.29	66.8	15189
			Full Load				
10	1.115	9.01	1.07	11.15	9.61	86.3	22175
12	.975	9.01	1.06	11.70	9.54	81.5	19907
14	.860	9.01	1.05	12.05	9.46	75.5	18789
16	.790	9.01	1.05	12.62	9.46	74.9	17848
18	.725	9.00	1.05	13.10	9.46	72.3	16752
20	.675	9.01	1.03	13.50	9.28	68.6	15560



increasing significantly with input voltage. Preliminary tests showed that a significant portion of the power losses at high input voltage occurred across the free wheeling diode. The diode used was a fast switching type, but had a typical forward drop of 0.8 volts at 1 amp. The conduction time of this diode increased to nearly 50% at 20 volts input because of the duty cycle requirement. The remainder of the losses in the filter occurred primarily across the choke as combined AC and DC losses with the DC losses alone being approximately one half watt.

The power stage and driver stage showed relatively high efficiency of operation; the average efficiency of these stages over the input voltage range was 94%. Measurements were made of the drive losses at the input of the main chopper transistor. The drive power was mainly a function of the input voltage and was relatively independent of load. For example, the drive power at 10 volts input varied from 105 milliwatts at no load to 110 milliwatts at full load; the drive power at 20 volts input varied from 405 milliwatts at no load to 470 milliwatts at full load.

The no load losses versus input voltage for each of the frequencies tested are shown in figure 20. These curves show the same general result as the full load efficiency curves. Note that the no load losses are nearly linear with increasing input voltage. These curves exhibit the non linear input impedance characteristic that is typical of the non-dissipative type regulated converter system.

The curves in figure 21, show the efficiency characteristic of the 30KC chopper under varying loads and input voltages. The following analysis could be made for a constant input voltage and varying load:

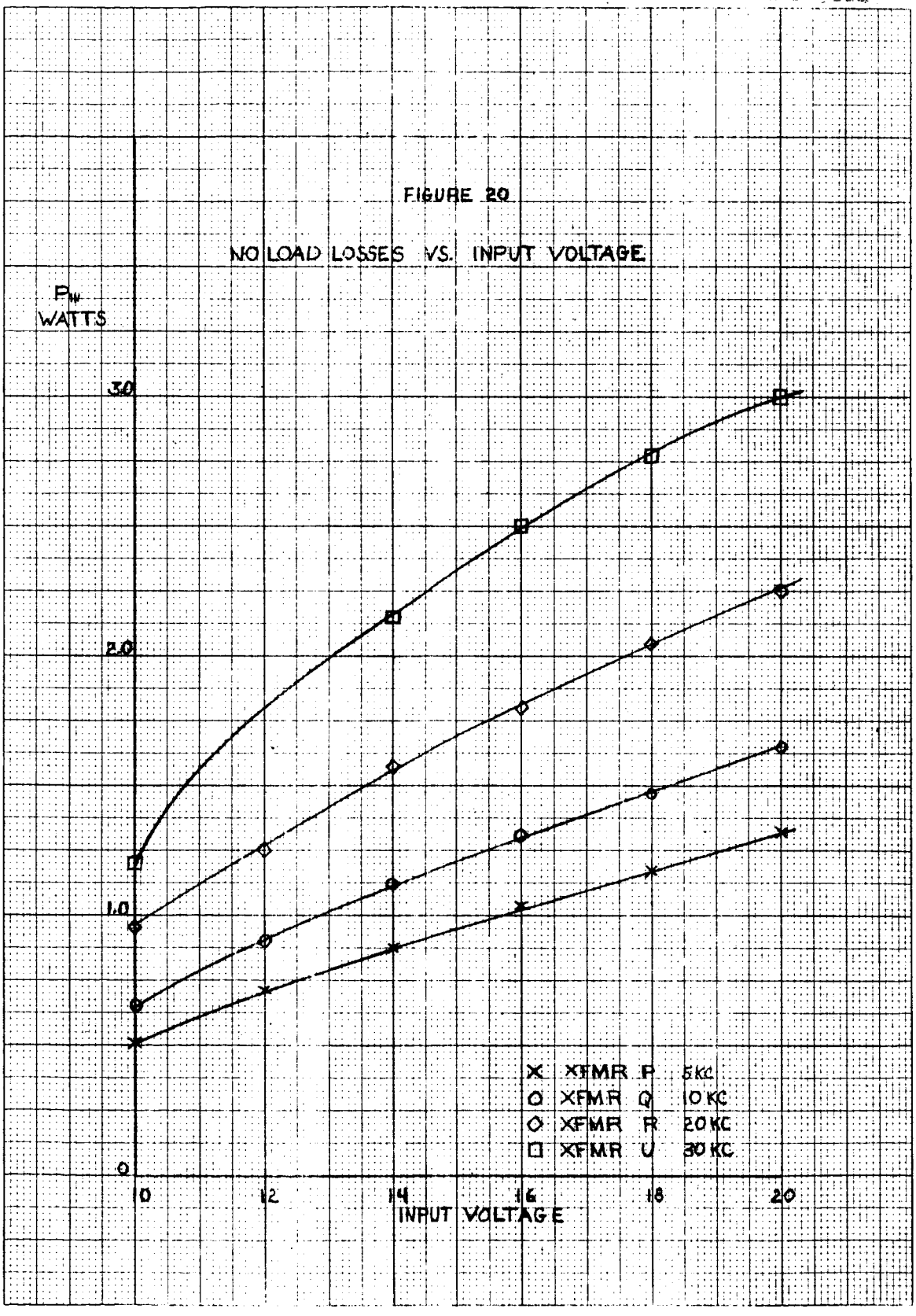
1. Drive losses are nearly constant since they have been shown to be voltage dependent only.

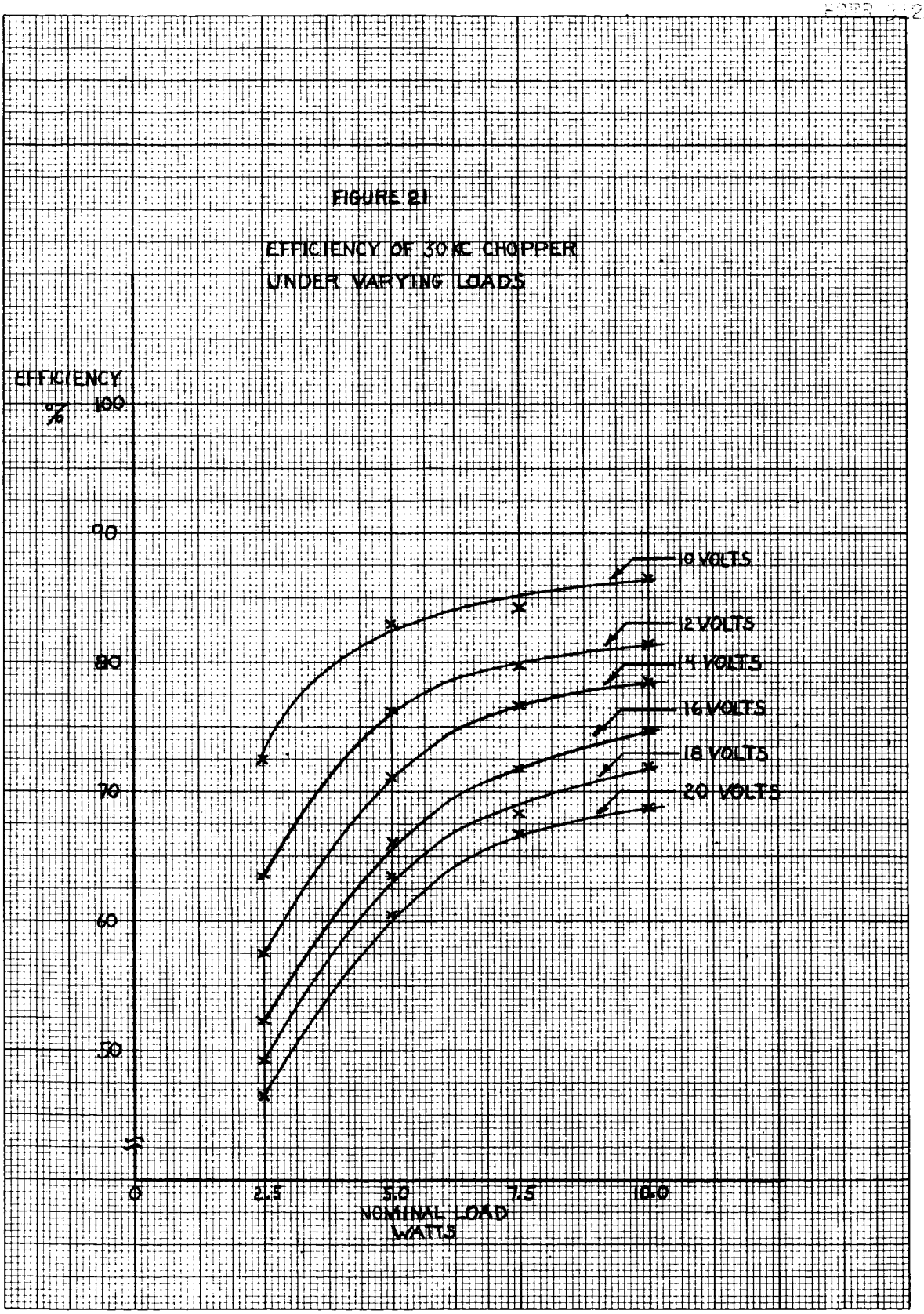
2. AC losses across the choke tend to increase for increasing load. because the switching frequency increases with increasing load.

3. DC losses across the choke increase rapidly for increasing load.

4. Free wheeling diode losses tend to decrease for increasing load, because increasing switching frequency decreases the free wheeling diode on time.

These losses, when combined, would produce the characteristics of these curves.





D. SIZE AND WEIGHT ANALYSIS OF THE 10 WATT CHOPPER-REGULATOR

A size and weight analysis was made on the chopper-regulator circuit shown in figure 22. The system schematic breaks the circuit into its several functional sections namely; the frequency control stage, the driver/gate stage, the main chopper stage, and the output filter stage. The size and weight analysis was conducted as a parallel effort along with the initial development work. Consequently, the main chopper stage shows the push-pull connection rather than the single ended connection finally adopted. The size and weight analysis was not modified for the single ended configuration as negligible weight changes would be involved.

Several switching frequencies were analyzed in an effort to determine the optimum frequency of operation for the circuit. The following switching frequencies were considered.

5 KC/S
10 KC/S
15 KC/S
20 KC/S
25 KC/S
30 KC/S

The assumptions on which the size and weight analysis were made are:

1. Resistors, Small Signal Capacitors, Diodes and Transistors

All components, except stud-mounted types, were taken as single geometric cylinders since the leads were considered negligible. For stud-mounted components, the size and weight of the mounting hardware were included.

2. Transformers

The size and weight estimates for all transformers were based on actual design. The designs were made for one frequency and appropriate scaling was made for the other frequencies.

3. Output filter

Output filter values were determined experimentally for two frequencies. Actual choke designs were made based on this experimental data and appropriate scaling factors were used for the remaining frequencies. Size and weight estimates were based on the following filter values:

Frequency	Inductance	Capacitance
5 KC	5 mh	120 μf
10 KC	3 mh	60 μf
15 KC	2 mh	40 μf
20 KC	1.5 mh	30 μf
25 KC	1.0 mh	25 μf
30 KC	.8 mh	20 μf

Tables 7 through 10 summarize the size and weight analysis for the circuit shown in figure 22. The total results are:

Frequency	Weight	Size
5 KC	.6490 lbs.	5.4822 cu. in.
10 KC	.5642	4.7220
15 KC	.4954	4.4408
20 KC	.4276	4.1248
25 KC	.3434	3.4322
30 KC	.2769	2.8674

No size and weight estimates were made on the voltage regulator circuit or on the input filter circuit since breadboard development work is still required for these circuits. However, it could be safely assumed that the resultant size and weight of the voltage regulator circuit would approximate that of the frequency control stage; also, the input filter size and weight would approximate that of the output filter.

The curve in figure 23, summarizes the size and weight analysis taking into account the voltage regulator and input filter stages. To insure meeting the design goal weight of 0.63 pounds for the 10 watt chopper regulator, the switching frequency should be at least 25 KC. The component weight versus switching frequency shows a fairly linear characteristic with a fall off rate of approximately 0.03 lbs/KC. The decrease in component volume is not linear but exhibits similar slope changes at 10 KC, 20 KC, and 30 KC. Around these points the fall off rate of volume is approximately 0.2 cu. in./KC. The non linearity of the volume characteristic is primarily associated with the non linear step changes in volume of the physical components, specifically that of the chokes.

The peak efficiency points discussed in section c are also shown in figure 23 Note that the peak efficiency is relatively flat over the frequency range 10 to 20 KC, whereas the component weight and volume are dropping off at a nearly linear rate. Note also that for frequencies below 10 KC the peak efficiency tends to flatten while component size and weight are continuing to increase. Also for frequencies above 20 KC the peak efficiency tends to begin falling off more rapidly than the size and weight decrease. This would tend to point to an optimum frequency range of 20 to 30 KC for this type of a power supply system where component size and weight are minimized and efficiency is maximized.

TABLE 7 WEIGHT AND VOLUME ANALYSIS OF THE FREQUENCY CONTROL STAGE

Type Component (Frequency Independent)	Weight Per Unit (lbs.)	Volume Per Unit (in^3)	No Used	Total Weight (lbs.)	Total Volume (in^3)
Composition Resistor 1/2W	.0014	.0085	3	.0042	.0255
Wirewound Potentiometer	.0060	.1280	1	.0060	.1280
Speed-Up Capacitor	.0040	.0291	2	.0080	.0582
Small Signal Control Transistor	.0030	.0280	2	.0060	.0560
Silicon Diode	.0004	.0024	1	..0004	.0024
Total			9	.0246	.2701

Frequency Dependent Type Component	No Used	At 5KC/s Wt. (lbs.)	At 5KC/s Vol. (in^3)	At 10KC/S Wt. (lbs.)	At 10KC/S Vol. (in^3)	At 15KC/S Wt. (lbs.)	At 15KC/S Vol. (in^3)	At 20KC/S Wt. (lbs.)	At 20KC/S Vol. (in^3)	At 25KC/S Wt. (lbs.)	At 25KC/S Vol. (in^3)	At 30 KC/S Wt. (lbs.)	At 30 KC/S Vol. (in^3)
Driver Transformer	1	.0083	.1997	.0059	.0844	.0059	.0844	.0033	.0486	.0033	.0486	.0026	.0208
Coupling Transformer	1	.0083	.1997	.0059	.0844	.0059	.0844	.0033	.0486	.0033	.0486	.0026	.0208
Total	2	.0166	.3994	.0118	.1688	.0118	.1688	.0066	.0972	.0066	.0972	.0052	.0416
Totals For Frequency Control Stage	11	.0412	.6695	.0364	.4389	.0364	.4389	.0312	.3673	.0312	.3673	.0298	.3117

TABLE 8

WEIGHT AND VOLUME ANALYSIS OF THE DRIVER/GATE STAGE

Type Component (Frequency Independent)	Weight Per Unit (lbs.)	Volume Per Unit (in^3)	No. Used	Total Weight (lbs.)	Total Volume (in^3)
Composition Resistor 1/2W	.0014	.0085	20	.0280	.1700
Coupling Capacitor	.0040	.0291	4	.0160	.1164
Small Signal Control Transistor To-5 Case	.0030	.0280	8	.0240	.2240
Silicon Diode	.0004	.0024	4	.0016	.0097
Totals for Driver/Gate Stage			36	.0696	.5201

The above total weight and volume are the same for all frequencies.

TABLE 9 WEIGHT AND VOLUME ANALYSIS OF THE CHOPPER POWER STAGE

Type Component (Frequency Independent)	Weight Per Unit (lbs.)	Volume Per Unit (in^3)	No. Used	Total Weight (lbs.)	Total Volume (in^3)
Composition Resistor 1/2 W	.0014	.0085	5	.0070	.0425
Small Signal Control Transistor To-5Case	.0030	.0280	2	.0060	.0560
Power Transistor 7/16 HEX	.00392	.1663	4	.0157	.6652
Silicon Diode	.0004	.00243	4	.0016	.0098
Total			15	.0303	.7735

Type Component (Frequency Dependent)	No. Used	At 5KC/S Wt. (lbs.)	At 5KC/S Vol. (in^3)	At 10KC/S Wt. (lbs.)	At 10KC/S Vol. (in^3)	At 15KC/S Wt. (lbs.)	At 15KC/S Vol. (in^3)	At 20KC/S Wt. (lbs.)	At 20KC/S Vol. (in^3)	At 25KC/S Wt. (lbs.)	At 25KC/S Vol. (in^3)	At 30KC/S Wt. (lbs.)	At 30KC/S Vol. (in^3)
Driver Transformer	1	.0083	.1997	.0059	.0844	.0059	.0844	.0033	.0486	.0033	.0486	.0026	.0208
Totals for Chopper Stage	16	.0386	.9732	.0362	.8579	.0362	.8579	.0336	.8221	.0336	.8221	.0329	.7943

TABLE 10

WEIGHT AND VOLUME ANALYSIS OF THE OUTPUT FILTER STAGE

Type Component (Frequency Independent)	Weight Per Unit (lbs.)	Volume Per Unit (in^3)	No. Used	Total Weight (lbs.)	Total Volume (in^3)
Rectifier	.0100	.1880	1	.0100	.1880
Total			1	.0100	.1880

Type Component (Frequency Dependent)	No Used	At 5KC/S Wt. (lbs.)	At 5KC/S Vol. (in^3)	At 10KC/S Wt. (lbs.)	At 10KC/S Vol. (in^3)	At 15KC/S Wt. (lbs.)	At 15KC/S Vol. (in^3)	At 20KC/S Wt. (lbs.)	At 20KC/S Vol. (in^3)	At 25KC/S Wt. (lbs.)	At 25KC/S Vol. (in^3)	At 30KC/S Wt. (lbs)	At 30KC/S Vol. (in^3)
Filter Choke	1	.4323	2.8314	.3575	2.4321	.2915	2.1659	.2343	1.9723	.1529	1.2947	.0913	.8283
Filter Capacitor	1	.0573	.3000	.0545	.2850	.0517	.2700	.0489	.2550	.0461	.2400	.0433	.2250
Total	2	.4896	3.1314	.4120	2.7171	.3432	2.4359	.2832	2.2273	.1990	1.5347	.1346	1.0533
Totals for Output Filter Stage	3	.4996	3.3194	.4220	2.9051	.3532	2.6239	.2932	2.4153	.2090	1.7227	.1446	1.2413

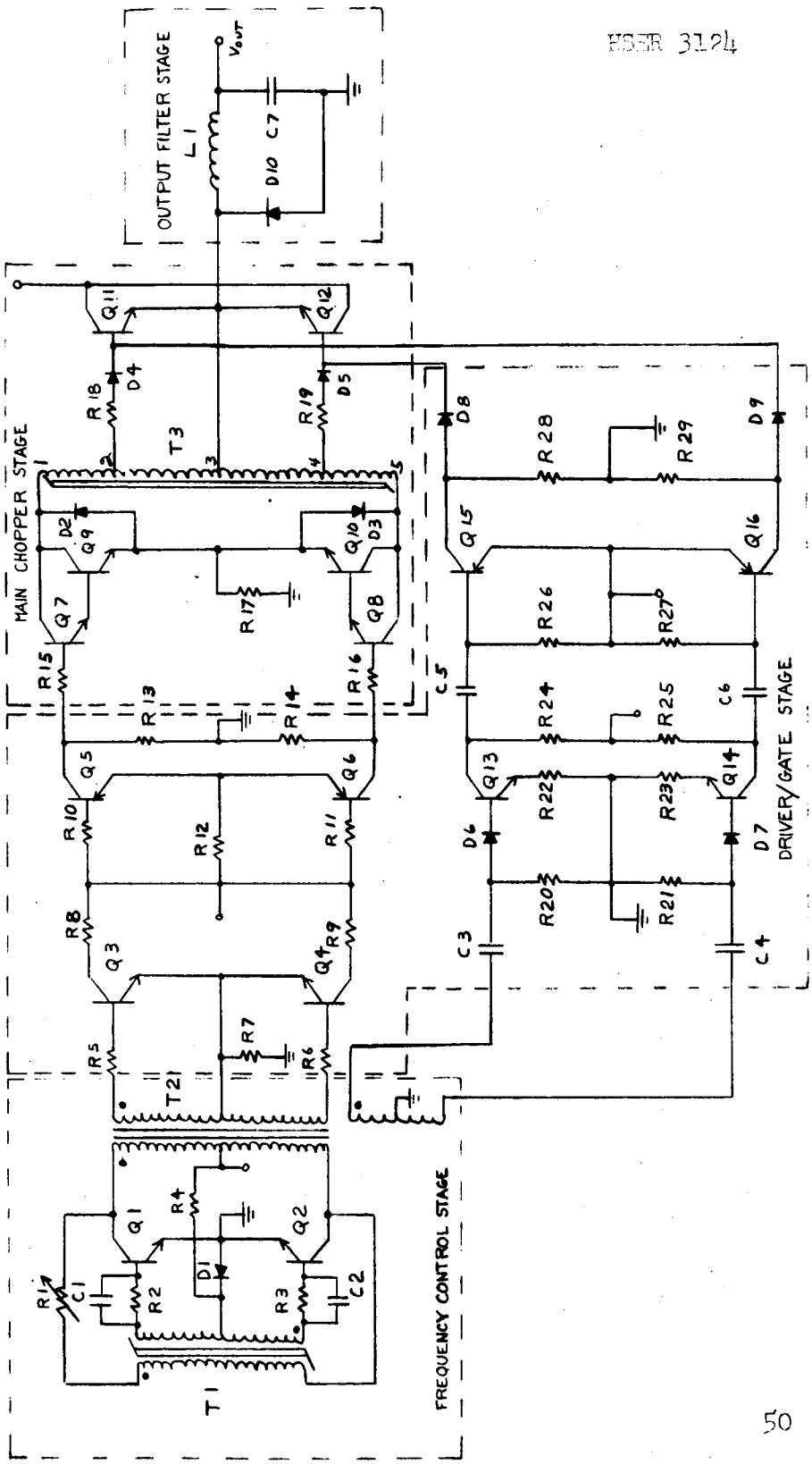


FIGURE 22. SYSTEM SCHEMATIC FOR SIZE AND WEIGHT ANALYSIS

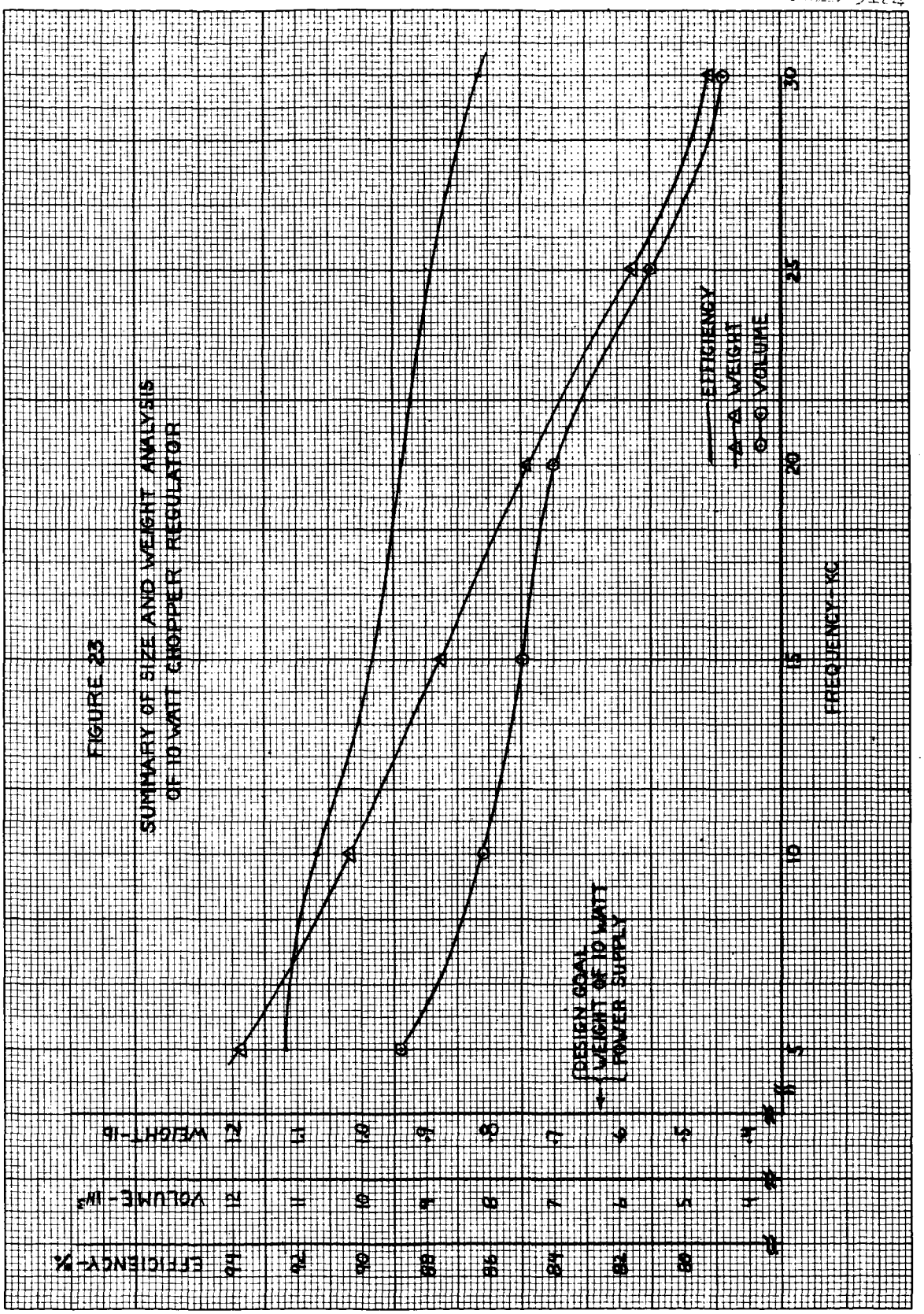


FIGURE 23
SUMMARY OF SIZE AND WEIGHT ANALYSIS
OF 10-WATT CHOPPER REGULATOR

V. CONCLUSIONS AND RECOMMENDATIONS

The final configuration selected for the power stage for the chopper-regulator series is the single - ended self-stabilizing chopper. External gate triggering has been selected as the most suitable means of circuit starting. The degenerative feedback method of current limiting has been shown to be the most effective method of improving circuit recovery time. This method of current limiting requires a significantly larger range of operating frequency to maintain output voltage control; investigations of this effect are presently in progress.

The saturating core square wave oscillator has been selected for this phase of the program as the variable frequency source. The limitations because of the low supply voltage requirement on the frequency range of the unijunction relaxation oscillator and the astable multivibrator oscillator have eliminated these circuits from further consideration for this phase of the program. However, modifications of these circuits should be considered in the follow-on program phase.

The results of the size and weight analysis for the 10 watt chopper regulator have shown that a minimum switching frequency of 25 KC is necessary to meet the design goal weight of 0.63 pounds. The frequency-efficiency tests conducted have shown that the maximum efficiency at this frequency to be limited to approximately 86%. The switching frequency of 25 KC will be selected for the scaling designs of the 25, 50, and 100 watt levels. Indications are that the efficiency at the 100 watt level will meet the design goal of 90%.

The frequency-efficiency tests on the chopper regulator have shown that the peak efficiency occurs at minimum input line and that the rate of efficiency fall off with increasing input line is frequency dependent. For the 5KC test the peak efficiency was 91% and fell off to 79% at maximum input line. For the 30 KC test the peak efficiency was 85% and fell off to 68% at maximum input line. Analysis of these tests have shown that bulk of the power losses are associated with the output filter. Optimization of the output filter in the follow-on program phase should improve this efficiency characteristic.

VI PROGRAM FOR NEXT INTERVAL

During the next quarterly period, effort will be directed to the following areas:

A. Booster Circuit Investigation. Breadboard investigations will be done to extend the self stabilizing concept to the booster converter power stage.

B. Breadboard designs. Scaling designs will be done for the four chopper power supplies and for the four booster power supplies. Performance testing will be done on all power supply breadboards, and detailed temperature testing will be done on one power supply breadboard.

C. Phase II Program. Phase II program will be initiated and will include detailed studies of control circuits, and filter circuits, along with improvements of the presently developed power stage circuits.

VII BIBLIOGRAPHY

The references used during this past quarter and in the preparation of this report are listed below.

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VIII CONFERENCES

A conference was held at NASA, Goddard on July 1, 1965. In attendance were Messrs. F. Yagerhofer and E. Pascuitti representing NASA, and Messrs. F. Trifari and F. Raposa representing HSED. Technical status and contract status of the program were reviewed. Program extension for the phase I program and initiation of the phase II program were discussed and agreed upon

IX NEW TECHNOLOGY

Not applicable during this report period.