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DIGITAL DATA PROCESSOR

PFM SEXADECIMAL-TO-DECIMAL CONVERTER

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GREENBELT, MARYLAND

DIGITAL DATA PROCESSOR
PFM SEXADECIMAL-TO-DECIMAL CONVERTER

by

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DIGITAL DATA PROCESSOR

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SECTION I

GENERAL DESCRIPTION

A. INTRODUCTION

This manual describes the operation and provides maintenance instructions for a Digital Data Processor, PFM Sexadecimal-to-Decimal Converter. This Digital Data Processor performs the basic operations of decoding a pulse frequency modulation signal and performs various operations on the data of that signal.

While the encoder in the satellite is being designed and tested, a simple but efficient decoding system is required to facilitate the design, checkout, and testing of the PFM encoding system. This special-purpose decoding system will transform the coded PFM signal into a digital printout for ease in interpreting the PFM signal. One can experiment with variations in the parameters of the satellite's encoding system and by having an immediate printout of the decimal equivalent of the PFM format, the results of the satellite's encoder experimentation can be analyzed. The inputs of the decoding system, or digital data processor, will be directly "hooked up" to the satellite's encoding system. The digital data processor does not have to contend with noisy signals as would result during the actual transmission from the orbiting satellite. Also, synchronizing signals are available from the encoder which would not normally be transmitted. Therefore, synchronization problems are minimized. The simplified data link from the satellite to the decoder is illustrated in Figure I-A-1. While the encoding system is still in its design, checkout, and test stages, the actual transmission link can be bypassed and the digital data processor used, as illustrated in Figure I-A-2.

Since the digital data processor is a piece of test equipment to be used in facilitating the design of present and future PFM encoders, it has been designed to have maximum flexibility.

The majority components of the system are assembled with the S-PAC line of digital modules manufactured by Computer Control Company, which are contained in sliding tilt drawers mounted in one standard 19" rack. A Franklin Series 1000 Hi-Speed Printer is also mounted in the rack.

This Manual begins with general information, including a brief section on the PFM format that can be decoded in this Digital Data Processor. The basic portion of the Manual is the functional description of the subsystems, giving for each subsystem the function and theory of operation, with photos and logic diagrams.

B. TECHNICAL SPECIFICATIONS

1. System Power

(a) Input Voltage
105 to 125 Vrms

(b) Frequency
60 cps, single phase
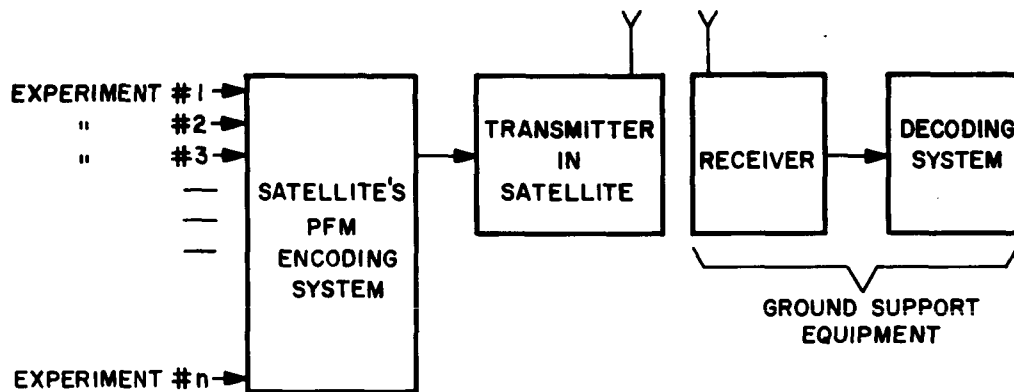
Figure I-A-1 — Simplified Data Link From Experiments to Decoding of Data.
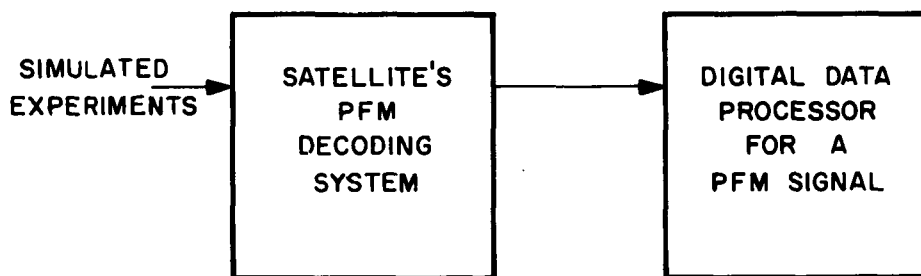
Figure I-A-2 — Digital Data Processor as it is Used in Facilitating the Design and Testing of the Satellite's PFM Encoding System.

(c) Current
   14 amperes

(d) Power Supply Voltages
   Computer Control Company, Model RP-32
      -18 Vdc, 0 to 20 amp
      -6 Vdc, 0 to 20 amp
      +12 Vdc, 0 to 20 amp
   Con Avionics Power Supply, Model R200-0.1-BX
      +200 Vdc, 0 to 0.1 amp

2. Dimensions

(a) Panel Height
   System requires 59-1/2 inches panel height in the rack

(b) Panel Width
   18-3/4 inches

(c) Maximum Chassis Depth
   24 inches

(d) Overall Dimensions
   Height, 71-7/8 inches
   Width, 21-1/16 inches
   Depth, 30-3/4 inches

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3. Mounting

All subsystems are designed for mounting in a standard 19 inch rack. "Chassis Track" slides are provided on all sliding tilt drawers.

4. Construction

Modular-type construction using plug-in printed circuit boards for ease of maintenance

5. Connectors, Printed Circuit

Elco, type 7008-35-5-2, used for Computer Control Company plug-in modules.

6. Accessibility

Most operating controls are accessible from front of system. Certain controls requiring initial adjustment only are mounted on the printed circuit cards, e.g., potentiometers. Access to plug-in modules is accomplished by sliding drawers forward.

7. Environmental Conditions

+10°C to +40°C

SECTION II

DESCRIPTION OF SYSTEM

A. INTRODUCTION

The scope of this section is to describe the system inputs, outputs and to generally indicate signal flow throughout the Digital Data Processor.

B. DESCRIPTION OF SYSTEM INPUTS

The digital data processor will accept the specified PFM format, two synchronization signals, and an automatic processing signal. These signals can come from the satellite's encoding system or from a simulator.

The data or information of a pulse frequency modulation system is contained in the frequency of a burst or tone. The bursts or tones are sequentially transmitted. The location of the burst in the telemetry sequence identifies the parameter being measured. Previously, PFM systems transmitted the frequency burst separated by blank or no signal periods between each frequency burst. This was known as a PFM blank-burst signal. As can be seen, only 50% of the PFM blank-burst signal contains data. In the latest PFM systems, the blanks are also filled with bursts of frequencies; this is known as PFM burst-burst signal and 100% of this signal contains data. This paper deals with the PFM burst-burst signal, the more advanced of the two PFM signals, and all references to PFM signals in what follows are to this type.

1. PFM Format

The PFM format consists of a series of frequency bursts. The frequency during any one burst or channel is constant and only varies from channel to channel. Each frequency burst is one of sixteen discrete frequencies in the 5 K cps to 15 K cps range. A PFM sequence consists of sixteen frames; each frame consists of thirty-two channels; each channel contains a discrete frequency which represents the information transmitted (See Figure II-B-1). Since sixteen frequencies are used, each channel conveys four bits of information. A seventeenth frequency, known as the sync frequency, is used in specific channels for synchronization purposes. Table 1 indicates the sexadecimal level, frequency and input bit configuration used for IMP's D, E, F & G.

2. Synchronizing Signals

The two synchronizing signals, the channel rate signal, and the sequence rate signal are available from the encoding system. While the satellite is in orbit only the PFM signal is transmitted to the ground stations and synchronization must be obtained from the synchronization frequency. While the satellite encoder is being designed and tested, the digital data processor is used and synchronization is obtained from the channel rate signal and sequence rate signal. The channel rate signal is normally 100 cps, which corresponds to a time of 10 milliseconds per channel. The sequence rate signal is also received from the satellite's encoding system. The sequence rate signal can be computed as follows:

Time of one sequence

$$= \frac{\text{\# of channels}}{\text{sequence}} \times \text{time of one channel}$$

$$= \frac{\text{\# of channels}}{\text{frame}} \times \frac{\text{\# of frames}}{\text{sequence}} \times \text{time of one channel}$$
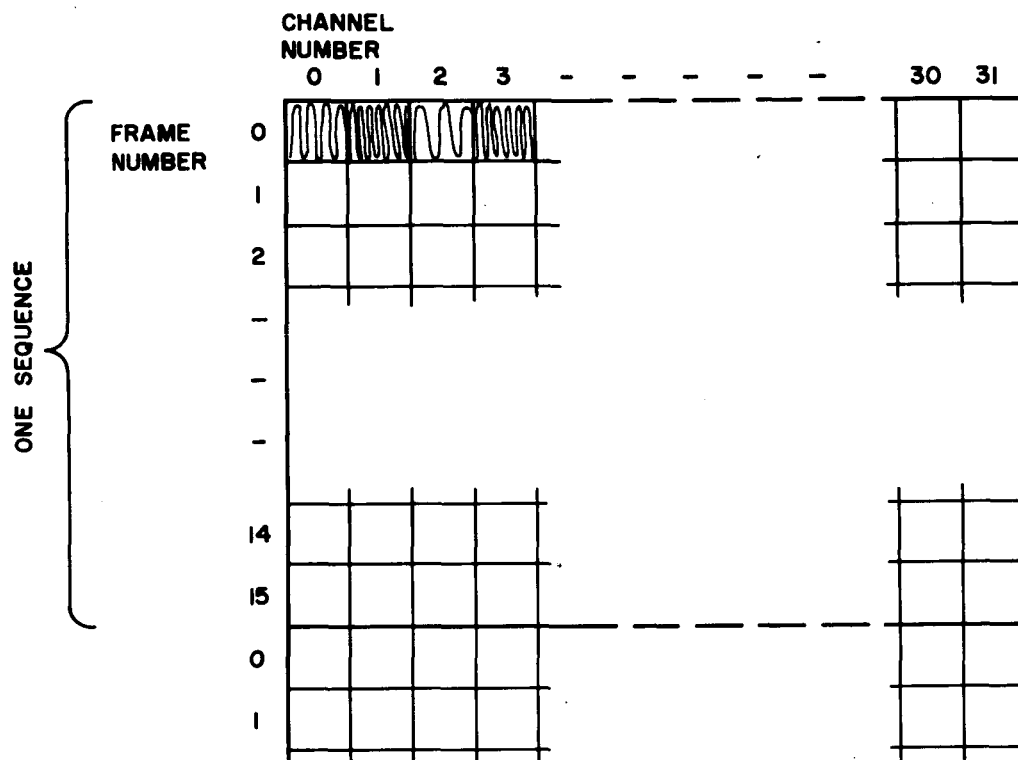
Figure II-B-1 — PFM Format.

Table 1

Sexadecimal Level, Frequency, and
Input Bit Configuration

Sexadecimal Level		Frequency (KCPS)	Input Bit Configuration (Most Significant Bit First)	
0 or	15	6.4	0000 or	1111
1	14	6.8	0001	1110
2	13	7.2	0010	1101
3	12	7.6	0011	1100
4	11	8.0	0100	1011
5	10	8.4	0101	1010
6	9	9.8	0110	1001
7	8	9.2	0111	1000
8	7	9.6	1000	0111
9	6	10.0	1001	0110
10	5	10.4	1010	0101
11	4	10.8	1011	0100
12	3	11.2	1100	0011
13	2	11.6	1101	0010
14	1	12.0	1110	0001
15	0	12.4	1111	0000

$$= 32 \frac{\text{channels}}{\text{frame}} \times 16 \frac{\text{frames}}{\text{sequence}} \times 10 \frac{\text{milliseconds}}{\text{channel}}$$

$$= 5.12 \frac{\text{seconds}}{\text{sequence}}$$

The time of one sequence (5.12 seconds) corresponds to a sequence rate of .1953 sequences/ second. The channel rate may be decreased in a binary fashion, i.e., the channel rate may be 100 cps, 100/2 cps, 100/4 cps, 100/8 cps, 100/16 cps, or 100/32 cps. Table 2 depicts the sequence rate, time to one sequence, and the time of one channel, for the different channel rates.

3. Automatic Processing Signal

The automatic processing signal selects groups of two consecutive channels to be processed. As an example, say channels 2 and 3, and channels 4 and 5, are to be processed. This automatic processing signal for this example, along with the channel rate signal $(2\bar{s})$ and the sequence rate signal $(\bar{A})$ are indicated in Figure II-B-2.

C. DESCRIPTION OF SYSTEM OUTPUTS

The output of the system is a printout on the Franklin Series 1000 Hi-Speed Printer. The printer will record the decimal equivalent of a 24 bit binary number (6 channels × 4 binary bits per channel) along with the frame in which it occurred, the first channel processed, and the number of channels processed. The printer has a top speed of 40 lines per second. Each line consists of 13 decimal digits. The Printer format is as follows.

Frame #	1st Channel Processed	# of Channels Processed	Decimal equivalent of the binary number
X X	X X	X	X X X X X X X X

Table 2

Channel Rate, Time of One Channel, Sequence Rate
and Time of One Sequence

Channel Rate (cps)	Time of One Channel (milliseconds)	Sequence Rate (cps)	Time of One Sequence (seconds)
100	10	.1953	5.12
$\frac{100}{2} = 50$	20	.0977	10.24
$\frac{100}{4} = 25$	40	.0488	20.48
$\frac{100}{8} = 12.5$	80	.0244	40.96
$\frac{100}{16} = 6.25$	160	.0122	81.92
$\frac{100}{32} = 3.125$	320	.0061	163.84
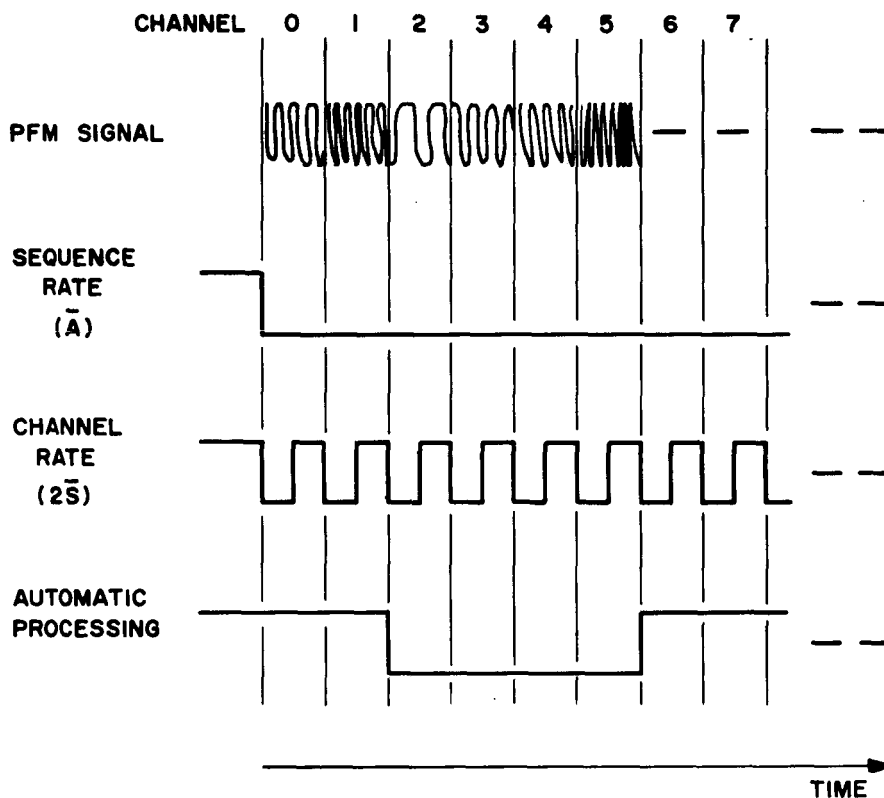
Figure II-B-2 — PFM Signal, Synchronizing Signals (Sequence Rate, Channel Rate) and Automatic Processing for Channels 2, 3 and 4, 5

D. DISCUSSION OF SYSTEM BLOCK DIAGRAM

The Digital Data Processor will accept a PFM signal, the automatic processing signal, the sequence rate signal, and the channel rate signal from the satellite's encoding system or from a simulator. A block diagram of the system is shown in Figure II-D-1.

The PFM signal will pass through an input amplifier and a bandpass filter in order to eliminate noise outside the pass band of 5 KC to 15 KC. The PFM signal will then be presented to the digital filter. The digital filter must be able to distinguish between the 16 frequencies (channels of information) of the PFM signal. The 16 frequencies and their bandwidth are selected and can readily be changed by use of the programming pinboard located on the front panel. A preselected sexadecimal number (1-16) is assigned to each of the 16 frequencies. An accumulating/shift register will accumulate consecutive 4-bit binary numbers (representing the frequency in the channels) for a maximum of six channels. Therefore, the basic word is a 24-bit binary number (6 channels times 4 bits per channel). A binary-to-BCD converter will operate on the 24-bit binary number in the accumulating/shift register and transform it into a BCD (binary coded decimal) number in order to be able to print this number as a decimal number. This decimal number (2^0-1 to $2^{24}-1$ or from 0 to 16,777,215) represents a datum point from one particular experiment or parameter in the satellite. It is also desired to print the location numbers of that decimal number; i.e., the frame and the channel in which the decimal number occurred. The channel occurring, frame occurring and the 8-digit decimal number will be displayed with Nixie tubes. A time control generator will also be required to generate control signals throughout the processor from the channel rate signal and the sequence rate signal.
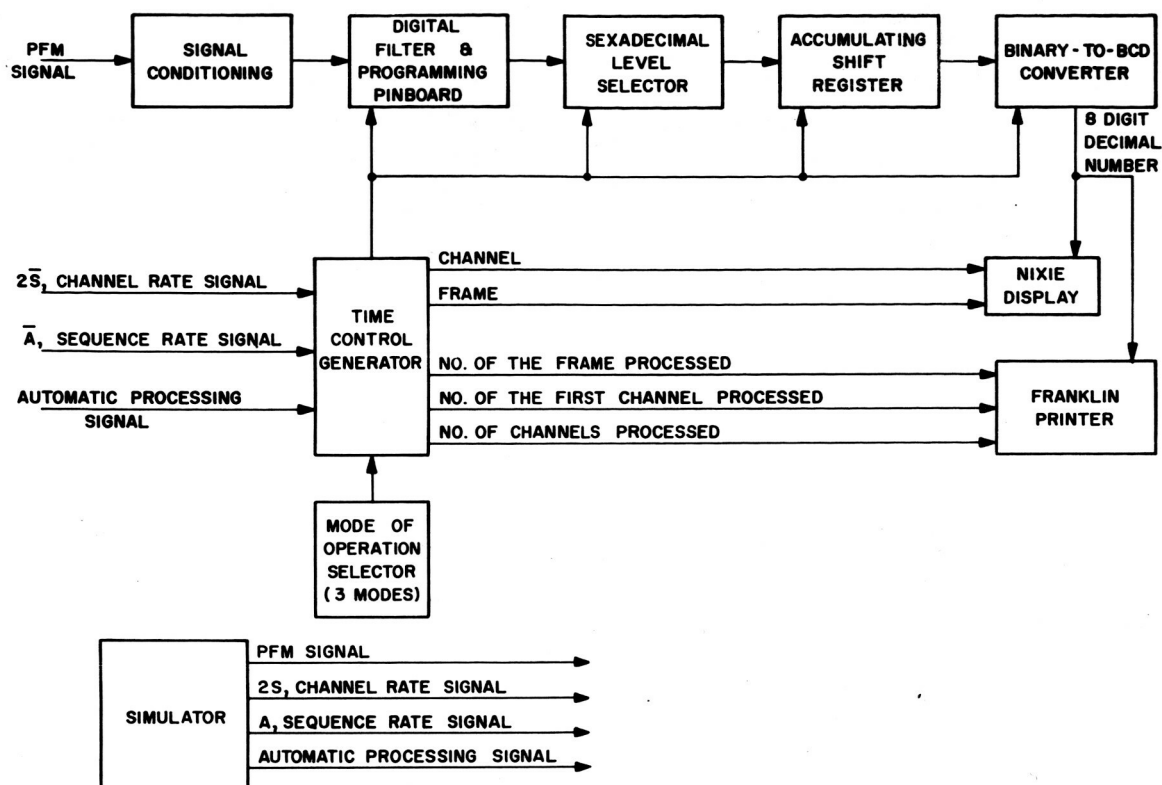
Figure II-D-1 — Data Digital Processor, Simplified Block Diagram.

The Digital Data Processor can be operated in three modes according to the Mode of Operation selector. In the Manual Mode, the first channel to start processing, the number of channels processed (1, 2, 3, 4, 5, or 6), and the frames selected are set by manual switches on the front panel. In the Automatic Mode, the channels to be processed are selected by the incoming automatic processing signal, whereby the number of channels processed is on a two channel basis. In the All Mode, every channel in the PFM sequence is processed on a two channel basis, where the first channels processed are the even numbered channels.

E.   UNIT LOCATION

Figure II-E-1 is a photograph of the Digital Data Processor showing unit location.

Unit A contains the Nixie Display of the channel, frame, and 8-digit decimal number, and associated time control generator logic.

Unit B contains the input BNC connections, signal conditioning, the simulator, binary-to-BCD converter, and associated time control generator logic.

Unit C contains the Franklin series 1000 Hi-Speed Printer.

Unit D contains the programming pinboard, digital filter, and sexadecimal level selector logic.

Unit E contains the power panel and power supply.
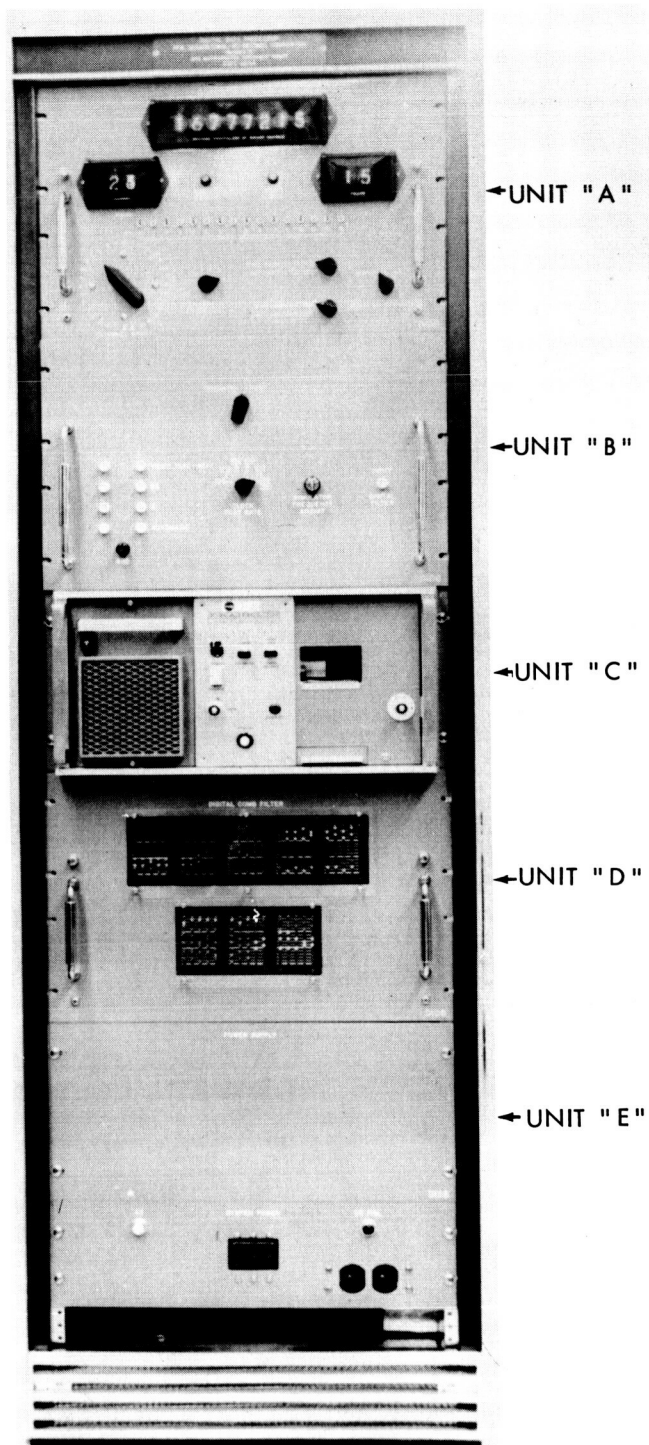
Figure II-E-1 — Digital Data Processor Showing
Unit Location.

SECTION III

DESCRIPTION OF SUBSYSTEMS

A. INTRODUCTION

The following paragraphs are functional descriptions of each subsystem of the Digital Data Processor. Each of the subsystems is described according to its implementation, and theory of operation where appropriate.

B. SIGNAL CONDITIONING

The Band Pass Filter card accepts the incoming PFM signal from the simulator or encoder. The first stage is a variable attenuator and an emitter follower used as a buffer for the input. The next two stages amplify the signal which is then presented to the Band Pass Filter through an emitter follower. The Band Pass Filter T configuration has been designed to pass the data band of 6.4 KC to 12.4 KC. The pass band of the filter is from 5.1 KC to 15 KC. The output of the filter is then passed through an emitter follower as the final output of the card.

The PFM Simulator is contained on the Oscillator, AGC, Amplifier card. The Colpitts oscillator circuit is variable over the data band of 6.4 KC to 12.4 KC. The oscillator output is then passed through an AGC circuit which will present a constant amplitude signal to a final amplifier and emitter follower output stage.

The Buffer card contains three identical emitter follower circuits used as interface circuitry to accept the sequence rate, the channel rate, and automatic processing signals, from the encoder and condition these signals for use by the DDP.

A block diagram of the signal conditioning circuits appears in Figure III-B-1.

C. DIGITAL FILTER

1. Theory of Operation

A digital filter can be defined as any linear computational scheme producing a discrete output from an input frequency if that frequency falls within the design criteria of the digital filter. The digital filter in this digital data processor is used as a frequency recognition device. The output response of the digital filter is that of an ideal filter; i.e., no attenuation inside the pass band, infinite attenuation outside the pass band, and with infinite slopes at the bandedge frequencies. If a frequency, f, falls within the range $f_1 < f < f_2$, the digital filter will give a recognition response, where f_1 and f_2 are the lower and upper bandedge frequencies, respectively. The bandedge frequencies will statistically vary due to the gate time allowed for measuring of the frequency, f. This variation is known as the quantization error.

The quantization error is defined as the error inherent in the measurement technique itself and exists whether or not noise is present on the input signal. The lower limit on the resolution obtainable is due to the quantization error. The quantization error in measuring a number of half periods of the frequency f can be evaluated by reference to Figure III-C-1.

The phase of the signal frequency f and the start of the gate time W are mutually independent. The quantization error is a combination of the time "a" that the gate time W started too soon and the time "b" that the gate time W ended too soon in relation to the phase of the input frequency f. Times "a" and "b" are limited by $0 < a < 1/2$ cycle and

BANDPASS FILTER CARD

```
PFM          INPUT        EMITTER      AMPLIFIER    EMITTER      BANDPASS     EMITTER
SIGNAL →   ATTENUATOR →  FOLLOWER  →             → FOLLOWER  →   FILTER    → FOLLOWER  →
```

PFM SIMULATOR CARD

```
  OSCILLATOR          AGC           AMPLIFIER  →
  (VARIABLE)   →            →
```

BUFFER CARD

```
SEQUENCE
RATE SIGNAL  →    BUFFER  A    →

CHANNEL
RATE SIGNAL  →    BUFFER  B    →

AUTOMATIC
PROCESSING   →    BUFFER  C    →
SIGNAL
```
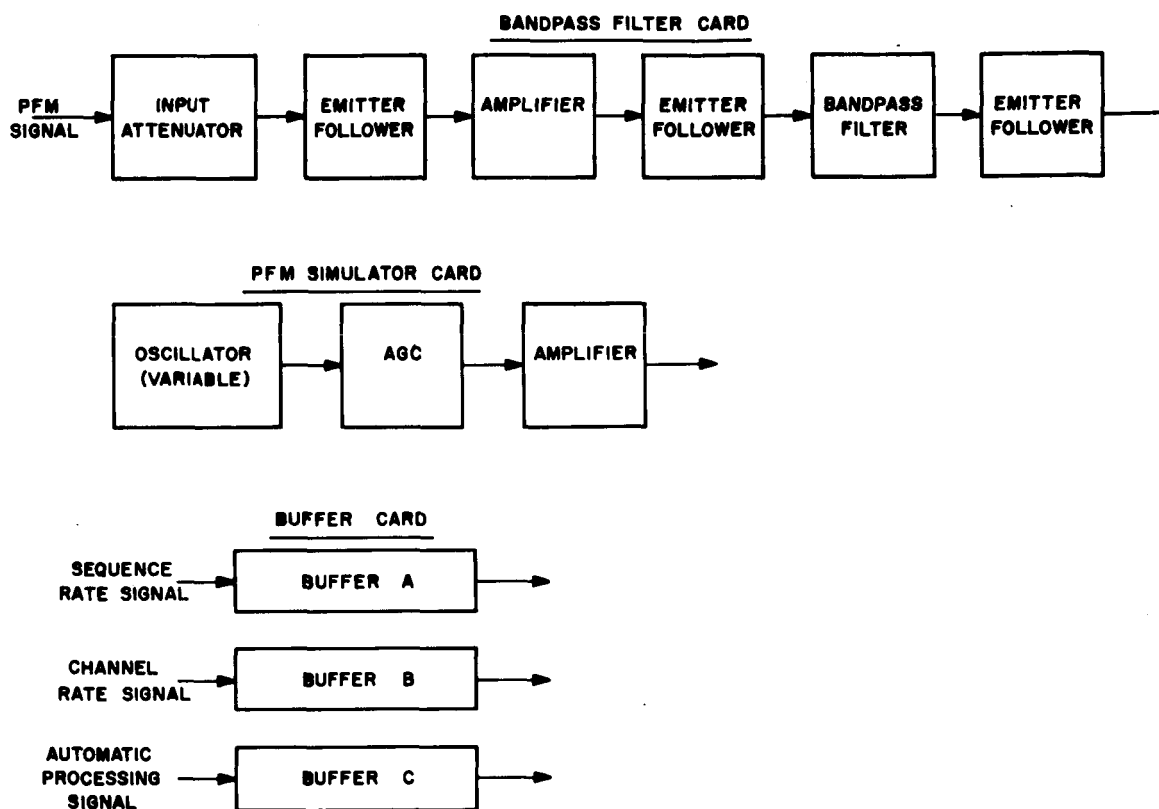
Figure III-B-1 — Signal Conditioners.
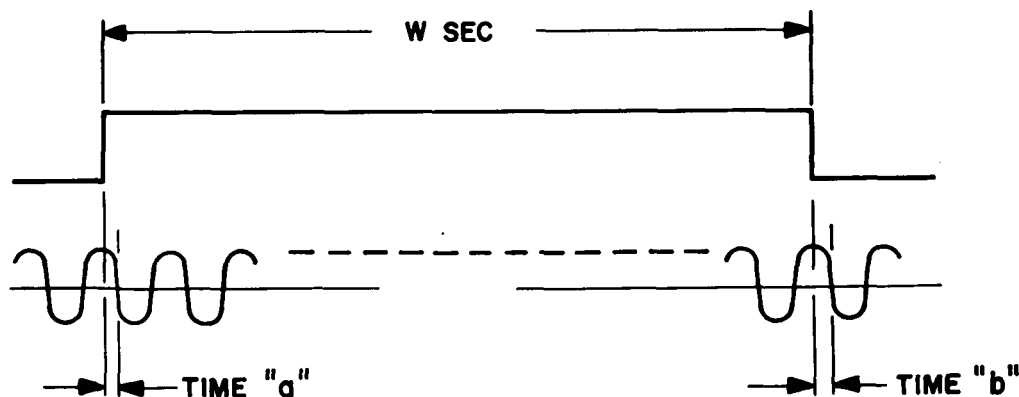
Figure III-C-1 — Phase Relationship of the Gate Time W, and the Frequency Being Measured.

$0 < b < 1/2$ cycle of the frequency f. Therefore, the total elapsed time measurement is in error by the time "$|a - b|$". Since the frequency f is independent of the gate time W, the time "a" and the time "b" each have a rectangular density distribution as shown in Figure III-C-2. The time "$|a - b|$" has the probability density distribution as shown in Figure III-C-2. The maximum error occurs when time "a" = 0 cycle and time "b" = 1/2 cycle or when time "a" = 1/2 cycle and time "b" = 0 cycle. Thus the maximum quantization error is 1/2 cycle of the frequency measured.

III-2
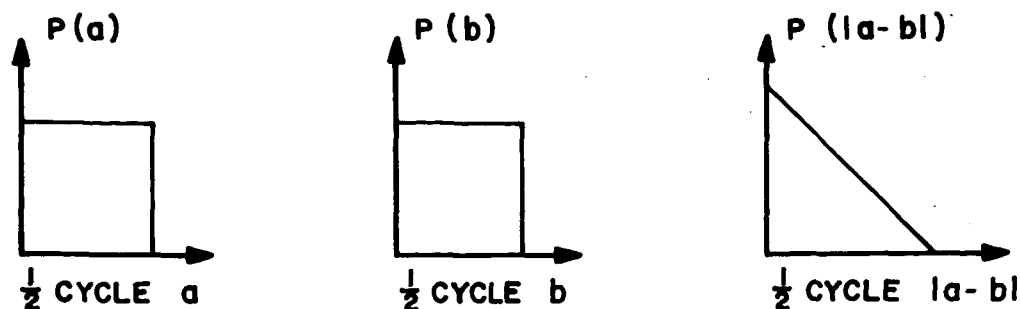
Figure III-C-2 — Probability Densities of a, b, and (a-b).

The digital filter that is used in this digital data processor is known as a digital comb filter. It must be able to distinguish between the sixteen discrete frequencies and indicate which of them occurred in a particular channel of the PFM sequence. The sixteen discrete frequencies used on the encoder in IMP's D, E, F, and G range from 6.4 KC to 12.4 KC in 400 cycle increments. The method of frequency recognition is to count the number of half periods of the input frequency within a given gate time. This gate time must be less than the time for one channel. Due to the encoding techniques in synthesizing the PFM signal, the frequency contained in a channel is not guaranteed stable until 600 microseconds after the beginning of the channel. This is due to the switching of the frequency at the beginning of each channel. Therefore, the gate time must begin at least 600 microseconds after the beginning of the channel. The minimum time for a channel is 10 milliseconds. It can be shown that the number of stages in the counter (n) is related to the highest frequency (f) that can be recognized and the gate time available (W) by the equation:

$$n = 1.443 \ln \left[(2f + 1) W \right]$$

To be able to recognize frequencies up to 14 K cps, using a gate time of 9 milliseconds, an 8 stage counter would be required.

$$n = 1.443 \ln \left[2(14,000) + 1 \right] \left[.009 \right]$$

$$n = 7.98$$

n must be in increments of 1; therefore, n = 8. The smallest difference in frequency that can be recognized is given by

$$\Delta f = \frac{1}{2W}$$

For a given gate time of 9 MS, the smallest difference in frequency that can be recognized is .0556 KC.

2. Implementation

The Digital Filter is implemented by use of a zero crossover detector, gate time generator, digital filter counter, programming pinboard and gating matrix, digital filter output holding register, and word error detector. The block diagram of the digital filter is represented in Figure III-C-3.
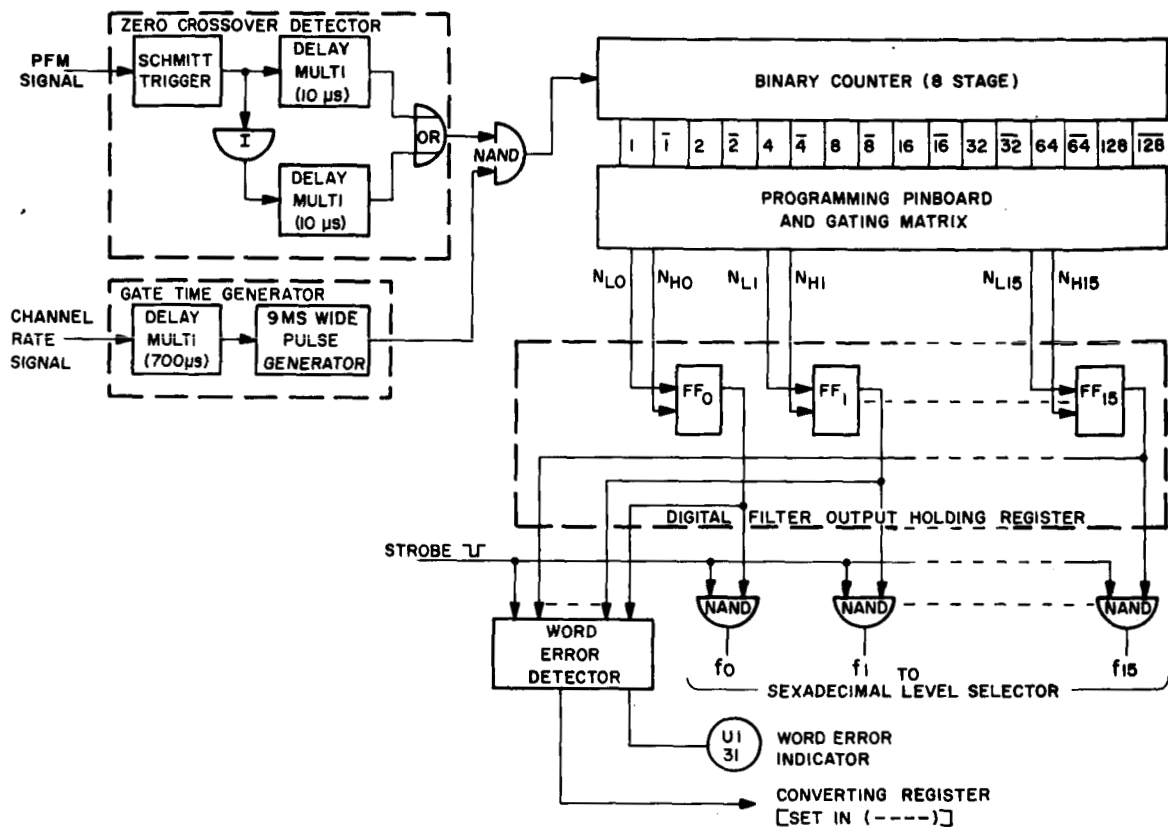
Figure III-C-3 — Digital Comb Filter.

In the zero crossover detector, the positive-going and negative-going transitions of the PFM wave are detected by a Schmitt Trigger which produces a square wave of which its transitions are representative of the zero crossings of the PFM wave.

The gate time generator is activated at the start of each channel. After a 700 us delay the 9 MS wide pulse is produced. The 9 MS wide pulse is gated with the output of the zero crossover detector.

The input to the digital filter counter is a series of pulses corresponding to the zero crossovers of the PFM wave during a gate time of 9 MS.

At the end of the gate time, if the number in the counter falls within a preselected range, that frequency is said to be recognized. Thus, the range is indicative of the bandwidth of the filter for that particular frequency. If the number in the counter is greater than N_1, the number corresponding to the lower bandedge frequency f_1, but less than N_h, the number corresponding to the upper bandedge frequency f_h, then that frequency is said to be recognized. When the count reaches N_1, a flip-flop is set and when the count reaches N_h, the flip-flop is reset. At the end of the gate time, the output of the flip-flop is strobed to see if the flip-flop has been set. If it has, the nominal frequency falling within the bandwidth $f_h - f_1$ is said to be recognized. The digital comb filter for this particular digital data processor consists of sixteen of these digital filters using the same zero crossover detector and counter. Due to the fact that the sixteen frequencies used in the satellite's encoding system may vary, as this digital processor is to be used in assisting in the checkout of various satellite encoders, a programming pinboard and gating matrix has been introduced between the binary counter and the digital filter output holding register. By merely rearranging the shorting pins on the programming pinboard, numbers

III-4

representing the different frequencies of the PFM signal (up to 14 KC), can be gated into the designator flip-flops.

If none of the sixteen flip-flops in the digital filter output holding register remained set at the end of the gate time, none of the filters recognized the incoming frequency. In this case, the word error detector is activated indicating that the input frequency was outside of the bandwidths of the digital comb filter. The output of the word error detector provides a response to the word error indicator and to the converting register to indicate that dashes (----) are to be printed by the Franklin Printer.

D. SEXADECIMAL LEVEL SELECTOR

1. Theory of Operation

The sexadecimal level selector will assign a preselected sexadecimal number (1 to 16) to each of the sixteen possible frequencies that can occur in a channel in the PFM sequence. The sexadecimal level, the frequency that is represented by that level, and its input bit configuration are indicated in Table 2 for IMP's D, E, F, and G. Note that there are two possible sexadecimal levels that can be selected.

The sexadecimal level selector is actually a decimal-to-binary converter. It converts a decimal number, each digit represented on a separate line, to a binary number. For converting the sexadecimal number (0 through 15), four output lines are required.

2. Implementation

The sexadecimal level selector can easily be implemented by a decimal-to-binary converter. Since the number of binary bits required is relatively small, (four binary bits) a direct conversion is simple and is the fastest way of conversion. A block diagram representation of the sexadecimal level selector is given in Figure III-D-1. The inputs to the sexadecimal level selector are sixteen lines, each representing one of the sixteen possible frequencies. A pulse will occur on one and only one of the lines, depending upon the frequency recognized by the digital filter. This pulse will set in to the four flip-flops its assigned sexadecimal level. The sexadecimal level selector is wired for the case where the lower frequency (6.4 K cps) corresponds to the input bit configuration 0000. If the opposite bit configuration is required (1111), the sexadecimal level selector switch at the output to the four flip-flops can be used.

E. ACCUMULATING/SHIFT REGISTER

1. Introduction

A register can be defined as a device which is capable of storing information. In this processor, the register is used both as an accumulating register and as a shift register. As an accumulating register, it will accumulate or store the information from the output of the sexadecimal level selector; a four bit binary number representing one of the sixteen possible frequencies. As a shift register, its contents will be read into the Binary-to-BCD Converter serially by shift commands.

2. Implementation

The accumulating register can be implemented by having a series of twenty-four flip-flops arranged as a twenty-four bit shift register with the capability of transferring information into the shift register in a parallel fashion. A block diagram of the accumulating/shift is given in Figure III-E-1.
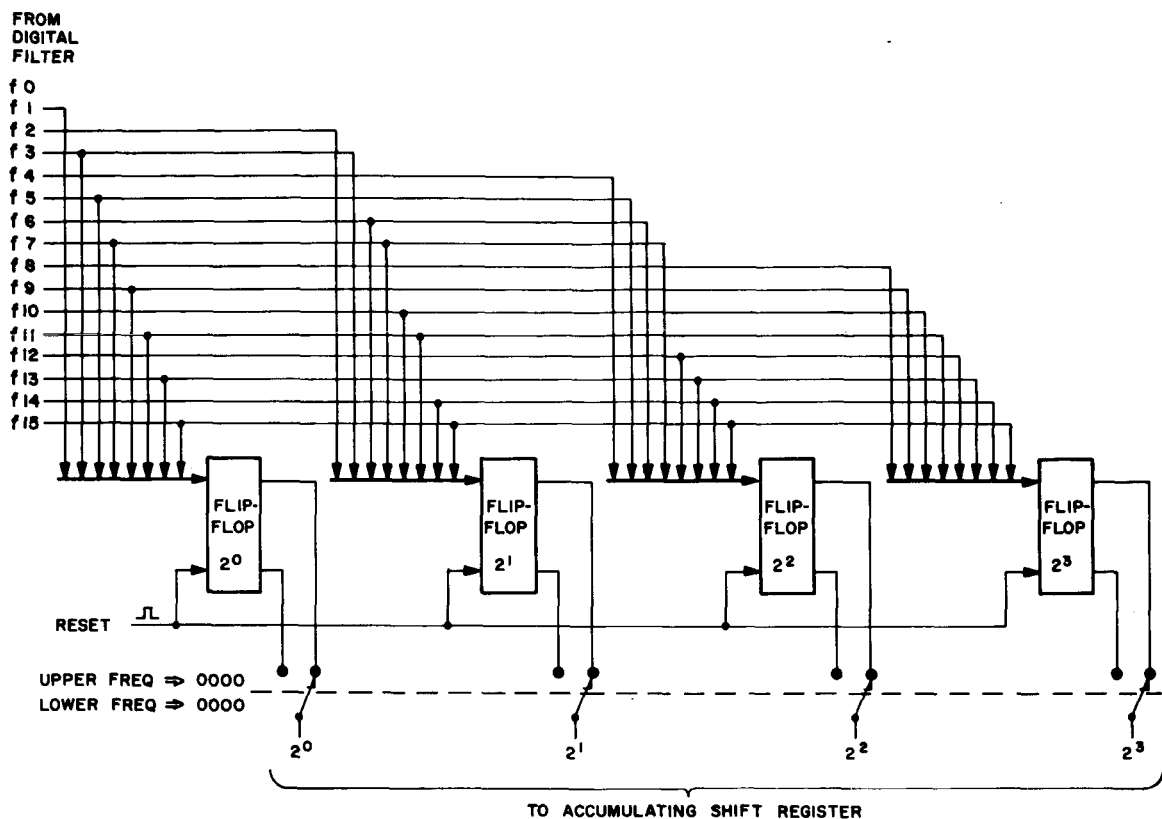
Figure III-D-1 — Sexadecimal Level Selector.
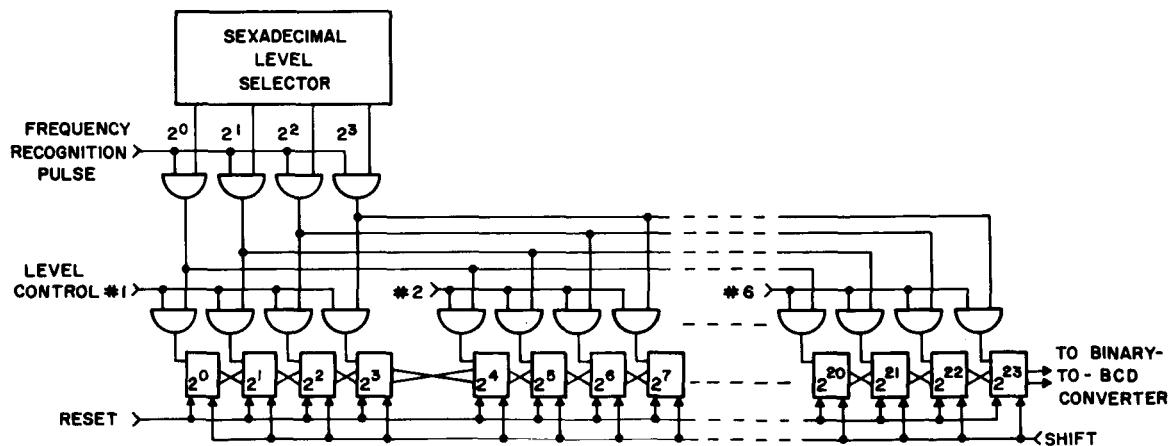
Figure III-E-1 — Accumulating/Shift Register.

After the frequency of a particular channel (e.g., Channel 4) has been recognized by the digital filter and had its four bit binary number assigned to it by the sexadecimal level selector, it is stored in the first four stages of the accumulating register. The next four bit binary number, representing the next channel (Channel 5) would be stored in the next four stages of the accumulating register, and so forth, until a total of six consecutive

four bit binary numbers representing six consecutive channels of the PFM sequence have been stored in the register. The first channel processed represents the least significant four bits of the twenty-four bit binary number. In some PFM formats, the most significant four bits occur in the first channel processed. In this case, the first four binary bits occurring in the first channel processed would be stored in the last four stages of the register. The next four binary bits occurring would be stored in the next to last four stages of the register and so forth. Least significant bits occurring first or most significant bits occurring first is predetermined and is set by a manual switch on the processor which controls the sequence of the six level control pulses.

After the twenty-four binary bits have been stored in the accumulating register, the conversion to a binary coded decimal number occurs. The Binary-to-BCD Converter requires the binary word that will be converted to be read into its converting register serially bit by bit. A clock pulse is applied each time a bit is read into the converting register. This causes all the bits in the register to be shifted one stage to the right. The bit that was in the last stage of accumulator is read into the converting register first.

At the beginning of the channel to be processed the accumulating/shift register is reset. The output of the sexadecimal level selector is strobed at the end of the gate time which transfers the four binary bits to their proper stages in the accumulating/shift register according to the level control pulses, which are derived from the time control generator. At the end of transferring six-four bit binary words consecutively into the register, the entire contents are shifted to the Binary-to-BCD Converter.

F. BINARY-TO-BCD CONVERTER

1. Theory of Conversion

The binary system of representing numbers does not lend itself to easy recognition by the human eye for interpretation. Analysis of the experiments is facilitated by transforming the binary information to the decimal system of representing numbers. Therefore, a binary-to-decimal conversion is required. In order to have a permanent record of this information that is continuously occurring at the input to the digital data processor, a printer will be used to record the decimal equivalent of the binary number along with its location in the PFM sequence. The printer being used requires the decimal input to be in the form of a BCD (Binary Coded Decimal) number. A BCD number requires four input lines per decimal digit versus ten lines per decimal digit for a decimal numbered input. Therefore, the binary-to-decimal conversion will actually be a binary-to-BCD conversion.

In general, any decimal number of any length can be expressed as a number in powers of 2 as follows:

$$(1) \quad N = A_n \times 2^n + A_{n-1} \times 2^{n-1} + \cdots + A_1 \times 2^1 + A_0 \times 2^0$$

where N is the decimal number, $n + 1$ is the number of bits, and A_n through A_0 are either 1 or 0. This can be rewritten by continuously factoring out powers of 2 as follows:

$$(2) \quad N = \left(\cdots (A_n)2 + A_{n-1} \right)2 + A_{n-2})2 + \cdots + A_1)2 + A_0$$

From equation (2), it can be seen that N can be represented as a series of multiplication by two (doubling) and adding the next most significant bit. This process is easily implemented in the binary number system because the doubling operation and adding the next most significant bit merely consists of a shift of all bits to one position toward the most

significant bit. However, the actual conversion process begins with a binary number and ends with a BCD number. Therefore, during the conversion process a correction is needed to convert to a BCD number after each shift.

The BCD number system will now be considered. Since n binary bits have 2^n states, the representation of 10 states of a decimal digit requires at least four binary bits ($2^4 > 10$). One of the most commonly used four bit codes is the 8-4-2-1 weighted code which is chosen from the first 10 binary numbers. As an example, the decimal number 527 represented in this manner is as follows:

	Hundreds of Units	Tens of Units	Units
Decimal Number	5	2	7
BCD Representation (Most Significant bit first)	0101	0010	0111

A Binary-to-BCD Converter that uses the principle of doubling and adding the most significant bit is known as the "Double-Dabble" or "Double-Dibble" Method of Conversion. Starting with the most significant bit, and by shifting one bit toward the most significant bit, one accomplishes the doubling if the next most significant bit is a zero and the "dibbling" (doubling and adding 1) if the next most significant bit is a one. After each shift, one must examine the number that has been converted thus far, to see if it needs an adjustment to the BCD representation. A property of a binary number is that it may be doubled by shifting one bit towards the most significant bit. BCD numbers may also be doubled by shifting one bit towards the most significant bit, but it must be adjusted because a radix of ten is imposed upon a BCD number. Doubling a BCD number which is less than five results in a BCD number which is less than 8, which is within the limitations of a BCD number. Doubling a BCD number which is 5 or greater will require an adjustment, resulting in two BCD numbers. After the doubling operation, if the number is 10 or greater, the adjustment is to add six to the number. This results in a two digit number; each represented as a BCD number; and each within the radix of ten. This can be illustrated by the following example:

Decimal	12:	
Binary	12:	1100
Add	6:	0110
Result in a BCD Representation	0001 / 1	0010 / 2

This additional six counts results whenever the BCD number shifts into the next decimal position; i.e., from units to tens of units, tens of units to hundreds of units, etc. An example of using the double-dibble method of conversion to convert the binary number 26 to a BCD number is as follows:
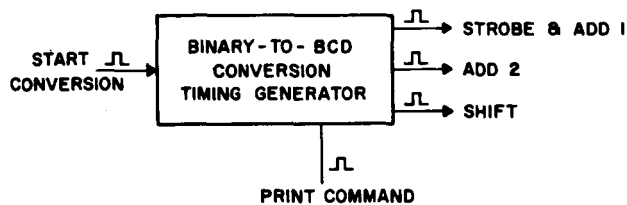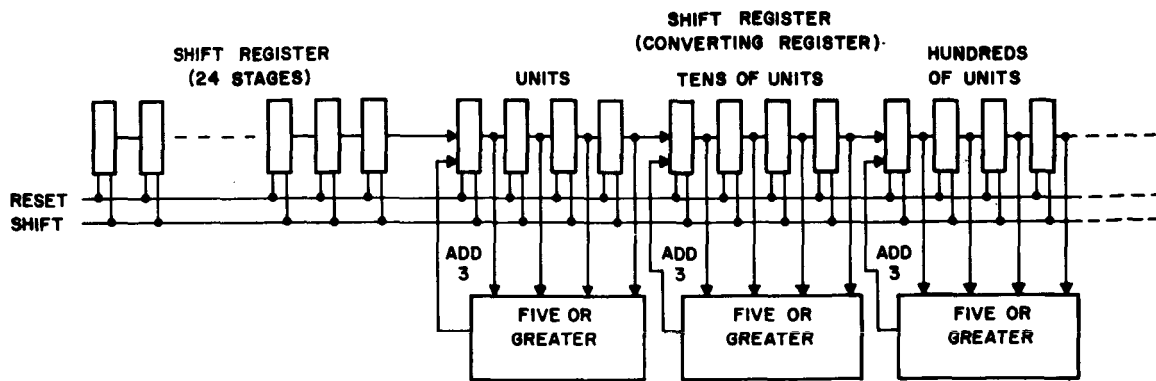
| Shift Register | | | | | Converting Register | | | | | | | |
| Binary Numbers | | | | | Units | | | | Tens of units | | | |
2^0	2^1	2^2	2^3	2^4	2^0	2^1	2^2	2^3	2^0	2^1	2^2	2^3
0	1	0	1	1	0	0	0	0	0	0	0	0
1—Shift 0	0	1	0	1	1	0	0	0	0	0	0	0
2—Shift 0	0	0	1	0	1	1	0	0	0	0	0	0
3—Shift 0	0	0	0	1	0	1	1	0	0	0	0	0
4—Shift & add six 0	0	0	0	0	1	0	1	1	0	0	0	0
					0	1	1	0				
0	0	0	0	0	1	1	0	0	1	0	0	0
5—Shift 0	0	0	0	0	0	1	1	0	0	1	0	0
					6				2			

Since there are five binary bits, five shifts are necessary, making the adjustment in the converting register after each shift, if necessary.

Note that adding six to the doubled number requires a carry generation between the decades in the converting register. Another method to implement the adjustment of adding six after the shift if the number is 10 or greater, is to add three before the shift operation if the number is five or greater. Adding three and then shifting is equivalent to adding six after shifting, but the need for a carry is eliminated by adding three before shifting.

2. Implementation

A block diagram representation of the Binary-to-BCD Converter is given in Figure III-F-1.

The number of decades (UNITS, TENS OF UNITS, etc.) required is dependent upon the length of the binary number to be converted to a BCD representation.

For a 24 bit binary number, the maximum decimal number that can occur is 16,777,215 which requires 8 decades.

The outputs of each decade of the conversion register are connected to driving gates required for the Nixie Display and for the Printer.

The five or greater detector can be implemented by considering the following equation.

five or greater = 5 + 6 + 7 + 8 + 9 + 10 + 11 + 12 + 13 + 14 + 15

redundant terms

Figure III-F-1 — Binary-to-BCD Converter.

The above equation using the BCD notation with the 1248 weighted code can be written as:

$$\text{five or greater} \ = \ 1\bar{2}\bar{4}8 + \bar{1}24\bar{8} + 124\bar{8} + \bar{1}\bar{2}48 + 1\bar{2}\bar{4}8 + \bar{1}2\bar{4}8$$

$$+ \ 12\bar{4}8 + \bar{1}\bar{2}48 + 1\bar{2}48 + \bar{1}248 + 1248$$

This can be simplified to read: $(\bar{1} + \bar{2}) \cdot 4 + 8$

The timing steps required for the conversion are as follows:

    a. Add three to each decade that contains a number five or greater.

    b. Shift all bits to the right (towards most significant bit).

    c. Repeat steps 2 and 3 until the least significant bit has been shifted into the conversion register.

The Binary-to-BCD Conversion Timing Generator provides the pulses required to perform the conversion. Timing steps a) and b) are required for each binary bit to be converted. For each bit converted, three pulses are required:

    1) a pulse that strobes the decade to see if its number is five or greater and adds a count of one to the decade if its number is five or greater

    2) a pulse that adds a count of two to the decade if its number is five or greater

    3) a shift pulse

If the least significant bits occur first in the PFM format, a twenty-four bit conversion is performed for any number of channels processed. If the most significant bits occur first in the PFM format, the number of bit conversions required depends upon the number of channels processed and is tabulated as follows:

# of channels processed	# of bit conversions required
1	4
2	8
3	12
4	16
5	20
6	24

At the end of the conversion, a print command pulse is generated. If a word error occurred during any one of the channels processed, the 1-2-4-8 weighted code for printing dashes (----) is transferred to the conversion register before the print command pulse is generated

G. TIME CONTROL GENERATOR

1. Introduction

The preceding sections have described techniques whereby logical operations may be performed and information may be read into and out of various storage devices. In order to utilize the speeds of the techniques and devices which have been illustrated, it is necessary to sequence automatically the various operations which occur at speeds comparative with those of the rest of the digital data processor. This section will deal with the Time Control Generator.

The Time Control Generator or "control element" may be defined as "those parts of a digital computer which effect the carrying out of instructions in proper sequence, the interpretation of each instruction, and the application of the proper commands to the arithmetic element and other circuits in accordance with this interpretation."*

2. Implementation

Synchronization is obtained by the use of two signals, the channel rate signal and the sequence rate signal. The channel rate signal is counted by the channel counter (a five stage binary counter). Thus, the channel counter cycles through the counts 0 through 31. The output of the last stage of the channel counter is the frame rate (32 channels in a frame) which is counted in the frame counter (a four stage binary counter). Thus, the frame counter cycles from 0 through 15. In order to have the channel counter and the frame counter begin at the 0 channel and the 0 frame, both counters are reset by the sequence rate signal. Another set of counters for the channel counter and the frame counter are required, but operating as BCD counters. The output of these counters are transferred to the Nixie Drivers and to the Output driving registers for driving the Franklin Printer. The counters operating in the BCD mode are necessary since the Nixie Drivers and the Franklin Printer require a BCD representation as its input.

One of the requirements of this processor is to be able to process a specified number of consecutive channels (from 1 to 6 channels) in a specified frame or frames. The first

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IRE Standards on Electronic Computers: Definition of Terms (New York: Institute of Radio Engineers, 1956).

channel to be processed is set by a manual switch. The number set by the switch is compared with the number occurring in the channel counter and when the two numbers agree an output from the comparison circuit will occur, indicating that this channel is the first one of a possible six consecutive channels to be processed. The comparison circuits will compare the two binary numbers bit by bit in parallel.

A parallel comparison of two binary numbers can be accomplished by the use of "exclusive OR" gates. Let A_0 and B_0 be two binary bits to be compared, and C the output of the exclusive OR circuit. Then,

$$C = \overline{A}_0 \cdot B_0 + A_0 \cdot \overline{B}_0$$

C is true if the A_0 bit and the B_0 bit are unequal.

For the parallel comparison of the channel start comparator, five bits will be compared. For this case:

$$C = A_0 \cdot \overline{B}_1 + \overline{A}_0 \cdot B_0 + A_1 \cdot \overline{B}_1 + \overline{A}_1 \cdot B_1 + A_2 \cdot \overline{B}_2 + \overline{A}_2 \cdot B_2$$
$$+ A_3 \cdot \overline{B}_3 + \overline{A}_3 \cdot B_3 + A_4 \cdot \overline{B}_4 + \overline{A}_4 \cdot B_4$$

The frames selected can be any combination of any of the sixteen frames. Therefore, let all sixteen frames be individually gated out of the frame counter. The output of each frame gate represents a particular frame and a frame can be selected by enabling the particular frame gate.

As each channel is decoded (i.e., its frequency recognized, and its sexadecimal level selected) the four bits of information that the channel conveys are stored in the accumulating/ shift register. Each four bits of each channel processed is stored in succeeding stages of the accumulating/shift register as described in Section III-E.

The number of channels processed (1, 2, 3, 4, 5, or 6) is selected by a manual switch and the number selected is the number of level control pulses required. Each level control pulse allows four bits to be transferred to the appropriate stages of the accumulating/shift register. The channel start pulse sets a flip-flop that enables the channel rate signal to be counted by the channels processed counter. The maximum number to be counted is six; therefore, a three stage binary counter is necessary ($2^3 > 6$). The number in this counter is compared in parallel to the number selected by the channels processed switch. The method of comparison is the same as that of the channel comparison, which was previously discussed, except that three binary bits are compared, instead of five binary bits. When the comparison is favorable, the channels processed counter is disabled from counting the channel rate signal.

A switch error can occur if the number of channels to be processed is greater than the number (32-channel start). If this condition occurs by an illegal setting of the channel start and number of channels processed switches, the switch error indicator will be on and the Franklin Printer will be inhibited.

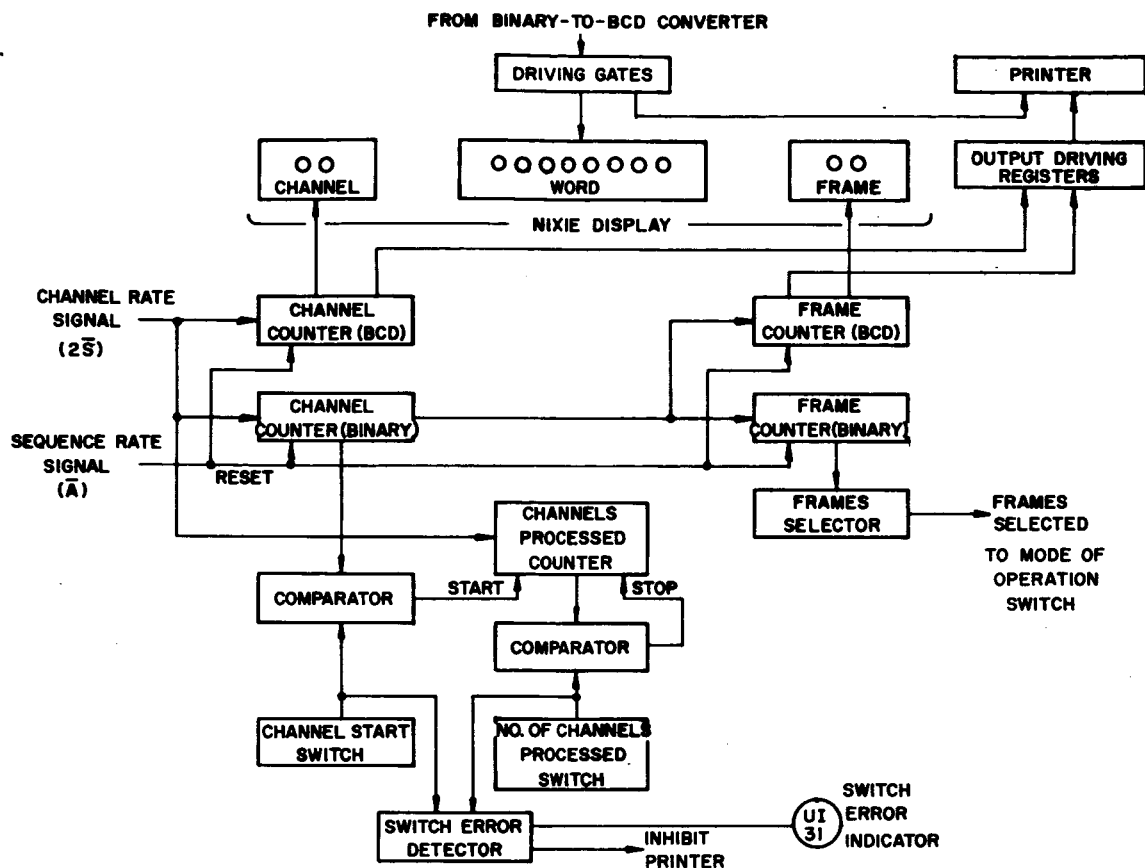A block diagram of the Time Control Generator is indicated in Figure III-G-1.

Figure III-G-1 — Time Control Generator.

H. MODE OF OPERATION SELECTOR

1. Introduction

The particular channels of the PFM signal that are to be processed are determined by three modes of operation as follows:

1) Manual Mode is when the channels to be processed are selected by front panel switches.

2) Automatic Mode is when the channels to be processed are selected by a signal from the encoding system.

3) All Mode is when all channels in the PFM sequence are processed.

2. Implementation

The Mode of Operation Selector is implemented by having three processing timing generators; an automatic processing timing generator, an all channels processed timing generator, and a manual processing timing generator. The Mode of Operation Switch selects one of the three processing timing generators. A block diagram of the Mode of Operation Selector is indicated in Figure III-H-1.

If the Manual Mode is selected, a channel start pulse will enable the counter in the manual processing timing generator to count channel rate pulses, and the channel stop pulse will disable the counter. A level control pulse will be gated out of the counter for
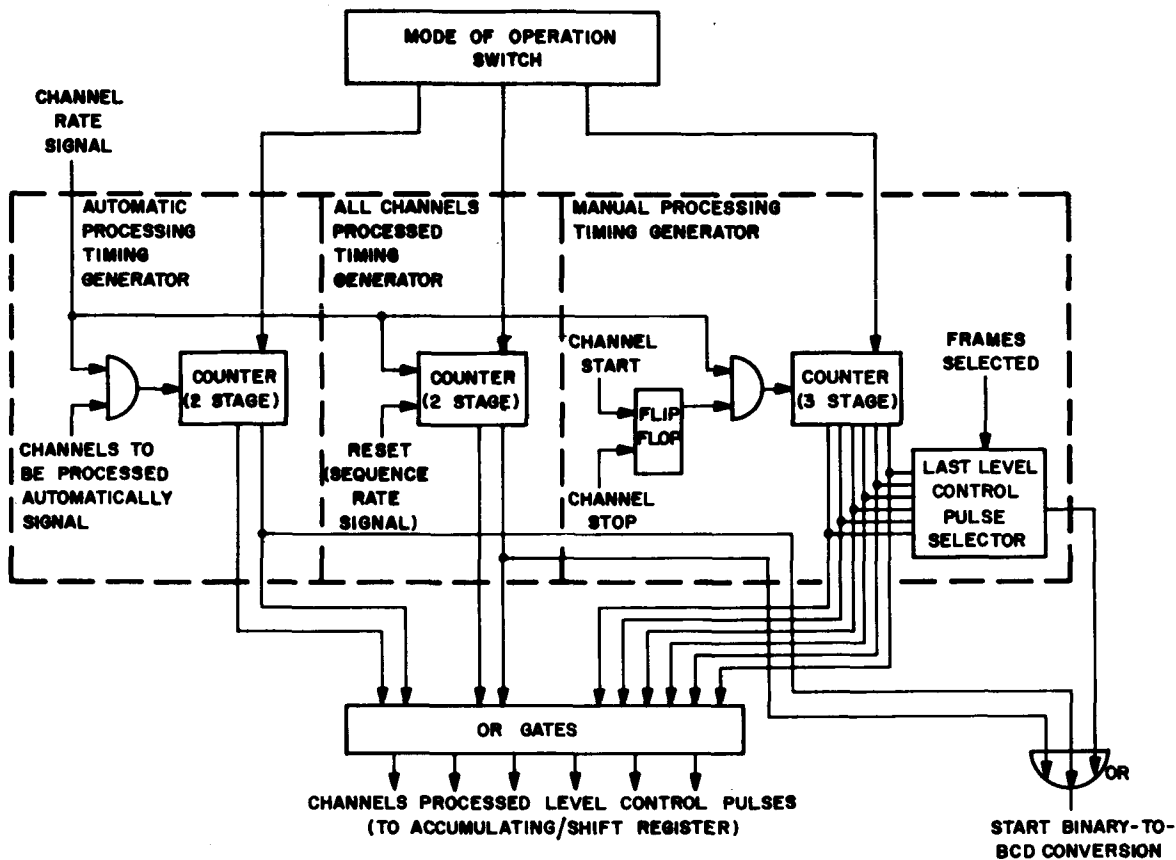
Figure III-H-1 — Mode of Operation Selector.

each channel rate pulse counted. The number of consecutive level control pulses produced is equal to the number of channels processed. Each level control pulse goes to the accumulating/shift register where it is gated with the four binary bits representing a channel tone in order to transfer the four binary bits to the correct stages of the accumulating/shift register. The trailing edge of the last level control pulse produced will start the Binary-to-BCD Conversion.

If the All Channels Processed Mode is selected, two level control pulses will be produced and the trailing edge of the second level control pulse will start the Binary-to-BCD Conversion. The counter is reset by the sequence rate signal in order to have the first channel processed to be all the even numbered channels in all frames.

If the Automatic Processing Mode is selected, the automatic processing signal from the encoder will select which channels to be processed by enabling the counter to count the channel rate signal. The number of channels processed will be in groups of two consecutive channels. The trailing edge of the second level control pulse will start the Binary-to-BCD Conversion.

I. SIMULATOR

    1. Introduction

        The simulator is a built-in feature of this digital data processor to be used for testing and checkout purposes. It will produce the channel rate signal, the sequence rate

signal, a specific automatic processing signal, and a PFM signal of constant frequency for all channels.

2. Implementation

A block diagram of the simulator is indicated in Figure III-I-1. The PFM signal is produced by simulating the burst-burst signal with a continuous wave, single frequency produced by the OSC AGC AMP card. This frequency is variable over the range of the data band by means of a front panel potentiometer control.

The synchronizing signals are produced by first generating a 100 cps signal with a multivibrator. This 100 cps signal is used as the channel rate $(2\bar{s})$ and is successively counted down to produce the sequence rate $(\bar{A})$. The Channel Rate Switch selects one of the following channel rates for test purposes; 100 cps, 100/2 cps, 100/4 cps, 100/8 cps, 100/16 cps or 100/32 cps.

Another signal, to be used in the automatic processing mode, is also derived from the count down of the channel rate. The proper output has been chosen to permit processing of certain predetermined channels.

J. DIGITAL DISPLAY

The digital display provides a visual presentation of the frame and channel occurring during the PFM sequence, and the decimal equivalent of the binary word representing the information in one, two, three, four, five, or six channels of the PFM sequence.

K. PRINTER

The printer used in this digital data processor is a Franklin Hi-Speed Series 1000 Printer. The output of the printer provides a permanent representation of the information processed by the digital data processor. For a complete description of the operation of the printer, the reader is referred to the Instruction Manual for the Hi-Speed Printer, Series 1000, Franklin Electronics, Inc. The format of the printer output is described in Section II-C.
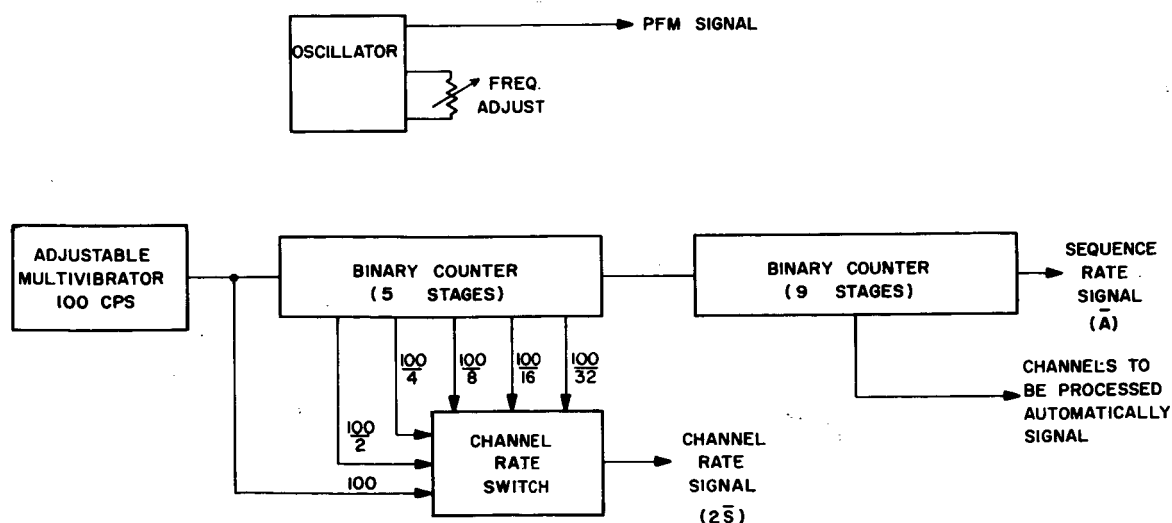

Figure III-I-1 — Simulator.

L. POWER PANEL

The power for the Digital Data Processor is supplied from one power supply. See Section I-B, for details and specifications pertaining to the power supply. AC and DC power status is visually represented on the power panel. The DC indicator lights when the DC power supply has failed. The AC indicator lights when AC power is applied to the Digital Data Processor.

SECTION IV

OPERATING CONTROLS, INDICATORS, AND PROGRAMMABLE PINBOARD

A. OPERATING CONTROLS AND INDICATORS

CONTROL	FUNCTION
Channel Start Switch	Determine Starting Channel
Channels Processed Switch	Determine number of channels to be processed
Mode of Operation Switch	Determine mode of operation
Frames Selected Switches	Determine frames to be processed
Upper, Lower Frequency $\Rightarrow$ 0000 Switch	Determine if upper or lower frequency $\Rightarrow$ 0000
Least, Most Significant First Switch	Select whether least or most significant bits are processed first
Operate-Test Switch	Choose to test or operate processor
Clock Test Rate Switch	Select clock rate for test
Simulator Frequency Adjust	Vary frequency of test PFM input
System Power Breaker	Control power to system
Push On Switch	Printer main power switch. Push in to turn "on" and/or "off."
Print Once-Paper Advance Switch	Allows printer to print once when elevated. Advances paper 5 inches per second when depressed.
Standby-Continuous Switch	In "standby" position, external print command signals will initiate a print cycle. In "continuous" position the printer prints continuously at its maximum print speed from internally generated print command signals.
Inhibit-Operate Switch	Normally in the "operate" position. When in the "inhibit" position the printer will not accept print command signals from any source.
Paper Release	Controls the idler wheel of the paper advance mechanism. When depressed the idler wheel rises from the driving wheel and paper can be pulled manually through the printer mechanism.

INDICATOR	FUNCTION
Decimal Equivalent of Binary Number Nixies	Indicates decimal equivalent of binary number of frequency detected in channels processed
Channel Nixies	Indicates channel occurring
Frame Nixies	Indicates frame occuring
Switch Error	Indicates error exists in setting of channel start and channels processed switches
Word Error	Indicates an undetected input frequency to the comb filter
Paper Out	Indicates printer is out of paper
Push On	Illuminated when printer power is on
AC Indicator	Illuminates when AC power is applied to DDP
DC Indicator	Illuminates when the DC power supply has failed
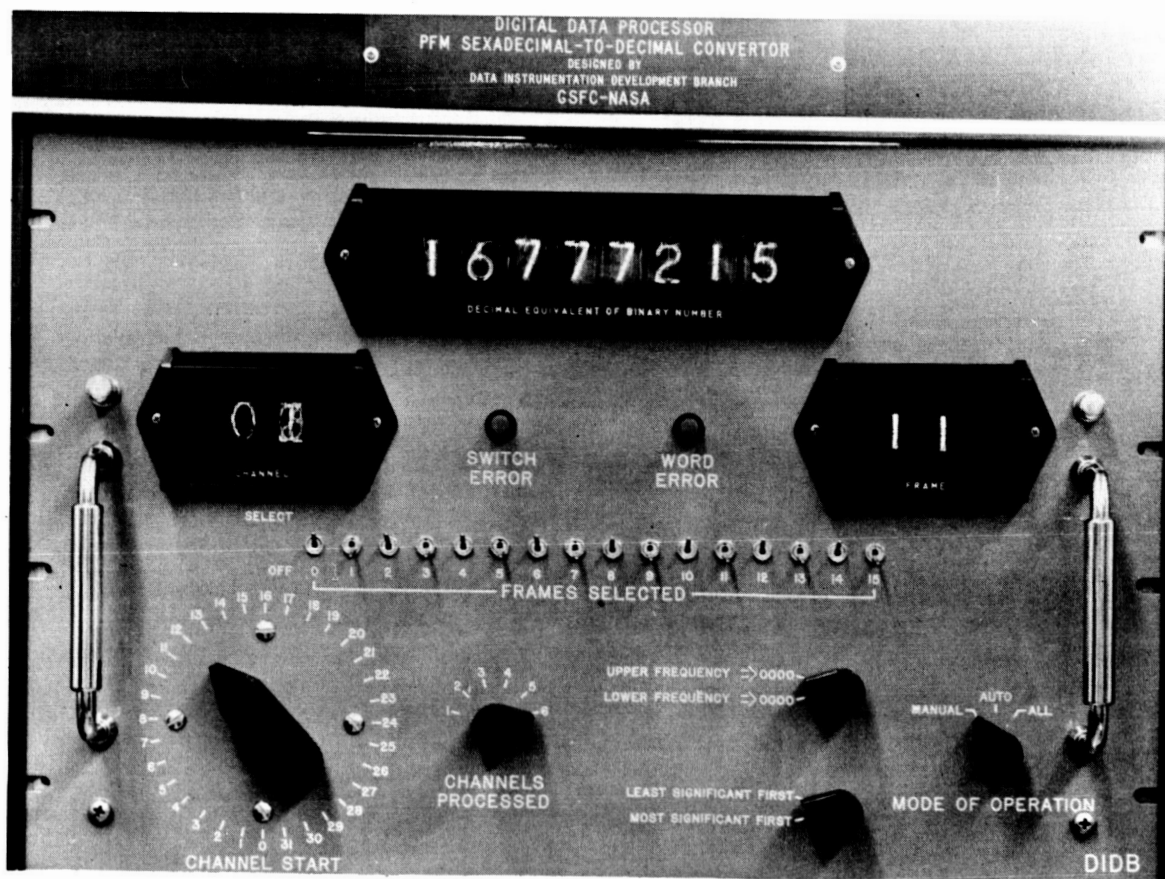
Figure IV-A-1 — Operating Controls and Indicators (Unit A).
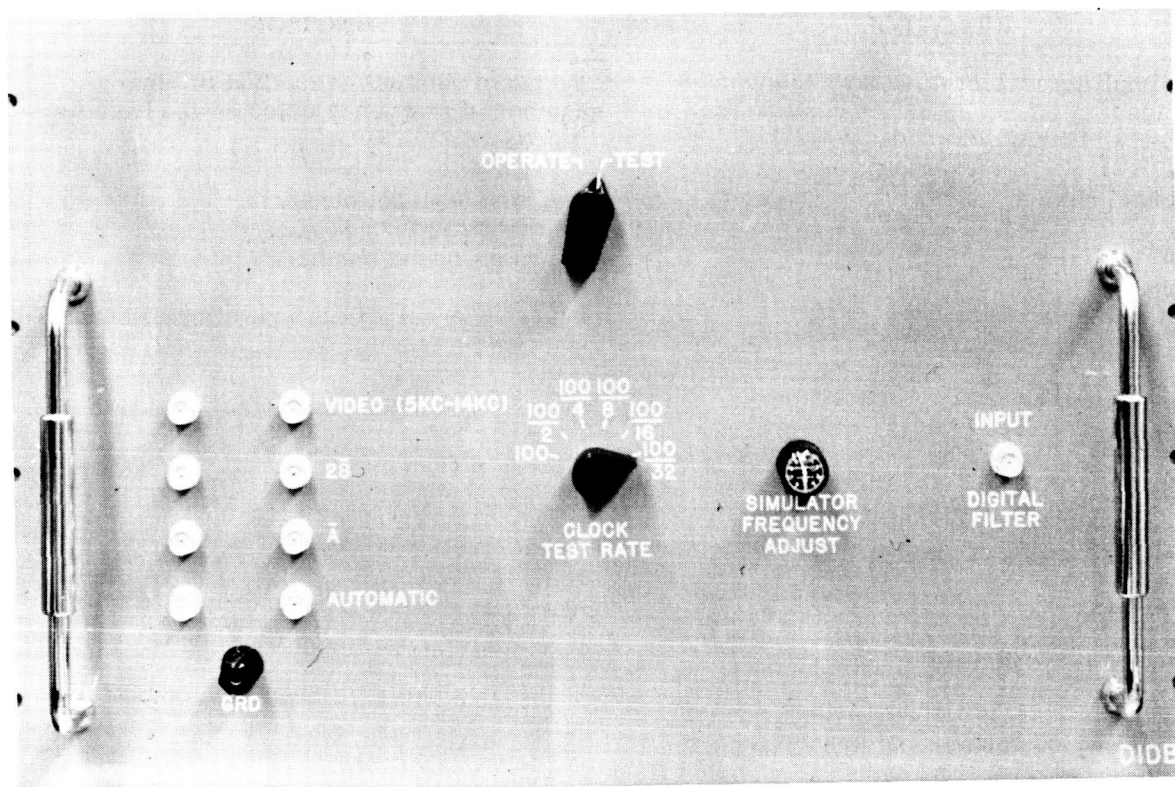
Figure IV-A-2 — Operating Controls and Indicators (Unit B).

B.   PROGRAMMABLE PINBOARD

By use of the programmable pinboard, the operator can select the upper and lower bandedge frequencies for each of 16 frequencies. Each frequency is selected by the proper location of 8 shorting pins on the pinboard. Figure IV-B-1 shows a photograph of the digital comb filter and Figure IV-B-2 shows a front panel view of the programmable pinboard indicating the locations for each of the frequencies. As an example, f_{0_L} represents the lower bandedge frequency for the 0th or lowest frequency to be recognized, and f_{0_H} represents the upper bandedge frequency for the 0th or lower frequency to be recognized. An eight bit binary number can be patched into the pinboard to represent a particular frequency by the use of 8 shorting pins. The number to be patched in (N, decimal) is related to the frequency by the equation: $N = 18f$, where f is the frequency in KC. From the decimal number, the equivalent binary number can be determined. The digital comb filter has a capability of representing frequencies up to 14.7 KC.
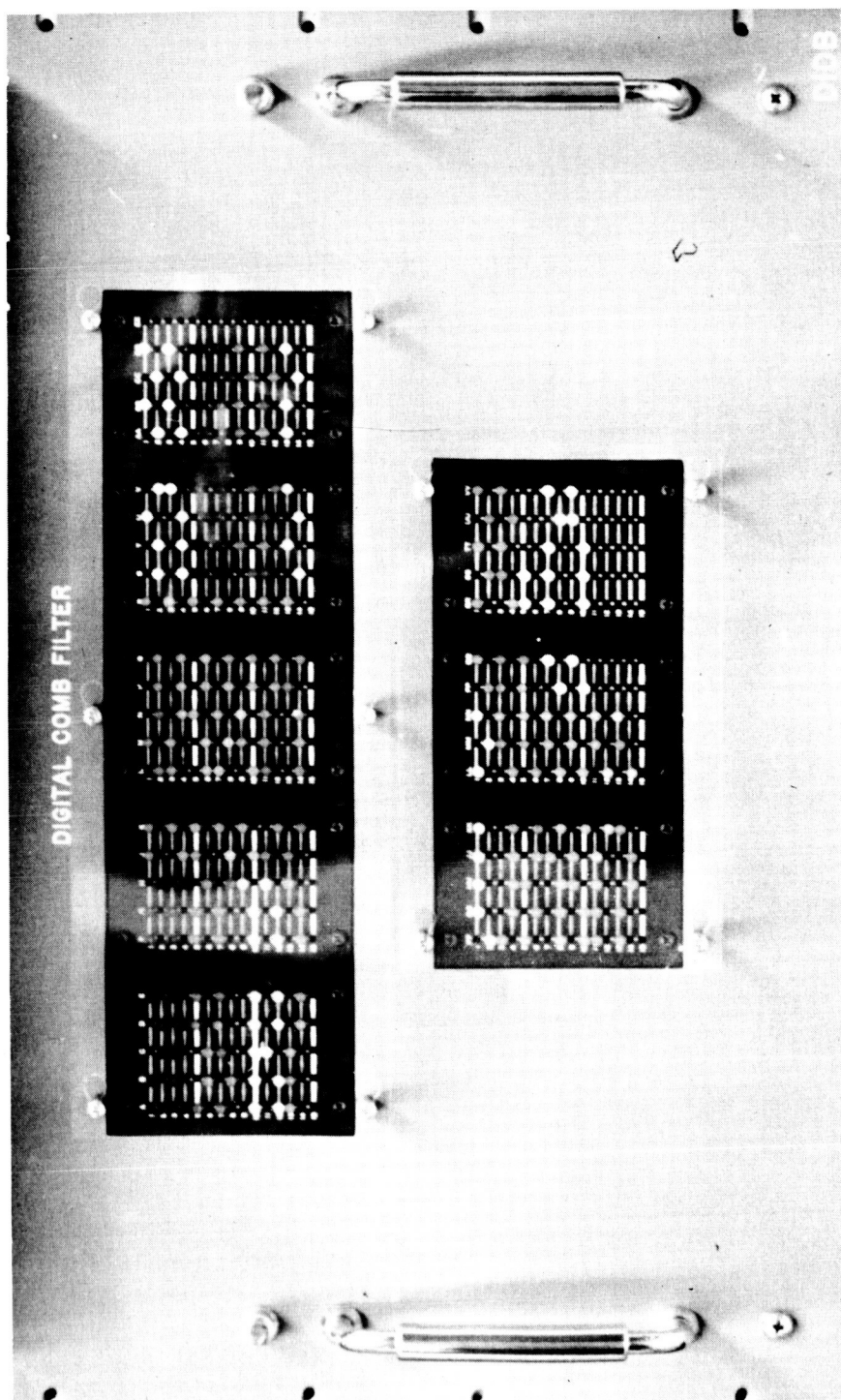
Figure IV-B-1 — Digital Comb Filter (Front Panel)

Figure IV-B-2 — Programmable Pinboard (Front View)

SECTION V

MAINTENANCE AND CHECKOUT

A. INTRODUCTION

The possibility of the occurrence of trouble in the equipment can be reduced greatly by following a periodic checkout and inspection procedure. The purpose of each inspection is to anticipate trouble and take the necessary steps to prevent it.

B. MAINTENANCE

Periodically make a complete visual inspection of the equipment as follows:

1. Mechanical

   (a) Check to see that all cable connections are firmly seated. Inspect each plug for looseness in receptacle, and for dirt and corrosion. Tighten all loose connectors.

   (b) Inspect indicator lamp assemblies for broken, cracked, or missing jewels; loose bulbs with loose bases; and loose, dirty, or corroded connections.

   (c) Inspect electrical terminals of switches for corrosion and dirt.

2. Cleaning

   (a) Remove all loose particles from the filters using low pressure air.

   (b) Clean all dust and dirt from chassis with a vacuum cleaner or with compressed air at a pressure of five pounds per square inch.

3. Electrical

   a. Power Supplies

      (1) Check the voltage of the primary ac power source. The ac power source should supply 115 volts ±10 volts.

      (2) Check the voltage of each power supply. The output voltage of each power supply should be as follows:

      Computer Control Corporation, Model RP-32

            -18 Vdc, 0 to 20 amp
            -6 Vdc, 0 to 20 amp
            +12 Vdc, 0 to 20 amp

      Con Avionics Corporation, Model R200-0.1-BX

            +200 Vdc, 0 to 0.1 amp

C. CHECKOUT

1. Simulator

The Digital Data Processor contains a simulator that can be used to partially check the operation of the system. To use the simulator, put the OPERATE-TEST SWITCH to TEST, and set the CHANNEL RATE SWITCH to the desired channel rate. The simulated PFM signal consists of a constant frequency in all of the channels of the PFM sequence. The desired frequency can be set by adjusting the SIMULATED FREQUENCY ADJUST potentiometer and monitoring the digital filter input BNC with an electronic counter. The mode of operation selector will determine which mode is in operation. For the automatic mode, channels 0,1,2,3,4,5,6,7,16,17,18,19,20,21,22,23, of all frames will be processed on a 2 channel basis with the even numbered channels as the first channel processed. In the all mode, all channels will be processed on a 2 channel basis with the even numbered channels as the first channel processed. In the manual mode, the channels and frames processed are determined by the manual setup of the CHANNEL START, NUMBER OF CHANNELS PROCESSED, AND FRAMES SELECTED SWITCHES.

Table 3 indicates the decimal equivalent of the binary number corresponding to the simulated frequency for 1, 2, 3, 4, 5, or 6 channels processed.

Table 3

Decimal Equivalent of the Binary Number Corresponding to the Simulated
Frequency for 1, 2, 3, 4, 5, or 6 Channels Processed

Frequency (KC)	Input Bit Configuration	Number of Channels Processed					
		1	2	3	4	5	6
6.4	0000	0	0	0	0	0	0
6.8	0001	1	17	273	4369	69905	1118481
7.2	0010	2	34	546	8738	139810	2236962
7.6	0011	3	51	819	13107	209715	3355443
8.0	0100	4	68	1092	17476	279620	4473924
8.4	0101	5	85	1365	21845	349525	5592405
8.8	0110	6	102	1638	26214	419430	6710886
9.2	0111	7	119	1911	30583	489335	7829376
9.6	1000	8	136	2184	34952	559240	8947848
10.0	1001	9	153	2457	39321	629145	10066329
10.4	1010	10	170	2730	43690	699050	11184810
10.8	1011	11	187	3003	48059	768955	12303291
11.2	1100	12	204	3276	52428	838860	13421772
11.6	1101	13	221	3549	56797	908765	14540253
12.0	1110	14	238	3822	61166	978670	15658734
12.4	1111	15	255	4095	65535	1048575	16777215

SECTION VI
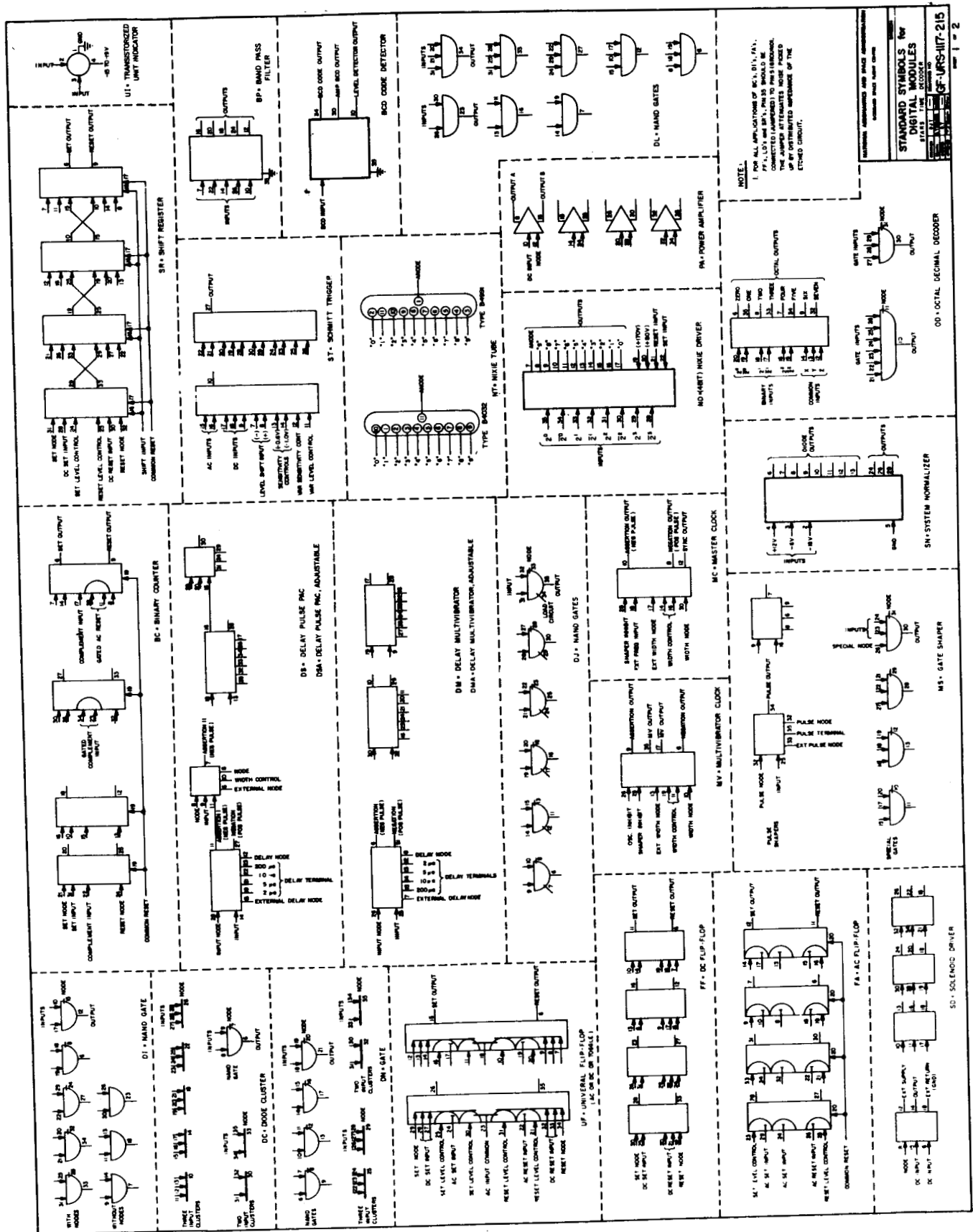
LOGIC AND CIRCUIT DIAGRAMS
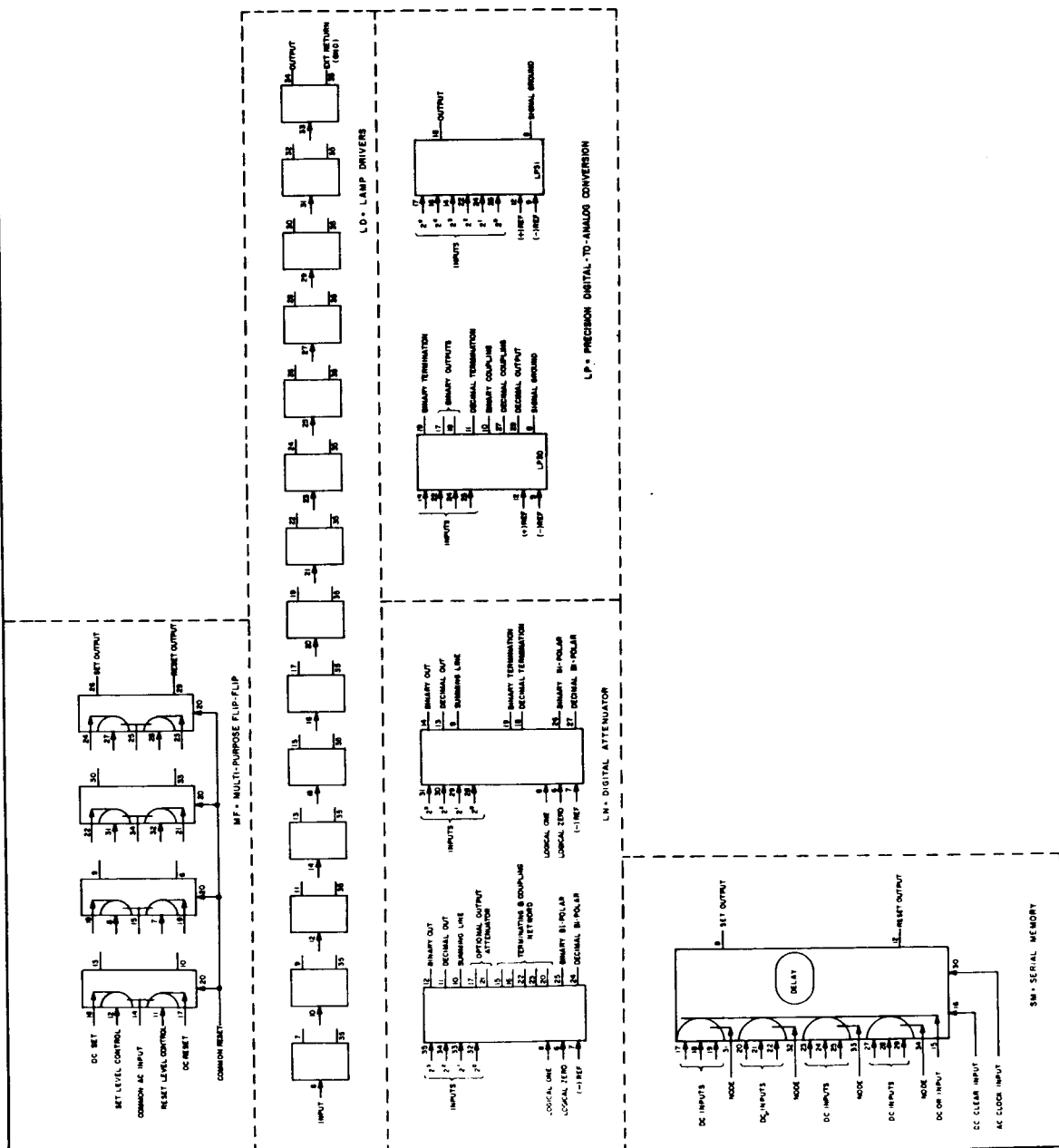
A. CONVENTIONS AND SYMBOLS

Except for the specially designed circuits, the Digital Data Processor employs Computer Control Company's S-PAC printed circuit, 200 KC and 1 Megacycle digital modules.

Reference 2 (the 3C Manual) should be used to decode logic symbols when working with the detailed logic diagrams of the subsystems. Each unit contains one to three standard S-blocs. S-bloc is the designation given to the SERIES S-PAC module mounting drawers. When reference is made to a circuit its location is designated by the S-bloc within the unit, the module position number, and the pin number of interest; e.g., III-4-8 refers to S-bloc III, board 4, pin 8. The logic levels required are: logical 1 = -6 V, logical 0 = 0 V. The following Figures VI-A-1 and VI-A-2 may be used as an overall guide for logic diagrams which appear in this manual.

B. LOGIC AND CIRCUIT DRAWINGS

In this section, each of the block diagrams discussed in Section III on the description of subsystems are shown indicating the logical circuit representation with connector numbers. The 3 special printed circuit cards for the signal conditioning circuits, input amplifier and simulator are included in this section.
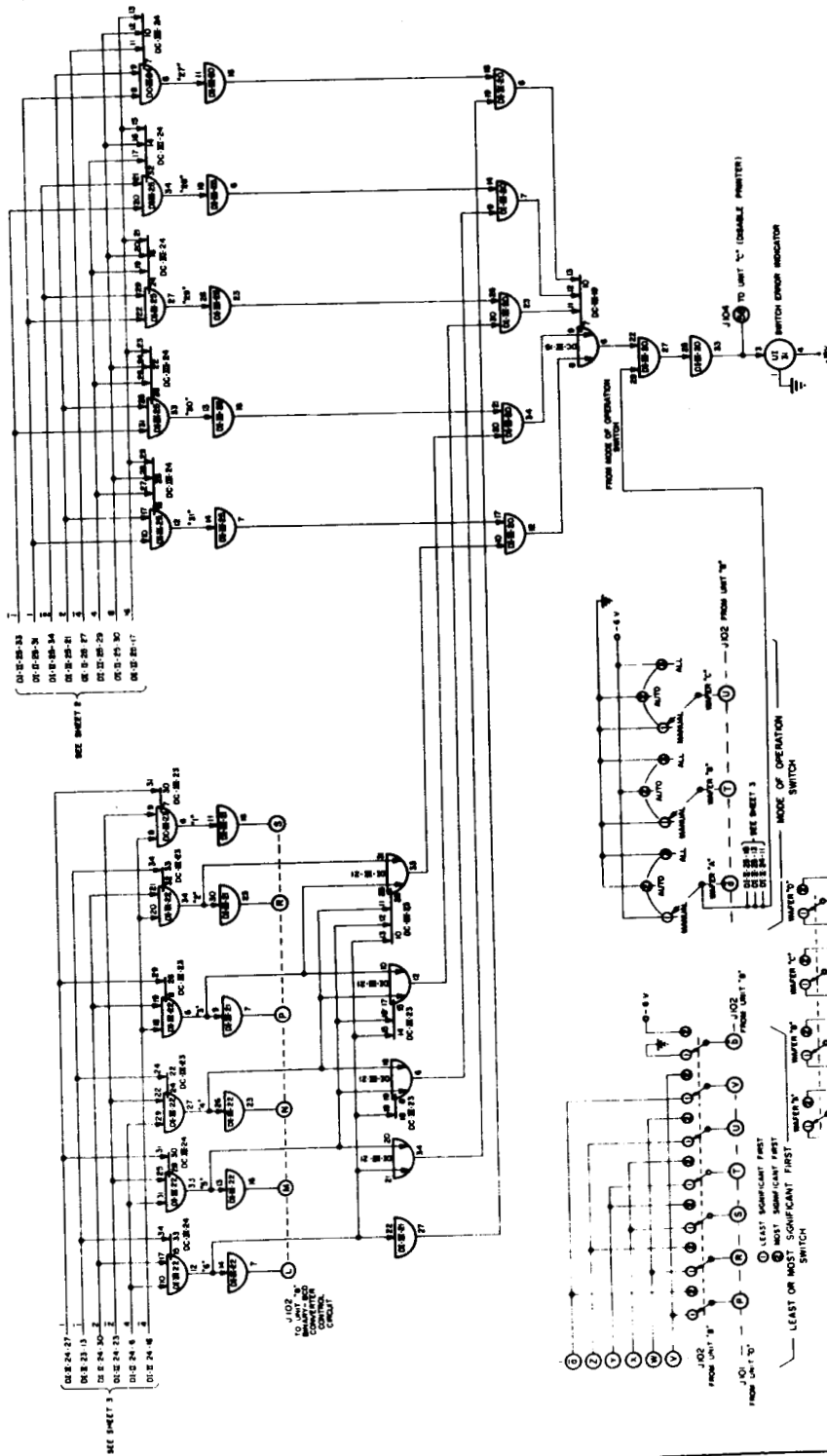
Figure VI-A-1 — Standard Symbols for Digital Modules (Sheet 1 of 2)

Figure VI-A-2 — Standard Symbols for Digital Modules (Sheet 2 of 2)

VI-5
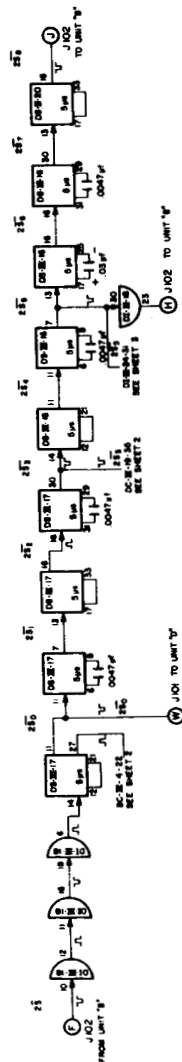
Figure VI-B-1 — Unit "A" — Time Control Strobe Pulse Generator & Switch Error Detector (Sheet 1 of 4)
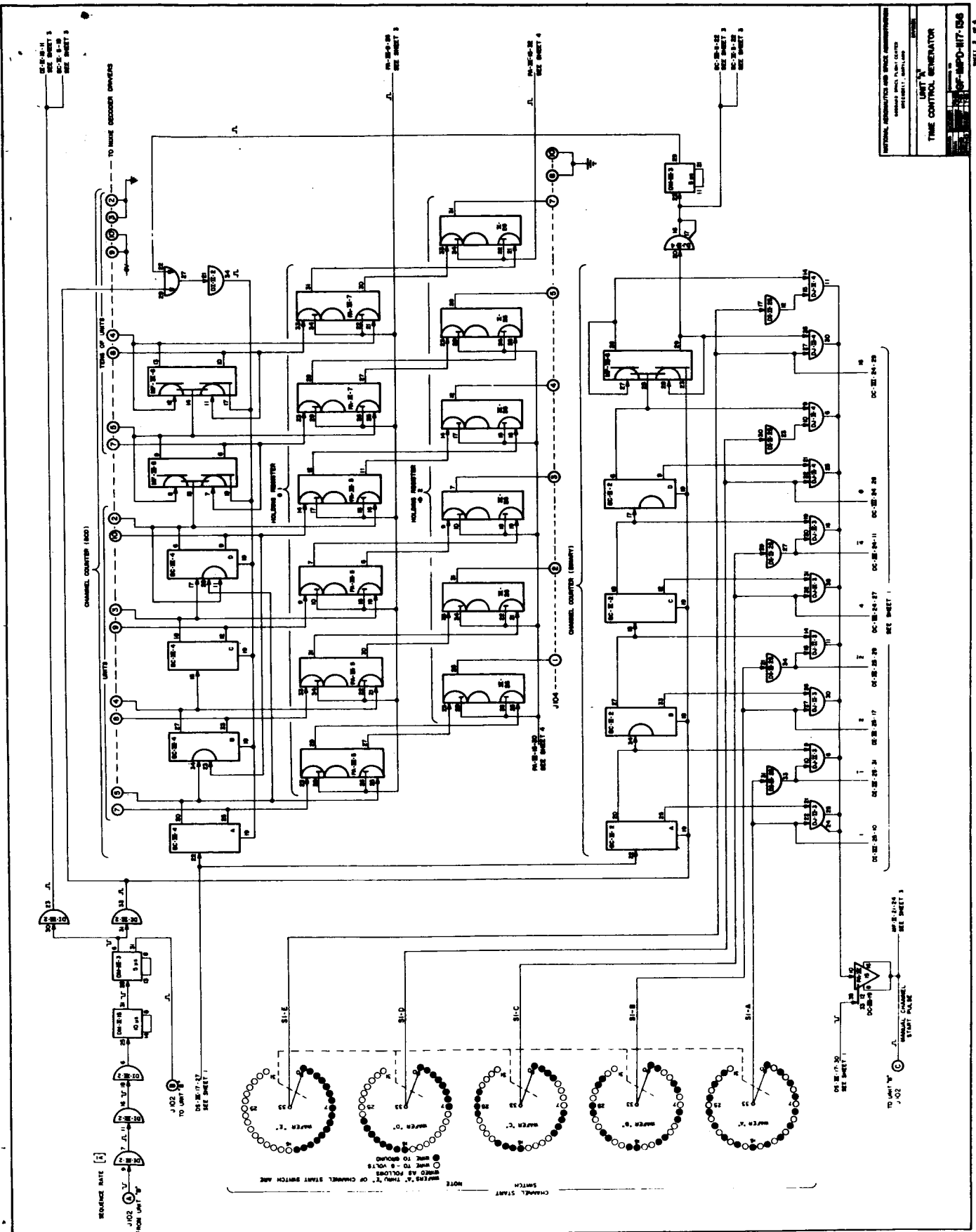
Figure VI-8-2 — Unit "A" — Time Control Generator (Sheet 2 of 4)

Figure VI-B-2 — Unit "A" — Time Control Generator, Frames Selector (Sheet 3 of 4)

Figure VI-B-4 — Unit "A" — Nixie Display & Printer Readout of the Decimal Equivalent of the Binary Number (Sheet 4 of 4)

Figure VI-B-5 — Unit "B" — Binary-To-BCD Conversion Timing Generator (Sheet 1 of 5)

Figure VI-B-6 — Unit "B" — Binary-To-BCD Conversion Register (Sheet 2 of 5)

VI-17

Figure VI-B-7 — Unit "B" — Binary-To-BCD Conversion Register (Sheet 3 of 5)

Figure VI-B-8 — Unit "B" — Simulator & Input Circuits (Sheet 4 of 5)
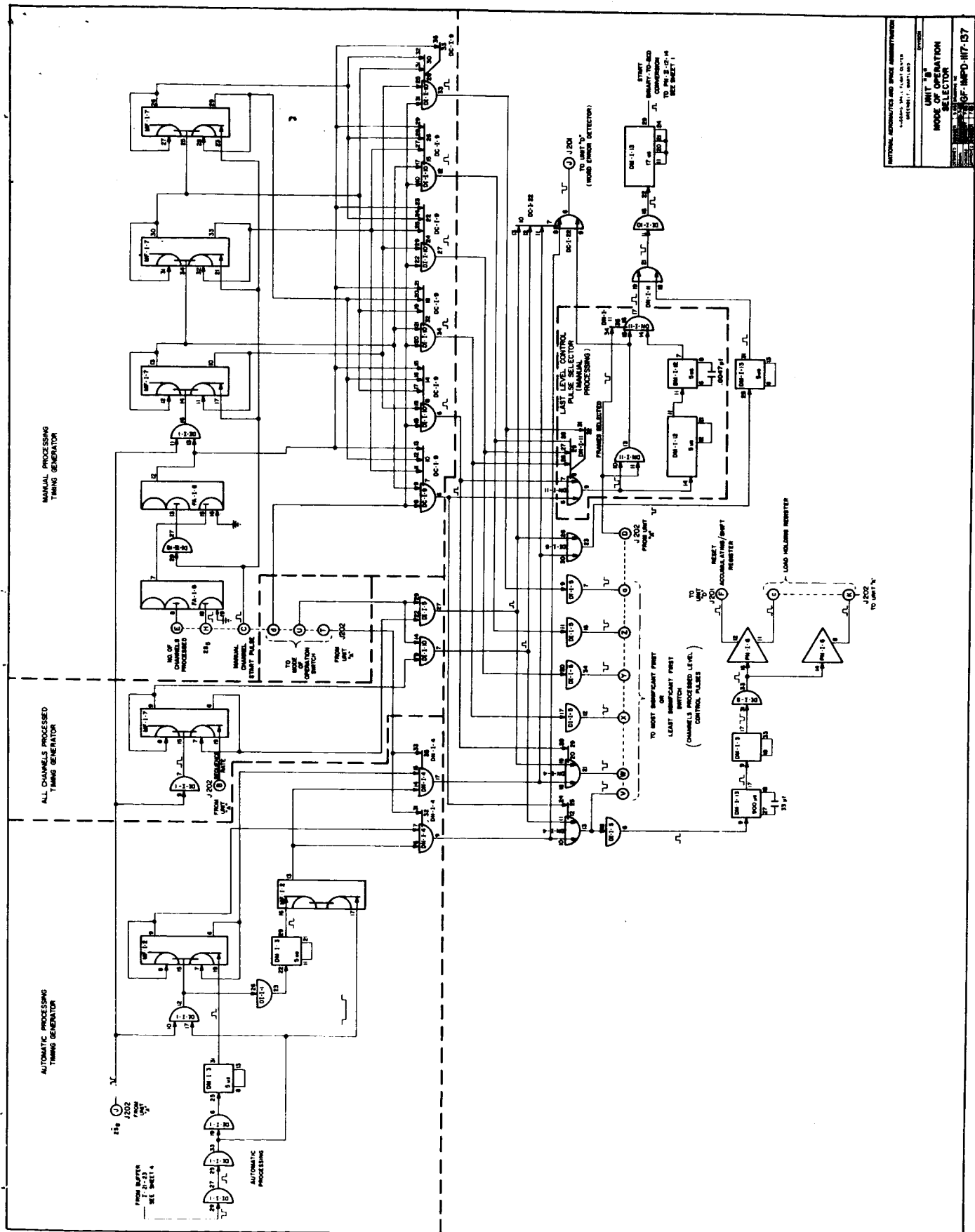
Figure VI-B-9 — Unit "B" — Mode of Operation Selector (Sheet 5 of 5)
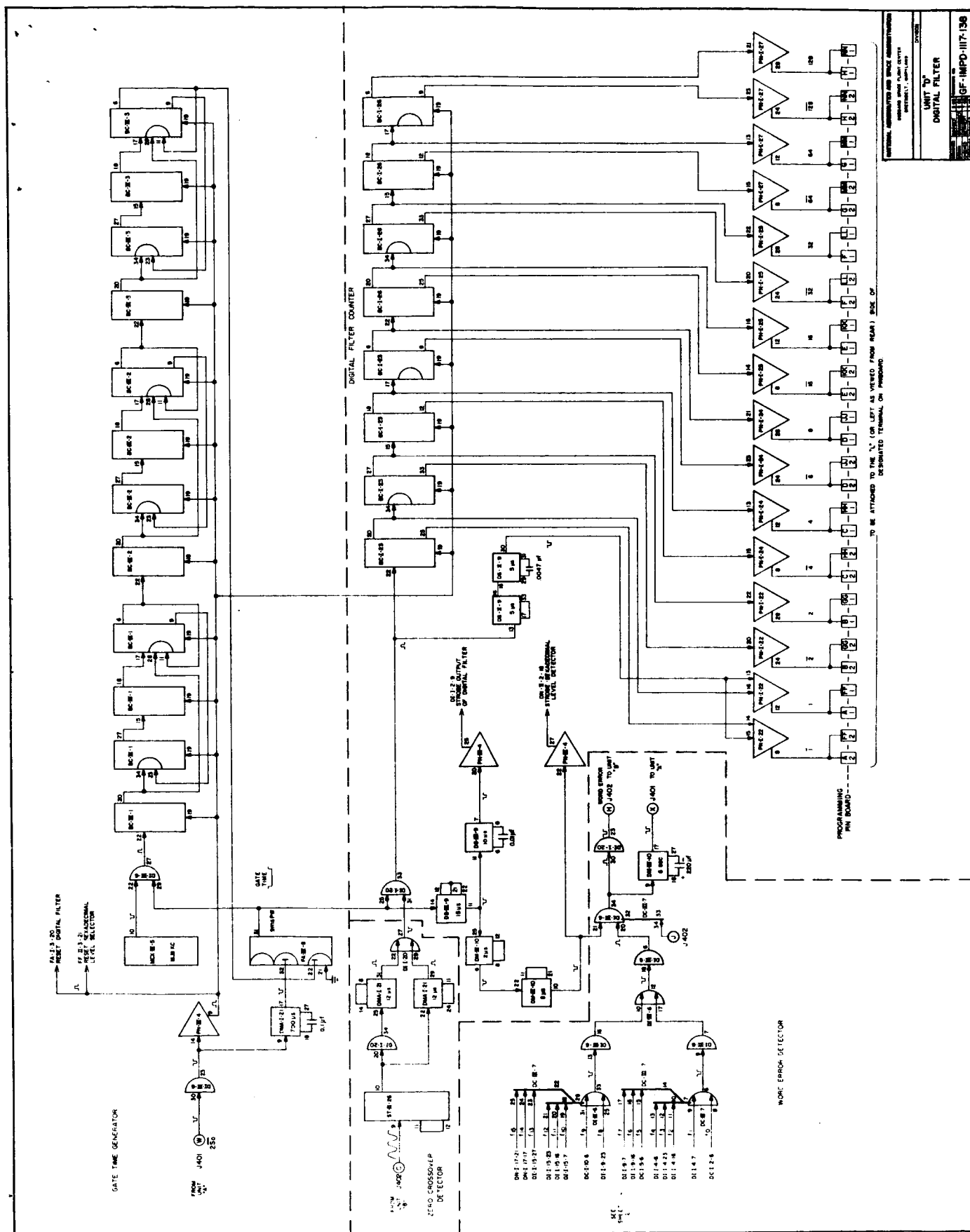
Figure VI-B-10 -- Unit "D" -- Digital Filter (Sheet 1 of 3)
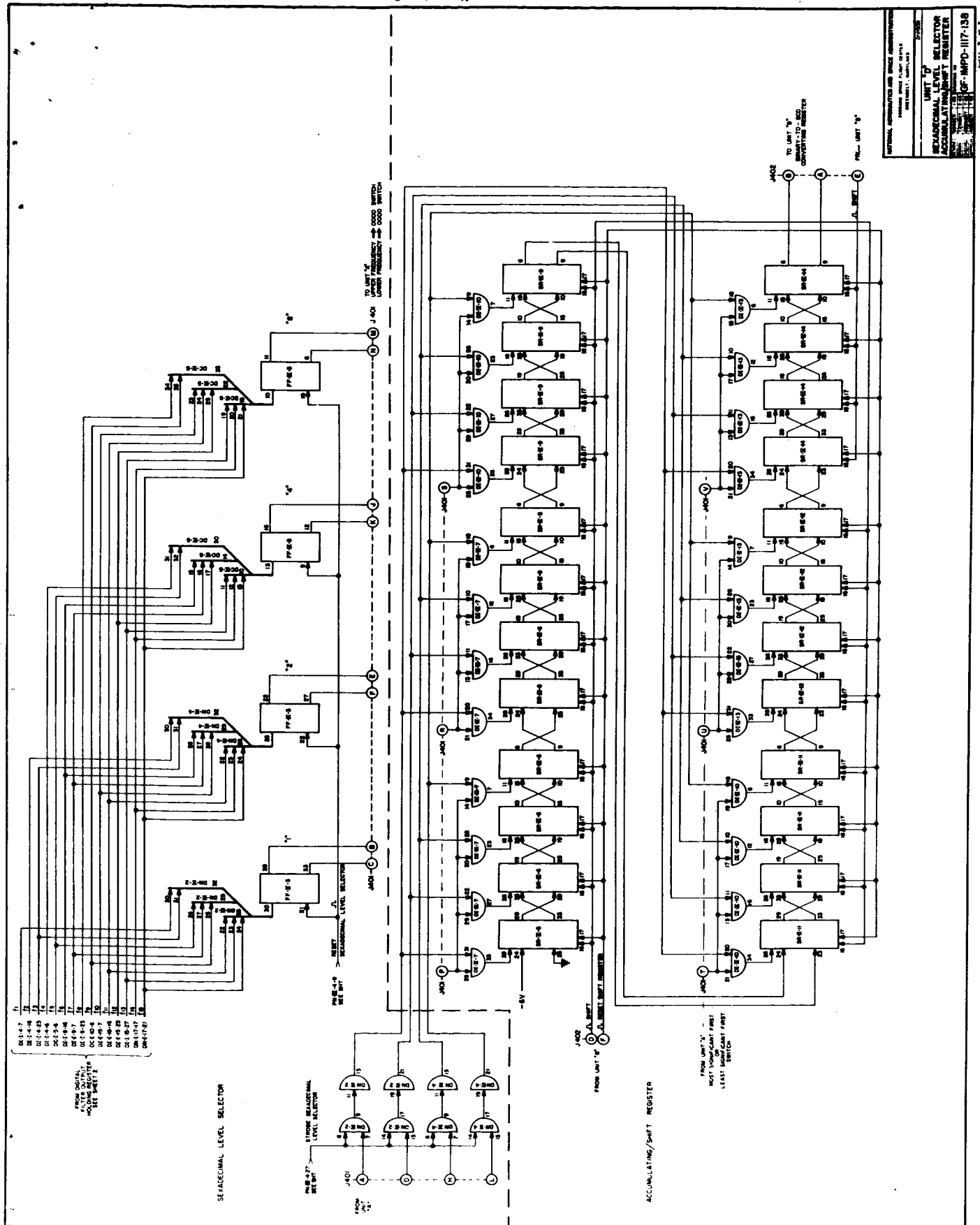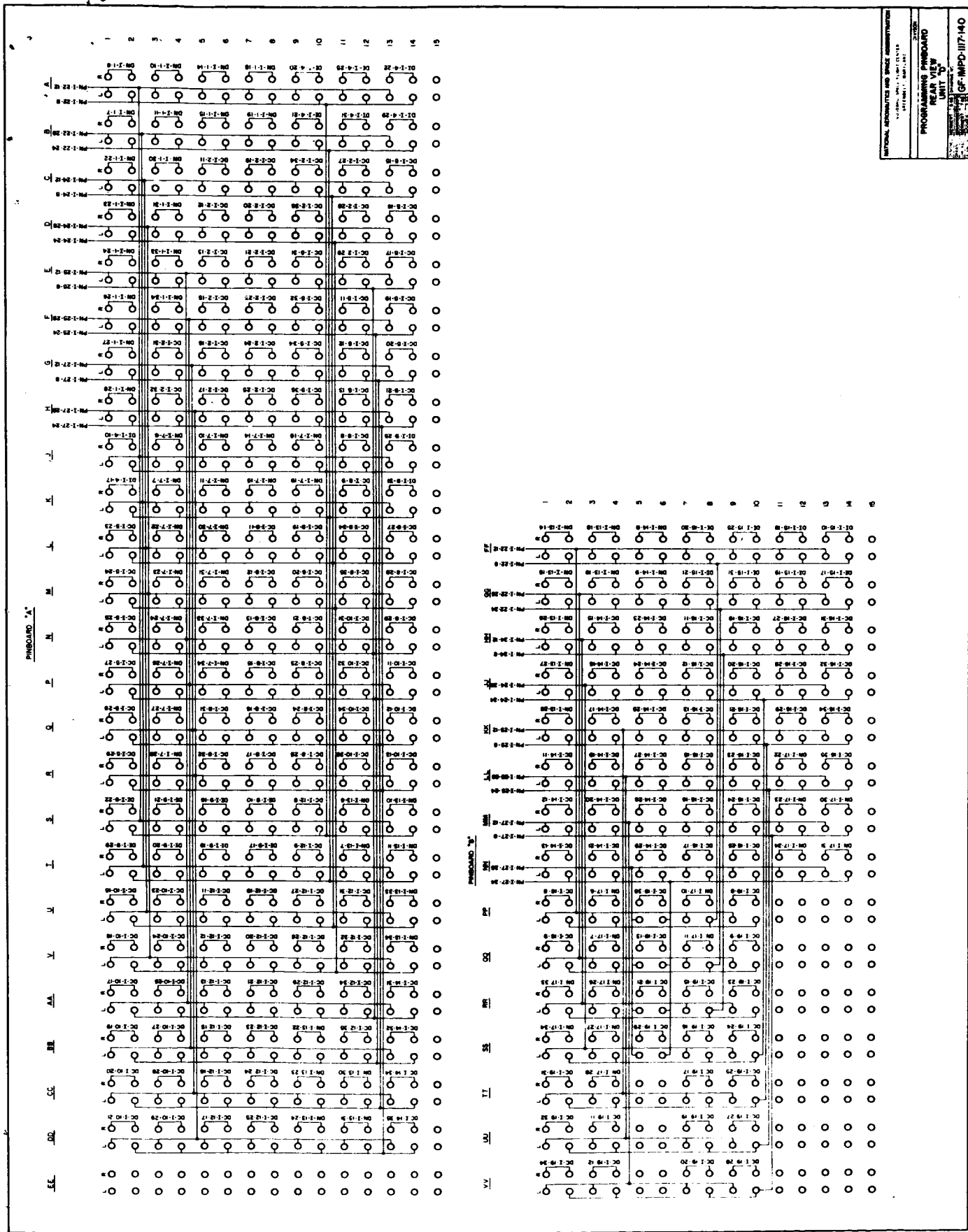
Figure VI-B-11 — Unit "D" — Digital Filter Output Holding Register (Sheet 2 of 3)

Figure VI-B-12 — Unit "D" — Sexadecimal Level Selector, Accumulating/Shift Register (Sheet 3 of 3)

Figure VI-B-13 — Unit "D" — Programing Pinboard, Rear View (Sheet 1 of 1)

Figure VI-B-14 — Unit "B" — Signal Conditioners (Sheet 1 of 1)

Figure VI-B-15 — PFM Simulator Card

Figure VI-B-16 — Band Pass Filter Card

Figure VI-B-17 — Buffer Card

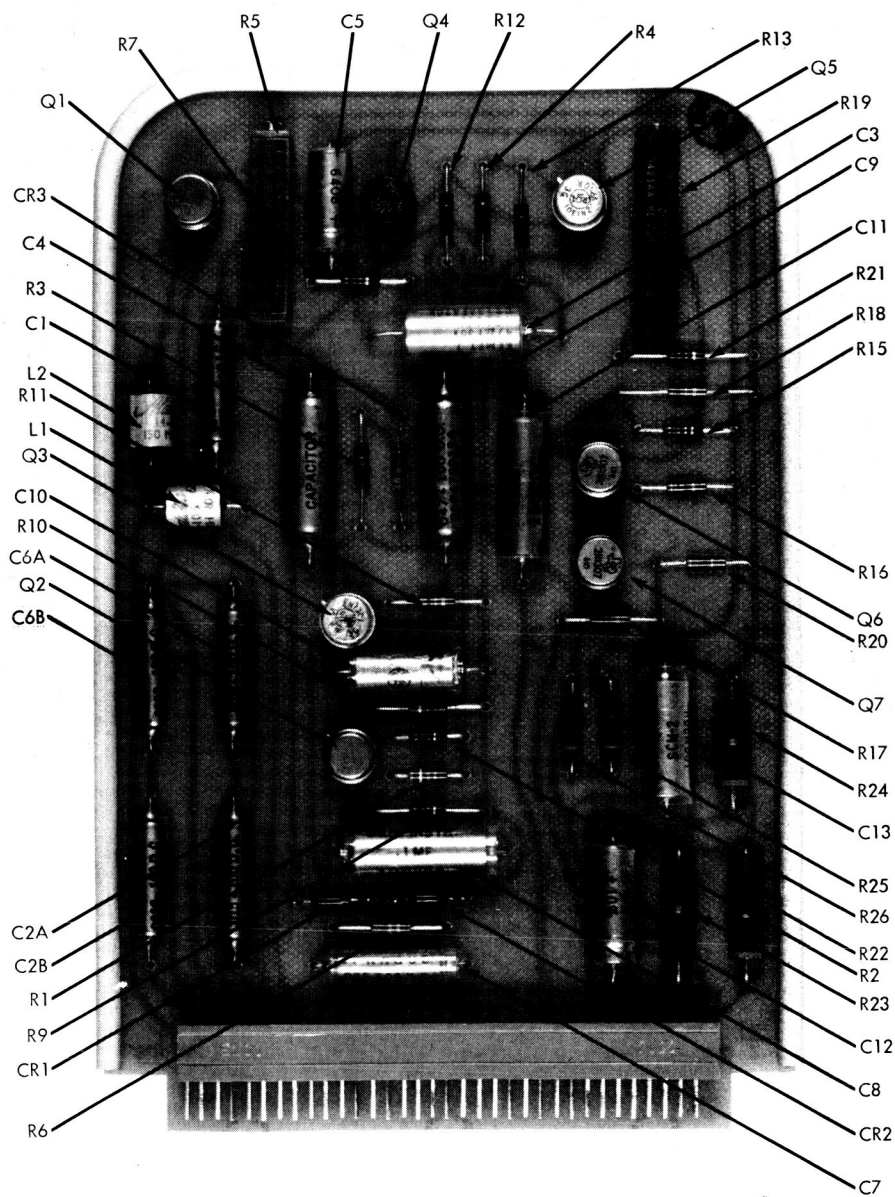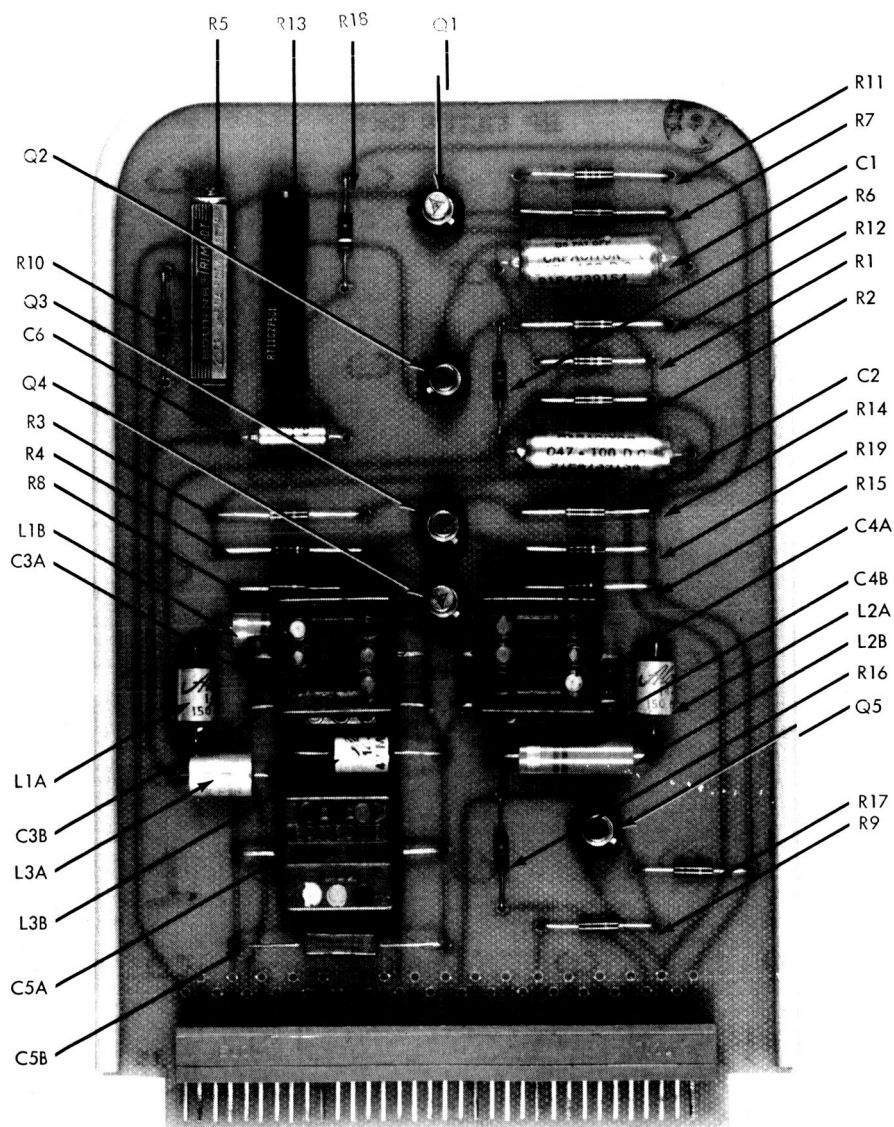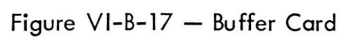# SECTION VII

CARD LOCATION DIAGRAMS

The card location diagrams are listed in Tables VII-1 through 3. These tables indicate the board type and connector number for each plug-in card.

Table VII-1 (Unit A)

Bloc No. I		Bloc No. II		Bloc No. III	
Board Type	Connector Number	Board Type	Connector Number	Board Type	Connector Number
	1		1		1
	2	BC	2	DI	2
	3	DJ	3	DM	3
	4	DJ	4	BC	4
	5	BC	5	FA	5
	6	DI	6	MF	6
	7	DC	7	FA	7
	8	DI	8	BC	8
	9	DC	9	FA	9
	10	DI	10	MDI20	10
	11	DC	11	MDI20	11
	12	DI	12	MDI20	12
	13	DC	13	MDI20	13
	14	DM	14	MDI20	14
	15	DM	15	PA	15
	16	DI	16	DS	16
	17	DI	17	DS	17
	18	DI	18	DI	18
	19	DI	19	DC	19
	20	DS	20	DI	20
	21	MF	21	DI	21
	22	DJ	22	DI	22
	23	IF	23	DC	23
	24	DI	24	DC	24
	25	DI	25	DI	25
	26	MFA20	26	MFA20	26
	27			MFA20	27

Table VII-2 (Unit B)

Bloc No. I		Bloc No. II		Bloc No. III	
Board Type	Connector Number	Board Type	Connector Number	Board Type	Connector Number
DI	1		1	UF	1
MF	2	BP Filter	2	UF	2
DM	3	OSC AGC AMP	3	DI	3
DN	4		4	DC	4
DI	5	DI	5	UF	5
PN	6	DI	6	UF	6
MF	7	DI	7	DI	7
FA	8	DI	8	FF	8
DC	9		9	DC	9
DI	10		10	UF	10
DN	11		11	UF	11
DS	12	PN	12	DI	12
DM	13	FA	13	UF	13
	14	MV	14	UF	14
	15	DM	15	DI	15
	16	DS	16	DC	16
	17	DM	17	FF	17
	18	DI	18	UF	18
	19	PN	19	UF	19
	20	FF	20	DI	20
Buffer	21	BC	21	UF	21
DC	22	MF	22	UF	22
	23	DI	23	DI	23
BC	24	DN	24	DC	24
BC	25	DN	25	UF	25
BC	26	DC	26	UF	26
MV	27			DI	27

Table VII-3 (Unit D)

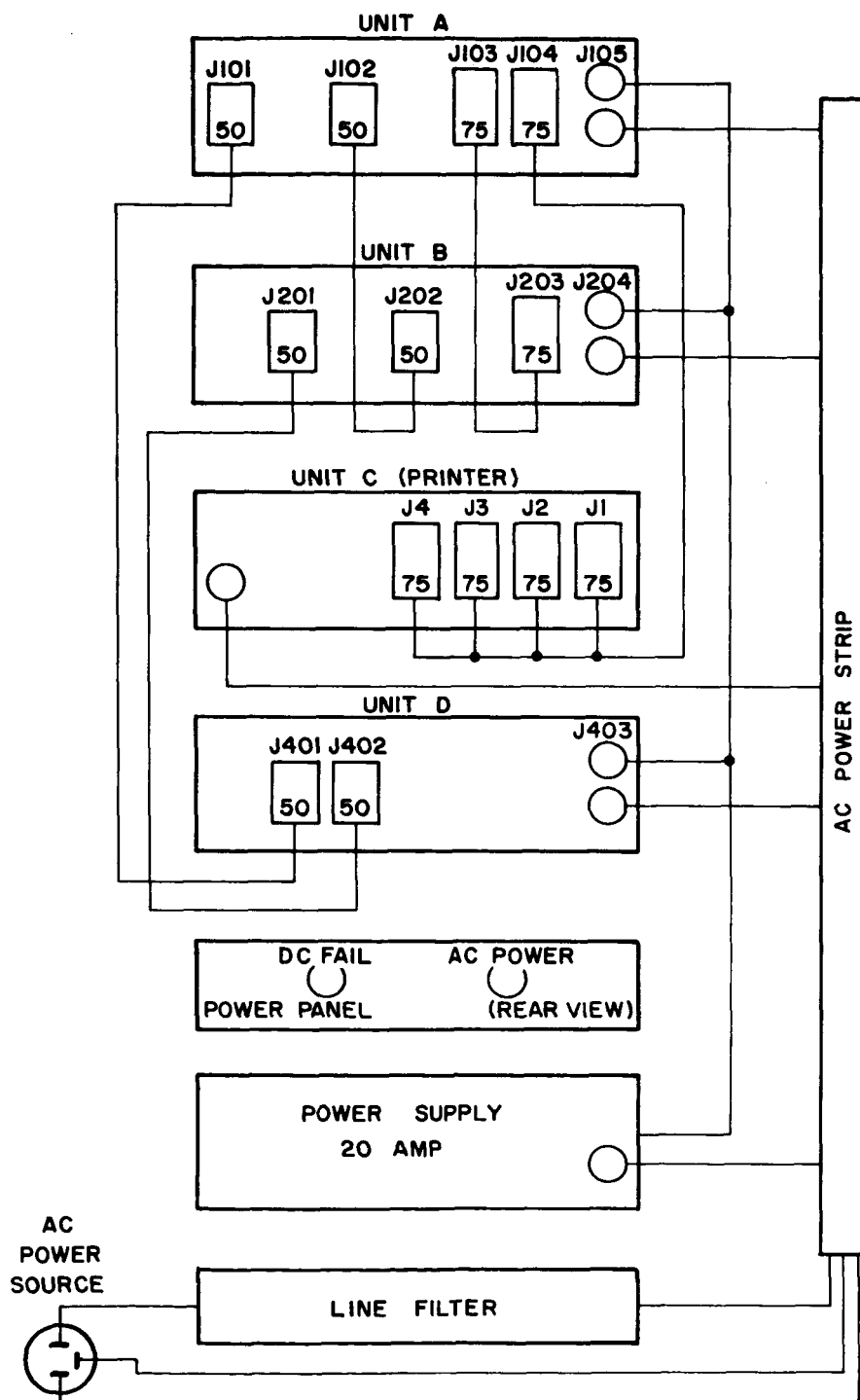| Bloc No. I		Bloc No. II		Bloc No. III	
Board Type	Connector Number	Board Type	Connector Number	Board Type	Connector Number
DN	1		1	BC	1
DC	2	DN	2	BC	2
FA	3	FF	3	BC	3
DI	4	DN	4	PN	4
DC	5	DC	5	MC	5
FA	6	SR	6	DI	6
DN	7	DI	7	DC	7
DC	8	SR	8	FA	8
DI	9	SR	9	DS	9
DC	10	DI	10	DM	10
FA	11	SR	11		11
DC	12	SR	12		12
DN	13	DI	13		13
DC	14	SR	14		14
DI	15		15		15
DC	16		16		16
DN	17		17		17
FA	18		18		18
DC	19		19		19
DI	20		20		20
DMA	21		21		21
PN	22		22		22
BC	23		23		23
PN	24		24		24
PN	25		25		25
BC	26	ST	26		26
PN	27				27

REAR VIEW

Figure VIII-1 — Interconnection Diagram.

SECTION VIII

INTERCONNECTION DIAGRAM

The interconnection cabling is shown in Figure VIII-1.

SECTION IX

REFERENCES

1. G. W. Nooger, "A Digital Data Processor for a Pulse Frequency Modulated Signal," M. S. Thesis, Department of Electrical Engineering, University of Maryland, May 1965.

2. Instruction Manual for S-Pac Modules and Equipment. Framingham, Massachusetts: Computer Control Company, Inc., 1964.

3. Instruction Manual for Hi-Speed Printer, Series 1000, Model 1040D-13-8A. Bridgeport, Pennsylvania: Franklin Electronics, Inc., 1965.