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APOLLO DIGITAL UP-DATA LINK DESCRIPTION

by Stuart D. Lenett

Manned Spacecraft Center

Houston, Texas

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SUMMARY

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This document describes the Digital Up-Data Link Equipment used on the Apollo command module. It is written in two parts: the first section is a general description of the equipment and its functions, and the second is a detailed description of the circuitry which makes up each subassembly and its individual unique function. This equipment, although similar to that used on the Gemini spacecraft, has had some major modifications; consequently, a description of the Gemini Digital Command System does not fit that of the Apollo Up-Data Link.

The Apollo Up-Data Link Equipment is a digital system comprised of three subassemblies, a UHF receiver, a sub-bit detector and a decoder.

The hardware is approximately 13.00 inches by 9.38 inches by 4.41 inches in size and weighs less than 20 pounds. It will fit in the lower equipment bay of the Apollo command module and operate from the spacecraft +28 V dc supply. The Up-Data Link will have the capability of interfacing with the Apollo guidance computer, central timing equipment, real-time command relays, and the PCM system. It will also be capable of receiving inputs from either a UHF receiver at a frequency range of 406 to 450 Mc or from an S-band receiver through the premodulation processor.

Author

INTRODUCTION

The Digital Up-Data Link Equipment used on the Apollo command module, although similar to Gemini Digital Command System, has undergone some major modifications. The present equipment is built by Motorola, Inc., Scottsdale, Arizona, under contract to North American Aviation, Inc., Downey, California.

The author wishes to express his gratitude and appreciation to Mr. John B. Hurst, Mr. William H. Harris, and Mr. J. D. Roberts, all of the Lockheed Electronics Company, for their aid and cooperation in the preparation of this document. He also wishes to thank Mr. Frank Jones of the Motorola Company, Scottsdale, Arizona, and Mr. Gary Covington, III, of North American Aviation, Inc., Downey, California, for their review and constructive comments on this document.

DEFINITIONS OF ABBREVIATIONS AND TERMS

BSN — The output signal of the divide-by-5 counter which is counting SBSN. This signal is phase-locked to the data bits and makes negative transitions for each 5 sub-bits.

SBSN — Sub-bit-sync-not is a signal which makes transitions with the sub-bit data signal and is phase-locked to it.

PG — This pulse is used to shift bits through the main-bit register; it has three frequencies determined by its mode of operation.

$\overline{CR}$ — The not-count register is the output of the programable counter. This output makes a negative going transition (6 V to 0 V) at the end of the programed count.

VA — The vehicle address refers to the vehicle flip-flop and associate circuits.

RTC — The real-time command is one of eight possible system commands. This command functions to energize 1 of 64 relay positions in the RTC matrix in the vehicle.

CTE — The central timing equipment is the clock and associated circuitry on the vehicle. It also is one of the eight possible system commands.

AGC — The Apollo guidance computer, located on the vehicle, can be loaded by one of the eight possible system commands.

TM — The test message, one of eight possible system commands, operates to provide the ground station a means of scanning an input word selectively for a bit status.

TLM — This is an eight-level output to the telemetry transmitter for 55 msec at each end-of-message reset time. This output indicates that the signal has been properly processed and shifted in the digital section.

SB — Sub-bit

SBN — Sub-bit not

EBNC — Error bit not correct

EPG — Enable pulse generator

PSK — Phase shift keyed modulation

EOMR — The end-of-message reset is a signal which makes a negative transition resetting the system after a proper message sequence is completed.

FF	The flip-flop is a bi-stable state device used to store and shift data bits.
NAND Gate	A device used as an inverting AND function.
NOR Gate	A device used as an inverting OR function.
INHIBIT	This pertains to NAND and NOR gates which inhibit the flow of data through the gate by applying 0 V to one input.
ENABLING	This pertains to NAND and NOR gates enabling the flow of data through the gate by applying +6 V to one input.
SET and SETTING	This pertains to FF operation causing pin Q to be +6 V.
CLEAR, CLEARING and RESETTING	This pertains to FF operation causing pin Q to be 0 V.
DIVIDE-BY-4 COUNTER	This term is used to describe the function of A25, A30 FF (shift register) which counts negative transitions of CR.
MAIN-BIT REGISTER	This contains flip-flops DR1 through DR24.
PROGRAMABLE COUNTER	This is a parallel loading counter which counts PG from PC0 through PC5.
QUALIFY or QUALIFYING	This pertains to an FF having the proper dc levels applied to its steering gate section so that it will set or clear if a negative transition is applied to its pulse input.

If FF is clear, to set: apply +6 V to ts2 and 0 V to ts1 followed by a negative transition on T.

If FF is set, to clear: apply 0 V to ts2 and +6 V to ts1 followed by a negative transition on T.

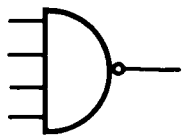
Alternate methods of setting a clear FF: apply 0 V to Sc and +6 V to Rc or leave Rc disconnected followed by a negative transition on S.

Alternate method of clearing a set FF: apply 0 V to Rc and +6V to Sc or leave Sc disconnected followed by a negative transition on R.

If both ts2 and ts1 have +6 V applied and a negative transition is applied to T, FF will not change state.

If both Sc and Rc have +6 V applied followed by a negative transition on the shift register, the FF will not change state.

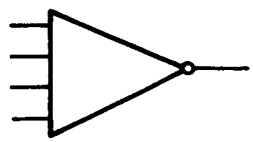
The NAND gate



All inputs = +6 V, output = 0 V

Any input = 0 V, output = +6 V

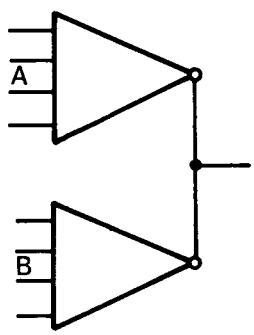
The NAND gate driver



Any one input = 0 V, output = +6 V

All inputs = +6 V, output = 0 V

The dual NAND gate

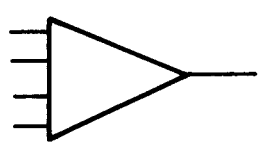


All A inputs = +6 V, output = 0 V

OR all B inputs = +6 V, output = 0 V

Any A input = 0 V,
and
Any B input = 0 V,
output = +6 V

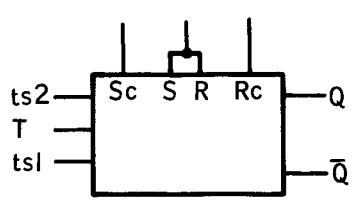
Relay select driver



All inputs = +6 V, output = +28 V

Any input = 0 V, output = 0 V

Flip flop



Clear state Q = 0 V

Set state Q = +6 V

Logic description

GENERAL SYSTEM DESCRIPTION

The Up-Data Link (UDL) used aboard the Apollo spacecraft is based upon a concept developed for the Gemini Agena program. This system is a digital system as opposed to the tone system used on the Mercury program. The Digital Command System, as it is known on Gemini, or the Up-Data Link, as it is known for Apollo, is a system over which digital information is transmitted to the spacecraft to perform three functions. First, it is used to enter words into the Apollo guidance computer (AGC) on board the vehicles; second, it is used to up-date the central timing equipment (CTE); and third, it is used to transmit real-time command (RTC) to turn equipment on or off by ground control.

The Digital Up-Data Link consists of a UHF receiver, a sub-bit detector, and a decoder. Audio may be fed into the decoder from an S-band receiver through the pre-mod processor to provide digital communications at lunar ranges.

The sub-bit detector recovers the timing information from a composite audio signal by means of a narrow-band phase-locked loop, and detects digital information by means of an optimum filter design.

The decoder detects the vehicle address and system address, stores and checks data, and processes the data to the appropriate spacecraft system.

The system is designed to receive an FM signal in the 406 to 450 Mc Band.

Data are transmitted by a PSK 2-kc tone. A second tone of 1 kc is linearly added to the phase-shifted tone to provide bit sync. This composite signal is then used to FM a UHF carrier for transmission to the spacecraft.

The word lengths proposed for the Apollo system are 12 bits for real-time commands, 22 bits for AGC word, and 30 bits for CTE up-date. The maximum word length is set at 30 bits. These bits are known as information or data bits. Each of the bits is sub-bit encoded to a 5-bit code.

All words contain 3 address bits for vehicle address, and 3 information bits for system address. This provides the choice of eight different vehicles and eight different systems. The remaining information bits comprise a real-time command, a computer word, CTE up-date or a test message.

After command reception, detecting, and decoding, the command, if completely valid, is transferred to the proper spacecraft system. After proper transfer of the command, a verification signal is transmitted via PCM telemetry to the surface command station.

A list of pertinent data is shown in the appendix.

FUNCTIONAL DESCRIPTION

A general description of the Apollo Up-Data Link was given in the general system description. In this section, a more detailed functional description will be covered. The system will be described in three parts – the UHF receiver, the sub-bit detector, and the decoder.

UHF Receiver

The Up-Data Link Receiver is a double conversion superheterodyne. It is designed to receive and demodulate an FM signal on a preset frequency within the 406 to 450 Mc region.

The choice of the local oscillator crystal frequency determines the operating frequency of the receiver.

The overall receiver noise figure is approximately 12 dB. For an IF bandwidth of 240 kc, the receiver noise level is -138 dBw and with an input signal level of -130 dBw, a signal-to-noise ratio of 8 dB can be obtained at the limiter input. The second IF amplifier is tuned to 10.7 Mc.

The signal passed through the limiter is detected in a Foster-Seeley type discriminator.

Sub-Bit Detector

A block diagram of the sub-bit detector is shown in figure 1.

Synchronization signals are detected by a phase-locked loop with a bandwidth of 20 cps. Data signals are detected by a phase-locked loop with a bandwidth of 1000 cps. Filtering is not required to separate the data subcarrier from the sync reference subcarrier since the two signals are orthogonal with respect to each other and are eliminated at their respective phase detectors.

The matched filter detects the data subcarrier and produces an output which consists of a series of sub-bits occurring at a rate of 1000 bits per second. The sub-bit sync signal, required by the matched filter, is fed to the decoder along with the detected sub-bits (fig. 2).

Decoder

The decoder, which performs the functions of address recognition, real-time command actuation, stored program data buffering, and data transfer to other spacecraft systems, can be segregated as follows:

1. Bit detection and basic timing generation
2. Address recognition

3. Program timing generation
4. Data buffer storage
5. Real-time command decoding
6. Interface circuits.

Bit detection and basic timing generation.- The detected sub-bits (data and sync signals) are used to clock the non-return-to-zero (NRZ) sub-bit information into a five-stage register. This register is sampled to determine if a bit 1 or 0 is present. If the bit recognition occurs during an invalid time, the system will automatically be reset. Basic timing is used to generate program timing. Generation of basic timing consists of dividing the sync signal by 5 to produce a bit-sync reference signal, starting at bit recognition time. Bit values 1 and 0 are fed to the 24-bit storage data register.

Address recognition.- Vehicle address and system address are each coded into 3 information bits (15 sub-bits), allowing the selection of any one of eight possible vehicles and eight possible systems. System address is recognized after the proper vehicle address has been received and 3 new information bits are stored in the data register. Decoding and storage of the system address is performed using clocked techniques. Stored system address determines program control operation and is required to enable data transfer function.

Program timing generation.- The Digital Up-Data Link has the capability of handling three different length commands. These may be 12, 22, or 30 bits long. The program timing system senses the correct command length from the system address and provides timing to control reception, data transfer, and verification in the proper sequence.

Data buffer storage.- Buffer storage is provided to hold an incoming command until processing and verification is complete. The data register also provides storage for real-time commands and addresses until decoding or output actuation is completed. Data bits are shifted serially into the 24-bit data storage register by clock and gating pulses received from the basic timing generator and program timing system. Upon receipt of a complete word stored command, the data will be serially shifted out to the using system.

Real-time command decoding.- The data register provides 6 bits to the real-time command decoder. The first 5 bits received select 1 of 32 relay drivers and the last bit (6th bit) determines the set or reset condition selected. The relays used in this system are dual coil magnetic latching relays. The set and reset drivers are capable of providing a minimum of 10 milliamperes into a load impedance between 900 and 1600 ohms.

Interface circuits.- The Up-Data Link System interfaces in six distinct areas. These are (1) UHF/off/S-band switch (located on the communications control panel), (2) Apollo guidance computer (AGC), (3) real-time command (RTC) units, (4) PCM telemetry, (5) central timing equipment (CTE), and (6) block-accept switch (located on computer control panel).

1. The UHF/off/S-band switch is used to select the UHF mode for near-earth operation, the off mode which opens the 28-V dc spacecraft power input to the Up-Data Link, and the S-band mode for deep-space operation. The inputs

to the mode switch are PSK audio from either UHF receiver or the premodulation processor. The premodulation processor input is the 70-kc subcarrier from the S-band transponder.

2. The Up-Data Link will serially feed computer words to the AGC upon correct receipt of an end-of-message command. The output pulses will be 4 ±1 microseconds at 50 percent amplitude at a 7 ±3-V dc amplitude. This signal is fed to the computer on two separate lines, one for data 1 and the other line for data 0.

3. The real-time command interface will be a relay closure which will energize a line to turn a selected piece of equipment on or off. These relays will have a dc coil resistance of 1240 ohms ±10 percent, a pickup current of 9 milliamps dc maximum, and an operating time of 12 milliseconds maximum with 10 milliamps coil current applied.

4. The verification interface will be an 8-bit digital-code verification word provided to the PCM in parallel format. The verification is direct coupled to the PCM telemetry equipment. The circuit will be capable of sustaining a pulse of 55 ±5 milliseconds.

5. The central timing equipment interface will reset the CTE time accumulator to 0 and up-date register to the new time, using pulse counting techniques.

6. The block-accept switch disconnects the UDL lines which go to the computer.

DETAILED CIRCUIT DESCRIPTION

The preceding section discussed the Apollo Up-Data Link in fairly general terms, elaborating the functional aspect more than the physical operation of the system. This section will describe the detailed operation of the circuits and subassemblies that make up the UDL.

UHF Receiver

The UHF receiver (fig. 3) used on the Apollo command module is a modified unit presently being used on the Gemini program. It consists basically of five assemblies. These are:

1. Tuned cavity pre-selector
2. RF amplifier
3. First IF amplifier
4. Band-pass filter
5. Second IF amplifier

The receiver is all transistorized and operates from -18 and -6 V dc. The output is a composite audio signal of a linear summed 1-kc and phase-shift

keyed 2-kc tone. In addition, the receiver signal strength is monitored in the second IF assembly and may be sent to the PCM-TLM system for transmission to ground stations.

Tuned cavity preselector assembly.- The tuned cavity preselector consists of two tunable band-pass sections and a low-pass section. The band-pass sections are tuned to the receiver operating frequency while the low-pass section is tuned to reject high frequencies. The coaxial connector to the receiver is an integral part of the preselector.

RF amplifier assembly.- The RF amplifier is an addition to the Gemini UHF receiver design. This amplifier allows a 6-dBm improvement in receiver sensitivity and yields approximately a 4-dB improvement in noise figure. This assembly is a two-stage amplifier using 2N2415 grounded emitter transistors. The amplifier is tuned by adjustable capacitors in a collector LC network. A resistor divider network is used to set bias levels of the amplifier stage. Transformer coupling is employed between each stage of the RF amplifier assembly and is used to couple the RF amplifier assembly to the first IF.

First IF amplifier assembly.- The first IF assembly consists of a crystal controlled Colpitts type local oscillator, two frequency doublers, three stages of amplification, a buffer amplifier, and mixer. A crystal controlled local oscillator (LO) which can be tuned to any frequency in the range from 83 to 92 Mc is used, and the choice of the local oscillator crystal frequency determines the operating frequency to which the receiver is tuned (406 to 450 Mc). The LO frequency is quadrupled before injection at the first mixer. The exact IF frequency is, therefore, determined by the frequency of the incoming RF signal and the setting of the local oscillator. Grounded base inductance tuned, common emitter and common collector amplifiers are employed. The LO output is also fed to a buffer amplifier and to a second mixer to yield a second IF frequency of 10.7 Mc. The output of the 10.7-Mc amplifier is fed to a band-pass filter. The IF amplifiers are broad tuned while the band-pass filter is narrow band tuned. This means that the receiver selectivity is governed primarily by the filter characteristics. The IF bandwidth of the receiver is not less than 220 kc at the -3-dB points and is not greater than 1200 kc at the -60-dB points. (Fig. 4.)

Band-pass filter.- The band-pass filter is a lumped constant LC filter with a 3-dB bandwidth of approximately 200 to 250 kc. It has a 1-Mc bandwidth at the 60-dB point. The filter insertion loss is less than 15 dB with a 50-ohm-input impedance and loaded by a 20-ohm-input impedance of the second IF amplifier.

Second IF amplifier assembly.- The second IF amplifier assembly consists of three stages of amplification prior to the limiter, a limiter and Foster-Seeley-type discriminator, and two stages of audio amplification. The 10.7-Mc IF amplifiers provide approximately 60 dB of gain to the limiter. The tuned circuit in the limiter collector serves as the discriminator. Two adjustable inductors (primary and secondary) are independently tunable to allow optimum sensitivity and linearity of design. The discriminator is followed by two stages of audio amplification using feedback techniques to insure stability.

Provision is made to set the output audio voltage at 1 volt ± 10 by selection of the gain resistor in the input circuit of the audio amplifier. (Fig. 5.)

Sub-Bit Detector

The primary function of the sub-bit detector in the Apollo UDL is to separate the data from the sync tones and transfer these sub-bits to the decoder for decoding, verification, and transfer to the user system. Inputs to the sub-bit detector may be from either the UHF receiver or from the premodulation processor. Both inputs are fed through a mode switch which can be externally controlled from the astronauts' control panel. (Fig. 6, 7, 8.)

Sync signal detection.- The sub-bit detector utilizes a 4-kc voltage controlled oscillator (VCO) which is used to mix with the incoming data and sync signals for detection. The 4 kc are divided first by two and then again by two to yield a 1-kc square wave signal 90° out of phase with the incoming 1-kc sync signal. The phase detector in the sync circuit, made up of a transformer (center tapped) and a chopper amplifier, multiplies the 1-kc reference and 1-kc-sync signal. Any difference in phase will produce a dc voltage at the center tap of the transformer which is fed to the loop filter. This voltage, after being filtered, is used to vary the VCO and correct for the phase difference. This lock of the VCO reference to the 1-kc sync must be accomplished prior to any data detection. Once lock is accomplished, the 1-kc reference signal is inverted and fed to the decoder for use there. The 2-kc square wave is fed to an AND gate and gated to the decoder by the 1-kc-square wave to generate the sub-bit-sync-not (SBSN) signal.

Information signal detection.- The information signal detector also utilizes the transformer chopper technique, but now the 2-kc square wave generated by the VCO is multiplied with the information signal (2 kc). The information signal product is fed to an integrator and dumped at a 1-kc-repetition rate. This dump signal is generated by a 30-microsecond monostable multivibrator triggered by the SBSN. The input signal to the matched filter amplifier is a narrow pulse whose polarity is determined by the integrator voltage. The output of the matched filter is fed to the first stage of the sub-bit decoder register located in the sub-bit detector and triggered by a 10-microsecond monostable. This is a different design than that used by the Gemini sub-bit detector which does not use the sub-bit detector flip-flop as the first stage of the decoder register.

Decoder

Sub-assembly functions applied to the integrated system.- Pulse generator (PG) pulses are used to shift bits through the main-bit register. The frequency of the PG pulses is 200 cps, 1 kc, or 10 kc, depending upon the mode. PG pulses are also NANDed with the Q output of the vehicle flip-flop (FF) to supply the negative going transitions to the trigger (T) input of the flip-flops of the programable counter when it is counting.

Five sub-bits are necessary to decode each information bit. The sub-bits are shifted serially into the sub-bit register. As each sub-bit is shifted into the register, the register is sampled in parallel form. Outputs of two NAND gates are used as steering levels to shift the bits into the main register. PG pulses will shift the decoded levels into the main-bit register.

The first three stages of the main-bit register are continuously monitored by eight NAND gates. These gates monitor all eight possible states of the first three stages. Before the vehicle is launched, the output of one of these gates will be connected as a steering level to the vehicle flip-flop. If this unique vehicle address is properly decoded, a level will be established at the vehicle flip-flop so that it is qualified to be set by a divide-by-5 counter in the sub-bit decoder.

As the vehicle FF is set, it causes three things to occur:

1. It loads a count of 3 into the programable counter.

2. It enables the gate, which passes shift pulses to the programable counter.

3. It switches the 2-sub-bit decoding gates to 2 other sub-bit decoding gates and, consequently, selects a different code for the logic 1- and 0-bit levels.

The third count of the programable counter causes a divide-by-4 counter to count 1, which loads the system address into the main storage register. There are eight storage FF in the register and the one corresponding to the system selected will be set.

The RTC system will be selected if S7FF is set. The following sequence of events will occur. The programable counter will be loaded with a count of 6. As the programable counter counts to 0, it causes a divide-by-4 counter to count to 2. This inhibits any further shift pulses to the main-bit register. It also energizes the proper relay in the relay decoding matrix. It also resets the main bit register which loads a count of 32 into the programable counter. The RTC relay selected will remain energized until the programable counter reaches 0. At count 0, the programable counter causes $\overline{CR}$ to make its third negative transition. This enables A21 (reset gate), and as CR goes to +6 volts, it resets the system. $\overline{CR}$, not count register, is the output of the programable counter. This output makes a negative going transition (+6 V to 0 V) at the end of the programed count.

The AGC operation for the vehicle and system address is similar to that described for an RTC word, with the exception of the system selection. When the AGC system is selected, it loads the programable counter with a count of 16. This clocks in the 16 information bits of the AGC word into the main-bit register.

At the count of 16, the last data bit has been placed in the register and $\overline{CR}$ from the programable counter makes its second negative transition. Also,

the generation of PG pulses are changed from BSN (200 cps) to the $\overline{1\text{-kc}}$ dependency, and the programable counter is reset to count 16 additional pulses of PG. The first 16 serially clock out the data through DR16 at a $\overline{1\text{-kc}}$ rate. At count 16 of the programable counter, $\overline{CR}$ makes its third negative transition and resets the system. (Fig. 9, 10.)

Central timing equipment operation.- The CTE operation for the vehicle and system address is similar to that described for an RTC word, with the exceptions of the system selection and inhibiting of the system resetting function.

When the CTE system is selected, it loads the programable counter with a count of 24. This clocks the 24 information bits of the CTE word into the main-bit register at negative transitions of BSN (200 cps) and puts out 24 pulses on the CTE reset line.

At the count of 0, the last information bit has been clocked into the register and $\overline{CR}$ from the programable counter makes its second negative transition. Also, the generation of PG pulses are changed from BSN (200 cps) to the 20-kc astable dependency causing PG to have a 10-kc frequency rather than 200 cps.

As $\overline{CR}$ returns to +6 V, it sets the RA FF. This causes the following events to occur, the output to the CTE seconds line is enabled, and the shift pulses to the main-bit register are disabled. The first 6 information bits which have been shifted into DR19 through DR24 are parallel dumped into the programable counter.

The counter counts the 10-kc pulses until it reaches the 0 count. During this time, these pulses are output over the CTE seconds line until $\overline{CR}$ goes to 0 V, which causes the RA FF to be cleared. This inhibits all outputs to the CTE equipment, enables data to be shifted in the main bit register, again loads a parallel count of 6 into the programable counter, and as the counter again counts to 0, the second 6 information bits are shifted into DR19 through DR24. At the count of 0, these information bits will be dumped into the programable counter and $\overline{CR}$ will make a negative transition which causes RA FF to be set.

As the RA FF is set, the second group of 6 information bits are parallel dumped into the programable counter, the shift pulses are inhibited in the main-bit register and the minutes line to the CTE is enabled. As the counter counts, the 10-kc PG pulses are output on the minutes line to the CTE equipment. When the programable counter reaches its programed count, $\overline{CR}$ makes a negative transition which clears the RA FF.

Clearing the RA FF causes the output to be inhibited to the CTE equipment, and the main-bit register shift-pulse gates are enabled. The programable counter is once again loaded with a count of 6, and the second count is given to TD1 and TD2 FF register.

As the programable counter again counts to 0, the third group of 6 information bits are shifted into the DR19 through DR24. At count 0 of the programable counter, $\overline{CR}$ makes a negative transition which sets RA FF.

Again, as the RA FF is set, it causes the third 6-information-bits group to be parallel loaded into the programable counter; the shift pulses are inhibited in the main-bit register, and the hour line to the CTE is enabled. As the counter counts the 10-kc PG pulses, they are output on the hours line to the CTE equipment. When the programable counter reaches its 0 count, $\overline{CR}$ makes a negative transition, which again clears the RA FF.

When clearing the RA FF causes the output to the CTE equipment to be inhibited, the main-bit register shift-pulse gates are enabled, the programable counter is loaded with a count of 6, and the third count is given to TD1, TD2 FF register.

As the programable counter again counts to 0, the fourth group of 6 information bits are shifted into DR19 through DR24. At the count of 0 of the programable counter, $\overline{CR}$ makes a negative transition which again sets RA FF.

As the RA FF is set, the fourth 6-information bits group are parallel loaded into the programable counter, the shift pulses are inhibited in the main bit register, and the day line to the CTE is enabled. As the counter counts the 10-kc PG pulses, they are output on the day line to the CTE equipment. When the programable counter reaches its programed count, $\overline{CR}$ makes a negative transition which clears the RA FF.

Clearing the RA FF causes the output to the CTE equipment to be inhibited, and the main-bit register shift-pulse gates are enabled. The programable counter is loaded with a count of 6, and the fourth count is given to TD1 and TD2 FF register.

The fourth negative transition to TD1 and TD2 FF register causes TD1 and TD2 to both be +6 V which qualifies A12 pin 10 to reset the system.

Test message operation.- The test message (TM) word is similar for the vehicle and system address to that discussed for the RTC word, with the exception that the system selected is the TM system. When the TM system is selected, it loads the programable counter with a count of 24. This clocks the 24 information bits of the TM word into the main-bit register. At the count of 0, the last data bit has been placed in the register, and $\overline{CR}$ from the programable counter makes its second negative transition. Also, the generator of PG pulses are changed from BSN (200 cps) to the 1-kc dependency, and the contents of the first 6 information bits are parallel dumped into the programable counter. As the counter counts the programed number of pulses, the remaining 18 bits are shifted into DR24. As the 0 count is reached, the bit which is in DR24 will be output to the TLM system, and an end of message reset is generated. The TLM output reflects the contents of DR24 in either the set or clear status by generating a unique 8-bit parallel code. This system permits the observation of any bit in the register and indicates the proper operation of the sub-bit section, main-bit register, programable counter, and reset function.

Generation of PG shift pulses.- The sub-bit levels are dumped into the sub-bit register in serial form as a bi-level signal from the sub-bit detector section. Other signals available from the sub-bit detector are 1-kc and 2-kc timing. A derivative of this timing, which is also available, is sub-bit-sync-not (SBSN). This signal makes negative transitions at a 1-kc rate and is phase locked to the data so that the negative transitions occur with the sub-bit data transition.

Bit-sync-not operation.- The divide-by-5 counter is triggered by the negative transitions of the SBSN. The output of this counter is AND with the 1-kc and 2-kc signals to generate an output which makes a negative transition mid-band of 1-sub-bit data bit for each 5 sub-bits and remains at 0 V for the period of 250 usec then returns to +6 V. This timing signal is termed BSN and is used to generate the main-bit timing PG. The main-bit timing is PG. The A3 FF divide-by-2 divides 20 kc down to 10 kc as long as gate 47 pin 1 is enabled with pin 2 and 4 equal to +6 V. When either pin 2 or 4 is 0 V, the counter will lock up so that it is in the clear state. If this condition occurs when it is in the set state, the next negative transition of the 20-kc astable signal will clear it and then lock it up in the clear state. If it is in the clear state already, it will remain there. (Fig. 11.)

PG operation.- PG has three modes of operation. The first mode will generate a negative transition signal which is 100 usec wide and returns to 0 V for 4.9 milliseconds and then makes another negative transition. For this mode, A7 pin 9 = 0 V, A13 pin 9 = 0 V, and A13 pin 8 inhibited = 0 V. The negative transition of BSN causes the enable pulse generator (EPG) FF to be set enabling A7 pin 1. PG will be clear from previous lock up; the first negative transition of the 20 kc sets PG. The second negative transition of 20 kc clears PG making Q go from +6 V to 0 V; this is a negative transition which resets FF EPG causing pin Q to be 0 V which inhibits A7 causing TS1 and TS2 of PG FF to be +6V. Therefore, A13 pin 9 will remain 0 V and PG will continue with negative transition of BSN.

The second mode of operation has a $\overline{\text{PG}}$ signal generating a negative transition signal which is 100 usec wide and returns to 0 V for 0.9 ms and then makes another negative transition. For this mode of operation, A13 pin 8 has a $\overline{\text{1-kc}}$ signal, A13 pin 9 is +6 V, and RC is 0 V. The PG and EPG FF's are both clear and BSN will have no effect, since TS1 and TS2 are both +6 V. The $\overline{\text{1-kc}}$ signal causes EPG pin S to make a negative transition setting the EPG FF. This enables A7 pin 2. This applies +6 V to TS2 and 0 V to TS1 of PG FF. The first negative transition of the astable sets PG FF and the second negative transition clears PG FF. This causes pin R of EPG FF to make a negative transition which clears it. EPG FF will remain clear, inhibiting A7 until the next negative transition of the $\overline{\text{1-kc}}$ timing.

The third mode of operation has a PG signal which is a square wave 10-kc period. For this mode of operation, EPG FF has RC + 6, TS1 + 6 V, S = 0. This causes EPG FF to be disqualified for setting by BSN and also disqualifies EPG for resetting by negative transition at Pin R. Since EPG cannot be reset,

it will remain in the set state and Q will be +6 V. This leaves A7 enabled and PG FF will continue counting the 20-kc astable. This causes PG to have a 100-usec period.

Operation of sub-bit shift register and decoding.- Sub-bits enter the bit detector-sub-bit synchronizer as two complementary dc levels from the output FF in the sub-bit detector. An FF in the register is designed to contain a logic 1, if Q = +6 V and a logic 0, if Q = 0 V.

The sub-bits are shifted into the register with negative transitions of SBSN. This is a +6 V level which makes a negative transition just before the end of each data sub-bit time, remains at 0 V for 250 usec and then returns to +6 V until the end of the next data sub-bit time.

The five sub-bits are translated into a logic 0 bit or a logic 1 bit by gates A4 and A14, respectively, before the vehicle address is decoded, and by A5 and A13 after the vehicle address is decoded. All inputs to these gates must be +6 V for their output to be 0 V. The outputs of A4 and A5 are in parallel; therefore, if either A4 or A5 have all inputs +6V, the common output line will be 0 V. The common line between the output of A4 and A5 will be 0 V whenever a logic 0 is decoded. The common line between the output of A14 and A13 will be 0 V whenever a logic 1 is decoded.

The divide-by-5 counter which controls the sub-bit sampling is composed of SB0, SB1, SB2, and A19. The counter functions as a shift register with one unique section; that is, the two level inputs to the first FF SB0. These levels, after the first negative transition of SBSN, will both be +6 V. SB0 will not change states on the second negative transition because both level inputs are +6 V. Figure 8 and table I indicate the states of this counter. The BSN signal is created by ANDing Q of SB2 and $\bar{Q}$ of SB0 with the 1-kc and 2-kc clock outputs of the sub-bit detector. When all of these inputs are +6 V, A26 pin 9 (BSN) will be 0 V.

Errors which may occur in sub-bit decoding: Two types of errors occur in the sub-bit decoder sampling unit. They are both detected by the composite NAND gate A17. This gate indicates an error by its output going to 0 V. This occurs when either inputs 2, 4, 6, or 5, 7, 9 are +6 V. If both sets of inputs have one logic 0 in each set, the output will remain +6 V, indicating no error. One form of error occurs when a bit is decoded and a sampling pulse is not present. This type of error is termed error wrong time (EWT) and is detected by A17 when inputs 2, 4, 6 are +6 V. Pin 6 will be +6 V for all counts of the divide-by-5 counter except sub-bit count 5 when it is 0 V. Pin 2 will be +6 V only when a bit is decoded. Therefore, if a bit decodes when there is no inhibit on pin 6, the output of FF A17 will be 0 V indicating an error which resets the counter and the system. The second form of error occurs when the divide-by-5 counter generates a sample pulse and a bit has not been decoded. This occurs when the inputs 5, 7, 9, to A17 are all +6 V. During the period while no bit is detected, inputs 7 and 9 are +6 V. Pin 5 will be 0 V except during the sample time when it goes to +6 V. During the sample time, if no bit is detected, 7 and 9 will be +6 V and pin 5 will go to +6 V causing the output of A17 to be 0 V, which indicates an error that resets the counter and system. This type of error is known as error bit not correct (EBNC).

An inhibit signal is provided by the divide-by-4 counter at the second negative transition of $\overline{CR}$. This inhibit signal disables the sub-bit error detection system after the information portion of the RTC or data word is shifted into the main-bit register until the system is reset. The second negative transition of $\overline{CR}$ causes A16 pin 3 to be 0 V. This disables the error detection circuits of the sub-bit detector A17 until reset time by making A17 pin 4, 7 equal to 0 V.

Vehicle address decoding.- The detected logic bits are shifted into the decoder register, and at that time, A1 pin 3 makes a negative transition initiated by PG. This gate will be inhibited whenever A29 pin 7 and 10 are both +6 V.

The first 3-detected-bit levels represent the vehicle address. These levels are shifted into the main bit register with transitions of PG. The vehicle address is continuously decoded as the 3 bits are shifted into the register. There are eight NAND gates which decode all eight possible states of these 3 bits. These outputs are A0 through A7. Before the vehicle is launched, it is necessary to hard wire a connection from the output of one of the gates which represents that unique vehicle address to A24 pin 5. As the third bit is shifted into the register, one of the eight gates output level goes to 0 V and stays at 0 V until the fourth bit is shifted into the register. If the wire was placed between the gate whose output goes to 0 V, it will place the 0 V on A24 pin 5. When A24 pin T makes a negative transition, the vehicle address FF is set. This FF will remain set until system reset occurs. The vehicle address FF serves three functions. Before the vehicle address FF is set, the sub-bit decoding is done by A4 and A14 because $\overline{VA}$ is +6 V and VA is 0 V inhibiting A5 and A13. After the vehicle address is decoded, $\overline{VA}$ is 0 V inhibiting A4 and A14, and VA is +6 V enabling A5 and A13. This causes the decoding to be done by A5 and A13. The vehicle address FF, after it is set, "enables" the shift gate for the programable counter A25 pin 5 with VA being +6 V. It also inhibits A34 pin 2.

Gate A34 pin 2 has been repeatedly setting DR23, DR24 which is loading a count-3 code into the programable counter; however, the counter has been inhibited from shifting until the VA FF is set. The last count of the 3-code which was loaded into the bit register will be dumped into the programable counter. When enabled by VA, a count of 3 additional transitions of PG will then load the system address (3 bits) into the register.

Divide-by-4 counter operation.- Before the system address is decoded, the divide-by-4 counter is in the reset state. $\overline{CR}$ makes its first negative transition and the divide-by-4 counter counts 1, loading the system selected into the S register. The states of the divide-by-4 counter are shown in figure 9 and table II.

Decoding sequence for system selection.- The system is decoded by the same eight NAND gates which decoded the vehicle address. These eight gates remain at +6 V until one of them decodes the particular system address. This gate outputs 0 V which is a dc steering level to one of the eight storage FF.

The remaining S FF will have both levels (TS1 and TS2) equal to +6 V. When the divide-by-4 counter counts 1, it generates a negative transition trigger at pin T of all the storage FF's in the register. All the FF's which have both inputs +6 V will not be affected. The FF which has 0 V applied to TS1 and +6 V to TS2 will be set. This causes its output pin Q to be +6 V. The other FF's in the S register will remain clear.

Programable counter operation.- The sequence of loading the programable counter in the main-bit register has been operating continuously from reset time until the vehicle address FF has been set. Before the vehicle address is decoded, $\overline{VA}$ is +6 V; therefore, each time $\overline{PG}$ is +6 V, 10 is 0 V. These negative transitions of 10 set DR23, DR24 in the main-bit register.

The programable counter remains inactive except for parallel loading since the shift pulses are inhibited by VA being 0 V until the vehicle address is decoded. The reset state of the programable counter causes pin 2 of A8 to be 0 V which causes $\overline{CR}$ to be +6 V. Each time 10 is 0 V, CR is +6 V.

The loading of count 3 into the programable counter is achieved when the vehicle address is decoded. This sets DR24, DR23 which is parallel loaded into the counter; however, as it is transferred, it causes PC0 and PC1 to clear and PC2, PC3, PC4, and PC5 to set. This loading is accomplished by CR making a negative transition. The programable counter has been inhibited prior to the vehicle address decoding; however, it will now begin to receive shift pulses since VA is decoded as +6 V. On count 3 of the programable counter, $\overline{CR}$ makes a negative transition which causes the divide-by-4 counter to count 1. This causes A26 pin 3 to make a negative transition which loads the S register. This negative transition will last for 50 usec which causes CR to be +6 V. CR goes to 0 V which is a negative transition. This reloads the programable counter to a reset state for a count determined by the state of DR19 through DR24. See figure 11 and table III for programable operation of count 3 and 6. See figure 12 for the programable counter sequence for the count of 32.

Functions Unique to Each System

RTC word sequence.- The first negative transition of $\overline{CR}$ causes the divide-by-4 counter to count 1 and load the RTC system into the S register. This causes S7 to be set and pin Q is +6 V. This causes the programable counter to be parallel loaded with the count of 6, which shifts the serial information into the main bit register, DR1 through DR6.

It should be noted that $\overline{CR}$ count 1 occurred at the time the system address was decoded and that $\overline{CR}$ count 2 will not occur until the end of 6 more bit times. The 6 additional shift pulses will load the register with the information portion of the RTC word. It can be seen from figure 9 that A29 pin 1 is 0 V from reset time until $\overline{CR}$ makes its second negative transition. This inhibits the RTC relay matrix until the second negative transition of $\overline{CR}$ and will only occur if the RTC system has been selected.

At this time, $\overline{CR}$ of the programable counter makes its second negative transition which causes the divide-by-4 counter to count 2. From figure 7, it can be seen at count 2, A29 pin 7 changes to +6 V and A29 pin 10 has been +6 V since the RTC selection at count 1. This causes A29 pin 9 to be 0 V until system reset, inhibiting any further PG shift pulses from the main-bit register. (Fig. 12.)

The RTC relay selection is achieved by applying ground to one side of the relay coil by causing a transistor switch to saturate; +28 V is applied to a 100-ohm resistor on the other side causing a transistor emitter follower to saturate. The relays are bi-polar latching type, with one coil for setting and another for resetting.

The real-time command is shifted into the main-bit register with the most significant bit entering first. This causes the bits to be arranged with the most significant bit in DR6 and the least significant in DR1. Table IV indicates this relationship of the 6 bits shifted into the register with respect to the octal code which they represent.

After the 6 bits of the RTC command have been shifted into the register, the output of A29 pin 1 goes to +6 V, enabling the emitter follower set, reset, drivers, and selecting the proper relay.

After the 6 information bits have been shifted into the register, $\overline{CR}$ makes its second negative transition and resets the programable counter for a count of 6 by resetting DR19 through DR21 and DR24 and setting DR22 and DR23. This clears the programable counter loading a count of 6. The system is reset by a negative transition of A26 pin 10. For this condition, A21 pin 1, 4, and 6 will be +6 V. At the third negative transition of $\overline{CR}$, the divide-by-4 counter counts 3, and $\overline{PRS1}$ and PRS2 will both be +6 V; therefore, when CR returns to 0 V, the system is reset.

The TLM output functions to supply data concerning the digital section to the TLM transmitter. It uses an 8-line output code which is updated by each EOMR (end of message reset) signal. As the system is resetting, the EOMR makes a negative transition and if TS1 of A15 is 0 V, it will be set or if TS1 of A19 is 0 V, it will be set. EOMR also triggers a 55 msec one shot which will reset the FF's after 55 msec. This leaves the code on the output lines for 55 msec. If the RTC command was set, S3 will be 0 V and since S0 is 0 V, then TS1 of A15 will be 0 V, and TS1 of A19 will be 0 V. This will cause both A15 and A19 to be set by EOMR. The output will be:

Bit no.	1	2	3	4	5	6	7	8
Status	0	+6	0	+6	+6	0	+6	+6

It will remain for 55 msec after the system is reset. It will then be reset to:

Bit no.	1	2	3	4	5	6	7	8
Status	+6	0	+6	0	0	+6	0	0

Computer word sequence.- The computer word sequence is identical to the RTC word for the sub-bit decoding, vehicle address and system selection. The only difference is that the system selected is the AGC system instead of the RTC system.

The first negative transition of $\overline{CR}$ causes the divide-by-4 counter to count 1 and load the AGC system into the S register. This causes the programmable counter to be parallet loaded with the count of 16 which shifts the word in serial form through the main bit register through DR16. At this time, $\overline{CR}$ of the programable counter makes its second negative transition which causes the divide-by-4 counter to count 2. This causes A29 pin 8 to be +6 V. (Fig 13.)

This disables the error detection circuits of the sub-bit detector A17 until reset time by making A17 pin 7, 4 equal to 0 V. Since the RTC system has not been selected, A29 pin 9 will remain at +6 V which permits PG pulses to continue shifting data into the main-bit register through A1 pin 3.

At the time the AGC system is selected the following conditions exist: $\overline{S7}$ remains +6 V, S4 remains 0 V, S0 remains at 0 V, and since S3 was selected it goes from 0 V to +6 V until reset time. Before the second negative transition of $\overline{CR}$, or count 2 of the divide-by-4 counter, EPG pin TS1 was 0 V which qualified BSN to set EPG with its negative transition. After count 2, PRS2 is +6 V which causes EPG pin TS1 to be +6 V which inhibits any further transitions of BSN from setting EPG. EPG will be set after count 2, by the negative transition of $\overline{1\text{-kc}}$ signal, through A13 pin 8. Each time EPG is set, A7 pin 2 goes to +6 V qualifying the 20-kc astable to set PG, the second negative transition of the 20-kc astable clears PG, causing pin Q to make a negative transition, resetting EPG. This causes A7 pin 2 to inhibit PG until EPG is set again. The result of this action is that the computer word is clocked into the bit register at negative transitions of BSN (200-cps rate) and is clocked out of the bit register at negative transitions of $\overline{1\text{-kc}}$ (1-kc rate).

When the programable counter reaches a count of 0, $\overline{CR}$ makes its second negative transition. This causes the programable counter to be parallel loaded to a reset state.

This will require PG to make 16 negative transitions for $\overline{CR}$ to make a third negative transition and reset the system. After the 16 bits are shifted into the register, PG will run at a 1-kc rate. The system will be reset after 16 additional counts of PG at a 1-kc rate. The resetting of the system is accomplished by A21 pin 9 going to +6 V.

If an AGC word was transmitted, S3 will be +6 V and the output of A10 pin 8 is 0 V. This causes A10 pin 9 and pin 1 to apply +6 V to TS1 of A15 and TS1 of A19. After the computer word is accepted, A10 pin 5 goes to 0 V. At the end of message time, EOMR makes a negative transition which sets A15, A19. This outputs the following code:

Bit no.	1	2	3	4	5	6	7	8
Status	0	+6	0	+6	+6	0	+6	+6

After 55 msec it will be reset, outputting:

Bit no.	1	2	3	4	5	6	7	8
Status	+6	0	+6	0	0	+6	0	0

If the AGC data accept signal is not actuated, TS1 of A15, A19 will be +6 V, and the FF will remain reset at EOMR time with the code being as follows:

Bit no.	1	2	3	4	5	6	7	8
Status	+6	0	+6	0	0	+6	0	0

CTE word sequence.- The CTE word sequence is identical to the RTC word sequence for the sub-bit decoding, vehicle address, and system selection. The only difference is the system selected is the CTE system instead of the RTC system.

The first negative transition of $\overline{CR}$ causes the divide-by-4 counter to count 1 and loads the decoded CTE system address into the S register. This action causes PRS 1 to be +6 V and also S4 to be +6 V. This enables A11 pin 6 so that as PG returns to +6 V, the CTE system is reset. The CTE system will continue being reset with PG, making positive transitions, until $\overline{CR}$ makes a third negative transition causing PRS 1 to be 0 V, inhibiting this resetting function of A21 pin 9. Then the system will not be reset at the third negative transition of $\overline{CR}$. The loading of the CTE system also causes the programable counter to be parallel loaded with the count of 24 which shifts the information portion of the word into the main-bit register. This is accomplished by setting DR20, DR21 which will be transferred in parallel to the programable counter. This clears PC3, PC4 and sets PC0, PC1, PC2, PC5 which loads the count of 24. After 24 additional pulses of PG have been counted by the programable counter, $\overline{CR}$ makes its second negative transition. This causes the divide-by-4 counter to count 2.

The generation of PG pulses is controlled by S4 and PRS2. Before $\overline{CR}$ makes a second negative transition, PRS2 is 0 V which places 0 V on A8 RC. This qualifies EPG FF to be reset by Q of the PG FF making a negative transition. Before $\overline{CR}$ counts 2, the following voltages exist: S4 = +6 V, S7 = +6 V, PRS 2 = 0 V, S3 = 0 V, S0 = 0 V. This applies to the following levels of EPG: TS1 = 0 V, S = 0 V, RC = 0 V.

Each negative transition of BSN sets EPG which enables A7 pin 2. The first negative transition of the 20-kc astable sets PG. The second transition of the 20-kc astable clears PG which causes a negative transition at pin R of EPG, thereby clearing EPG. This inhibits A7 and no further 20-kc pulses will activate the PG FF until the next negative transition of BSN which sets EPG and repeats this sequence. After count 2 of $\overline{CR}$, PRS 2 is +6 V which will apply the following levels to FF EPG: RC = +6 V, TS1 = +6 V, S = 0 V. This causes EPG FF to be disqualified for setting by BSN and also disqualifies EPG for resetting by negative transitions at pin R. Since EPG cannot be reset, it will remain in the set state and Q will be +6 V. This leaves A7 enabled and PG FF will continue counting the 20-kc astable. This causes PG to have a 1/10-kc period rather than a 1/200-cps period.

At count 2 of the divide-by-4 counter, PRS2 goes to +6 V. This causes the output of A7 pin 9 to be +6 V. This enables A7 pin 5; therefore, when $\overline{CR}$ goes to 0 V, A7 pin 8 will make a negative transition setting the RA FF and loading the contents of the main bit register, DR19 through DR24, into the programable counter. The programable counter is parallel loaded with the count of 6 by setting DR22, DR23, and clearing DR19, DR20, DR21, and DR24. When the RA FF is set, $\overline{RA}$ goes to 0 V; this inhibits PG pulses from shifting data into the main bit register. Also, the RA FF enables the seconds line to the CTE equipment so that as PG pulses are counted by the programable counter, there will be an output on the seconds line to the CTE. This is accomplished by TD1, TD2 FF's being in the reset state and FF RA pin Q = 0 V. When the programable counter reaches its programed count, $\overline{CR}$ makes its third negative transition. This clears the RA FF which loads the count of 6 into the programable counter. $\overline{RA}$ goes to +6 V which enables the PG shift pulses to shift data in the main-bit register. Also, as RA FF is cleared, pin Q makes a negative transition giving count 1 to the TD1, TD2 shift register. Then $\overline{Q}$ of the RA FF goes to +6 V which inhibits any pulses to the CTE equipment. (Fig. 14.)

As the programable counter counts to 0, the second group of 6 information bits are shifted into the main-bit register, DR19 through DR24. At the count of 0, $\overline{CR}$ makes its fourth negative transition which sets the RA FF. Then RA FF is set and $\overline{RA}$ goes to 0 V which inhibits shifting data in the main-bit register. Then $\overline{Q}$ goes to 0 V which enables the minutes output line to the CTE equipment. It also parallel loads the second 6 information bits into the programable counter.

As the programable counter counts the PG pulses, they are output to the CTE on the minutes line. When the programable counter reaches its programed count, $\overline{CR}$ makes its fifth negative transition which clears the RA FF. As RA FF is cleared, the output to the CTE is inhibited and the shift pulses to the main-bit register are enabled. Then the count of 6 is loaded into the programable counter and TD1, TD2 receives the second count. The counter counts PG pulses until count 0 when $\overline{CR}$ makes its sixth negative transition which sets the RA FF. The RA FF is set and $\overline{RA}$ goes to 0 V which inhibits shifting data in the main-bit register. The $\overline{Q}$ of the RA FF goes to 0 V and enables the hours output line to the CTE equipment. It also parallel loads the third 6-bit information bits into the programable counter.

As the programable counter counts the PG pulses, they are output to the CTE on the hours line. When the programable counter reaches its 0 count, $\overline{CR}$ makes its seventh negative transition which clears the RA FF. As the RA FF clears, the output to the CTE is inhibited, the shift pulses to the main-bit register are enabled. The count of 6 is loaded into the programable counter and TD1, TD2 receive the third negative transition count. The counter counts PG pulses until count 0, when $\overline{CR}$ makes its eighth negative transition which sets the RA FF. The RA FF is set and $\overline{RA}$ goes to 0 V which inhibits shifting data into the main-bit register and $\overline{Q}$ goes to 0 V which enables the days output line to the CTE. It also parallel loads the fourth group of 6 information bits into the programable counter. As the programable counter counts the PG pulses, they are output on the CTE on the days line. When the programable counter reaches its programed count, $\overline{CR}$ makes its seventh negative transition which

clears the RA FF. As the RA FF clears, the output to the CTE is inhibited, and the shift pulses to the main bit register are enabled. The count of 6 is loaded into the programable counter and TD1, TD2 receive the fourth negative transition count. As TD1, TD2 receive the fourth negative transition count, TD1 and TD2 both become +6 V. This qualifies A21 pin 9 to reset the system when R3 makes a negative transition.

When CR returns to 0 V, A24 pin 3 goes to +6 V and A29 pin 8 goes to 0 V which is R3. This resets the system.

TM word sequence.- The TM word sequence is identical to the RTC word sequence for the sub-bit decoding, vehicle address, and system selection. The only difference is the system selected is the TM system instead of the RTC system.

The first negative transition of $\overline{CR}$ causes the divide-by-4 counter to count 1 and load the S register by setting S0. This causes $\overline{S0}$ to be 0 V which sets DR20, DR21, loading the count of 24 into the programable counter. As CR makes a negative transition, this count is parallel loaded into the programable counter. As the counter counts to 0, the PG pulses are shifting the 24 information bits into the main register.

Before the 24th pulse is counted, the PG pulses are generated as follows: S0 = 0 V, PRS2 = 0 V, $\overline{S7}$ = +6 V, S4 = 0 V. This places the following levels on EPG FF: RC = 0 V, TS1 = 0 V, S = 0 V. If PG and EPG FF's are clear, BSN makes a negative transition which sets EPG FF making pin Q +6 V. This enables A7 NAND gate which places 0 V on TS1 of PG. This qualifies PG FF to be set by the next negative transition of the 20-kc astable. The PG FF is set which causes Q to be +6 V and $\overline{Q}$ to be 0 V. This applies 0 V to TS1 and +6 V to TS2. The second negative transition of the 20-kc astable FF clears the PG FF which causes pin Q to make a negative transition which resets the EPG FF by pin R making a negative transition. Then EPG will remain reset until the next negative transition of BSN.

After the 24 information bits are shifted into the main-bit register, and at the count of 0, $\overline{CR}$ makes its second negative transition which causes the divide-by-4 counter to count 2. This causes PRS2 to become +6 V and since the TM system was selected, S0 will be +6 V. This causes the PG pulses to be generated by the $\overline{1\text{-kc}}$ negative transitions. At the second negative transition of CR, the following levels will be established at the EPG FF: TS1 will be +6 V, RC = 0 V, S = 1 kc.

If both EPG and PG are cleared, the first negative transition of the 1 kc sets EPG FF. This causes pin Q to be +6 V which enables A7 NAND gate. The first negative transition of the 20-kc astable will set PG FF. This applies 0 V to TS1 and +6 V to TS2. This second negative transition of the 20-kc astable clears the PG FF causing pin Q of PG to make a negative transition. This will reset EPG because RC is 0 V. Since EPG FF is cleared, A7 will remain disabled until EPG is set by the next negative transition of the 1-kc timing. This causes PG pulses to be dependent upon the negative transition of $\overline{1\text{-kc}}$ timing after the second negative transition of $\overline{CR}$.

The second negative transition of $\overline{CR}$ dumps the first 6 bits of the 24 information bits into the programable counter which were shifted into DR19 through DR24. As the programable counter counts to the programed count, the remaining 18 information bits are shifted through DR19 to DR24.

When the count is reached, $\overline{CR}$ makes its third negative transition; this causes A21 to produce an EOMR signal which resets the system.

As the system is reset, the contents of DR24 and $\overline{DR24}$ are loaded into the TLM output storage FF A and B.

At the EOMR time, if DR24 is set, the TLM output will be:

Bit no.	1	2	3	4	5	6	7	8	
Status	+6	0	+6	+6	+6	0	0	0	(test message A)

At the EOMR time, if DR24 is clear, the TLM output will be:

Bit no.	1	2	3	4	5	6	7	8	
Status	0	+6	0	0	0	+6	0	0	(test message B)

After 55 msec, the 1 shot will reset the TLM A and B FF's and the output code will be:

Bit no.	1	2	3	4	5	6	7	8	
Status	+6	0	+6	0	0	+6	0	0	(standby condition)

These messages will remain at the TLM output for 55 msec until pin Q resets A15, A19. This is a verification that the sub-bit register, main-bit register, vehicle decoding, and system decoding system are operational.

SUMMARY OF FUNCTIONS USED IN DECODER

From the analysis, the following characteristics of word format can be established:

RTC Command

Vehicle address	System address	Information section
1 2 3	4 5 6	7 8 9 10 11 12

The vehicle address is shifted with BSN, a 200-cps signal requiring 15 msec. The system address is shifted with BSN and requires 15 msec. The RTC information is shifted with BSN, a 200-cps signal requiring 30 msec. The RTC command actuation signal is present for 6 counts of the PG in the programable counter which occurs at 200 cps. Total time required is 90 msec. At the end of this time, the system is reset. (Fig. 15.)

AGC Command

Vehicle address	System address	Information section
1 2 3	4 5 6	7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

The vehicle address is shifted at negative transitions of BSN, a 200-cps signal, time required is 15 msec. The system address is shifted at negative transitions of BSN, a 200-cps signal, time required is 15 msec. The information section (16 bits) is shifted into the main-bit register at negative transitions of BSN, a 200-cps signal, time required is 80 msec. The information section (16 bits) is shifted into the computer with 16 PG pulses at negative transitions of the $\overline{1\text{-kc}}$ timing requiring 16 msec. Total time required is 126 msec.

CTE Command

Vehicle address	System address	Seconds information
1 2 3	4 5 6	7 8 9 10 11 12

Minutes information	Hours information
13 14 15 16 17 18	19 20 21 22 23 24

Days information

25 26 27 28 29 30

The vehicle address is shifted at negative transitions of BSN, a 200-cps signal requiring 15 msec. The system address is shifted at negative transitions of BSN, a 200-cps signal requiring 15 msec. The 24 data bits are shifted at negative transitions of BSN, a 200-cps signal requiring 120 msec.

The first 6 information bits, seconds, are parallel loaded into the programable counter. The counter runs with negative transition of PG which is occurring at a 10-kc rate. The length of time required will be (number programed) 10^{-1} msec. A count of 6 will be programed into the counter and loaded by the 10-kc PG pulses. This will require 0.6 msec.

The second 6 information bits, minutes, are parallel loaded into the programable counter. These PG pulses also occur at a 10-kc rate. The length of time required will be (number programed) 10^{-1} msec. A count of 6 will be programed into the counter and the 10-kc PG pulses will be loaded. This requires 0.6 msec.

The third 6 information bits, hours, are parallel loaded into the programable counter. These PG pulses occur at a 10-kc rate. The length of time

required will be (number programed) 10^{-1} msec. A count of 6 will be programed into the counter and the 10-kc PG pulses will be counted. This requires 0.6 msec.

The fourth set of 6 information bits, days, are parallel loaded into the programable counter. These PG pulses occur at a 10-kc rate. The length of time required will be (number programed) 10^{-1} msec. At the end of this time, the system will be reset. As each set of PG pulses was counted, the second, minute, hours, and days PG pulses were output on the appropriate lines to the CTE.

The total time required for the CTE command is 169 msec maximum.

Bits 7, 8, 9, 10, 11, and 12 determine the number of pulses output on the seconds line. They will be parallel word loaded into the programable counter.

Bit no.	7	8	9	10	11	12
Count no.	1	2	4	8	16	32

The same sequence applies to minutes, hours, and days outputs. A maximum count of 63 pulses is available if all FF's are set.

TM Command

Vehicle address System address Scan information

1 2 3 4 5 6 7 8 9 10 11 12

Information to be scanned

13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30

The vehicle address is shifted at negative transitions of BSN, a 200-cps signal requiring 15 msec. The system address is shifted at negative transitions of BSN, a 200-cps signal requiring 15 msec. The 24 data bits are shifted at negative transitions of BSN, a 200-cps signal requiring 120 msec.

The first 6 information bits are loaded into the programable counter. The CO counter counts PG pulses occurring at a 1-kc rate. The time required is the programed count msec. At the end of the count, the system is reset and the contents of 1 of the remaining 18 information bits will be dumped from DR24 and $\overline{\text{DR24}}$ FF. The bit selected depends on the number of shifted pulses programed in the first 6 information bits. The TLM will output a unique load for a set or reset condition of DR24. The total time required for the TM command is 174 msec, maximum.

Bits 7, 8, 9, 10, 11, and 12 determine a parallel code which is loaded into the programable counter and determine which of the following information

bits will be shifted into DR24 at reset time:

Bit no.	7	8	9	10	11	12
Count no.	1	2	4	8	16	32

The set condition of +6 V at pin Q is a logic one. A possible count of 63 is available if all FF are set. At the EOMR time, if DR24 is set, TLM output will be:

Bit no.	1	2	3	4	5	6	7	8
Status	+6	0	+6	+6	+6	0	0	0

If DR24 is clear, TLM output will be:

Bit no.	1	2	3	4	5	6	7	8
Status	0	+6	0	0	0	+6	0	0

APPENDIX

APOLLO DIGITAL UP-DATA LINK

Pertinent Data

1. Nomenclature: Up-Data Link, digital (UDL)
2. Components: Receiver, detector, decoder
3. Subcontractor: Motorola, Inc.
4. Chief Engineer: Ken Porter, Motorola, Inc.
5. NAA Project Engineer: Gary Covington, NAA
6. NASA-IESD Lead Project Engineer (C&SM): E. L. Chicoine
7. NASA-IESD Project Engineer: S. D. Lenett
8. UDL frequency range: 406 to 450 Mc
9. UDL size: 13.00 inches by 9.38 inches by 4.41 inches
10. UDL weight: approximately 20 lbs
11. UDL power required:

receiver	-18 V dc at 60 ma
	- 6 V dc at 5 ma
detector-decoder	+ 6 V dc at 385 ma
	- 6 V dc at 50 ma
	+28 V dc at 53 ma

12. Receiver sensitivity: -129 dBw
13. Receiver type: double conversion - superheterodyne
14. Modulation method: PSK/FM
15. Local oscillator frequency: tuned from 83 to 92 Mc
16. Second IF frequency: 10.7 Mc
17. S/N ratio (UHF input): 10 dB in a 70 kc Bw
18. S/N ratio (ext. audio input): 8.6 dB in a 3.5 kc audio Bw
19. Discrete command capability: 64 commands

20. Command word lengths: RTC - 12 bits
AGC data word - 24 bits
Max. word length - 30 bits

21. Modulating frequencies: Data 2 kc tone
Sync 1 kc tone

22. UDL interfaces: AGC
Telemetry
UHF/off/S-band switch (located on communication control panel)
RTC relays
Central timing equipment (CTE)
Block/accept switch (located on computer control panel)

REFERENCES

Digital Command Monitor (52E190019) Technical Specification and Description of, Contract No. Y-20223-R, Project No. 2774-23
Motorola, Inc.
Military Electronics Division
Western Center
Scottsdale, Arizona

DCS Test Set (52E190020) Technical Specification and Description of, Contract No. Y-20223-R, Project No. 2774-23
Motorola, Inc.
Military Electronics Division
Western Center
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DCS Module (Sandwich) Test Adaptor (52E190023), Technical Specification and Description of. Contract No. Y-20223-R. Project No. 2774-23
Motorola, Inc.
Western Center
Military Electronics Division
Scottsdale, Arizona

DCS Test Set Tape Control (52E190025), Technical Manual Operation and Maintenance Instructions
Motorola, Inc.
Military Electronics Division
Scottsdale, Arizona

Apollo Up-Data Link Design Review - February 1964
Motorola, Inc.
Military Electronics Division
Scottsdale, Arizona

TABLE I.- TRUTH TABLE FOR GENERATING BSN

SBSN	SB0		SB1		SB2		A19
	Q	$\overline{Q}$	Q	$\overline{Q}$	Q	$\overline{Q}$	Pin 10
Reset	0	+6	0	+6	0	+6	0
1	+6	0	0	+6	0	+6	+6
2	+6	0	+6	0	0	+6	+6
3	0	+6	+6	0	+6	0	+6
4	0	+6	0	+6	+6	0	+6
5	0	+6	0	+6	0	+6	0

TABLE II.- TRUTH TABLE FOR RTC COMMAND (DIVIDE-BY-4 COUNTER)

$\overline{CR}$	A25 PRS1		A30 PRS2		A29	A26	A29	A29
	Q	$\overline{Q}$	Q	$\overline{Q}$	Pin 7	Pin 3	Pin 9	Pin 1
Reset	0	+6	0	+6	0	+6	+6	0
1	+6	0	0	+6	0	0	+6	0
2	+6	0	+6	0	+6	0	0	+6
3	0	+6	+6	0	+6	+6	0	+6
4	0	+6	+6	0	+6	+6	0	+6
5	0	+6	+6	0	+6	+6	0	+6

TABLE III.- TRUTH TABLE FOR COUNT 3 LOAD SYSTEM AND COUNT 6 LOAD SYSTEM

Count 6 Load System

	PC 0				PC 1				PC 2				PC 3				PC 4				PC 5			
	TS1	TS2	Q	$\bar{Q}$	TS1	TS2	Q	$\bar{Q}$	TS1	TS2	Q	$\bar{Q}$	TS1	TS2	Q	$\bar{Q}$	TS1	TS2	Q	$\bar{Q}$	TS1	TS2	Q	$\bar{Q}$
Reset	+6	0	+6	0	0	+6	0	+6	+6	+6	0	+6	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0
1	0	+6	0	+6	+6	+6	+6	0	+6	+6	0	+6	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0
2	+6	0	+6	0	+6	0	+6	0	0	+6	0	+6	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0
3	0	+6	0	+6	+6	+6	0	+6	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0
4	+6	0	+6	0	0	+6	0	+6	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0
5	0	+6	0	+6	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0
6	+6	0	+6	0	+6	0	+6	0	+6	0	+6	0	+6	0	+6	0	+6	0	+6	0	0	+6	+6	0

Count 3 Load System

	PC 0				PC 1				PC 2				PC 3				PC 4				PC 5			
	TS1	TS2	Q	$\bar{Q}$	TS1	TS2	Q	$\bar{Q}$	TS1	TS2	Q	$\bar{Q}$	TS1	TS2	Q	$\bar{Q}$	TS1	TS2	Q	$\bar{Q}$	TS1	TS2	Q	$\bar{Q}$
Reset	0	+6	0	+6	+6	+6	0	+6	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0
1	+6	0	+6	0	0	+6	0	+6	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0
2	0	+6	0	+6	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0	+6	+6	+6	0
3	+6	0	+6	0	+6	0	+6	0	+6	0	+6	0	+6	0	+6	0	+6	0	+6	0	0	+6	+6	0

TABLE IV.- DECODING SEQUENCE CHART FOR UDL

[Real Time Commands as They Appear in the Register DR1 - DR6]

Octal number for decoding	Binary digits as they are in register					
	8^0 Octal			8^1 Octal		
	DR1 2^0	DR2 2^1	DR3 2^2	DR4 2^0	DR5 2^1	DR6 2^2
0	0	0	0	0	0	0
01	1	0	0	0	0	0
02	0	1	0	0	0	0
03	1	1	0	0	0	0
04	0	0	1	0	0	0
05	1	0	1	0	0	0
06	0	1	1	0	0	0
07	1	1	1	0	0	0
10	0	0	0	1	0	0
11	1	0	0	1	0	0
12	0	1	0	1	0	0
13	1	1	0	1	0	0
14	0	0	1	1	0	0
15	1	0	1	1	0	0
16	0	1	1	1	0	0
17	1	1	1	1	0	0
20	0	0	0	0	1	0
21	1	0	0	0	1	0
22	0	1	0	0	1	0
23	1	1	0	0	1	0
24	0	0	1	0	1	0
25	1	0	1	0	1	0
26	0	1	1	0	1	0
27	1	1	1	0	1	0
30	0	0	0	1	1	0
31	1	0	0	1	1	0

TABLE IV.- DECODING SEQUENCE CHART FOR UDL - Continued

Octal number for decoding	Binary digits as they are in register					
	8^0 Octal			8^1 Octal		
	DR1 2^0	DR2 2^1	DR3 2^2	DR4 2^0	DR5 2^1	DR6 2^2
32	0	1	0	1	1	0
33	1	1	0	1	1	0
34	0	0	1	1	1	0
35	1	0	1	1	1	0
36	0	1	1	1	1	0
37	1	1	1	1	1	0
40	0	0	0	0	0	1
41	1	0	0	0	0	1
42	0	1	0	0	0	1
43	1	1	0	0	0	1
44	0	0	1	0	0	1
45	1	0	1	0	0	1
46	0	1	1	0	0	1
47	1	1	1	0	0	1
50	0	0	0	1	0	1
51	1	0	0	1	0	1
52	0	1	0	1	0	1
53	1	1	0	1	0	1
54	0	0	1	1	0	1
55	1	0	1	1	0	1
56	0	1	1	1	0	1
57	1	1	1	1	0	1
60	0	0	0	0	1	1
61	1	0	0	0	1	1
62	0	1	0	0	1	1
63	1	1	0	0	1	1
64	0	0	1	0	1	1
65	1	0	1	0	1	1

TABLE IV.- DECODING SEQUENCE CHART FOR UDL - Concluded

Octal number for decoding	Binary digits as they are in register					
	8^0 Octal			8^1 Octal		
	DR1 2^0	DR2 2^1	DR3 2^2	DR4 2^0	DR5 2^1	DR6 2^2
66	0	1	1	0	1	1
67	1	1	1	0	1	1
70	0	0	0	1	1	1
71	1	0	0	1	1	1
72	0	1	0	1	1	1
73	1	1	0	1	1	1
74	0	0	1	1	1	1
75	1	0	1	1	1	1
76	0	1	1	1	1	1
77	1	1	1	1	1	1

Logic 1 = Q = +6 V
Logic 0 = Q = 0 V

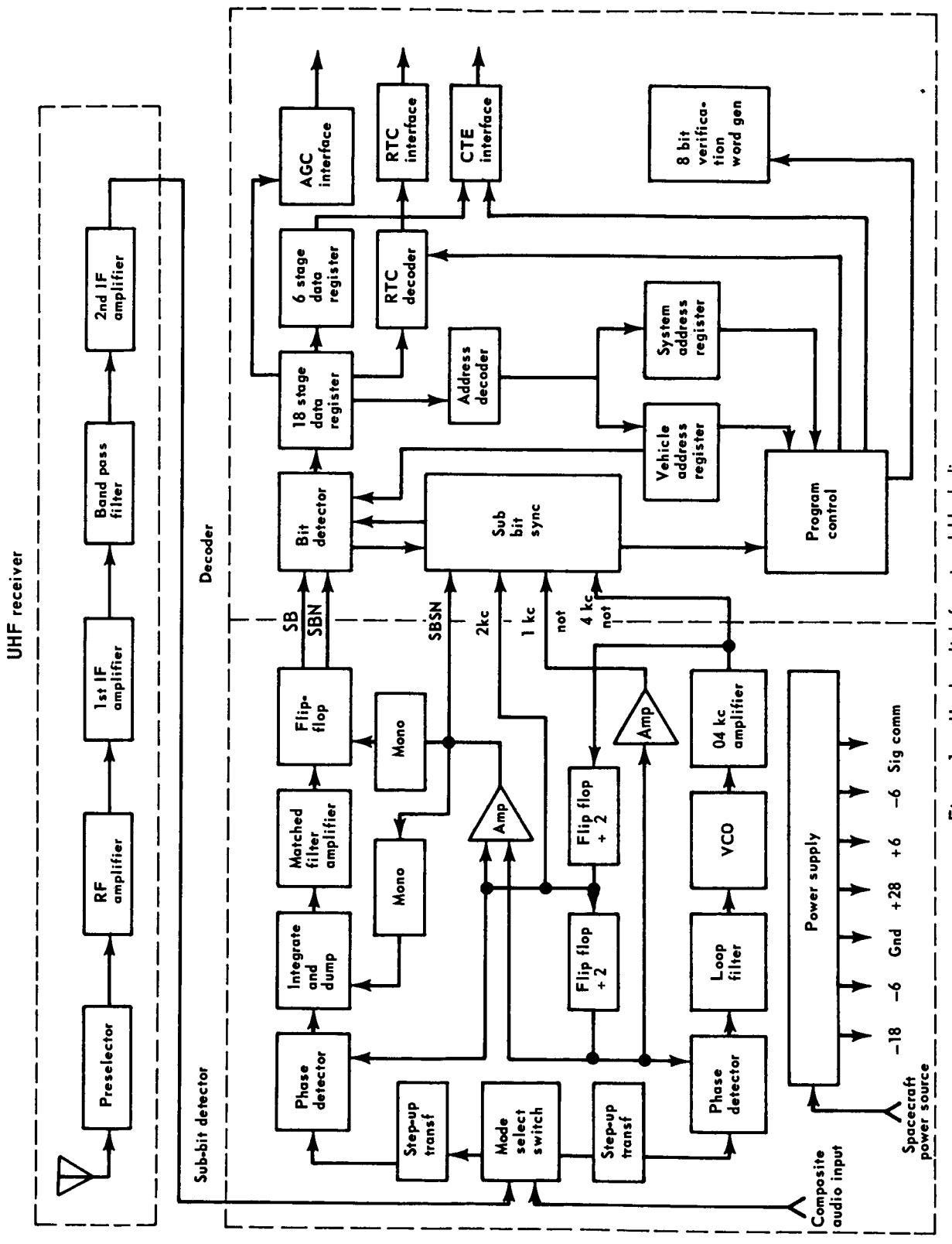
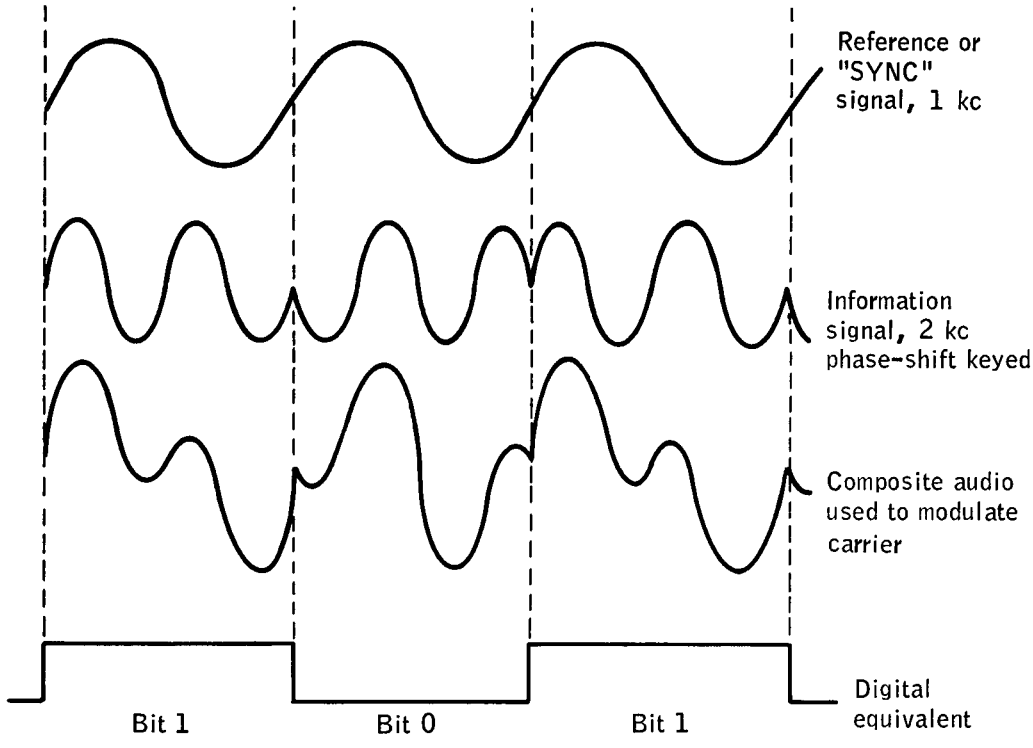


Figure 1. - Up-data link functional block diagram



Notes:

1. Information bit 1 = 1 kc in phase with 2 kc.
2. Information bit 0 = 1 kc 180° out of phase with 2 kc.
3. Message structure: 30 information bits maximum (150 sub bits).

Figure 2. - Composite audio signal

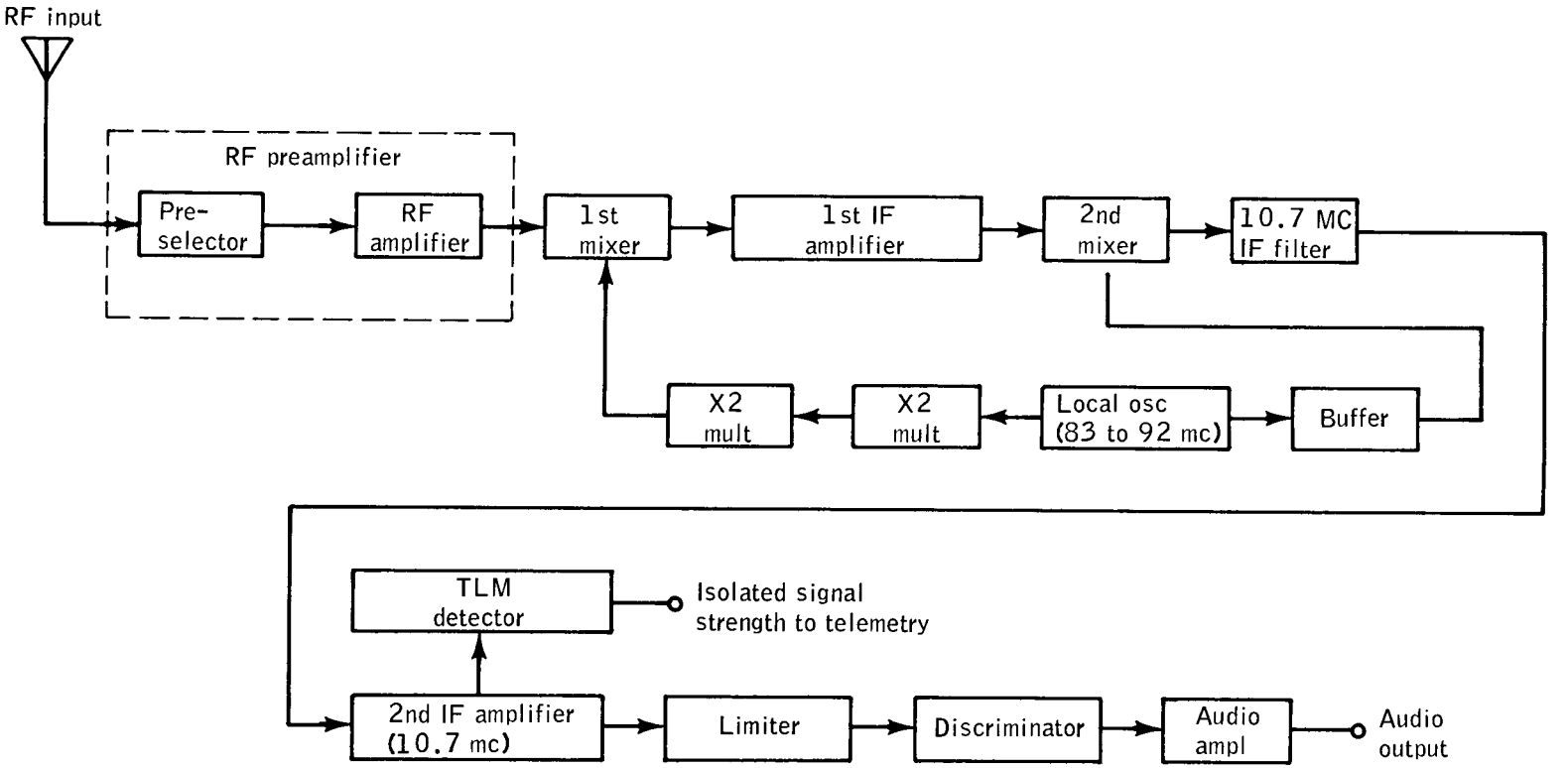


Figure 3. - UHF receiver, block diagram

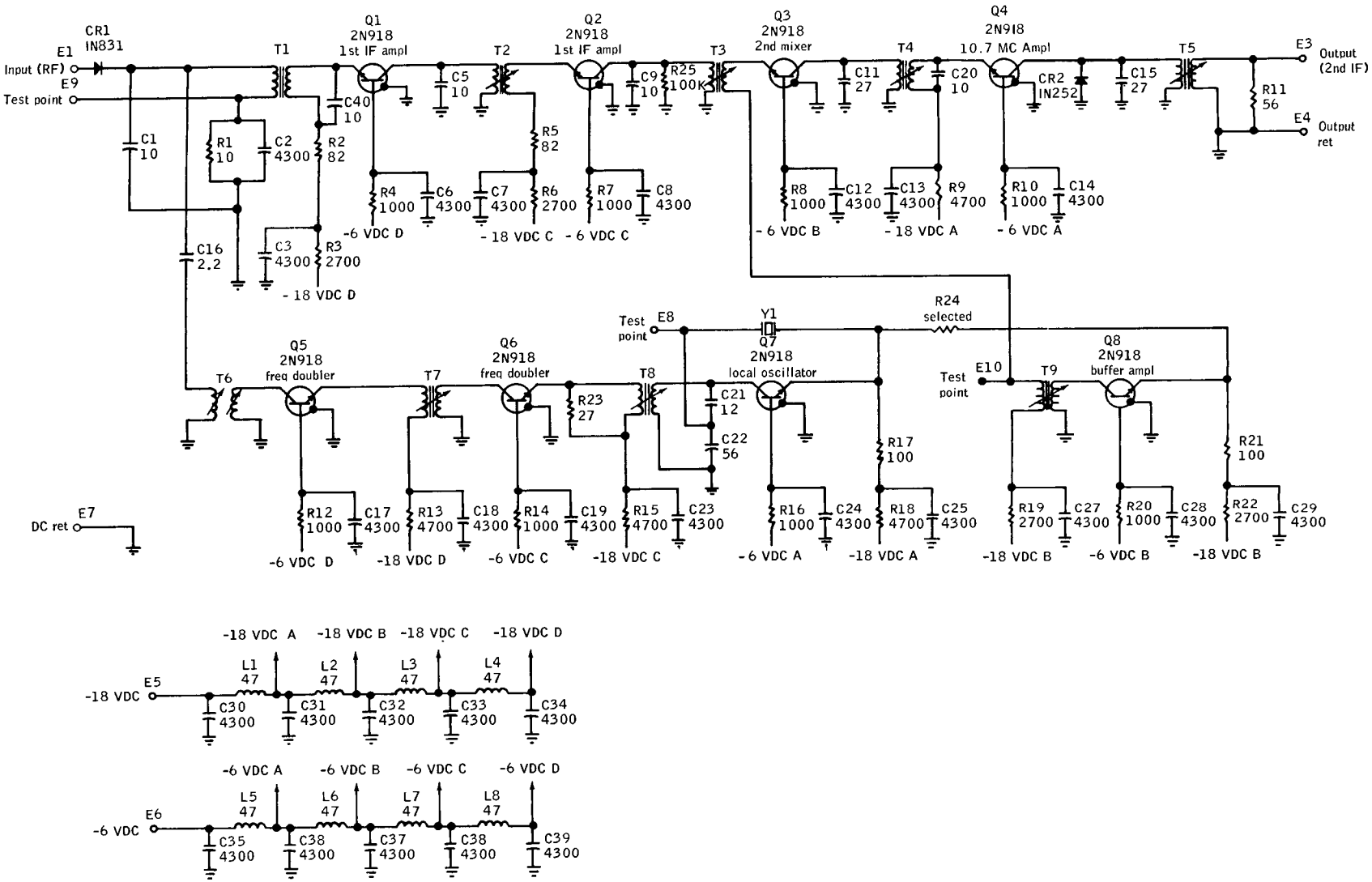


Figure 4. - UHF receiver, first IF amplifier, local oscillator, schematic diagram

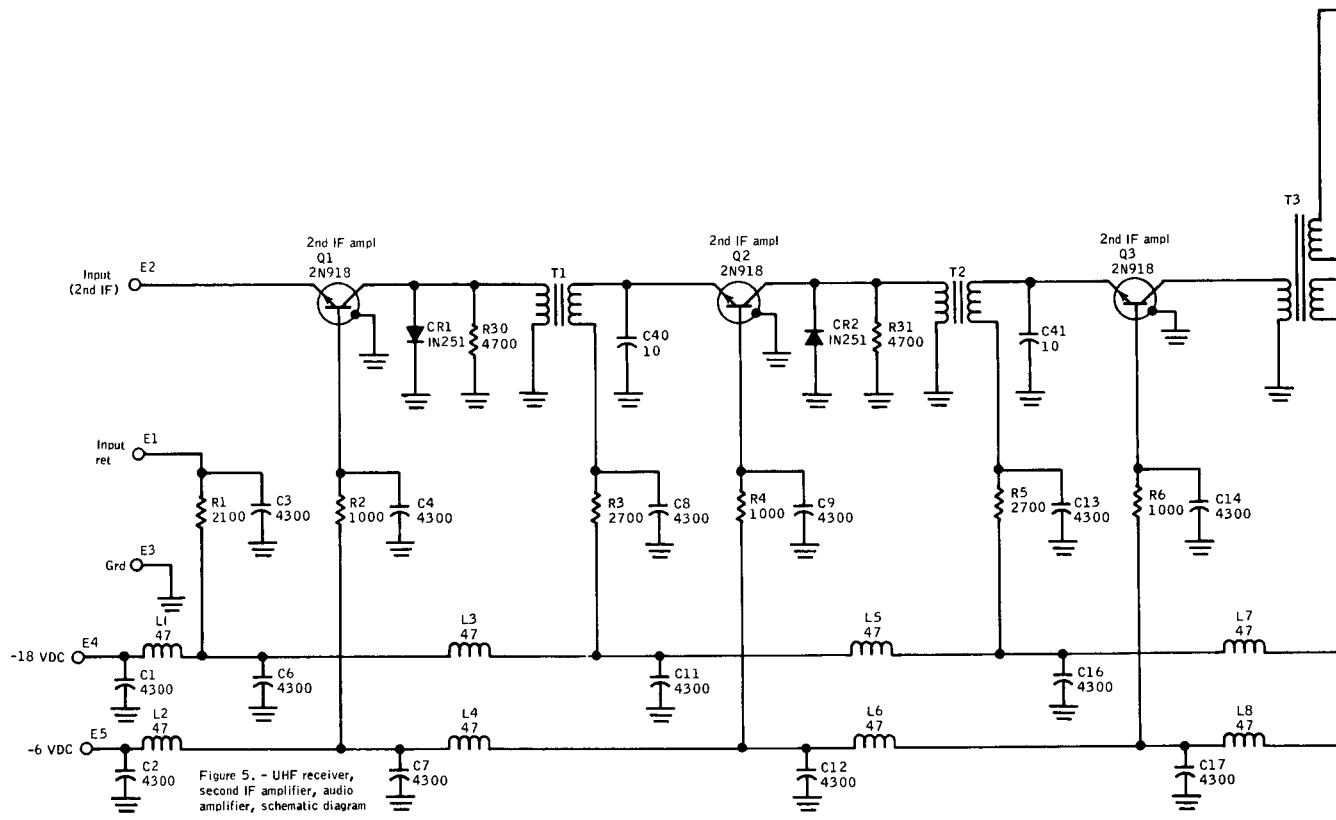
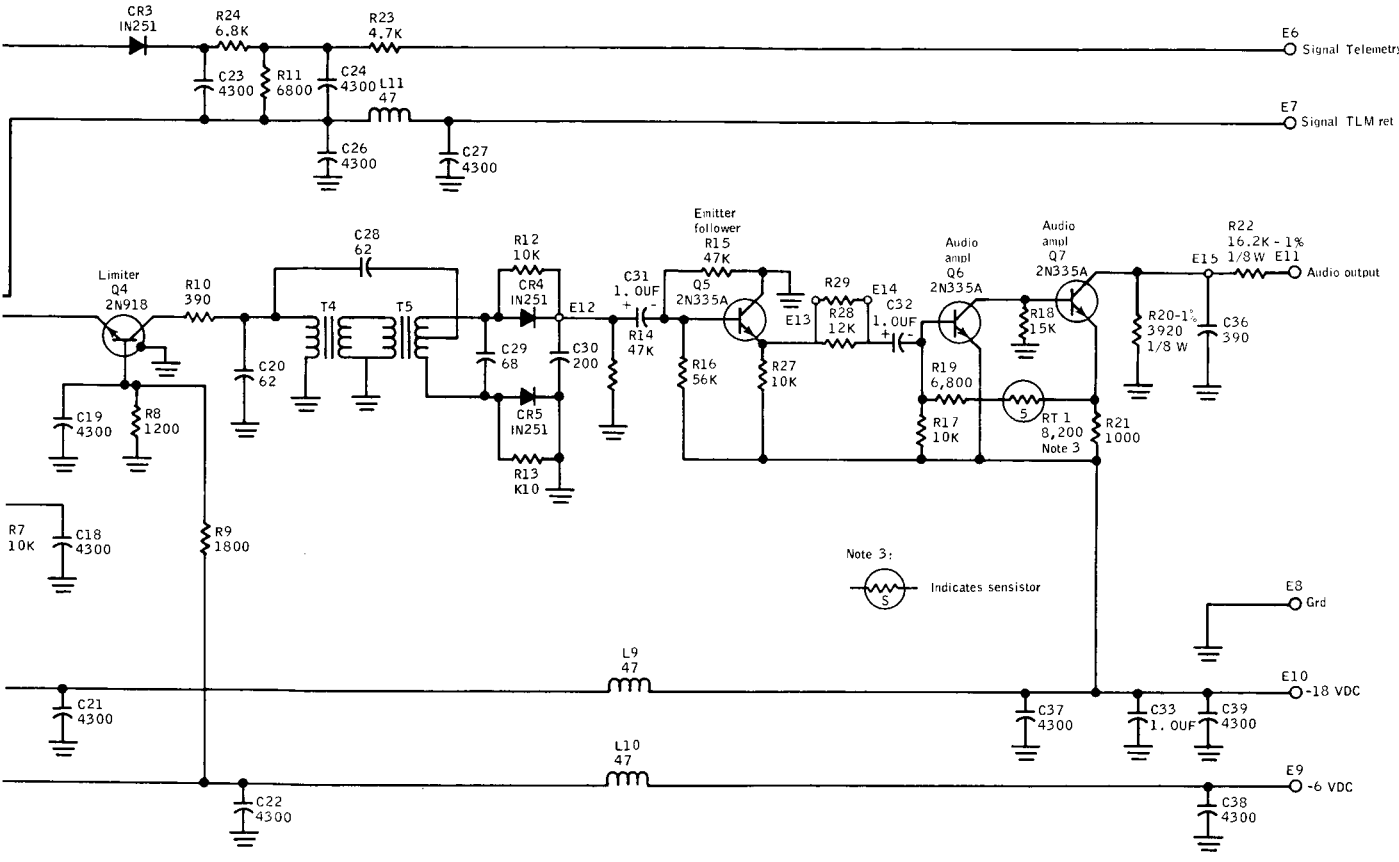


Figure 5. - UHF receiver, second IF amplifier, audio amplifier, schematic diagram


CR3
IN251
R24
6.8K
R23
4.7K
E6
Signal Telemetry
C23
4300
R11
6800
C24
4300
L11
47
E7
Signal TLM ret
C26
4300
C27
4300
C28
62
R12
10K
Emitter
follower
R15
47K
Audio
ampl
Q6
2N335A
Audio
ampl
Q7
2N335A
R22
16.2K - 1%
E15
1/8W
E11
Audio output
Limiter
Q4
2N918
R10
390
T4
T5
CR4
IN251
E12
C31
1. 0UF
Q5
2N335A
R29
E14
C32
1. 0UF
R18
15K
R20-1%
3920
1/8 W
C36
390
E13
R28
12K
C19
4300
R8
1200
C20
62
C29
68
C30
200
R14
47K
R16
56K
R27
10K
R19
6,800
R17
10K
RT 1
8,200
Note 3
R21
1000
CR5
IN251
R13
K10
R7
10K
C18
4300
R9
1800
Note 3:
Indicates sensistor
E8
Grd
L9
47
E10
-18 VDC
C21
4300
C37
4300
C33
1. OUF
C39
4300
L10
47
E9
-6 VDC
C22
4300
C38
4300

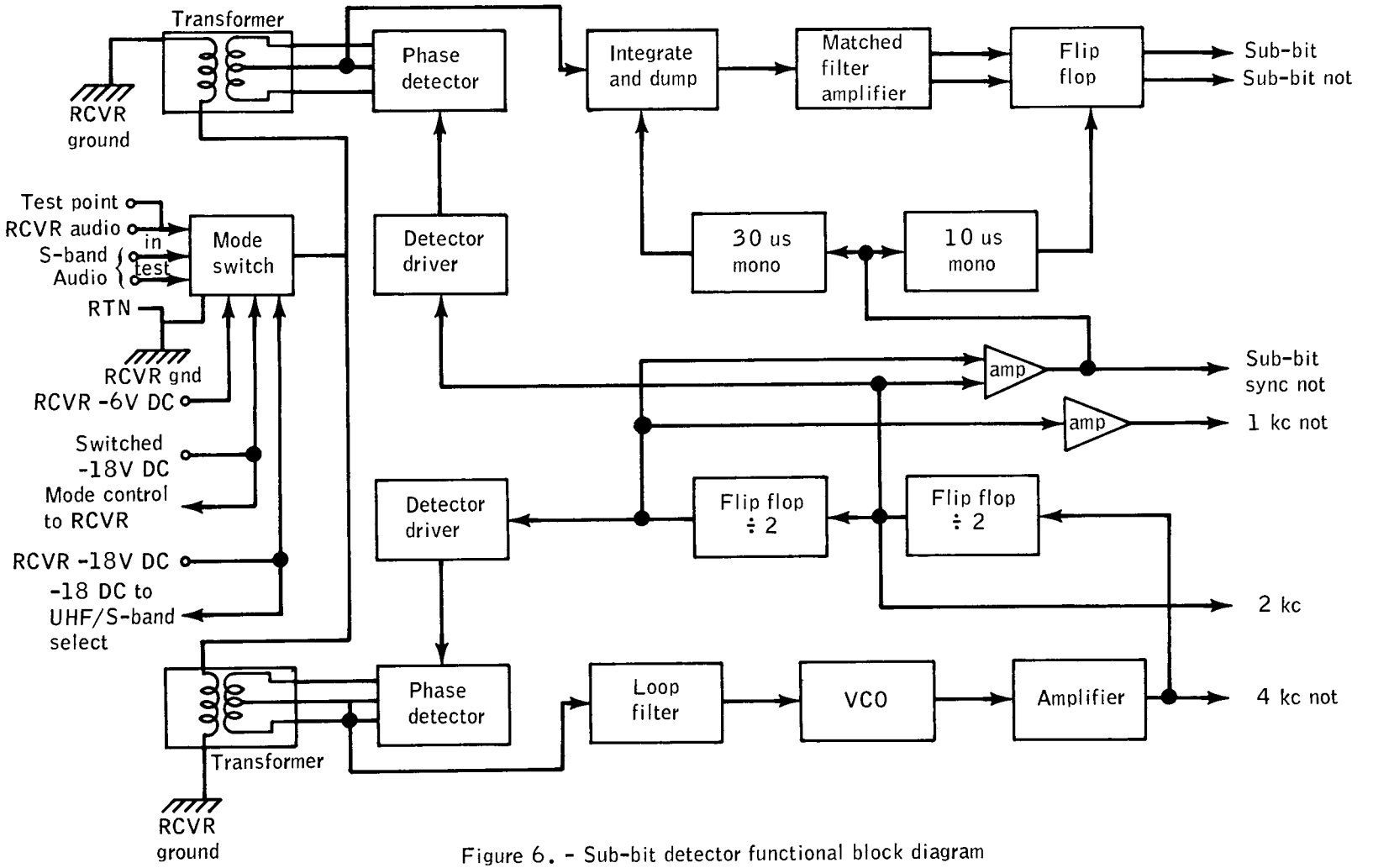


Figure 6. - Sub-bit detector functional block diagram

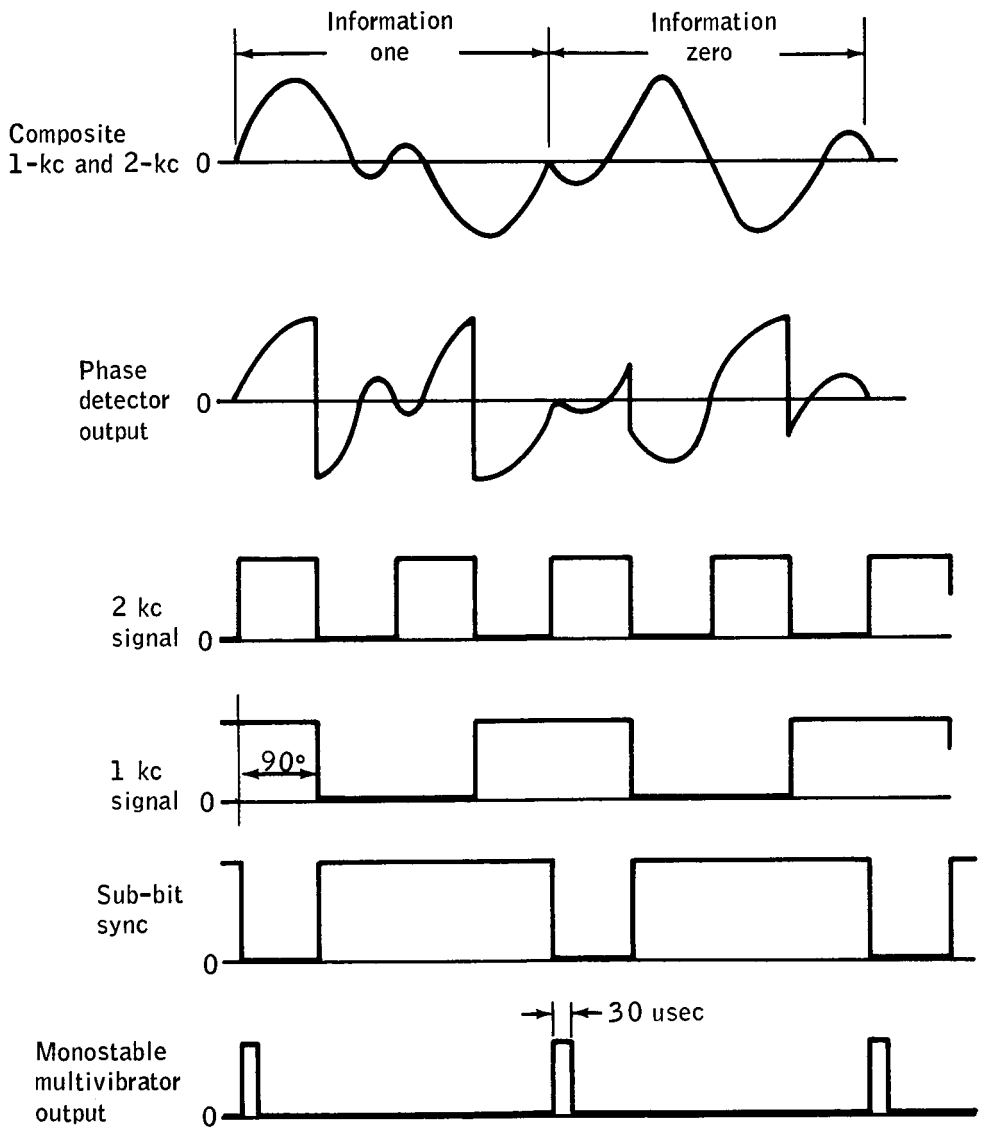


Figure 7. - Synchronization channel, typical waveforms

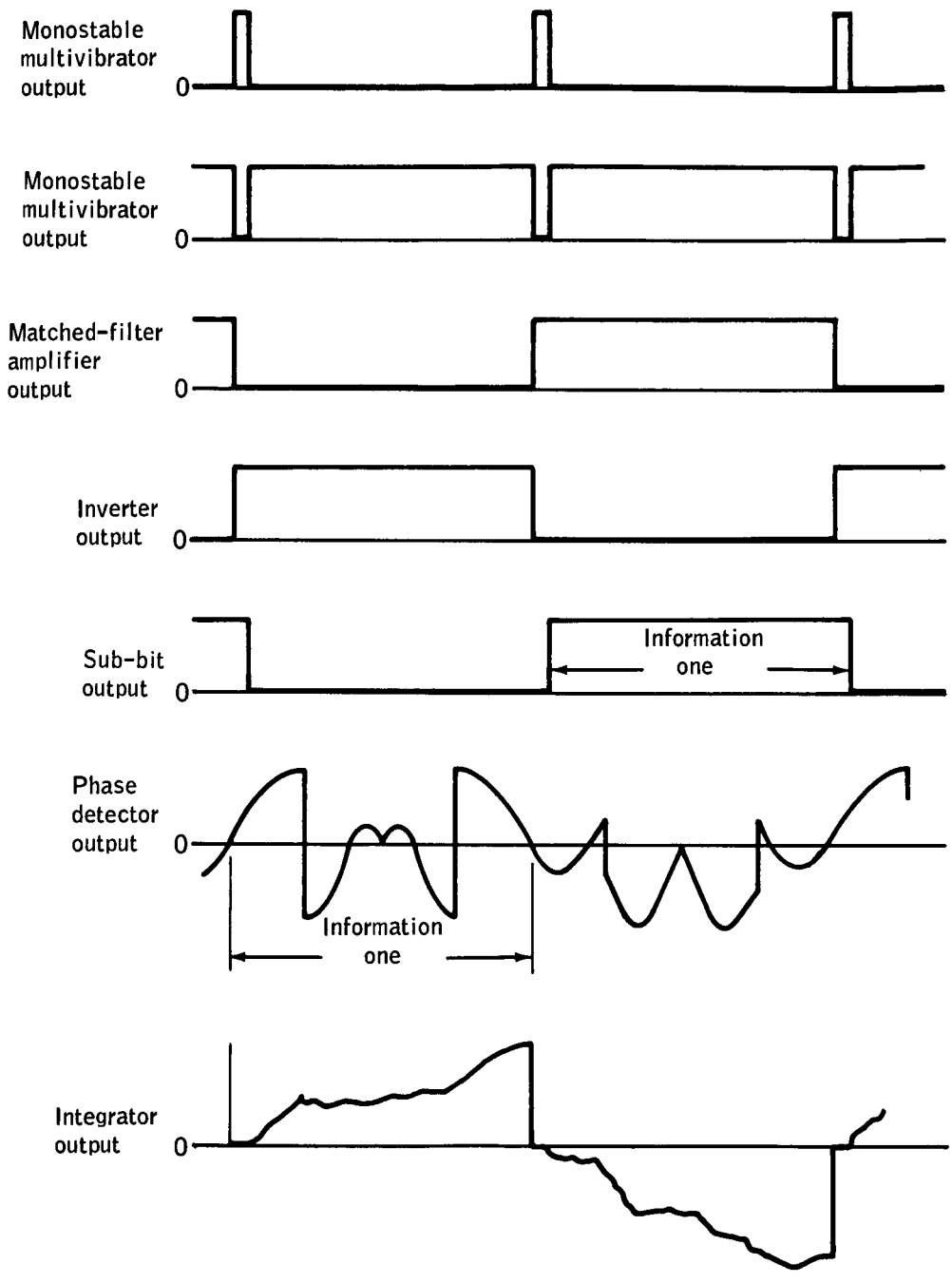


Figure 8. - Information channel, typical waveforms

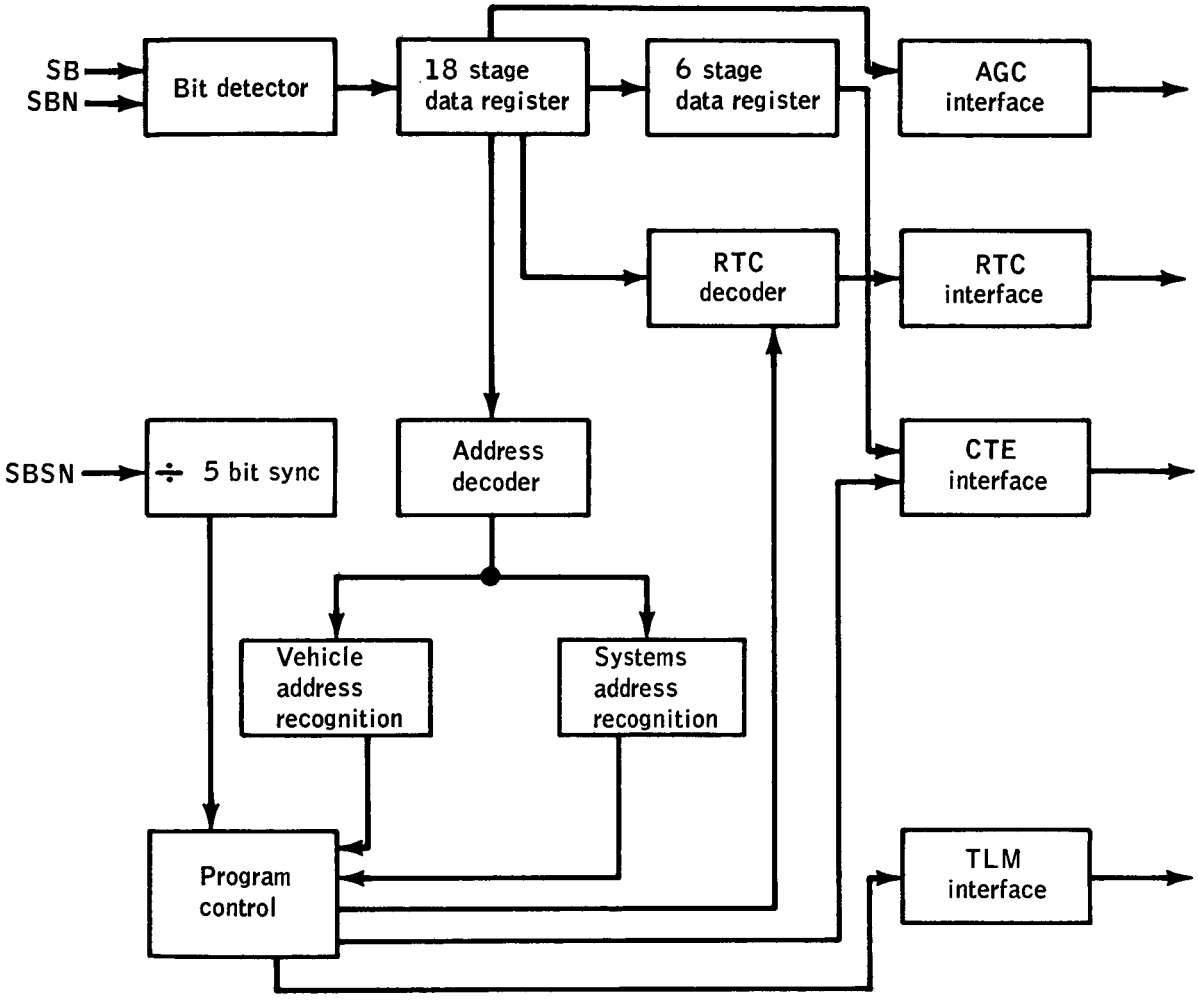


Figure 9. - Simplified block diagram of UDL decoder

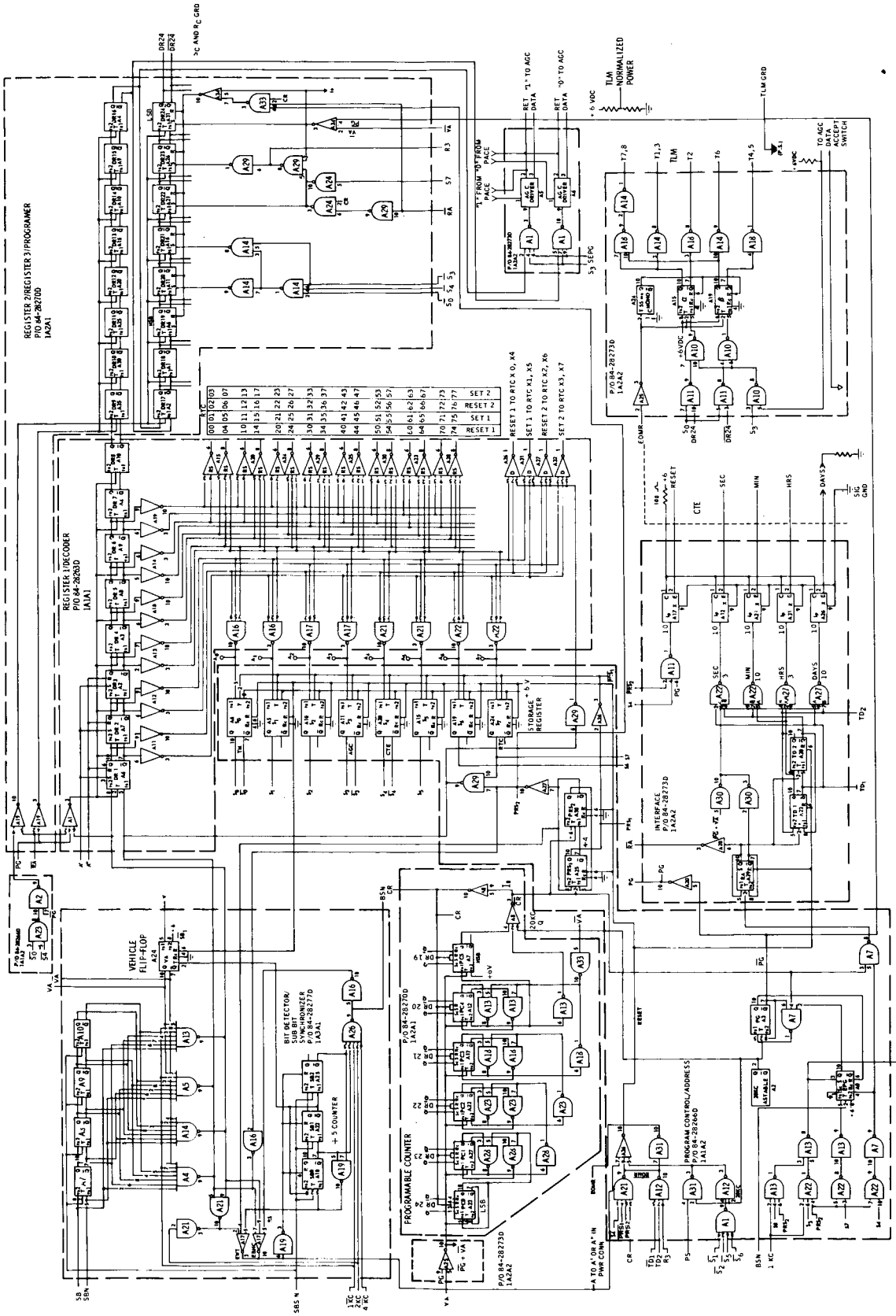


Figure 10 Decoder logic diagram

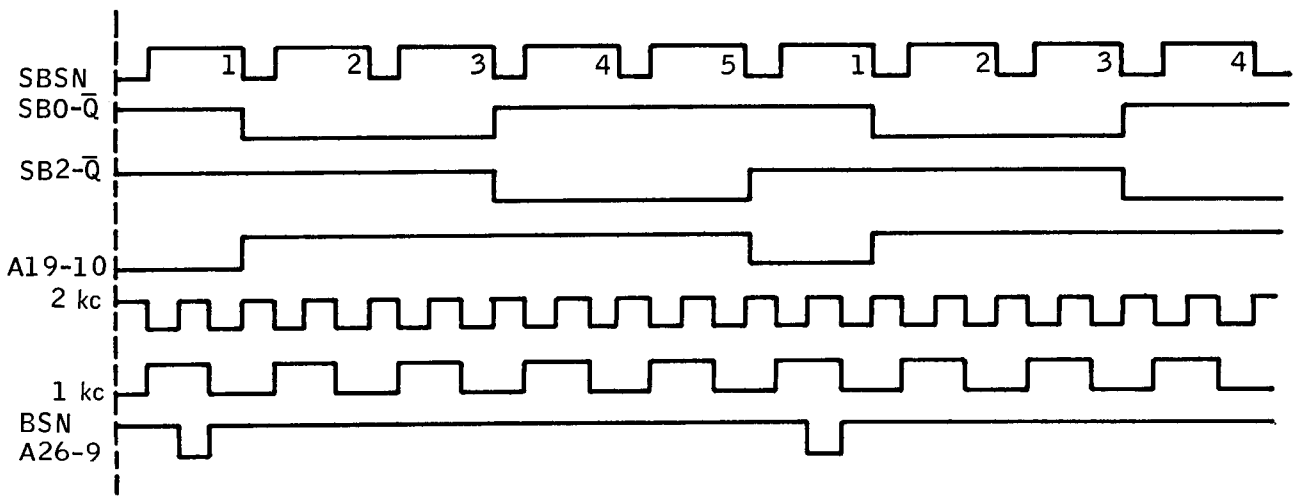


Figure 11. - Time diagram for generating BSN

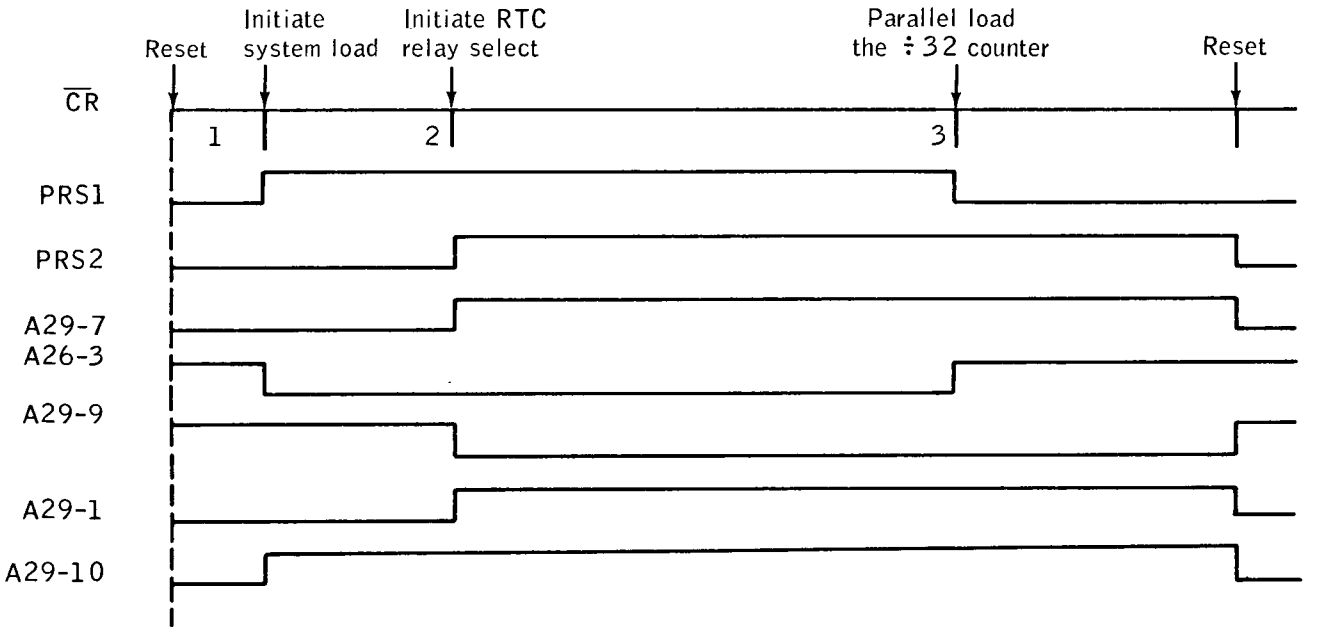


Figure 12. - Time diagram for RTC command (÷4 counter)

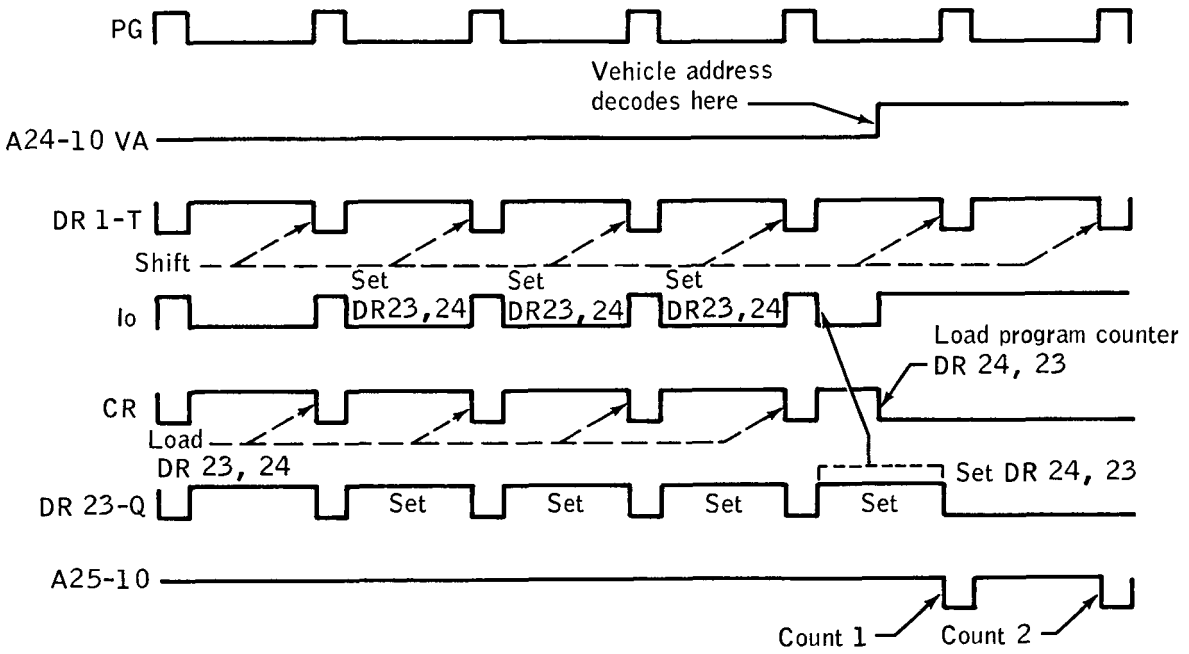
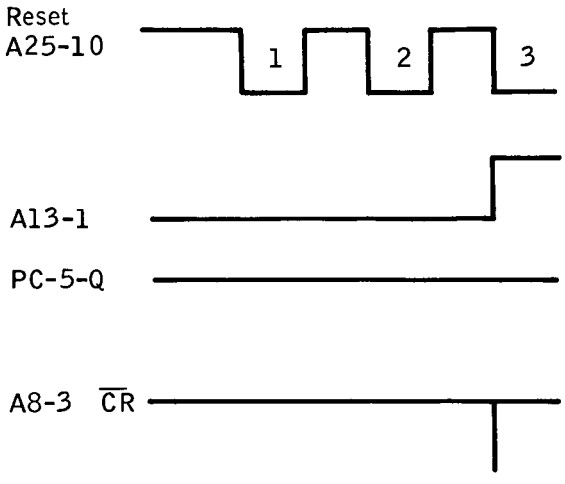
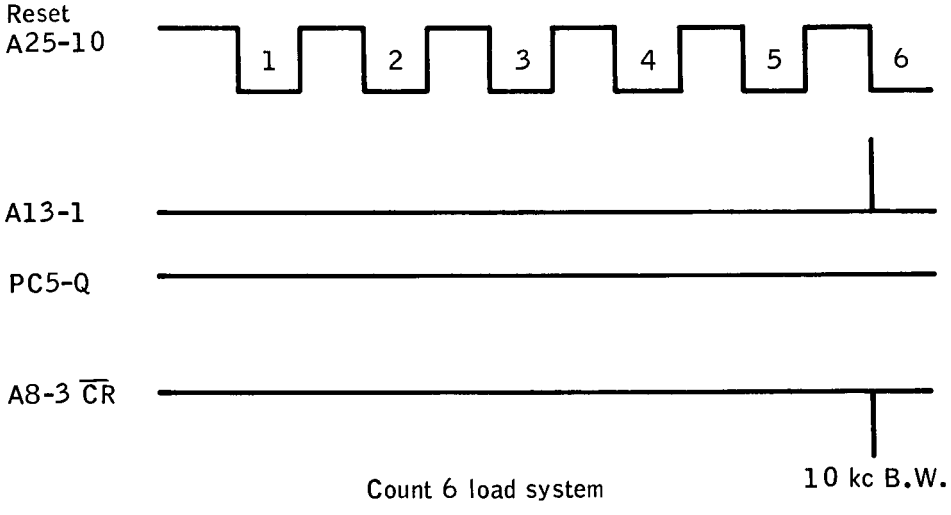


Figure 13. - Parallel loading sequence of the programable counter



Count 3 load system



Count 6 load system

Figure 14. - Time diagram for count 3 load system and count 6 load system

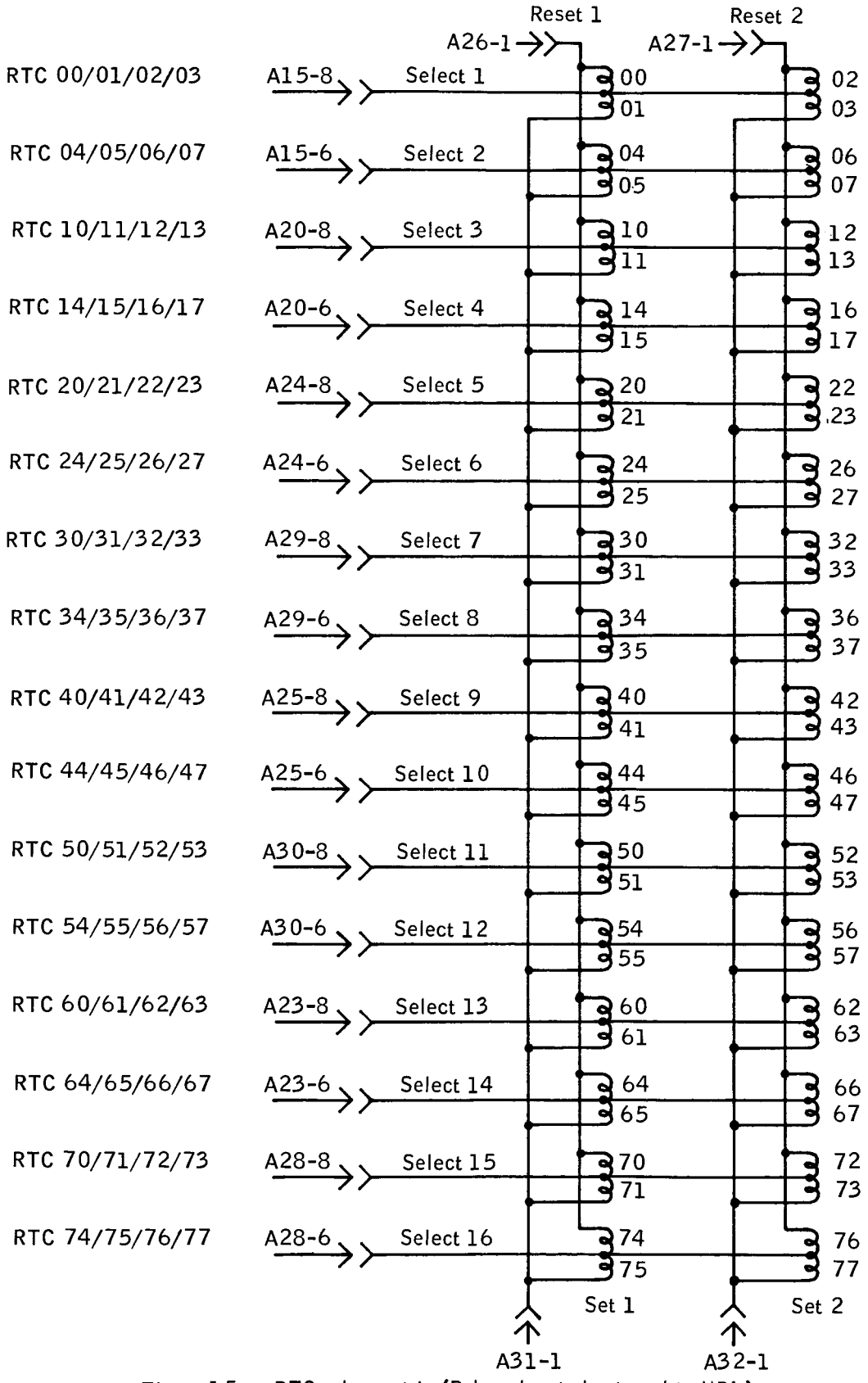


Figure 15. - RTC relay matrix (Relays located external to UDL)