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FINAL REPORT NO. 618

1 x 10^7 BIT MAGNETIC TAPE RECORDER DEVELOPMENT

Contract No. 950105, Modification No. 6, Phase II

(REL W.O. 1787)

To

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Raymond Engineering Laboratory, Inc.
Middletown, Connecticut

FINAL REPORT NO. 618
(REL W.O. 787)

1 x 10^7 BIT MAGNETIC TAPE RECORDER DEVELOPMENT

ABSTRACT

The basic task of Raymond Engineering Laboratory, Inc. (REL) under this development program was to design, develop, test, and deliver one prototype 1 x 10^7 bit magnetic tape recorder with the capability of multiple record and playback rates. Other design criteria are listed in paragraph I of this report. Shortly after work began on this contract, Jet Propulsion Laboratory (JPL) increased the four playback rates. The original playback rates specified in the contract of 21, 42, 84, and 168 bits per second were increased to 84, 168, 336, and 672 bits per second.

The 1 x 10^7 bit tape recorder developed under this contract is similar in some respects to the design and performance of the 1 x 10^6 bit recorder, also designed and developed by REL for JPL under JPL contract number 950105, Phase I. The major differences are: (1) the 10^7 bit recorder is larger in size and capacity, making use of four tape tracks rather than the two provided on the 10^6 bit recorder, (2) it provides four record speeds and four synchronous playback speeds instead of one each, and (3) it has an endless tape loop having 700 feet of tape rather than the 330 feet of tape used in the 10^6 bit recorder.

The first step taken by REL in this recorder development program was to make a breadboard system of the transport and

playback amplifier. Along with the breadboard development, a parallel program was conducted for designing and fabricating the components for the final prototype transport assembly. After the transport and playback amplifier breadboard system had been completed, specific circuits and sub-systems were then breadboarded in a table-top rack cabinet. An extensive development and test program of the breadboard electronic system followed, requiring several months to complete.

Following development and testing at REL, further electronic breadboard tests were conducted at JPL, including extensive environmental tests at type approval level. Upon completion of the tests at JPL, which resulted in some mechanical failures, the recorder was returned to REL to incorporate mechanical design improvements.

The preliminary study phase of this development program was concentrated in the following areas:

1. design and development of playback amplifiers capable of handling the very low amplitude (less than 100 microvolts), very low frequency (as low as 8 cps) playback signals;
2. design and development of a completely new integrator system (compared with the integrator system used in the previous 10^6 bit recorder) demanded by the requirements of the multispeed phase-locked loop control system;

3. design of logic systems for data and sync signals and for control purposes;
4. design of variable voltage power supply required by the multiple speed motor requirements.

In addition to reliably storing the required information, considerable effort was expended in designing flexibility of operation into the system. The recorder's ultimate use in the spacecraft required that it be possible to play back a block of data without disturbing the state of previously recorded information. To facilitate scanning, a slew or fast-forward mode was built into the recorder. This slew mode is further enhanced by the use of a system of data block coding. Means are provided in the system to identify the end of tape pack. This device is called the end-of-tape sensor.

The engineering prototype 10^7 bit tape recorder built under this contract meets the design and environmental requirements of JPL specification 31009A and the Mariner Engineering Data Recorder Characteristics as shown in REL Drawing D1737-1. See Figures 1 and 2 for photographs of the front and rear views respectively of the 10^7 bit recorder.

Electrically, the 10^7 bit recorder meets JPL specifications with the exception of power consumption. A maximum power consumption of 2 watts was specified; the 10^7 bit recorder has a power consumption of 2.5 to 4.6 watts on playback and 2.7 to 4.8 watts on record. JPL agreed in the contract to relax the

2-watt maximum power requirement to a value mutually agreeable to both JPL and REL.

The maximum specified weight of 10 pounds has been exceeded by approximately 1.6 pounds. The weight of the 10^7 bit recorder is 11.66 pounds without shock mounts and 13.2 pounds with shock mounts. The overall size of the recorder meets the specified 300 cubic inches.

I. SCOPE OF WORK

A. Contract Requirements

The requirements for the 1 x 10^7 bit magnetic tape recorder development are defined in JPL Contract 950105, Phase II, as modified in Modification No. 6 dated 1 May 1963. REL's task was to design, develop, functionally test, environmentally test, and deliver one Flight Prototype Magnetic Tape Recorder capable of meeting the design and environmental requirements of JPL specification 31009A entitled "Mariner B Flight Equipment, Telemetering Development, 10^7 Bit Capacity, Engineering Magnetic Tape Recorder" dated 13 September 1962. Additional design criteria for the prototype development were as follows:

1. Relaxation of the power, weight, and size limitations in paragraphs 3.3.19, 3.3.20, and 3.3.21 of JPL specification 31009A as approved by the JPL cognizant engineer;
2. Packaging of the prototype to be done by REL in accordance with paragraph 3.4 of JPL specification 31009A;
3. JPL to furnish the circuitry for the digital logic functions;
4. JPL to furnish one Government-owned data encoder simulator on a loan basis to be used during the development of the 10^7 bit recorder;

5. REL to submit a complete test program for the prototype which may modify the requirements stated in paragraph 3.4 of JPL specification 31009A where deemed necessary. This test program must be approved by the JPL cognizant engineer.

B. Brief Description of 1×10^7 Bit Magnetic Tape Recorder

The 10^7 bit magnetic tape recorder consists of a packaged sub-assembly which receives NRZ fully serial binary data on a single input line stores this data for an indefinite period, and synchronously supplies this data in NRZ binary form to a single output line upon command.

The readout from the recorder is synchronous with the bit and word synchronizing clock signals from the data encorder system of the spacecraft. Appropriate buffer stages and logic circuits are provided as part of this magnetic tape recorder to achieve a synchronized readout. The recorder's performance characteristics are as follows:

Bit storage capacity	1×10^7 bits (minimum)
Record rates	336, 672, 1344, and 2688 bits per second
Playback rates	84, 168, 336, and 672 bits per second

Error rate	Less than 1 in 10^5
Input impedance	Equal to or greater than 10 kilohms unbalanced to ground
Output impedance	Equal to or less than 1 kilohm unbalanced to ground
Input voltage	4.5 $\pm$1.5 volts
Output voltage	4.5 $\pm$1.5 volts
Start and stop time in the record mode	Equal to or less than 5 seconds

II. DESIGN PHILOSOPHY FOR DEVELOPMENT OF 10^7 BIT RECORDER

The realization of a successful digital satellite tape recorder was met with the REL Model 1656 10^6 bit system built for JPL. This machine used a 330-foot endless loop tape reel utilizing 1/4-in. wide tape and employing two tape tracks. Because readout was to be synchronous with the JPL Mariner spacecraft clock system, a very stable phase-locked loop servo system was designed which proved to be extremely reliable. This phase-locked loop made use of one of the two tracks, leaving the other track for data use. Data was recorded in serial configuration at a tape packing density of 278 bits per inch.

With the success of Model 1656 in mind, REL undertook, at the request of JPL, the task of developing and building a recorder system having a storage capacity of 10^7 digital bits. The record - reproduce system of this 10^7 bit recorder was to incorporate four record and four playback

rates. These new requirements dictated increased packing density and increased tape footage.

The state of the art at the time this development program commenced did not permit the use of packing densities in excess of 500 bits per inch per track. In order to serially record 10^7 bits of data on a single track system and use 500 bits per inch, a tape length of approximately 1660 feet would be required, which was not practical. By using three tracks, the 1660 feet is reduced to approximately 555 feet. If a more conservative packing density of 400 bits per inch per track is used, the required length would be about 692 feet.

Other means of reducing tape length are to reduce tape speed or increase the number of data tracks. REL's past experience with low tape speeds indicates that 0.01 ips is the lowest practical tape speed obtainable with today's state of the art. A maximum of four tracks can be obtained with 1/4-inch tape. Further increase of the number of tracks results in serious degradation of the signal-to-noise ratio due to the narrow widths. Therefore, the 10^7 bit system was designed around a 700-foot endless loop tape and three data tracks. The sync system requires one more track, making a total of four tracks.

The unique requirements of multiple rate record and playback operation prompted considerable effort to be expended in the areas of variable speed motor drive systems,

low level amplifier design, and motor speed control systems.

Three of the most important requirements, minimum size, minimum weight, and minimum power, imposed many design considerations that directly affected the overall complexity of the system.

The total system is made more complex due to the fact that incoming data must be extensively treated prior to being stored on tape. It was, therefore, necessary to use a number of logic circuits and associated control systems.

III. DISCUSSION OF MECHANICAL DESIGN AND DEVELOPMENT

A. Weight

The maximum weight of the 10^7 bit magnetic tape recorder, when fully packaged, is specified in JPL specification 31009A to be 10 pounds. This 10 pounds was a preliminary estimate, and the final tape recorder weighs 11.66 pounds without vibration isolators and 13.2 pounds with vibration isolators. These weights do not include externally mounted electronics. An approximate weight breakdown of the recorder, not including the major portion of electronics which is external to the transport assembly, is as follows:

Rotating mechanical modules and miscellaneous hardware	3.41 lb
Motors	1.12
Covers	1.76

Cover hardware	0.30 lb
Playback amplifiers	1.08
Chassis	2.72
Reel assembly	1.27
	11.66 lb
Vibration isolators and hardware	1.5
TOTAL	13.2 lb

B. Size

JPL specification 31009A states that the volume of the magnetic tape recorder, when fully packaged, shall be equal to or less than 300 cubic inches. The volume of the complete assembly, except for electronics and vibration isolators, is 260 cubic inches, well within the 300 cubic inches specified. The four vibration isolators will occupy slightly less than 20 cubic inches. The recorder chassis dimensions are 7.37 in. long by 9.0 in. wide, with a thickness from cover-to-cover of 4.0 in. These dimensions do not include the connector protrusions and vibration isolators. External electronics are also excluded.

C. Tape Transport System

REL's previous experience with the double capstan system to drive tape prompted the incorporation of

this design in the present unit. The principle of the dual capstan drive system is discussed in the following paragraphs.

Any tape reel assembly is subject to momentary increases in tape friction. This is particularly true of endless loop configurations, since their success requires that individual turns of tape slip against each other. This comes about due to the fact that tape is being pulled out of the pack at the center hub, a small diameter, and being played back into the reel at the outside of the pack, a much larger diameter. Equalization of tape movement relative to the withdrawal velocity can only take place if the remaining tape in the reel can slip to make up the required difference. In order to isolate these minute irregularities from the critical area of the tape heads, a dual capstan method is used.

The upstream capstan imparts initial driving power to the tape, thus determining its velocity. The downstream capstan is then used to draw the tape across the heads. The two capstans have a speed differential on the order of 2.5%. The downstream capstan turns at a faster rate; and by proper adjustment of tension belts, it can be made to slip at a very constant rate. If this action takes place, the upstream capstan will

then be the controlling factor concerning tape speed. The downstream capstan assures tape tautness and isolation of reel-produced irregularities. Were this approach not taken, serious degradation of signal quality would result. Flutter components would be introduced by minute velocity variations and amplitude modulation effects due to non-uniform tape-to-head contact.

Earlier recorders used rubber pressure rollers to force the tape into contact with the capstans. One of the requirements of the 10^7 bit recorder is that it not be in operation during launch. Rubber rollers develop serious dents if allowed to stand idle for a long period of time. As a means of eliminating this problem, REL has developed and proven a Mylar tension belt system which overcomes all of the problems caused by rubber idlers and also permits much more control over the adjustment of operating parameters.

Two motors, one for record and one for playback, are used in the 10^7 bit recorder in order to provide the eight different tape speeds required. Mechanical tape speed selection methods that use belts and clutches would have provided the required speed range but would not offer the reliability required for this tape recorder.

Other methods were investigated, such as the possibility of using a multi-polar motor winding. However, this would necessitate the switching of many pairs of motor leads and was eliminated as a possible means of providing the multiple speeds required. REL decided that a more efficient method would be to simply vary the frequency and voltage used to operate the synchronous motors driving the capstans.

To allow the use of two motors, one for record and one for playback, two slip clutches are used. Each clutch consists of an input pulley having a metal surface which is axially aligned with a high-slip surface on the output pulley. These two pulleys rotate within a helical spring which will slip only when the relative speeds allow. This couples the record or playback motor to the capstan system only if the speed ratio so permits. The clutches are arranged so that whichever is driven faster will lock and drive the capstans while the other overruns. This method accomplishes selection of mode and speed by merely switching power to the proper motor.

D. Tape

The 10^7 bit recorder was originally equipped with Minnesota Mining and Manufacturing Company (3M) LR1220 tape. During the first series of engineering acceptance tests conducted at JPL during June, 1963, the LR1220 tape failed due to its inability to

withstand the temperature extremes and due to a mechanical defect in the transport. As a result, 3M LR1353 tape was then tried in the recorder as it is supposedly able to withstand the required temperature extremes of -10 C to +75 C.

The LR1353 tape and some design changes resulting from the JPL tests were incorporated into the machine, and it was subjected to extensive testing at REL. It appeared that the LR1353 tape would be satisfactory, and the machine was hand-carried to JPL for a second series of tests with this tape installed. During this series of tests held in October, 1963, high flutter developed when operating at the temperature extremes. The machine was again returned to REL for additional study and redesign. The actions taken by REL, other than on tape, as a result of these tests at JPL are discussed in paragraph V.E of this report.

Analysis of the machine showed that a low frequency component was evident after modifying the capstan speed differential. This was occurring at the capstan rotational period and was due to a build-up of foreign matter on the capstan. This foreign matter was the shedding of the oxide from the active surface of the LR1353 tape. Microscopic examination of the tape indicated that loss of oxide had occurred and there were some small areas that showed complete

oxide removal.

The machine, while inoperative, was baked over night in an inert gas atmosphere at 80 C. On the following morning when attempting to manually advance the capstans, it was discovered that the tape was stuck to the capstans. When motor power was applied to the machine, the capstans were freed from the tape. Microscopic examination of the tape areas that had been in contact with the capstans revealed that oxide had been removed from the tape. The oxide had built up on the capstans to such an extent that the flutter amplitude increased to greater than 6%. It became necessary to clean the capstans in order to reduce the flutter to its normal value. This test was repeated with the same results.

The machine was then reduced to room temperature and operated. The oxide build-up was still evident but at a slower rate. It was still necessary to clean the capstans in order to maintain a low flutter level. The tests were then repeated using a new pack of LR1353 tape at both 80 C and room temperature. The results were still the same. The LR1353 tape was then replaced with the originally used LR1220 tape. The oxide build-up problem was eliminated.

REL conducted several tests with the same LR1353 tape pack in the transport as used at JPL.

This tape pack had seen at least 500 complete passes since it had been installed. Little or no information concerning the long term stability of 3M LR1353 tape was available. It had been originally installed since it was believed to be superior to LR1220 for high temperature operation. Examination of removed ball bearings showed an accumulation of foreign particles. Some bearings contained dirt identified as Graphitar, the substance used in the spring clutch assemblies. However, some doubt still existed concerning the other bearings. The possibility of tape lubricant and oxide flaking off of the tape and getting into the bearings still existed.

Information was received concerning the graphite lubricant used on the LR1353 tape. It appears that graphite will lose its lubricant properties if operated in total absence of oxygen or water vapor. Tests are being conducted at REL to determine the validity of this theory.

Since funds for further investigation had been exhausted, the 10^7 bit machine was returned to JPL for operating tests. The JPL cognizant engineer was advised of the problems existing in the area of tape stability, and it was mutually agreed that LR1220 tape would be installed in the recorder. This permits reliable room temperature operation but does

not allow operation of the machine at the temperature extremes.

E. Tape Reel

The tape is housed within a 5-3/4-inch diameter enclosed reel. This reel is mounted at a 5° angle to the main plate. The loop pack revolves on a bearing-mounted central hub in the form of a right conical section from which the tape is pulled. Withdrawing tape from the inside causes rotation of the pack so that tape will wind on the outside. One flange of the tape reel is provided with several rollers having their axes along the diameters of the flange. These provide bearing surfaces for one side of the tape pack. The other flange rotates with the hub and pack.

The tape pays out of the hub at an angular displacement of about 45° from its normal capstan approach plane. A wire guide is provided at the exit point of the reel to control the path of the tape so that it will approach the upstream capstan in a parallel manner. The original wire tape guide had a tendency to serrate the tape edge causing an increase in effective tape thickness. This caused the reel to eventually bind. As a result, a new wire guide was designed which eliminated this problem and is currently installed in the machine.

F. Tape Speed

Initially, JPL specification 31009 indicated four data rates to be used in the playback mode, the lowest being 21 bps. REL's considerable previous experience in low speed tape operation indicated that a tape speed of 0.01 ips was the minimum tape speed obtainable within the present state of the art. A few of the problems occurring at this speed are: (1) very low head output, less than 100 μV, (2) low signal frequency which places serious demands on the signal amplifiers, and (3) flutter and jitter components which could have a detrimental effect on data reconstruction.

Since we have three data tracks with a density of 400 bpi per track, a total packing density of 1200 bpi results. Therefore, $1200 \times 12 = 1.44 \times 10^4$ bits per foot of tape, yielding about 700 feet of tape. At the lowest playback rate of 21 bps, $\frac{21}{1200} = 0.0175$ inches per second which was the lowest playback speed.

At the other extreme, the highest record rate is 2688 bps. Thus, $\frac{2688}{1200} = 2.24$ ips, this speed posing no problem.

Tape speed is directly proportional to data rate, i.e., if the data rate is doubled, then the tape speed must be doubled. Tape speeds of 0.0175, 0.0350, 0.0700, and 0.140 ips were established for the playback mode.

In the record mode, 0.28, 0.56, 1.12, and 2.24 ips were determined to fulfill the four record rate requirements.

Shortly after REL had started this development program, JPL warned of a forthcoming increase in playback data rates. At the JPL-REL conference held in August, 1962, the new playback rates were established at 84 through 672 bits per second. Because of this increase in playback rates, it was necessary to increase the tape speeds as follows:

Playback Rate (bps)	Tape Speed (ips)
84	0.07
168	0.14
336	0.28
672	0.56

A fast-forward mode, designated slew, is included as an operating requirement. This slew makes use of the 2.24 ips tape speed and is elected by proper programming of the control system. This mode is of value when scanning the tape to return to the beginning of the tape pack. In order that the exact beginning of the tape cycle be accurately known, an electromechanical device, the end-of-tape sensor, is included in the design.

More conventional systems employ a mechanical timer which operates from the record mode pulley system and

indicates the end of each tape passage. This method was not accurate enough to meet the requirements set forth in JPL specification 31009. Most timers are subject to belt slippage and cannot compensate for variations in tape length. For the 10^7 unit, a number of methods were investigated, including photoelectric sensing of a fixed mark on the tape and the use of conductive material on the tape splice. It seemed that the latter method, the use of a splice sensor, was the only one offering all of the advantages of a true tape end indicator and did not have the usual weaknesses of conventional mechanical timers. A detailed description of the operation of this system is given in paragraphs III.I and IV.F of this report.

G. Motors

In an effort to remain within the desired power consumption goal, motor design became very important, as the motors use most of the total power. With motor efficiency of prime importance in this particular recorder, considerable time was devoted to preparing motor specifications. H. C. Roters, one of the few qualified sources, was selected to perform this motor development which took several months to complete.

A typical motor when designed for and operated at its maximum conversion efficiency very often hunts. This hunting effect comes about due to the equivalent

spring mass system as produced by the motor and its rotating load. Therefore, REL had to be careful to avoid this critical area. This could be done only by sacrificing efficiency. The motors were built to provide maximum electromagnetic efficiency and maximum shaft torque per milliwatt of input power. Appendix I shows the tabulated results of tests of both motors.

Initially, it was planned to provide two motors in the 10^7 bit recorder. However, it became possible that one motor might suffice rather than two with the new playback rates. Further action on the motor procurement and the mechanical design of parts was temporarily halted at that time, pending a firm decision on the new playback rates. Tests of speed control at the higher playback rates would be required to determine motor requirements. Speed control tests were then conducted over the new playback rate range of 84 to 672 bits per second. At this time it was decided to retain the two-motor configuration, including a separate power supply for each of the motors.

An experimental playback motor was ordered from H. C. Roters to investigate speed control. To speed up procurement, only the torque requirements were specified, leaving the mechanical details to Roters. Various difficulties were encountered with the experimental motor which delayed development somewhat at

that time. The breadboard motor power amplifier supplied to Roters was damaged in shipment. Delays were incurred in receiving the amplifier back at REL, repairing it, and returning it to Roters. A circuit failed during the initial motor test, probably due to exceeding the maximum voltage limitation of the motor drive transistors. After considerable delays due to damage encountered in shipment of the motor amplifier on two different occasions, the motor was finally installed in the breadboard and initially tested in late September, 1962. The phase-locked loop was operated briefly at 84, 168, 336, and 672 bits per second with encouraging success.

Each motor is required to operate at four speeds. As stated earlier, this is accomplished by selection of input frequency. Input voltage must be varied also in order to maintain the ampere-turns, torque relationship.

It has been found that synchronous motors can operate over a maximum speed range of 8:1. This figure is limited by such factors as possible cogging at minimum speed and problems of bearing life at the high end. The selection of motor shaft speed is based upon the best possible compromise consistent with life expectancy. The motor shaft speed is then reduced to a suitable capstan speed by the use of pulleys and endless

Mylar torque transmission belts.

Usually the motor speed should not exceed 8000 rpm if life greater than 1000 hours is desired. The minimum practical frequency is 50 cps which, with a 6-volt motor supply, results in a speed of 1000 rpm. The disadvantage of this system is the magnitude of bearing losses at higher speeds and lower temperatures. It was estimated that the motor should develop a shaft torque of 0.1 in.-oz at 8000 rpm. Therefore, electromagnetic torque must be 0.22 in.-oz to account for the losses at low temperature. This torque, at a speed of 8000 rpm, is equivalent to power of 1.33 watts.

REL was requested by JPL to furnish information on the relative complexity of other mechanisms to provide data rates other than those within the present scope. The items investigated were:

1. provide switching in the present mechanism so that the playback motor can be used in recording 336 and 672 bps;
2. use just one motor for four record rates and four identical playback rates;
3. add a motor to (2) for recording at 21 bps;
4. use two motors, independent of mode, one for 21 - 168 bps and the other for 336 - 2688 bps.

At a meeting held at REL with JPL in mid-September, 1962, it was mutually agreed that extra switching would

not be included which would allow recording with the playback motor at certain rates.

Roters' first step on the record motor was to build a model to determine rotor-stator parameters. At this time it was decided that the playback motors would be identical in power level to the record motors.

During H.C. Roters' final testing program of the playback motor, it was discovered that the motor could not develop sufficient torque at minimum temperature. This necessitated the fabrication of a new rotor which further delayed the delivery of the playback motor. This particular slip on the playback motor was longer than usual and was attributed to a combination of circumstances. Early in the design, general fabrication troubles caused Roters to completely review the design and build a special test model. As stated previously, when the design was finally completed, it did not meet REL requirements. A month was required to fabricate new parts and retest the unit.

H. Heads

An initial study of the problems caused by the very low playback speeds of the 10^7 bit recorder indicated that a significant gain in recovered signal amplitude could be achieved by using two coplanar blocks rather than conventional in-line heads. Therefore, the 10^7 bit recorder is provided with two sets of interleaved

coplanar heads. These two sets of heads were completely analyzed during the development program. The head specifications are given in REL Dwg C1737-102. A new source for the heads was selected, IMI Magnetics of Glendale, California, who have more experience with high temperature and multi-track problems than REL's previous suppliers.

Since the existing mechanical breadboard did not have enough distance between capstans to permit simultaneous mounting of the two coplanar blocks, a new chassis plate was fabricated during the initial evaluation of the heads. Tests were conducted to determine the combined effects on skew and gap scatter which are measurements directly related to the geometry of the heads of the coplanar head assemblies. Paragraph V.B.4 of this report describes these tests in detail.

Four tracks are provided on the tape -- three data tracks and one sync track. The selection of the sync track was based upon the results of the skew and gap scatter tests referenced above. Since the head gap scatter and skew tests were repeated using each of the four tracks in turn as a reference, an excellent analysis of the poorest conditions could be made. As a result of this analysis, it was determined that the best compromise of gap scatter and skew was achieved using track 2 as the reference. Figure 3 shows the

plotted wave forms of gap scatter and skew tests.

I. End-of-Tape Sensor

One of the requirements of the system is an end-of-tape sensor which provides a signal when the end of the 700-foot tape pack has been reached.

The end-of-tape system consists of three parts (see REL Dwg B1737-5):

(1) The stationary contact assembly, sensor, which also serves as a tape guide. The sensor consists of two coils of Paliney wire would in close proximity to each other. A spacing of about 0.050 in. is used between the two coils.

(2) A gold leaf approximately 1 in. long is bonded to the oxide side of the tape. As the gold passes over the coils, they are electrically shorted which completes an external circuit.

(3) The associated electronic end-of-tape pulse shaping circuit is discussed in paragraph IV.F of this report.

This end-of-tape system provides a multi-point contact. This reduces any possibility of introducing noise and greatly improves reliability.

The first tape splice sensor tried was of the segmented washer configuration and was supplied by the head manufacturer. This sensor was used with aluminum-

backed splicing tape. The initial tests of this splice sensor in the mechanical breadboard were not very encouraging. The aluminum oxide that is normally present on the surface of the splicing tape prevented proper contact which could not be obtained without resorting to abnormal tape wrap pressures. Also, the tape lubricant was too good a conductor. The sensor had to contact the lubricated surface of the tape with a [illegible] design.

Efforts were then directed to affix a suitable actuating material on the oxide side of the tape. It was believed that gold foil would be suitable, but none could be found with satisfactory adhesive material. Several methods of bonding the gold foil to the tape were tried, including shellac with a suitable thinning agent and Plicbond 20 with methyl ethyl ketone solvent.

The next step was to attach several gold foil strips to a 700-foot tape loop using both of the above methods of bonding. This tape was installed in the breadboard drive assembly along with the sensor and operated as much as possible to determine any existing problems. It was set up to determine whether or not the oxide would wear away the sensor contact surfaces, whether the lubricant would affect the sensor,

and whether the foil would be damaged in any way during continual motion. In addition, the suitability of the bonding methods was determined. The splice sensor completed approximately 1000 cycles of operation and then it became short circuited by a deposit of a lubricant-oxide mixture. The conclusion was that the adjacent conductors of the sensor were too closely spaced. Alternate sensor designs were investigated and the problem eliminated. Also, it was determined that Pliobond 20 with methyl ethyl ketone was the most stable method of bonding the gold foil to the tape.

A new tape with new gold foil was life tested. The results showed that freshly lubricated tape would not cause contamination problems. After about 400 passes, the foil began to crack and some foil separated from the tape. Examination showed that either the foil had moved along the tape or the tape had expanded or contracted relative to the foil. These particular tests had been conducted without allowing sufficient time for the adhesive to set--a possible cause for the failure.

A short tape loop was installed in the breadboard tape transport on which two foil strips were attached with a 50 per cent mixture of Pliobond 20 and methyl ethyl ketone solvent, allowing a day for curing.

These foil strips completed 4000 passes after which cracking, but no flaking, was observed. The test was repeated with increased tape tension and a greater tape wrap angle at the capstan. It was found that the tape tension and wrap angle had to be increased to abnormal values before damage due to wear would occur.

Following many additional tests, it was found that a Paliney wire sensor with a gold foil actuator proved to be the best combination. A gold foil thickness of 0.0003 in. was quite flexible and showed very good life. Spacing of the sensor coils was modified and the surface finish controlled to eliminate particle clogging. This end-of-tape sensor proved most adequate for the 10^7 bit recorder developed under this contract. However, the bonding operation is quite time-consuming and costly. In addition, a possible source of trouble could occur in the mixing and curing of adhesives. The entire operation does not lend itself to an efficient manufacturing process for flight hardware.

Near the end of the 10^7 bit recorder development program, investigations were directed toward finding a means of eliminating the gold foil bonding operation. It was hoped that a suitable material could be found that would be spliced directly into the type

pack. This new material must have high mechanical strength and excellent electrical conductivity.

A commercial Mylar material with either aluminum or copper foil laminated to it was obtained. While no specific information could be obtained on the bonding adhesive used because it is proprietary information, it was determined that the adhesive apparently had the following characteristics:

(1) a very high cure temperature, approaching that of Mylar,

(2) stable mechanical and thermal properties as evidenced by its resistance to at least ten extreme thermal shock cycles covering the range of -30 C to + 125 C,

(3) the substance is chlorine-free and chemically inert.

With reference to (3) above, studies are presently being conducted to determine the extent of out-gassing at low atmospheric pressures.

It is possible to gold plate both the copper and aluminum laminates so that good electrical conduction occurs. Since the gold plated laminate appears to be superior to the gold foil, the final 10^7 bit recorder shipped to JPL in November, 1963, incorporated the gold plated copper laminate sensor splice.

J. Covers and Container Sealing

Two covers, each containing an intergrally molded Viton Gask-O-Seal, attach directly to the chassis. Both covers are 8.984 in. long x 7.359 in. wide. The cover for the rear of the chassis is 1.866 in. deep; the front cover is 1.384 in. deep. The Gask-O-Seals behind the connecters affect a hermetic seal to maintain atmospheric pressure within the assembly. Loss of pressure could cause rapid evaporation of lubricants and other possible defects leading to early failure of the tape recorder.

Initial data received from the Parker Seal Company indicated that their leakage rate was reasonably close to the predicted values. REL insisted that Parker measure leakage both at room temperature and at 80 C where leakage is usually several times greater. Initial leakage measurements of the covers yielded expected values at room temperature but excessive values at 80 C. By coating the inner surface of the covers with grease, this rate was reduced. Even though these parts were fabricated from rolled stock rather than castings, it appeared that vacuum impregnation was essential. It was determined that although the leakage is not excessive in terms of a one year mission, at 80 C the covers were apparently more porous than others made from similar stock. An attempt was made to

determine whether fused tin plating would yield a worthwhile improvement, impregnation having been of limited value according to Parker's test.

When the transport was brought to JPL in accordance with a prearranged schedule, the covers were still being tested at the Parker Seal Company. Consequently, it could not be determined prior to delivery whether a good seal could be obtained with a particular set of hardware. These covers were later obtained by the REL engineer assigned to the evaluation and were installed at JPL. The Parker Seal Company indicated that their initial tests showed that the fused tin plating was not particularly successful in reducing the apparent porosity of the magnesium base metal. The results of the leakage rate tests conducted at JPL and the problems encountered during the tests are given in paragraphs V.D. and V.E. of this report.

K. Vibration Isolation

In order to operate successfully during mild vibration and to survive severe vibration and shock, it is essential that the transport mechanism be protected by vibration isolators. The vibration isolation problem was initiated by further investigation of the REL design of the isolators used with the 10^6 bit machine. Along with the further study of the REL design, several design proposals and cost estimates for fabricating the isolation mounts were sought from subcontractors.

M. B. Electronics, Lord, and Barry were among the vendors contacted.

Cutback of the project funds precluded any further development of shock mounts. The matter could not be pursued any further without large expenditures of both time and money. REL decided to use Lord HT 1-10 shock mounts. While these units proved to perform quite well, a better vibration system could have been obtained with more time.

It was apparent that REL's original value of transmissibility or Q of the system was substantiated. The Q appeared to be slightly greater than 2.5. The resonant frequency was 40-45 cycles for the full package.

Unfortunately, the JPL mounting data was received too late in the project to allow the construction of sophisticated brackets. When the JPL mounting data was received, it was discovered that the original mounting holes located along the chassis plate of the recorder could not be used. A new set of mounting holes had to be drilled in the recorder main plate. This resulted in the use of a mechanically poor mounting bracket configuration.

IV. DISCUSSION OF ELECTRONIC DESIGN AND DEVELOPMENT

A. Power Consumption

Initial power calculations and analysis indicated that the recorder power consumption would be considerably

higher than usually necessary because of the variable speed feature. The initial calculations were based upon experience which indicated that at 8000 rpm, the electromechanical conversion efficiency would be on the order of 40 per cent. Motor input, therefore, would be 3.31 watts. The breadboard power converter to be used and operated from the 2400 cycles per second power source was designed for an efficiency of 70 per cent. Thus, the total power taken from the 2400 cycles per second line would be about 4.7 watts. An additional 0.1 watts from the +20 Vdc source would be used to control the 2400 cycles per second converter and some motor drive circuits. An extra 50 per cent must be allowed for starting transients which brings the peak power consumption up to 7 watts momentarily.

The initial power consumption calculations were based upon original motor data. Because of a few uncontrollable parameters, such as bearing drag at higher motor speeds, the final power consumption was higher than originally anticipated. The bearing data supplied by Barden was probably conservative, which affected the calculations.

The recorder power consumption is considerably higher than normal because of the variable speed feature. The power consumption of the 10^7 bit tape recorder is as follows: Playback -- 2.5 to 4.6 watts, depending upon speed; Record -- 2.7 to 4.8 watts,

depending upon speed. REL's approach was to obtain the best possible efficiency under the variable speed conditions required of this recorder. The programmable power supply helped to obtain this efficiency.

B. Programmable Power Supply

The purpose of the programmable power supply is to provide dc voltage to the record and playback motors. This is programmed from data rate selection logic lines. There are two programmable power supplies in the 10^7 bit tape recorder: REL Dwg D1737-73 shows the record programmable power supply, and REL Dwg D1737-74 shows the playback programmable power supply.

The programmable power supply design was approached with efficiency utmost in mind and with suitable circuit flexibility in order that the system would be compatible with the available logic control systems. The original motor power supply program centered around attempts to design a system enbodying phase-controlled rectifiers. A considerable number of approaches were tried and none of these were acceptable.

A method was tried using R-C phase shift networks to control firing points of conventional silicon-controlled rectifiers (SCR's). While this method is about the simplest of all, efficiency is low due to the large amount of power required to fire the SCR's. The system also requires the use of fairly large

components. Since size and weight must be kept low, this method was rejected.

Other methods, including the use of generated timing pulses, were attempted. Little or no information exists concerning the practical use of SCR's at frequencies above standard 60 cycles per second sine wave power. Again, unijunction timing circuits require considerable power. A simple circuit using a unijunction timing pulse generator had to be abandoned because of this limitation. Serious problems arose due to slow SCR firing time and the problems introduced by the 2400 cycle per second square wave rise time. Since the 2400 cycle per second satellite power is a square wave, the reverse spikes occuring at each cycle change caused severe misfiring of the rectifier timing circuits. Means were provided to clamp the SCR gates during the unwanted part of the cycle but excessive power was lost due to the relatively low impedance of the SCR gate.

The use of transformer coupling worked quite well. However, it became necessary to modify other parts of the circuit, particularly the timing pulse generator system, so that sufficient energy could be transferred to the SCR gate.

Various other methods and circuit configurations were tried, but usually component size or power consumption were limiting factors and precluded their

eventual use.

The present system makes use of chopped dc analagous to the output of a phase-controlled rectifier. Figure 4 is the block diagram of the programmable power supply. In this system a group of four selectable voltage-controlled oscillators (VCO) are used to generate timing pulses. Figure 5 shows the equivalent circuit of a typical VCO. The VCO consists of a silicon-controlled switch (SCS) which is used very much as a unijunction. An R-C network having a differential amplifier to control charging time is used as a frequency determining element. The electrode potentials of the SCS are chosen to fire at a point on the R-C curve which will give fair linearity and also eliminate temperature problems.

The output of the VCO is a positive-going spike having a fast rise and fall time. Selection of a particular VCO is accomplished by logic switches (transistors) operated from any one of four input command lines.

One of the two inputs to the differential amplifier is a reference voltage stabilized by a Zener diode. The other input is obtained from the final dc output voltage after being reduced to a proper level by the input voltage divider. The VCO frequency at any instant is a function of the difference of the reference voltage

and the power supply output voltage. The frequency range is determined by the SCS operating point, the capacitor value, and the ratio of resistor values which control the charging rate of the capacitor.

The VCO signal drives a unique one-shot circuit as shown in Figure 6. This monostable circuit is capable of producing very narrow pulses of fixed width while introducing very little jitter. A standard JPL flip-flop card is triggered to SET mode by a pulse from the VCO. The output Q goes high, thereby allowing Q1 to complete the charging path of capacitor C1. The SCS Q2 is arranged with its cathode gate potential such that when C1 charges, the cathode voltage will fall, finally reaching a point where the SCS will fire. Upon firing, the capacitor is discharged through the SCS, and a negative-going voltage is obtained at the SCS anode which is used to reset the flip-flop. Thus, the flip-flop, upon changing state to RESET, will turn off Q1. The next VCO pulse will again set the flip-flop and repeat the cycle. The result is a signal taken from the Q output of the flip-flop which has a width determined by the R-C constants of the SCS circuit and a repetition rate controlled by the VCO. The pulse duration is 50 μ sec.

The 50-μ sec pulse generated by the monostable circuit is transformer-coupled to a silicon power

transistor Q1 -- see Figure 7 for this chopper circuit. This chopper transistor is in series with a fixed dc voltage obtained from a transformer-rectifier system operating from the 2400 cycle per second power line. The nominal design center voltage is 50 V. The chopper stage interrupts the fixed dc at a rate determined by the VCO. The chopped dc is smoothed to an average level by the action of the L-C filter stage L1 and C1. Inasmuch as the output voltage is determined by the rate at which the chopper is driven, this voltage can be fed back to the VCC differential amplifier. This maintains a steady state voltage at the supply output terminals.

It was mentioned earlier that a Zener reference is used in the VCO. This Zener voltage compared with a segment of the supply output voltage causes the selected VCO to operate at a frequency which will give the desired dc voltage output. Since the system contains the above-mentioned feedback path, the output dc voltage can be selected to any value below the original rectified 50 V and can be regulated for both load and input voltage changes. Typical VCO frequencies to produce wanted motor voltages are as follows: 672 bps - 5800 cps; 336 bps - 3000 cps; 188 bps - 1700 cps; 84 bps - 1100 cps. These are design center values and in practice may vary slightly. These represent

motor voltages of approximately 32, 15, 8, and 5 V.

The advantages of this method of power control are:

1. No waste of unwanted power. Voltage drop across the chopper stage is quite low, typically 0.4 - 0.6 V. Thus, little power is dissipated as heat.
2. Driving power is low since SCS oscillators will operate reliably at low power levels. No power is wasted in attempting to control the system.
3. Ease of output voltage selection by logic line. Simply adjusting the frequency of each VCO will allow large changes in output voltage while maintaining this value over wide temperature and load variations.
4. Size of complete four-speed motor supply system is not excessively large. The only components contributing to size and weight in any appreciable amount are the transformers and capacitors.

In reviewing the power supply problems, it may be seen that the power system used in the 10^7 bit recorder more than fulfills all requirements. Further refinements could yield a system which could provide a wider output range with a smaller physical size.

The efficiency under worst case conditions of load and temperature is about 70 per cent.

C. Logic Circuits

1. General Discussion of Logic System

Three signals are received from the spacecraft: (1) NRZ data input, (2) word sync, and (3) bit sync. In order to achieve a maximum packing density of 400 bits/inch/track, serial input data is converted to semi-parallel data. This permits the three data tracks to be loaded, bit-by-bit, to ultimately achieve the packing density of 1200 bits/inch on 1/4 in. tape. This was REL's original design intent, and this result was successfully accomplished.

It was necessary to count both word and bit pulses to derive sync pulses which would allow the word bit to be fed to each data track in the proper sequence. See REL Dwg E1737-56 for the overall logic system circuit and REL Dwg C1737-70 for wave form timing diagram.

As mentioned above, data to be recorded is routed by discreet bits into three tape tracks. Various methods are available for accomplishing this. It would be possible to record all data on one track for the entire tape length, then transfer to the next track for another tape pass,

and finally use the third track. This method has so many drawbacks that serious consideration was not practical. Other systems involve scanning the tracks electrically and feeding data onto the tracks in a parallel manner. None of these methods were worth considering inasmuch as certain requirements concerning error rate and synchronous operation made their use entirely impractical. REL elected to use a more sophisticated system whereby the maximum possible packing density was obtained.

The method used resembles a parallel feed system except that the bits are laid onto the tape in a quasi-parallel manner. The trigger pulses which set up the record process are derived from the bit counter shift register. A word counter is provided so that every fourth word will have its first word bit again routed to track 1.

The bit counter block diagram is shown in Figure 8, and the wave form timing diagram is shown in REL Dwg C1737-70. This circuit consists of a shift register receiving its toggle from the bit sync linc. Steering is so arranged that a pulse will be present in the three output lines in the sequence of 100100100, shifted by a 1-bit interval. The shift line pulse is inhibited during reset of the bit counter. This is required so that the

first bit of every fourth word will occur at the proper time to allow storage on track 1. The reset and shift inhibit signal is obtained from the word counter.

Since the storing of bits in the manner outlined requires some means of word identification, a word counter is required. This need is made even greater by the decision to operate the phase-locked loop system on every fourth word or one integration per three words. Thus, the word counter serves a dual function. Originally a simple two-stage binary counter with short-count feedback was used to divide by 3. However, the short-count feedback pulse showed up on the counter output lines. This pulse caused serious triggering problems in the remainder of the system. The counter with the short-count feedback was abandoned in favor of the present method.

The present word counter is much like a shift register except that steering is determined by logic. Figure 9 is the word counter block diagram. The shift line is driven from the word sync. Thus, the output line of the last stage will change state on the third word pulse and hold for 7 bits (1 word) and then reset on the next word. The output lines are used to set or reset the tape word sync

flip-flop by means of a gate circuit so that the flip-flop output signal will have close to a 50 per cent duty cycle over a 3-word interval. The ratio is 10 bits on, 11 bits off. This signal is recorded on the tape for use as the sync signal. The word counter output is also used to reset the bit sync counter on every third word.

2. Date Recording

The date line fed to the recorder system carries inverted serial NRZ data. This signal is inverted again, and the two signals consisting of NRZ and its inverse are applied to the toggle steering points of the three record flip-flops. Refer to Figure 10 for the block diagram of the record logic system. The condition of the incoming data determines the possible state to which an individual flip-flop might shift.

The toggle signal is obtained from a group of three dual gates, one for each flip-flop. These gates receive inputs from the bit counter and the bit sync line. In the early stages of development, untreated bit sync was used to interrogate and open the gates. Severe problems of coincidence existed using this method. The difficulty was due to the propagation time of the bit shift register. The strobing pulse and the bit sync did not always

arrive simultaneously. This problem was overcome by using differtiated bit sync. The bit sync pulse is R-C differentiated, and the negative-going pulse is inverted. The result is a bit signal arriving late by 1/2 of a bit pulse width. Thus, the gate is opened after arrival of the strobing bit pulse derived from the bit counter. Stability is built into the system.

Upon coincidence, the gate output will go to 0. The steering of the flip-flops by the data and data inverse causes trading, the direction of which is determined by the 1 or 0 condition of the data. This action is done sequentially as dictated by the strobe pulses from the bit counter. Each data bit will be strobed into each data track in their own order of occurance.

The record flip-flop signal output is supplied to push-pull driver stages which feed the center-tapped record head coils. REL Dwg C1737-63 is a schematic diagram of the head driver stage. A driver is used for each track. The tape is magnetized first in one direction for a 1 and then in the other direction for a 0. This results in one flux reversal per discreet bit change.

The voltage used to operate the track drivers is derived from a PNP transistor power switch.

This is done so that record power can be inhibited when not in record mode, thus insuring that recorded data will not be indiscriminately erased. The inhibit signal for this circuit is derived from the recorder control logic system.

3. Playback Logic

In the playback mode, practically the reverse operation occurs of that described in the record logic system. The recovered playback data signals, consisting of differentiated pulses, are reconstructed by a level detector similar in operation to a Schmidt trigger. The level detector output is a square wave having a relationship to recovered pulses as shown in Figure 11. The block diagram of the playback logic system is shown in Figure 12.

The recovered data is strobed by means of the output of the bit counter similar to that during recording. Differentiated bit sync is used to eliminate possible coincidence effects. The three data track gates are wired in an OR configuration, thus the readout data is put back in serial arrangement. Because of the 90° phase relationship of the tape signal to the clock reference made necessary in the operation of the phase-locked loop, some means must be provided to eliminate this

phase error. In addition, the jitter present on the reconstructed signals must be eliminated.

The signals at the outputs of the playback OR gates are used to SET and RESET a flip-flop which in turn programs the toggle steering points of an output flip-flop. The output flip-flop is toggled from the bit sync line. By this means the data readout is fully serial and synchronous with the incoming bit and word sync. Since the 90° phase slip is present, the output shift register also eliminates the slight delay or time shift introduced by the phase-locked loop.

A follow-up gate is used so that the NRZ output line will go high whenever the system is commanded to go record or slew. This added inhibit feature effectively keeps extraneous pulses off of the output line whenever the machine is not in the playback mode.

4. Control Logic System

The external command system simulates the spacecraft system which controls the recorder and has override controls to facilitate testing. This system receives command signals from the spacecraft through bit rate command lines. These command signals are as follows: (1) Record, (2) Playback, (3) Slew, and (4) Stop.

A two-phase motor drive is obtained from a series of flip-flops and gates. The motor drive signal is derived either from the VCO for the playback mode or from the 1512 cycle per second clock line for the record mode. The signals enter the OR function in the mode selection gate. It is then possible to derive output signals which when counted down through the motor clock frequency divider will be the correct frequency for the intended mode. Another series of OR functions are used to pick up various points along the motor clock frequency divider. These receive commands from speed control gates so that selection of the proper motor clock can be initiated from the data rate selection lines. A group of flip-flops are used as a two-phase generator and receive their inputs from the motor clock frequency selector. The outputs of the flip-flops feed the motor drive amplifiers.

Inhibit lines derived from various logic functions within the control system are used to shut down the motor power amplifiers when not in use and for making the energizing output line go high when in the playback mode. Other control functions derived from this system provide switching commands for the programmable power supply, integrator time

constant control, and gain switching stages in the playback amplifier. In addition, signals from the frequency divided motor clock and other delayed inhibit lines are extracted from the control system for use in the end-of-data system.

5. End-of-Data System

The function of the end-of-data system is to supply an output pulse whenever a block of previously recorded data has been played back. Every time the recorder changes from record to stop or playback, an end-of-data code is recorded on the sync track. This is accomplished by counting down the record motor clock signal and feeding it into the sync track record gate. REL Dwg. 1737-55 shows the end-of-data system. This gate also receives a time delayed signal derived from the frequency divider and a signal from the record command line ES-1. The output of the end-of-data gate is fed to the sync track record flip-flop.

Upon going from record mode to any other mode, including off, the end-of-data marking code overrides the data signal and is recorded on track 2 of the tape. The end-of-data code burst is readily identifiable by the end-of-data detector because the end-of-data code has a repetition rate greatly in excess of the tape sync signal.

When the end-of-data signal is played back, it is fed through a counter which receives a dc reset pulse from the word sync counter system.

The end-of-data detector will not count the low speed signals, such as tape sync signals, because it gets reset at the end of every word. It can only develop its count-to-three pulse when fed by a signal of a faster repetition rate, such as the end-of-data code. The end-of-data detector output gate is fed an inhibit signal so that it will not deliver an output signal when in the record mode. The follow-up one-shot is triggered from the end-of-data detector output. This one-shot delivers a 50-millisecond end-of-data pulse ES-4.

D. Multispeed Phase-locked Loop Control System

The data to be played back to the earth upon command must be synchronous with the spacecraft clock system. A simple free-running transport would require that the tape readout data be stored in an appropriate buffer shift register prior to transmission. This shift register would then be interrogated by the spacecraft bit pulse, reading out the stored tape pulses bit by bit. This method imposes severe limitations on the flexibility, size, and stability of a system. It would be far better to have a recorder which would provide

synchronous readout when supplied appropriate word and bit signals.

This is done in the 10^7 recorder by the inclusion of a phase-locked loop tape speed control. In this system, word, bit, and data are fed the recorder circuits during the record mode. A word sync signal, derived from a combination of word and bit signals, is recorded on a separate track. Upon playback, the tape sync signal is compared in phase to the satellite clock sync. The resultant of this comparison is used to control the average speed of the motor driving the tape. Therefore, the bits read out of the data tracks will have a rate dependent upon the reference clock. Further use is made of the word and bit signals in a simple buffer shift register to eliminate jitter components from the recovered data pulses. Since all reconstruction of tape signals and the speed of the machine is referenced to the satellite clock, the end result is NRZ data in perfect synchronism with the reference clock.

A complete study was made of speed control both on the breadboard transport and the prototype machine. This was time consuming because of the four rates required. Motor torque had to be varied during these tests, since the mechanical system dynamics played an important role in the stability of the system.

Originally, the performance of the servo was very good when tested with the breadboard tape transport using breadboard motors. All four rates were tried, and some instability was noticed, particularly when using high loop gain. Some of the instability may have been due to externally generated noise which shock excited the system.

At about this time in the development of the 10^7 bit recorder, JPL notified REL of the new increased playback rates of 84, 168, 336, and 672 bps. This necessitated some back-tracking with respect to the development of the phase-locked loop control system. Initial breadboard tests at the new rates showed no major problems, and the servo system was developed for the new rates.

Further work was done with the prototype tape transport. Again, all four rates were tried but more time was consumed in this study because its success would have a direct effect upon the finalized system. Whenever attempts were made to operate the system at high VCO deviations, serious instability was found as evidenced by severe hunting. This is the equivalent of high-loop gain in conventional servo systems. The hunting could be eliminated by a reduction in gain but at a sacrifice of lock-in time. Also, very little reserve gain would be available to allow for normal temperature and torque variations.

A single stage lag filter was then tried, and the results were quite good. The constants were chosen while operating at high loop gain, ±15% deviation, at a rate of 672 bps. The filter time constant was selected to allow peak response at the low frequency end of the servo pass band -- below 10 cycles. REL believes that by extending system response into the higher frequencies would cause more trouble, since flutter components have most of their energy above 14 cycles per second.

An interesting observation was made during this investigation period. It was found that flutter was increased when the servo loop was closed. Nominal open loop flutter was usually 1.3%; closing the loop caused an increase of greater than 2:1. However, by shifting the phase characteristics of the system using a filter of phase limited design, the flutter could actually be reduced during closed-loop operation. Filter requirements became less critical at lower readout rates. Thus, efforts were primarily directed in achieving stability at 672 bps.

One of the most difficult problems was caused by capstan "stiction" or the slip-grab effect. Flutter pulses produced by this phenomenon tend to be quite rapid and have steep sides. Total energy content may not be great due to the small area under the wave form,

but continuous pulsing can cause the servo to excessively correct. If the system has a positive feedback area, it will eventually be shock excited into oscillation. A temporary step taken to eliminate stiction was to stop the downstream capstan, thus eliminating the rough surface finish. Stiction effects are quite a serious problem in many other machines.

The inclusion of a filter having two roll-off break frequencies was later installed in the servo system. This filter provides exceptionally good results, since it shapes the frequency response of the loop so that large levels of flutter can be accumulated without causing serious over-correction, even when using high values of loop gain. The response curve of the loop filter used in the recorder shipped to JPL is shown in Figure 13.

1. Gated Integrator

A gated integrator system is provided in the phase-locked loop control system to convert the relative phase angle of two signals to provide a dc voltage which could be used to control motor speed. The gated integrator was selected over conventional phase detector and filter systems because the latter: (1) have high power consumption, (2) have inadequate linearity, and (3) are often restricted in dynamic operating range.

The reconstructed tape word signal and the word sync signal from the recorder logic system are fed into the selected phase comparator at the input of the gated integrator circuit. There are four phase comparator circuits in the phase-locked loop control system, one for each tape speed. The output of the phase comparator (diode gate) is a pulse having a width equal to the phase difference of the two input signals. The gated integrator converts the phase change of two signals to a voltage change that is fed back to the VCO which is tuned to the center frequency. The VCO then shifts frequency in a direction as determined by the integrator output. This signal is then fed to the motor to increase or decrease speed, thereby effecting synchronism.

The square wave output of the phase comparator is fed into the integrator. Figure 14 shows the block diagram and REL Dwg D1737-69 shows the circuit of the gated integrator.

The integrator circuit includes a silicon-controlled switch (SCS) used to provide rapid reset rise time. The reset pulse causes a reduction in anode gate voltage which fires the silicon-controlled switch. The SCS cathode

is connected to the mid-point of a capacitor divider network through a hold-off diode. Firing of the SCS causes the mid-point of this network to rapidly rise in voltage until the cathode voltage reaches a point to extinguish the SCS. This voltage is determined by the selection of the voltage divider resistors which determine the SCS operating point. The hold-off diode presents the stored charge from leaking off.

Rundown is accomplished by applying the resultant from the phase comparator to a gate transistor. Figure 15 shows a typical plotted integrator output wave form. When the gate transistor is conducting, the voltage at the mid-point of the capacitor network discharges at a constant rate which is determined by the values of the resistors in the collectors of the integrator time constant switches. There are four such switches provided to accommodate the four different playback rates. Voltage rundown continues for a time interval determined by the width of the output pulse of the phase comparator. This integrated voltage will hold at this level until another reset pulse occurs which returns the output to its original reset value. The high output impedance of the

integrator is converted to a low output impedance by means of a Darlington amplifier having a very high current gain. This amplifier, along with the proper selection of hold-off diodes, produces a very low output droop during the reset and hold periods of the integrator. Typically droop is less than 5% over any three-word period.

Assuming a tape speed of 0.07 ips, the signal recorded on the sync track will be a square wave having a 50% duty cycle, 1 cycle per 3 words and a frequency of 4 cycles per second. The signal which is generated by the recorder logic system at 84 bps has a width of 35.75 ms. Adjustment of the individual timing resistors is done with each of the four rates using the full pulse width (35.75 ms). The resistors are then adjusted to provide a maximum integration to 5 volts. This is then repeated for each one of the four playback rates. Because the system is set up to run with the tape and sync pulses at 50% coincidence, this will yield 1/2 of the full pulse width or an integrator output voltage of 10 volts. This is the "in-sync" condition.

If the pulse of the recorder sync track occurs late, the integration period is shorter, and the integrator output voltage averages less than +10 Vdc. The VCO which controls the frequency supplied to the playback motor, and therefore the tape speed, increases so that the next sync pulse on the tape will occur earlier. Thus, the tape speed and playback frequency are varied according to the relative phase angle between the external word sync and the sync extracted from the tape.

If both pulses that are to be compared in phase have the same duration, a plot of the overall control characteristics versus relative phase angle shows two immediately adjacent areas, one representing the negative feedback and the other a positive feedback condition. As the phase changes rapidly during lock-in, this condition will cause overshooting and general difficulty in achieving lock. If, however, these positive and negative feedback areas are separated by lengthening one pulse with respect to the other, phase lock is achieved in the least amount of time. Ideally, one of the signals will have a 50% duty cycle, provided in this case by the tape sync.

2. Voltage-Controlled Oscillator (VCO)

The output of the gated integrator is fed through the low pass filter network to the VCC. REL Dwg D1737-69 shows the VCO circuit. The basic circuit of the voltage-controlled oscillator originally designed for the 10^6 bit recorder under JPL contract 950105 was not sufficiently stable for use as a servo reference in this 10^7 bit recorder. Frequency drift with temperature of the 10^6 bit recorder was on the order of +120 cycles at 85 C and -72 cycles at -15 C.

A differential type of compensator is used in the 10^7 bit recorder. Typical drift is on the order of 0.4% at 85 C and 0.27% at -15 C, both in the positive direction. The circuit was temperature cycled at least ten times with no indication of departure from the original results. Transistor replacement showed no severe changes due to parameter spreads. However, parts selection was quite critical and could be a problem for flight hardware. Some of the conclusions reached from using this type of VCO are as follows:

a. very good temperature stability and very low hysteresis,

b. critical component selection in at least three circuit positions,

c. no data existing concerning long-term drift,

d. fairly good stability with power supply changes,

e. drift and emitter follower not yet compensated,

f. considerable flexibility in choosing temperature/frequency deviation.

The VCO consists of a silicon-controlled switch working as a relaxation oscillator, similar to a unijunction configuration. An R-C network is used to determine the frequency of oscillation. The frequency of the VCO is varied and is determined by the potential on the base of a transistor which varies the resistance component of an R-C network. The center frequency of the VCO is adjusted for 1512 cycles per second with a 10-volt input.

To provide temperature stability, the variable impedance transistor is in the configuration of a differential amplifier, the other half of which merely supplies reference voltage. Frequency drift, as a function of

increased transistor leakage, is compensated. Resistance networks are used between an emitter follower and the control transistors to get the required frequency deviation at the stabilized operating point. Linearity of frequency deviation is better than 0.1% over the operating range.

E. Playback Amplifier

The major problem associated with the low playback speeds required of the 10^7 bit tape recorder is low voltage output at the head at very low frequency. To obtain a stable output for the level detector, the conventional R-C coupled amplifier system was abandoned. The reasons for this were that direct coupling would give linear response down to almost dc, would eliminate bulky interstage coupling capacitors, and would eliminate interstage coupling capacitor leakage. Four playback amplifier circuits are provided, one for each track. This discussion is typical of all four circuits. REL Dwg E1737-57 shows the playback amplifier circuit.

Initial efforts were expended in investigating chopper amplifiers. These efforts were partially successful, but it appeared that the ability of the choppers were somewhat magnified by the manufacturer.

Extensive studies were made on the ability of the playback amplifier to handle the 8:1 change in amplitude and frequency. The four playback rates require that the playback amplifier be capable of handling a head output voltage dynamic range of 18 db. As the rate is increased from the lowest rate, an output voltage-frequency relationship of 6 db per octave results. The preamplifiers used in the 10^7 bit recorder are capable of handling this dynamic range. However, it was necessary to provide some means of gain control to prevent successive voltage stages from overloading.

An attempt was made for a 6 db per octave filter to maintain a constant output voltage and prevent overloading. Unfortunately, passive filters cannot be easily designed to handle such a wide range of signal frequency and still have the linear phase transfer which is needed for proper signal reconstruction. The definition of the record signal would suffer causing an error. A Butterworth filter was breadboarded. While it would have been suitable, the dc drift introduced by the necessity of direct coupling the filter amplifier could not be tolerated. Filtering was not practical.

1. Preamplifier Stage

The signals present at the head terminals are differentiated NRZ pulses. These

must be amplified before the original NRZ data can be reconstructed. The preamplifier stage is a straightforward differential, direct-coupled amplifier -- reference REL Dwg D1737-59. This is a two-stage, push-pull amplifier with extensive feedback to make the amplifier stable over the required temperature range. The advantage of this type of circuit is that it permits a wider selection of parts. Standard stocked transistors and other components are used.

The playback system was developed with a high ac gain and a low dc gain from a temperature stability viewpoint. From a push-pull head input, a single-ended output signal is derived.

The reason for the differential system is that due to low signal levels, common mode noise must be eliminated. Much of this noise is generated internally by the square wave motor system. The design includes complete shielding of the playback amplifier, motor power amplifier, common power supply leads, and ground leads. Considerable care in routing the dc power

distribution leads keeps motor noise out of the amplifier. The differential system of the preamplifier stage deters noise -- the signal-to-noise ratio is greater than 40 db.

As may be seen in REL Dwg D1737-59, the preamplifier system has an R-C network to provide high frequency roll-off.

2. Drift Corrector

The drift corrector circuit corrects dc drifts resulting from thermal variations in the preamplifier circuit. The single-ended output of the preamplifier stage is fed into the drift corrector. REL Dwg D1737-60 shows the drift corrector circuit.

The drift corrector is a two-stage, direct-coupled amplifier. Both stages are of a differential design. Again, loop feedback is used. However, one leg of the push-pull feedback loop contains a shunt capacitive reactance element which bypasses audio frequency. This keeps the signal gain high yet is not passive for dc drift. The dc gain is reduced to nearly unity. The result: high ac gain with little dc gain. The single-ended output of the drift

corrector is fed to the main amplifier circuit.

3. Main Amplifier Circuit

The main amplifier has two push-pull stages and is a direct-coupled amplifier with considerable push-pull feedback. However, this sytem differs from the previous stages described in that it has three feedback switching stages. The amount of feedback is controlled by the relationship of R6 and R11 as shown in REL Dwg D1737-61. Since it is necessary to change the gain with each playback rate, the switching stages can be switched from the command logic to correct gain for each rate.

If a 1 is put on any line, the associated stage will conduct. The recorder is supplied by four logic lines to indicate the bit rate at which the recorder should operate. As the tape speed increases from 84 bits per second to 336 bits per second, the feedback increases, thus maintaining constant output at all tape speeds. When a 1 is applied at 672 bits per second, automatically a 0 appears on the other three speed lines -- none of the three switches are operating.

Gain adjustments are made in the following manner:

a. Gain is adjusted to provide 14 V peak-to-peak output when operating at 672 bps.

b. Step a is repeated at 336 bps.

c. Step a is repeated at 168 bps.

d. Step a is repeated at 84 bps.

When the system is in the record mode, the playback amplifiers are in operation with gain control only at 336 and 672 bps. The remaining two record speeds have no gain control effect on the amplifier and the output wave forms are considerably distorted. This is due to overloading the amplifier.

Figure 11 shows a typical amplifier output signal wave form with dc offset voltage under normal conditions. Figure 16 is a frequency response curve of the playback amplifier system.

4. Level Detector Circuit

The output of the main amplifier is a differentiated NRZ pulse that is fed into the level detector. This is a modified Schmidt trigger using a complimentary configuration -- see REL Dwg C1737-62. The

pulses recovered from the tape are amplified to a level suitable to conversion to NRZ. The REL design uses slope detection in which the pulse changes the state of a flip-flop (Schmidt trigger) about half-way up the leading edge. Figure 11 shows the voltage wave form, with values of the level detector circuit.

Other approaches of data reconstruction were attempted. It was originally believed that a peak detector could be used for data reconstruction. Difficulties presented by high power consumption and the necessity for some possible component switching precluded the use of this system. Contrary to the common belief that peak detectors are widely used and that typical circuits exist throughout current technical literature, REL encountered considerable difficulty in obtaining any information on peak detectors. As a matter of interest, REL has developed a workable peak detector since the time of this initial investigation.

The approach used in the 10^6 recorder could not be used because it offered very little control over the selection of

operating points along the tape pulse wave form. This method of slope detection is quite susceptible to noise.

5. Power Decoupling Circuit

It is necessary to use a power decoupling circuit because there is considerable noise on the ± 6-volt lines. This noise is in the pass band of the amplifier system. Conventional R-C decoupling networks were found to be inadequate for this purpose.

The power decoupling circuit functions as a simple series voltage loss circuit with operating points derived from a Zener diode operating off of a 20-volt line. REL Dwg C1737-58 shows the power decoupling circuit. This circuit has three major functions as follows:

a. takes the ± 6 volts available to the system and drops it to ± 4 volts,

b. isolates ± 4-volt input to preamplifier from any noise present in the ± 6-volt line,

c. accomplishes some degree of regulation per the tolerances in the JPL specification.

F. End-of-Tape Sensor Circuit

The end-of-tape sensor circuit was designed to eliminate noise from the end-of-tape signal -- reference REL Dwg C1737-68. The output pulse of the end-of-tape sensor may have noise spikes due to discontinuity of the gold.

The Schmidt trigger used in this circuit is conventional except for the capacitive time constant at the input which provides ac hysteresis. Upon the initiation of the end-of-tape pulse, there will be no change in state of the Schmidt trigger until C1 has discharged to a new net value. The Schmidt trigger then fires. Any spikes of noise will not cause the Schmidt trigger to return to its normal state until proper time has elapsed. Since the required time is greater than 100 ms, no output will occur with spikes having a deviation less than this. Therefore, noise has been eliminated from the end-of-tape signal. The Schmidt trigger returns to its normal state following the elapsed time determined by the aforementioned time constant. This triggers the one-shot, and the output is ES-5 - a go-to-zero pulse.

G. Motor Drive Amplifier

In the interest of efficiency, it is necessary to operate the motor from a square wave power source.

In order that REL would not waste power, an efficient and reliable drive amplifier was developed for the motor which operates off of the output of the programmable power supply. There are two motor drive amplifiers: one for playback motor (REL Dwg D1737-72) and one for the record motor (REL Dwg D1737-71). This discussion of the motor drive amplifier is for one-half of the amplifier; the other half is identical.

The amplifier consists of dual bridge-connected power switches. The two-wire input to one phase of the amplifier is a conventional logic output square wave. This provides a push-pull drive system. The signal is diode coupled to a pair of buffer transistors. This buffer output is then diode coupled to a pair of transistors functioning as drivers. The output of the driver stage is fed to two coupling transformers which, in turn, supply base drive current for the bridge-connected output stage. The output of the last driver stage is fed to one phase winding of the motor. This same circuit is used for the other phase winding.

Since the buffer driver stages are direct-coupled, there is a possibility that if the drive signal is lost, a condition could exist whereby one-half of the driver system may come to quiesence in a heavily conducting state. This could cause heavy

current to flow through the primary of the driver transformer and possibly result in serious damage to the transformer. To prevent this from happening, an inhibit line was inserted into the sytem which, when made high ($\pm$ 6 volts), will cause the buffer stages to conduct. This effectively cuts off the driver stage.

H. Packaging of Associated Electronics

One of REL's earliest goals was to have much of the associated circuit elements housed within the recorder transport assembly. Owing to the complexity of the evolved system, this was not feasible. The use of standard JPL breadboard logic cards necessitated that the bulk of the logic and control systems be housed external to the recorder proper. The electronics of the 10^7 bit recorder are housed as follows: the playback preamplifiers are integral with the recorder transport. All other circuit elements are housed in a table-top rack assembly which uses plug-in JPL card trays.

The low level output from the heads requires that noise be kept out of the circuit. Motor drive voltages are used which have frequencies within the tape signal pass band. Since two separate systems occur and an interconnecting cable is used, the best way to handle these low level head signals is to build the preamplifiers into the transport housing.

This resulted in a packaged four-channel preamplifier assembly which is located below the motors on the rear of the transport. The head leads are quite short and go directly into this shielded amplifier package. The output level of these amplifiers is on the order of 2 volts, a level which can be fed over the umbilical cord without risk of noise pickup.

The rack assembly contains the following active components:

Control logic circuit: 15 ea Flip-flop Cards
22 ea AND Gate Cards
2 ea Driver Cards

Record and playback logic circuits: 15 ea Flip-flop Cards
22 ea AND Cards
6 ea Driver Cards

2 ea Programmable Power Supply Units

1 ea Dual Motor Drive Amplifier

1 ea Playback Main Amplifier Assembly (4 Channels)

1 ea End-of-Tape Sensor Pulse Shaper Circuit.

Other circuits, such as record head drivers, VCO, and integrator, are mounted on JPL type plug-in cards and are housed in the tray assemblies.

REL could not pursue an extensive packaging program with the funds available. The original agreement

was that Texas Instruments, Inc. (TI) would package the electronics system. At the time TI was preparing a quote for the electronics package, JPL notified REL of the cutback of the Mariner funds. This precluded any further study of the electronics packaging problem.

V. TEST PROGRAM

The "Interim Test Plan Type Approval Testing of 10^7 Bit Magnetic Tape Recorder" (Appendix II) was used as a basis for testing the 10^7 bit tape recorder. This document lists the specific environmental tests performed at JPL and lists certain functional tests performed on the mechanism before, during, and after the environmental tests. This interim test plan and the test fixtures used in testing were approved by JPL. All circuits were tested prior to mounting in the breadboard cabinet.

JPL furnished REL with all of the circuitry for the digital logic functions in the form of plug-in cards. These cards were used exclusively in the testing of the 10^7 bit tape recorder and were not modified in any way by REL.

A. Environmental Tests

Only one environmental test was conducted at REL -- temperature extremes. All other environmental tests, such as shock and vibration, were run at JPL. At a meeting held in April, 1963, JPL and REL mutually agreed that the thermal shock and mechanical shock environmental

tests would be conducted at the end of the development program. This decision was made because these tests could be destructive. At that meeting, some environmental tests were waivered: thermal bacteriological sterilization test and rf interference test.

1. Vibrations Tests

The first vibration test conducted at JPL was with plastic covers in order that the transport could be viewed during vibration. A problem arose at the time of the first scheduled test -- the recorder did not fit into JPL's hex box designed for accepting the recorder during vibration testing. Sufficient space had not been allocated to accommodate possible package excursion during vibration. A new vibration fixture was designed and built, thereby insuring that the c.g. of the recorder would be such that equal loads would be presented to each of the shock mounts. This new fixture was of a cantilever design. Test results with the shock mounts in this configuratio were satisfactory.

Vibration tests were then reconducted using metal covers. The results were good except that one 4-40 nut came loose. This was reassembled and loctited. Flutter was checked

after each vibration test and was satisfactory.

As a result of the problems encountered with the tape binding at low temperature during the first set of tests at JPL, a reel brake was installed in the transport. Paragraph V.D. of this report discusses the first tests at JPL in greater detail. A special vibration test fixture was fabricated by REL and vibration tests conducted here to determine vibration effects on the reel brake. The special test fixture was necessary because a slide plate attachment for REL's vibration equipment was not available.

The machine was vibrated in three mutually perpendicular planes from 10 cycles to 1500 cycles with 5 g's rms input to the shake table. The results were good with satisfactory flutter readings after vibration in each plane and no severe tape looping occurred. The machine appeared to be satisfactory for further testing at JPL.

The second series of tests at JPL were conducted in the same manner as the first tests, using plastic covers. The results of the vibration test were again satisfactory.

2. Acceleration Test

During the first series of tests at JPL, the acceleration test was conducted with metal covers and in accordance with JPL specification 30257. The machine was mounted in the same test fixture as that used in the vibration test except it was mounted on the centrifuge arm. The recorder was operated after the acceleration test and performance was good. Flutter was also checked and was satisfactory.

The recorder was again subjected to acceleration tests during the second series of tests at JPL. The test procedure and results were the same as the first JPL tests.

B. Operational Tests

All of the operational checks listed in paragraph 5.4 of the Interim Test Plan Type Approval Testing of 10^7 Bit Magnetic Tape Recorder were conducted at room temperature, and the results were satisfactory. These operational checks included: Recording, Playback, Coding, End-of-Data Detection, End-of-Tape Detection, Pressure Transducer, and Temperature Transducer.

C. Performance Tests

1. Flutter

Flutter refers to tape speed irregularities evidenced by a variation of the playback signal frequency. Flutter is generally applied to tape speed

change rates in excess of a few cycles, while WCW is used to denote a slow change in speed occuring below a few cycles per second. In a typical machine, the cyclic components of flutter, such as caused by bearing defects and shaft runout, can be identified by their relationship to the known period of rotation of these parts. Flutter data is used as the mechanical criteria for any system, analog or digital. Flutter will affect a digital system in quite a unique manner, since its relation to jitter determines the area over which a phase-locked speed control will work and determines the total data sync stability.

In a digital machine, it is more common to refer to the effects of flutter as jitter, since pulse position stability is involved.

Measurements of flutter require that the machine reproduce a signal output of several thousand cycles per second with a practical frequency demodulation by a sub-carrier discriminator. The output of the discriminator, indicating instantaneous speed deviation, is generally plotted by means of a Visicorder so that individual sources of flutter may be determined from their respective repetition rates coupled with the knowledge of the various rotational speeds. It is customary to refer to flutter in

terms of percent deviation from the mean speed.

Initial tests of the system indicated that the transport had high flutter. An unusually high flutter amplitude was traced to the downstream capstan, against which the tape is supposed to slip smoothly. The problem was aggrevated by the pull exerted by the tape in the reel assembly as it winds. This flutter did not cause erratic functioning of the phase-locked loop and further tests were conducted. Later replacement of an associated capstan bearing assembly reduced flutter to the 1% level.

Flutter was measured by programming a steady state frequency on an entire tape using a Hewlett-Packard Model 211A square wave signal generator. The output of the playback amplifier was fed to the frequency discriminator EMR 189D. The output of the discriminator was then fed through suitable low pass filters to the Visicorder.

The results of this test showed that the machine had a peak-to-peak flutter value of 1.4%. A typical Visicorder chart of the flutter tests is provided in Figure 17.

2. Amplitude Modulation

The tape used for the flutter test was played back and the signals viewed on a Tektronix oscilloscope 503. By reducing the sweep rate of the scope

to show the playback signal envelope, amplitude modulation will appear as modulation of the envelope. The percent modulation can then be calculated.

The results showed an amplitude modulation at all times of less than 5%.

3. Jitter

The maximum jitter error which can be tolerated is determined by the relationship of bit interval to data pulse interval. Usually about 10% jitter can be permitted in a typical synchronous system. The combined effects of skew and gap scatter reduce the effective usable width of any recovered tape pulse. In order to achieve reliable synchronous readout, it becomes necessary to set up a system so that considerable time shift of the tape signal can be tolerated before errors occur.

Strobing of data bits during quiescent periods rather than at leading or trailing edges is an effective method of insuring reliable operation.

Jitter was measured at REL by two methods. For the preliminary investigatory testing, with no logic circuitry available, a square wave was recorded on the tape through the record head drivers. The same square wave generator used in the flutter test was used in the jitter test. The differentiated signal

was played back using a positive-going pulse to trigger the scope, while at the same time the relative time shift of the negative-going pulse was observed.

The second method used for testing jitter, with logic circuitry available, was similar to the first method except the phase-locked loop system was used. The reference signal was the bit sync from the logic circuitry. Percent jitter was a measure of the maximum $\pm$ deviation from a mean position of tape data pulse with respect to the bit sync.

The results showed a maximum jitter of 10%. Figure 18 is a graphical representation of typical jitter.

4. Head Gap Scatter and Skew

a. Head Gap Scatter

Gap scatter is a characteristic determined by the mechanical tolerances in the manufacture and alignment of the head assemblies. Gap scatter is a measure of the amount of misalignment of the gap positions as it occurs in co-planar, interleaved heads.

This test was conducted by recording the same signal on all tracks simultaneously by feeding a square wave signal into the four record amplifiers tied together. A Tektronix

dual-trace oscilloscope type 531 with type CA plug-in was used for these measurements. Only one of the four tracks was selected to trigger the scope. Extreme care was taken in maintaining as accurate as possible the trigger point along the slope of the waveform. One of the remaining three signals was also displayed. With this method, any fixed difference in position of the pulses as a function of gap scatter (gap misalignment) could be seen. This time difference was then readily converted to microinches, practical units for expressing gap scatter. This procedure was repeated using all four tracks as the reference signal. A typical value of gap scatter is 200 microinches based on track 2 as a reference. Figure 3 gives other typical values of head gap scatter.

b. Skew

Skew is a shift in position similar to scatter except that it is of a variable nature. Skew appears as a sinusoidal time shift, and the skew error is measured from the scatter error as a reference. The same system was used for measuring skew that was used for measuring scatter. A typical value of skew is ± 120 microinches. Figure 3 also gives other typical values of skew.

c. Combined Effects of Gap Scatter and Skew

The combined effects of gap scatter and skew cause a bit cell displacement of approximately 350 microinches. This is based on a normal bit cell width of 0.002 in. Since the gap scatter is a fixed displacement, the resulting 120-150 microinch shift due to skew effects only amounts to 10% of the bit cell width. This reduces the usable width of the bit cell but not to the extent that operating range is affected.

5. Acceleration/Deceleration Time

The acceleration/deceleration test was run at all three environmental conditions: -10 C, 25 C, and 80 C. A suitable signal was recorded on the tape to provide an available signal for playing back. The Visicorder was set up with two galvanometers. One galvanometer was fed by the motor power source in such a manner as to show deflection whenever the motor was turned off or on. The other galvanometer received its signal from the playback amplifier. With the Visicorder on, the motor was allowed to reach speed, then shut off.

The playback head and a line carrying dc whenever the record motor was on were connected to two respective channels of a Visicorder. The amplitude

of the pen displacement caused by the reproduced signal was indicative of relative tape speed. Displacement of the other pen indicated the time at which the motor power supply was removed. A typical chart of the output of the acceleration/deceleration test is reproduced in Figure 19. This shows tentative maximum acceleration and deceleration times at -10 C and minimum voltage of:

record mode -- 0.4 sec accel
1.0 sec decel

playback mode -- 0.35 sec accel
0.52 sec decel.

6. Motor Load

The playback motor was functionally tested for power consumption, output power, and bearing losses at temperatures of - 15 C, room, and 80 C prior to installation into the transport. Power output and input power were measured at no load, maximum load, and stall at the four speeds of 945, 1890, 3780, and 7560 rpm and at ± 10% of each speed. One motor was calibrated to indicate its operating load in the transport to determine how much power the transport demanded.

The record motor was checked in the same manner as the playback motor, except it was not tested at

± 10% of its normal speed. Appendix I includes a series of environmental performance data sheets for the motors.

7. Power Consumption

Power measurements were taken only on the four dc power lines. Power consumption on the 2400-cycle line was not measured because of noise problems which could influence the readings. The results of the power consumption tests are given below.

Motor Power Based Upon True Motor Requirements Modified By Measured Power Supply Efficiency

	Minimum Powers (1)	Maximum Power (2)
Record	0.798 watts	4.55 watts
Playback	0.847 watts	3.36 watts

(1) Minimum power at -10 C and maximum speed

(2) Maximum power at -10 C and minimum speed

DC Line Power Consumption

Line (volts)	Record Mode (ma)	Power Consumption (watts)	Playback Mode (ma)	Power Consumption (watts)
+6	150	0.900	260	1.560
-6	27	0.162	32	0.192
+20	57	1.140	64	1.280
-20	3.8	0.076	3.8	0.076

8. Phase-locked Loop

This test was designed to analyze the performance of the integrator and to determine the VCO output limits. If the phase-locked loop system acheives the lock condition, the integrator output is at 10 volts.

The first investigation of the phase-locked loop system was done using the breadboard transport. Breadboard electronics were used in record and playback circuits but the integrator and VCO were similar to the prototype. This test revealed satisfactory low speed operation of the servo but indicated some instability at the higher rates.

The next test series was conducted with the prototype transport. Data was obtained showing excessive jitter -- over 10%. The most serious jitter occured at the highest rate, 672 bps. Following the filter installation, a proglonged series of tests wre performed to determine overall system performance using the phase-locked loop.

9. Leakage Rate

Based upon data received from the Parker Seal Company, the maximum acceptable total leakgae rate is 1000 cc per year at elevated temperatures. This 1000 cc per year divided by the total seal length of approximately 72 inches gives the leak rate per

inch -- 13.9 cc per inch per year. For room temperature operation, the maximum acceptable leakage rate is 300 cc per year total.

The CEC Mass Spectrometer type 24110A leak detector was used in this test. The recorder, with covers secured, was evacuated to 10 microns, then back-filled with dry nitrogen. The unit was again evacuated to 10 microns and then back-filled with a 90-10% mixture of helium and nitrogen to a pressure of 20 psia. (When the fitting is removed to plug the fill hole, this pressure reduces to one atmosphere.) During the investigatory stages of this program, some measurements were taken using 100% helium.

During the first tests conducted at JPL, a 90-10% mixture of helium and nitrogen was used. The initial tests performed at JPL were with unqualified covers, since the vendor had not yet completed his evaluation of previous failures. Initial readings at JPL showed an enormous leakage. The unit was helium probed to determine the origin of the leak which was found to be a leaky connecter in the main plate. The connecter assembly that caused the leak was through a blind hole in the side of the main plate. This hole was originally planned for use with the vibration isolators and now no longer used. The hole was plugged.

Subsequent leakage tests showed that the leak rate was at its proper level at room temperature -- about 4 cc per inch per year. The unit was leak checked after each vibration test in each of the three planes with the same satisfactory results.

Leakage tests were also conducted at the temperature extremes. The system was placed in a thermal vacuum chamber, and the temperature dropped to -10 C. This was done in a bell jar with a pressure of 10^{-5} mm (0.01 microns) of Hg. Unfortunately, the leak detector readings taken were completely invalid because of excessive residual noise.

The JPL tests were temporarily halted due to a JPL vacation shutdown, and the REL engineer returned home. When JPL resumed the tests, problems were encountered which indicated apparent excessive leakage. When the machine was returned to REL, this problem was examined along with the other mechanical problems that developed at JPL.

To help solve the leakage rate problem, the leaky screw hole in the side of the recorder main plate was epoxy sealed using an epoxy recommended by Ardel. Helicoils were installed with the thought of eliminating the long stainless steel through-plate screws originally used. A shorter overall screw length is now being used with much less thermal

expansion. Preliminary tests have borne out this theory.

The basic configuration for the gas-fill hole plug has been changed with emphasis on anti-rotational devices for preventing O-ring galling during the sealing operation. The device now installed is the same as that used on the 5×10^6 bit recorder. With this device, it is possible to get long term stability from the O-ring bore configuration.

Prior to returning the machine to JPL, a series of leakage tests were conducted by Ardel Corporation of Glendale, California. The results showed excessive leakage at both room and elevated temperatures when using the metal covers. Consequently, JPL and REL agreed to run the temperature extremes test at atmospheric pressure only. The thermal vacuum test was waivered by JPL. All tests were run with plastic covers.

D. First Series of JPL Tests and Resulting Design Changes

The tape recorder failed the JPL testing program conducted in June, 1963, due to a bound tape problem attributed to the reel design. This was thoroughly investigated at REL, and it was determined that the tape reel spilled tape whenever sufficient momentum was applied to the recorder to cause the reel to spin. The wire guide that was used during the JPL tests was

defective and caused permanent damage to the tape. The two major problems were that the tape would spill out of the tape exit point forming a loop which would snag on the wire guide and the tape would cinch around the reel hub causing a pinching effect which prevented the reel assembly from moving. These problems, when coupled with high temperature softening of the tape, caused serious damage to the tape pack.

The original approach for solving these reel problems consisted of lightening the reel hub and cover. A felt damping pad was also used to minimize any free spinning of the reel when under the influence of shock or vibration. This solved the problem, but for reasons of reliability was not permanently installed.

A brake mechanism was installed in the machine which mechanically clamps the reel and prevents it from turning. The brake mechanism contains an electromagnetically-operated latching solenoid. The solenoid carries an arm equipped with a pointed finger which seats in a knurled area cut into the extreme radius of the reel cover. With this method, it is possible to pulse the brake on or off using a standard 20-volt relay circuit. The 10^7 bit tape recorder was reworked to install this brake into the system.

Since it was felt that the tape used in the 10^7 bit tape recorder suffered some mechanical instability,

particularly at the high temperature extremes, Minnesota Mining and Manufacturing LR1353 tape was installed in place of the usual LR1220, with an improvement in high temperature performance as discussed in paragraph III.D of this report. Also, the capstan-to-capstan speed differential was decreased from 2.5% to 0.2%. This reduced total tape tension, thereby reducing tape "stiction." The overall result is a drive system in which the tape is positively driven, using only a slight differential to achieve proper tape tension across the heads. The increased tape drive belt pressure will further isolate tape reel distrubances from the immediate capstan area. Test results indicate a reduction in flutter, particularly tape "stiction" spikes, which were formerly a source of severe trouble.

This reduction in capstan-to-capstan speed differential appeared to solve the tape stiction problem at that time. However, during the second series of tests at JPL, it was discovered that this adjustment had incurred other problems in the operating parameters of the recorder. This is discussed in greater detail in paragraph IV.E. of this report.

Other problems that occurred during the first series of tests at JPL are as follows:

a. oil seepage from the motor because of an excessively oiled bearing,

b. a poor hermetic seal on one connecter which required replacing the connecter,

c. poor threads in the gas vent hole which caused gas leakage at the O-ring seal,

d. gas leakage from a blind hole which had been made too deep and located on the side of the chassis plate,

e. an improperly secured nut,

f. tape spillage from the reel because of insufficient break-in of the tape prior to tension adjustment.

In spite of these difficulties, the transport demonstrated its ability to pass low and high frequency vibration and static acceleration.

E. Second Series of JPL Tests and Resulting Design Changes

Following the design changes of the 10^7 recorder resulting from the first JPL tests, the machine was returned to JPL in October, 1963, for retesting. Prior to any tests at JPL, flutter measurements were taken. The flutter was 1.8% peak-to-peak. This is quite acceptable, and system operation was very good. The vibration and acceleration phases of the test program were conducted using the plastic covers provided by REL.

The vibration test was run in accordance with JPL specification 30257. The reel brake was set during

the three planes tested. The original shock mounts used in the original acceptance tests were again employed. Following vibration in the three planes, the machine was subjected to flutter and system tests. There were no failures observed during these tests.

The static acceleration test was conducted in accordance with JPL specification 30257. Again, the machine passed with no indication of failure.

Flutter was measured before proceeding to the thermal portion of the test program. Normal flutter readings were obtained. The recorder was placed in an oven, and the temperature was reduced to -10 C. Following the prescribed soak time, the recorder was returned to room temperature. No difficulty was observed in either operating mode and the measured flutter amplitude had not increased or changed in characteristics

After a weekend shutdown, the recorder was subjected to further temperature tests at 80 C. An increase in flutter was noted and the servo system showed abnormal instability. Some doubt existed as to the nature of the trouble. Since spacecraft tests were being conducted in the immediate area and considerable radio frequency radiation was taking place, it was believed that this rf noise might be causing the instability. Some of the trouble was later attributed to RFI effects, but later it was determined that the difficulty was due to a machine malfunction. Observations at that time

indicated severe flutter of a very definite period. The R&L engineer, with the agreement of the JPL cognizant engineer, shut down further tests and the recorder was returned to R&L.

The first thing R&L did after analyzing the recorder was to change the reel bearings. Replacement of the bearings decreased the flutter to some extent--about 4%. However, the flutter had a predominant 32 cycle per second component. This frequency did not correlate with any known rotational frequencies within the system. Following more intensive analysis, the source of the 32 cycle per second component was traced to a clutch spring assembly. It was determined that under the load conditions of the transport, the spring clutch was free to oscillate under the shock of variable torque pulses which are normally present due to tape irregularities. This was borne out by mechanically locking the clutches so that the override spring was no longer part of the torque transfer system.

Locking the clutch eliminated the 32 cycle per second signal but could not be used as a repair because the clutch must be free to drive or slip, a demand which is determined by mode selection. A shift to a higher torque operating point was accomplished by increasing the capstan speed differential by 0.25%, bringing the differential up to 0.5%. This reduced

the 32 cycle per second flutter by more than 2:1.

Another problem encountered during the second series of tests at JPL was a serious low frequency component directly related to the capstan rotational frequency. Investigation finally seemed to indicate that the upstream capstan was causing the trouble. It was determined that oxide from the tape was building up on the capstan. This problem is discussed in detail in paragraph III.D.

VI. CONCLUSIONS

The 10^7 bit recorder program culminated in the successful realization of a multiple-rate, high-storage capacity recorder. Some problems naturally occurred which have been discussed throughout this report.

The tape and associated bearing problem was the most serious encountered. Further modification of the clutch design should eliminate the introduction of extraneous flutter components due to resonances.

Tape reliability is of prime importance in tape recorder operation. Very little data is obtainable from the tape manufacturers. Practically all information concerning effects of temperature, lubricity, and operating life was determined at REL by actual operation in test transports. This is a very expensive and time consuming method. Future research of various tapes should eliminate the problems encountered during the development of the 10^7 bit recorder.

REL has been conducting research in the area of bearing life and lubricant properties. While further bearing studies are being conducted, no serious problems seem to exist. Bearing life has been determined to such an extent that reliability is quite high. The 10^7 bit recorder program discussed in this report has indicated that the current bearings used in this recorder are capable of excellent life. The contamination encountered in the bearings during the 10^7 bit recorder development originated from external sources, such as lubricant and oxide from the tape and Graphitar from the override clutches. If these sources of contamination are eliminated, the bearing life would be even better than that in the present machine.

The motors used in the 10^7 recorder proved not to be as difficult a problem as was originally anticipated. No serious difficulties were experienced in getting reliable operation over the 8:1 speed range. Input power was slightly higher than origianlly estimated, but the overall figures are reasonable. In the future, delivery problems such as were experienced early in this program will no longer exist, inasmuch as REL is now producing these motors in-plant under license to H. C. Roters. We will be able to control design and fabrication to a greater degree, thus enabling delivery dates and test programs to be handled with greater efficiency.

The area of motor drive systems is well under control, and no future difficulty should arise if the present motor philosophy is retained.

The heads used in the 10^7 system worked out very well. Wear was found to be at a minimum, and electrical and mechanical parameters subject to little or no change. Skew can be reduced to some extent by transport design modifications. Gap scatter is a manufacturing problem, and future work with the head vendors could yield assemblies having improved gap alignment.

The design of variable gain playback amplifiers was quite successful. Novel approaches to the problems of low input signal levels were used. No difficulty due to temperature drift was experienced. AC gain of these amplifiers is quite constant over the specified temperature range of -10 C to +75 C; and in most cases, parts selection is not criticial. The ability of these amplifiers to work at low input levels, such as less than 100 μvolts, with a signal-to-noise ratio of 40 db, indicates that machines may be built in the future with high packing density and small reels without severe limitations as were originally imposed due to the use of conventional amplifier circuits.

Because of early test results and the improved heads used, REL believed that the packing density could be increased to 500 bits per inch per track with no degradation in the overall performance of the recorder. Since the tape reel had been designed to accommodate sufficient tape for

400 bits per inch, REL tried a design at 500 bits per inch which yielded a total storage capacity of 1.25×10^7 bits. Results of the few tests performed at this increased packing density proved that the machine could easily operate with this higher storage capacity.

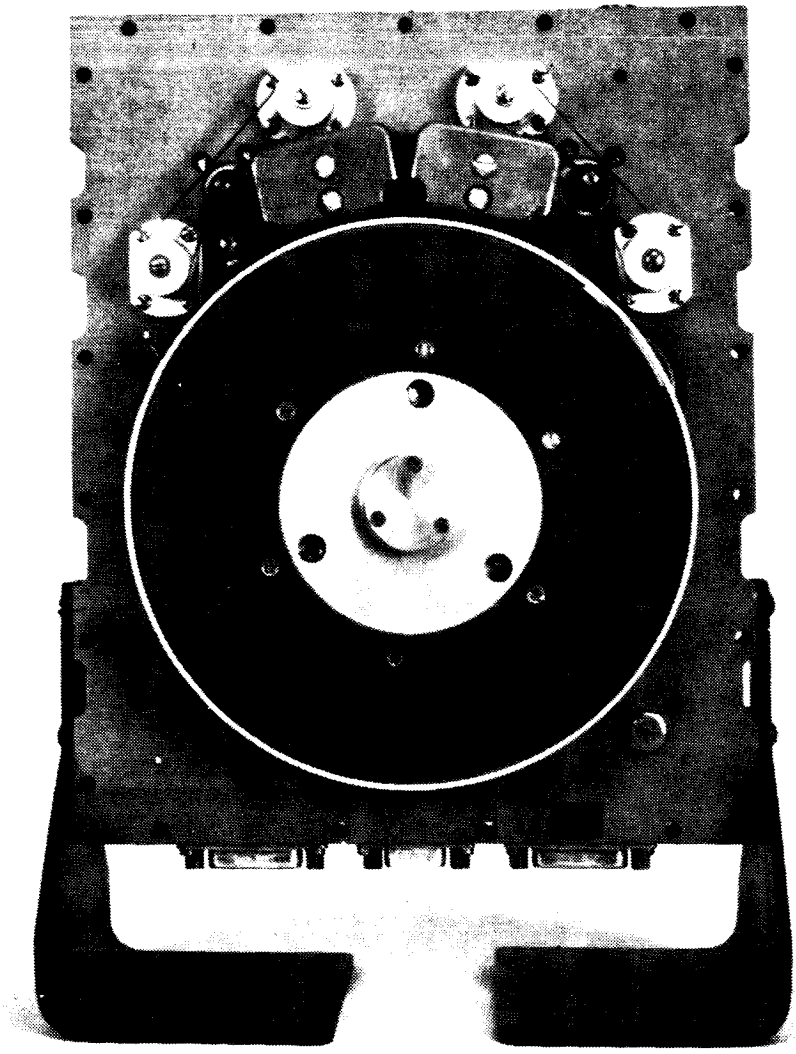


Figure 1

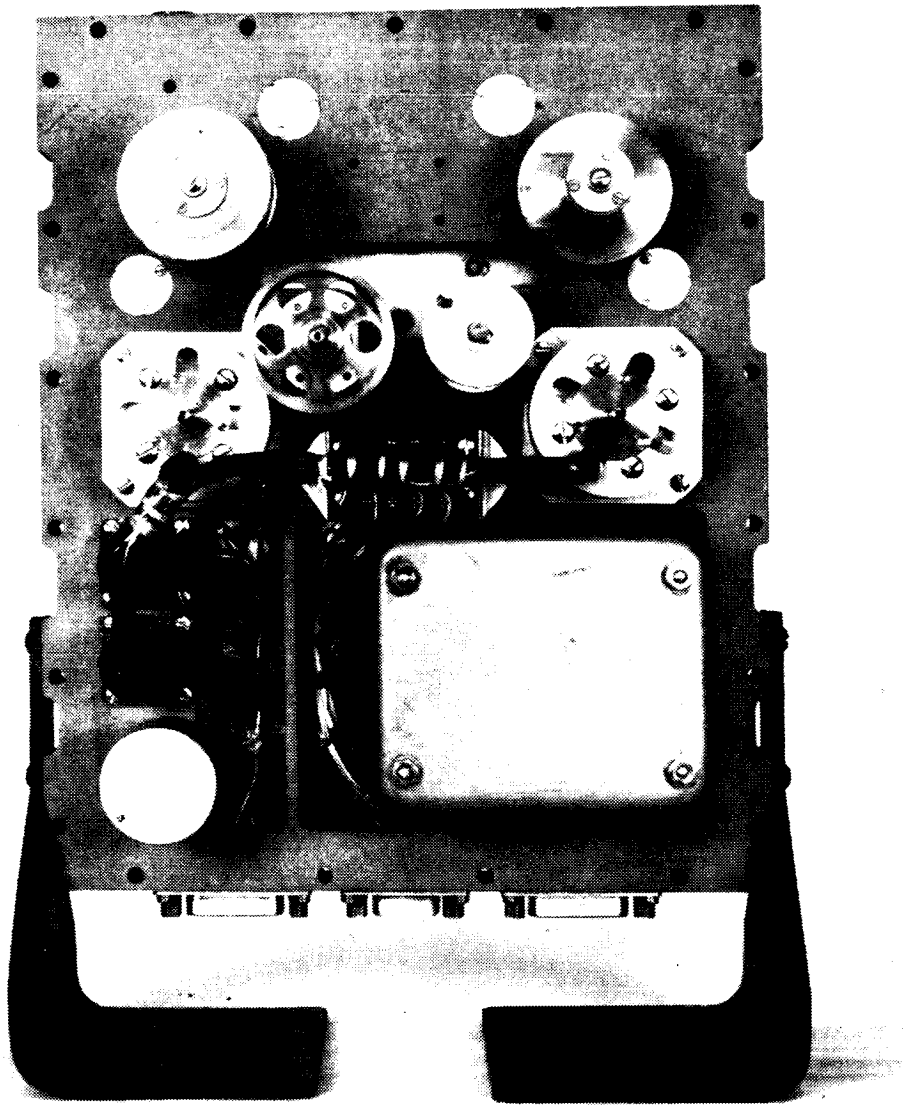


Figure 2

TYPICAL GAP SCATTER & SKEW TEST RESULT

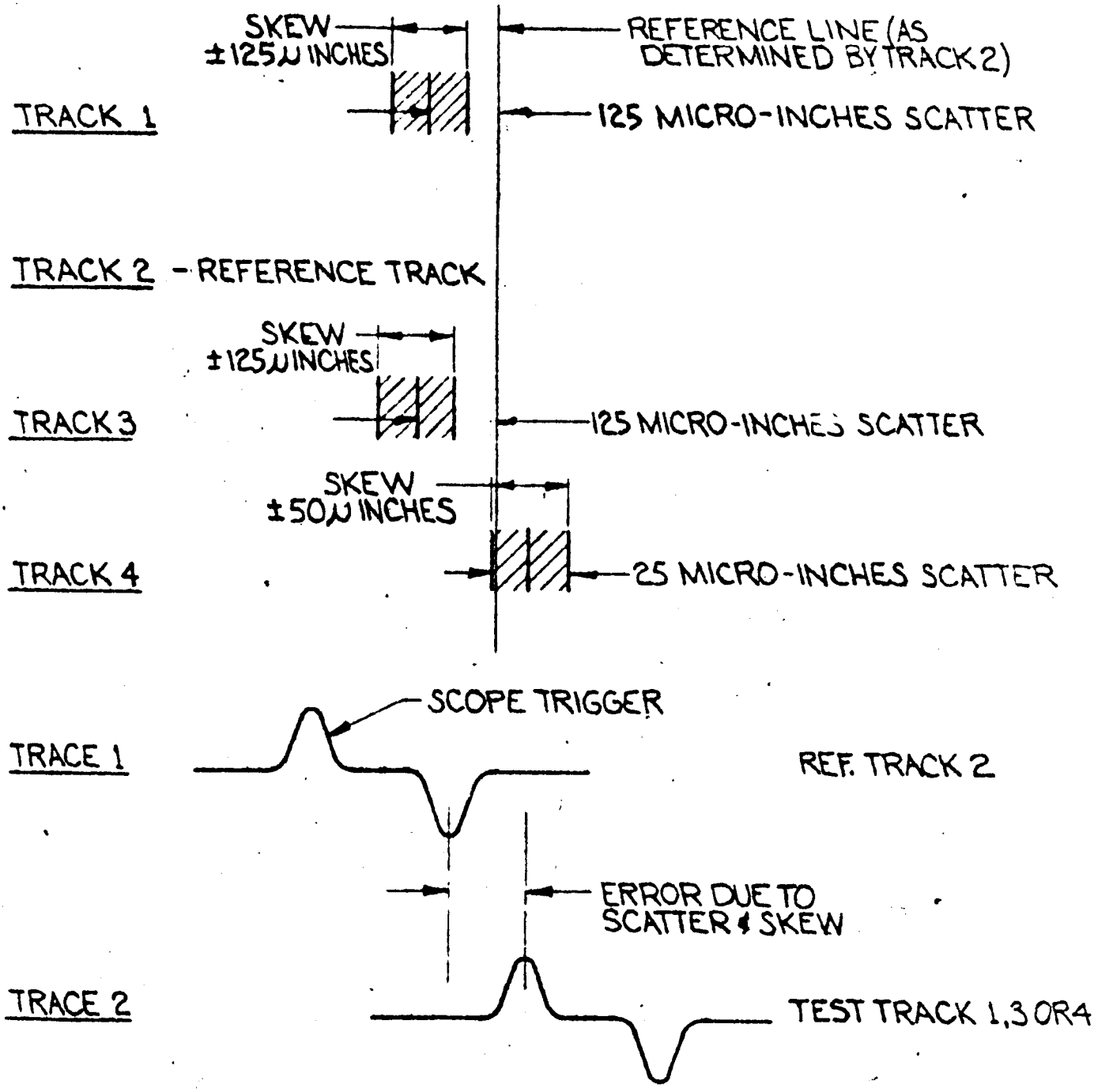
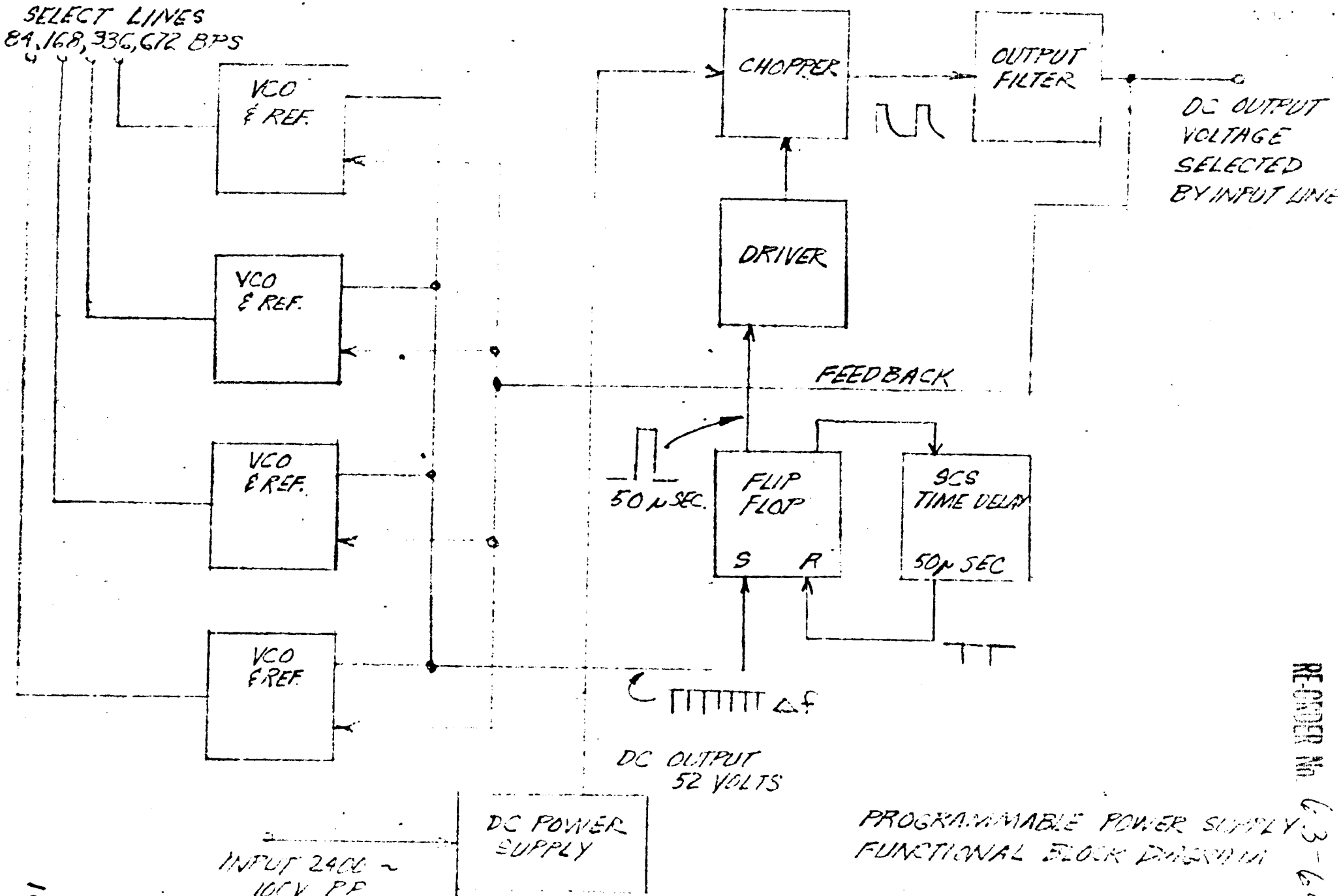


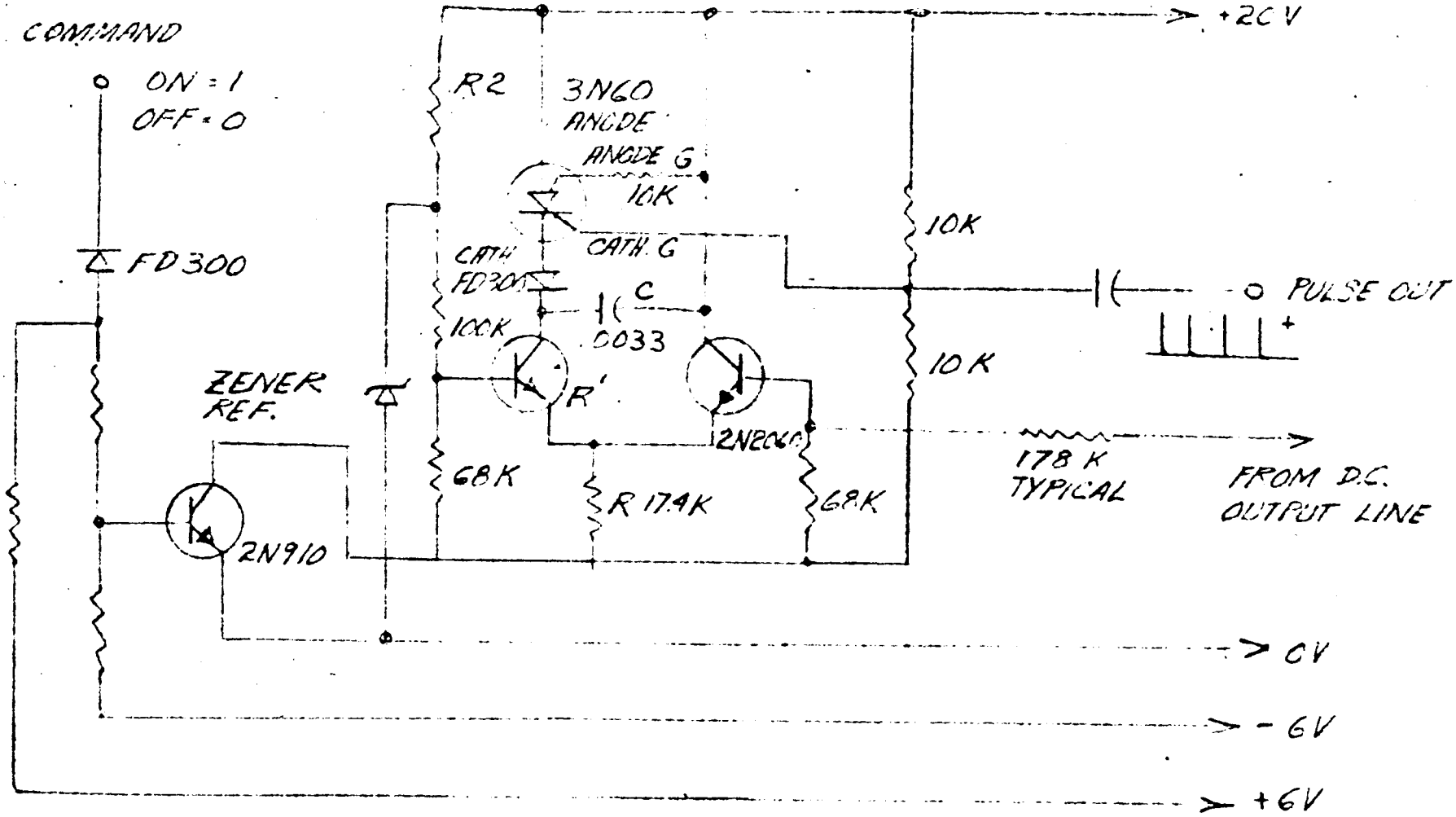
FIGURE 3



PROGRAMMABLE POWER SUPPLY FUNCTIONAL BLOCK DIAGRAM

RE-ORDER NO. 63-6411

FIGURE 4

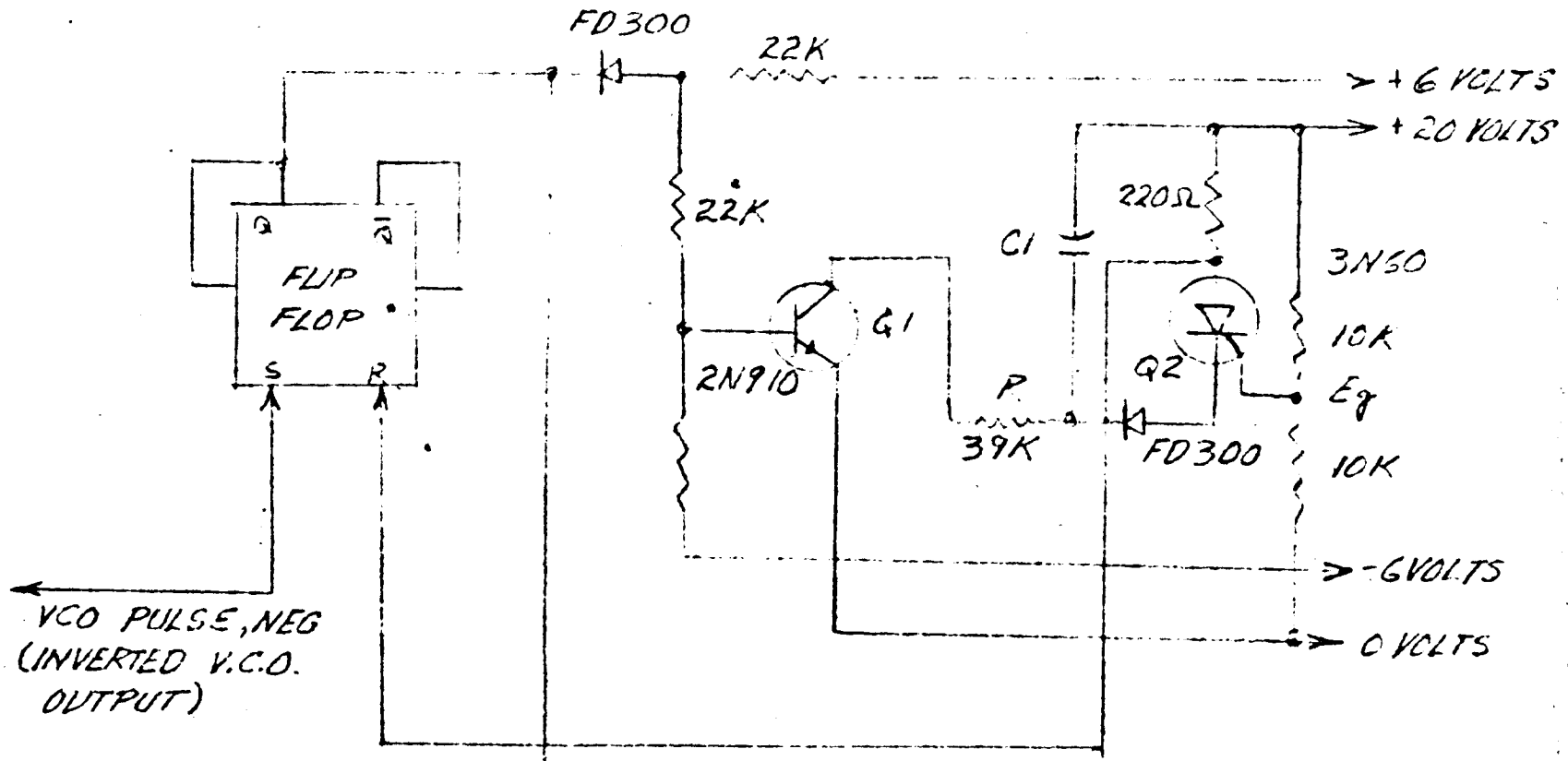


C = DETERMINES FREQ.
R " "
R' = EQUIVALENT IMPEDANCE WHICH CONTROLS FREQ.

TYPICAL VOLTAGE-CONTROLLED OSCILLATOR AS USED IN PROGRAMMABLE POWER SUPPLY

FIGURE 5

RE ORDER NO 43-141



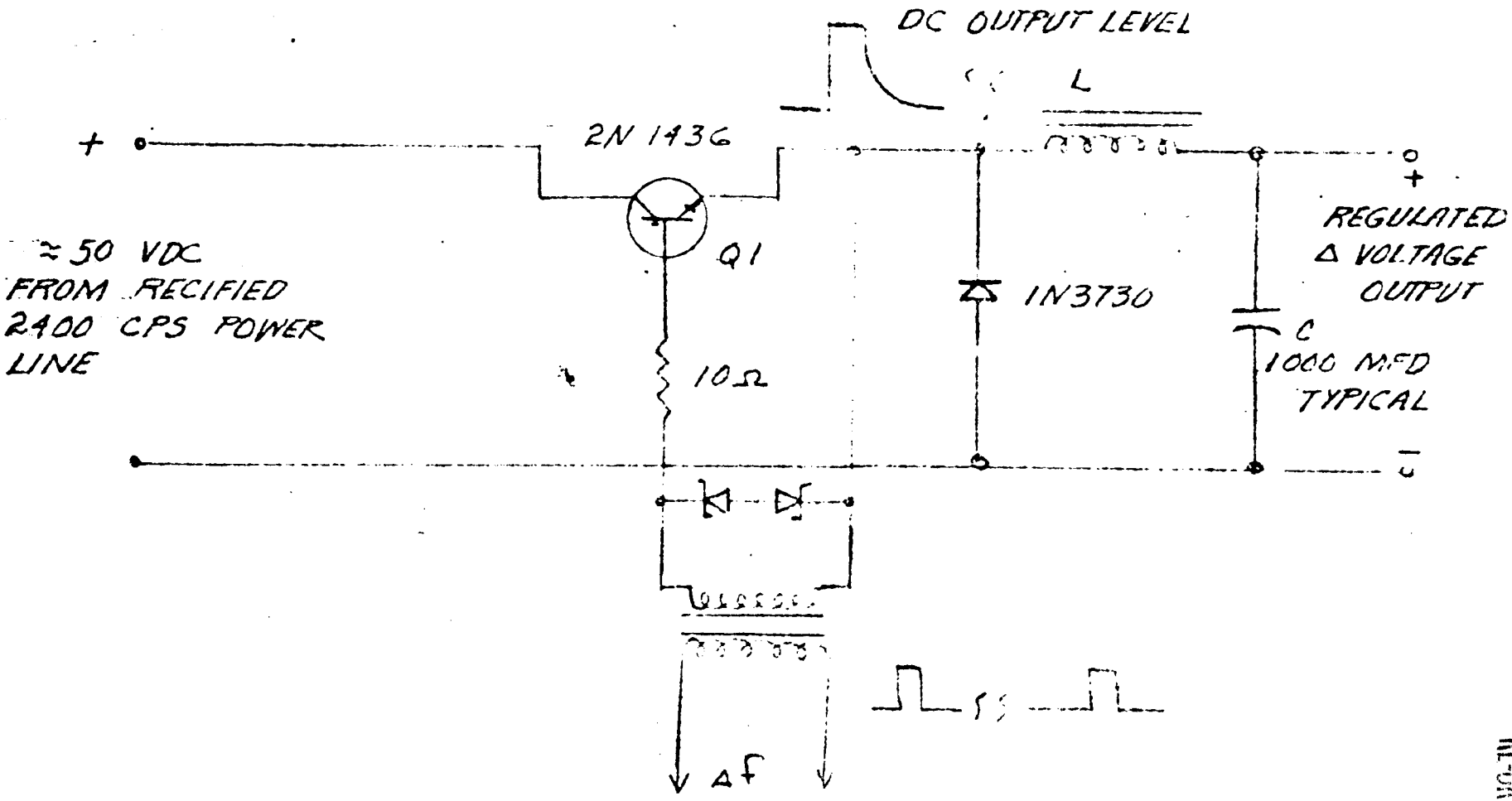
C1 = DETERMINES TIME
R = " "
Eq = CONTROLS FIRING POINT OF SCS

PULSE GENERATOR (ONE SHOT)
PROGRAMMABLE POWER SUPPLY

011

FIGURE 6

142-63-64



PROGRAMMABLE POWER SUPPLY CHOPPER STAGE & OUTPUT FILTER

FIGURE 1

RE-ORDER NO. 63-9-71

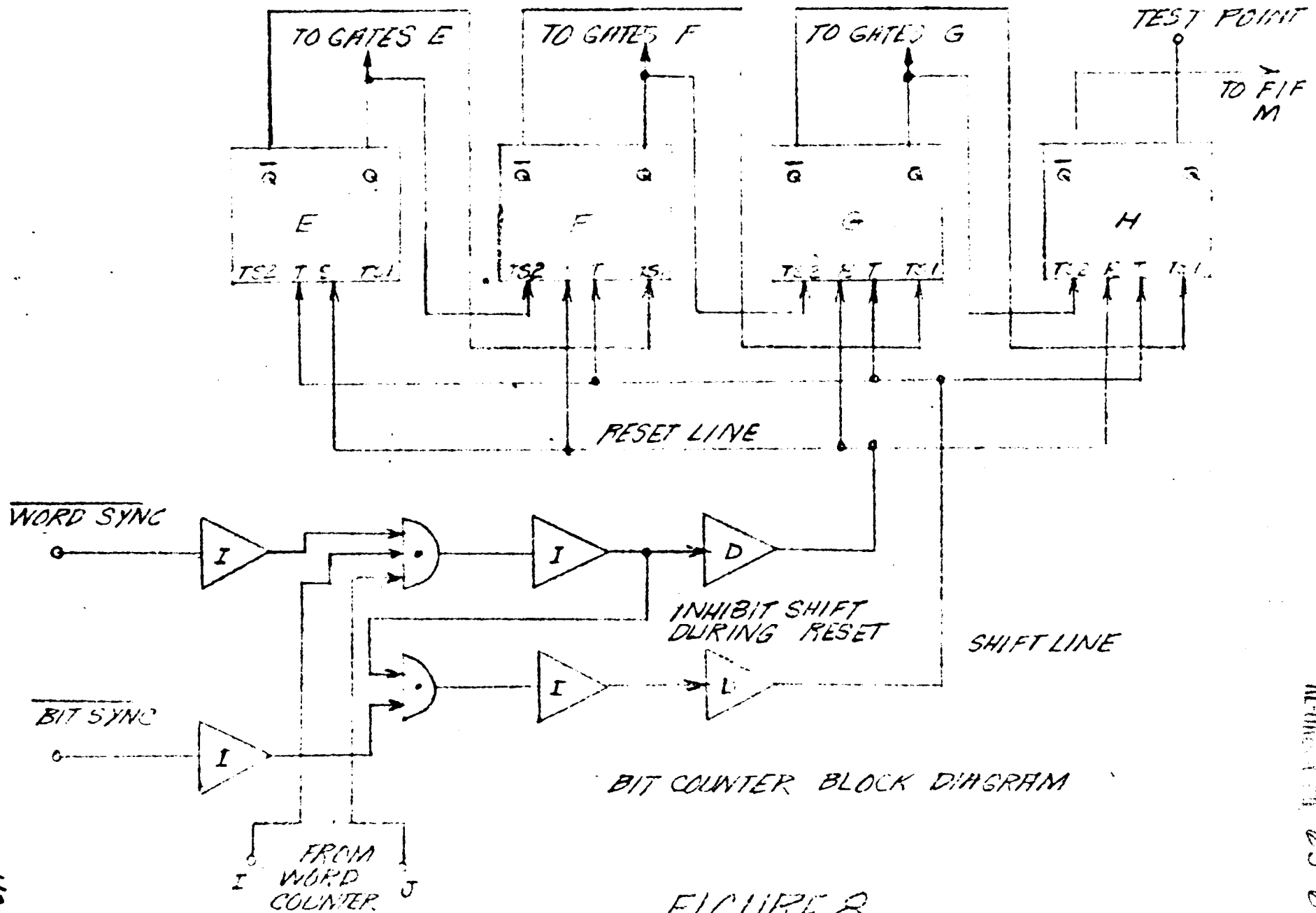
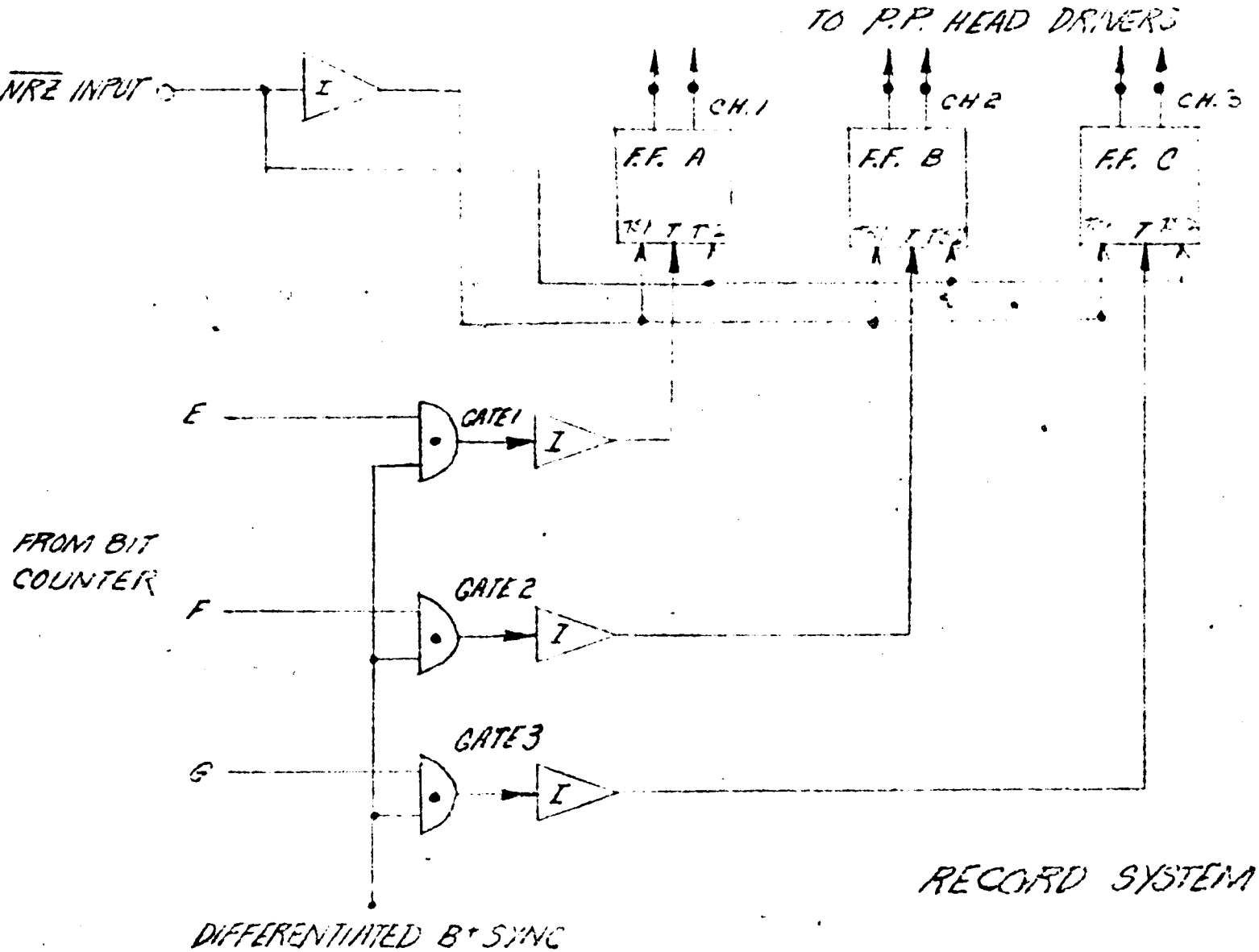
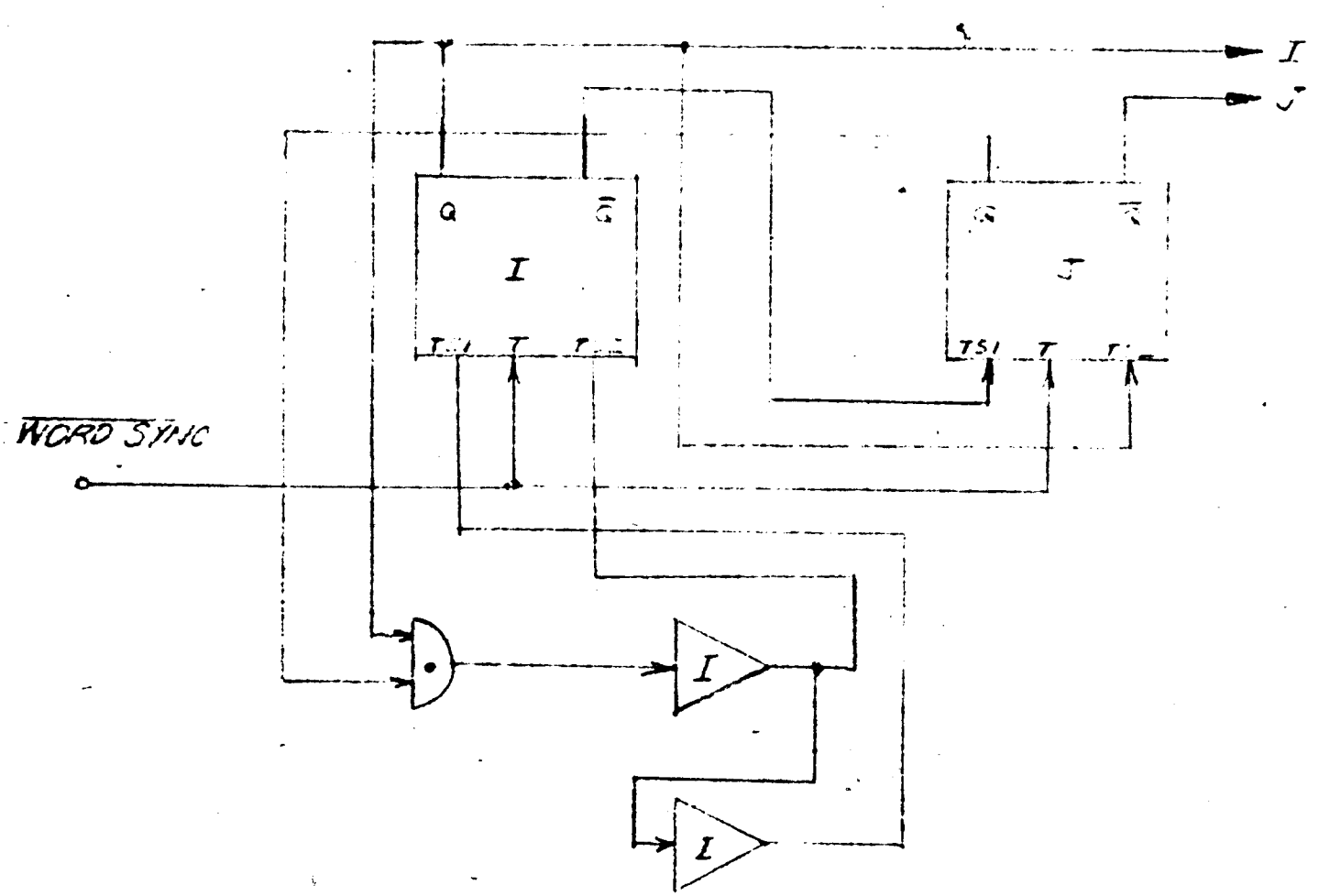


FIGURE 8



RECORD SYSTEM BLOCK DIAGRAM

FIGURE 10



WORD COUNTER BLOCK DIAGRAM

FIGURE 9

RE-ORDER No. 63-641

TAPE SIGNAL & LEVEL INDICATOR WAVEFORMS

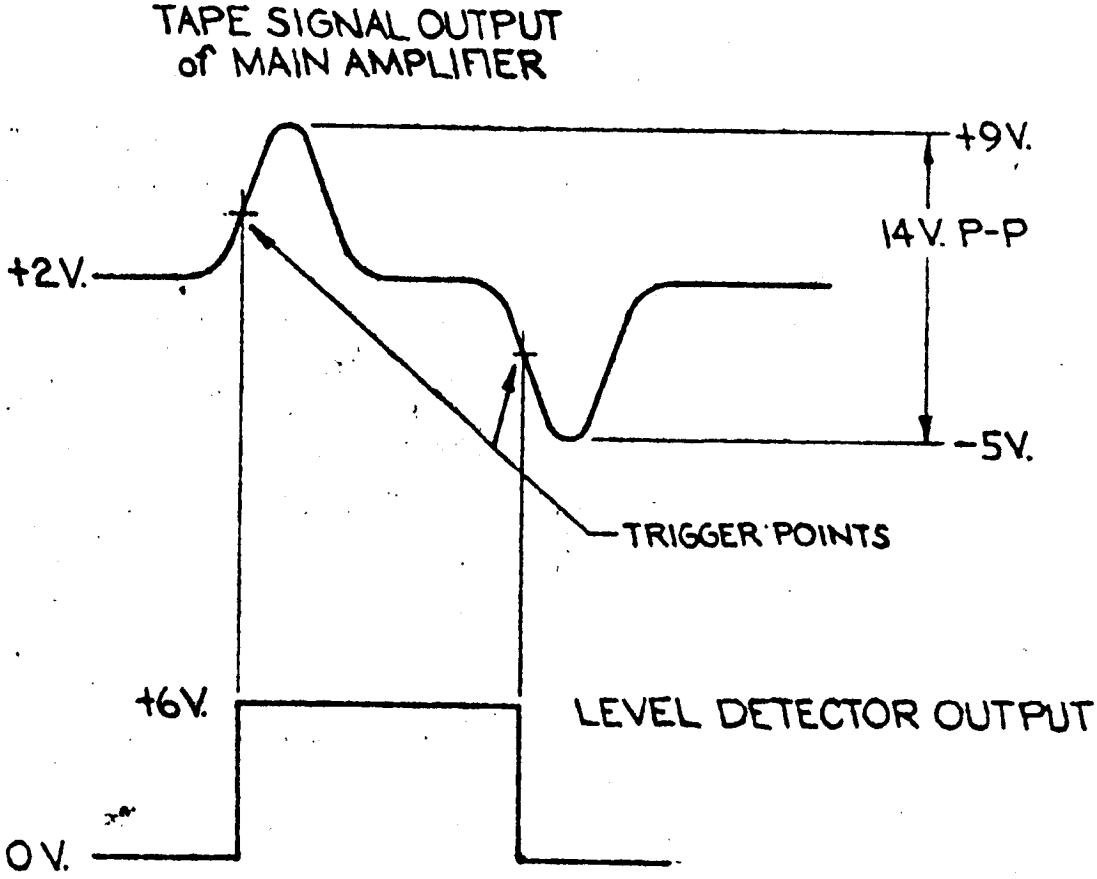
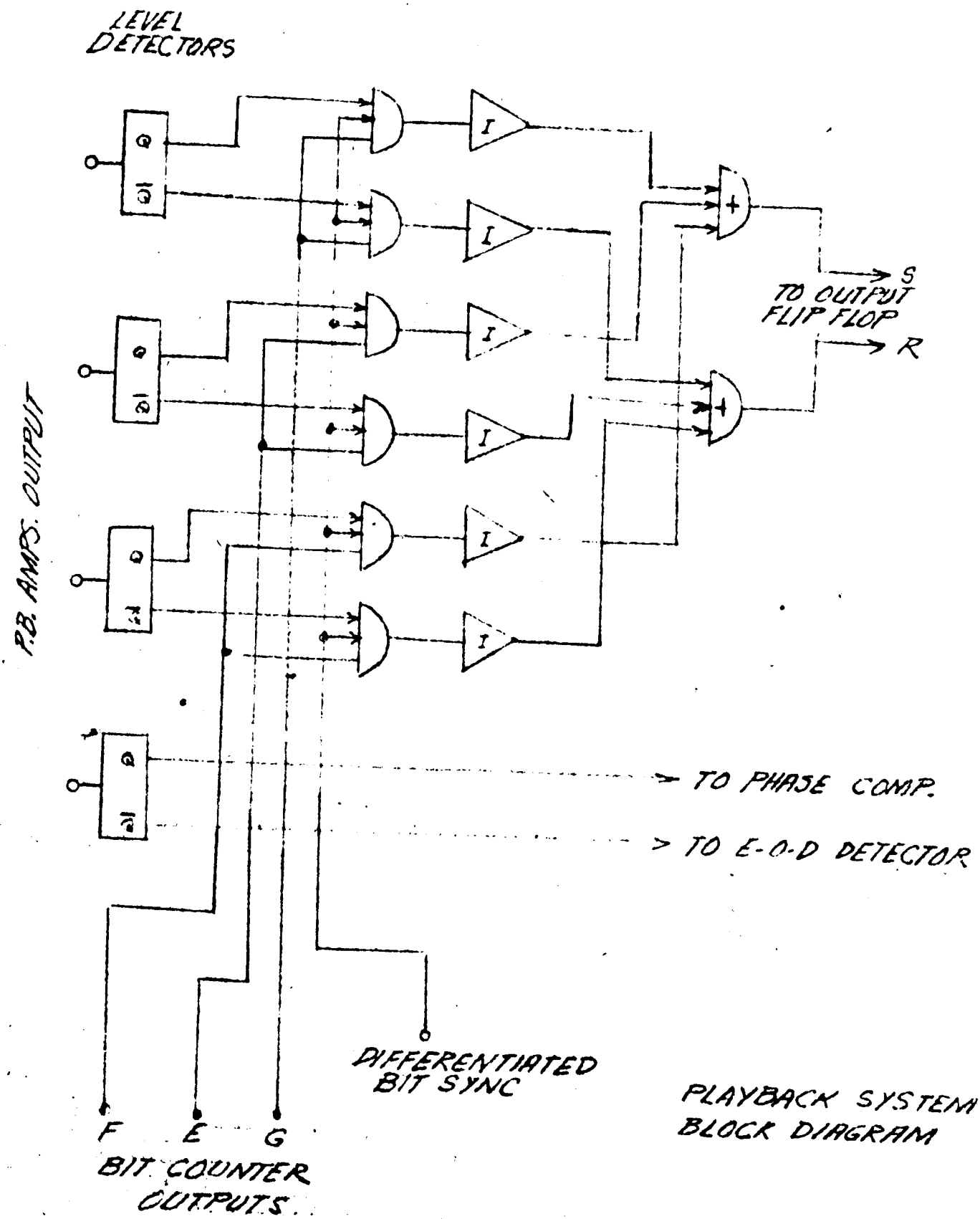


FIGURE 11



PLAYBACK SYSTEM BLOCK DIAGRAM

FIGURE 12

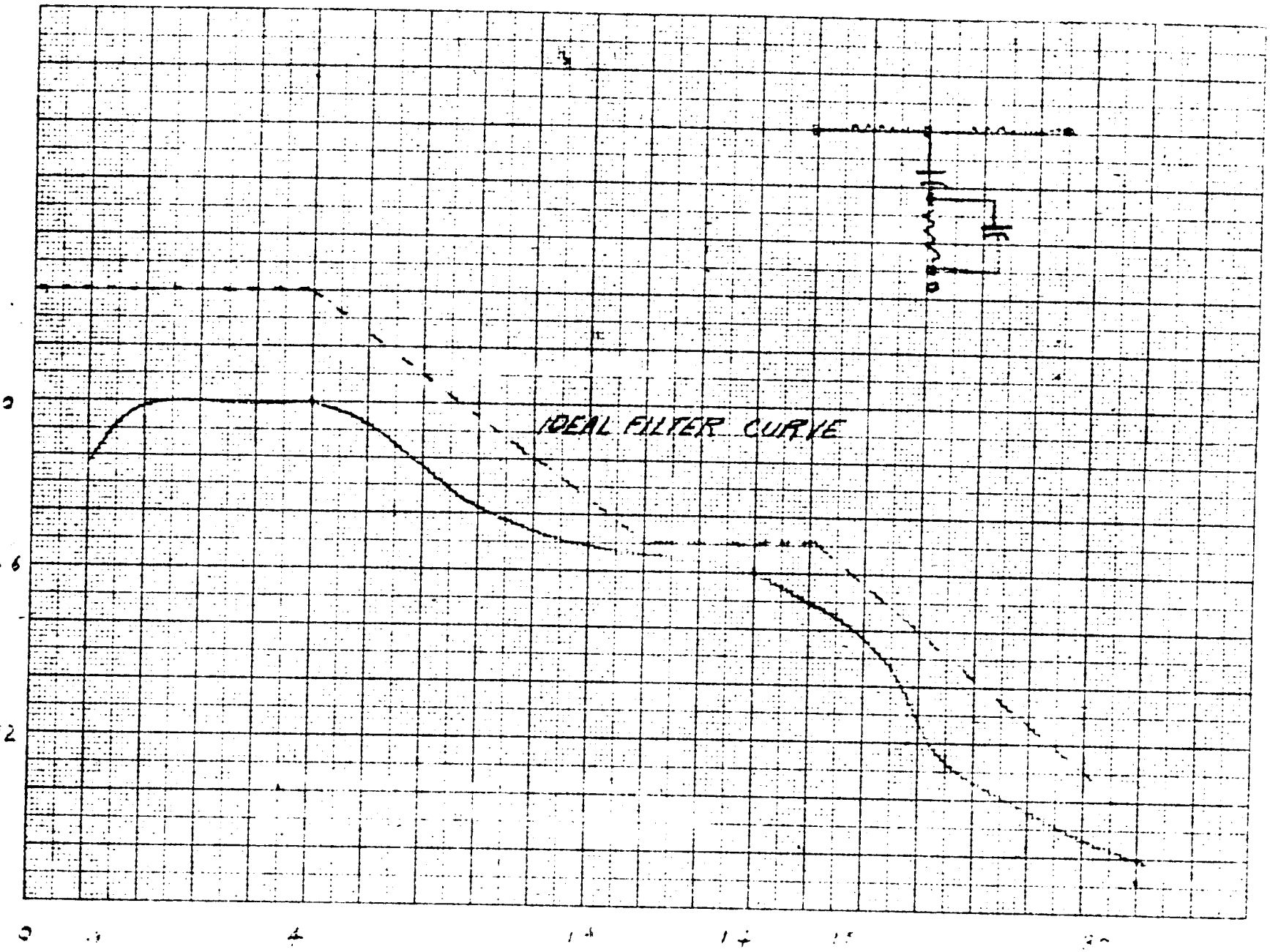
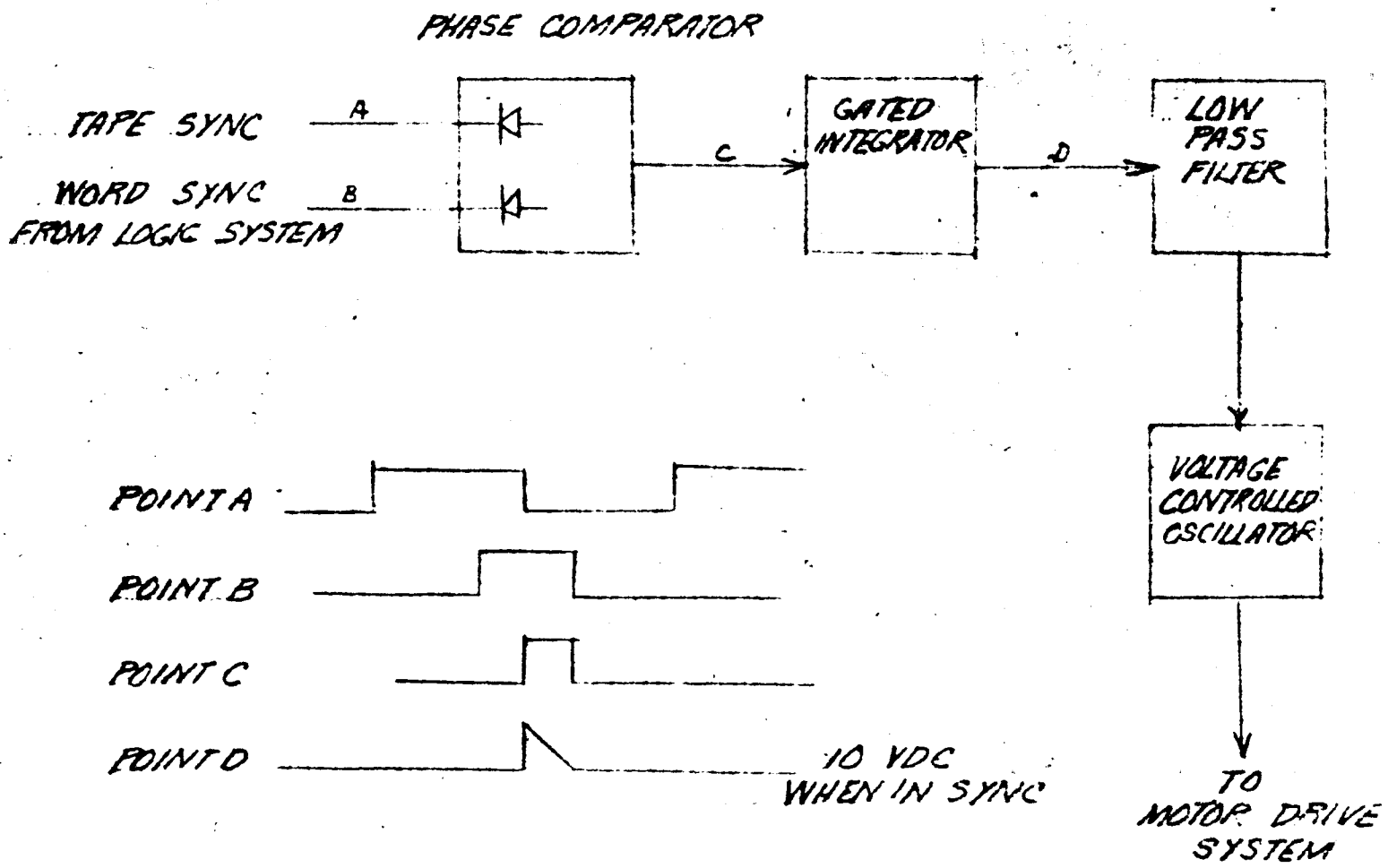


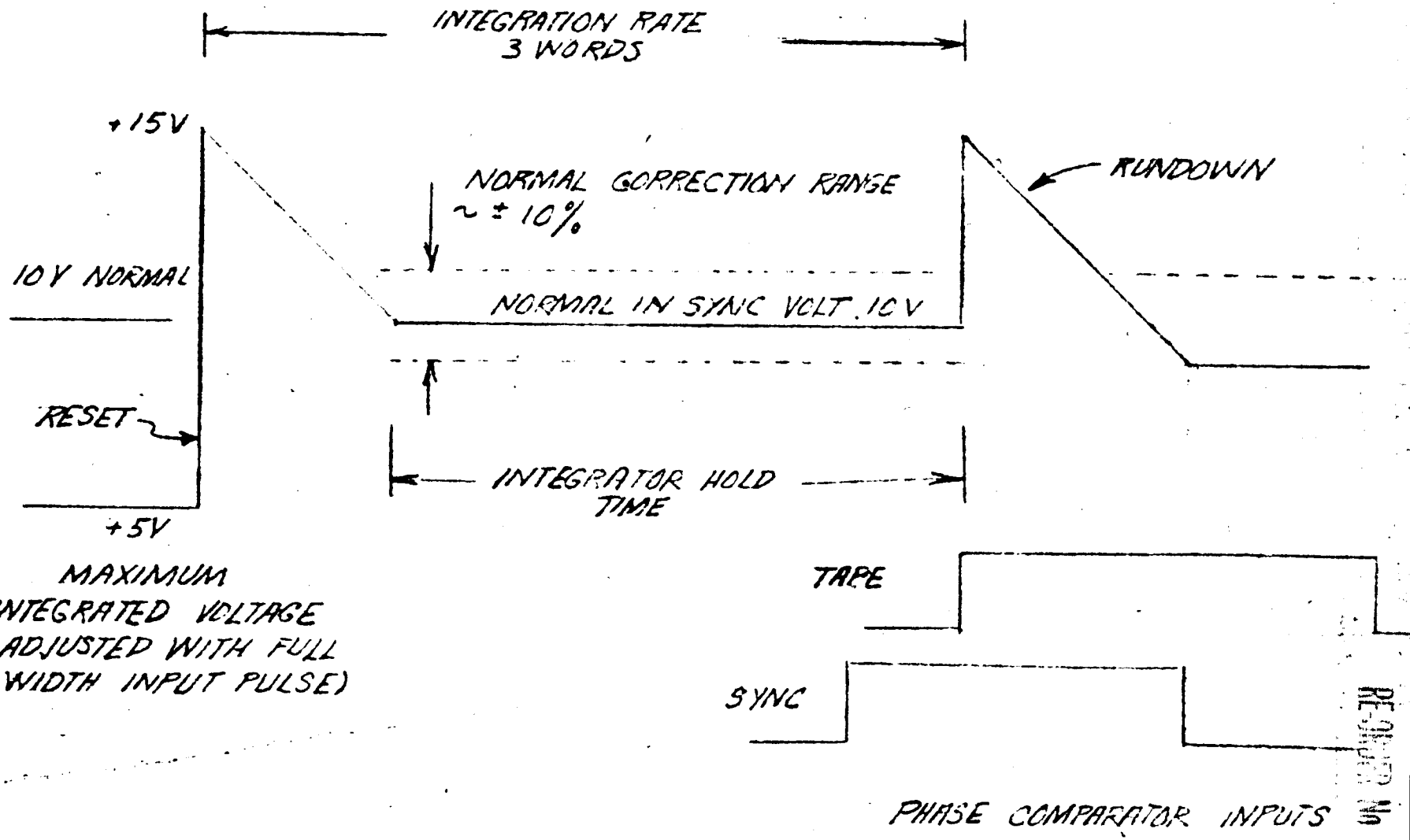
FIGURE 13

PHASE LOCK LOOP FILTER
TYPICAL CHARACTERISTICS



PHASE LOCK LOOP BLOCK DIAGRAM

FIGURE 14



INTEGRATOR WAVEFORM

FIGURE 15

NOTEBOOK No. 63-64

0DB REFERRED TO 15 VOLTS
PEAK TO PEAK OUTPUT AT
100 ~, 100 MV INPUT
GAIN 5 X 10⁴
SIGNAL TO NOISE RATIO > 40DB

OUTPUT DB

0 -3 -6 -12 -18

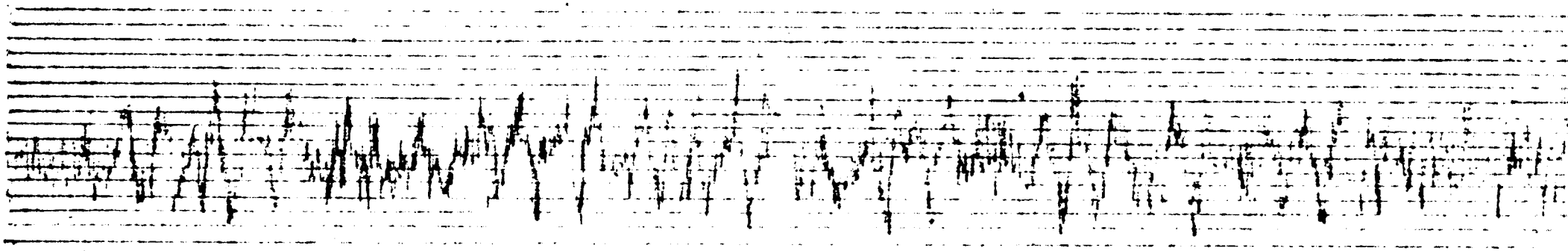
120

1000 ~

100 ~

KEUFFEL & ESSER CO.
SEMI-LOGARITHMIC
3 CYCLES X 70 DIVISIONS

FLUTTER CHART, TYPICAL



TIME SCALE 5" = 1 SEC.
AMPLITUDE: 10 LINES = 1%

FIGURE 17

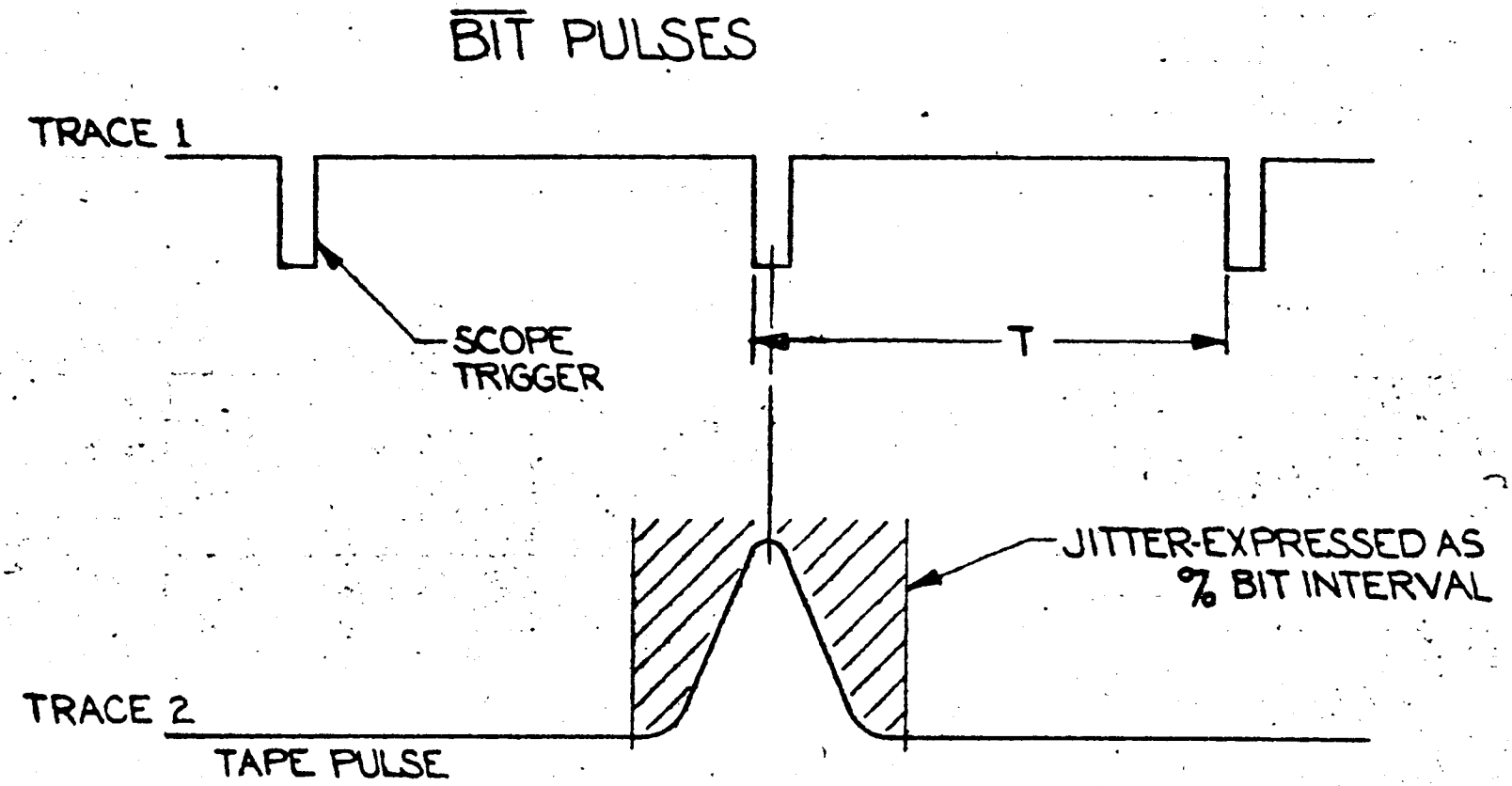
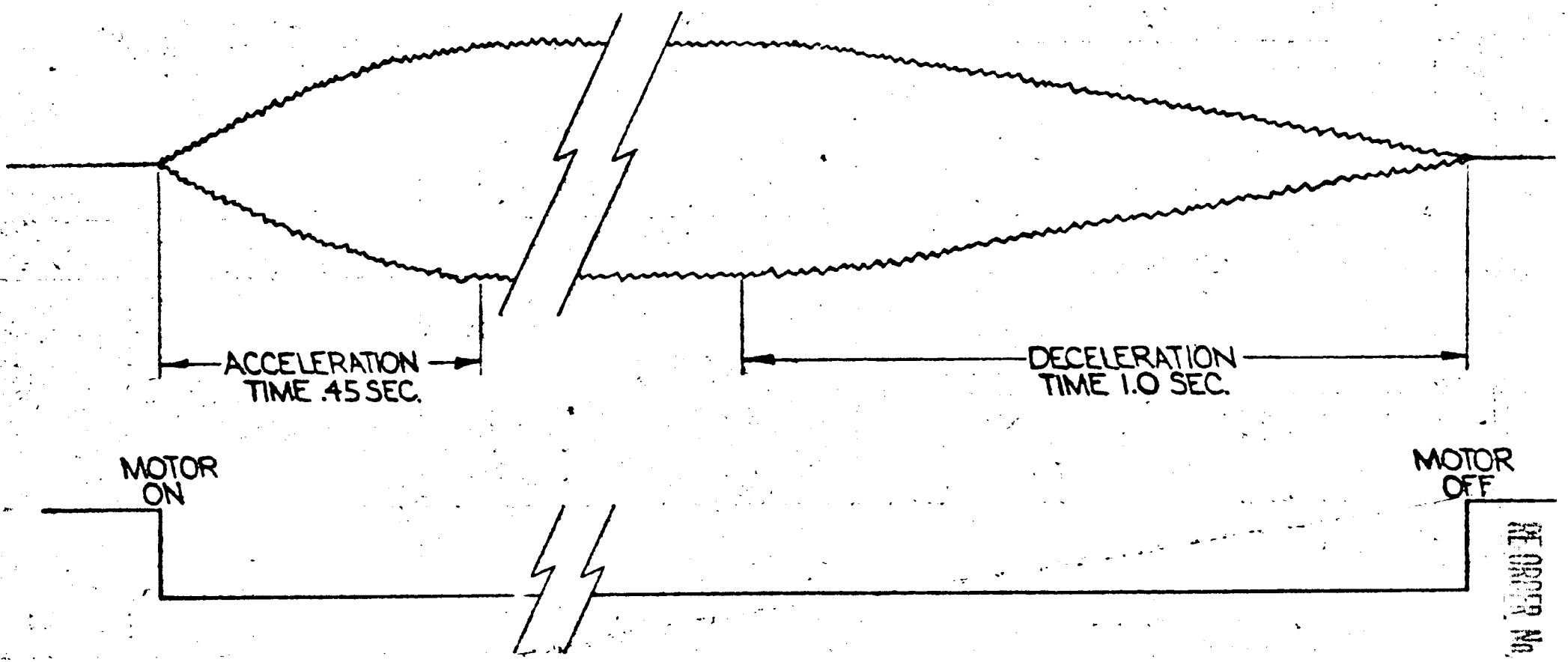

$\overline{\text{BIT}}$ PULSES
TRACE 1
SCOPE TRIGGER
T
JITTER-EXPRESSED AS % BIT INTERVAL
TRACE 2
TAPE PULSE
PLOTTED JITTER WAVEFORM

FIGURE 18



ACCELERATION & DECELERATION CHART

FIGURE 19

RECORDER No. 63-641

RE-ORDER No. 63-641

-10° C MOTOR PERFORMANCE PLOT

MOTOR # 141 PLAYBACK
TYPE 113J-10 107BIT
RECORDER

MOTOR RATING
SPEED 3780
NOM TORQUE .140 OZ-IN
@ FREQUENCY 157 CPS

FREQ	I	E	INPUT M.W POWER	CHART SPEED	OZ IN CHART TORQUE	SLIP	ELECTRONIC EFFICIENCY %
42.5	114	5.0	720	860	.160	4	16.4
47.2	121	5.0	605	745	.116	4	12.0
52.5	110	5.0	550	1040	.111	4	[illegible]
83.1	101	8.0	808	1702	.180	4	34.0
94.5	91	8.0	728	1870	.135	4	26.0
104.0	81	8.0	648	2080	.075	4	26.5
170.1	92	15.0	1380	2402	.189	4	50.4
189.0	82.5	15.0	1238	3780	.132	4	51.1
204.5	71.5	15.0	1073	4158	.091	4	51.0
340.2	87.5	30.0	2625	6504	.196	4	58.0
378.0	80.0	30.0	2400	7560	.125	4	56.2
405.8	71.0	30.0	2130	8016	.087	4	59.4

STALL DATA

		OZ-IN STALL TORQUE
42.5	5.0	.171
47.2	5.0	.151
52.5	5.0	.128
83.1	8.0	.182
94.5	8.0	.142
104.0	8.0	.098
170.1	15.0	.205
189.0	15.0	.160
204.5	15.0	.108
340.2	30.0	[illegible]
378.0	30.0	.176
405.8	30.0	.120

STATOR # 167
ROTOR # 145

DATE 3/22/63

APPENDIX I

MOTOR PERFORMANCE TEST DATA

RE-ORDER No. 63-641

=10°C MOTOR PERFORMANCE TEST

MOTOR # 131 RECORD
TYPE 113J 10 BIT
RECORDER

MOTOR RATING
SPEED 1890 RPM
@ 94.5 CPS
NOM. TORQUE .140 OZ-IN

INPUT FREQ	I	E	POWER	SHAFT SPEED	TORQUE	SLIP	ELECTRICAL EFFICIENCY %
CPS	M.A	VOLTS	M.W.	RPM	OZ-IN	RPM	
43.2	112	4.7	526	945	.103	4	23.0
94.5	95	8.4	798	1890	.103	4	34.6
181	85	16.5	1402	3780	.103	4	45.3
378	89	35.3	3140	7560	.098	4	45.1

STALL SHAFT TORQUE

43.2		9.7	649	.112
94.5		8.4	933 1070	.134
181		16.5		.196
378		35.3	2850	.286

STATOR # 159
ROTOR # 154

DATE 1-12-65

480 C MOTOR PERFORMANCE TEST

MOTOR #141 PLAYBACK
TYPE 1130-10 10.7 BIT
RECORDER

MOTOR RATING
SPEED 3150 NOMINAL
NOM TORQUE .190 OZ-IN
@ FREQUENCY 157 CPS

INPUT FREQ CPS	I MA.	E. VOLTS	POWER M.W	SHAFT SPEED RPM	TORQUE OZ-IN		ELECTROMAGNETIC [illegible]
						RPM	
42.5	127	5.0	635	[illegible]	.176	4	17.9
47.2	110	5.0	550	745	.152	4	[illegible]
52.5	101	5.0	[illegible]	1040	.141	4	[illegible]
85.1	97	8.0	776	1702	.131	4	35.1
94.5	89	8.0	712	1890	.126	4	36.2
104.6	80	8.0	640	2080	.120	4	35.1
170.1	69	15.0	1035	3402	.267	4	[illegible]
189.0	80	15.0	1200	3780	.200	4	[illegible]
207.9	76	15.0	1140	4158	.165	4	[illegible]
140.2	87	[illegible]	2349	[illegible]	.267	4	[illegible]
378.0	43	[illegible]	1161	7560	.214	4	[illegible]
415.8	61	[illegible]	[illegible]	8316	.162	4	[illegible]

	STALL PATH		STALL SHAFT TORQUE OZ-IN
42.5	5.0	750	.133
47.2	5.0	690	.109
52.5	5.0	625	.094
85.1	8.0	976	.187
94.5	8.0	880	.136
104.6	8.0	792	.098
170.1	15.0	1650	.227
189.0	15.0	1365	.169
207.9	15.0	1218	.134
140.2	30.0	8180	.276
378.0	30.0	2730	.209
415.8	30.0	2400	.162

STATOR # 167
ROTOR # 145

DATE [illegible]

RE-ORDER No 63-641

23° C MOTOR PERFORMANCE TEST

MOTOR # 41 [illegible]
TYPE INST-M 10 KIT
RECORDER

MOTOR RATING
SIZE 23-0 NOMINAL
NOM. TORQUE .190 OZ-IN
FREQ [illegible] 185 CPS NOM

INPUT FREQ CPS	INPUT I MA	INPUT E VOLTS	INPUT POWER M.W.	SHAFT SPEED RPM	TORQUE OZ-IN	SLIP RPM	ELECTRICAL OUTPUT [illegible]
42.5	139	5.0	695	850	.135	4	13.6
47.6	120	5.0	600	945	.131	4	17.4
52.5	107	5.0	545	1040	.125	4	19.4
85.1	101	8.0	808	1702	.224	4	37.2
94.5	90	8.0	720	1890	.171	4	35.4
104.0	80	8.0	640	2080	.134	4	33.2
170.1	90	15.0	1350	3402	.238	4	48.1
189.0	80	15.0	1200	3780	.187	4	42.5
207.9	72	15.0	1080	4158	.139	4	41.0
340.2	76	30.0	2280	6804	.248	4	64.4
378.0	74	30.0	2220	7560	.197	4	57.4
405.8	70	30.0	2100	8116	.146	4	57.4

STALL PATH

			OZ-IN [illegible]
42.5	5.0	800	.151
47.6	5.0	705	.114
52.5	5.0	645	.0[illegible]
85.1	8.0	[illegible]	.187
94.5	8.0	[illegible]	.138
104.0	8.0	[illegible]	.098
170.1	15.0	[illegible]	.214
189.0	15.0	[illegible]	.[illegible]
207.9	15.0	[illegible]	.099
340.2	30.0	3000	.247
378.0	30.0	2670	.182
405.8	30.0	2250	.124

STATION # 167
MOTOR # 145

DATE 3/22/63

RE-ORDER No. 63-641

23°C MOTOR PERFORMANCE TEST

MOTOR # 131 RECORD
TYPE 113J 10⁷ BIT
RECORDER

MOTOR RATING
SPEED 1510 RPM
@ 11.5 VDC
NOM TORQUE .140 OZ IN

FREQ CPS	INPUT I M.A.	E VOLTS	POWER M.W	SHAFT SPEED RPM	TORQUE OZ-IN	SLIP RPM	ELECTRIC EFFICIENCY
47.25	121	4.7	570	945	.126	4	18.3
94.5	100	8.4	840	1890	.172	4	28.1
189.0	92	16.5	1520	3780	.223	4	43.2
378	92	35.3	3250	7560	.222	4	47.3

STALL SHAFT TORQUE

47.25		4.7	649			.014	
94.5		8.4	933			.15-	
189.0		16.5	1650			.216	
378		35.3	3520			.21-	

STATOR #159
ROTOR #154

DATE 1/[illegible]/[illegible]

RE-ORDER No. 63-641

+80°C MOTOR PERFORMANCE TEST

MOTOR # 131 RECORD
TYPE 113J 10 POLE
RECORDER,

MOTOR RATING
SPEED 1590 RPM
@ 94.5 CPS
NOM TORQUE .140 OZ-IN

FREQ	INPUT			SHAFT SPEED	TORQUE	SLIP	ELECTROMAGNETIC EFFICIENCY %
CPS	NO. A.	VOLTS	W. W	RPM	OZ-IN	RPM	
97.25	111	4.7	522	945	.134	4	19.7
94.5	97	8.4	815	1890	.207	4	37.1
189	85	16.5	1400	1780	.253	4	55.9
378	70	35.3	2450	1760	.295	4	55.0

			STALL SHAFT TORQUE OZ-IN
47.25	4.7	625	.650
94.5	8.4	1010	.162
189	16.5	1750	.233
378	35.3	4150	.336

STATOR #
ROTOR #

DATE 1-11-63

APPENDIX II

INTERIM TEST PLAN

TYPE APPROVAL TESTING OF

10^7 BIT MAGNETIC TAPE RECORDER

Raymond Engineering Laboratory, Inc.
Middletown, Connecticut

REL W.O. 787 (JPL)

INTERIM TEST PLAN

TYPE APPROVAL TESTING OF 10^7 BIT

MAGNETIC TAPE RECORDER

1.0 SCOPE

This document lists specific environmental tests to be performed on the 10^7 bit Magnetic Tape Recorder (Model 1737) as part of its acceptance test program by Jet Propulsion Laboratory in accordance with pertinent JPL specifications, and lists certain functional tests to be performed on the mechanism, before, during, or after environmental tests.

2.0 PURPOSE

The purpose of the Interim Test Plan is to define the types of tests to be performed. The plan is termed "Interim" because the mechanism is of an advanced development status such that all physical details are not necessarily representative of flightworthy equipment.

3.0 REFERENCES

The following documents are applicable to this Test Plan:

JPL Specification Number 31009A
JPL Specification Number 30236
JPL Specification Number 30257

4.0 ENVIRONMENTAL TESTS

4.1 Specifications

Environmental tests shall be performed in accordance with JPL Specification Number 30236 and Number 30257.

4.2 General Procedure

Only those tests listed in the following paragraphs shall be performed. The sequence of tests may be other than as listed below. The recorder assembly shall be subjected to sufficient functional tests before, during, and after the environmental tests in order to determine whether its performance is satisfactory and stable. Functional tests are described in Section 5.

4.3 Ethylene Oxide Gas Sterilization Test

Per 30257 paragraph 4.1.1.2.

4.4 RF Interference Tests

Per 30236, Class I.

4.5 Static Acceleration

Per 30257 paragraph 4.3.1.

4.6 Vibration

Per 30257 paragraph 4.3.2 including midcourse correction simulation.

4.7 Shock

Per 30257 paragraph 4.4.1, alternate (a) only.

4.8 Space Flight Temperature

Per 30257 paragraph 4.4.2, deleting thermal shock.

5.0 FUNCTIONAL TESTS ON RECORDER MECHANISM

5.1 Purpose

These tests are intended to evaluate the condition of the mechanical and electronic subassemblies before and after the environmental tests, and where applicable to monitor the effects of environmental extremes upon the subassemblies when operation during the extreme conditions is required.

5.2 Specifications

The recorder performance shall be compared with requirements of applicable sections of JPL Specification Number 31009A.

5.3 Special Provisions

Because of the extended period of time required for one passage of the tape loop, certain electronic operational tests before and after the environmental series can better be performed with a short loop of tape (3 - 6 feet) which is not wound in a reel. However, tests whose data reflect the performance of the transport itself (flutter, A.M., motor load, etc.,)should be performed with a complete tape reel assembly. Most environmental tests will be conducted in an ambient pressure of one atmosphere. To simulate operating conditions for the cover seal, it is necessary to pressurize the transport assembly to two atmospheres absolute (90% nitrogen -

10% Helium). Internal pressure should be reduced to one atmosphere absolute for thermal-vacuum tests.

5.4 Operational Checks

5.4.1 Recording

Check the ability of the system to record at each of its record rates.

5.4.2 Playback

Check the ability of the system to playback at each of its playback rates.

5.4.3 Coding

Check the coding of the sync track following each STOP RECORD command.

5.4.4 End-of-Data Detection

Check the operation of the End-of-Data code detection during playback.

5.4.5 End-of-Tape Detection

Check the operation of the End-of-Tape detection system during recording and playback.

5.4.6 Pressure Transducer

Check the operation of the pressure transducer. Obtain calibration data during gas purging and filling of the transport assembly.

5.4.7 Temperature Transducer

Check the operation of the temperature transducer.

5.5 Performance Checks

5.5.1 Flutter

Obtain Visicorder charts of flutter by recording and playing back at the maximum record rate and at the maximum playback rate.

5.5.2 A.M.

Measure A.M. using the recordings above.

5.5.3 Jitter

Obtain oscillographic or Visicorder records of the time relationship between each channel output during playback of the above signals. Establish a time reference with respect to the sync track in order that the data will show the combined effects of transport jitter and skew plus head gap scatter and azimuth error.

5.5.4 Acceleration/Deceleration Time

Use the above recordings in conjunction with a Visicorder to measure transport acceleration and deceleration time.

5.5.5 Motor Load

Determine the minimum supply voltage at which each motor will start and run at the various speeds. These data will be compared with subsequent calibrations of the motors

to determine motor load.

5.5.6 Power Consumption

Measure power drain from each source for each operating mode and speed. Note current waveforms where ripple is significant.

5.5.7 Phase Locked Loop

Obtain Visicorder records of integrator output during playback under all possible synchronous playback conditions. Note the time required to achieve lock. Obtain Visicorder or oscillographic records of each channel output prior to parallel-to-serial conversion showing the time relation to each channel's respective transfer pulse.

5.5.8 Leakage Rate

Measure the transport leakage rate, being careful to note the gas mixture used and the transport temperature during the measurement. Note the pressure transducer reading from time to time during the environmental tests.