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A COMMANDABLE TAPE-RECORDER DELAY TIMER AND CLOCK SYSTEM FOR AE-B

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A COMMANDABLE TAPE-RECORDER DELAY TIMER AND CLOCK SYSTEM FOR AE-B

by
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October 1965

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SUMMARY

A system developed for the AE-B spacecraft will permit the delayed recording of any 4-minute orbital data sector. The delay is adjustable in 1-minute increments from 1 to 127 minutes. The selected time delay is made by presetting a delay timer through the command link. A clock is incorporated in the system to verify the preset commands and to record the time of data acquisition. This report describes the application of the system to the AE-B project and provides the circuit parameters for application to other projects.

CONTENTS

ILLUSTRATIONS

A COMMANDABLE TAPE-RECORDER DELAY TIMER AND CLOCK SYSTEM FOR AE-B

INTRODUCTION

The atmospheric explorer satellite AE-B has two unique features in its data-collection process which set it apart from previous scientific satellites. These features are:

- a remotely programmed recorder delay timer capable of controlling recorder turn-on after an interval of from 1 to 127 minutes

- a parallel-driven clock which provides a binary timebase for verification of the record event; verification is achieved by parallel recording of this timebase during the actual data-recording period and by transmitting it in real time before data playback

The recorder delay timer and the binary clock, plus associated control circuitry, make up the system known as the commandable recorder clock and timer system.

The AE-B spacecraft closely resembles its predecessor Explorer XVII (S-6) in concept and operational aspects, but in addition will include (a) a spin-axis orientation system, (b) limited solar-cell capability for modest battery recharge, and (c) a tape recorder for extended geographical coverage. The Explorer XVII satellite was commanded on over a station for a 4-minute readout. The inclusion of a tape recorder and a commandable delay timer and clock system in AE-B makes possible a complete experiment-data mapping of the orbit regardless of tracking-station availability. The system therefore provides a means of choosing, in time, any 4-minute sector of the orbit in 1-minute increments for the recording of experimental data. This unsophisticated system consists of a delay timer and clock.

OPERATIONAL CONSIDERATIONS

The system operates in three steps:

(1) A reset command is transmitted through the command link to ready the on-board recording system. The spacecraft beacon transmitter is automatically turned ON for 10 seconds to verify receipt of this reset command.

(2) A digital binary code (7 bits) is transmitted through the command link requesting a certain delay time in 1-minute increments from 1 to 127 minutes.

(3) Finally, a start command is transmitted which starts the countdown of the delay timer from its present position and also starts a count-up of a clock (from zero). Both the timer and the clock are shifted by the same timebase generator (a 400-cps tuning fork). This start command is also verified by a 10-second turn-on of the beacon transmitter.

When the delay timer counts down from its preset time to zero, the tape recorder is turned ON to the record mode. The clock output and experimental data are now recorded. The record time is controlled by the programmer which turns the recorder OFF at the end of 4 minutes. The clock continues running.

When the satellite nears a tracking station, a playback command is transmitted. The clock time is transmitted for 20 seconds and then shut off. Playback of the tape recorder commences and continues for a period of 4 minutes plus 20 seconds. At the end of the playback, the beacon transmitter is again automatically energized for 10 seconds to indicate end of playback.

This three-step procedure starting the generation of a delay time for recording may be changed at any time by the use of the reset command. If the system were reset and a certain delay time were preset, the system's flexibility permits a new or different delay time to be entered, even if the clock delay timer system had been started. By initiating two reset commands (one to stop the countdown and the second to reset), a new delay time may be entered into the system and then started by a start command. In the case of giving the two reset commands, the beacon transmitter is initiated only for its 10-second verification or when the system is ready to receive its preset commands.

FUNCTIONAL REQUIREMENTS

Requirements called for a reasonably low-powered solid-state logic system to perform the following functions:

(1) Accept and store a series of preset commands containing recorder turn-on delay-time information ranging from 1 to 127 minutes.

(2) Upon receipt of a start command, commence the delay-time runout and start an elapsed-time clock. Inhibit any further preset command information.

(3) At timer runout, energize the recorder drive and record electronics. Provide a pulse, FF_1 or FF_2, to programmer No. 1 on an alternate cycle basis. Provide elapsed-time information to the recorder. Remove the timer from its power source.

(4) Accept an OFF bus signal from programmer No. 1 and terminate recorder operation.

(5) Accept a playback command and provide elapsed-time information to the encoder for real-time transmission for 20 seconds. Provide a power pulse (to playback) to programmer No. 1 synchronous with the playback command.

(6) Following the 20-second transmission of real-time elapsed time, energize the recorder drive and playback electronics. Provide a power pulse (t_{20} playback) to programmer No. 1.

(7) Following a second 20-second interval, provide a power pulse (t_{40} playback) to programmer No. 1. Remove all inactive logic from power sources. Prepare system to accept and store a new series of preset commands containing new recorder turn-on delay-time information.

(8) Accept an OFF bus signal from programmer No. 1 and terminate playback operation. If a new series of preset commands is not in storage, remove the entire logic system from power sources. If new series of preset commands is in storage, commence delay timer and elapsed-time clock upon receipt of a start command.

(9) Install sufficient safeguards to guarantee that functional switching is truly sequential in nature. Provide a non-lockup feature to cope with unforeseeable occurrences.

(10) Provide a reliable system.

Inputs and Outputs

Figure 1, a simplified block diagram of the system, shows the combined array of inputs and outputs and their association with the major logic blocks.

A total of ten commands is available to provide the following capabilities:

- Reset (1 command) Channel 14
- Timer preset (7 commands) Channels 15 thru 21

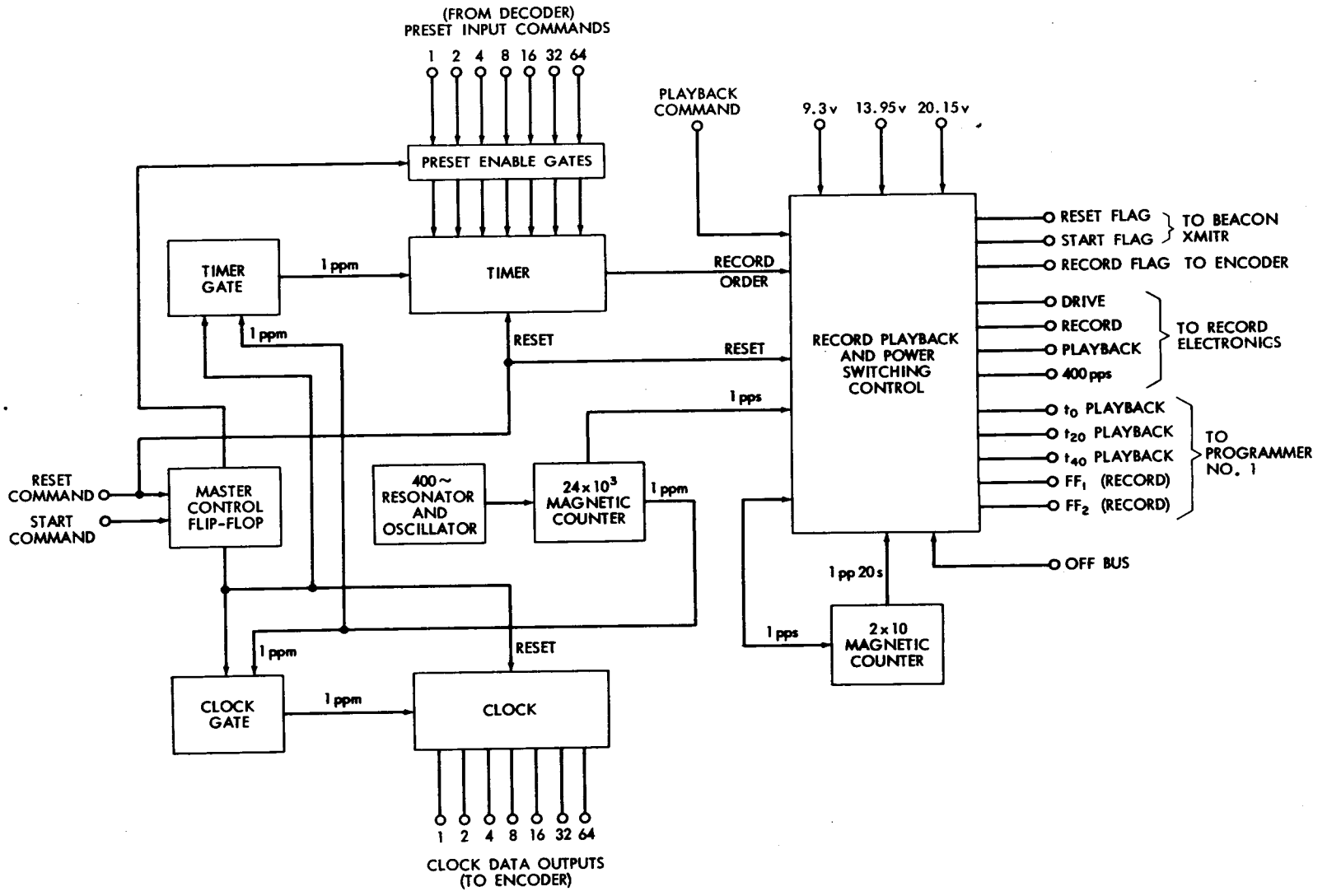


Figure 1. Clock and Timer Electronics

- Start (1 command) Channel 22
- Playback (1 command) Channel 13

Output information and switching signals consist of:

(1) Seven binary-clock data bits - To encoder

(2) Recorder drive control

(3) Record electronics control - To record system

(4) Playback electronics control

(5) 400-pps

(6) t_0 playback

(7) t_{20} playback

(8) t_{40} playback - To programmer No. 1

(9) FF_1 (record)

(10) FF_2 (record)

(11) Reset flag

(12) Start flag - To beacon transmitter

(13) Record flag - To encoder

Input power and switching signals consists of:

(1) 9.3 v

(2) 13.95 v - From battery pack

(3) 20.15 v

(4) Off bus - From programmer No. 1

Logic

Figure 2 is the actual finalized logic diagram of the clock and timer electronics. The legend indicates the symbols used for the various logic elements. The presence of a circled letter or number denotes the power source used to supply that particular element. Power considerations dictated gating of the power supply; this gating is performed according to the schedule presented in Figure 3. The cross section shows that the period of maximum power consumption occurs during the recorder turn-on delay timer operation, and that it approximates 150 mw.

A 400-cps 0.05% resonator provides the basis for accurate timer and clock operation. Differentiating and shaping circuits produce the 30μs pulsewidth required by the recorder drive circuits. A 24×10^3 incremental magnetic counter also uses the 400-pps to produce 1-pps and 1-ppm outputs. The 1-pps drives a 2×10^1 incremental magnetic counter during the period from t_0 to t_{40} playback. The 1-ppm serves as the clock inputs to the timer and the elapsed time clock. Appropriate gates are injected into the timing chain for control. Additionally, a strobe output is made available to the timer to prevent premature recorder turn-on due to ambiguities.

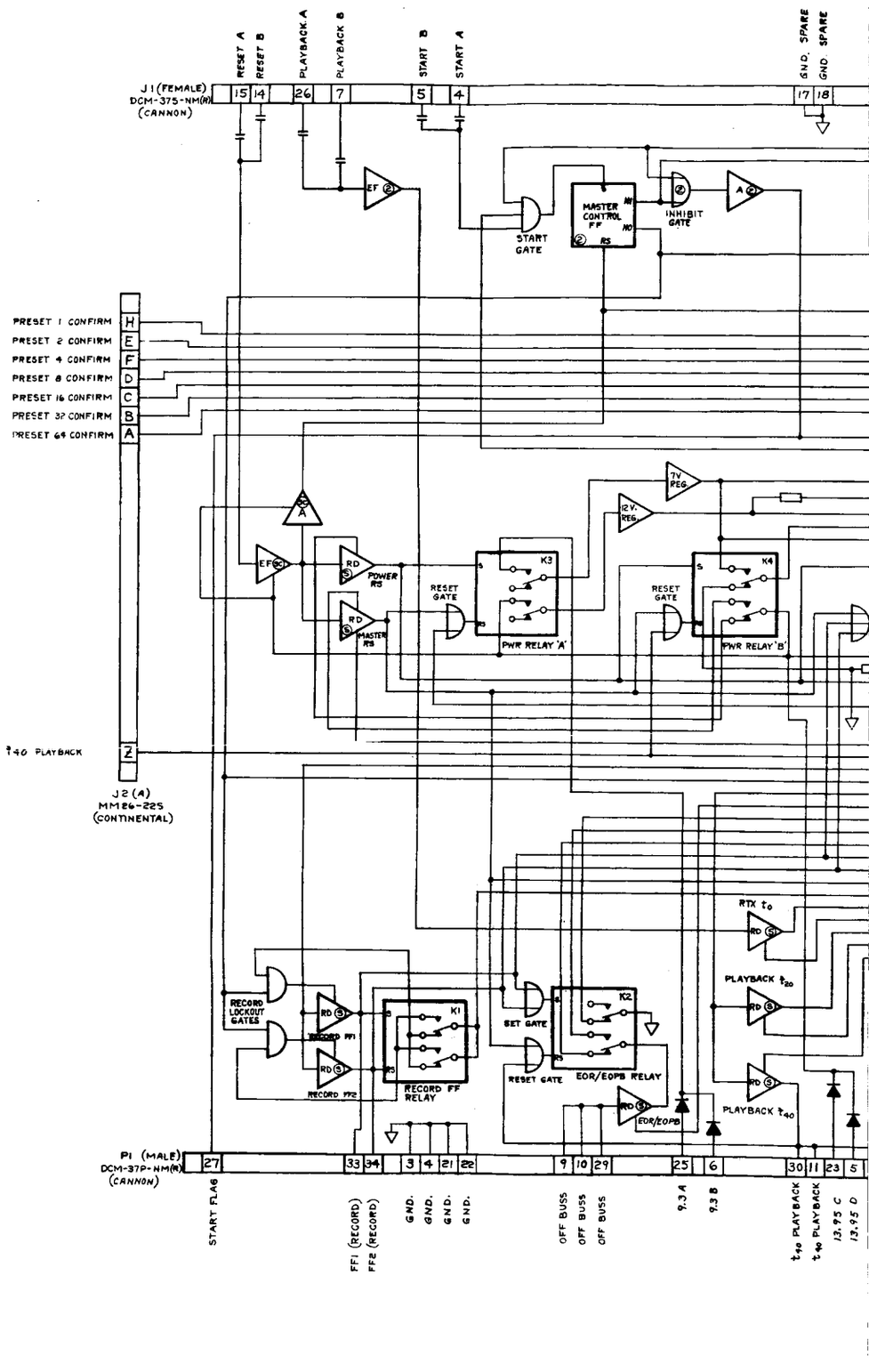
The delay timer and the elapsed time clock consist of diode-transistor logic counter-type flip-flops specially designed to provide high noise immunity and maximum reliability. Triggering threshold levels were set at approximately 2 volts, about 30 percent of the available triggering amplitude. Special considerations were made to minimize ground-loop effects by careful routing and use of ground returns.

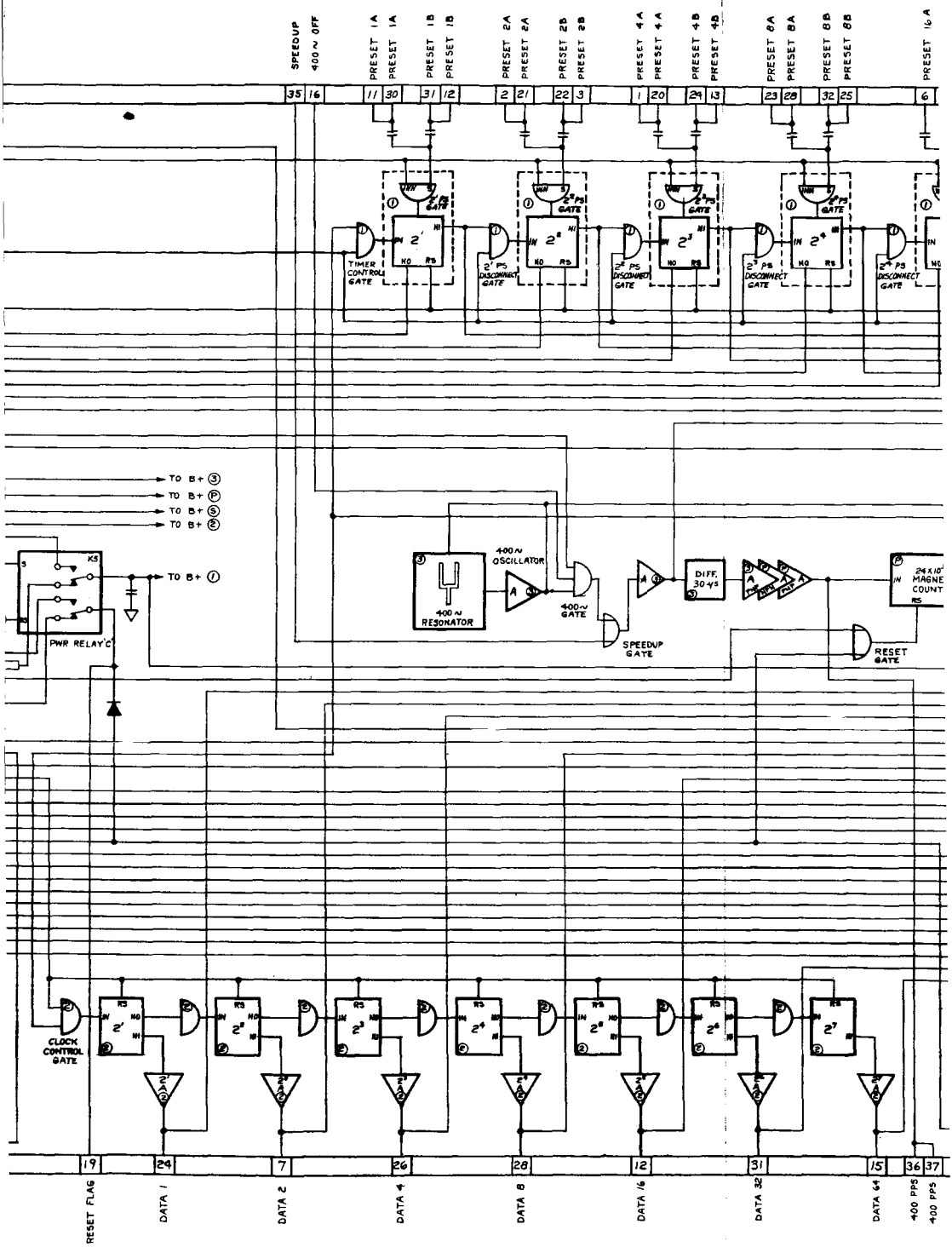
The outputs of the clock are buffered before being forwarded to the encoder to minimize undesirable loading of the clock as well as to isolate the clock from extraneous externally-generated noise voltages. Clock data are in the form of a seven-bit binary code.

The purpose of the clock is to provide elapsed time updated on a minute-by-minute basis in synchronism with the delay timer, but active for a longer duration, in order to serve as a timebase for verifying the delay timer's operation.

The delay timer is quite similar to the clock with these exceptions:

- It can be programmed externally from a command source to assume an updated timecode whose completion cycle is in the form of the desired delay time.


J1 (FEMALE)
DCM-37S-NM(R)
(CANNON)
RESET A
RESET B
PLAYBACK A
PLAYBACK B
START B
START A
GND. SPARE
GND. SPARE
15
14
26
7
5
4
17
18
EF
START GATE
MASTER CONTROL FF
INHIBIT GATE
A
PRESET 1 CONFIRM
PRESET 2 CONFIRM
PRESET 4 CONFIRM
PRESET 8 CONFIRM
PRESET 16 CONFIRM
PRESET 32 CONFIRM
PRESET 64 CONFIRM
H
E
F
D
C
B
A
7V REG.
12V REG.
RD
POWER RS
MASTER RS
RESET GATE
K3
PWR RELAY 'A'
K4
PWR RELAY 'B'
t40 PLAYBACK
Z
J2 (A)
MM86-225
(CONTINENTAL)
RTX t0
PLAYBACK t20
PLAYBACK t40
RECORD LOCKOUT GATES
RECORD FF1
RECORD FF2
K1
RECORD FF RELAY
SET GATE
K2
RESET GATE
EOR/EOPB RELAY
EOR/EOPB
P1 (MALE)
DCM-37P-NM(R)
(CANNON)
27
33
34
3
4
21
22
9
10
29
25
6
30
11
23
5
START FLAG
FF1 (RECORD)
FF2 (RECORD)
GND.
GND.
GND.
GND.
OFF BUSS
OFF BUSS
OFF BUSS
9.3 A
9.3 B
t40 PLAYBACK
t40 PLAYBACK
13.95 C
13.95 D


SPEEDUP
400 ~ OFF
PRESET 1A
PRESET 1A
PRESET 1B
PRESET 1B
PRESET 2A
PRESET 2A
PRESET 2B
PRESET 2B
PRESET 4A
PRESET 4A
PRESET 4B
PRESET 4B
PRESET 8A
PRESET 8A
PRESET 8B
PRESET 8B
PRESET 16A
35
16
11
30
31
12
2
21
22
3
1
20
24
13
23
28
32
25
6
TIMER CONTROL GATE
2' PS DISCONNECT GATE
2² PS DISCONNECT GATE
2³ PS DISCONNECT GATE
2⁴ PS DISCONNECT GATE
TO B+ ③
TO B+ Ⓟ
TO B+ ⑤
TO B+ ②
TO B+ ①
K5
PWR RELAY'C'
400 ~ RESONATOR
400 ~ OSCILLATOR
400 ~ GATE
SPEEDUP GATE
DIFF. 30 μs
RESET GATE
CLOCK CONTROL GATE
RESET FLAG
DATA 1
DATA 2
DATA 4
DATA 8
DATA 16
DATA 32
DATA 64
400 PPS
400 PPS
19
24
7
26
28
12
31
15
36
37

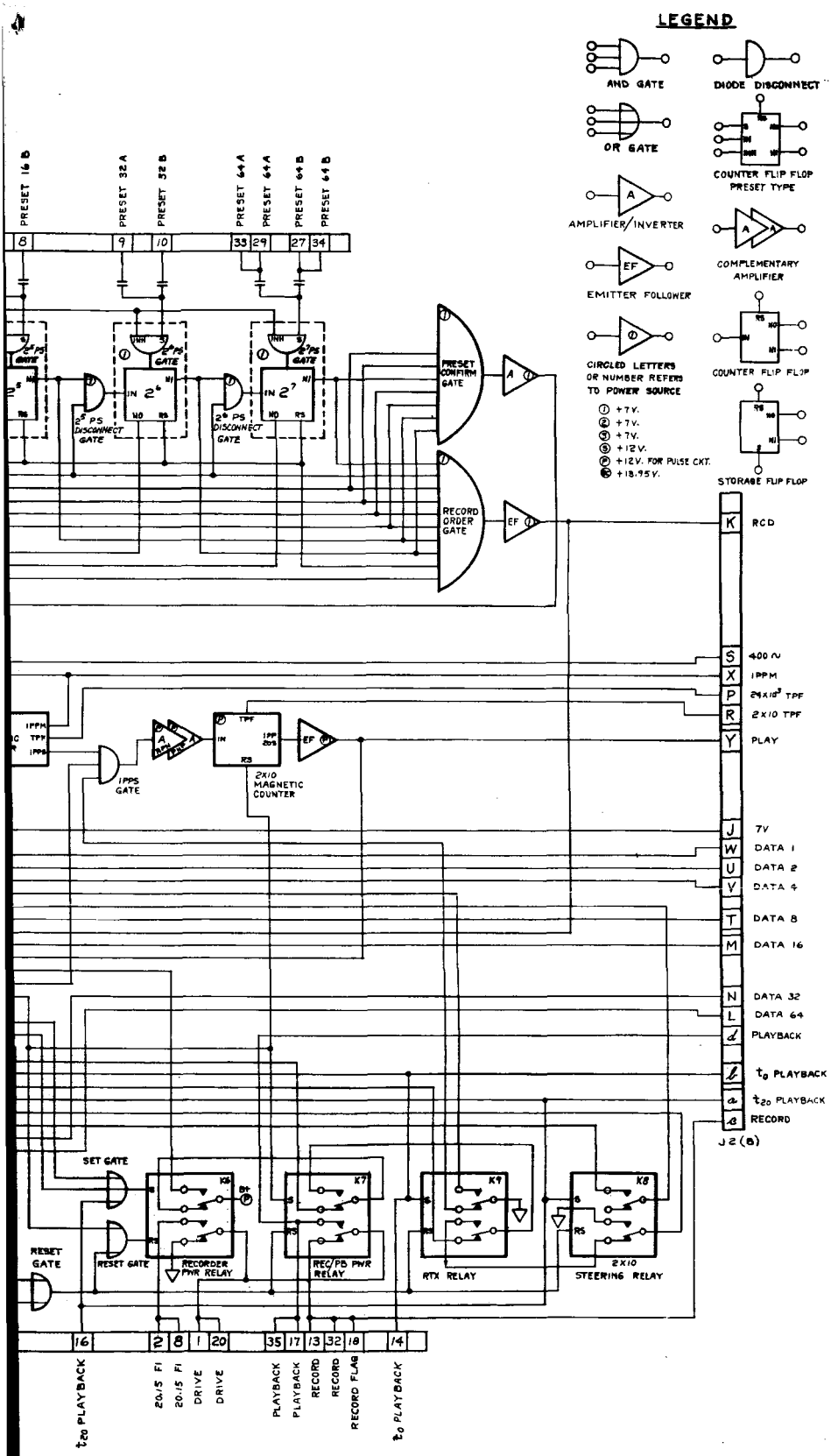


Figure 2. Clock and Timer Electronics, Logic Diagram

■ = ON LINE

EVENT	POWER SOURCE						TOTAL CURRENT vs EVENT 9.3 v (ma)	TOTAL CURRENT vs EVENT 13.95 v (ma)	PEAK CHARGE CURRENT 13.95 v (ma)
	9.3 VOLT PACK			13.95 VOLT PACK					
	① +7 v 2.8 ma	② +7 v 6.5 ma	③ +7 v 2.0 ma	Ⓢ +12 v 1.6 ma	Ⓟ +12 v 1.2 ma	Ⓢⓒ +13.95 v 0.11 ma			
RESET COMMAND (NO HORN)						■	0.0	0.11	0.15
RESET COMMAND (HORN)	■	■	■	■		■	11.3	1.7	2.2
PRESET COMMAND (S)	■	■	■	■		■	11.3	1.7	1.7
START COMMAND (HORN)	■	■	■	■	■	■	11.1	2.9	3.3
RECORD		■	■	■	■	■	8.3	1.9	2.3
OFF BUS		■	■	■	■	■	8.3	1.9	2.3
PLAYBACK COMMAND		■	■	■	■	■	8.3	1.9	2.7
$t_0 - t_{20}$		■	■	■	■	■	8.3	1.9	2.7
$t_{20} - t_{40}$		■	■	■	■	■	8.5	1.9	2.3
t_{40}			■	■	■	■	2.0	1.9	2.5
OFF BUS						■	0.0	0.11	0.12
RESET COMMAND (HORN)	■	■	■	■		■	11.3	1.7	2.2
RESET COMMAND (NO HORN)						■	0.0	0.11	0.12
RESET COMMAND (HORN)	■	■	■	■		■	11.3	1.7	2.2
PRESET COMMAND (S)	■	■	■	■		■	11.3	1.7	1.7
START COMMAND (HORN)	■	■	■	■	■	■	11.1	2.9	3.3
RECORD		■	■	■	■	■	8.3	1.9	2.3
OFF BUS		■	■	■	■	■	8.3	1.9	2.3
PLAYBACK COMMAND		■	■	■	■	■	8.3	1.9	2.7
$t_0 - t_{20}$		■	■	■	■	■	8.3	1.9	2.7
$t_{20} - t_{40}$		■	■	■	■	■	8.5	1.9	2.3
t_{40}			■	■	■	■	2.0	1.9	2.5
RESET COMMAND (HORN)	■	■	■	■	■	■	11.1	2.9	3.4
PRESET COMMAND (S)	■	■	■	■	■	■	11.1	2.9	2.9
OFF BUS	■	■	■	■		■	11.3	1.7	1.7
START COMMAND (HORN)	■	■	■	■	■	■	11.1	2.9	3.3

Figure 3. Power Cross Section

- Internal binary information is fed to a strobed gate to yield the record order at the completion of count-up.

- This binary information is also fed to a gate which prevents the start command from becoming operable until at least one preset bit is installed in the timer.

- A disconnect system to permit delay timecode programming.

Control of the timing source, timer, and clock is the prime function of the master control flip-flop. At reset command this flip-flop:

- Prepares the timer to accept and store delay-time information

- Controls the transmission of 400 cycles to the shaping and counting circuits

- Places the clock in a ready status

A secondary function is to inhibit premature recorder turn-on by disarming the relay drivers.

At start command the master control:

- Enables timer operation

- Prevents the introduction of any additional timecode information

- Enables the 400-cps timing source

- Enables the operation of the elapsed time clock

Latch relays switched by silicon-controlled rectifiers switch the record drive, record electronics, and playback electronics. High-powered output pulses (t_0 playback, t_{20} playback, t_{40} playback, FF_1 (record), and FF_2 (record)) are derived through SCR circuitry also.

Voltage regulation is performed by two regulators: a 7-volt regulator working from a 9.3-volt source, and a 12-volt regulator working from a 13.95-volt source. Three power-disconnect relays switch power busses to meet prevailing requirements and conserve power.

To maintain functional switching on a truly sequential basis, SCR drive circuits are gated by switching anode power through contacts available on power

switching and other latch relays. This feature prevents occurrence of a function such as playback until after all the required preceding functions have taken place.

Command System

Reset command — The reset command is used to place the system into one of two distinct modes on an alternate or non-alternate basis, depending upon the program event in process at the time of reset command transmission. A reset command (horn) may be applied 45 seconds after the application of the 9.3-volt and 13.95-volt power sources. This command resets the entire clock and timer electronics system and prepares it for delay-time preset information. A second reset command (no horn) applied a minimum of 45 seconds after the first returns the system to a de-energized status. This reset action is alternate in nature and may be used to abort, clear, or recycle the system during any program event before t_{40} playback.

Transmission of a reset command (horn) after t_{40} playback (non-alternate) energizes the de-energized logic systems. Insertion of a new delay-time program is now possible during the recorder playback mode. This feature permits the immediate transmission of a start command after playback termination. Note that a reset command transmission after t_{40} playback must be delayed a minimum of 45 seconds after t_{40} playback has been observed.

Preset commands — The preset commands program the timer with a seven-bit binary delay timecode. Entries can be made immediately after the reset command (horn) in serial or parallel fashion. Changes to the entry can be made only by transmitting a reset command (no horn), followed 45 seconds later by a reset command (horn).

Start command — This command begins the clock and timer operation. A start horn verifies command execution providing that reset (horn) and preset commands were received. At least one bit of delay-time information must be in the timer register before the system can be started.

Playback command — The playback command initiates the t_0 playback through t_{40} playback series of events which includes energizing the playback system. Its acceptance depends upon the completion of previous sequential events. The action of the OFF bus signal from programmer No. 1 in terminating the record mode is the playback-command arming feature. A minimum delay of 45 seconds after the OFF bus signal is required before playback-command transmission.

FUNCTIONAL SEQUENCE

Operational procedures required to program the clock and timer electronics are:

(1) Power 9.3 volts, 13.95 volts, and 20.15 volts

(2) 45-second wait

(3) Reset command (horn)

(4) Preset command(s) (timecode entry)

(5) Start command (horn) (delay runs out, recorder energizes, OFF bus terminates record mode)

(6) 45-second minimum wait after termination of record mode and before playback command

(7) Playback command (t_0 playback through t_{40} playback, OFF bus terminates playback mode)

If new time code entry is to be made during playback mode, then:

(8) 45-second wait after t_{40} playback

(9) Reset command (horn)

(10) Preset command(s) (new timecode entry)

(11) Start command (horn) after OFF bus terminates playback mode

This format and other sequences are diagrammed in Figure 4.

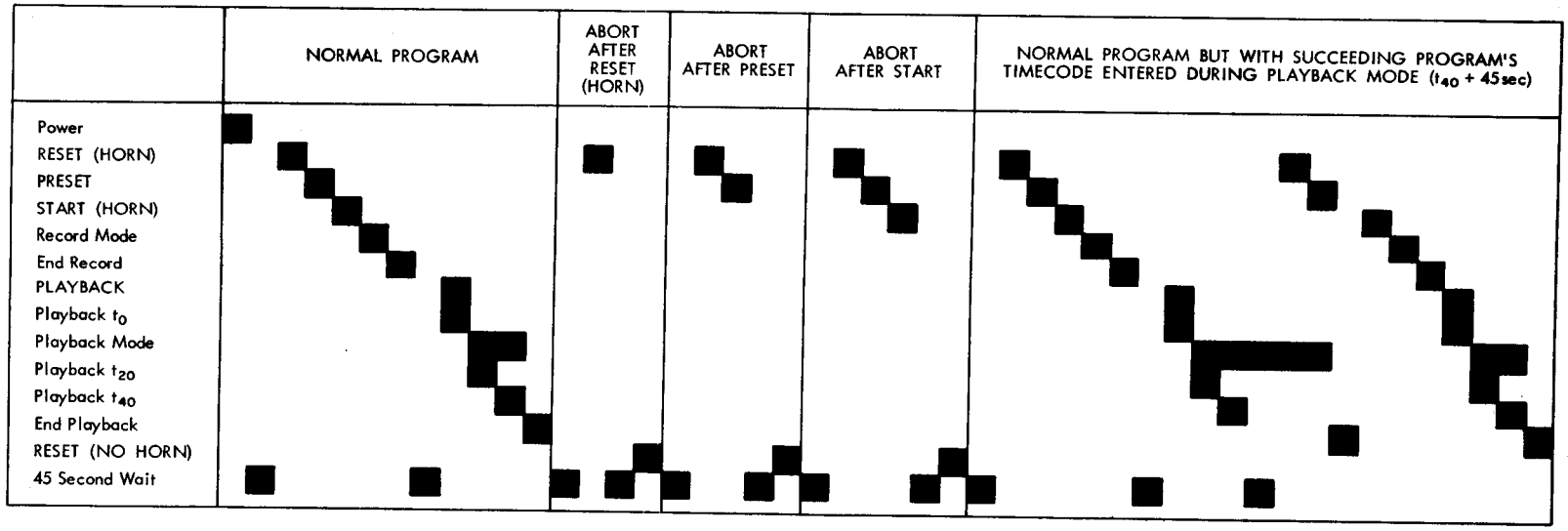


Figure 4. Sequence Format

SPECIFICATIONS

Mechanical

Size:	5 x 7 x 1-1/4 inches
Weight:	760 grams; 840 grams potted
Connectors:	J-1 Cannon DCM-37S-NMC-2 (commands)
	P-1 Cannon DCM-37P-NMC-2 (power, switching, & signals)
	J-2 Continental MM-26-22S (test points)
Construction:	Welded-modular
Potting:	Eccofoam FP8, 10 lb per ft^3

Electrical

Power: 9.3 volts - O.D. mw (OFF), 20-110 mw range (ON)

13.95 volts - 1.5 mw (OFF), 10-40 mw range (ON)

20.15 volts - recording system switching

Components:

Transistors	63
Diodes	266
Zener diodes	2
Capacitors	76
Resistors	294
Relays	9
Incremental counters	2
Resonators	1

Environmental

Operating temperature range: -20° C to +60° C.

Other environmental information may be found in AE-B specification literature.

Connector Pin Assignments

J-1 DCM-37S-NMC-2 (Cannon)

1. Preset 4A
2. Preset 2A
3. Preset 2B
4. Start A
5. Start B
6. Preset 16A
7. Playback B
8. Preset 16B
9. Preset 32A
10. Preset 32B
11. Preset 1A
12. Preset 1B
13. Preset 4B
14. Reset B
15. Reset A
16. 400 ~ OFF
17. gnd spare
18. gnd spare
19. N.c.
20. Preset 4A
21. Preset 2A
22. Preset 2B
23. Preset 8A
24. Preset 4B
25. Preset 8B
26. Playback A
27. Preset 64B
28. Preset 8A
29. Preset 64A
30. Preset 1A
31. Preset 1B
32. Preset 8B
33. Preset 64A
34. Preset 64B
35. Speedup
36. N.c.
37. N.c.

P-1 DCM-37P-NMC-2 (Cannon)

1. Drive
2. 20.15 F_1
3. gnd
4. gnd
5. 13.95 D
6. 9.3 B
7. Data 2
8. 20.15 F_1
9. OFF bus
10. OFF bus
11. t_{40} playback
12. Data 16
13. Record
14. t_0 playback
15. Data 64
16. t_{20} playback
17. Playback
18. Record flag
19. Reset flag
20. Drive
21. gnd
22. gnd
23. 13.95 C
24. Data 1
25. 9.3 A
26. Data 4
27. Start flag
28. Data 8
29. OFF bus
30. t_{40} playback
31. Data 32
32. Record
33. FF_1 (record)
34. FF_2 (record)
35. Playback
36. 400-pps
37. 400-pps

J-2 MM26-22S (Continental) Test Points

A. Preset 64 confirm
B. Preset 32 confirm
C. Preset 16 confirm
D. Preset 8 confirm
E. Preset 4 confirm
F. Preset 2 confirm
L. Data 64
M. Data 16
N. Data 32
P. 24×10^3 TPF
R. 2x10TPF
S. 400~
W. Data 1
X. 1-ppm
Y. Play
Z. t_{40} playback
a. t_{20} playback
b. t_0 playback

H. **Preset 1 confirm**

J. 7v

K. **Record**

T. **Data 8**

U. **Data 2**

V. **Data 4**

c. **Record**

d. **Playback**

Figure A-1. Module Photograph, Top View

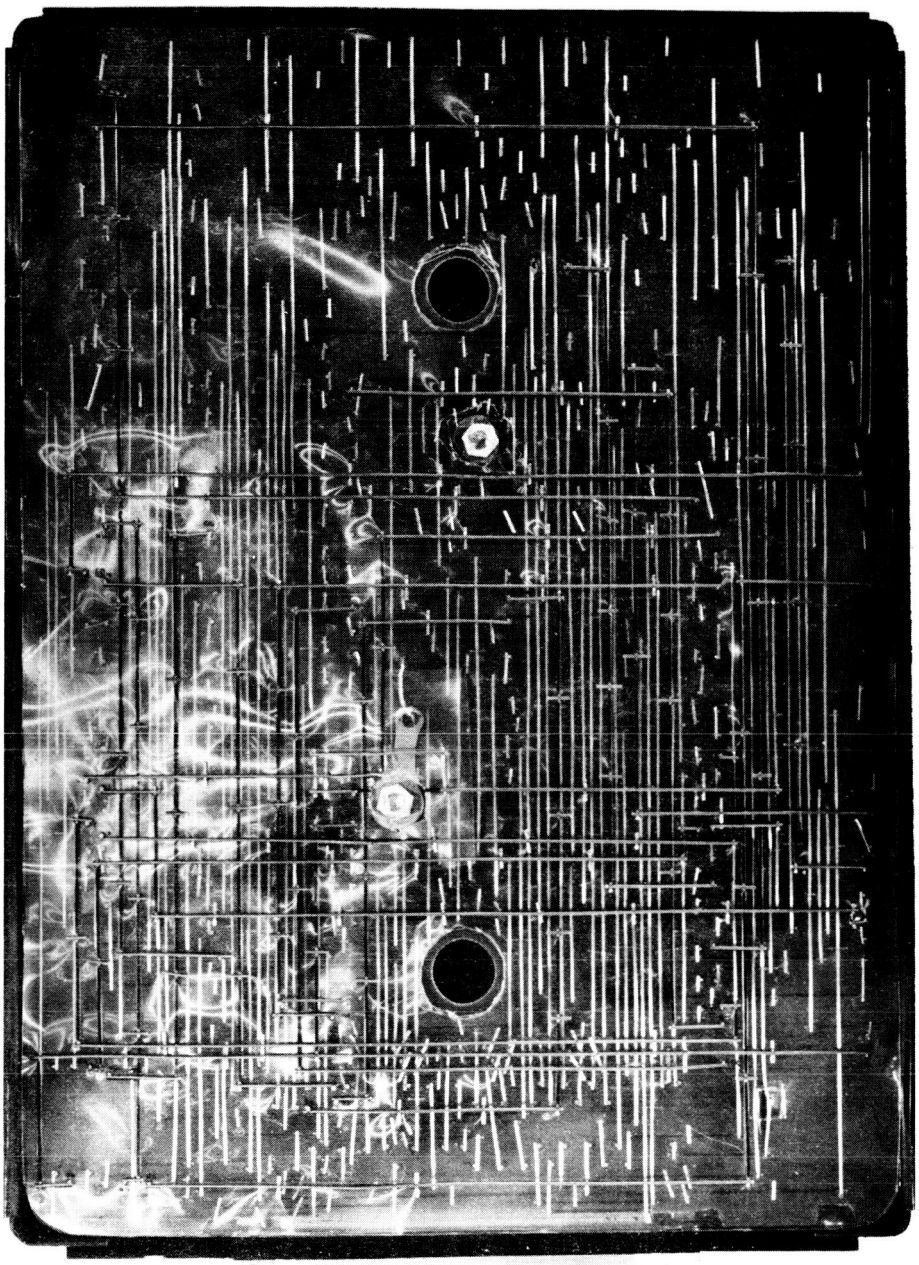


Figure A-2. Module Photograph, Bottom View

J07B-01

PIN	CONNECTION	FUNCTION
1	J08B-01-03	+20 FI-TAPE DRIVE
2	P01F-01-16	20.15 (FI) IN
3	P01A-01-12	SYSCOM A
4	P01B-01-28	SYSCOM B
5	P01D-01-05	13.95 D IN
6	P01B-01-20	9.3 B IN
7	J04B-02-04	CLOCK DATA 2 OUT
8	P01F-01-19	20.15 (FI) IN
9	J07C-01-03	OFF BUSS IN
10	J07C-01-36	OFF BUSS IN
11	J07C-01-28	T_{40} PLAYBACK OUT
12	J04B-02-01	CLOCK DATA 16 OUT
13	J08A-01-06	RECORD 20FI OUT
14	J07C-01-11	T_8 PLAYBACK OUT
15	J04B-01-04	CLOCK DATA 64 OUT
16	J07C-01-21	T_{20} PLAYBACK OUT
17	J08A-01-07	PLAYBACK 20 FI OUT
18	J04B-02-06	PLAYBACK FLAG
19	J03A-01-11	CLOCK RESET
20	J08B-01-04	+20 FI-TAPE DRIVE
21	P01C-01-14	SYSCOM C
22	P01D-01-28	SYSCOM D
23	P01C-01-25	13.95C IN
24	J04B-02-05	CLOCK DATA 1 OUT
25	P01A-01-06	9.3 A IN
26	J04B-02-03	CLOCK DATA 4 OUT
27	J03A-01-06	START SIGNAL
28	J04B-02-02	CLOCK DATA 8 OUT
29	N.C.	OFF BUSS OUT
30	J07C-01-27	T_{40} PLAYBACK OUT
31	J04B-01-25	CLOCK DATA 32 OUT
32	J08A-01-18	RECORD 20 FI OUT
33	J07C-01-31	RECORD OUT (FFI)
34	J07C-01-14	RECORD OUT (FFII)
35	J08A-01-19	PLAYBACK 20 FI OUT
36	J08B-01-07	400 PPS OUT
37	J08B-01-19	400 PPS OUT

J07B-02

PIN	CONNECTION	FUNCTION
1	J02B-01-02	CH 17A IN
2	J02B-01-36	CH 16A IN
3	J02D-01-36	CH 16B IN
4	J02B-01-11	CH 22A IN
5	J02D-01-11	CH 22B IN
6	J02B-01-18	CH 19A IN
7	J02D-01-04	CH 13B IN
8	J02D-01-18	CH 19B IN
9	J02B-01-34	CH 20A IN
10	J02D-01-34	CH 20A IN
11	J02B-01-05	CH 15A IN
12	J02D-01-05	CH 15B IN
13	J02D-01-02	CH 17B IN
14	J02D-01-20	CH 14B IN
15	J02B-01-20	CH 14A IN
16	N.C.	T.P. 400 /\ OFF
17	S.P.	SYSCOM C
18	S.P.	SYSCOM D
19	N.C.	
20	J07D-01-31	CH 17A OUT
21	J07D-01-37	CH 16A OUT
22	J07D-01-19	CH 16B OUT
23	J02B-01-35	CH 18A IN
24	J07D-01-33	CH 17B OUT
25	J02D-01-35	CH 18B IN
26	J02B-01-04	CH 13A IN
27	J02D-01-27	CH 21B IN
28	J07D-01-35	CH 18A OUT
29	J02B-01-27	CH 21A IN
30	J07D-01-01	CH 15A OUT
31	J07D-01-03	CH 13B OUT
32	J07D-01-17	CH 18B OUT
33	S.P.	
34	S.P.	
35	S.P.	
36	S.P.	
37	S.P.	

J1 (FEMALE)
DCM 37S-NM(E)
(CANNON)

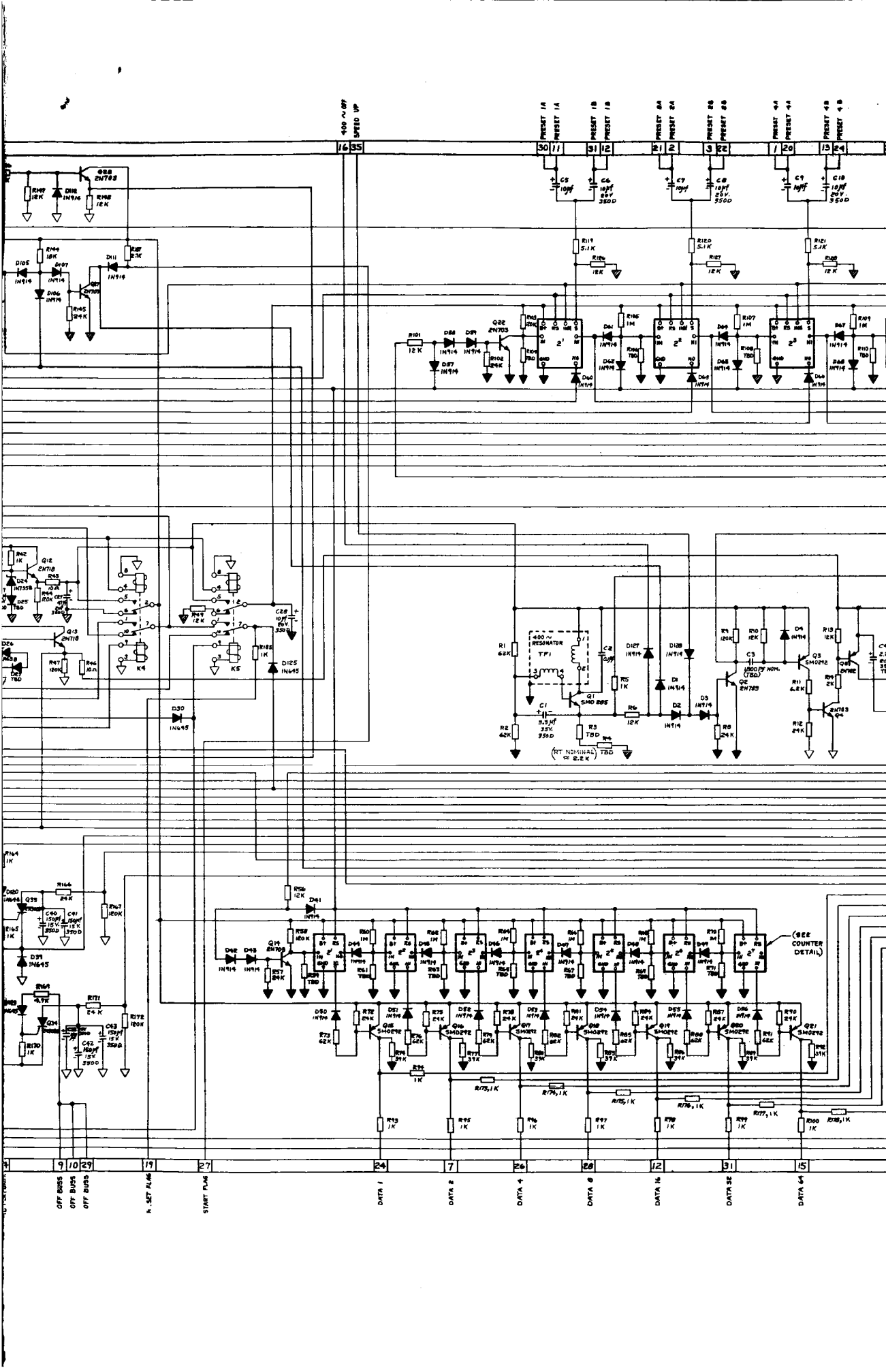
PRESET 1 CONFIRM H
PRESET 2 CONFIRM E
PRESET 4 CONFIRM F
PRESET 8 CONFIRM D
PRESET 16 CONFIRM C
PRESET 32 CONFIRM B
PRESET 64 CONFIRM A

T_{40} PLAYBACK Z
T_{20} PLAYBACK a

J2(A)
MM26-225
(CONTINENTAL)

P1 (MALE)
DCM 37P-NM(E)
CANNON

GND. A
GND. B
GND. C
GND. D
13.95 C
13.95 D
FFI (RECORD)
FFII (RECORD)
T_{20} PLAYBACK
T_{40} PLAYBACK
T_{40} PLAYBACK
9.3 A
9.3 B


400 ~/ OFF
SPEED UP
PRESET 1A
PRESET 1B
PRESET 2A
PRESET 2B
PRESET 4A
PRESET 4B
PRESET 8A
PRESET 8B
16
35
30
11
31
12
2
3
22
1
20
13
24
Q28 2N708
R149 12K
D118 IN916
R148 12K
C5 10pf
C6 10pf 25V. 350D
C7 10pf
C8 10pf 25V. 350D
C9 10pf
C10 10pf 25V. 350D
D105 IN914
D107 IN914
D106 IN914
D111 IN914
R145 24K
Q27 2N708
R119 5.1K
R120 5.1K
R121 5.1K
R124 12K
R127 12K
R128 12K
R101 12K
D86 IN914
D87 IN914
Q22 2N703
R102 24K
D87 IN914
D88 IN914
D89 IN914
D90 IN914
R106 1M
R107 1M
R109 1M
R110 TBD
R103 TBD
R104 TBD
R105 TBD
R108 TBD
2^1
2^2
2^3
R1 62K
R2 62K
R3 TBD
R4 TBD
(RT NOMINAL ≈ 2.2K)
400 ~/ RESONATOR TF1
C1 .5 Mf 35V 350D
C2 .05f
R5 1K
R6 12K
Q1 SMD 885
D127 IN914
D128 IN914
D1 IN914
D2 IN914
D3 IN914
R7 24K
R8 24K
R9 2K
R10 12K
R11 4.2K
R12 24K
R13 12K
C3 (800 PF NOM. (TBD))
Q2 2N769
Q3 SM0212
Q4 2N783
D4 IN914
Q12 2N718
D24 IN755B
R42 1K
R43 .02
R44 120K
C27 47Mf 35V
Q13 2N718
D26 TBD
R47 120K
R46 10K
K4
K5
R48 12K
C28 10Mf 25V 350D
R185 1K
D125 IN645
D30 IN645
R164 24K
R167 120K
D39 IN645
R169 4.7K
R171 24K
R172 120K
R170 1K
C40 150pf 15V 350D
C41 150pf 15V 350D
C42 150pf 15V 350D
C43 150pf 15V 350D
Q34 2N708
Q35 2N708
R56 12K
D41 IN914
Q14 2N703
R58 120K
R57 24K
R59 TBD
D42 IN914
D43 IN914
R60 1M
R61 TBD
R62 1M
R63 TBD
R64 1M
R65 TBD
R66 1M
R67 TBD
R68 1M
R69 TBD
R70 1M
R71 TBD
D44 IN914
D45 IN914
D46 IN914
D47 IN914
D48 IN914
D49 IN914
D50 IN914
D51 IN914
D52 IN914
D53 IN914
D54 IN914
D55 IN914
D56 IN914
D57 IN914
(SEE COUNTER DETAIL)
R72 24K
R73 62K
R74 24K
R75 62K
R76 24K
R77 62K
R78 24K
R79 62K
R80 24K
R81 62K
R82 24K
R83 62K
R84 24K
R85 62K
R86 24K
R87 62K
R88 24K
R89 62K
R90 24K
R91 62K
R92 24K
R93 62K
Q15 SM0212
Q16 SM0212
Q17 SM0212
Q18 SM0212
Q19 SM0212
Q20 SM0212
Q21 SM0212
R94 1K
R95 1K
R96 1K
R97 1K
R98 1K
R99 1K
R100 1K
R175, 1K
R176, 1K
R177, 1K
R178, 1K
9
10
29
19
27
24
7
26
28
12
31
15
OFF BUSS
OFF BUSS
OFF BUSS
K. SET FLAG
START FLAG
DATA 1
DATA 2
DATA 4
DATA 8
DATA 16
DATA 32
DATA 64

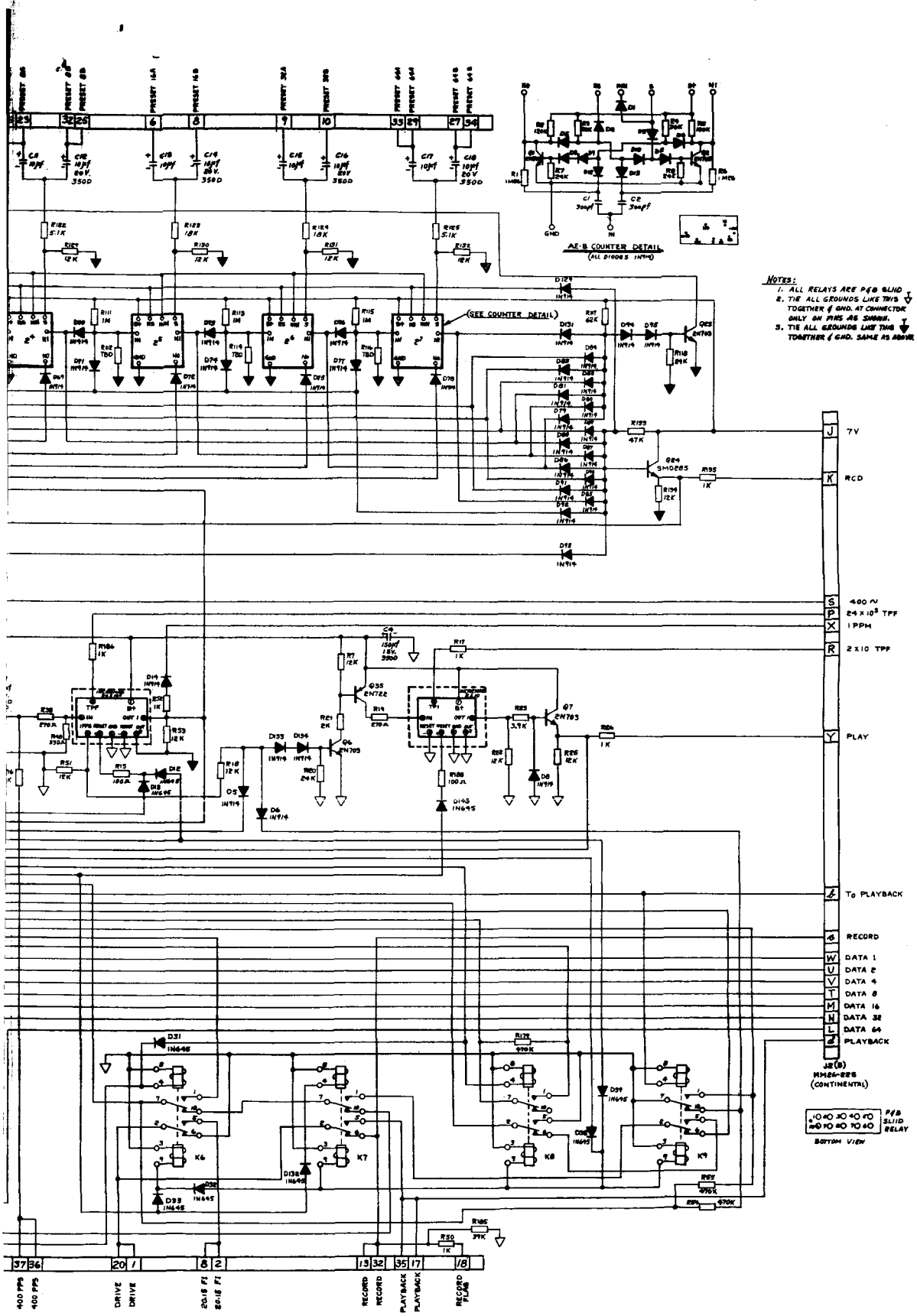


Figure A-3. Clock and Timer Electronics, Schematic Diagram