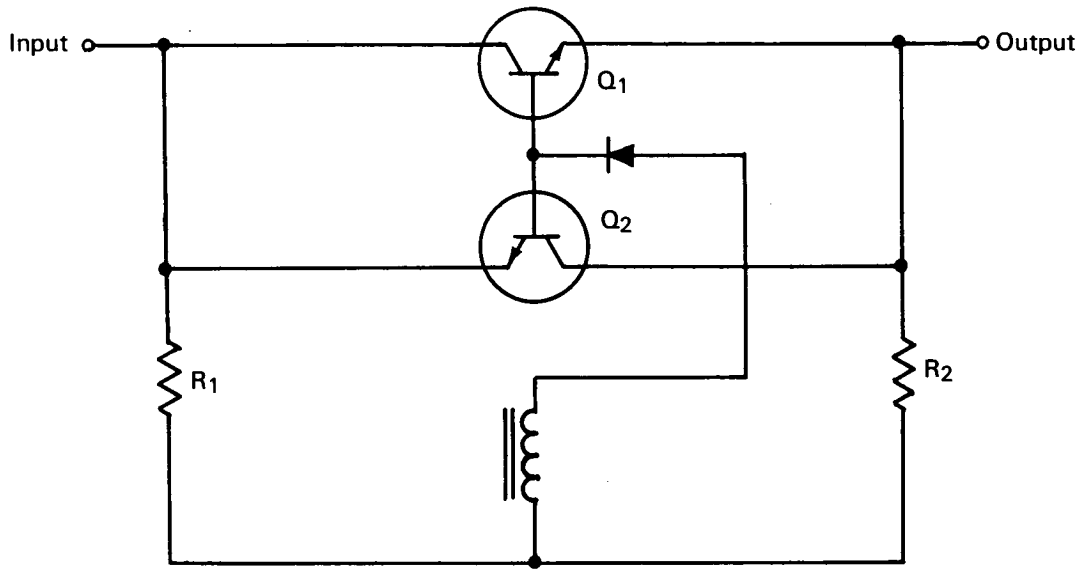
NASA TECH BRIEF

Improved Chopper Circuit Uses Parallel Transistors



The problem:

To develop a transistor chopper circuit with improved performance over that of a series transistor chopper circuit. In the series circuit the saturation resistances of the transistor pair add and become one of the major causes of chopper loss. The series circuit also requires close matching of transistors in order to accomplish cancellation of the offset voltages appearing at the outputs due to base drive current in the transistor junctions. Matched characteristics degrade during the operating life of the transistors causing degraded chopper performance.

The solution:

A parallel transistor chopper circuit in which one transistor operates in the forward mode and the other operates in the inverse mode, thus acting as a single, symmetrical, bidirectional transistor.

How it's done:

The active chopping element is composed of Q_1 and Q_2 operating in parallel. The transformer (only the secondary is shown) couples the chopper drive signal into the chopping element. The peak amplitude of the chopper drive signal is adjusted to be greater than the maximum input voltage being chopped to prevent the input signal from overriding the chopper drive signal. This prevents the transistor pair from turning on when the chopper drive signal is in the negative half of its cycle.

When the drive signal is in the negative half of its cycle, the diode will be reverse biased, blocking the

(continued overleaf)

flow of base current and turning off the transistor pair. The chopping element leakage during this portion of the cycle is determined by the sum of resistances R_1 and R_2. The use of planar construction in the transistors allows satisfactory operation in this half of the cycle, without negative base voltage, to insure cutoff.

When the drive signal is in the positive half of its cycle, the diode will be forward biased and current from the transformer will flow to the bases of Q_1 and Q_2. Current will flow through the collector-base junction of Q_1 and the emitter-base junction of Q_2 in parallel and back to the transformer through R_1. At the same time, current will also flow through the emitter-base junction of Q_1 and the collector-base junction of Q_2 in parallel back to the transformer through R_2. All four transistor junctions are thus biased on, enabling the transistor pair to conduct current from the input voltage source to the output in either direction.

The parallel circuit has a combined saturation resistance two to four times less than the series circuit. The voltage developed in one junction is partly cancelled by the voltage developed in the other junction. Only the difference of these voltages appears from collector to emitter. The transistor operating in the inverse mode (lowest saturation resistance) shunts the voltage difference developed by the transistor operating in the forward mode, thus further reducing and stabilizing the offset voltage.

Notes:

1. The sum of the emitter-base breakdown voltages for the two transistors determines the maximum input voltage that can be chopped.
2. Resistors R_1 and R_2 should be equal in value to within a few percent to insure good symmetry and low offset voltages. The value of the resistors should be selected so that the average base current from either resistor will be slightly greater than the maximum current being chopped. Increasing the base current beyond this point will give slightly lower saturation resistance at the expense of increased chopper noise.
3. Inquiries concerning this invention may be directed to:

   Technology Utilization Officer
   Marshall Space Flight Center
   Huntsville, Alabama, 35812
   Reference: B66-10113

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C., 20546.

Source: International Business Machines
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Marshall Space Flight Center
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