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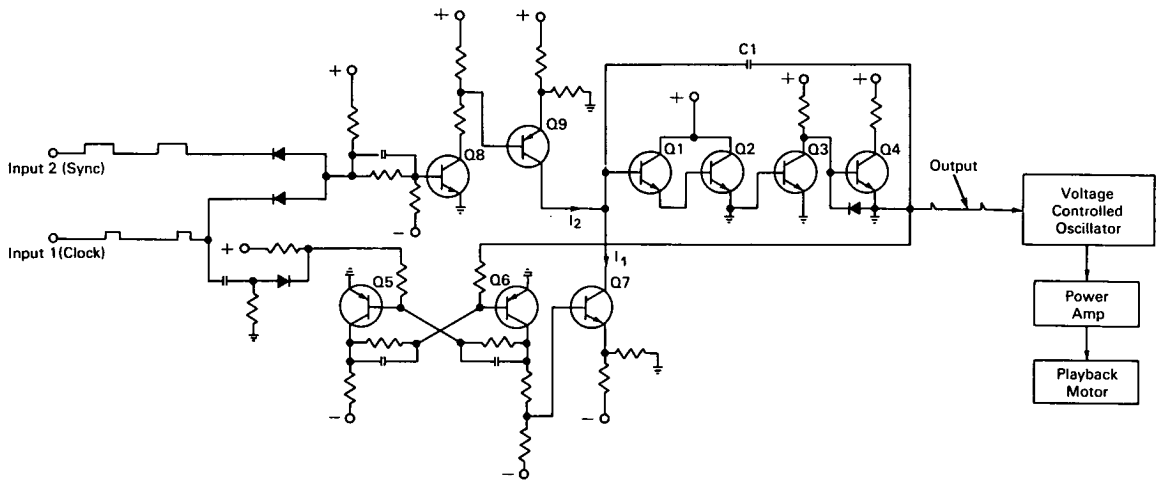
NASA TECH BRIEF

Electronic Phase-Locked-Loop Speed Control System Is Stable



The problem:

To design a stable speed control circuit for playback motors used in digital tape recorders where the reproducer output must remain in exact synchronism with an external reference clock over extended periods. Electromechanical speed control systems which have been used for tape recorders are inherently unstable and require damping to prevent oscillation.

The solution:

A phase-locked-loop circuit that permits phase comparison of two signals whose frequency is much less than the local oscillator frequency (the local oscillator frequency is divided before its signal reaches the phase comparator), and thereby removes the motor dynamics from the control loop dynamics, so that the loop is stable without damping.

How it's done:

A phase error or time displacement between the frequency of the sync pulses and the reference clock input of somewhat less than $\pm 1/2$ bit is permitted, so that the reference clock pulses are approximately 1 bit wide. These pulses are applied to input 1. The sync pulses from the tape are converted to a square wave by a one-shot multivibrator and applied to input 2.

Transistors Q1, Q2, Q3 and Q4 and capacitor C1 act as an electronic integrator. Transistors Q5, Q6, and Q7 are used to establish the initial condition of the integrator. Transistors Q8 and Q9 control the integration process. At the beginning of the reference clock pulse, Q5 is pulsed to turn on Q7. This action initiates a large current, I_1, which produces a rapid rise in the integrator output voltage. When this voltage reaches a predetermined value, Q6 shuts off Q7. Then as long as there are pulses at inputs 1 and 2, the integrator output falls slowly. When either one of the pulses drops to zero, I_2 ceases to flow and the integrator output holds at some intermediate value until the next reset and integration. If input 1 tends to speed up, the resulting integrator output causes the playback motor to slow

(continued overleaf)

down. If input 1 tends to slow down, the resulting integrator output causes the motor to speed up. The tape speed is thus automatically readjusted whenever input 1 varies. Since the speed correction is made very quickly, the dynamics of a quick response motor do not cause instability. The memory feature of the integrator keeps the tape at constant speed during the integration period and permits comparison of very low frequency pulses (on the order of 1 cps).

Note:

Inquiries concerning this invention may be directed to:

Technology Utilization Officer
Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, California 91103
Reference: B66-10232

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

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