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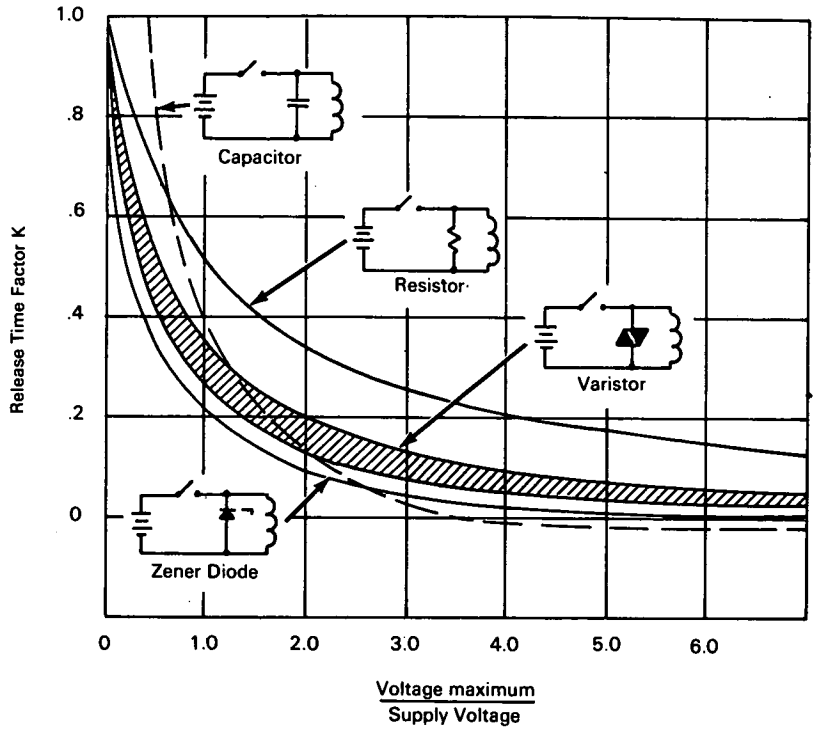
NASA TECH BRIEF

Basic Suppression Techniques Are Evaluated



GENERALIZED PLOT OF RELEASE TIME FACTOR VS. NORMALIZED VOLTAGE MAXIMUM FOR FOUR BASIC SUPPRESSION CIRCUITS

The problem:

Switching of inductively loaded circuits often causes interference in adjacent electronic equipment. Suppression can be accomplished on an individual basis by trial and error using well known techniques. Such procedures are time consuming and it is difficult to design in advance for later use during system development.

The solution:

An investigation of standard suppression methods to facilitate straightforward and consistent designs of

(continued overleaf)

optimized circuits. The data are reduced to tabular form and rapid selection of components by the designer can be made without lengthy calculations or trial and error manipulations. Release times for four suppression cases are shown in the graph and a general evaluation of basic suppression techniques is presented in the following table.

GENERAL EVALUATION OF
BASIC SUPPRESSION TECHNIQUES

Suppression Techniques	1 Reliability	2 Effectiveness $V_m \leq E$	$V_m \leq 2E$	$V_m > 2E$	3 Arc Inhibiting Properties	4 Operate Interference	5 Physical Size	6 Design Complexity
Resistor	1	4-5	5	5	poor (2)	none	2	2
Capacitor	5 (1)	5-4	4	3-2	good	current-spike	5	5
Resistor-Capacitor	6	3	3-2	1	fair-good	Possible high currents	6	6
General purpose diode	3	6	–	–	fair (2)	none	1	1 (3)
Zener diode	4	1	1	2-3	poor (2)	none	3	3 (3)
Varistor	2	2	2-3	4	poor (2)	none	4	4

Notes:

(1) For ceramic capacitors the reliability is comparable to resistors. Ceramics should be used for small arc suppression capacitor. Electrolytic capacitors are the least reliable of any components tested.

(2) It is recommended that small arcing capacitors be used in these cases.

(3) Assumes an ideal component.

Column explanation:

1. Reliability: suppression circuits ranked in order of decreasing reliability.
2. Effectiveness: ranked in order of lowest attainable release time for voltage maxima indicated (first number of double rating corresponds to low region within each voltage range).
3. Arc Inhibiting Properties: (applies to arcs which occur across controlling switch contacts)
   good—usually prevents arcing.
   fair—arcing occurs but is greatly reduced.
   poor—arcing occurs and is somewhat reduced.
4. Operate Interference: type of interference that will be encountered (due to presence of suppression circuit) when the solenoid is energized.
5. Physical Size: ranked in increasing order.
6. Design Complexity: ranked in increasing order of design computation complexity.

Note:

Inquiries concerning this investigation may be directed to:

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No patent action is contemplated by NASA.

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