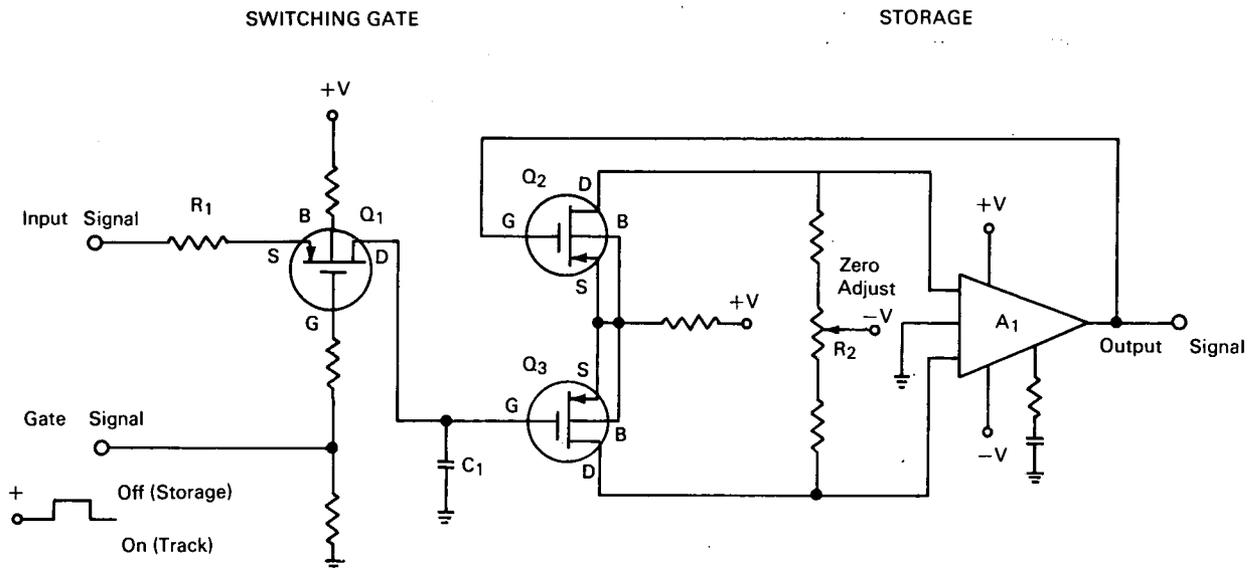


NASA TECH BRIEF



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MOSFET Analog Memory Circuit Achieves Long Duration Signal Storage



The problem:

To provide a means of maintaining the signal voltage at the output of an analog signal amplifier when the input signal is interrupted or removed. For some automatic control and instrumentation applications, it is desirable to store and read out the last signal level input received prior to signal interruption so that no information is lost during the absence of input signal. In addition to a signal-storage mode, the unit must have a tracking mode of operation during which the output voltage of the unit must duplicate the input voltage.

The solution:

A memory circuit using MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices as voltage-controlled switches, triggered by an external

voltage-sensing device. The circuit makes use of the zero offset switching capability and extremely high input impedance characteristics of MOSFET devices.

How it's done:

The memory unit is composed of three main parts: filter, R_1 , C_1 , to remove unwanted voltage variations or noise; an analog signal gate, Q_1 , to switch the unit between its two modes of operation (tracking mode and storage mode); and a highly accurate unity gain storage device, Q_2 , Q_3 , R_2 , A_1 , to provide a duplicate of the input voltage at its output terminals.

When the input signal is applied, an external sensing device turns the input gate, Q_1 , "on" and places the unit into its tracking mode of operation. The voltage on the capacitor, C_1 , represents the desired signal data and is applied to the unity gain amplifier, consisting of

(continued overleaf)

a pair of MOSFET devices, Q₂, Q₃, and an integrated operational amplifier, A₁. Balance control, R₂, is used to cancel any amplifier offset voltage.

Upon loss of input signal, the input gate is switched "off" by an external voltage-sensing device, thus converting the unit from a tracking mode to a storage mode of operation. The latest signal level received prior to signal dropout is stored in capacitor C₁ and is maintained at the output terminals of the circuit. Leakage of charge from capacitor C₁ through the two MOSFET devices, Q₁, Q₃, is impeded by the extremely high input and gate-off impedances of the MOSFET devices. Since the time constants of the capacitor-MOSFET impedances are extremely high, the voltage on the capacitor decays very slowly and can be considered essentially constant during the relatively short signal-dropout periods. When the input signal returns, the circuit is switched back into its tracking mode of operation by the external voltage-sensing device.

Notes:

1. Selection of a capacitor of proper material has resulted in time constants in the order of 10⁵ to 10⁶ seconds, values much larger than the longest signal dropout time anticipated.
2. The choice of time constant at the memory input is determined by the following:
 - a. Amount of smoothing required
 - b. Amount of decay encountered during switching time of gates
 - c. Expected time between signal dropouts
 - d. Time derivative of input signal
3. Inquiries concerning this innovation may be directed to:

Technology Utilization Officer
Marshall Space Flight Center
Huntsville, Alabama 35812
Reference: B66-10603

Patent status:

No patent action is contemplated by NASA.

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