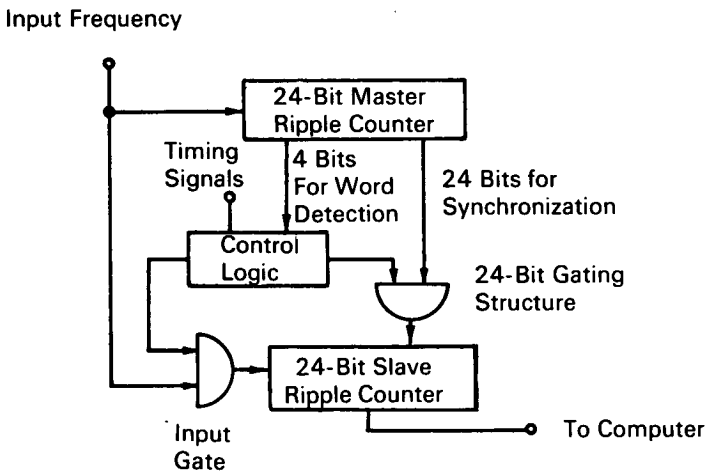
NASA TECH BRIEF

Digital Frequency Counter Permits Readout Without Disturbing Counting Process



The problem:

To devise a digital frequency counter that can be read out accurately at one-second intervals without interrupting or disturbing the counting process. This counter is to be used to monitor the frequency of a programmed exciter that serves as a local oscillator capable of providing frequencies from 0 to 50 Mc/sec in steps of 0.01 cps. Previous counters required an inordinate amount of gating logic and high circuit speed.

The solution:

A system incorporating a master counter and a slave counter with novel logic interconnections.

How it's done:

Two 24-bit ripple counters are used, one a master, and the second, a slave. Both counters count the input frequency, but in addition, the slave counter may either be synchronized to the master counter or disconnected from the input frequency by the control logic.

Sometime before the count value is desired, both the input signal from the input gate and the synchronizing signals from the master counter are connected to the slave counter. The synchronizing signals are fed directly into the dc inputs of the slave counter flip-flops, which are represented by the 24-bit gating structure. When a carry ripple is propagating down the master counter, the slave counter is in an indeterminate state because of possible interference between the synchronizing signals and the slave internal ripple signals. When no ripple is present in the master counter, the state of the slave counter is exactly that of the master counter. The control logic disconnects the synchronizing signals from the slave counter at a time when no ripple is in the master counter (since

(continued overleaf)

the ripple in the slave counter occurs at the same time as the ripple in the master counter). The condition of no-ripple exists when the first 4 least significant bit positions of the master counter are equal to 1, indicating that 15 counts of the input frequency have occurred after the previous major carry bit has been propagated. Sufficient time has thus been allowed for all carries to have been completely propagated. At this time both counters are counting the same signal and contain the same count, but otherwise are completely independent of each other. When the instantaneous count value is desired, the input signal is disconnected from the slave counter. After any carry ripples have finished propagating in the slave counter, the individual slave counter flip-flops may be read by the computer.

Notes:

1. The counter can be readily adapted to provide frequency readouts at 0.1 second intervals.
2. Inquiries concerning this invention may be directed to:

   Technology Utilization Officer
   Jet Propulsion Laboratory
   4800 Oak Grove Drive
   Pasadena, California 91103
   Reference: B66-10658

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

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