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A STUDY OF THE JPL MARK I RANGING SUBSYSTEM

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SUMMARY

A study of the Mark 1 ranging subsystem was made at the Goddard Space Flight Center (GSFC). This report discusses the system in terms of locally generated flow charts which describe its operation. A brief discussion of the rf components and the spacecraft transponder (as they apply to the ranging system) is included to present a more comprehensive picture of the ranging operation. The report also contains a discussion of basic system considerations: translation equations, the derivation of the Chinese Numbers, and the correlation relationships.

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1.0 INTRODUCTION

The Mark 1 ranging subsystem is a special purpose version of the MOD II ranging equipment used by the Jet Propulsion Laboratory (JPL) in their Deep Space Instrumentation Facility (DSIF). This system, which is designed to measure distances unambiguously to 800,000 kilometers, will be installed in the Unified S-band sites for use in the Apollo mission.

A study of the Mark 1 ranging subsystem was made at the Goddard Space Flight Center (GSFC). As part of that study, the digital portion was duplicated to experimentally check some of the theoretical results, and to facilitate the dissemination of operating information to locally interested personnel. This document is primarily intended to describe that portion of the system. A brief discussion of the rf components and the spacecraft transponder, as they apply to the ranging system, is included to present a more comprehensive picture of the ranging operation.

The interpretive studies, the flow charts, the discussion of system operation, and the rf translation equations presented in this document were generated at GSFC. Information included to describe the system concept, the correlation relationships, and the Chinese Remainder Theorem was taken from the Reports and Research Summaries published by JPL, and standard text books.

2.0 THE MARK 1 RANGING CONCEPT

The Mark 1 ranging system uses a pseudo-random code as a ranging signal to measure distance unambiguously to more than 800,000 kilometers. The code, created by a boolean combination of four subcodes and a two bit clock signal, operates at a 1 mc bit rate to produce a pseudo-random sequence with a period of 5,456,682 microseconds.

The distance to the spacecraft is determined by measuring the phase displacement of the received code-clock combination with respect to the transmitted code-clock combination. This displacement is composed of a discrete number

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of code bits, plus a small sub-bit interval which reflects the phase difference between the transmitted and received clock signals.*

The discrete bit displacement is measured by the introduction of a duplicate code generator (called the receiver coder) which is shifted bit by bit from a coincidence with the transmitter code to a coincidence with the received code. The coincidence with the received code is determined by standard correlation techniques. The number of shifts required to achieve this code correlation is recorded in a range tally. The measurement itself takes place in the following three step process:†

Step 1. Initial Conditions

The receiver coder is driven by the transmitter clock and slaved to the transmitter coder. The transmitted carrier is phase modulated by the transmitter clock only. This signal is propagated to the spacecraft and returned to the tracking equipment to provide the received clock signal, which is coherently detected in a phase locked filter.

Step 2. Establishment of Phase Displacement

The transmitted carrier is phase modulated by the code-clock signal. This is propagated to the spacecraft and returned to provide the received code clock signal. When a range measurement is to be made, the receiver coder assumes its normal input logic, and the clock drive is transferred to that of the received clock. Since both the received code and the receiver coder are now controlled by the same clock, the bit displacement between them will remain frozen and can be measured by using time averaging or correlation techniques. The incremental phase shift introduced by shifting the clock drive will be accounted for in the doppler measurement to be described below.

Step 3. Acquisition

The receiver coder is delayed in one bit increments until it is synchronized with the received code. This condition is determined by a correlation process

*The 1 megacycle bit rate clock which drives the code generator is actually the clock signal multiplied by two. For convenience, the incremental phase shift between the received and generated codes is expressed in terms of this two bit clock.

†The components and a detailed discussion of the implementation of the processes referred to in this section will be given under their appropriate headings as they occur in the text.

in the range clock receiver in which the output of the receiver coder is added modulo two ($\oplus$) to the received code clock signal. Each one bit delay of the receiver coder is equivalent to a one bit transit time delay, and therefore to a discrete distance interval (nominally 150 meters in range).

The distance traveled by the spacecraft during the time consuming acquisition process is determined by an integration of the doppler on the received clock. Since the reference for this doppler signal is the transmitted clock, this integration process automatically includes the small shift incurred in step two of the above process. After the range to the spacecraft has been determined in this manner, it is updated by an integration of the UHF doppler for finer resolution. The UHF doppler is defined as the doppler on 1/4 of the carrier frequency.

All distance measurements reflected by the shifting of the receiver coder, and the integration of the clock and UHF doppler signals are recorded in a range tally in terms of range units. The range unit, which is the smallest increment that can be tallied, is defined as one rf doppler interval (i.e., 4 UHF doppler periods). Proper weighing is made to account for the differences in distance represented by a one bit shift of the code, and the clock and UHF doppler periods. Thus:

4 UHF doppler periods	=	1 RU
1 Clock doppler period	=	288 RU
1 Code bit shift	=	144 RU

The ranging code is composed of four subcodes which have been selected and combined in a manner that allows the overall code to be acquired serially, one subcode at a time (See Appendix F). This arrangement reduces the maximum number of shifts needed in the acquisition process from 2,728,341 to 232 (the sum of the four subcode lengths). In this method, a one bit shift of any of the subcodes is equivalent to a multibit shift of the overall code. The multibit shift that occurs for a one bit shift in any of the subcodes has been determined using the Chinese Number Theorem (See Appendix E) so that the proper number of shifts could be accounted for in the range tally. As discussed in Appendices F and G, a fully correlated subcode does not give a full correlation indication, due to the method chosen for code combination. The uncorrelated and correlated indications obtained during the acquisition process are given in Appendix G. The serial acquisition process requires one reset and seven distinct acquisition steps called program states. These steps are given below:

State	Operation Performed
Reset	Transmit transmitter clock only, and lock up the range clock receiver. Transmit code-clock combination.
1.	Connect the input of the code clock transfer loop to the transmitter coder clock. (The output of the loop drives the receiver coder.)
2.	Synchronize the transmitter and receiver coders. Reset the range tally to zero. Connect the code clock transfer loop to the received clock. Start the integration of the clock doppler signal.
3.	Send the $\overline{X}$ A portion of the receiver coder to the range clock receiver. Shift the X code only and acquire the X subcode components.
4.	Send the $\overline{X}$ A portion of the receiver coder to the range clock receiver. Shift the A code only and acquire the A subcode components.
5.	Send the $\overline{X}$ B portion of the receiver coder to the range clock receiver. Shift the B code only and acquire the B subcode components.
6.	Send the $\overline{X}$ C portion of the receiver coder to the range clock receiver. Shift the C code only and acquire the C subcode components.
7.	Send the total receiver coder output to the range clock receiver. Enable the range readout of the tally, and switch the doppler integration from the clock doppler to the UHF doppler for tallying.

3.0 THE RANGING SYSTEM

The ranging portion of the Unified S band equipment determines the position of the spacecraft with respect to the tracking station. Distance is determined by the Mark I ranging subsystem. The range rate (or radial velocity) is derived from a measurement of the two way doppler on 1/4 of the carrier frequency by the doppler extractor. The spacecraft angular position is determined by the antenna angular reading.

The simplified block diagram given in Figure 1 shows that this portion is made up of a transmitter, a spacecraft transponder, a ground receiver, a doppler extractor and the Mark 1 ranging subsystem. The ranging signal, which is produced by the ranging subsystem is modulated on the transmitted carrier, and propagated to the spacecraft. The spacecraft transponder demodulates the signal to baseband, and remodulates it on the down link carrier frequency. The received ranging signal is demodulated from the received carrier by the ground receiver, and passed into the ranging subsystem to determine the distance. The ground receiver also provides an output signal which is phase coherent to that of the received carrier. This signal along with a sample of the signal being transmitted is fed into the doppler extractor which provides the range rate, or doppler information.

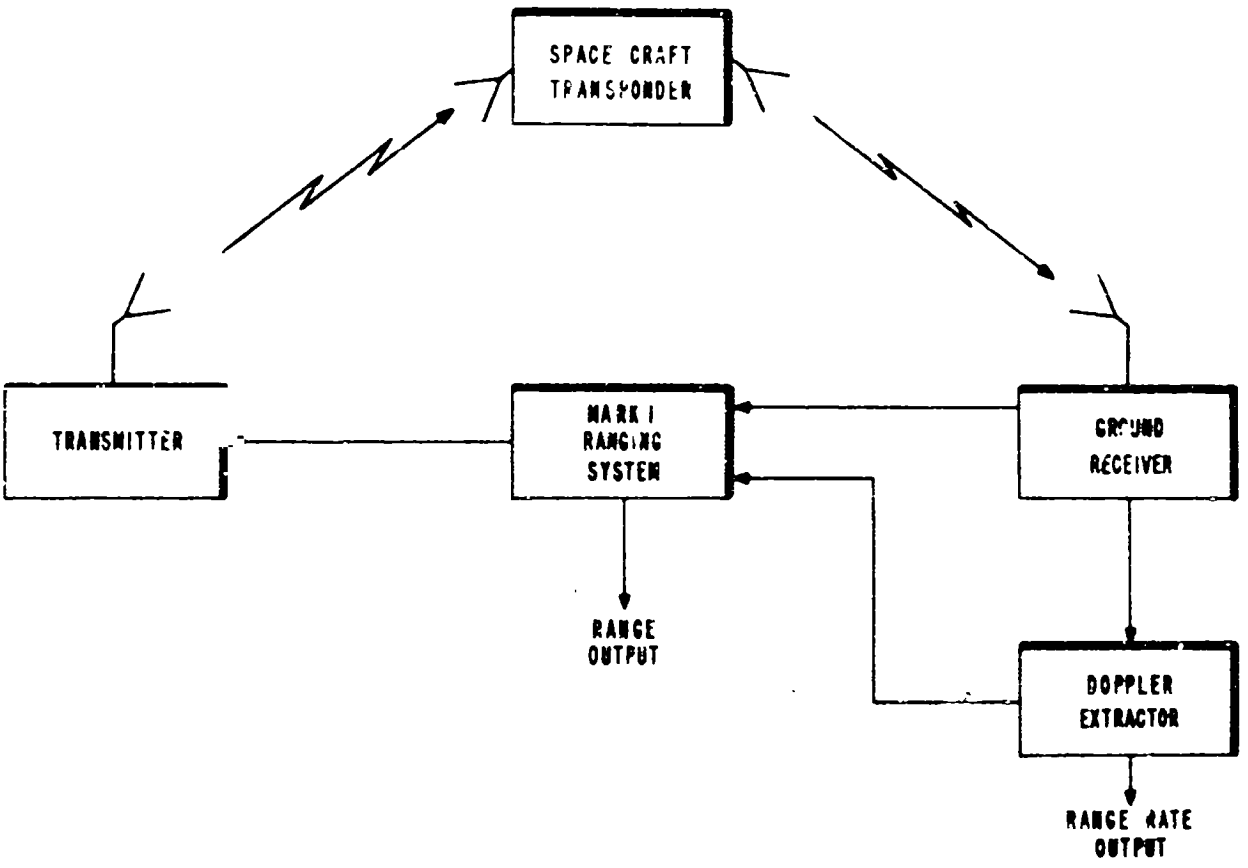

Figure 1. Block Diagram of Apollo Ranging Subsystem

It should be noted that the transmitter, the transponder and the ground receiver are also used by the non-ranging portions of the Unified S-band system. The angle measuring equipment is not shown.

3.1 The Transmitter

The transmitter is composed of an ultra-stable frequency source, a modulator, an exciter, and a power amplifier. Since this unit does not make any contribution to the ranging operation, a detailed description of its operation is not needed, nor included.

3.2 The Spacecraft Transponder

A simplified block diagram of the portion of the transponder which is utilized in the ranging process is shown in Figure 2. The rf signal which enters the transponder through a preselector is fed into a mixer preamplifier combination which translates the rf carrier to IF frequencies of 47 and 9.5 mc. The mixing frequencies used in this process are derived by multiplying the output of the carrier locked VCO by 108 and by 2 as needed. The output is passed through the 9.5 mc IF amplifier to the modulation phase detector, where it is mixed with the output of the same carrier tracking VCO divided by two. The output of this detector, which contains the ranging signal, is passed through a wideband filter and phase modulated on a signal obtained by multiplying the carrier locked VCO output by four. The output of the phase modulator is then multiplied in frequency by 30 for retransmission to the tracking station. The 9.5 mc output of the mixer preamplifier combination is also passed through a narrow band filter to provide the input signal to the phase locked loop which controls the VCO frequency.

Since wide band filtering must be employed to preserve the ranging signal, the up data or up voice subcarriers which may be phase modulated on the received rf signal will be retransmitted along with the ranging signal. The relationships that result from the spacecraft and ground frequency mixing and translation processes are given in Appendix B.

3.3 The Ground Receiver

The ground receiver coherently recovers the received ranging signal for the Mark 1 subsystem; and provides a signal which is phase coherent with the received carrier for the doppler extractor. A block diagram of the unit is given in Figure 3.

The received S band signal, taken from the output of the parameteric amplifier, is fed to the first mixer and mixed with a signal derived from the carrier tracking loop VCO multiplied by 96. The output of this mixer (at a center frequency of 50 mc) is passed through a 50 mc IF amplifier and then mixed with 60 mc (derived by tripling the output of a 20 mc reference oscillator) to produce a 10 mc output signal. The output of this mixer is then passed through two 10 mc

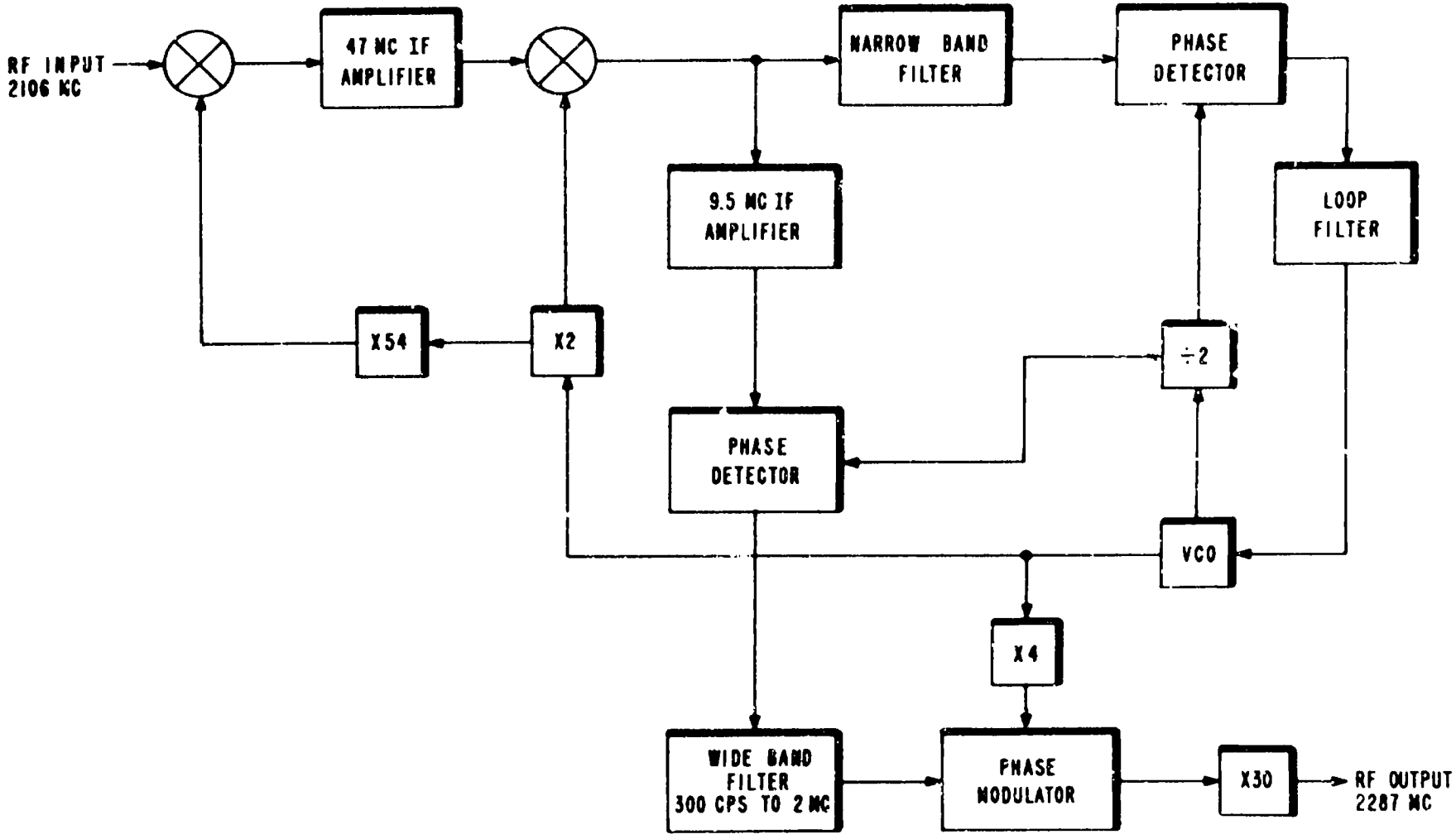

Figure 2. Block Diagram of Ranging Portion of Spacecraft Transponder

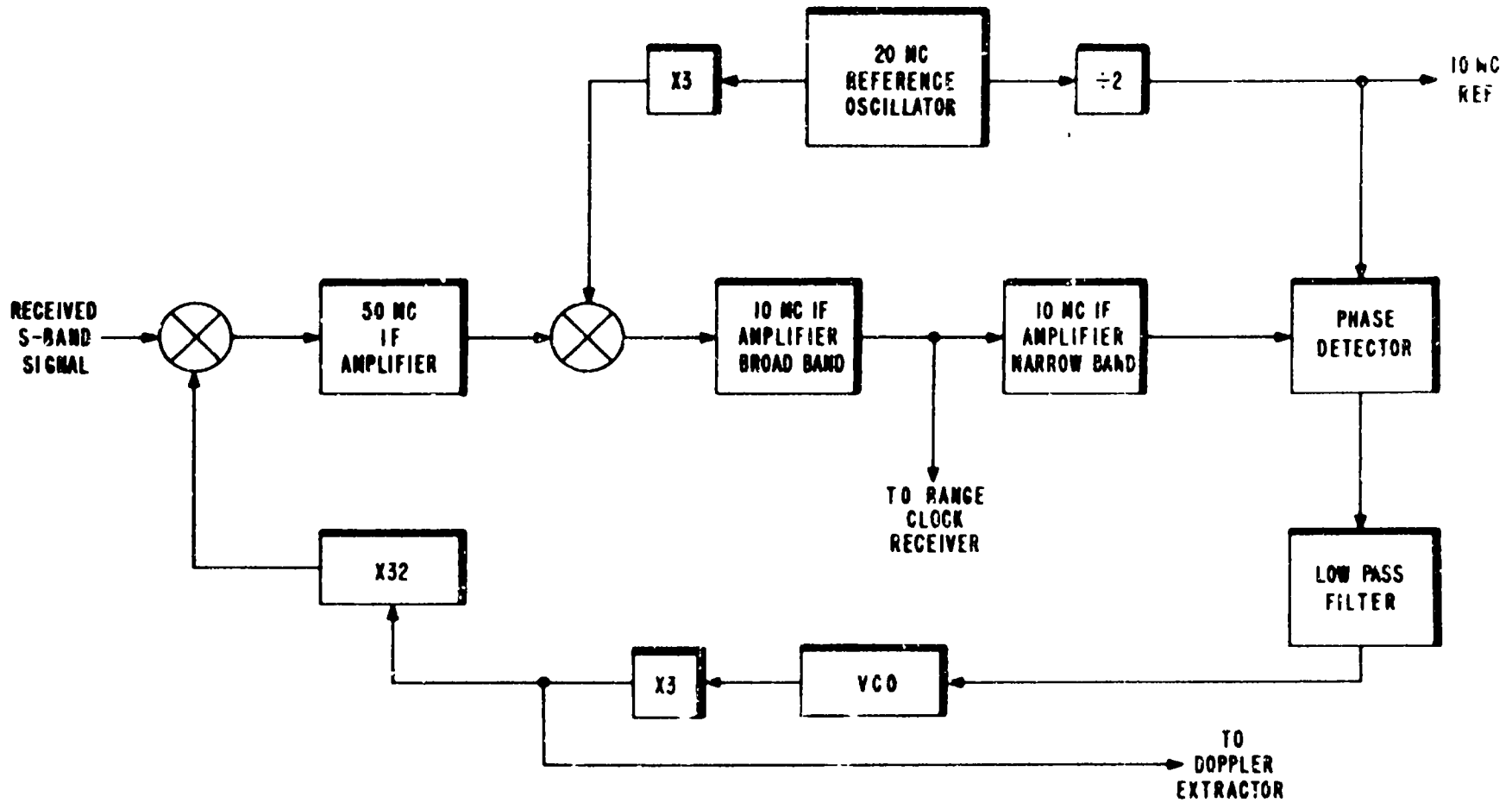

Figure 3. Block Diagram of Ground Receiver

IF amplifiers in series. The output of the first (or broad band) amplifier contains the received ranging signal which is fed to the range clock receiver. The output of the second (or narrow band) amplifier is fed into a phase detector where, by comparing it with a 10 mc signal (derived from the same 20 mc reference oscillator) an output is obtained which is used to control the frequency and phase of the carrier loop VCO. Once the carrier loop is locked. the output of the VCO (when multiplied by three) provides the received S band carrier signal which is fed to the doppler extractor. As shown in Appendix B, any drift in the reference frequency oscillator does not effect the doppler signal.

3.4 The Doppler Extractor

The doppler extractor compares the frequency of the received carrier with that of the transmitted frequency, to derive the two way doppler on the carrier. This signal, superimposed on a 1 mc bias signal, provides the range rate output of the system. The bias frequency both eliminates the ambiguity caused by the doppler transition through zero frequency, and alleviates the problems of handling very low doppler frequencies. One fourth of the two way carrier doppler is also derived and passed through quadrature phase detectors to provide the UHF doppler signal required by the Mark 1 ranging subsystem. A block diagram of the extractor is given in Figure 4. A discussion of the mixing and multiplication operation is given in Appendix B.

3.5 The Mark 1 Ranging Subsystem

The subsystem is composed of a transmitter coder, a receiver coder, a code clock transfer loop, a clock doppler extractor, an automatic acquisition and programming unit, a range tally and a readout register. Its operation can be followed with the aid of the block diagram given in Figure 5. The transmitter coder produces the ranging signal which phase modulates the transmitted carrier. This signal is propagated to the spacecraft and back to the ground receiver, which demodulates the ranging signal from the receiver carrier. The ranging signal is fed to the range clock receiver, where it is mixed with the output of the receiver coder (controlled by the automatic Acquisition and Programming Unit) to recover the clock signal. The amplitude of the recovered clock signal reflects the degree of alignment between the received ranging signal and the receiver coder, and is used as the correlation indication for the acquisition circuitry. A local representation of the clock signal is taken from the VCO of the range clock receiver and fed to the code clock transfer loop*.

*During the synchronization process, the input to the code clock transfer loop is taken from the transmitted clock signal.

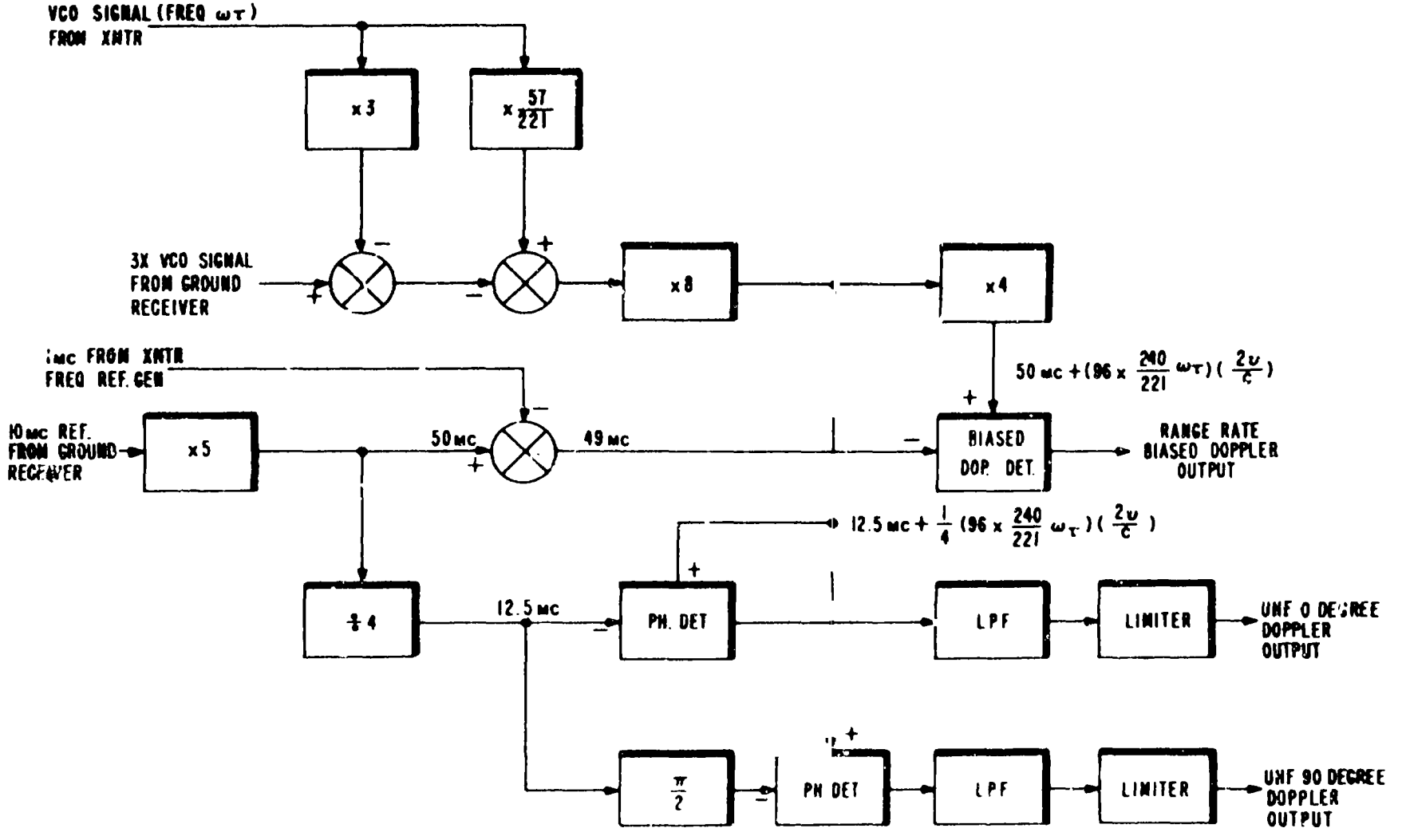

Figure 4. Block Diagram of the Doppler Extractor

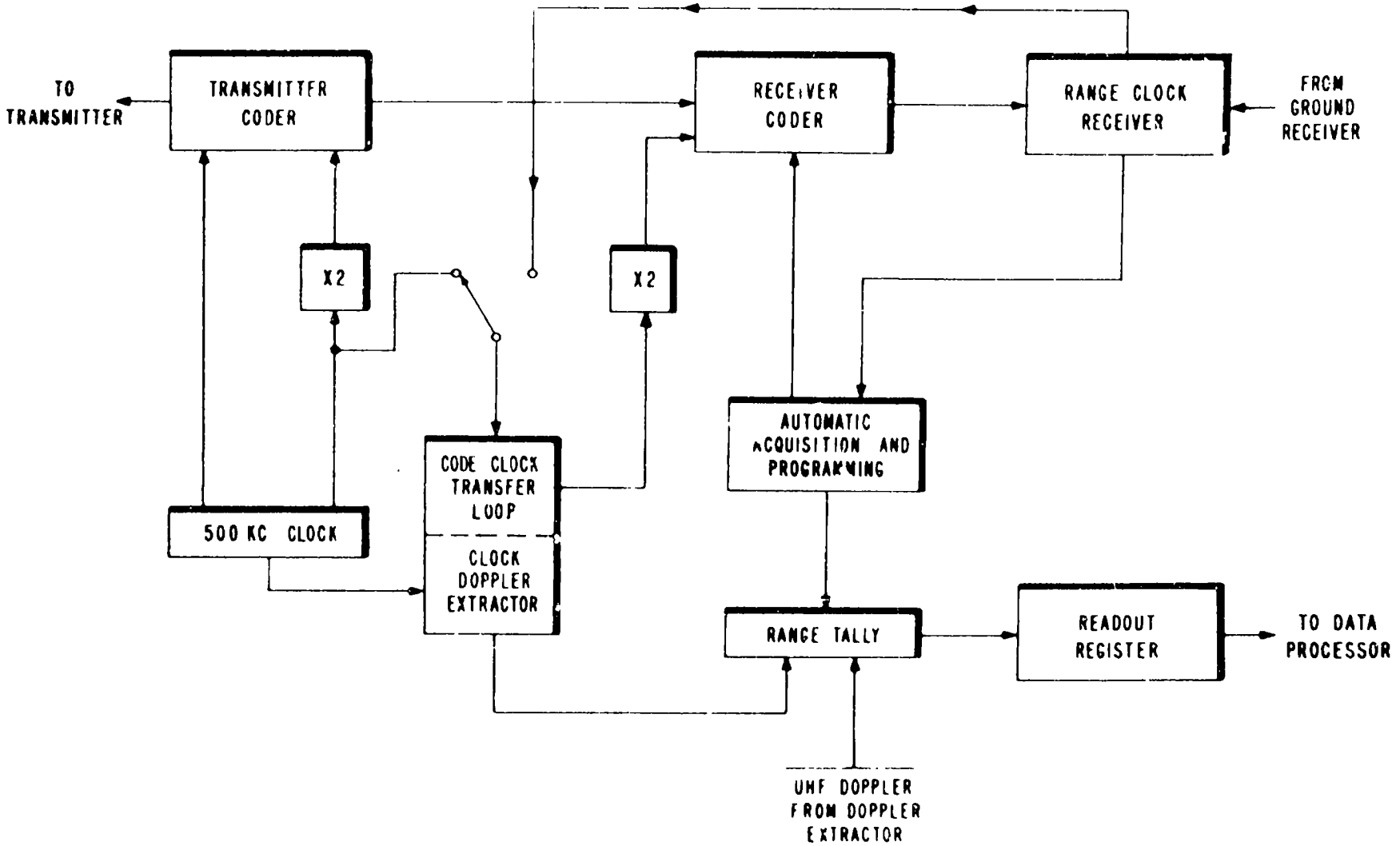

Figure 5. Block Diagram of Mark 1 Ranging System

The clock drive to the receiver coder is obtained by doubling the frequency output of the code clock transfer loop. The output of the code clock transfer loop is also phase compared with the transmitted clock to obtain the clock doppler signal. The range equivalent of the delay that must be inserted into the receiver coder by the acquisition circuitry as well as each cycle of clock (and later UHF) doppler are recorded in the range tally to indicate the range to the spacecraft. The resultant range measurement is fed into the readout register for sampling by the data processor.

3.5.1 The Range Clock Receiver—The range clock receiver is designed to extract the clock from the received ranging signal, and to furnish a correlation voltage which is a function of the alignment between the received code (Steps 3, 4, 5 and 6) and the subcode being acquired. The block diagram given in Figure 6, shows that it is composed of three basic parts, namely a balanced detector, a received clock phase locked loop, and a coherent amplitude detector.

The balanced detector is basically a comparison circuit in which the received code clock combination is compared with the local subcode being acquired to recover a representative clock signal. For better resolution, these signals are phase modulated on a 10 mc carrier. The balanced detector is designed to provide a full clock output only when the individual bits of the two codes are in phase. Therefore, the amplitude of the clock component exhibits an abrupt increase when the code is synchronized. The output of the detector is passed through a narrow band amplifier and used to control the frequency and phase of the received clock phase locked loop. The amplitude of the clock component is detected in a coherent amplitude detector, to provide an indication of correlation, or match, between the received and locally generated codes. The output of the VCO is also fed to the code clock transfer loop as a locally generated received clock signal.

3.5.2 The Code Clock Transfer Loop—The code clock transfer loop is locked to either the transmitted clock or the output of the range clock receiver loop VCO (or received clock) depending on the program state of the system. There are two outputs. One which is passed through a frequency doubler and used to drive the receiver coder, and one which provides the quadrature clock doppler signals (i.e. clock doppler 0 degree and clock doppler 90 degree) to the range tally.

4.0 DIGITAL PORTION OF THE RANGING SYSTEM

The digital portion of the ranging subsystem contains the logic circuitry by which the distance to the spacecraft is determined, updated and fed into the data

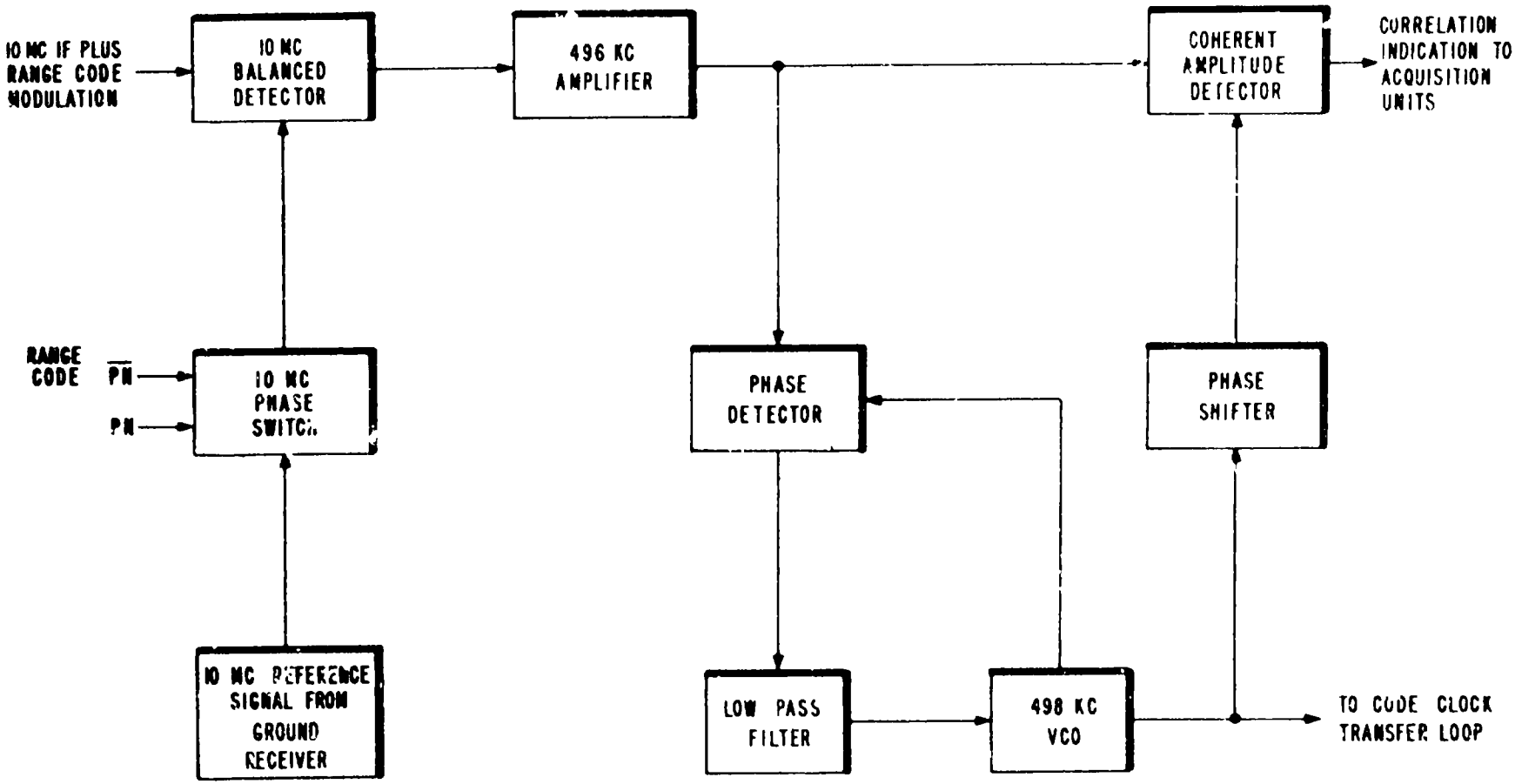

Figure 6. Block Diagram of the Range Clock Receiver

processing equipment. It consists of a Transmitter Coder, a Receiver Coder, a Timer, a Program Unit, an Automatic Acquisition Unit, a Number Generator, a Range Tally and a Readout Register. It is fed by the output of the range clock receiver, which supplies the correlation indication; the clock doppler extractor, which supplies the clock doppler signal; and the doppler extractor which supplies the UHF doppler signal. The system can operate in either an automatic or a manual mode. All test signals required to check the operation of the system are generated internally.

Drawing No. 1* shows the interrelationships and the signals that flow among the various units of the system. A pictorial presentation showing the equivalent logic for each of the individual units is given in Drawings 2 through 10 inclusive. An explanation of the conventions used in compiling these logic diagrams is given in Appendix A. A detailed discussion of the actual design and implementation of these units is presented in the succeeding sections of this document.

There are several places where signals are shown which seem to have no useful purpose. Since this is still an evolving system, this situation is not unexpected. These signals have not been deleted from the diagrams since they are still contained in the actual system.

4.1 Transmitter Coder

The transmitter coder produces the pseudo random ranging code which is phase modulated on the transmitted carrier. It is composed of four subcodes (a, b, c, and x) and a two bit clock signal. These are combined in a boolean manner to produce the $\overline{x}\ (a\cdot b + b\cdot c + a\cdot c) \oplus cl$† function which can be acquired serially during the acquisition process. The "a", "b" and "c" subcodes are $2^n - 1$ bits long and are generated in maximum length shift registers; the "x" subcode is 11 bits long and is generated by a direct logic Legendre sequence. The coder can produce either of two code lengths by changing the length of the "b" and "c" subcodes. The normal code length is used for measuring lunar distances. The short code (or normal code‡) is used for measuring short orbital distances, or for exercising the system. The following chart shows the composition of the two codes.

*For the convenience of the reader, all drawings are presented at the end of the appendices.

†This is actually produced as $x\cdot cl + \overline{x}\ [(a\cdot b + b\cdot c + a\cdot c) \oplus cl]$ which is equivalent.

‡Whenever a definite selection between two output conditions must be made, the preferred output is called by name, and the alternate is designated as the preferred output (read as preferred output bar).

Designation	Length	"a" subcode	"b" subcode	"c" subcode	"x" subcode
Normal Code	5,456,682	31	63	127	11
Short Code	71,610	31	7	15	11

The use of a dynamic logic system allows a shift register to be replaced by a generating function and a tapped delay line which feeds the proper signals back to the generating function. The generating logic is a function of the number of stages in the register. The "a" subcode uses $af_1 \oplus af_3$; the "b" subcode uses $bf_3 \oplus bf_4$ for the normal code and $bf \oplus bf_1$ for the short code; while the "c" subcode uses $cf_4 \oplus cf_5$ for the normal code and $cf \oplus cf_2$ for the short code. The "x" subcode, which is a Legendre sequence, is produced by the $\overline{xg} \cdot \overline{xf}_2 + \overline{xf} \cdot \overline{xf}_3 + \overline{xf}_1 \cdot xf_2 \cdot xf_3$ generating function.

If all n stages of a maximum length shift register happen to be in the zero state, when the generator is initially energized, the code can not be generated. When this occurs, an all zero detector inserts a 1 into the delay line to initiate the sequence. This zero set stage is not required by the "x" subcode.

The all 1's condition (i.e. all n stages of the code are in the logical 1 state) is used to define an unique point in the overall code and in each of the subcodes. It has many applications in the system. The output of the "a" subcode all 1's detector provides the 31 microsecond base for the minor and major machine cycles which run the system. The time delay between the occurrence of the all 1's position of the transmitter and receiver coders provides an unofficial station readout of spacecraft distance once acquisition has occurred. In addition, the all 1's position is the only point in the sequence where a one bit shift of the subcodes is possible. The all 1's position is detected at an earlier position in the sequence to allow for the processing delays that must occur between recognition and use in a clocked system.

A flow diagram of the transmitter coder is given in Drawing No. 5. It shows the generating logic, the tapped delay line, the zero start mechanism, the all 1's detector and the code length selector for the various subcodes as they apply. The diagram also shows the logic circuitry by which the subcodes are combined to produce the final forms of the transmitter coder output. This consists of the majority function combiner, the code combiner, the clock synchronizer, the cl $\oplus$ code circuit, the squaring amplifier, and the controls required to permit either the clock or cl $\oplus$ code to reach the transmitter modulator. A code only signal which has a 34 microsecond delay time (relative to the actual generating time) is also produced. This signal is $\oplus$ with the output of the receiver coder to produce a pseudo-correlation test signal for the acquisition unit.

4.2 The Receiver Coder

The receiver coder produces the code sequence which is used in the acquisition of the received code. Except for the following additions imposed by the acquisition process, the receiver coder and the transmitter coder are duplicate units:

1. The output of the receiver coder must present a different subcode combination (without the clock) for each program state during the acquisition process.

2. The receiver coder must be synchronized to the transmitter coder at the start of the acquisition process to provide a zero set condition.

3. The receiver coder must have the circuitry required to shift its code position one bit at a time (either right or left).

The circuitry required for conditions 1 and 2 is provided by the addition of a few simple "and" gates. The code shifting signal (Condition 3) can be generated either manually or automatically, and is tied to that portion of the system using the transmitter clock.* This signal must be converted to a single pulse synchronized to the receiver coder clock before it can be used. As will be shown later, this in turn must then be introduced at the only spot in the code sequence where it is possible to make the desired one bit shift without disrupting the rest of the sequence. The generation of the right shifting pulse from a manual right shift signal is shown in Figure 7. The left shifting pulse is generated in the same manner, when initiated by the manual left shift signal. As can be seen, the use of two flip flops and the AW timing pulses creates a situation whereby only one shift pulse, synchronized to the receiver clock is generated for every manual shift signal generated, regardless of its duration. The circuitry used to generate the code shifting pulse from the automatic shift signal is shown in Figure 8. Again two flip flops and the AW timing pulses are used to convert this signal to a single shift pulse, synchronized to the receiver clock.

The B code has been chosen to illustrate the integration of the shifting mechanism into subcode generator. A flow diagram is given in Figure 9. It consists of the same type of generating logic, zero start mechanism, delay line, all 1's detector and code length selector as in the transmitter code generator. However there are also the synchronization mechanism and shift right and left circuits

*The basic 996 KC clock driving the T pac units is derived by doubling the frequency of the transmitter clock, and is common to all T pac units except the receiver coders which are driven by twice the received clock frequency.

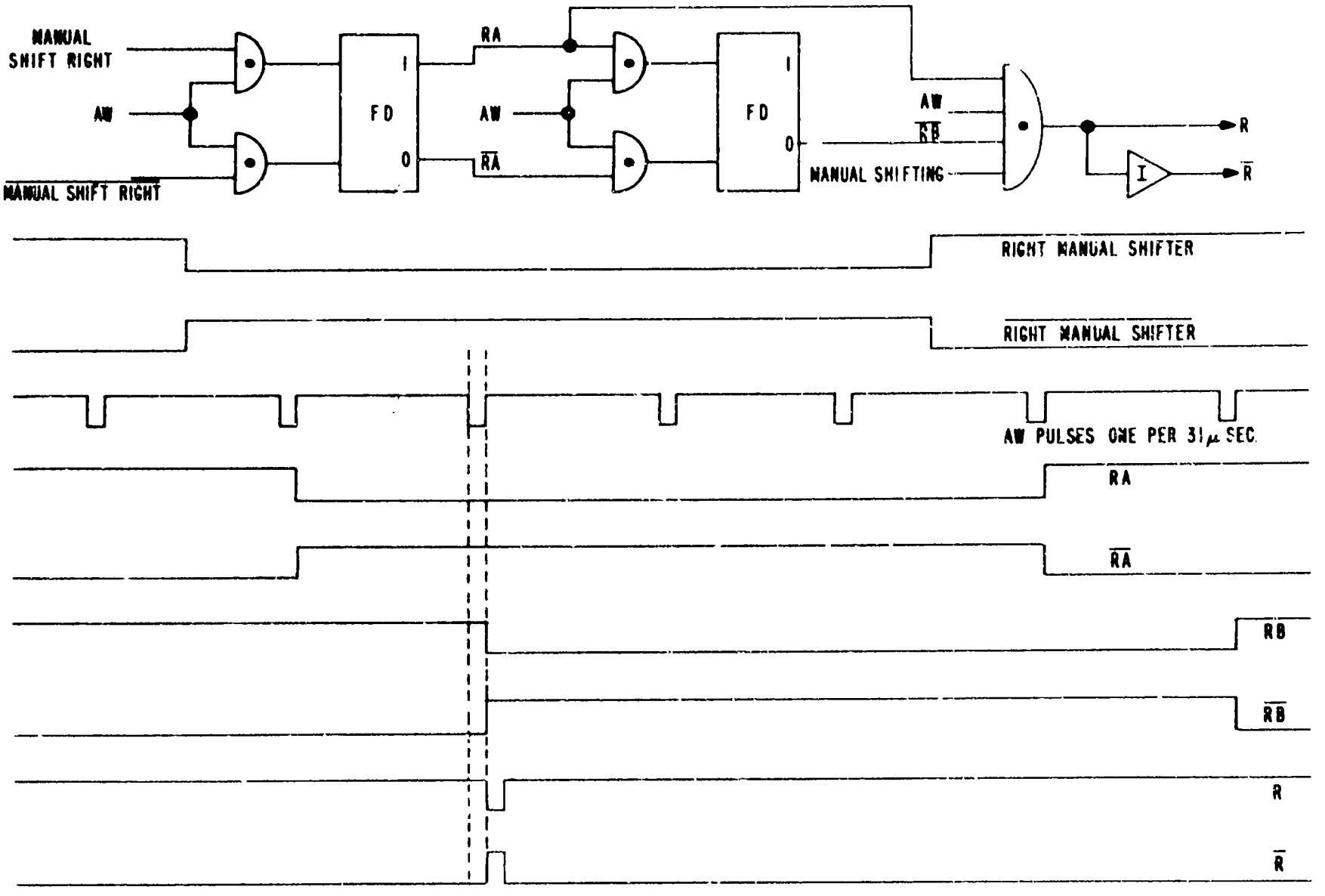

Figure 7. Flow Diagram Showing Generation of Right Shift Pulse from Manual Shift Signal

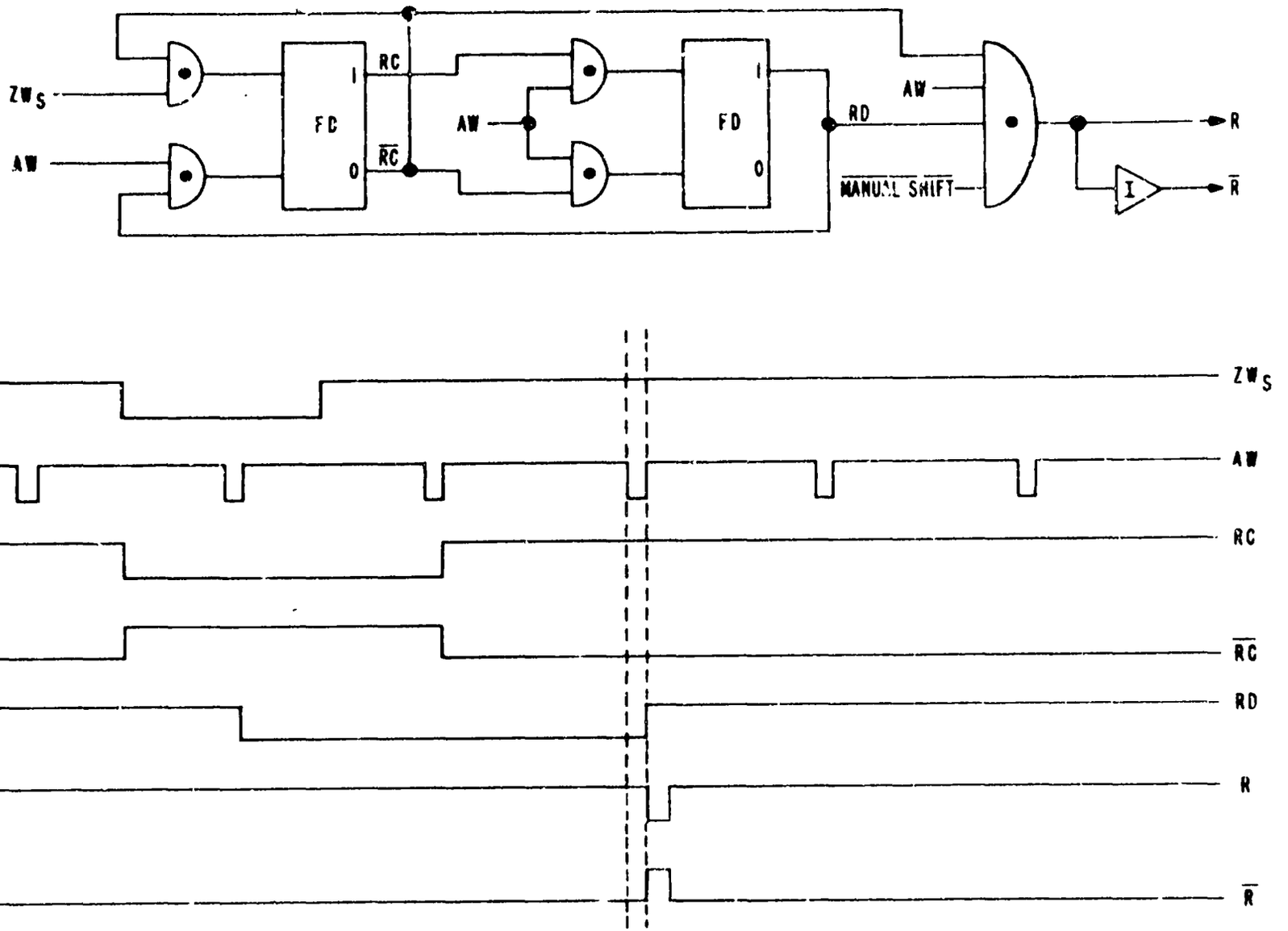

Figure 8. Flow Diagram Showing Generation of Right Shift Pulse from Automatic Code Shift Pulse

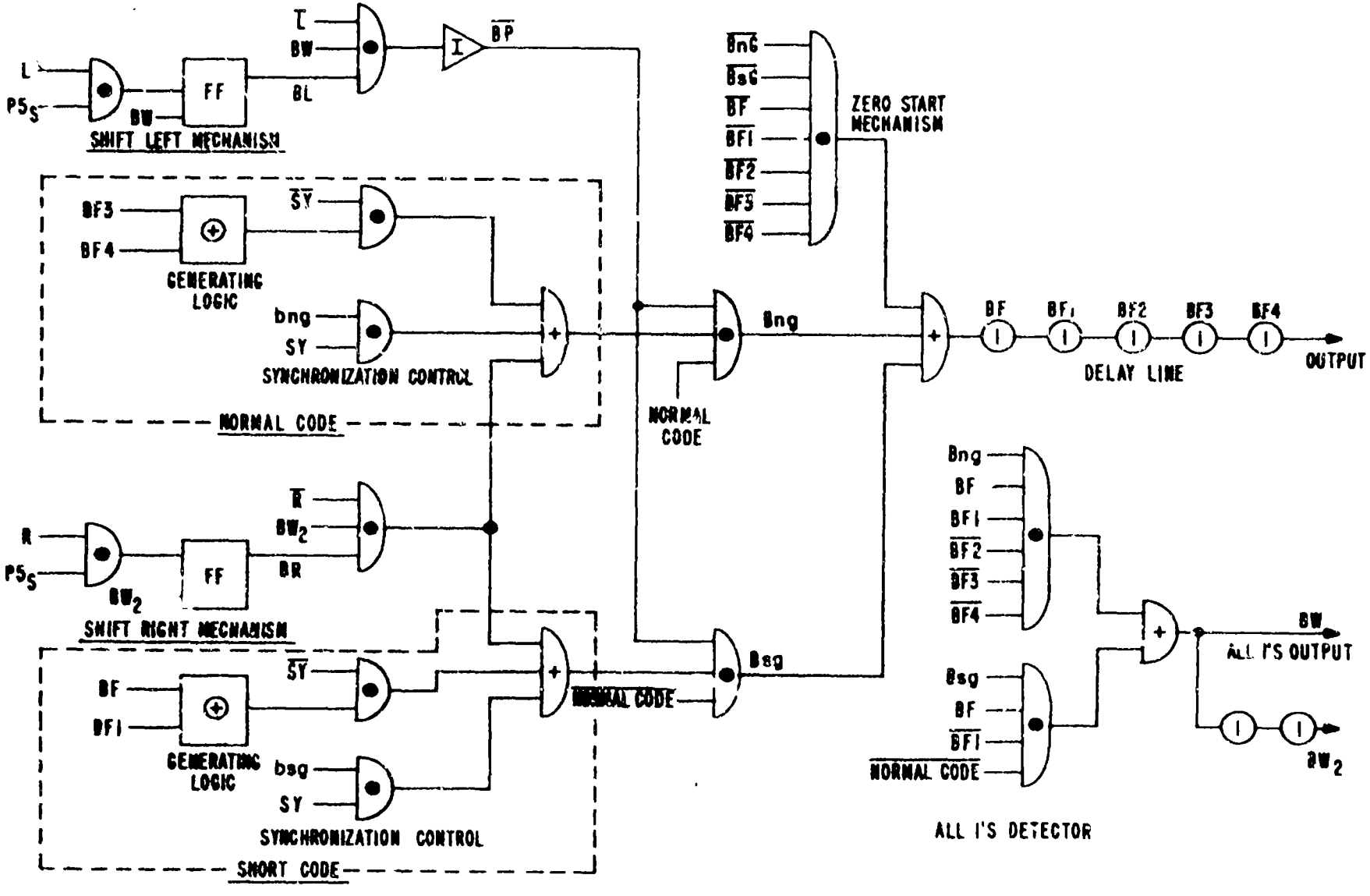

Figure 9. Flow Diagram of B Subcode Generator of Receiver Coder

required by the receiver coder only. The code synchronization mechanism consists of two "and" gates which control the logic input to the delay lines and thereby the code sequences. The timing of the shifting circuitry can be seen by the use of table 1, in which the normal as well as the right and left shifted B code sequences are illustrated. Notice that a single right shift can be obtained by repeating the all 1's word which in effect lengthens the code sequence by one bit. A single left shift can be obtained by deleting the all 1's word, which in effect shortens the code by one bit. The all 1's word is unique in that its repetition or deletion does not effect the rest of the sequence. The all 1's is repeated by inserting a 1 into the delay line instead of the 0 normally generated by the logic during the BW_2 state. This is done by the shift right flip flop and the control gate. The flip flop is set by any shift right pulse (R) which occurs during state P 5, allowing the first BW_2 pulse to pass through the control gate, putting a 1 into the delay line. The BW_2 pulse simultaneously resets the flip flop making the control gate inoperative 1 microsecond later so that only one pulse per shift is passed by the control gate. The all 1's is deleted by introducing a 0 into the delay line instead of the 1 normally generated as the output of the BW state. This is done by the shift left flip flop and a control gate. The flip flop is set by any shift left pulse (L) which occurs during state P5, and allows the first BW pulse to inhibit the input to the delay line for one microsecond, thus inserting a zero. The BW pulse simultaneously resets the flip flop making the control gate inoperative one microsecond later, so that only one BW pulse per shift is passed by the control gate.

The receiver X subcode is similar to that of the transmitter x subcode with the above mentioned modifications. Since it is a direct logic generated Legendre sequence however, the shifting mechanism actually generates a new sequence with each code shift. It requires two bits after a right shift and four bits after a left shift to revert back to the original code sequence with the proper shifts inserted. This sequence is also shown in Table 1, and in Figure 10.

A complete flow diagram of the circuitry used by the receiver coder is given in Drawings 6 and 7.

4.3 Timer

The timer is made up of a 31 microsecond, 31 tap, open ended shift register. The starting pulse comes from the word detector (aw) of the 31 bit "a" subcode of the transmitter coder. The individual tap outputs, referred to as timing pulses, are designated as t0, t1, t2, t3, ... t30. They provide all the timing required by the system, and are the time base for the generation of all numbers used throughout the system. The unit also defines a 31 microsecond minor machine cycle. Four of these minor machine cycles, designated as tA, tB, tC, and tD are

Table 1
Code Sequence As Effected By Shifting

B SHORT CODE SEQUENCE

LEFT SHIFT	NO SHIFT	RIGHT SHIFT	TIMING SEQUENCE
111	111	111	
011	011	011	
001	001	001	
100	100	100	
010	010	010	BW detected
101	101	101	BW
110	110	110	BW_1
011S	111	111	BW_2
001	011	111S	
100	001	011	
010	100	001	
101	010	100	
110	101	010	
111	110	101	
011	111	110	

X CODE SEQUENCE

LEFT SHIFT	NO SHIFT	RIGHT SHIFT	TIMING SEQUENCE
10110	10110	10110	
11011	11011	11011	XW detected
11101	11101	11101	XW
01110	01110	11110S	XW_1
00111	00111	01111	XW_2
00011	00011	00111	XW_3
00001S	10001	00011	
10000	01000	10001	
11000	10100	01000	
01100	11010	10100	
10110	01101	11010	
	10110	01101	

S indicates Shift point (first different word)

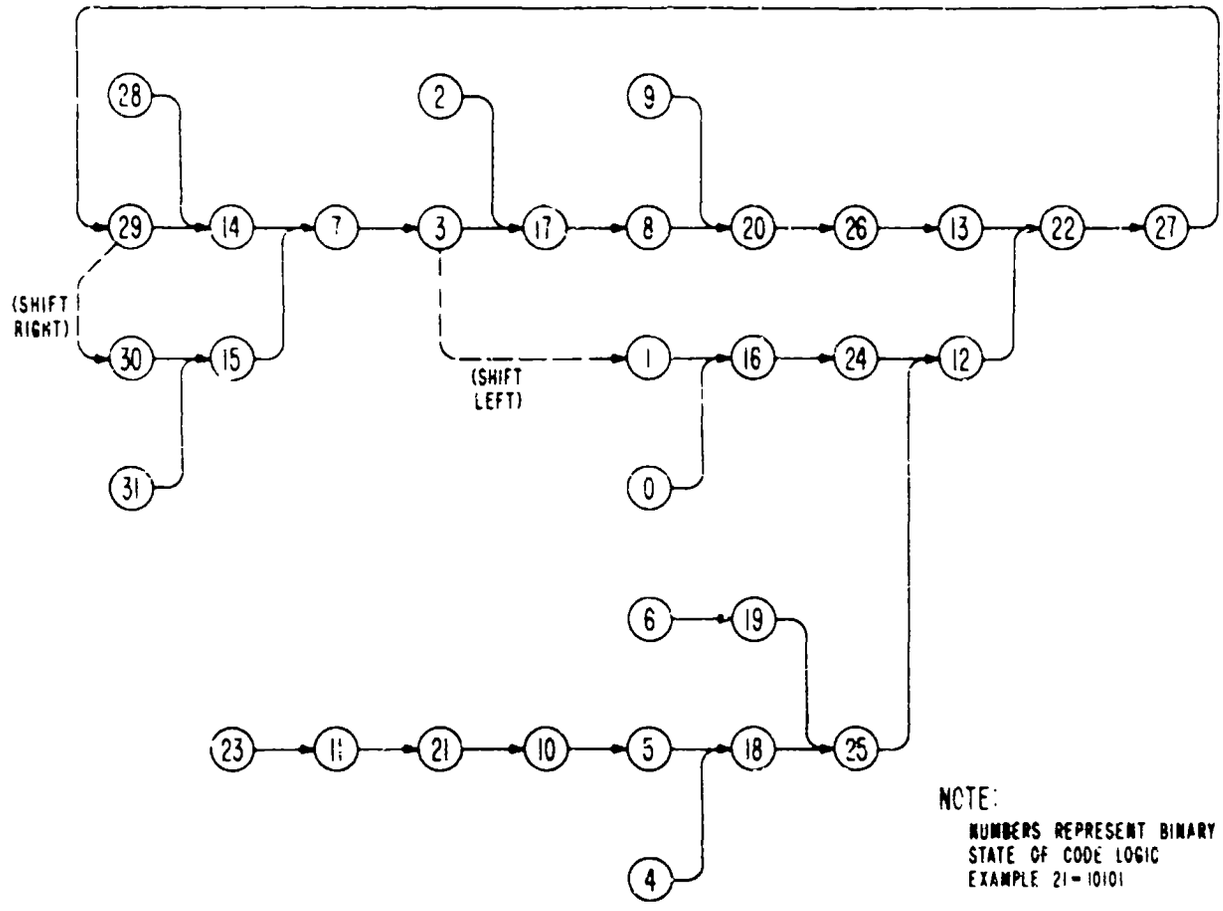

Figure 10. Receiver and Transmitter Subcode X (11 Bits Long) State Diagram

generated sequentially by the t29 pulse (because of a two microsecond processing delay) in a ring counter to form the 124 microsecond major machine cycle. The ring counter is physically located in the program unit mo..

A flow diagram of this unit is included as part of Drawing No. 10.

4.4 The Program Unit

The Program unit controls the sequential acquisition of the ranging subsystem. It is a permanently wired unit, which can be operated manually or automatically, and is designed to meet the needs of the Apollo mission. It is divided into a non-reset and seven program states. A complete flow diagram of the circuitry which compose this unit is given in Drawing No. 2. The wave forms of the signals generated by the program unit are given in Drawings 11 and 12.

The initial control of the unit rests with two push buttons (reset and start) located on the control panel. In the automatic mode, the start button must be depressed to step the system from the reset state to P1. From there the system

goes through the other states automatically. Control of the system is passed back and forth between the program urit and the acquisition unit, as each performs its required sequential function. The program unit determines the particular acquisition routine to be performed and passes control to the acquisition unit by initiating the proper acquire command signal. The acquisition unit accomp'ishes the designated subroutine and returns control to the program unit by generating the proper component acquired signal. The program unit, which reaccepts control, steps the system to the next state. The process is repeated until state P7 designating the completion of the acquisition process is reached. In the manual mode, the system is stepped from one program state to the next by means of the start push button.

The system automatically reverts to the non-reset state whenever the receiver in lock (RL) signal is not maintained. The maintenance of the receiver in lock (RL) signal is dependent on the presence of three externally supplied signals, and one internal signal. The external signals require that the receiver be operational, and that both the selected S band receiver and the clock loop are in lock. The internal or reset command bar ($\overline{RP}$) signal provides the manual reset control of the system. The reset button, when depressed, removes the reset command bar ($\overline{RC}$) signal for one microsecond, to reset the system.

The step pulse (T) when accompanied by the proper acquire signal from the acquisition unit, steps the system from one program state to the next. It is generated at t30 of the tA minor machine cycle. In the automatic mode, it is generated once every major machine cycle, whenever the system is not in the non-reset state. In the manual mode, or in the non-reset state, it can only be initiated by the start button. The start button when depressed, produces the start Command (SC) signal which generates a train of start gate (S) pulses. The last of these pulses occurring at t29 of the tA minor machine cycle fulfills the required input logic to generate the step pulse (T).

Entrance into each program state is controlled by means of a flip flop which is set by the required input logic for that state. The system is kept in each program state until the flip flop is reset by either the initiation of the next program state, or the automatic reset of the system (by the loss of the receiver in lock (RL) signal). Except for the non-reset state, the individual input logics have most signals in common. They each require a step pulse (T), and a positive indication that the system is in the previous state. States 2 through 7 inclusive require a return signal from the acquisition unit. In states 2 and 3, this takes the form of a count finished (UK) signal; in states 4 through 7 inclusive, it is in the form of a component acquired (ZQ) signal. States 2 and 3 are the only ones that require an additional signal. State 2 requires an indication that the transfer loop has been locked to the transmitter clock, while state 3 requires an indication that it is again locked to the receiver clock.

The output of the program state flipflops are in the form of a train of pulses synchronized to the transmitter clock. As such, they cannot be used with the logic inputs to the receiver subcode selection circuits (which are synchronized to the received clock), nor for applications such as controlling the program state indication lights which require a static type signal. An FD 10 flip flop is used to convert these dynamic to static indications.

There are six acquire signals, generated at definite times in the machine cycle or the programming process, that are required in the automatic acquisition process. The first of these is the Start delay (SD) signal. It is used by the acquisition unit during the transition from states 1 to 3 inclusive to provide a sufficient time delay for all the synchronization processes to have occurred. It is generated by a flip flop which is set by the transition into states 1 or 2 and reset 31 microseconds thereafter. The second signal is the synchronization signal (SY). Its main function is to command the synchronization of the receiver coder to the transmitter coder during the P2 program state. It is generated by a static flip flop which is set by the transition into state 2, and reset by the first pulse in the next tC minor machine cycle. The third signal, which is generated in the same process is the operate switch loop (SL) signal. It guarantees that the receiver coder is driven by the received clock, except for the brief interval, when being synchronized to the transmitter coder, it is driven by the transmitter clock. The FD 10 flip flop which generates the switch loop (SL) signal is originally set when the system leaves the nonreset state. It is then reset by the start of the P1 program state and set again at the termination of the code synchronization interval during state P2. Note that sufficient time is allowed for the loop to be phase locked to the transmitter clock before the code synchronization takes place, and that sufficient time is allowed for the loop to be again phase locked to the received clock before the start of the correlation process starting at P3. The fourth signal is the four microsecond convert command (C) which is generated once every major machine cycle. It gates the voltage digitizer to sample and digitize the current correlation voltage as needed by the acquisition process. This signal is generated by an FD 10 type flip flop which is set at t0 and reset at t4 of every tD minor machine cycle. The fifth and sixth signals which are generated during program states 3, 4, 5 and 6 are the acquire gate (A) signal which triggers the acquisition of the subcodes, and the shift time (ST) signal which allows the subcodes to be shifted only at the start of the tB minor machine cycle. The acquire command (AC) signal which is initiated at the start of each program state, triggers the acquire gate flip flop (A) giving a 31 microsecond train of pulses. The shift time (ST) signal is generated by a simple series of gates as shown.

4.5 The Acquisition Unit

This unit programs the internal routines required for passage from one acquisition state to the next. During states 1 and 2, this involves the generation of

a sufficient time delay to insure that the transients created by shifting the code clock transfer loop have settled out of the system. In states 3, 4, 5, and 6 this entails the generation of all shifting and detection signals required for the complete acquisition of the received code by the receiver coder. The acquisition is done one subcode at a time as determined by the program state. Each subcode is shifted one bit at a time until the correlation level at all shift positions has been examined. The subcode is then returned to the position with the highest correlation indication to complete the subcode acquisition. The range, which is determined by the number of shifts, is accumulated in the range tally.

For descriptive purposes, the acquisition unit can be divided into five basic sections. They are the correlation level detector which measures the correlation value; a high correlation level storage which stores the highest correlation value received; a shift position counter which counts the number of times the subcode has been shifted; a high correlation level shift position storage which records the shift position with the highest correlation value; and a code shift generator which generates the shift pulses required to shift the code after each correlation interval is over.

A flow diagram showing the logic circuitry which controls the acquisition process, and the generation of the signals that are required is given in Drawings 3 and 4. The waveforms of these signals showing their timing effects on the operation of the system is given in Drawings 13 and 14. A detailed discussion of the component parts of the acquisition unit is given in the following sections.

4.5.1 The Correlation Level Detector — The correlation level detector consists of a voldicon, a serializer, an integrator, a digiswitch, and a time counter. The correlation level, which is measured as an analogue voltage, is sampled once during each major machine cycle and converted to digital form by the voldicon. It is then fed into the system through the serializer which converts the parallel binary output of the voldicon into the serial binary numbers used by the system. An adequate number of samples* (as determined by the received S/N ratio) is taken for each shift position and integrated to insure that the correlation indication is independent of background noise. The number is set manually by the operator prior to a ranging mission by means of the digiswitch, which determines the number of machine cycles counted by the time counter.

The parallel binary output of the voldicon is converted to series binary during tC minor machine cycle. Because of the limited number of input gates on the LE 10. several cards, connected in series are used. Since true reference time

*The total acquisition time is a direct function of the number of samples. To keep this time at a minimum, only an adequate number of samples can be taken.

occurs only at the output of the last card, the inputs to all other cards are referenced to smaller binary numbers to allow for the required processing delay (which will recreate the correct number). The 2's complementer circuit is used as a subtraction circuit. The final output of the serializer (VF) is passed into the integrator only when the timing counter is actually counting (as controled by $\overline{UK}$). The integrator is a combination addition circuit and storage register. It is set to zero by simply inhibiting all sum and carry outputs for 31 microseconds by means of the start integration gate bar ($\overline{UN}$) signal. When all samples have been added, the register contains the correlation integral for the particular code shift position.

The number of samples taken for each shift position is determined by the manual setting of digiswitch located on the control panel. The switch setting permits a binary choice from 2^0 to 2^{19} samplings per shift position. The binary number corresponding to the switch positions is set into the series binary logic of the system through the use of four LE 10 logic cards (each gate of which is connected to one switch position).

The timing counter, which uses a decremental type action, measures the required time delays for entrance into program states 1 and 2, and sets the number of samples fed into the integrator during states 3, 4, 5 and 6. It consists of a delay counter loading (UF) circuit, which determines the maximum (or initial) count; a pulse generator, which generates the sample time pulse (ZC) once every major machine cycle (at t3 and tC); a unity subtract circuit which does the actual decrementing to furnish the delay count down (UG) output; a storage register, which reintroduces the counter storage (UH) signal as the new input to the counter; and a negative detector which triggers the 124 microsecond train of delay count finished (UK) pulses.

The counter loading number is determined by the program state. Since it is not used during the program reset state, the counter is kept in the count finished condition by the introduction of a continual stream of pulses ($\overline{NR}$) as a loading signal. At the start of program states 1 and 2, the start delay (SD) signal loads the counter with a t13 timing pulse, which (because of processing time delays) puts a 2^{12} initial count into the timer. During states 3, 4, 5 and 6 two input loading signals are generated. The counter would normally be loaded after each shift gate signal (ZW). However, after any code component shift, a certain amount of time must be allowed for the transients introduced in the correlation detection circuits to settle down. The timing counter is used for the determination of this interval. The shift command signal first loads the counter with a t7 timing pulse, which puts a 2^6 initial count into the timer. The delay count finished (UK) signal obtained after this quieting interval allows the $\overline{ST}$ signal to trigger the start integration (UN) gate which allows the number selected by the digiswitch to preset

the counter for the proper integration time. Note that the presence of control signals on one gate to allow the proper loading are accompanied by controls on the other gates to erase all previous counts by inhibiting the feedback from the register. The absence of loading signals allows the feedback from the register to load the counter with the decremented number.

Since the largest loading number to the counter is the 2^{19} input from the digiswitch, the 2^{30} position in the register can be filled only when the count goes negative (i.e. when the zero count is decreased by one). Therefore the negative detector which generates the count finished signal need only examine this point. Because the serializer interrogates the voldicon during the tC machine cycle, the t30 position occurring in the tD cycle has been selected to generate the count finished pulse. Note that the sample time pulse (ZC) is also generated during the tC machine cycle to correspond to this selection. The delay count finished signal (UK) prevents the serializer output from feeding into the integrator, and furnishes the control for the generation of the shift command (ZV) and the start integration gate (UN) signals.

4.5.2 The High Correlation Level Storage Unit — The high correlation storage unit contains a storage register, a gate, and a magnitude comparator. The register is composed of a 31 microsecond circulating delay line and the appropriate ... in (YD) and read out (YE) circuitry. It retains any number fed into it, until replaced by another number, since there is no erase mechanism. The magnitude of the numbers in the integrator and high correlation storage registers are compared continuously in the comparison circuit, which makes an algegraic comparison. The output of the comparator, called the voltage ± gate (YF), is examined at the end of each code shift by the next shift command signal (ZV) to determine the higher value. If the integrator output (YC) is higher, it replaces the number circulating in the storage register.

At the start of each subcode acquisition, the storage register is loaded with a negative number (all binary positions are filled) by the action of the acquire gate (A) and $\overline{t30}$ control gate. This guarantees that the integrator output at the end of the first code shift will be fed into the register. In the automatic acquisition process, the output of the comparator (YF) is read on command of the following shift command (ZA). A favorable comparison triggers the transfer gate flip flop, generating a 31 microsecond transfer gate (YG) which allows the number stored in the integrator storage register to pass into the high correlation storage register. The transfer gate (YG) can also be triggered manually by the store pulse. The waveforms by which this manual signal is synchronized to the system timing logic are similar to those described earlier.

4.5.3 The Shift Position Counter — The shift position counter consists of a code length generator, and a counter. It is similar to the timer counter in that it

uses a decremental action, selective loading arrangements, a count finished detector, and is loaded twice per program state. The actual implementation is quite different. At the start of each acquisition period, it is loaded with the appropriate code length plus one. It is then decremented by each shift gate pulse (ZW) until the finish one detector (ZK) has been reached which triggers the count finished (ZL) flip flop. The reload shift position counter (ZR) signal which is also triggered by the (ZK) signal again loads the counter. This time the counter decrements to the value stored in the high correlation shift position storage, as detected by the equality detecter ($\overline{ZP}$) which triggers the component acquired signal (ZQ).

Because of the two sequential output signals required (ZL and ZR), it is easier to implement the counting mechanism by starting with the code length plus one. The proper loading number is selected by a series of "and" gates, and fed into the counter as a shift position input signal (ZE). (Note that all loading numbers are generated in sufficient time to allow for processing delays). The shift gate (ZW) which acts as a decrement pulse initiates a train of shift position counter control pulses (ZF). The number of pulses is a function of the number currently circulating in the register, since the occurrence of the first "one" in the series binary number coming from the register automatically resets the (ZF) flip flop. When the resultant train of pulses is added modulo two to the number currently in the register, it reduces that number by one.

The finish (one) detector is a simple flip flop (ZK) which is set at t1 and reset by the occurrence of the first "one" in the series binary number coming from the register. The state of the flip flop is examined at t30. As long as there are ones coming from the register, between t1 and t30, the flip flop will be in a reset condition at t30. However when the count has decreased to one, the flip flop will still be in the set state at time t30 and the ZL flip flop will be triggered to give the count finished (ZL) signal. The output of the (ZK) flip flop is also used in the generation of the reload shift position counter (ZR) signal. This signal is not required until two machine cycles later; it is generated by examining the output of the (ZK) flip flop at time t1. The (ZR) flip flop generates a train of 31 microsecond pulses which allows the counter to be reloaded. Again, note that all time is relative to that of the position input (ZE) signal.

4.5.4 The Shift Position Storage — The shift position storage contains a gate, a storage register and a shift position equality detector. When a new number is stored in the high level correlation storage, the equivalent shift position of the subcode is gated into the shift position storage. When the correlation level at all shift positions has been examined, the code is reshifted to the position stored in the shift position storage, as indicated by the equality detector.

The unit is loaded by the number currently in the shift position counter delay line (ZH) by the same transfer gate (YG) signal that loads the high correlation storage register described earlier. This number circulates in the storage register until a new number is introduced to replace it. A new number cannot be stored after the count finished (ZL) signal is generated.

The inputs of both the shift position counter (ZG) and the shift position storage (ZM) are fed into a modulo two adder, whose output is zero only if the two numbers are alike. The actual comparator generator is a flip flop which is reset by every t30 timing pulse, and set by the output of the modulo two adder. The output of the equality detector flip flop (ZP) is also sampled by every t30 timing pulse. When the output of the modulo two adder is zero, the flip flop will still be in a reset state at the next t30 interval, and the equality detector ($\overline{ZP}$) will trigger the component acquired (ZQ) flip flop. This signal denotes the completion of the code acquisition process and the system progresses to the next program state.

4.5.5 The Code Shift Generator — The code shift generator produces the three signals (ZV, ZW, and UN) needed by the timers to set the subcode to the shift position with the highest correlation. The shift command (ZV) is generated by the first count finished (UK) signal from the timing counter. It examines the output of the high correlation magnitude comparator (YF), triggers the shift gate (ZW) flip flop and sets the (UP) control mechanism for the generation of the start integration gate (UN) signal. The shift gate (ZW) signal permits the loading of the correlation time interval counter for the quieting interval following each one bit shift of the subcodes. The second count finished (UK) signal which is generated at the end of this quieting interval triggers the start integration gate (UN), which loads the counter with the preselected digiswitch number. The count finished signal (UK) which is generated at the end of this time interval is again directed to the shift command logic and ZV is generated to repeat the sequence. Note that to guarantee a proper two sequence operation during state P3, the acquire command (AC) signal automatically sets the shift gate static (ZWS) and the selector flip flop (UP) since they can be in either position when initially energized.

After the desired shift position is determined the code is returned to that position, by generating the required shift gate (ZW) pulses without the accompanying timer counter delays. This mode of operation occurs during that interval when the finish signal (ZL) from the shift position counter has occurred and the component acquired (ZQ) signal has not. It is implemented by the (ZL, $\overline{ZQ}$, SD and manual shift bar) "and" gate which acts on the (ZW) flip flop. These (ZW) pulses are generated once every major machine cycle by the ($\overline{ST}$) pulse train.

4.6 The Range Tally

The range tally is an accumulation device which stores the range number (in series binary form) in a 31 microsecond, 31 bit circulating register. It consists of a 28 microsecond magnitostrictive delay line and three binary adders connected in series, which are called appropriately the chinese number adder, the doppler adder, and the modulo number adder. A flow diagram of the tally is given in Drawing 9. The input to the adders are the number circulating in the delay line (DL), the chinese number ± gate ($\Sigma \pm$), the doppler ± gate (D ±), and the modulo number ± gate (M ±). The output of the range tally is that of the modulo number adder (MA) which is fed into the readout register. All range numbers have their true values here, since there are no processing delays at this point. Since this is a circulating register, a blocking mechanism is included in the carry portion of each unit to prevent overflow. These blocks occur at t 27, t 28, and t 29 for the successive units.

The range tally is zero set during program state 2, when the code synchronization takes place. The same signal (SY) which was used to synchronize the codes, blocks the flow of range numbers through the chinese and modulo adders to clear them. The lock out (LO) signal (which will be discussed later) clears the doppler adder.

4.7 The Chinese Number Generator

The chinese number generator provides the range numbers in serial form which correspond to the total code delay resulting from a one bit shift in each of the subcodes. These numbers are brought into play during the acquisition process. The actual numbers themselves are derived in Appendix E.

A flow diagram showing the method by which these numbers are generated and fed into the system is given in Drawing 8. These numbers are generated using the negative output of the LE 10 (to reduce the required circuitry). The logic input is advanced to compensate for the processing delay between the generation and use of these numbers. For example, $\overline{AS}$ is generated as an octal number of 10000012115 (or 1,073, 747,021 range units) but is used as 2,423,300 (or 665,288 range units), which is the correct chinese number. Once generated, the flow of the individual chinese numbers is controlled by the use of "and" gates so that they are fed into the system only during the appropriate acquisition states. When a subcode being acquired is shifted one bit, the control mechanism opens the proper gate for 31 microseconds allowing the selected number to be fed into the chinese number ± ($\Sigma \pm$) gate. In the automatic acquisition mode, all shifts are in the shift right direction. During the manual mode which is used only for test purposes, a shift left, which requires a subtraction of the equivalent number,

is also possible. This subtraction is converted to an addition by means of the 2's complementer. Notice that all control circuitry is initiated at t26 to account for the processing time delay between the point of control and the true time occurring at the output of the range tally (MA). The wave forms and the timing associated with these control signals are given in Drawing 14, showing their relationship with the acquisition process.

4.8 The Doppler Number Generator

The range measured at the start of the acquisition process is updated by doppler numbers fed into the tally at intervals corresponding to every quarter cycle of clock doppler during the acquisition process, and every four cycles of rf doppler thereafter. The doppler signals are fed into the system through axis crossing detectors located in the Voldicon which transform them into square wave equivalents. These are synchronized to the basic system clock by the doppler synchronizer shown in Drawing 9. Two doppler signals, obtained by quadrature detectors are provided to detect the direction of the doppler signal. These signals are called the clock 0° and clock 90°. The wave shapes given in Drawing 15 show the method by which the direction of the doppler signal, and its zero crossings are detected to furnish the add and subtract pulses as needed. For simplicity, the clock doppler going in a positive (i.e. 0° signal before 90°) direction is chosen as an example. The true sense of the doppler can be determined from the resulting waveforms by examining the changes in polarity of the signals at the zero crossings. The four relationships selected by the detection logic define each of the four possible combinations that can occur only for a positive going signal. The detection of a negative going signal requires four different relationships. In the acquisition states, denoted by $\overline{DS}$, in which the clock doppler is detected, all four zero crossings give an add pulse (AP). In state P7 where acquisition has been accomplished (denoted by DS), and only the rf doppler is to be tallied, only one add pulse per doppler cycle is derived.

The add pulse is converted to a 31 microsecond train of add signal (AD) pulses which permits the addition of the appropriate range number into the tally. Because of the frequencies used, this requires 72 range units per quarter cycle of clock doppler, and one range unit per 4 rf doppler cycles. A flow diagram of this logic circuit is shown in Drawing 9. In the code acquisition states (P3, P4, P5 and P6) the add pulse (AP) goes directly to the input of the add signal (A) flip flop because the doppler select (DS) signal inhibits the divide by four logic. In the non-acquisition state (i.e. P7) only one add pulse out of four (by means of the two binary stages) are allowed to be gated to the add flip flop. During the acquisition states, denoted by $\overline{DS}$ the 72 range units generated in the number generator ($\overline{NG}$) are fed into the doppler ± gate, while in the non-acquisition state denoted by DS, only one range unit generated at t27 (to allow for processing delays) is fed

into the gate. This circuit utilizes the same type of add and subtract mechanism as the chinese number generator discussed earlier.

Two important doppler control signals that are required during the acquisition process are the lock out (LO) signal and the subtract two (SZ) signal. The flip flop used to generate these signals is reset during state P2 by the synchronization signal (SY). It is important to remember at this point, that there is no doppler signal during the synchronization state (P2). Both signals are generated at the start of the acquisition process by the doppler signal. If it has a positive direction, the lock out signal (LO) is generated in coincidence with the first zero crossing of the 90 degree doppler signal. The add pulse which is generated simultaneously by the same logic allows one doppler range number to be inserted into the tally. If the doppler has a negative direction however, the lock out signal (due to its input logic) will not be generated until the first zero crossing of the doppler 0 degree signal which occurs at 180 degrees (90 degrees later than for a positive going signal). Therefore the first subtract pulse (which was generated at the first crossing of the 90 degree doppler signal) canot be tallied because it occurred before the lock out signal enabled the output of the doppler generator. The subtract pulse which is generated simultaneously with the lock out signal must therefore subtract two doppler numbers from the tally. This condition is recognized by the subtract two input logic which generates the new number by inserting a one microsecond time delay into the doppler number fed into the range tally (see Drawing 9). Note that the subtract two signal can only be generated during the interval between the synchronization of the codes and the generation of the lock out signal. The waveforms and the timing associated with the generation of the lock out (LO) signal are also shown in Drawing 15.

The r f doppler selector signal (DS) determines which doppler signal is bein tallied. It allows the clock doppler to be tallied during the acquisition state and the r f doppler thereafter. The doppler selector ($\overline{DS}$) signal is automatically generated when the system is energized. The first add or subtract doppler signa that occurs during program state P 7 triggers the DS flip flop to generate the Doppler Select condition.

4.9 The Modulo Number ± Gate

The Modulo number corresponds to the unambiguous range of the system. It is numerically equal to the product of the four subcode lengths and the two bit clock. It is generated by the same type of logic used to generate the chinese numbers. When the subcodes are being shifted, it is possible for the indicated range number to exceed the modulo number. The modulo number must therefore be subtracted to give a true reading. When the range number goes negative, under the same conditions, the modulo number must be added. These two unnatural

states are recognized by the greater than comparator (G), and negative detector (ND) which feed the correcting numbers into the modulo ± gate. A flow diagram showing the generation of these signals is given in Drawing 9.

The modulo number ± gate signal is derived in the same manner as the other ± gates. When the range number goes negative, the negative detector enables a control gate and the modulo number is gated into the range tally. When the range number exceeds the modulo number, the greater than comparator (G) triggers the subtract M gate (SM) which allows the 2's complement of the number to enter the tally. Since the most significant digit ever required to display the range number is 2^{29}, a one can exist in the t30 position only if the number has gone negative. Therefore the negative detector is merely an "and" gate designed to examine this point which occurs at t27 to account for processing delays. The presence of a one triggers the negative detector flip flop generating a 31 microsecond train of pulses, which gates the modulo number into the tally. The greater than comparator is more complicated than the negative detector because all the digit places must be examined. Since the comparison is made on a digit to digit basis, a greater than output signal can occur several times during the 31 microsecond comparison interval. However only the final state of the comparator circuit (occurring at t28) is allowed the trigger the (SM) flip flop due to the intervening gating circuitry. Note that a control is added to the input logic of both the SM and ND flip flops to guarantee that one signal will not be generated while the other is activating the modulo ± gate.

4.10 The Readout Register and Output Buffer

The readout register is made up of a static 31 stage shift register. When a readout command pulse is received from the data handling system, it causes the number currently stored in the register to be cleared, and allows the range number circulating in the range tally to replace it. The contents of the register remain static until the next readout command is received. The readout register is disabled until the end of the acquisition process (state P7).

The readout command pulse (or time tick) is passed through a synchronous generator to provide a single pulse RO synchronized to the 1 mc bit rate of the system. This signal resets the first flip flop to provide the Priming Gate (PG) signal which resets the shift register (i.e. zero sets all stages) and triggers the one's filler (OF), and zero's filler (ZF) flip flops. These signals which are on for 30 microseconds (starting at t0) provide the drive to the shift register allowing them to record the output of the range tally.

The error light flip flop is also set during the clearing process by the readout command pulse. If a complete 30 bit shift does not take place during the readout of the tally, the flip flop will remain set, and give an error indication.

The odd even flip flop indicates that a complete acquisition has taken place. It does so by changing its logic state one per acquisition interval.

The output buffer consists of 31 relays which are activated on a one for one basis by the zero outputs of the corresponding flip flops of the 31 stage readout register. Their state is sampled by the data handling system at desired intervals. The output, given in binary form, can be converted to any desired form for reading and transmission.

A flow diagram showing the operation of these units is given in Drawing 10.

4.11 Test Signals

The entire system is capable of being exercised manually for test purposes. Switches on the control panel, operate on control gates in the system to shift the receiver coder either right or left; store the output of the correlation integrator in the high correlation storage register; advance the program state; reset the system; or feed the output of the range tally into the readout register. The mechanization of these controls has been described earlier under their respective sections.

The system can be exercised in the automatic mode if two important signals which simulate the spacecraft are supplied. These are the doppler signals which indicate motion, and the correlation signal which is a measure of the initial range, or code displacement.

The simulated doppler signals can be generated either manually or automatically as desired. A three position switch on the test panel determines which doppler signal (normal, manual, or automatic) is fed into the digital system. There are two sine-cosine potentiometers located on the test panel which manually generate the 0 and 90 degree versions of the clock or the rf doppler when rotated. Noise is introduced by jiggling the handles. There are two sets of FD 10 flip flops located in the range tally module which automatically generate the 0 and 90 degree versions of the clock and rf doppler when triggered by an externally supplied source of drive pulses. These pulses are usually obtained from the time base generator of the Systron Donner Counter used for check out purposes. A flow diagram showing the generation of these automatic doppler signals is given in Drawing 8. As can be seen the flip flops are arranged as a shift register. A change in one effects the other, but both must be set before the first can be reset, and both must be reset before the first can again be set. The switch rate is dependent on the input pulses which are passed through the usual synchronous generator.

A simulated correlation voltage is obtained by adding modulo two the delayed output of the transmitter coder (db4) with the output of the receiver coder. As is the case with the true correlation signal, the maximum voltage is obtained when the receiver coder has been shifted the proper number of bits. The circuitry required to generate the delayed transmitter coder (i.e. received code) signal, and the required receiver coder signal was discussed previously under the appropriate sections.

5.0 THE GSFC STUDY MODEL

The digital portion of the JPL Mark 1 ranging system has been duplicated at GSFC. It is electrically identical to that of the original. Since the rf portion was not built, the clock and doppler signals normally derived from that portion of the system are not available. Two special impedance matching amplifiers were built, so that the oscillator and time base outputs of the Systron Donner Counter could be used for those purposes. The oscillator amplifier (Figure 11) furnishes the one mc drive for the T pac units. The time base amplifier (Figure 12) can be used to furnish either the drive for the automatic doppler generator, or the time tick signal for the readout register. The output of the modulo two adder which correlates the delayed transmitter coder output with the receiver coder output was passed through an r c integrating circuit to furnish the correlation input to the voldicon.

The operation of the local system is identical to that of the JPL version when operated in the manual mode. Automatic operation of the local system was made possible by the introduction of switches designed to simulate the external indicating signals fed into the JPL system during a normal automatic acquisition process.

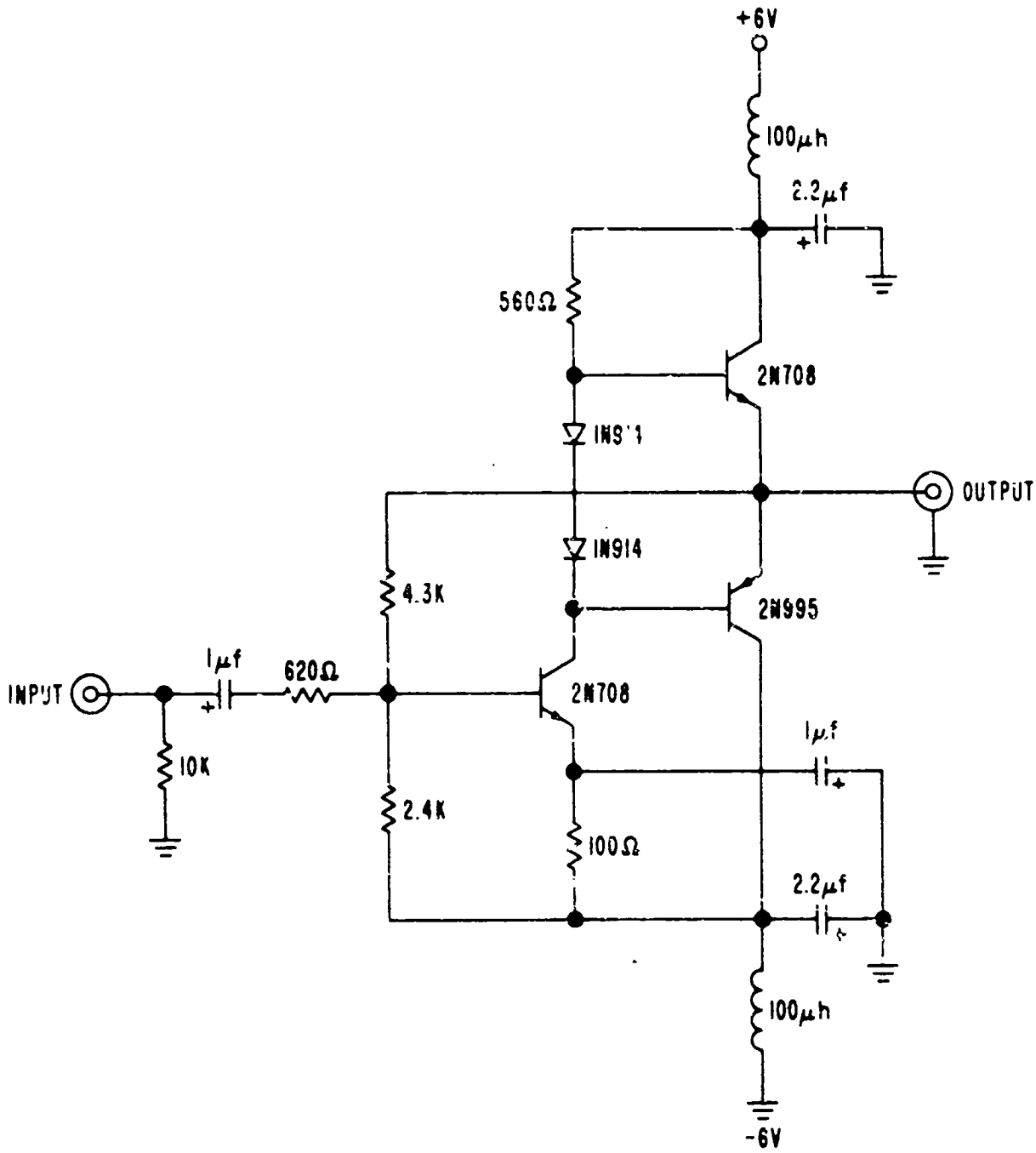

Figure 11. Schematic Diagram — Clock Oscillator Drive Amplifier

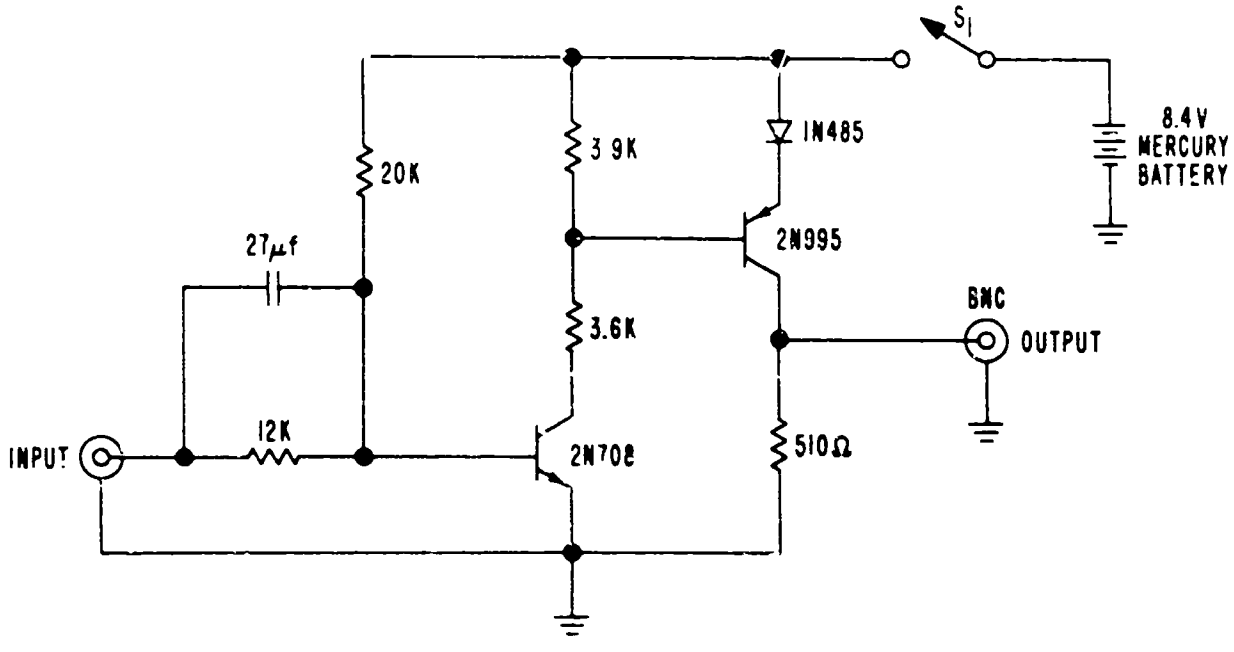

Figure 12. Time Base Amplifier

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APPENDIX A
DESCRIPTION OF EQUIVALENT LOGIC CIRCUITS

The digital portion of the Mark 1 system has been implemented by means of the digital cards described in Appendix C. A set of equivalent circuits (Drawings 2-10 inclusive) has been generated at GSFC which describe the logical operation of the system in terms of these cards. Several conventions have been adopted to simplify the logic and hence the understanding of the presentation. These conventions, and the reasoning behind them are given below:

1. The T pac system is basically a clocked system. Most of the cards have a dynamic return to zero (RZ) output waveform. The FD 10, the special cards and the relays however use static logic and have a non-return to zero (NRZ) output waveform. Since only the state of the signal during the clocked interval is important, all waveforms will be presented in a NRZ form.

2. Each card making up the subsystem is identified by a unique mnemonic name (i.e., shorthand notation by a couple of letters and numbers) according to function. In the development of the system, however, some names have inadvertently been assigned to two cards. These cards are distinguished from each other by the simple expedient of adding, in parenthesis, the unit from which they originated.

3. When a mnemonic name appears on the drawings, the designated function corresponds to the output of a card. All other points on the drawings are equivalent circuit logic points which may or may not correspond to actual internally identifiable logic points on the card. Since each name identifies the output of a card, the one bit delay which is inherent between input and output of each T pac card must be assumed as occurring at these points.

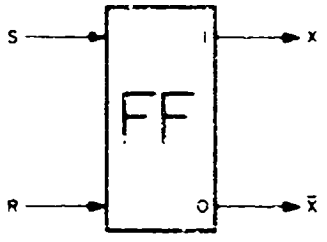
4. The LE 10, the FD 10, the SM 10 and the TG 10 all have both a true and a false output available. To simplify the drawings, only the true output is shown. An inverter has been incorporated into the drawings to show the false output when needed.

It is difficult to incorporate the internal logic of the cards into the overall logic of the system. Therefore, an equivalent circuit has been evolved to simplify the presentation. Although these equivalent circuits describe the properties of the card, they may not be exact with respect to the internal operation. However, it is not necessary to do so since the internal operation of each card to

present an overall description of the system. For example, where feedback has been used in the LE 10, the logical properties usually constitute a flip flop or other storage device. Since it is this feedback which complicates the understanding of the logic, it has been incorporated into an equivalent logic element which presents the card in terms of its overall usage. These equivalent circuits are given in Figures 13 and 14. Any equivalent circuit not found in these figures is self-explanatory as presented.

There are three types of flip flops appearing in the drawings. The flip flop labeled binary trigger (number 3) has only one input, and will change its output state each time it is pulsed with a clock pulse. The other two have both a set and a reset input. The state of the flip flop depends on the application of the last input signal. If for any reason, the reset and set inputs of an FF flip flop (number 1) are triggered simultaneously, the set input will always predominate. If the set and reset inputs of an FD flip flop (number 2) are triggered simultaneously, the output will change state for each clock pulse for which this condition is true. Circuits number 4, 5 and 6 are respectively an "and" gate, an "or" gate and an inverter. These logic units are used to represent internal parts of the LE 10 and FD 10 cards. Circuit number 7 represents the one bit delays found on a DF 10 card. Circuit number 8 represents an LE 10 card used as a modulo two adder. Circuit number 9 represents a TG 10 card which accepts an input pulse and generates a pulse which is synchronized to the internal clock drive of the T pac system. Circuit number 10 is used to present the serial delay line represented by an SM 10. Circuit number 11 represents an adder which is used for adding two binary numbers. It generates a sum bit and a carry bit, and uses more than one card in its operation. Circuit number 12 represents an algebraic comparator for comparing two serial numbers. The numbers are fed in lower order first. The output is valid only after the most significant bit has passed through the comparator. Circuit number 13 represents a unity subtractor. It subtracts a single pulse S from the serial input number A. Circuit number 14 is a 2's complementer. Input A is subtracted from all zeros and the final borrow is discarded. Input R resets or inhibits any overflow carry from the first serial number into the next serial number. Circuit 15 is a special buffering card which has essentially no time delay.

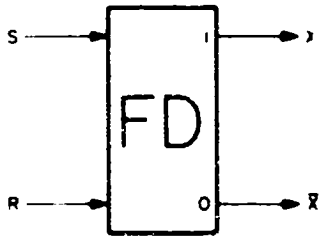
(1) (LE-10 CARD)



$x^1 = x\bar{R} + S$

S	R	X^1 (ONE BIT TIME LATER)
0	0	X (PREVIOUS VALUE)
0	1	0
1	0	1
1	1	1

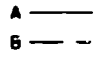
(2) (FD-10 CARD)



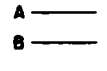
$x^1 = x\bar{R} + \bar{X}S$

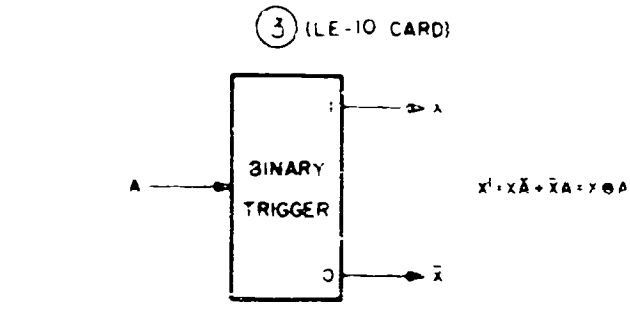
S	R	X^1 (ONE BIT TIME LATER)
0	0	X (PREVIOUS VALUE)
0	1	0
1	0	1
1	1	$\bar{X}$ (COMPLEMENT OF PREVIOUS VALUE)

(4) AND GATE

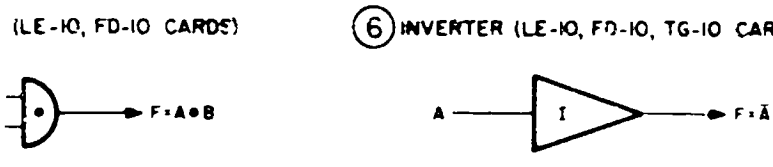


(5) OR GATE





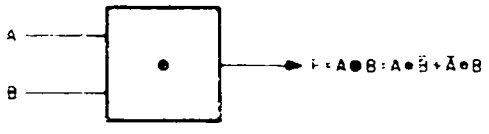
A	x^1 (ONE BIT TIME LATER)
0	x (PREVIOUS VALUE)
1	$\bar{x}$ (COMPLEMENT OF PREVIOUS VALUE)



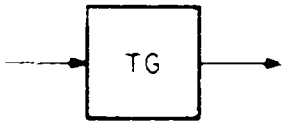
SIGNATURES		DATE	NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
DESIGNED			GODDARD SPACE FLIGHT CENTER
DRAWN	YAGEL	3/18/65	GREENBELT, MD
APPROVED	SPAFFORD		
DIVISION — NET ENGRG & OPRS			APOLLO RANGING DATA SUBSYSTEM
BRANCH — NETWORK ENGINEERING			EQUIVALENT LOGIC CIRCUITS
BLDG 12	ROOM E-14	PHONE 4677	
SECURITY CLASSIFICATION			ASSEMBLY DRAWING NO / SCALE / DRAWING NO

Figure 13. Equivalent Logic Circuits

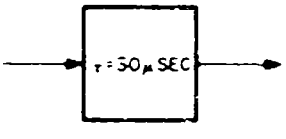
(8) EXCLUSIVE OR (LE 10 CARD)



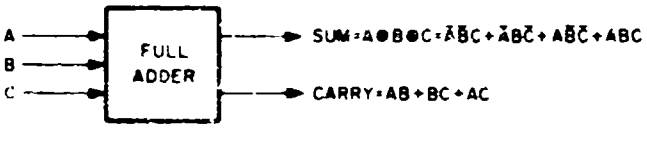
(5) (TG-10 CARD)



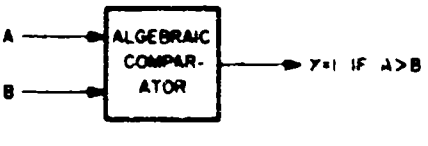
(10) DELAY LINES (DELAY TIME IS τ)



(11) (LE-10 CARD)



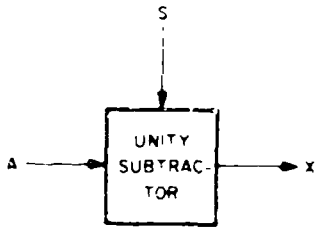
(12) (LE-10 CARD)



Y=XAB+XĀB̄+AB̄ t̄o+ĀB to

to=SIGN BIT

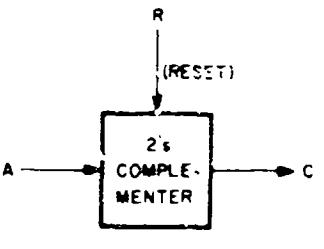
(13) (LE-10 CARD)



$X^1 = \bar{X}\bar{S}A + X\bar{A}\bar{A}^1 + AA^1\bar{S} + \bar{A}S$

$A^1 = A$ (DELAYED ONE BIT TIME)

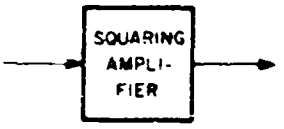
(14) (LE-10 CARD)



$C^1 = \bar{A}^1 \cdot A \cdot \bar{C} + A^1 \cdot \bar{A} + \bar{A} \cdot C \cdot R$

$A^1 = A$ (DELAYED ONE BIT TIME)

(15) BUFFERING AMPLIFIER AND SHAPER WITH NEGLIGIBLE TIME DELAY (SPECIAL CARD)



SIGNATURES		DATE	NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MD
DESIGNED			
DRAWN	YAGEL	3/[illegible]/66	
APPROVED	SPAFFORD		
DIVISION — NET ENGRG & OPRS			APOLLO RANGING DATA SUBSYSTEM
BRANCH — NETWORK ENGINEERING			EQUIVALENT LOGIC CIRCUITS
BLDG: 12	ROOM: E-IC	PHONE: 4877	
SECURITY CLASSIFICATION		ASSEMBLY DRAWING NO	SCALE / DRAWING NO

Figure 14. Equivalent Logic Circuits

APPENDIX B
R F TRANSLATION CALCULATIONS

The following calculations describe the frequency translations of the ground transmitted signal which occur in the spacecraft transponder, and the ground receiver to derive the equations for the output of the doppler extractor. The equations are written in terms of the individual VCO's of the ground transmitter, the spacecraft transponder, and the ground receiver. The biased doppler output of the doppler extractor is given in terms of the two way doppler on the received carrier frequency (240/221 f_t) superimposed on a bias frequency. The UHF doppler is given in terms of the two way doppler as $\frac{1}{4}$ the received carrier frequency.

Frequency Translations in the Spacecraft Transponder (see Figure 2)

The frequency of the signal received by the spacecraft is given by

$$f_t \pm f_{td} = 96\ (f_{vcot} \pm f_{vcotd}) = f_{rs/c}$$

where f_t = frequency of transmitted signal

f_{vcot} = frequency of ground VCO

d = doppler on the signal designated by preceding subscripts.

The frequency of the signal out of the 1st IF mixer is given by

$$(f_t \pm f_{td}) - 216\ (f_{vcos/c} \pm f_{vcos/cd}) = \text{1st IF}$$

where $f_{vcos/c}$ * = 1/2 frequency of the spacecraft VCO. i.e. the frequency of the input to the VCO phase detector.

The frequency of the signal out of the second IF mixer is given by

$$(f_t \pm f_{td}) - 216\ (f_{vcos/c} \pm f_{vcos/cd}) - 4\ (f_{vcos/c} \pm f_{vcos/cd}) = \text{2nd IF}$$

or $$(f_t \pm f_{td}) - 220\ (f_{vcos/c} \pm f_{vcos/cd}) = \text{2nd IF}$$

but $$\text{2nd IF} = (f_{vcos/c} \pm f_{vcos/cd})$$

*Since the spacecraft VCO is divided by two for use in the phase locked loop's phase detector, it is used as $2f_{vcos/c}$ in the calculations, for convenience.

therefore $(f_t \pm f_{td}) = 221\ (f_{vcos/c} \pm f_{vcos/cd})$

or $\frac{f_t \pm f_{td}}{221} = f_{vcos/c} \pm f_{vcos/cd}$

It follows therefore that

$$f_{vos/c} = \frac{f_t}{221} \text{ and } \pm f_{vcos/cd} = \frac{\pm f_{td}}{221}$$

These equations can be checked by letting $f_{vcos/c}$ derived from the 1st IF equation equal $f_{vcos/c}$ derived from 2nd IF equation and inserting the actual values for known constants, so that in the static case

$$\frac{f_t - \text{1st IF}}{216} = \frac{f_t}{221}$$

or 9.53 mc = 9.53 mc

The frequency of the signal transmitted by the spacecraft is given by

$$240\ (f_{vcos/c} \pm f_{vcos/cd}) = f_{s/c}$$

but $(f_{vcos/c} \pm f_{vcos/cd}) = \frac{f_t \pm f_{td}}{221}$

therefore $f_{s/c} = \frac{240}{221}\ (f_t \pm f_{td})$

Frequency Translations in the Ground Receiver (see Figure 3)

The frequency of the signal received from the spacecraft is given by

$$\frac{240}{221}\ (f_t \pm f_{td}) = f_{td'} \pm (240\ f_{vcos/cd}) = f_{rr}$$

where $f_{td'}$ is the down doppler on the up doppler.* For simplicity, this term will not be carried in succeeding equations.

*This term is numerically equal to $\pm 240\ f_{vcos/c\ dd}$

But as was derived above,

$$\pm f_{vcos/cd} = \pm\frac{f_{td}}{221} \text{ so that } \pm 240\, f_{vcos/cd} = \frac{\pm 240}{221} f_{td}$$

and therefore

$$\frac{240}{221}(f_t \pm 2 f_{td}) + f_{td'} = f_{rr}$$

The signal out of the 1st IF mixer is given by:

$$\frac{240}{221}(f_t \pm 2f_{td}) - 96\,(f_{vcor} \pm f_{vcord}) = \text{1st IF frequency}$$

or $$96\,(f_{vcor} \pm f_{vcord}) = \frac{240}{221}(f_t \pm 2f_{td}) - \text{1st IF frequency}$$

so that

$$(f_{vcor} \pm f_{vcord}) = \frac{240}{96 \times 221}(f_t \pm 2f_{td}) - \frac{\text{1st IF frequency}}{96}$$

Since in this system, the 1st IF frequency is held relatively constant, the doppler ($2f_{td}$) must be removed at the first mixer by the difference frequency of the VCO (resting frequency $\pm\Delta f$ due to the doppler). The full doppler excursion must be removed at the 1st IF because the 2nd IF is mixed with a constant frequency.

The equation above can be broken into the static and dynamic cases. The static case is given by:

$$f_{vcor} = \frac{240}{96 \times 221} f_t - \frac{\text{1st IF frequency}}{96}$$

The dynamics is given by:

$$\pm f_{vcord} = \pm\frac{240}{96 \times 221}(2 f_{td})$$

The signal out of the 2nd IF mixer is given by:

$$6f_{ref} - \text{1st IF} = \text{2nd IF}^*$$

or replacing the value of the 1st IF by its value derived above,

$$6\ f_{ref} - \frac{240}{221}\ (f_t \pm 2\ f_{td}) + 96\ (f_{vcor} \pm f_{vcord}) = \text{2nd IF}$$

where f_{ref} = reference frequency = 10 mc

from which:

$$(f_{vcor} \pm f_{vcord}) = \frac{\text{2nd IF}}{96} - \frac{6}{96} f_{ref} \pm \frac{240}{96 \times 221}\ (f_t \pm 2\ f_{td})$$

This equation may also be broken down into the static case where

$$f_{vcor} = \frac{\text{2nd IF}}{96} - \frac{6}{96} f_{ref} + \frac{240}{96 \times 221}\ f_t$$

and the dynamic variations where:

$$\pm f_{vcord} = \frac{\pm 240}{96 \times 221}\ (2f_{td})$$

These equations can be checked by letting f_{vcor} derived from the 1st IF equation equal f_{vcor} derived from the 2nd IF equation and inserting the actual values for known constants, so that in the static case

$$\frac{240}{96 \times 221} f_t - \frac{\text{1st IF}}{96} = \frac{\text{2nd IF}}{96} - \frac{6}{96} f_{ref} + \frac{240}{96 \times 221} f_t$$

or $-\text{1st IF} = \text{2nd IF} - 6\ f_{ref}$

or -50 mc $= 10$ mc $- 60$ mc $= -50$ mc

Frequency Translations in the Doppler Extractor (see Figure 4)

The frequency of the signal received from the Receiver Phase locked loop is given by

$$3\ (f_{vcor} \pm f_{vcord}) = f_{rde}$$

*Although no dynamics exist in the 2nd IF, after acquisition, the above equation reflects a dynamic compensation in order to carry the f_{ref} and f_{vcor} terms which are needed for the doppler extracter equations which follow.

Note that f_{vcor} of the 2nd IF is chosen because it contains f_{ref} which must be cancelled out in the doppler extractor or it will contribute errors to the doppler measurement.

The signal out of the 1st mixer is given by:

$$3(f_{vcor} \pm f_{vcord}) - 3\ f_{vcot} = \text{1st IF}$$

The signal out of the 2nd mixer is given by:

$$\frac{57}{221} f_{vcot} - 3\ (f_{vcor} \pm f_{vcord}) + 3\ f_{vcot} = \text{2nd IF}$$

The signal out of the times 8 output is given by:

$$3\left[\frac{57}{221} f_{vcot} - 3\ (f_{vcor} \pm f_{vcord}) + 3\ f_{vcot}\right] = \text{X8 output}$$

The signal out of the UHF range Extractor is given by:

$$8\left[\frac{57}{221} f_{vcot} - 3\ (f_{vcor} \pm f_{vcord}) + 3\ f_{vcot}\right] - \frac{5}{4} f_{ref} \pm \text{UHF Doppler}$$

In order to get the UHF doppler in terms of the doppler on the transmitted signal f_{td} only, a series of substitutions are made in this equation.

Replacing $(f_{vcor} \pm f_{vcord})$ by its equivalent term derived above, gives

UHF Doppler =

$$8\left\{\frac{57}{221} f_{vcot} - 3\left[\frac{\text{2nd IF}}{96} - \frac{6}{96} f_{ref} + \frac{240}{96 \times 221}(f_t \pm 2f_{td})\right] + 3\ f_{vcot}\right\} - \frac{5f_{ref}}{4}$$

which reduces to

$$\text{UHF Doppler} = \frac{456}{221} f_{vcot} - \frac{\text{2nd IF}}{4} + \frac{f_{ref}}{4} - \frac{60}{221}(f_t \pm 2f_{td}) + 24\ f_{vcot}$$

Replacing f_t by its equivalent term of 96 f_{vcot}, the 2nd IF by 10 mc and f_{ref} by 10 mc reduces this to its basic term of

$$\text{UHF range doppler} = \frac{-60}{221}(\pm 2f_{td})$$

The signal out of the biased doppler output is given by

$$4(\text{X8 output}) - 5 f_{ref} + f_B = \text{Biased doppler output}$$

where f_B = the bias frequency added to the doppler to eliminate the need for ± circuitry. It has a value of 1 mc.

Expanding this equation gives:

$$4\left\{8\left[\frac{57}{221} f_{vcot} - 3(f_{vcor} \pm f_{vcord}) + 3f_{vcot}\right]\right\} - 5 f_{ref} + f_B = \text{biased doppler}$$

Replacing $(f_{vcor} \pm f_{vcord})$ by its equivalent term derived above, gives:

$$\frac{23040}{221} f_{vcot} - \text{2nd IF} + f_{ref}\frac{-240}{221}(f_t \pm 2 f_{td}) + f_B = \text{doppler output}$$

Replacing f_t by its equivalent value of 96 f_{vcot}, 2nd IF by 10 mc and f_{ref} by 10 mc reduces this to its basic value of

$$\text{Biased Doppler output} = f_B - \frac{240}{221}(\pm 2 f_{td})$$

to which the down doppler on the up doppler must be added to obtain

$$\text{Biased Doppler output} = f_B - \frac{240}{221}(\pm 2 f_{td}) \pm \frac{240}{221} f_{td}$$

Note that the 240/221 ratio is used to translate the up doppler to equal the down frequency doppler which is the highest of the two. Therefore the derived equation equals the two way doppler on the received frequency.

APPENDIX C
LOGIC CARD DESCRIPTIONS

There are nine different logic cards used in the subsystem. Five are standard T-Pac units built by Computer Control Company, Inc; one is a modified T-Pac unit; and three are special cards designed for the JPL system by Decisional Control Assoc., Inc.

The LE 10 is the basic unit of the T-Pac system. Information is obtained at a one mc bit rate by the presence (assertion output) or absence (negation output) of pulses. The input logic is composed of four 4-legged and gates. The fulfillment of the logic requirements on any one of the 4 input gate; will give an output. As many as three of these gates can be ganged together to make a 4, 8, or 12 legged input. An inhibit gate, which can override the logic decision of the other gate inputs is provided for added flexibility.

The DP 10 is a standard T-Pac unit which contains four independent delay lines of one pulse period duration. They can be used to delay either assertion or negation pulses, and can be cascaded together for greater delay with tagged outputs at one pulse period intervals.

The FD 10 is a standard T-Pac unit which contains two independent static (NRZ) flip flop circuits. Each unit has three independent set gates and one reset gate. Internal steering insures that inputs applied simultaneously to both sides will complement the flip flop.

The TG 10 is a standard T-Pac unit which produces a synchronized pulse compatible with the T-Pac logic for every asychronous or random input pulse.

The SM 10 is a standard T-Pac serial memory module. It is made up of a magnitostrictive delay line, an amplifier-driver stage and a detector-amplifier stage. It is driven from a standard LE 10 negation output which provides both the write in and erase control logic. Both assertion and negation outputs are provided. Both 29 and 30 microsecond delay units are used in the system.

The JPL-1 is a modified T-Pac unit, which contains one FD 10 flip flop and one squaring amplifier driver. Contrary to standard T-Pac design, the output of the amplifier is balanced with respect to ground. The unit has a variable gain control on the amplifier. A schematic diagram of the amplifier section is given in Figure 15.

The SRT-8A is a custom made eight unit, relay card, which is used to feed control signals into the system. A schematic diagram is given in Figure 16.

Note that the output is similar to that of the digiswitch in that, the absence of an assertion signal is indicated by the presence of a negation signal.

The SRO-4 is a custom made four unit relay card, which is used to feed control signals out of the system. A schematic diagram of the unit is given in Figure 17.

The CSO-1 is a custom made clock synchronization card. It provides a means of deriving a standard logic level output synchronized with a clock coherent sine wave input. When the set trigger is enabled during the negative half cycle of sine wave input, a coincident clock pulse will set the flip flop, producing a negative output level. The next clock pulse resets the flip flop. A schematic diagram of the unit is given in Figure 18.

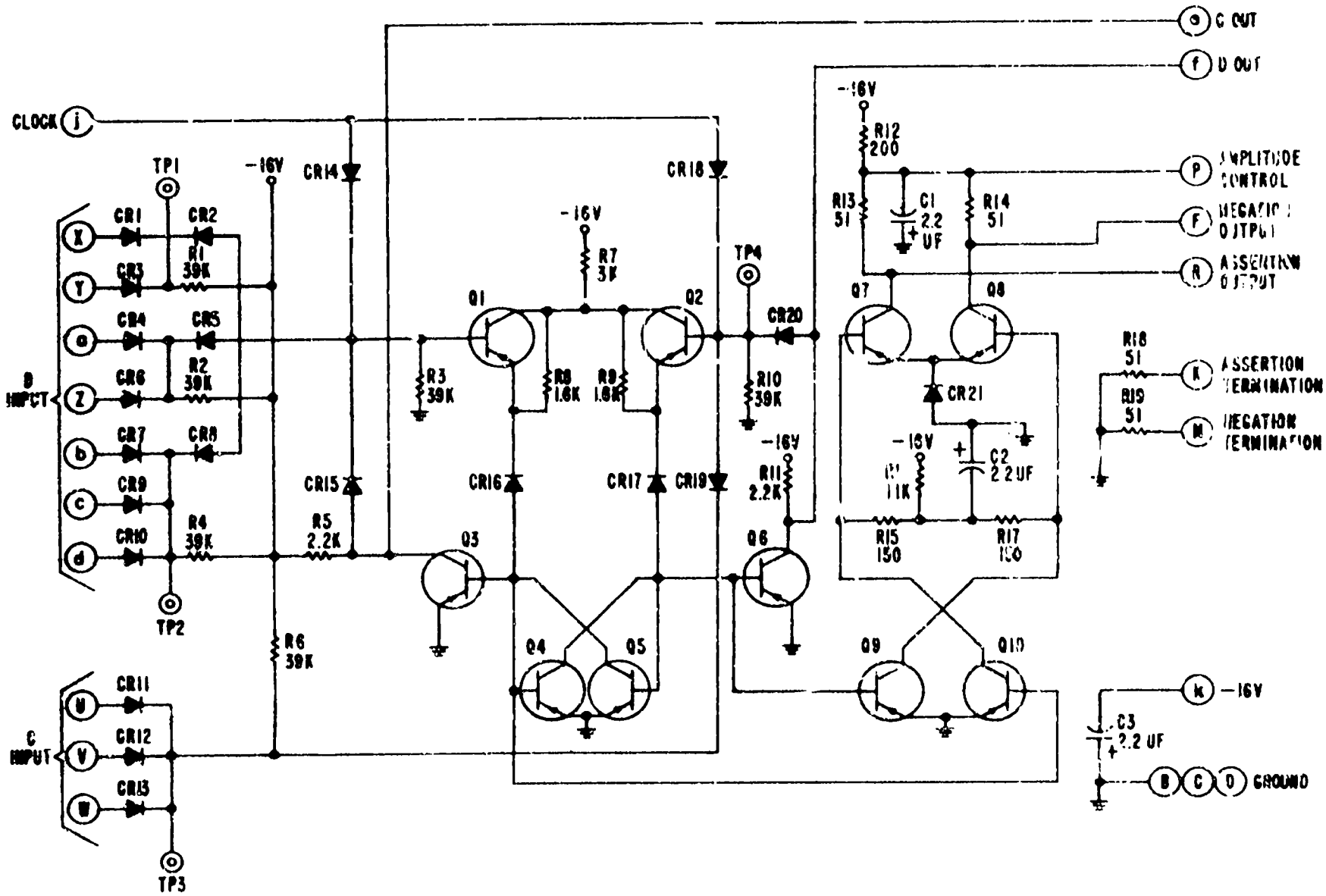
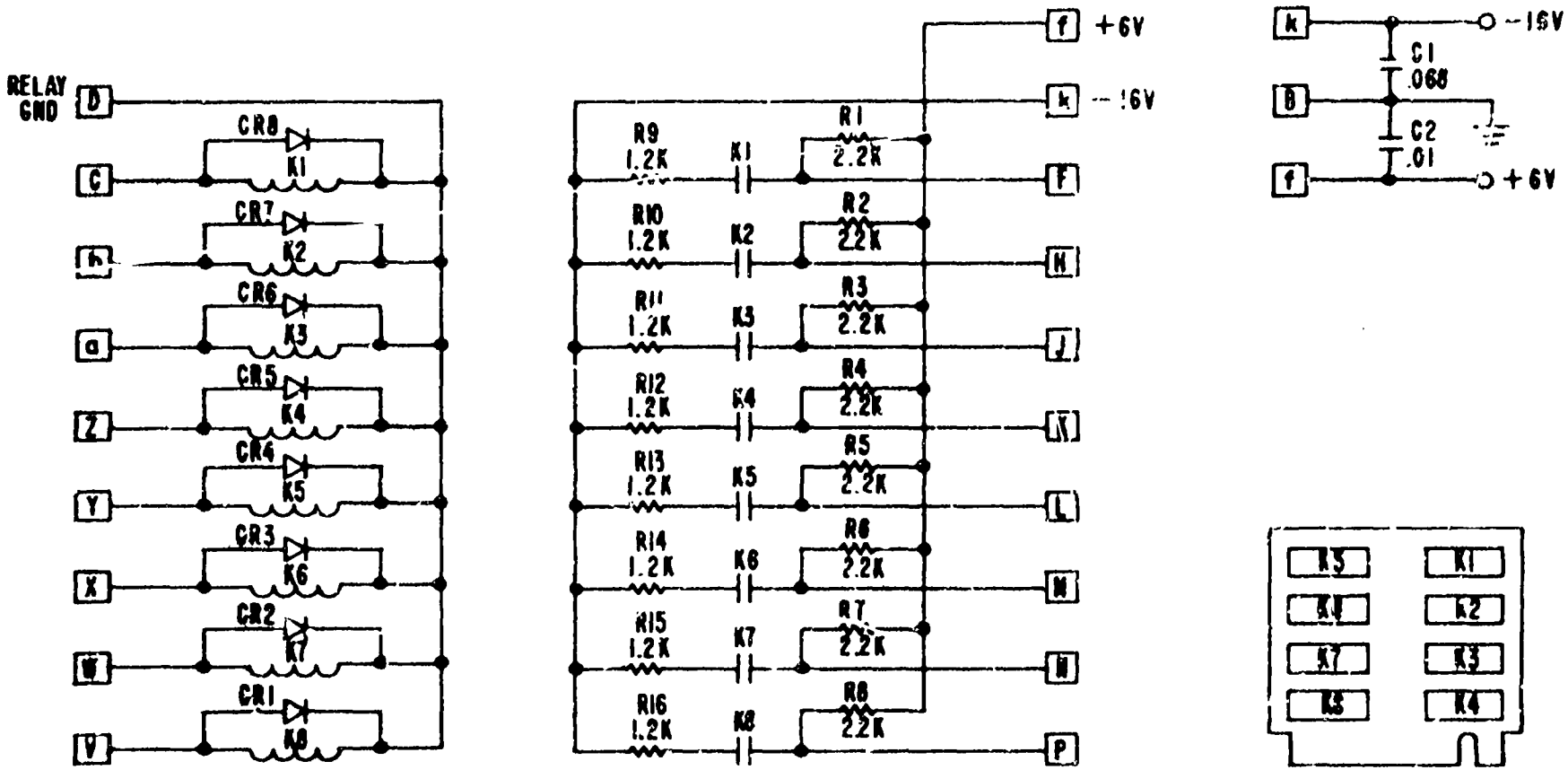


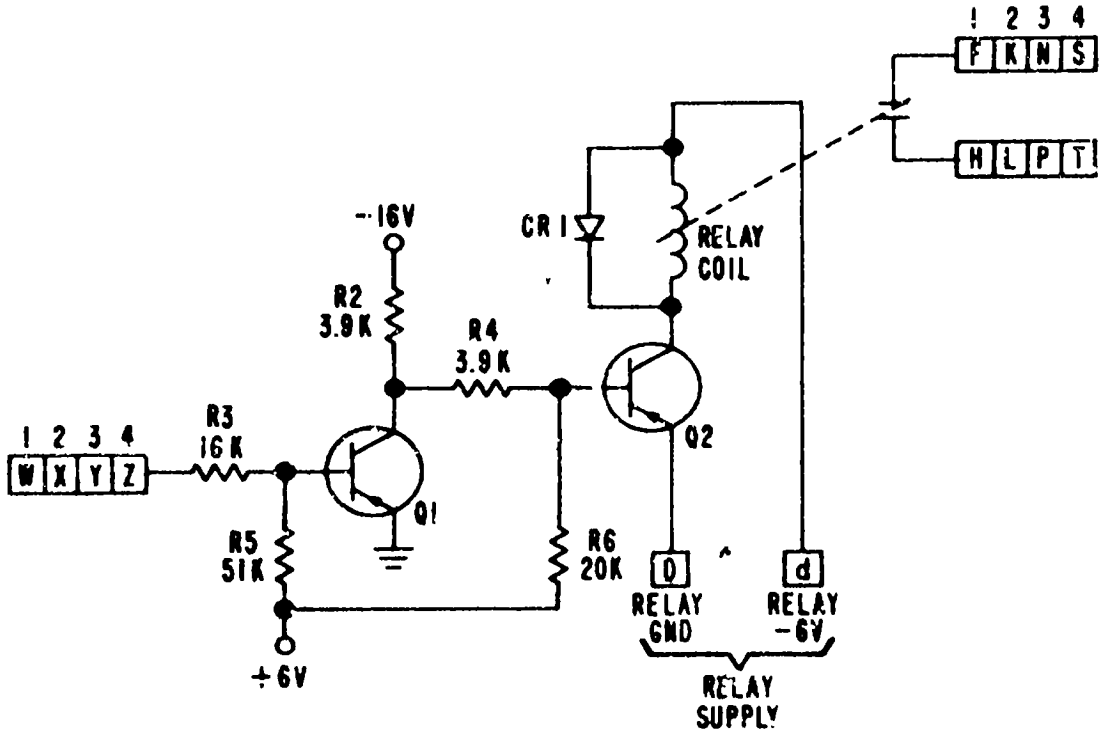
Figure 15. Schematic Diagram JPL-1 Amplifier Section

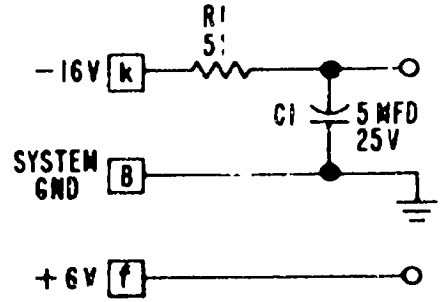


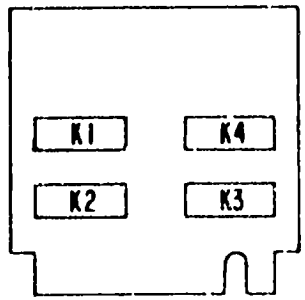
NOTES:

1. ALL RESISTORS 1/2 W, 5%
2. ALL DIODES S1011
3. ALL RELAYS STRUTHERS-DUNN TYPE MRR-1A 6VDC 288 OHM

Figure 16. Schematic Diagram SRI-8A



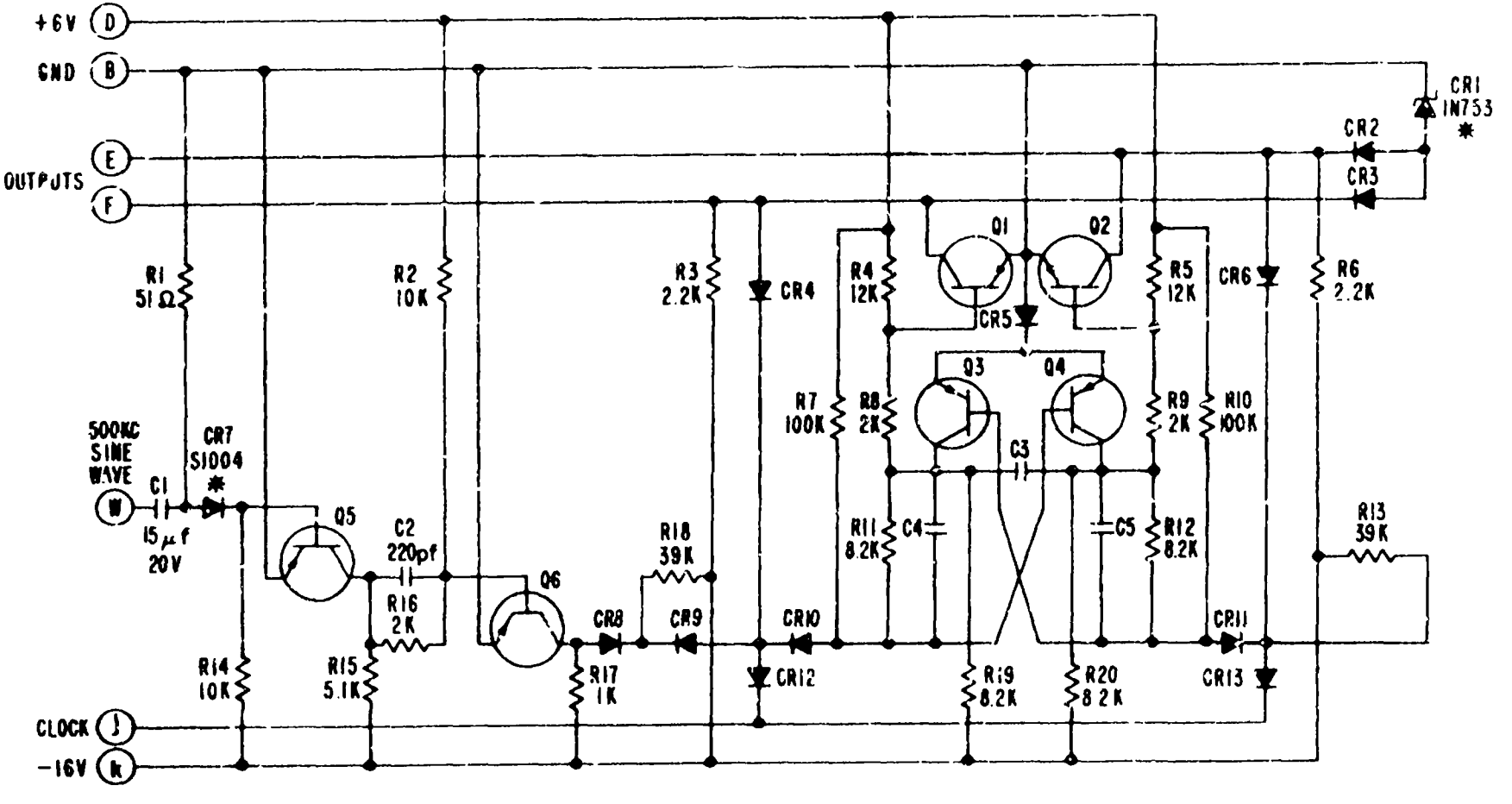




NOTES:

1. ALL RESISTORS 1/2W, 5%
2. ALL DIODES S1011
3. ALL TRANSISTORS S1007
4. ALL RELAYS STRUTHERS-DUNN MRR-1A, 6VDC, 288 OHM

Figure 17. Schematic Diagram SRO-4



NOTES:

1. ALL TRANSISTORS 2N1499A
2. ALL DIODES SI0N EXCEPT AS NOTED *
3. ALL CAPACITORS 62 μμf EXCEPT AS NOTED
4. ALL RESISTORS 1/2 W 5%

Figure 18. Schematic Diagram of CSO 1

APPENDIX D
WIRING CHARTS

The digital portion of the ranging system is made up primarily of individual T-Pac units which have been grouped into 10 modular assemblies. These have been designated, according to their function as the Program Unit, Acquisition Units 1 and 2, Transmitter Coder, Receiver Coders 1 and 2, Number Generator, Timer, Range Tally, and Readout Register. Each modular assembly is composed of one T bloc chassis and either two or four DUI terminal blocks attached to its sides.* The T bloc is the basic building block of the T-Pac system. It contains enough slots and connectors for 32 individual T-Pac cards. All connections between cards are made on a taper pin plug board located on the front panel. The DUI terminal block contains 20 slots. Each slot is composed of three internally connected taper pin inserts. It is the connecting link (for all non-relay type signals) between the T blocs and the rest of the system. The block derives its name from the convention used in its wiring. All wires between it and a T bloc located below come from the outside terminal which is designated as down (or D). All wires between it and a T bloc located above come from the middle terminal designated as up (or U). All wires between it and the T bloc itself are called in (or I). Hence the name of the block—DUI. The ten modular assemblies are contained in two subracks. All wires passing into and out of these subracks must pass through one of two terminal strips, located on top of each rack. Each of these blocks contain 60 independent sleeve type taper pin inserts. Connections are made by taper pin insertion to both ends of the sleeve.

Each modular assembly is wired according to its own signal location chart, consisting of a grid on which the location of the appropriate input signals has been plotted. The assembly is completely wired when all the grid locations having the same signal designation have been interconnected. A sample chart given in Figure 19 will be used to illustrate the wiring conventions used to simplify the signal location charts. As can be seen, the chart is broken down into two major parts, namely the DUI and the T bloc sections.

Each DUI section contains seven columns. Taken in order, they are the subrack terminal designation; the in/out designation; the A, B, and C (or DUI) connections, the slot location; and the slot function columns. All signals passing out of the subrack must go through the subrack terminal strip. The first column

*The DUI blocks are attached so that slots #1 through 20 are on the right and #21 to 40 are on the left. If more slots are needed numbers 41 through 60 again go on the right and 61 through 80 go on the left.

gives the designation of the interconnection, although the final destination of the signal is given in the DUI columns. The second column locates the origin of the signal. A signal generated in the assembly is denoted by a dot (·); a signal generated outside of the assembly is designated by a plus (+). The A column shows the interconnection between the DUI block and the T Bloc. If the signal originates in the T bloc, the A column will show the source (i.e. it will designate the proper T-Pac output). If the signal originates outside of the T bloc, this space will be blank, although a connection must be made to the T bloc as will be explained later. The B column shows the terminating point of all wires leaving the modular assembly in an upward direction. The C column shows the terminal point of all wires leaving the modular assembly in a downward direction. The number designation column identifies the DUI slot and the slot function column defines the use or purpose. Since the A (or in) column must be closest to the T bloc, the A, B, C, and in/out columns are reversed for slots numbered 21 to 40 and 61 to 80 when the DUI bloc is on the left.

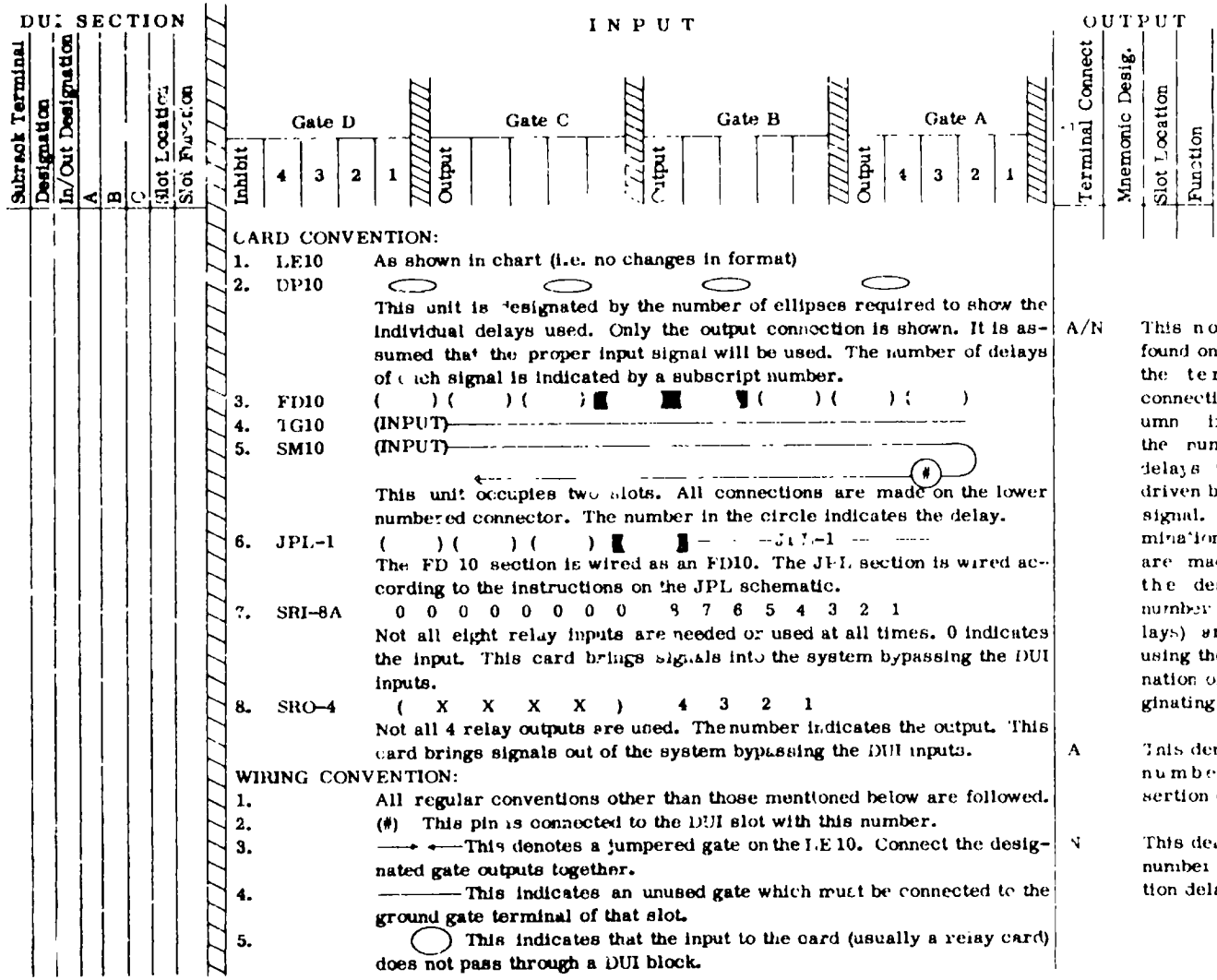
The T bloc part is divided into two major sections, namely the input and the output wiring charts. The format of the input section represents that of the customized front panel taper pin board.* Since most of the cards are LE 10's the columns are drawn to represent those input connections. When other cards are used, their input designation and their connections are superimposed across the columns. The convention used to identify these other cards is given on the sample chart. There are four wiring conventions which are used in this section to mate the design logic to the T-Pac requirements. The designation of these signals is also given on the sample chart.

The output section of the T bloc format is divided into four columns, namely the function, the slot number, the mnemonic designation, and the terminal connections. The first three are self explanatory. The last column (△) indicates that the output of the card is connected to a DP 10 delay line. This designation is supplied because proper T-Pac wiring requires that all cards feeding a delay line must be terminated after the delay. This column is also used to indicate the second mnemonic designation for an FD 10. This convention is not contradictory because the FD 10 which cannot be delayed, would never use this column.

Although each slot on the T bloc plug board should have an appropriate identification strip, this is not always the case. Some strips are not supplied; others which identify the custom designed units are not available. Each slot on the T bloc comes from the manufacturer with an LE 10 strip attached. The chart given

*The plugboard is made up of 32 taper pin blocks. Appropriate identification strips are attached to each block to define the proper connections for the card being used in that block.

T BLOC SECTION



CARD CONVENTION:

1. LE10 — As shown in chart (i.e. no changes in format)
2. DP10 — This unit is designated by the number of ellipses required to show the individual delays used. Only the output connection is shown. It is assumed that the proper input signal will be used. The number of delays of each signal is indicated by a subscript number.
3. FD10
4. TG10 (INPUT)
5. SM10 (INPUT) — This unit occupies two slots. All connections are made on the lower numbered connector. The number in the circle indicates the delay.
6. JPL-1 — The FD 10 section is wired as an FD10. The JPL section is wired according to the instructions on the JPL schematic.
7. SRI-8A — 0 0 0 0 0 0 0 0 8 7 6 5 4 3 2 1
   Not all eight relay inputs are needed or used at all times. 0 indicates the input. This card brings signals into the system bypassing the DUI inputs.
8. SRO-4 — (X X X X) 4 3 2 1
   Not all 4 relay outputs are used. The number indicates the output. This card brings signals out of the system bypassing the DUI inputs.

WIRING CONVENTION:

1. All regular conventions other than those mentioned below are followed.
2. (#) This pin is connected to the DUI slot with this number.
3. ——→ ←—— This denotes a jumpered gate on the LE 10. Connect the designated gate outputs together.
4. ———— This indicates an unused gate which must be connected to the ground gate terminal of that slot.
5. ◯ This indicates that the input to the card (usually a relay card) does not pass through a DUI block.

A/N — This notation found only under the terminal connection column indicates the number of delays that are driven by output signal. All terminations (which are made after the designated number of delays) are made using the termination of the originating card.

A — This denotes the number of assertion delays.

N — This denotes the number of negation delays.

Figure 19. Sample Wiring Chart

in Figure 20 gives the equivalent LE 1[illegible] position so that all other units can be wired properly.

The signal location chart for each of the ten modular assemblies is given in Drawings 16 to 25 inclusive.

MARK I — DIGITAL MODULES — PIN CONNECTIONS

	LE-10	DP-10	FD-10	TG-10	SM-10	JPL-1	SRI-8A	SRO-4	CS-01	
D	UG		UG	UG			Relay GND.		+6v.	D
E	1		A_o						A_o	E
F	2 A		B_o			a OUT	1	1a	B_o	F
H	3	1	1	IN			2	1b		H
J	4	(A)	2				3			J
K	A		3			a TRM	4 O	2a		K
L	1		4		n IN		5 U	2b		L
M	2 B		5			n TRM	6 T	O		M
N	3		6				7	3a U		N
P	4	(B)	7			AMPLIT.	8	3b T		P
R	B	1	1		n TRM	n OUT				R
S	1	2	2					4a		S
T	2 C		3					4b		T
U	3	1	1		n OUT	1				U
V	4	(C)	2			2	8			V
W	C		3			3	7	1	IN	W
X	1	1	1			1	6	2 I		X
Y	2 D	2	2			2	5 I	3 N		Y
Z	3	3	3			3	4 N	4		Z
a	4	(D)	4	a TRM		4	3			a
b	INH	5	5		a OUT	5	2			b
c	a OUT	6	6	a OUT		6	1			c
d	n	7	7	n		7				d
e	a TRM		C_o		a TRM	C_o				e
f	n		D_o			D_o	+6v.			f

Figure 20. Parallel display of T bloc pin connections for all cards used in digital portion of system.

APPENDIX E
CHINESE REMAINDER THEOREM

The pseudo-random code used by the Mark 1 ranging system is a boolean combination of four subcodes and a 2 bit clock. The chinese remainder theorem* is a mathematical tool which is used to determine the overall code shift caused by a one bit shift of one of the subcodes. The theorem states that if m_1 m_2 m_3 ..... m_k are given moduli, relatively prime in pairs, then the system of linear congruences

$$x \equiv a_1 \bmod m_1$$

$$x \equiv a_2 \bmod m_2$$

$$\vdots$$

$$x \equiv a_i \bmod m_k$$

where. a_i are given remainders

has a unique solution modulo m, where $m = m_1\ m_2\ m_3 \ldots\ldots\ m_k$. If M_i is defined by requiring that $m_i\ M_i = m$, then since the m_i are relatively prime in pairs, it follows that $(m_i\ M_1) = 1$, and there exists an integer x_i such that $M_i\ x_i \equiv 1 \bmod m_i$ for $i = 1, 2, 3 \ldots\ldots$, k. Then a solution (x) of the given

*Definition of Terms:

Chinese Number:	A chinese number for a given subcode is that number in bits which the combined code is shifted for a one bit shift in the subcode.
Relatively Prime:	Two numbers are relatively prime if the greatest common divisor is unity.
Modulo:	This is the base of a number system being used. For example the decimal system is modulo 10.
Linear Congruence:	Two numbers are linearly congruent in a given number system under the following definition:

a ≡ b modulo m
if and only if a − b = k m where k is an integer.
This reads a is linearly congruent b modulo m.

system of congruences is given by

$$x = \sum_{i=1}^{k} M_i \; x_i \; a_i$$

For if x is substituted in any of the given congruences, say the ith congruence, then M_j for every $j \neq 1$, contains m_i as a factor, so that $M_j \equiv 0 \bmod m_i$, $j \neq 1$; but $M_i \; x_i \equiv 1 \bmod m_i$, hence $x \equiv a_i \bmod m_i$ as required.

The computation of the actual chinese numbers for the Mark 1 system is given below. The tabulation of the results is given in Table 2.

Short Code

$$M = m_X \; m_A \; m_B \; m_C \; m_{C!}$$

$$M = (11)\;(31)\;(7)\;(15)\;(2)$$

$$M = 71610 \text{ bits} = \text{modulo number}$$

and

$$M_x = \frac{M}{m_x} = 6510; \quad M_A = \frac{M}{m_A} = 2310; \quad M_B = \frac{M}{m_B} =$$

$$10230; \quad M_C = \frac{M}{m_c} = 477$$

Since by definition:

$$M_i \; x_i = 1 \bmod m_i = a \; x_i$$

then $$6510 \; x = a \; x = 1 \bmod 11 \text{ for the x code}$$

and $$a^* = -2$$

*To get a, simply divide $\frac{M_i}{m_i}$ and use the remainder, whether positive or negative.

so that $x = 5$

and $1 \bmod 11 = 32550$

Likewise:

$2310\ x = a\ x=1 \bmod 31$ for the A code

so that $a = 16$ and $x = 2$

and $1 \bmod 31 = \underline{4620};$

$10230\ x = a\ x = 1 \bmod 7$ for the B code

so that $a = 3$ and $x = 5$

and $1 \bmod 7 = \underline{51150};$

$4774\ x=a\ x=1 \bmod 15$ for the C code

so that $a=4$ and $x=4$

and $1 \bmod 15 = \underline{19096}$

Long code

$$M = m_X\ m_A\ m_B\ m_C\ m_{CL}$$

$$M = (11)\ (31)\ (63)\ (127)\ (2)$$

$M = 5{,}456{,}682$ bits = modulo number.

and

$$M_x = \frac{M}{m_x} = 496062;\ M_A = \frac{M}{m_A} = 176022;\ M_B = \frac{M}{m_B} =$$

$$86614;\ M_C = \frac{M}{m_c} = 42966$$

Again

$$M_i \; x_i = 1 \bmod m_i = a \; x_i$$

496062 x = a x = 1 mod 11 for the x code

so that a = 6 and x = 2 or 1 mod 11 = 992,124;

176022 x = a x = 1 mod 31 for the A code

so that a = 4 and x = 8 or 1 mod 31 = 1408176;

86614 x = ax = 1 mod 63 for the B code

so that a = 52 and x = 40 or 1 mod 63 = 3464560;

and finally, 42966 x = ax = 1 mod 127 for the C code

so that a = 40 and x = 54 or 1 mod 127 = 2320164

Table 2

LONG CODE

Sub-code Component	Length	Chinese # in bits	Chinese # in Range Units
X	11	992,124	142,865,856
A	31	1,408,176	202,777,344
B	63	3,464,560	498,896,640
C	127	2,320,164	334,103,616
M	(X) (A) (B) (C) (cl)	5,456,632	785,762,208
SHORT CODE			
Sub-code Component	Length	Chinese # in bits	Chinese # in Range Units
X	11	32,550	4,687,200
A	31	4,629	665,280
B	7	51,150	7,365,600
C	15	19,096	2,749,824
M	(X) (A) (B) (C) (cl)	71,610	10,311,840

Once acquisition is complete, the range to the spacecraft can be measured (for display purposes only) by determining the phase displacement between the transmitter and receiver coders. Since the receiver coder is driven by the received clock, the phase displacement of the codes reflects the actual current range to the spacecraft. The phase displacement is measured by starting a counter when the all 1's position occurs in the transmitter coder, and stopping the counter when the all 1's occurs in the receiver coder.

This method is also used to ascertain that a proper shifting of the subcodes occurs while in the manual check mode of operation. It should be noted, however, that only the subcodes are involved in this process. Therefore, the numbers which will be displayed on the counter for a one bit shift are not the same chinese numbers which are derived above for the code clock combination. In this case $m = m_X\ m_A\ m_B\ m_C$. The chinese numbers for this combination have been derived in a similar manner and are given below for convenience.

	Long Code	Short Code
X code	992,124	32,550
A code	1,408,176	4,620
B code	736,219	5,345
C code	2,320,164	19,096
Modulo number	2,728,341	35,805

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APPENDIX F
PROPERTIES OF PSEUDO-RANDOM CODES

The Mark 1 ranging subsystem measures range from the time delay encountered by a signal in its transmission to a satellite and return. The signal consists of an rf carrier, phase modulated by a coded waveform which belongs to a family of codes called pseudo-random sequences.

Pseudo-random sequences consist of a two level (binary) waveform, generated usually in a circulating shift register. These codes, while completely deterministic, possess certain unique properties which cause them to be extremely recognizable when perturbed or masked by noise. The most important of these is the so called "autocorrelation" function. The autocorrelation function of a signal represents its "signature" in time, i.e. the mark, or determining factor, which when comparing two signals tells whether the two are identical or different. Ideally, an autocorrelation function — that is, the correlation function of a received signal, and a synthesized replica of the transmitted signal would have a uniform low value when the two differ, and a single sharp peak, when the two are identical. In particular, binary correlation is defined as follows:

$$\text{Correlation} = \frac{\text{number of agreements} - \text{number of disagreements}}{\text{number of agreements} + \text{number of disagreements}}$$

This means that when two binary signals are compared on a bit by bit basis, their levels will either agree, or disagree, and the correlation represents the relative level of agreement. Stated mathematically,

$$C = \frac{A - D}{A + D}$$

where: C = correlation factor
A = number of agreements
D = number of disagreements

If two pseudo-random sequences, identical except for a time difference (or bit shift) are compared according to the rule that a one is generated whenever a bit of the original and a bit of the shifted sequence are different (exclusive- or , or mod - 2 addition, signified by $\oplus$), the result will always be the same code. (see reference 1 for a complete example). Since a pseudo-random sequence always has a distribution of 1's and 0's such that there is one more 1 than 0, such a correlation will be:

$$C = 1/N$$

where N = number of bits in the sequence.

On the other hand, when the codes agree, the correlation will be:

$$C = N/N = 1.$$

Therefore the autocorrelation function of a pseudo-random sequence (for reasonably long codes) is essentially zero when the code is not matched and unity when the code is matched.

The "acquisition" of such a code sequence is defined as the process of comparing a received sequence with a locally generated replica and shifting the local reference one bit at a time until the two are determined to be in synchronism. Obviously to acquire a sequence it is necessary to observe and compare all possible states, or bit positions, for positive identification. A sequence of length P, may require P trials, or correlations, before acquisition is complete. However, it has been shown (see references), that the process can be shortened if a given sequence P can be represented as the product of several shorter subsequences P_1, P_2, P_3, ———P_n, subject to certain conditions. The length P of the sequence is equal to the product of the lengths P_1 ——— P_n of the subsequences, while the maximum number of trials needed to determine correlation is equal to the sum $P_1 + P_2 + P_3 +$ ——— P_n of the bit lengths of the individual subsequences. Since the product of the bit lengths is a far greater sum in general, than the sum of the individual subsequences, an obvious advantage is produced in acquisition time.

The conditions required for the above to be true are as follows:

1. The subsequence lengths must be relatively prime, i.e. they must not be evenly divisible by one another, or by any common denominator other than one.

2. All subsequences must belong to the family of codes having pseudo-random properties.

3. The subsequences must be combined in such a way that each individual subsequence can be acquired independent of the state of correlation of all the others.

Although the above discussion is admittedly somewhat heuristic, the stated requirements and results have been rigorously demonstrated in the literature. Further discussion is beyond the scope of this document, and the interested reader is referred to the references for further information.

APPENDIX G
CORRELATION MECHANICS

The degree of correlation which occurs during the subcode component acquisition can be calculated from the normalized correlation function. It can also be done graphically by means of a Karanaugh graph. This was done by P. L. LINDLEY of JPL. Because of the limited circulation of this memo, and the interest expressed in its contents, it is included here as part of this summary of the ranging subsystem.

CODE COMPONENTS CORRELATION & ACQUISITION IN THE RANGING SUBSYSTEM MARK 1.

1. Introduction

This note has as its purpose to clarify the correlation operation used, in the Mark 1 Ranging Subsystem and the pertinent S band Radio Subsystems, to acquire the individual code components. In the first analysis, the actual lengths (in bits) of the individual code components will be ignored, i.e., no account will be taken of code component unbalance (%) due to the fact that the number of zeros and the number of ones differ by one.

Lower case letters designate the transmitter code components. They are x, a, b, c, and cl; all generated in the digital equipment. Upper case letters designate the receiver code components; they are X, A, B, and C, generated in the digital equipment, and CL generated in the rf equipment.

2. Acquisition Program States

The component cl is acquired in the R (Reset) program state by non-digital means, viz locking up the receiver clock loop. The components x, a, b, c are acquired in program states p3, p4, p5 and p6 respectively, by digital means. Program states p1, p2, and p7 does not directly serve the acquisition purpose.

3. Transmitter Code

The transmitter code is written, and re-written as follows:

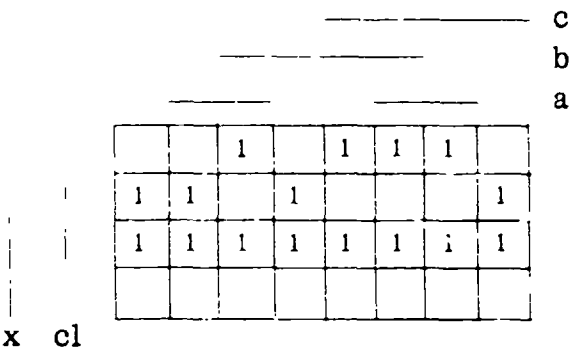
$$x\,cl + \bar{x}\left[(ab + bc + ac) \oplus cl\right]$$

$$= x\,cl + \bar{x}\left[(ab + bc + ac)\,\bar{cl} + (\bar{a}\,\bar{b} + \bar{b}\bar{c} + \bar{a}\bar{c})\,cl\right]$$

$$= cl\left[x + \bar{x}\,(\bar{a}\bar{b} + \bar{b}\bar{c} + \bar{a}\bar{c})\right] + \bar{cl}\left[\bar{x}(ab + bc + ac)\right]$$

$$= cl\left[x + \bar{a}\bar{b} + \bar{b}\bar{c} + \bar{a}\bar{c}\right] + \bar{cl}\left[\bar{x}ab + \bar{x}bc + \bar{x}ac\right]$$

This function can be plotted on a Karnaugh Map (Veitch chart) as shown below:



4. Receiver Code

The output of the (digital) receiver coder is often referred to as the receiver code. For the purpose of this note, we shall distinguish between the receiver coder output and the "full" receiver code; the latter is the result of combining the former with the CL component by the ⊕ operator.

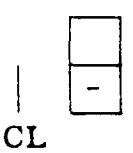
In the following we shall write down the full receiver code for each acquisition program state and plot it on an appropriate Karnaugh Map (For reasons which will appear later, we shall not use the arabic "one" (1), but rather the Chinese "one" (—).

Reset State Coder output = 0

Full code = $0 \oplus CL$

$= 0 \cdot \overline{CL} + 1 \cdot CL$

$= CL$

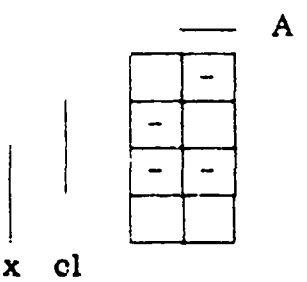


State p3 Coder output = $\overline{X}A$

Full code = $\overline{X}A \oplus CL$

$= \overline{X}A\overline{CL} + (X+\bar{A})CL$

$= CL\left[X + \overline{A}\right] + \overline{CL}\left[\overline{X}A\right]$



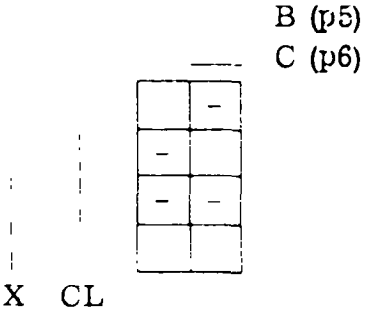
State p4

Same as state p3.

State p5 Coder output = $\overline{X}B$

Full code = $\overline{X}B \oplus CL$

$= CL\left[X + \overline{B}\right] + \overline{CL}\left[\overline{X}B\right]$



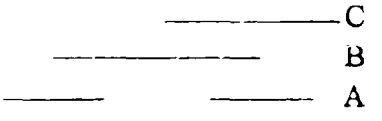
State p6 Coder output = $\overline{X}C$

Full code = $\overline{X}C \oplus CL$

$= CL\left[X + \overline{C}\right] + \overline{CL}\left[\overline{X}C\right]$

State p7 Coder output

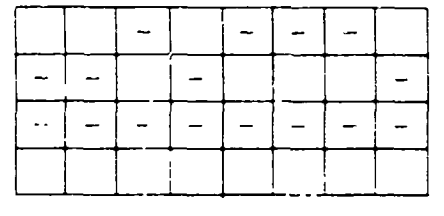
$= \overline{X}(AB + BC + AC)$



Full code = $\left[\overline{X}(AB + BC + AC)\right] \oplus CL$

$= \overline{X}(AB + BC + AC)\ \overline{CL}$

$+ \left[X + (\overline{A} + \overline{B})(\overline{B} + \overline{C})(\overline{A} + \overline{C})\right] CL$



$= \overline{X}(AB + BC + AC)\ \overline{CL}$

$+ (X + \overline{A}\overline{B} + \overline{B}\overline{C} + \overline{A}\overline{C})\ CL$

$= CL\left[X + \overline{A}\overline{B} + \overline{B}\overline{C} + \overline{A}\overline{C}\right] + \overline{CL}\left[\overline{X}AB + \overline{X}BC + \overline{X}AC\right]$

which as can be seen, is the same as the transmitter code

5. Component Acquisition Basics

Since we are assuming balanced, random code components, each component of the transmitter code (or receiver code) is entirely independent of each other component of that code. Further, each unacquired component of the transmitter code is independent of each component of the receiver code and, of course, vice versa. In the Karnaugh Maps, which follow, then, transmitter and receiver code components are listed separately (the latter with a wavy row or column designator)

when the component is not acquired. They are collapsed into one (solid) designator when the component is acquired.

The percentage correlation is derived from the normalized correlation function and reads:

$$C = \frac{A - D}{A + D} \times 100\%$$

where: A is the total number of agreements (i.e. true-true or false-false)

D is the total number of disagreements (i.e. true-false or false-true)

Since we use "1" for the transmitter code "true" and "____" for the receiver code true, we can readily spot and count agreements by the super-position or absence of these symbols in the following charts. Obviously we can also count disagreements, indicated by "1" (transmitter code true, receiver code false) or "_____" (receiver code true, transmitter code false).

The following charts have been thus prepared from the information (functions) developed in sections 3 and 4 and using the above conventions.

6. Determination of Correlation

a) Reset State, no clock lock (initial) ———— c

Full receiver code = CL ——— b

Agreements (A) = 32 ——— a

Disagreements (D) = 32

$$C = \frac{A - D}{A + D} = \frac{32 - 32}{64} = 0\%$$

				1	1	1	
1	1		1				1
1	1	1	1	1	1	1	1
–	–	–	–	–	–	–	–
+	+	+	+	+	+	+	+
+	+	–	+	–	–	–	+
–	–	+	–	+	+	+	–

CL x cl

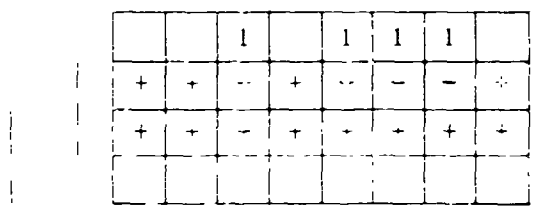
b) Reset State, clock lock (final) ——————— c

Full receiver code = CL ——————— b

A = 24 ——— ——— a

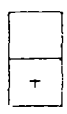
D = 8

$$C = \frac{24 - 8}{24 + 8} = \frac{16}{32} = 50\%$$



x cl
CL

Note: An operational check of the Subsystem if often made at this point, switching the (transmitter) code switch from "CODE" to "CLOCK". The transmitter code is then cl, the (full) receiver code is CL. Then A = 2, D = 0 and



cl,
CL

Correlation = 100%

c) State p3, x and a not acquired (initial)

Full receiver code ~~~~~~~~~~~~~~~~~~~~ A

= CL(X + $\bar{A}$) + $\overline{CL}$($\bar{X}$A) ——————————— c

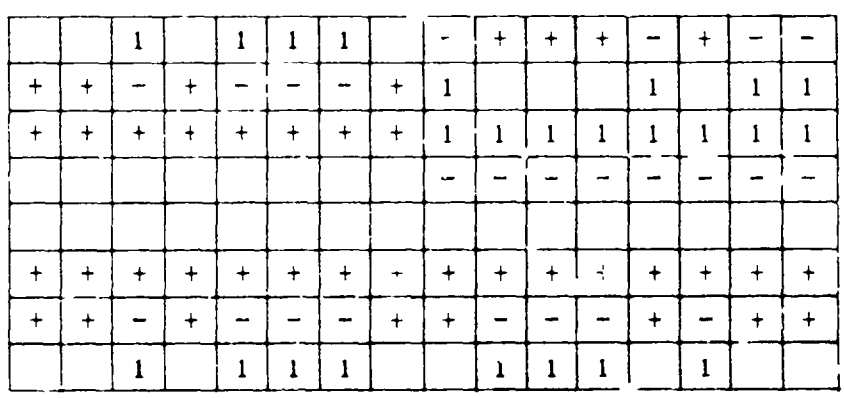
A = 80 ——————— ——————— b

D = 48 ——— ——— ——— ——— a

$$C = \frac{80 - 48}{80 + 48}$$

$$= \frac{32}{128}$$

= 25%



X x cl
CL

d) State p3, x acquired, a not acquired (final)

Full receiver code ——————————— A

= $CL(X + \overline{A}) + \overline{CL}(\overline{X}A)$ ——————————— c

——————— ——————— b

A = 48

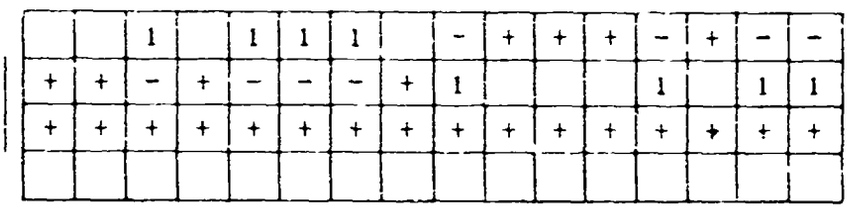
D = 16

——— ——— ——— ——— a

$$C = \frac{48 - 16}{48 + 16}$$

$$= \frac{32}{64}$$

$$= 50\%$$



x cl
X CL

---

e) State p4 (initial) is same as State p3 (final).

---

f) State p4, "a" acquired (final) ——————— c

Full receiver code = $CL(X + \overline{A}) + \overline{CL}(\overline{X}A)$ ——————— b

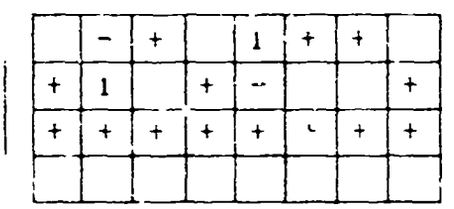
A = 28

D = 4

——— ——— a,A

$$C = \frac{28 - 4}{28 + 4}$$

$$= \frac{24}{32} = 75\%$$



x cl
X CL

---

g) State P 5, "b" not acquired (initial)

Full receiver code = $CL\ (X + \overline{B}) + \overline{CL}\ (\overline{X} \cdot B)$

Graph same as P 3 (final)

h) State p5, b acquired (final) Same as p4 (final)

---

i) State p6, c not acquired (initial)

Full receiver code = $CL(X + \overline{C}) + \overline{CL}(\overline{X}C)$ Same as p3 (final)

---

j) State p6, c acquired (final) Same as p4 (final)

---

k) State p7, all acquired.

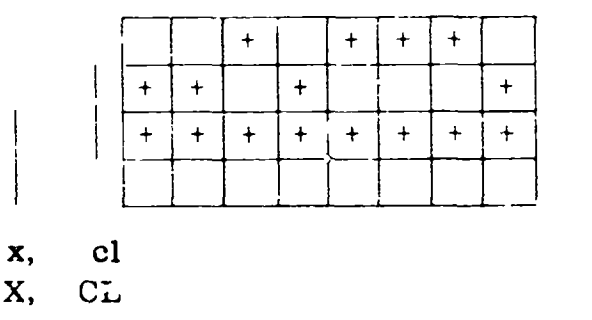
Full receiver code =

transmitter code

Hence A = 32

D = 0

C = 100%



Summary Tabulation

In the following tabulation are given both the idealized correlation values, as determined in Section 6, and the precise correlation values taking into account unbalance of code components as determined in Section 7.

PROGRAM STATE	RECEIVER CODER OUTPUT	COMPONENT BEING ACQUIRED	% CORRELATION	
			IDEALIZED INIT. FINAL	ACTUAL INIT. FINAL
Reset	0	cl	0 → 50	0 → 53
p1	0	-	50 → 50	53 → 53
p2	0	-	50 → 50	53 → 53
p3	$\overline{X}A$	x	25 → 50	28 → 54
p4	$\overline{X}A$	a	50 → 75	54 → 77.5
p5	$\overline{X}B$	b	50 → 75	54 → 77.5
p6	$\overline{X}C$	c	50 → 75	54 → 77.5
p7	$\overline{X}(AB+BC+AC)$	-	100 → 100	100 → 100

7. The Precise Correlation Determination

In the preceding discussion and evaluation, we had made the assumption (see introduction) that all code components are balanced, i.e., that there is an equal number of 1's and 0's in each, respectively. This is valid for the cl and CL, but not for the x, a, b, c, X, A, B, and C components, all of which have an odd number of bits, there being in each case one more 1 than there are 0's. Specifically,

x and X; total = 11 bits; probability of "1" = 6/11, probability of "0" = 5/11
a and A; total = 31 bits; probability of "1" = 16/31, probability of "0" = 15/31
b and B; total = 63 bits; probability of "1" = 32/63, probability of "0" = 31/63
c and C; total = 127 bits; probability of "1" = 64/127, probability of "0" = 63/127

To obtain the precise correlation, then, the squares in each Karnaugh Map must be weighed by the product of the row and column probabilities to obtain the squares own probability: This weight must be carried into the summations of the "agreement" and "disagreement" squares.

In the following analysis, direct reference is made in each case to the acquisition status and its pertinent Karnaugh Map in the correspondingly lettered sub-package of section 6.

It has been found easier to make the calculations in decimals, rather than fractions, of probability. Then,

x, X: p(o) = .91, p(1) = 1.09 a, A: p(o) = .97, p(1) = 1.03
b, B: p(o) = .98, p(1) = 1.02 c, C: p(o) = .99, p(1) = 1.01

a. In this Karnaugh Map the agreement and disagreement squares are equally balanced between the true and false fields of each of the components. Hence the question of relative probability does not arise.

$$\text{Correlation} = 0\%$$

b. In the Karnaugh Map for this case the upper two rows ($\bar{x}$) have p = 0.91, the lower two rows (x) have p = 1.09. The probabilities of the eight columns from left to right are: 0.94, 1.0, 1.04, 0.98, 1.0, 1.06, 1.02, 0.96.

The sum of agreement squares, each multiplied by the double probability of its weight (product of row and column) is 24.5; the sum of disagreements therefore is 7.5. Correlation then is

$$\frac{24.5 - 7.5}{24.5 + 7.5} = \frac{17}{32} = 53\%$$

Note: When the transmitter code at this point is changed to "clock" (cl), the correlation will be exactly 100%, since both clocks are balanced.

c. The probabilities for rows and columns are as follows:

Row 1 = .83	Column 1 = .91	Column 9 = .99
Row 2 = .83	Column 2 = .97	Column 10 = 1.05
Row 3 = .99	Column 3 = 1.01	Column 11 = 1.09
Row 4 = .99	Column 4 = .95	Column 12 = 1.03
Row 5 = 1.19	Column 5 = .97	Column 13 = 1.01
Row 6 = 1.19	Column 6 = 1.03	Column 14 = 1.07
Row 7 = .99	Column 7 = .99	Column 15 = 1.03
Row 8 = .99	Column 8 = .93	Column 16 = .97

The weighted agreements can then be found to add up to 82, the weighted disagreements add up to 46. Then the precise correlation at this point is

$$\frac{82 - 46}{82 + 46} = \frac{36}{128} = 28\%$$

d. The probabilities for the sixteen columns are the same as in c.

The probabilities for the four rows are 0.91, 0.91, 1.09, and 1.09. Then the sum of the weighted agreements is 49.4; the sum of the weighted disagreements is 14.6. The precise correlation is

$$\frac{49.4 - 14.6}{49.4 + 14.6} = \frac{34.8}{64} = 54\%$$

e. Same as d.

f. The row and column probabilities are:

Row 1 = .91	Column 1 = .94	Column 5 = 1.0
Row 2 = .91	Column 2 = 1.0	Column 6 = 1.06
Row 3 = 1.09	Column 3 = 1.04	Column 7 = 1.02
Row 4 = 1.09	Column 4 = .98	Column 8 = .96

Sum of weighted agreements are 28.4, disagreements are 3.6. The precise correlation is

$$\frac{28.4 - 3.6}{28.4 + 3.6} = \frac{24.8}{32} = 77.5\%$$

k. When all components are acquired of course we have a Karnaugh Map filled with agreement squares, so that unbalance of the components has no effect. Correlation = 100%.

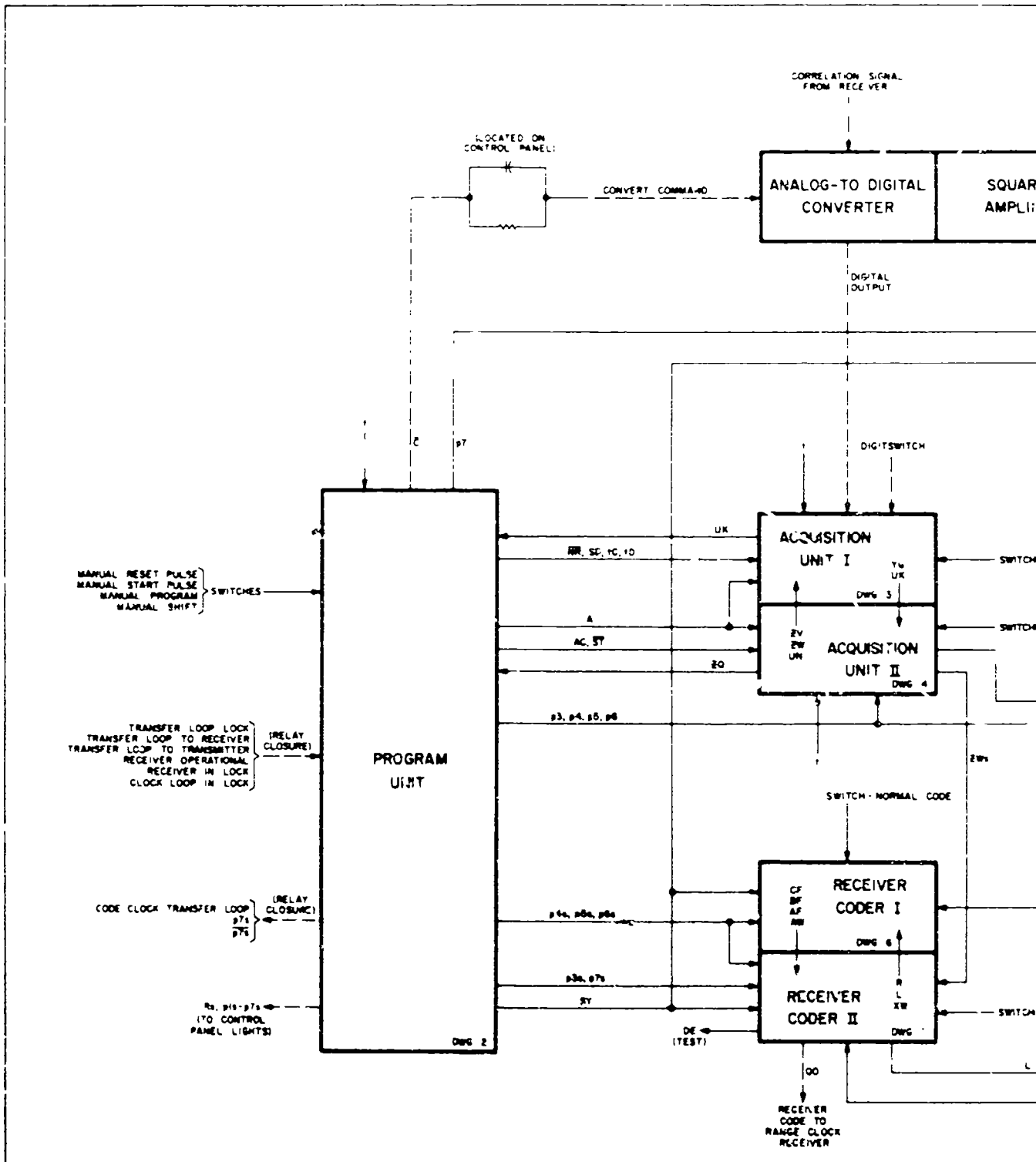
REFERENCES

1. "Pseudo-Random Binary Coded Waveforms," by M. P. Ristenbatt, U. of Michigan, Ann Arbor, Michigan.

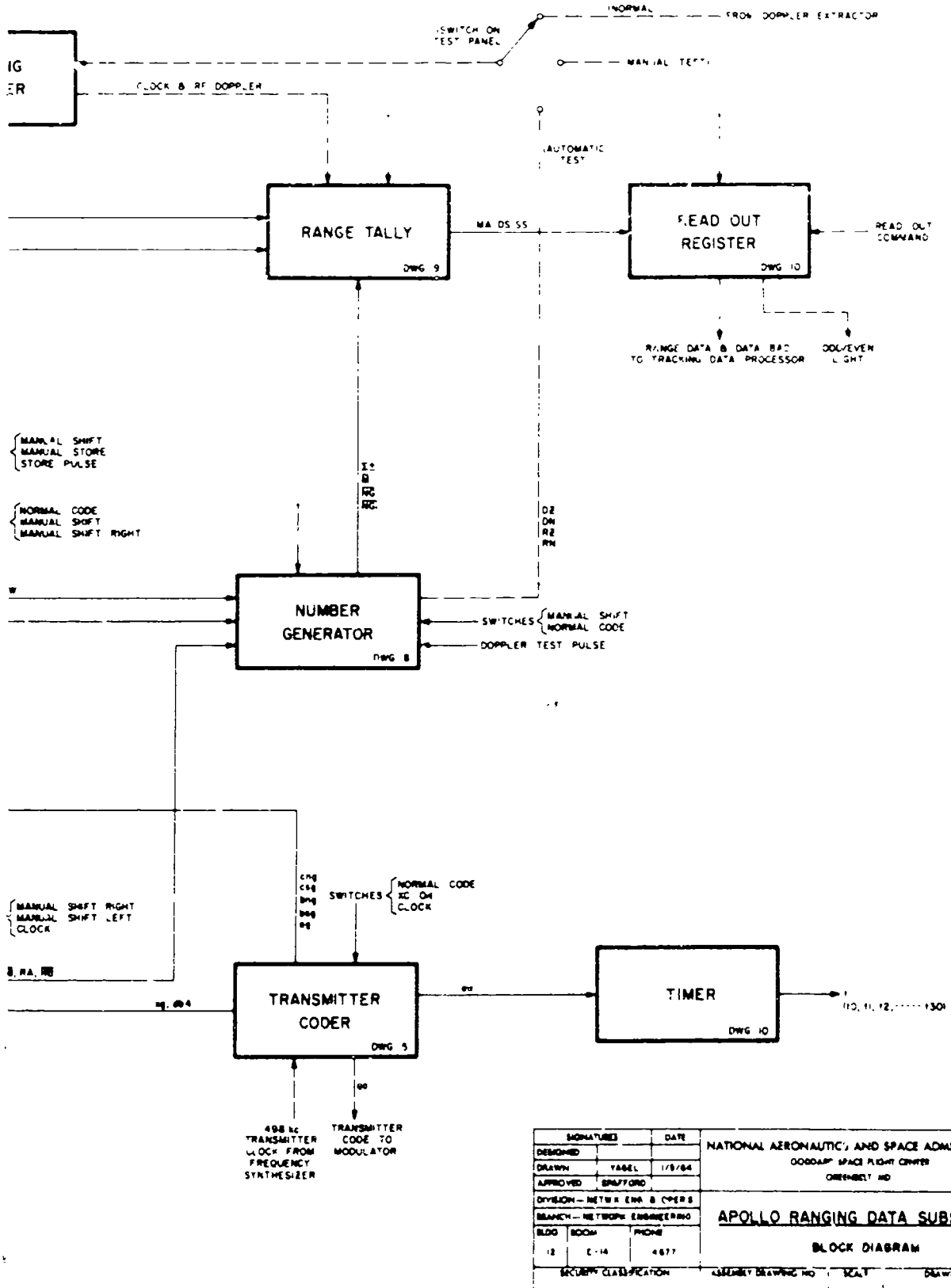
2. "A Hybrid Ranging System for Spacecraft," by R. T. Fitzgerald, P. Engels, H. Shaffer, E. Habib, and M. Mitchko, Goddard Space Flight Center Report X-521-64-71, Goddard Space Flight Center, Greenbelt, Md.

3. "Coding Theory and its Applications To Communications," by L. Baumert, M. Easterling, S. W. Golomb, and A. Viterbi, JPL T.R. 32-67.

4. Research Summaries 36-1 to 37-23 Jet Propulsion Laboratory.



NOTE
DOTTED LINES INDICATE EXTERNAL CONNECTIONS



SIGNATURES		DATE
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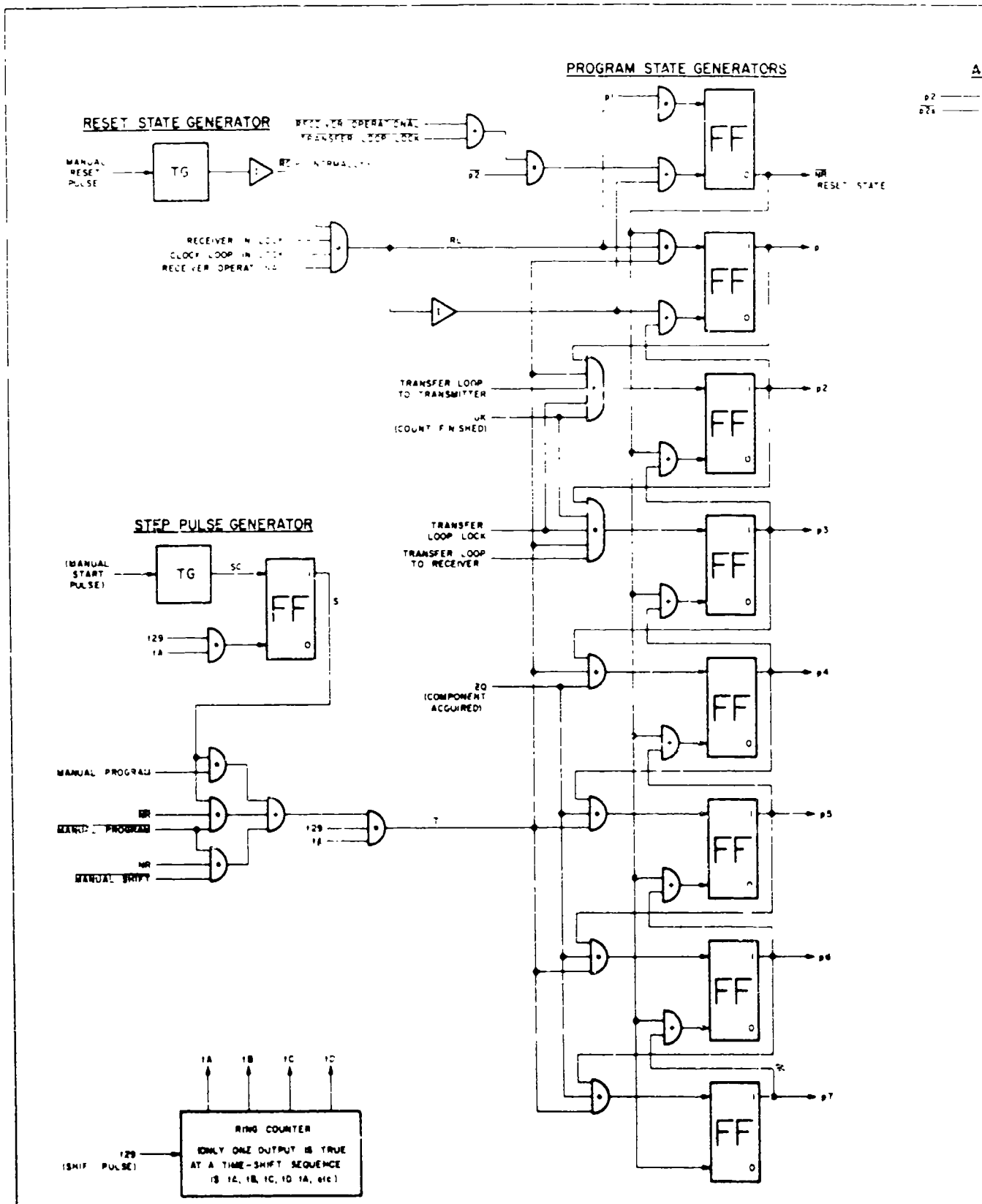
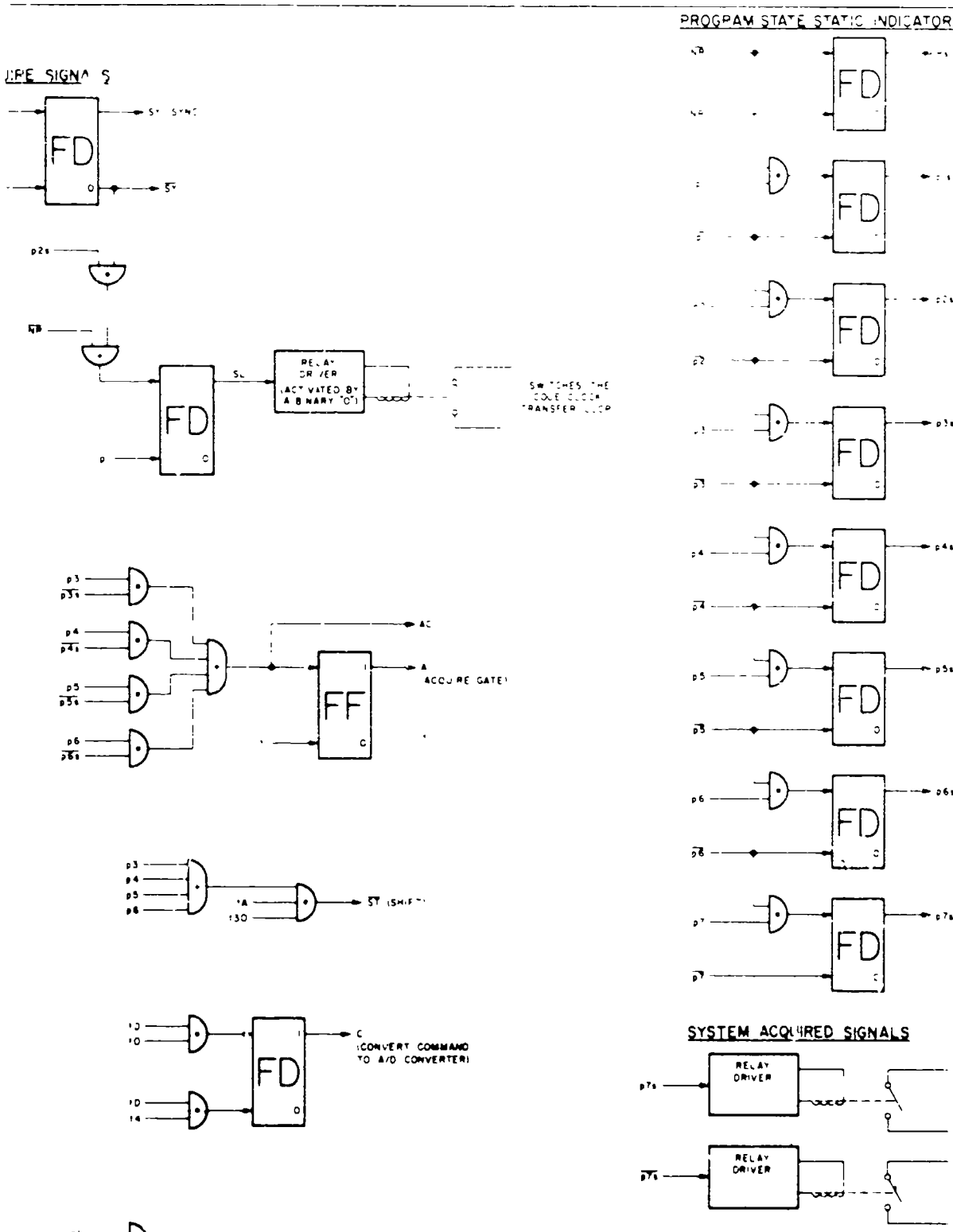
APOLLO RANGING DATA SUBSYSTEM

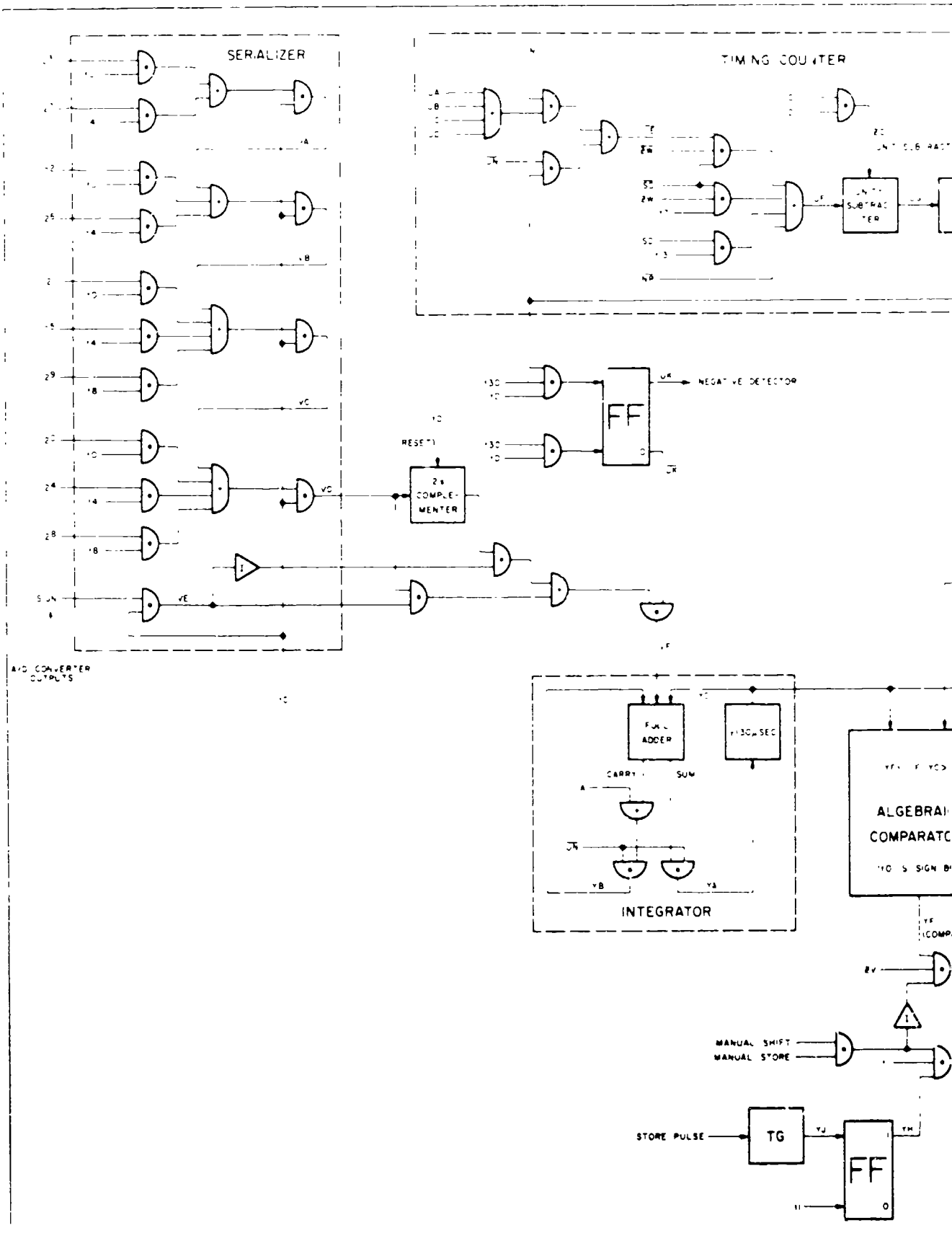
BLOCK DIAGRAM

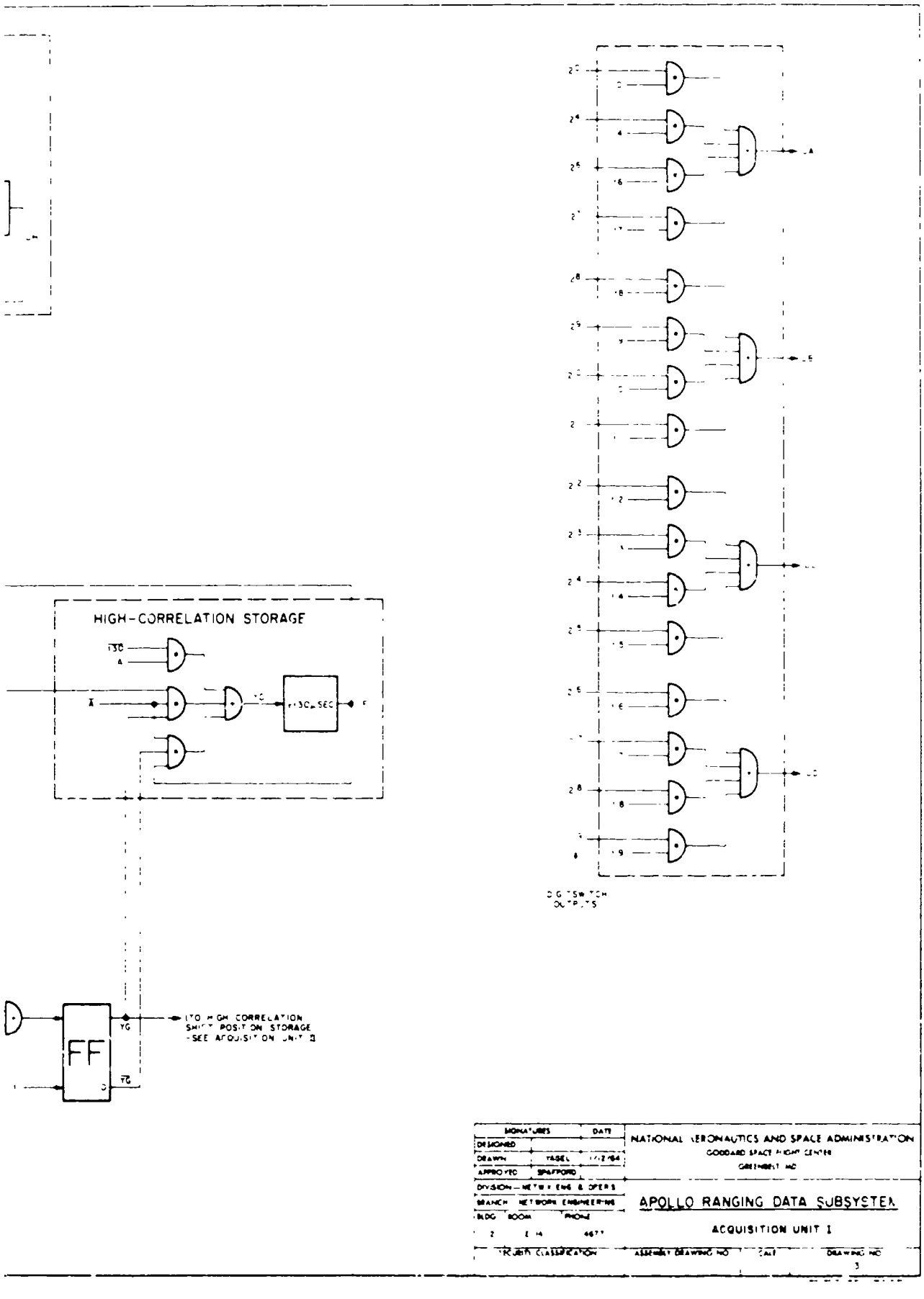
SECURITY CLASSIFICATION | ASSEMBLY DRAWING NO | SCALE | DRAWING NO

2


PROGRAM STATE GENERATORS
RESET STATE GENERATOR
MANUAL RESET PULSE
TG
RECEIVER OPERATIONAL
TRANSFER LOOP LOCK
p2
FF
RESET STATE
RECEIVER IN LOOP
CLOCK LOOP IN LOCK
RECEIVER OPERATIONAL
RL
p
TRANSFER LOOP TO TRANSMITTER
UK
(COUNT FINISHED)
p2
STEP PULSE GENERATOR
(MANUAL START PULSE)
TG
SC
FF
S
129
1A
TRANSFER LOOP LOCK
TRANSFER LOOP TO RECEIVER
p3
ZQ
(COMPONENT ACQUIRED)
p4
MANUAL PROGRAM
MR
MANUAL PROGRAM
MR
MANUAL SHIFT
129
1A
T
p5
p6
p7
1A
1B
1C
1D
RING COUNTER
(ONLY ONE OUTPUT IS TRUE AT A TIME-SHIFT SEQUENCE (S 1A, 1B, 1C, 1D, 1A, etc.)
129
(SHIFT PULSE)


PROGRAM STATE STATIC INDICATORS
SYSTEM ACQUIRED SIGNALS
RELAY DRIVER
RELAY DRIVER
FD
FF
(CONVERT COMMAND TO A/D CONVERTER)
(START DELAY)
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
APOLLO RANGING DATA SUBSYSTEM
PROGRAM UNIT


SERIALIZER
TIMING COUNTER
FF
NEGATIVE DETECTOR
RESET
2's COMPLEMENTER
A/D CONVERTER OUTPUTS
FULL ADDER
CARRY
SUM
INTEGRATOR
ALGEBRAIC COMPARATOR
MANUAL SHIFT
MANUAL STORE
STORE PULSE
TG
FF


HIGH-CORRELATION STORAGE
FF
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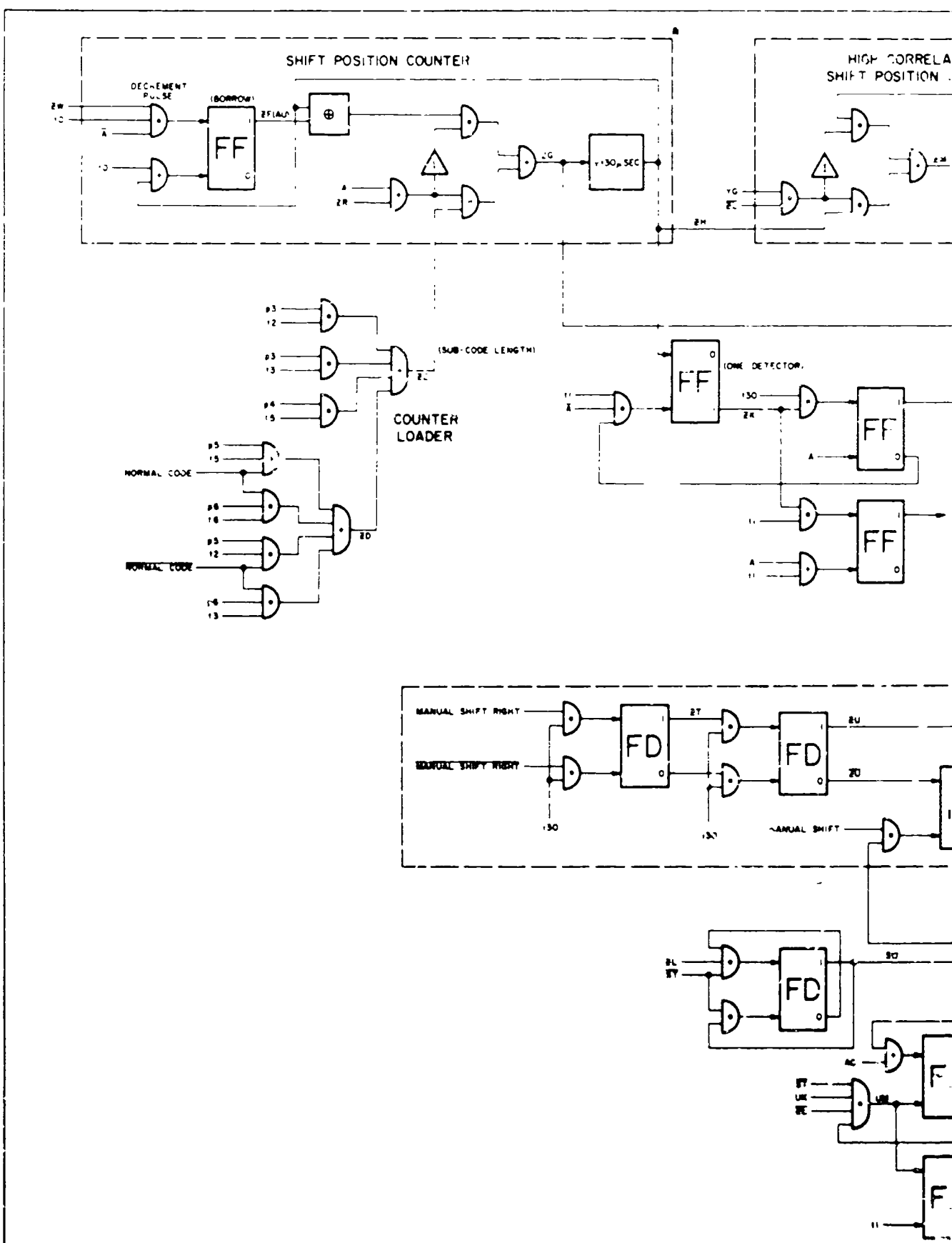
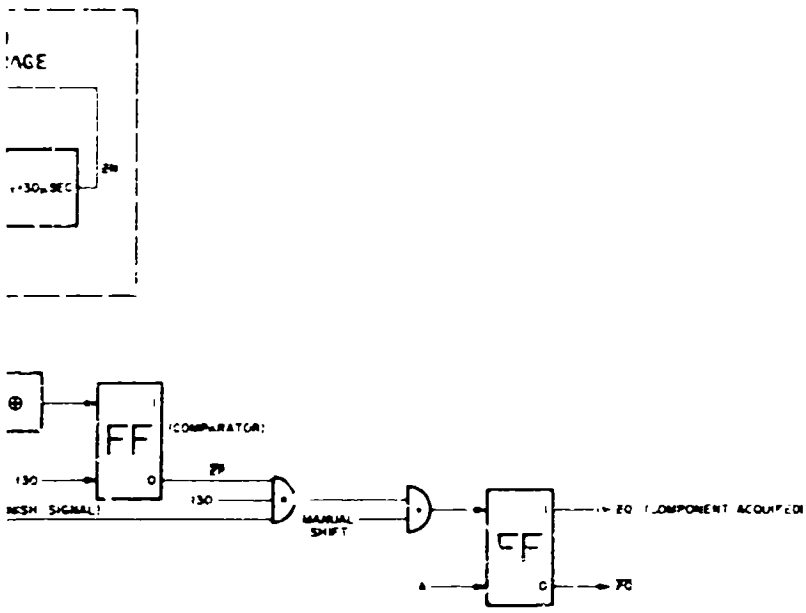
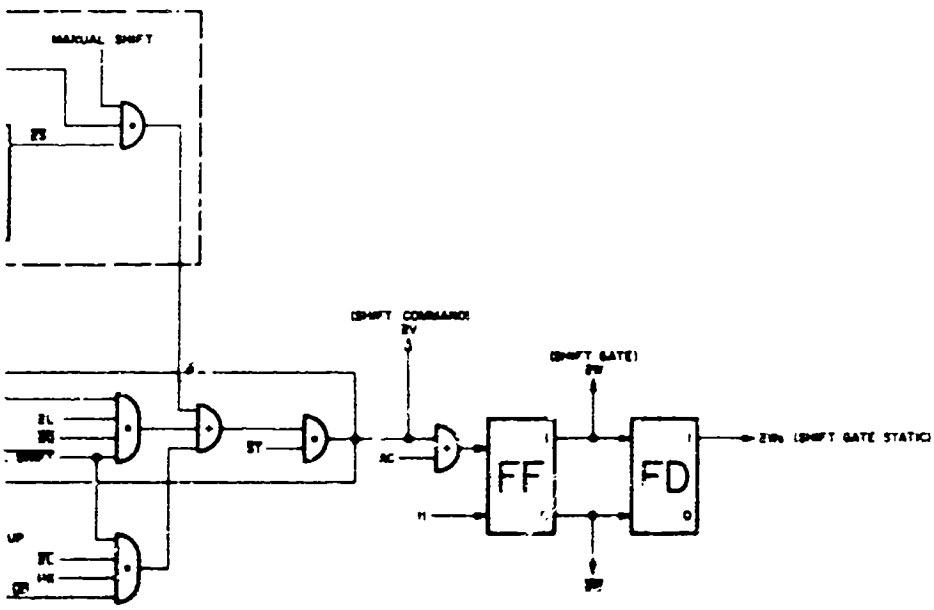
ACQUISITION UNIT I


SHIFT POSITION COUNTER
DECREMENT PULSE
(BORROW)
FF
COUNTER LOADER
(SUB-CODE LENGTH)
NORMAL CODE
NORMAL CODE
(ONE DETECTOR)
FF
FF
FF
MANUAL SHIFT RIGHT
FD
FD
FD
MANUAL SHIFT



LOAD SHIFT POSITION COUNTER)



			DATE
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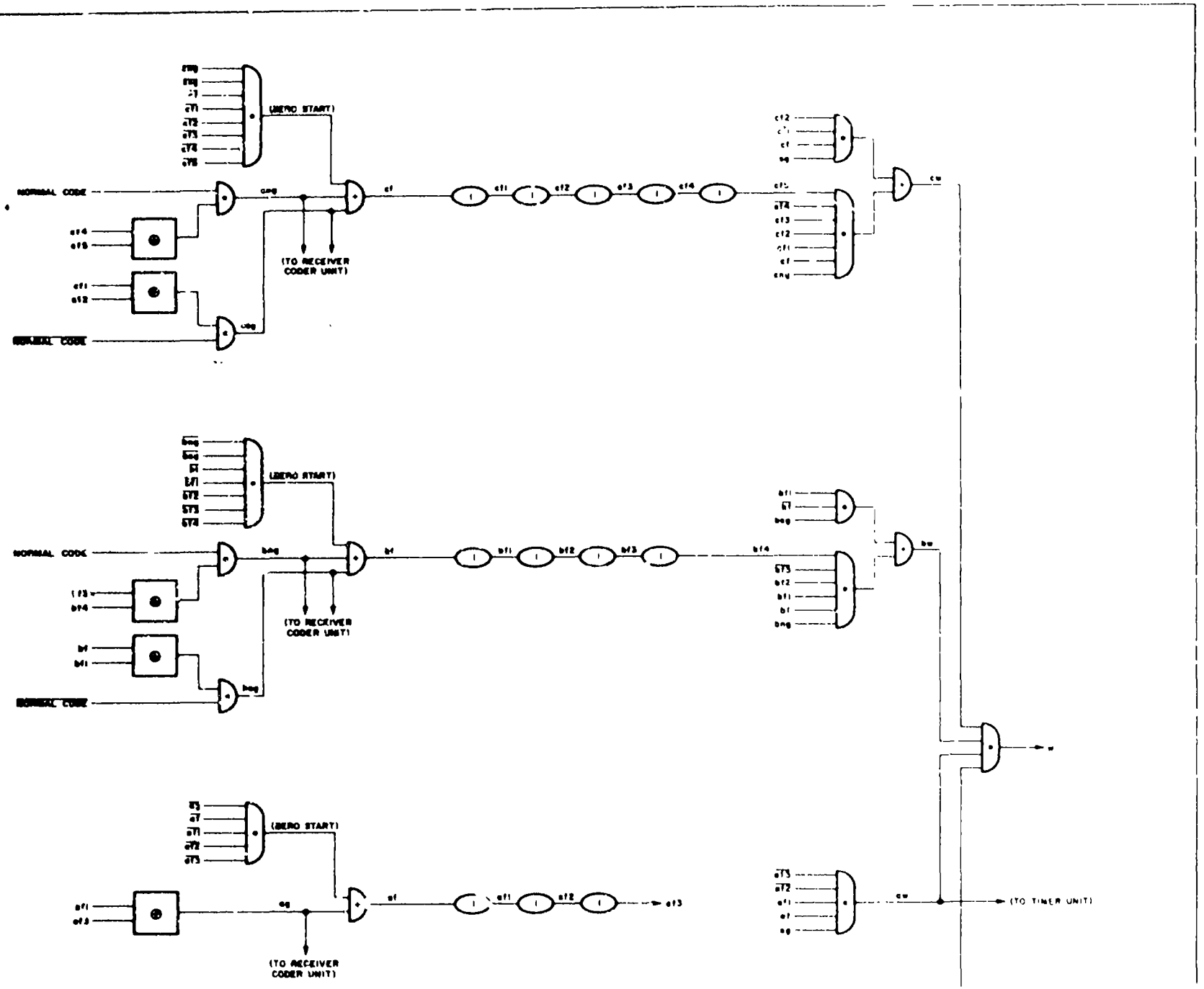
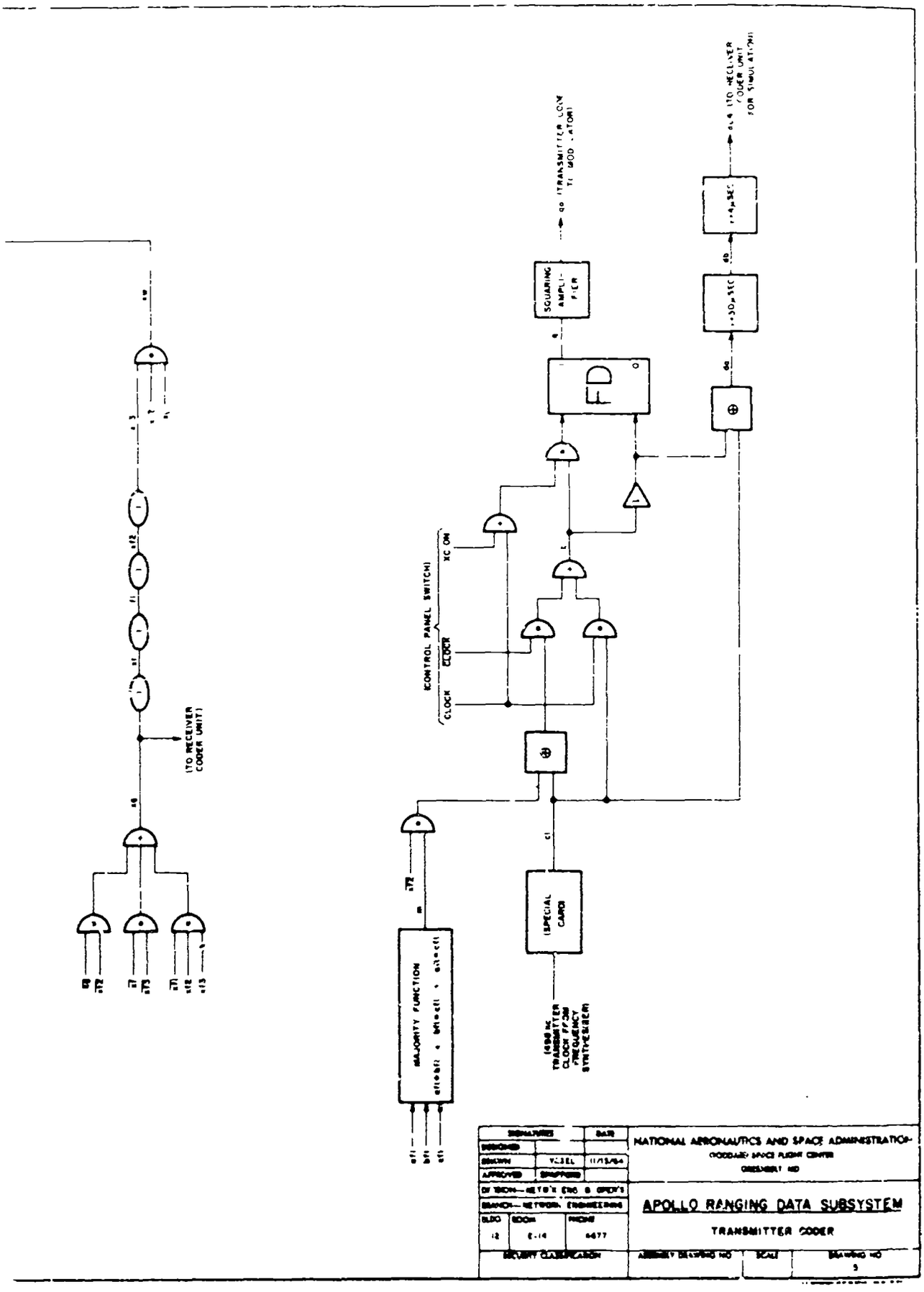
APOLLO RANGING DATA SUBSYSTEM

ACQUISITION UNIT II


(ZERO START)
NORMAL CODE
(TO RECEIVER CODER UNIT)
(ZERO START)
NORMAL CODE
(TO RECEIVER CODER UNIT)
(ZERO START)
(TO RECEIVER CODER UNIT)
(TO TIMER UNIT)


SQUARING AMPLI-FIER
FD
(SPECIAL CARD)
MAJORITY FUNCTION
CONTROL PANEL SWITCH)
XC ON
CLOCK
CLOCK
(TO RECEIVER CODER UNIT)
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
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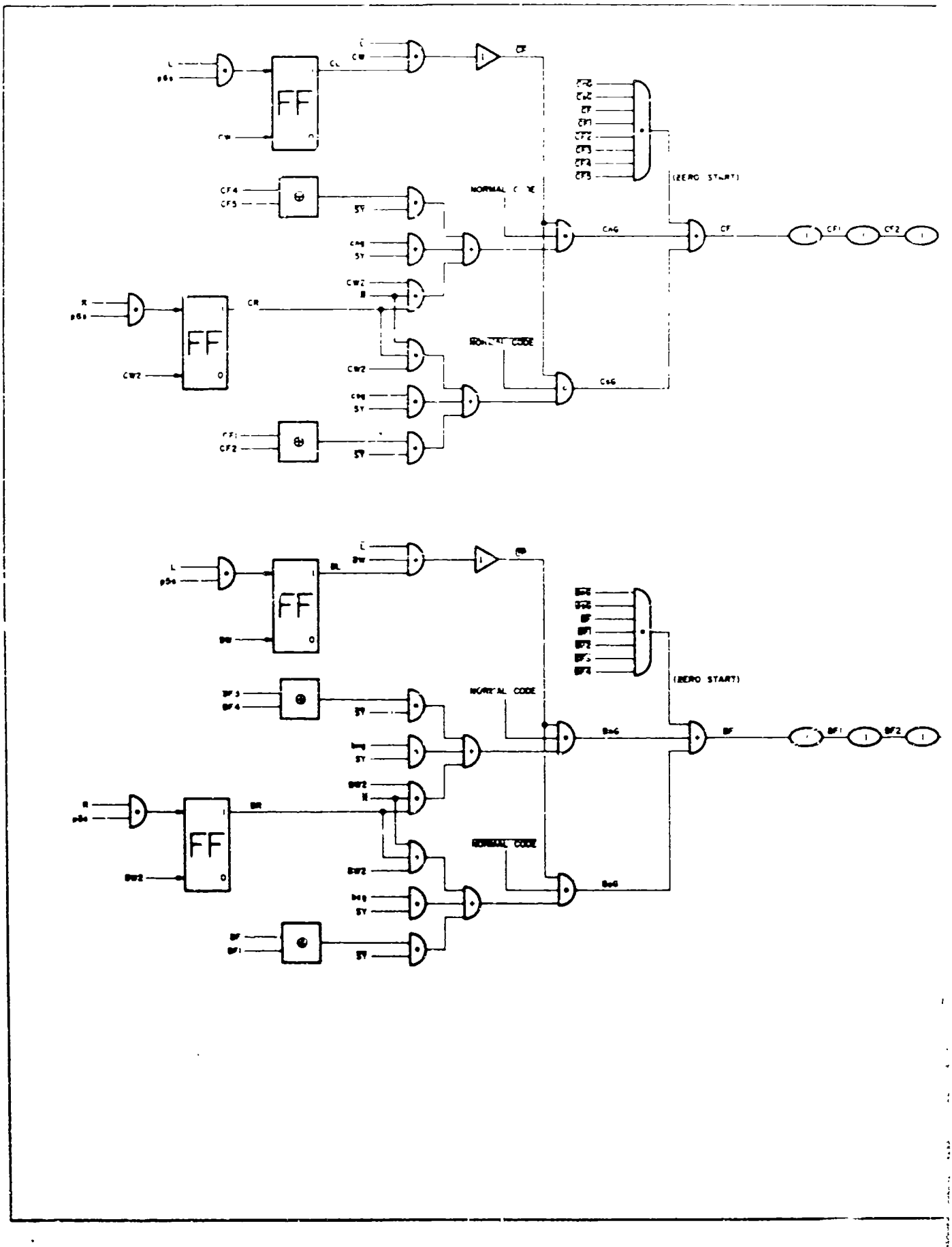
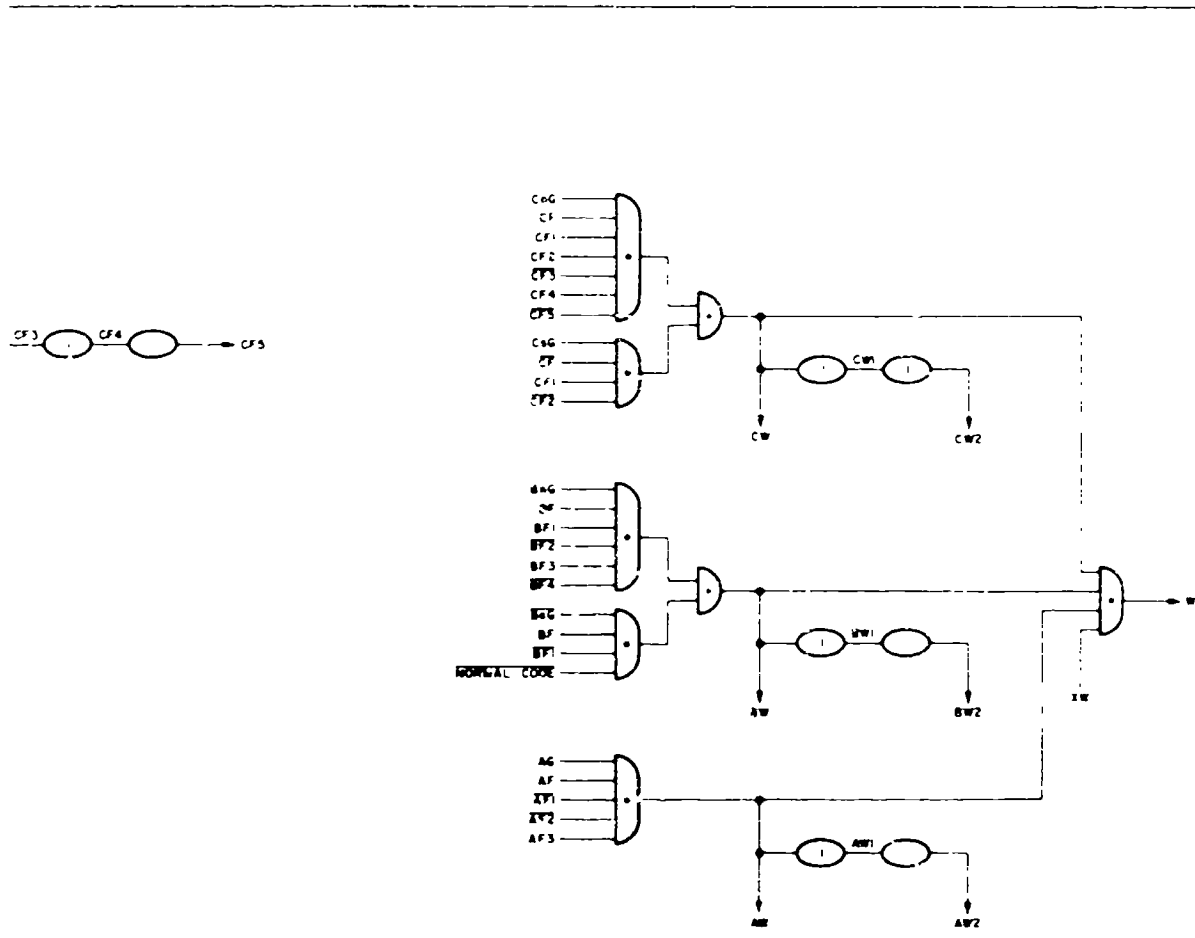
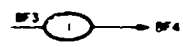
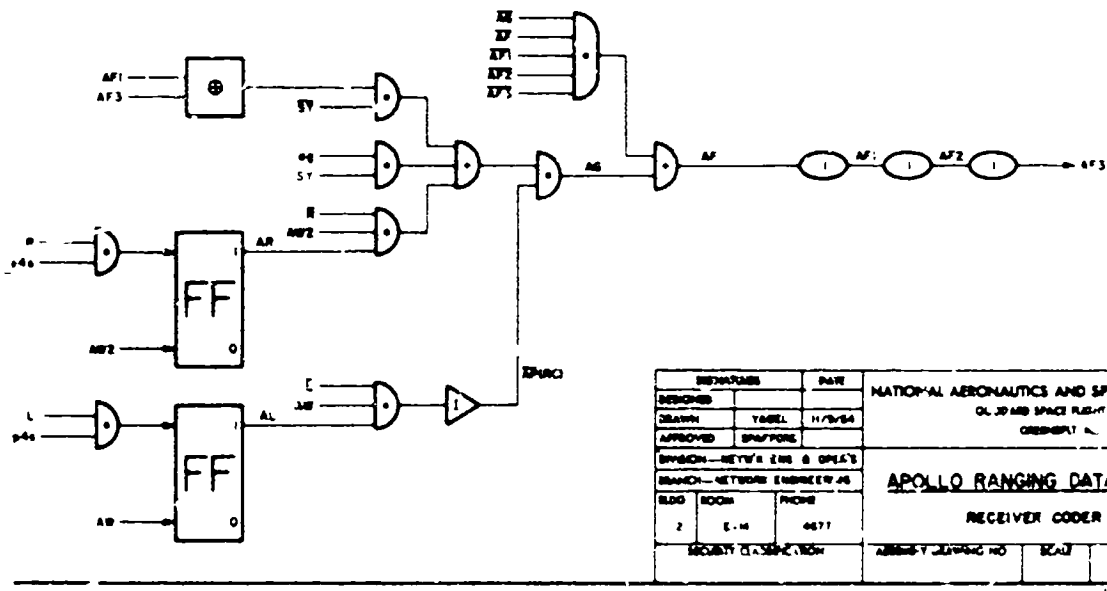
TRANSMITTER CODER

2


FF
FF
(ZERO START)
NORMAL CODE
(ZERO START)
NORMAL CODE







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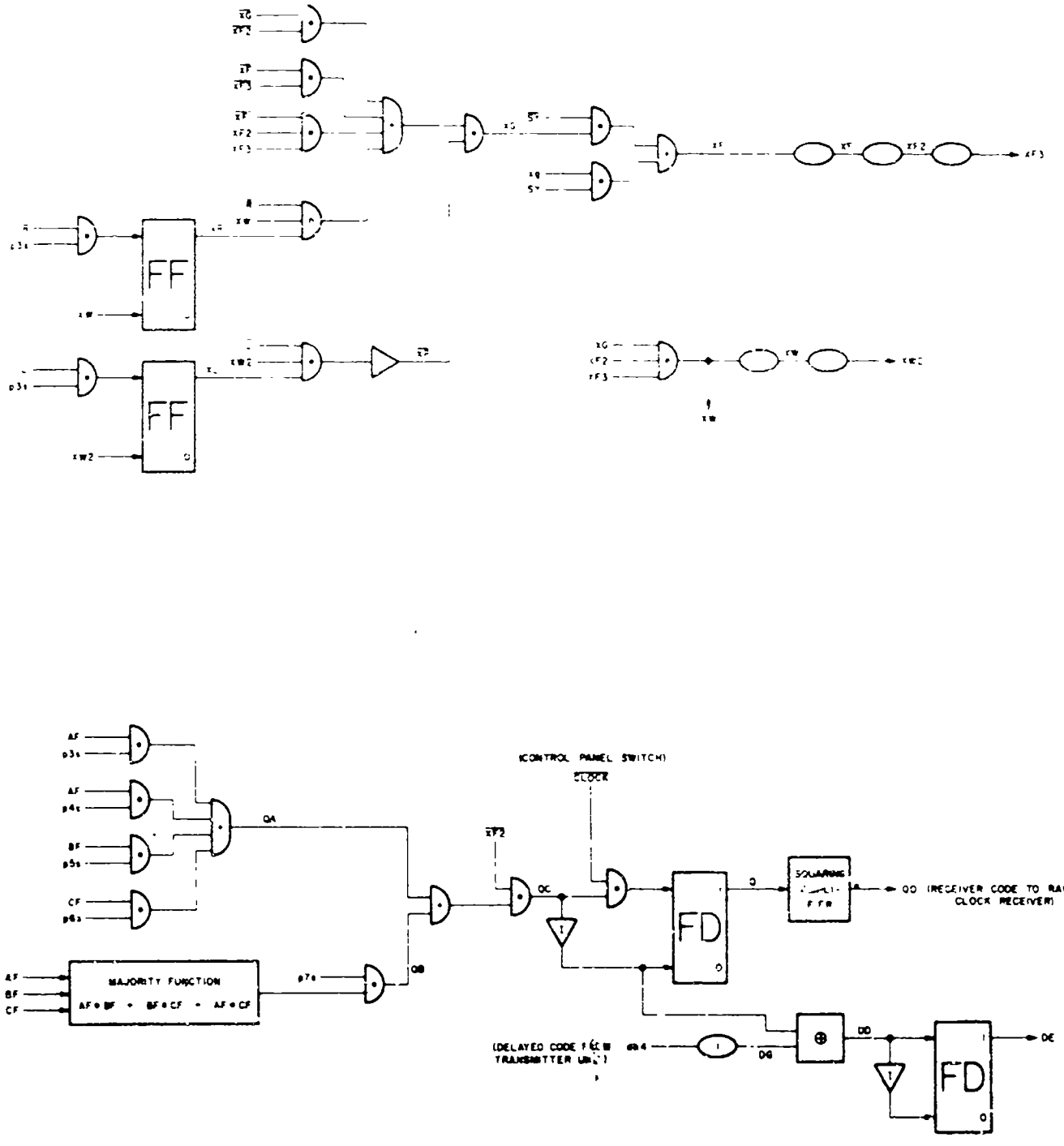
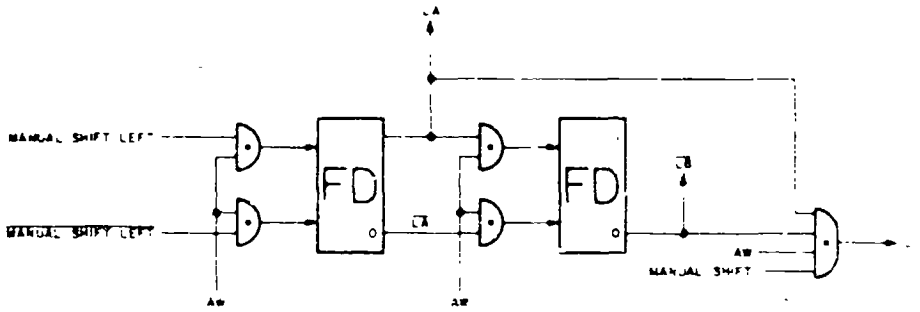
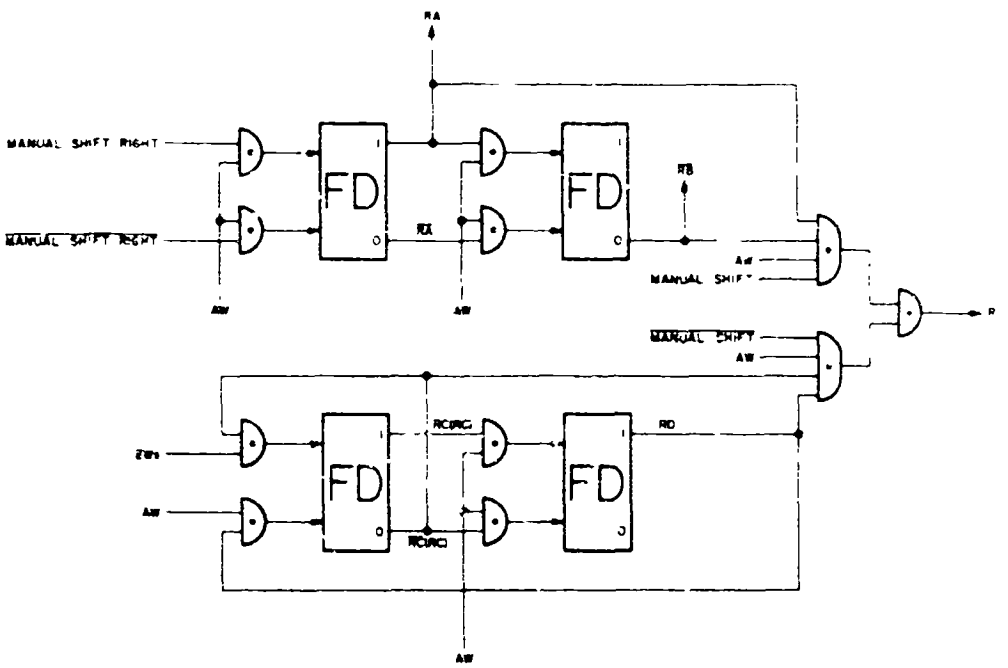
ASSEMBLY DRAWING NO | SCALE | DRAWING NO
A


FF
FF
(CONTROL PANEL SWITCH)
CLOCK
MAJORITY FUNCTION
FD
FD
SQUARING
(DELAYED CODE FROM TRANSMITTER UNIT)

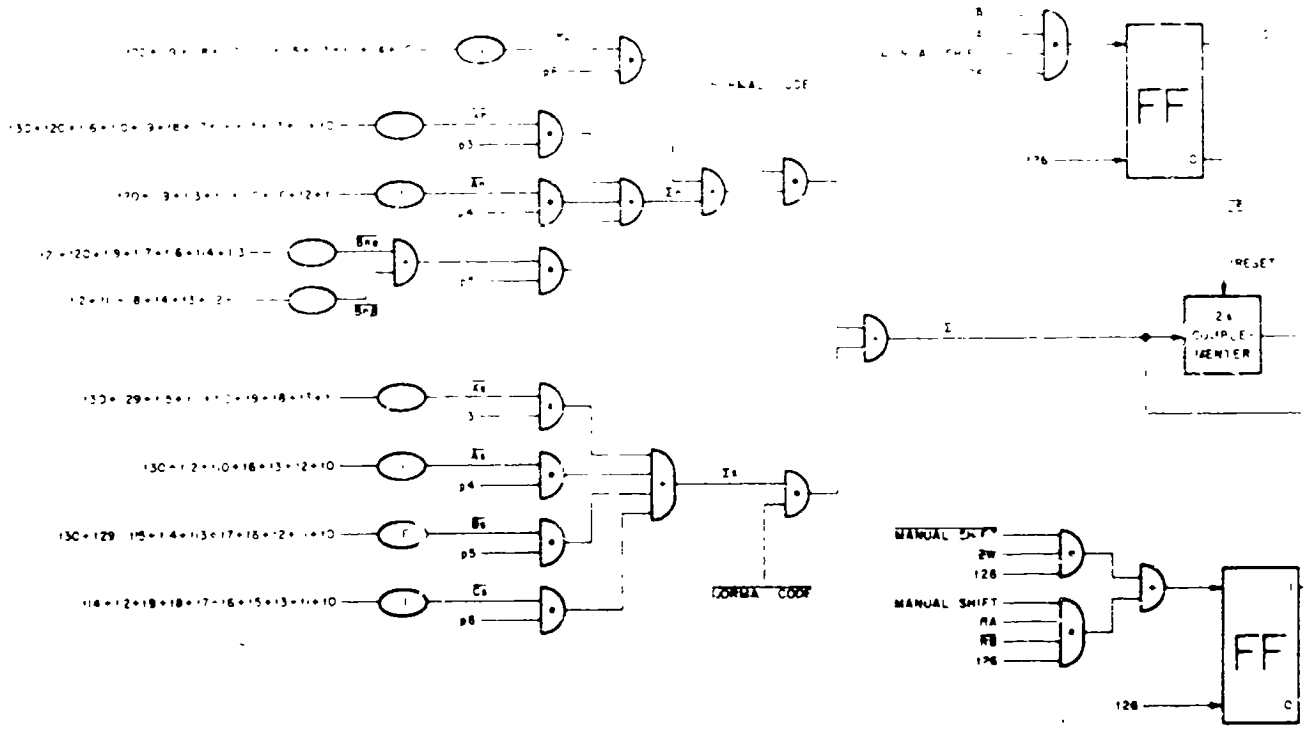




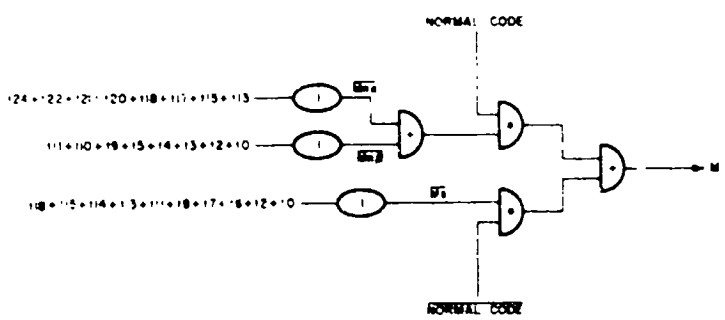
ORRELATION OUTPUT)

SIGNATURES		DATE	NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
DESIGNED			GODDARD SPACE FLIGHT CENTER
DRAWN	YAGEL	11/17/64	GREENBELT MD
APPROVED	BRAFFORD		
DIVISION— METEOR & ENVIR. SYSTEMS			APOLLO RANGING DATA SUBSYSTEM
BRANCH— NETWORK ENGINEERING			RECEIVER-CODER UNIT II
BLDG 12	ROOM E-14	PHONE 6677	
SECURITY CLASSIFICATION			ASSEMBLY DRAWING NO. / SCALE / DRAWING NO. 7

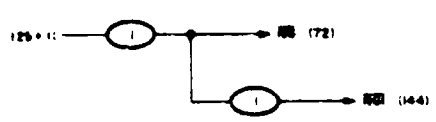
CHINESE NUMBER GENERATOR



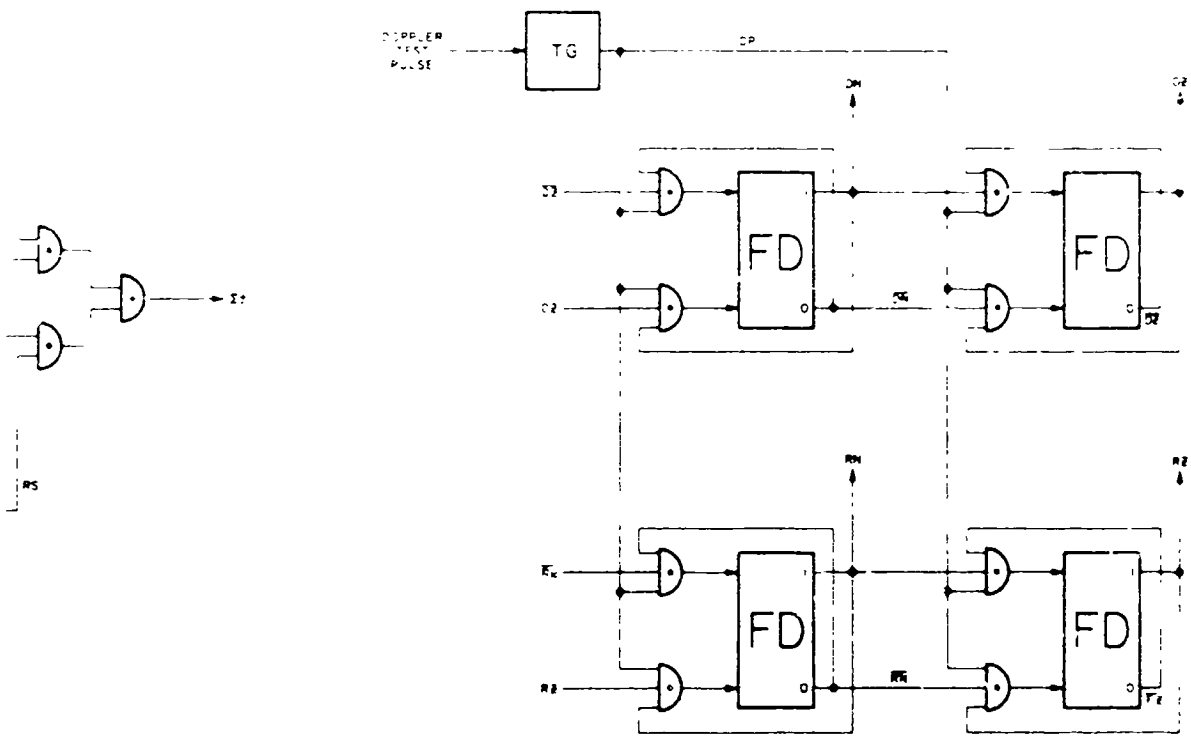
MODULO NUMBER GENERATOR



DOPPLER NUMBER GENERATOR



DOPPLER TEST GENERATOR



SIGNATURES		DATE
DESIGN		
DRAWN	YAGEL	11/2/64
APPROVED	SHAPPIRO	
DIVISION— NETW'K SYN & OPER'S		
BRANCH— NETWORK ENGINEERING		
BLDG 10	ROOM	PHONE 4-577
SECURITY CLASSIFICATION		

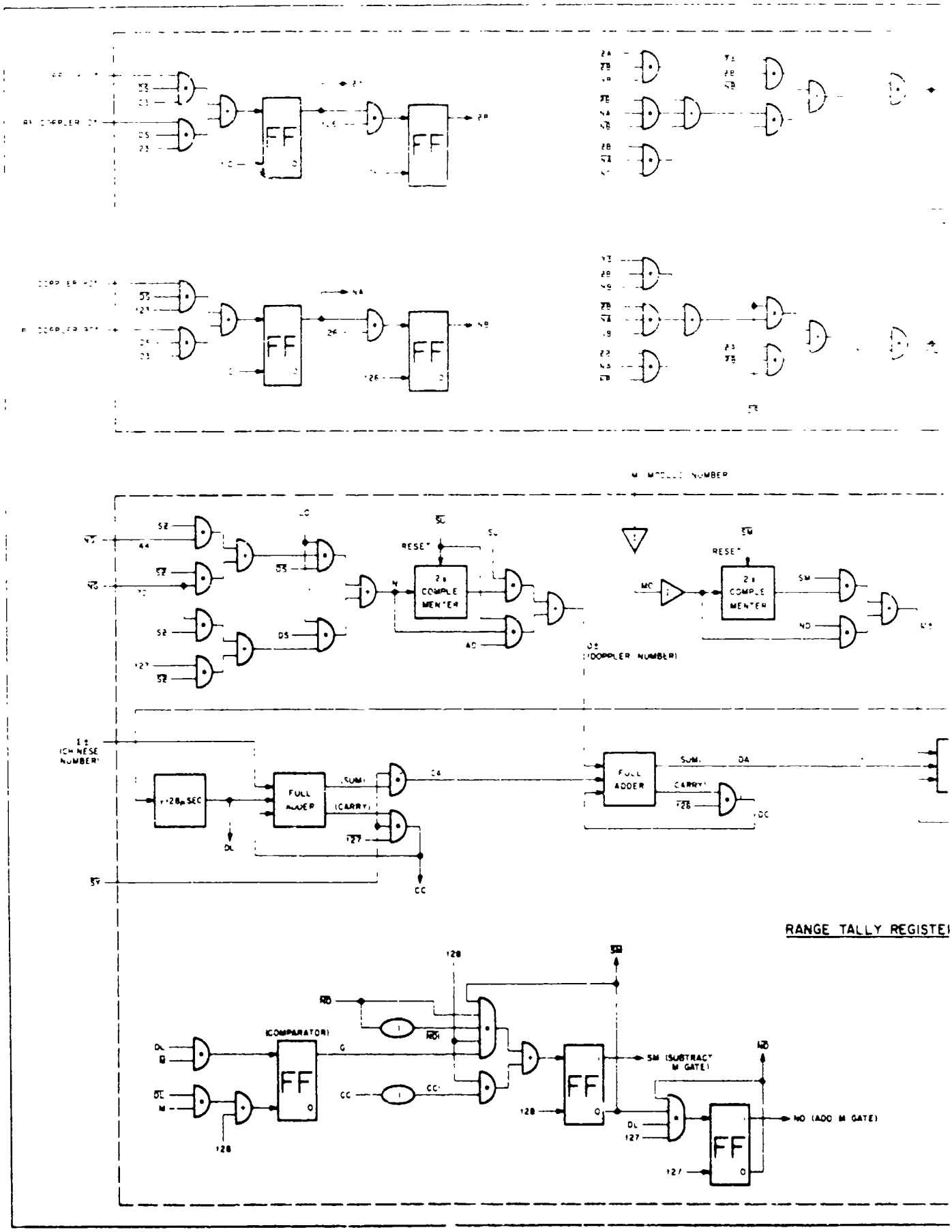
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT MD

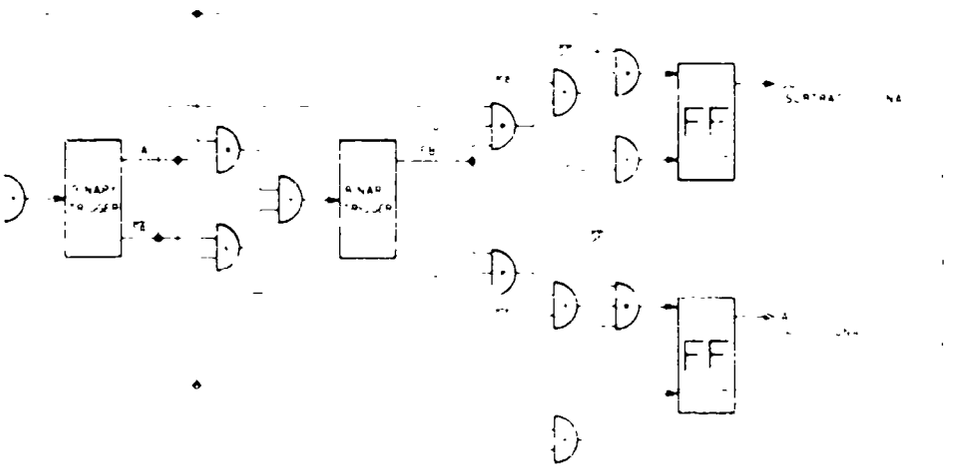
APOLLO RANGING DATA SUBSYSTEM

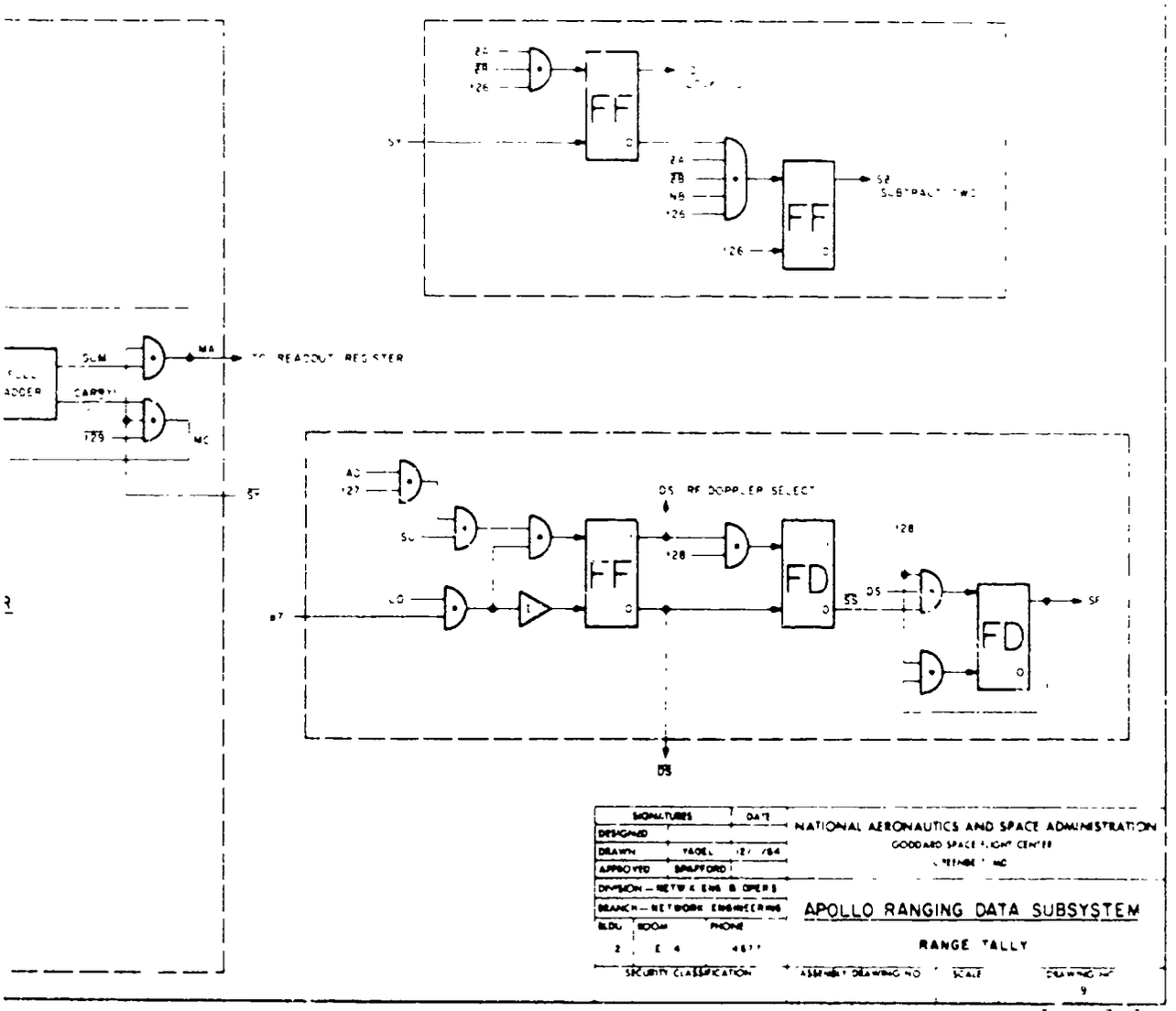
NUMBER GENERATOR

ASSEMBLY DRAWING NO	SCALE	DRAWING NO
		8

2


FF
FF
FF
FF
RESET
2's COMPLE MENTER
RESET
2's COMPLE MENTER
FULL ADDER
FULL ADDER
RANGE TALLY REGISTE
(COMPARATOR)
FF
FF
FF
SM (SUBTRACT M GATE)
NO (ADD M GATE)





SIGNATURES	DATE
DESIGNED	
DRAWN YAGEL	12/64
APPROVED BRADFORD	
DIVISION — NETWORK ENG & OPERS	
BRANCH — NETWORK ENGINEERING	
BLDG ROOM PHONE	
2 E 4 4677	

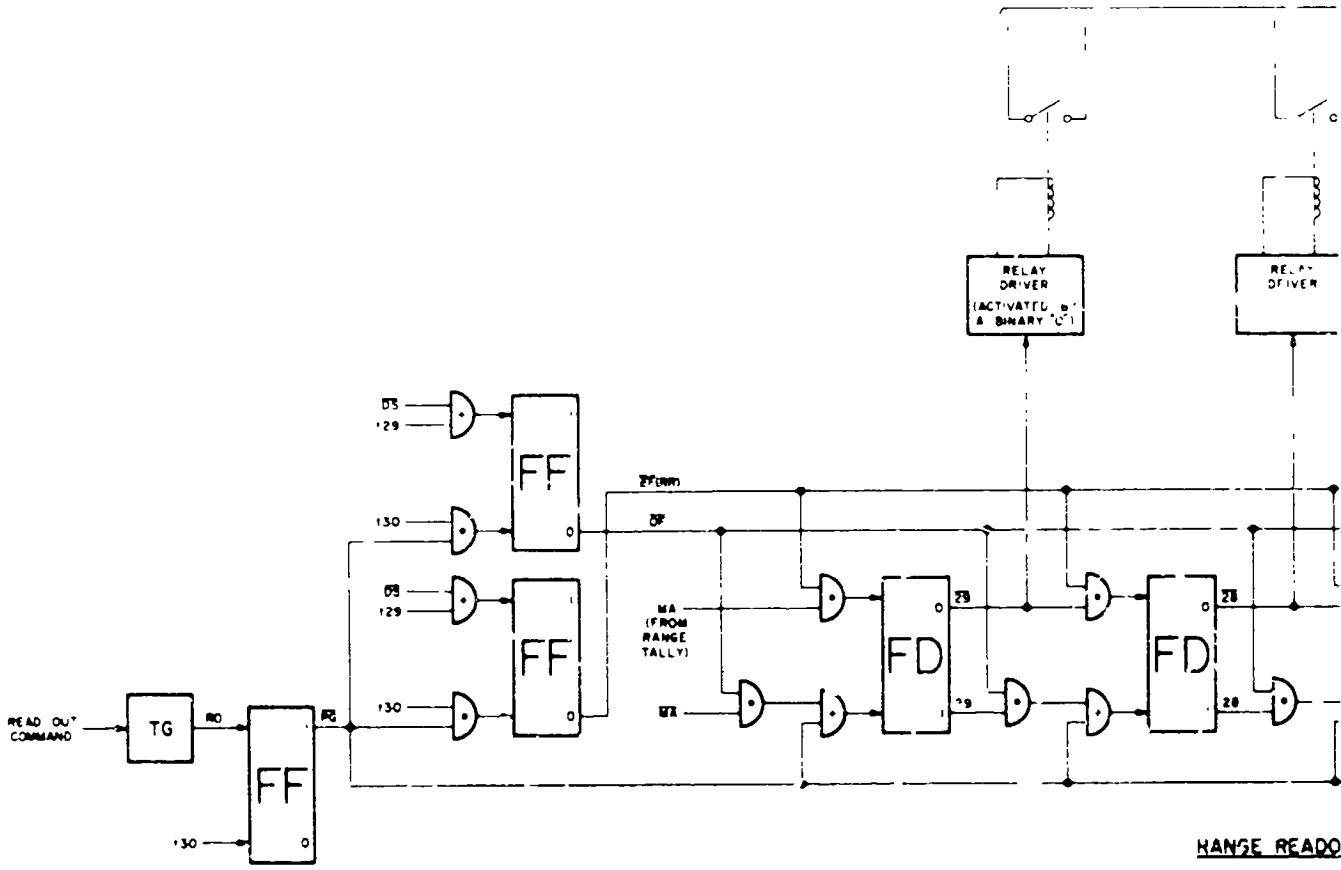
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MD

APOLLO RANGING DATA SUBSYSTEM

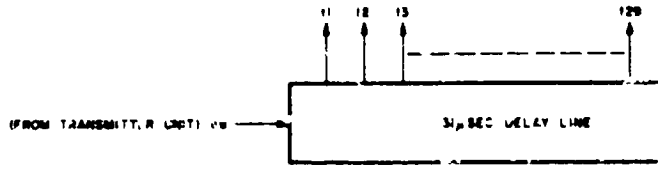
RANGE TALLY

SECURITY CLASSIFICATION — ASSEMBLY DRAWING NO — SCALE — DRAWING NO 9

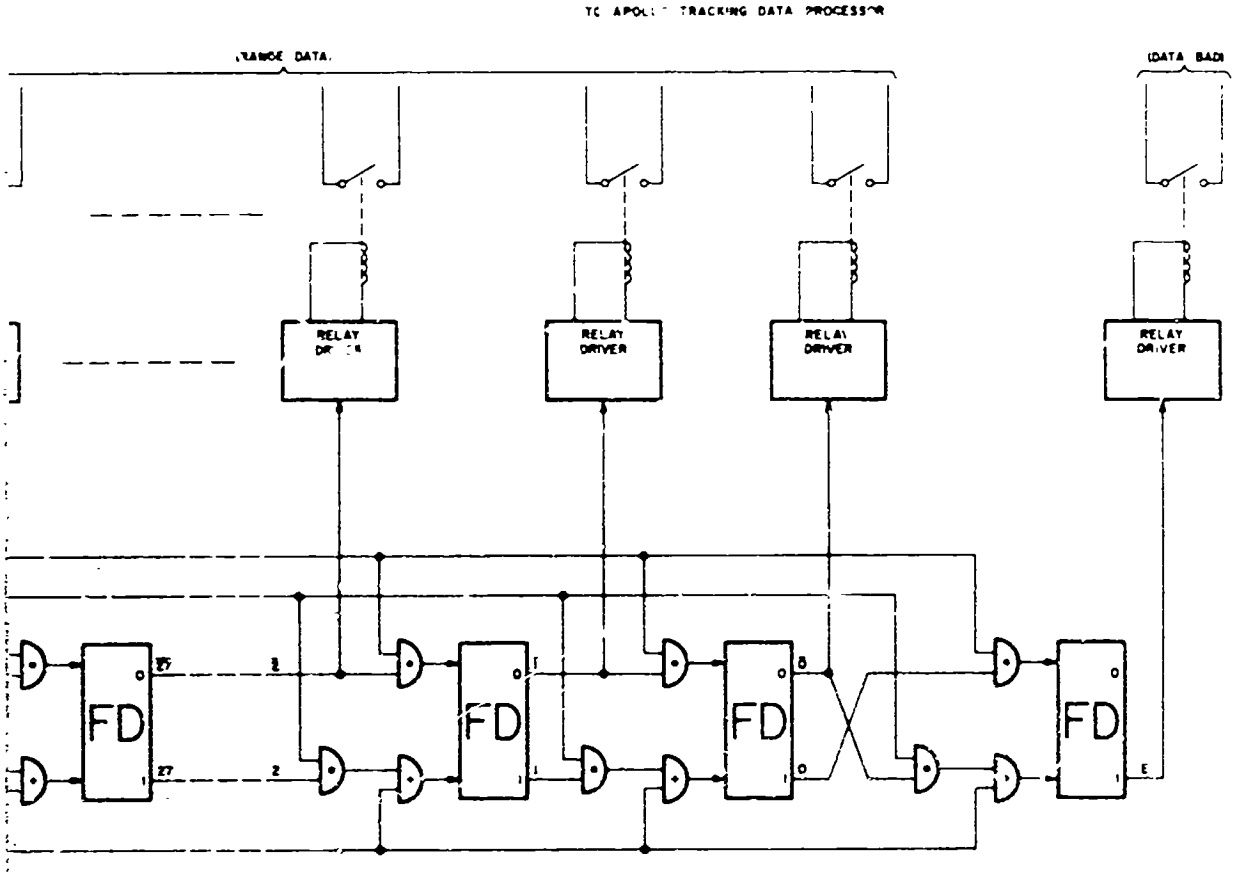
2



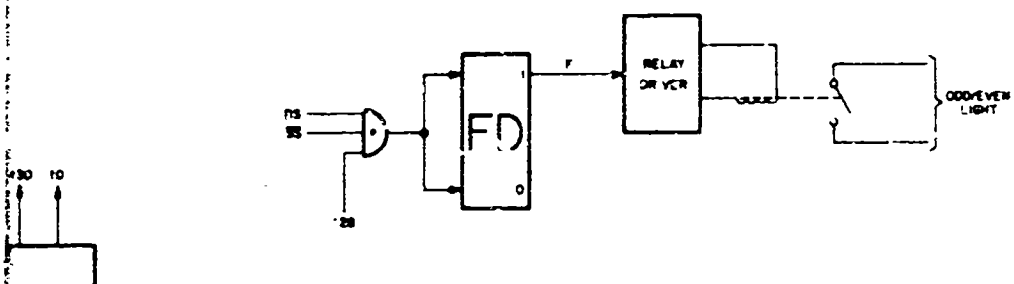
RANGE READO



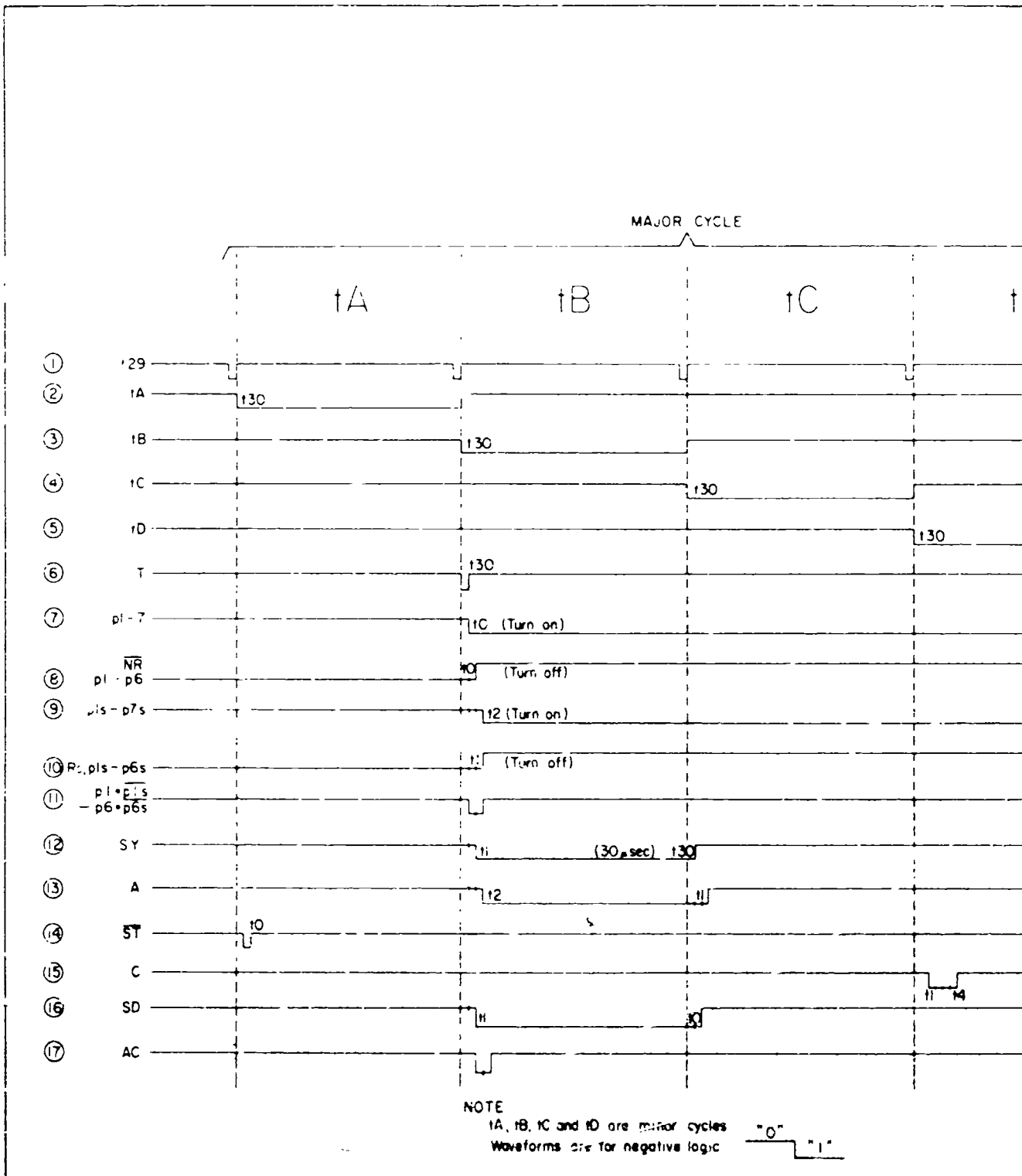
TIMER UNIT

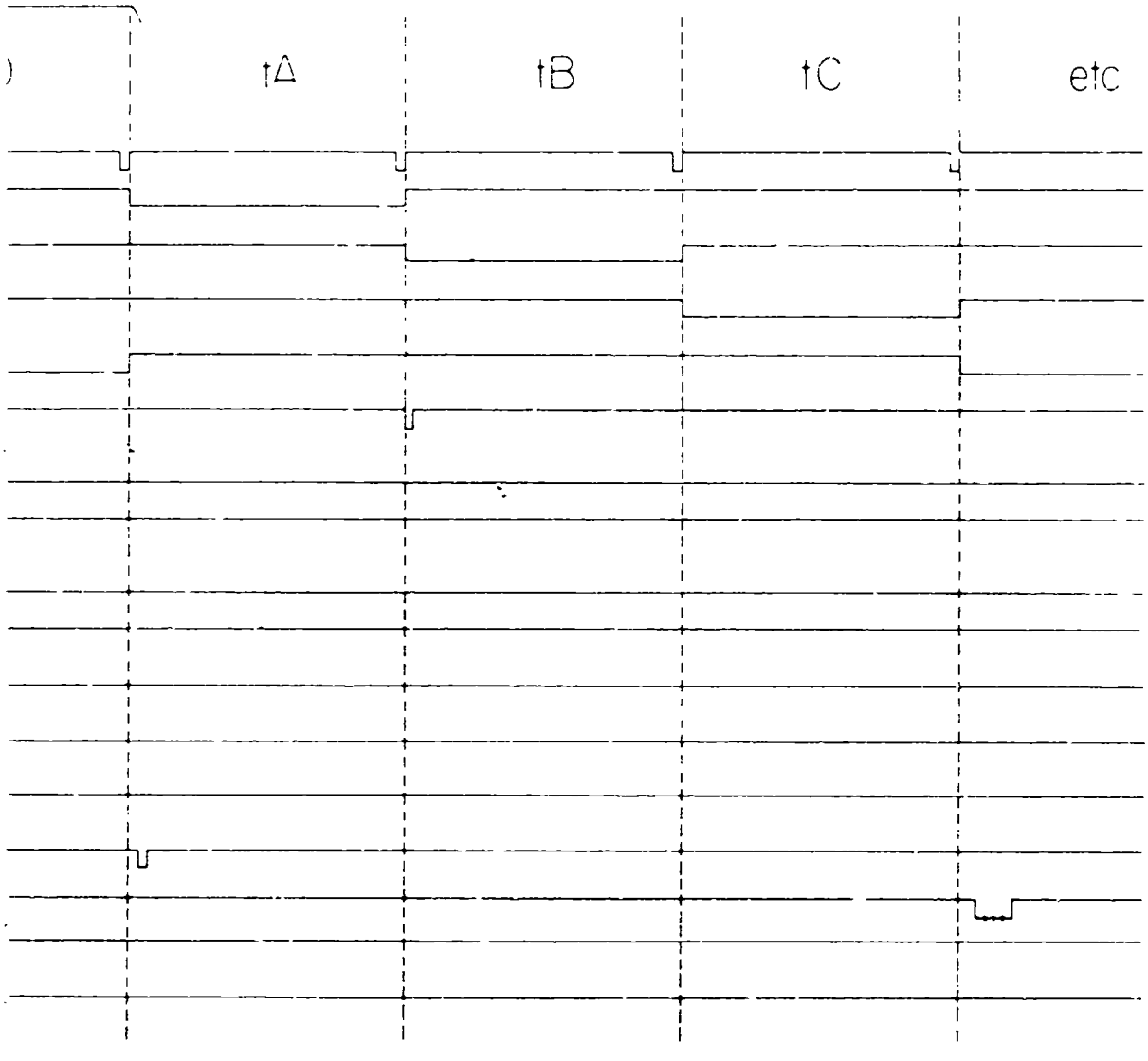


UT UNIT



SIGNATURES		DATE	NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
DESIGNED			GODDARD SPACE FLIGHT CENTRE
DRAWN	[illegible]	11/12/64	GREENBELT MD
APPROVED	[illegible]		
DIVISION— [illegible]			APOLLO RANGING DATA SUBSYSTEM
BRANCH— NETWORK ENGINEERING			READ OUT REGISTER & TIMER UNIT
BLDG 12	ROOM E-14	PHONE 4677	
SECURITY CLASSIFICATION			ASSEMBLY DRAWING NO — SCALE — DRAWING NO 10


MAJOR CYCLE
tA
tB
tC
t
① t29
② tA t30
③ tB t30
④ tC t30
⑤ tD t30
⑥ T t30
⑦ p1 - 7 tC (Turn on)
⑧ NR p1 - p6 t0 (Turn off)
⑨ p1s - p7s t2 (Turn on)
⑩ R, p1s - p6s t1 (Turn off)
⑪ p1•p1s - p6•p6s
⑫ SY t1 (30 μsec) t30
⑬ A t2 t1
⑭ ST t0
⑮ C t1 t4
⑯ SD t1 t3
⑰ AC
NOTE
tA, tB, tC and tD are major cycles
Waveforms are for negative logic
"0"
"1"



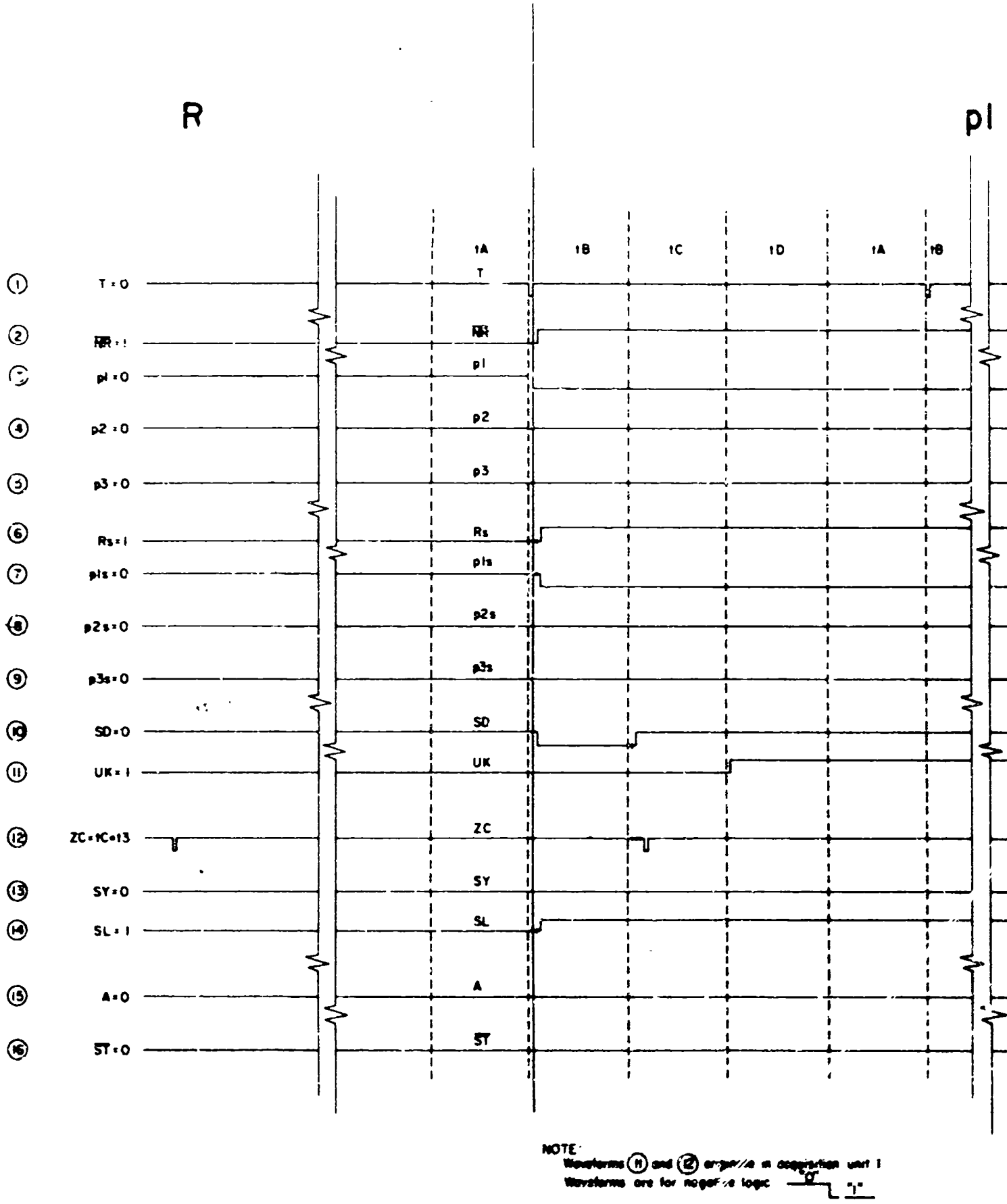
SIGNATURES		DATE
DESIGNED		
DRAWN	PLANNER	NOV 64
APPROVED	DRAFTSMAN	NOV 64
DIVISION— NETWORK SYSTEMS & OPERATIONS		
BRANCH— NETWORK SYSTEMS		
BLDG 12	ROOM E 14	PHONE 4477
SECURITY CLASSIFICATION		

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MD

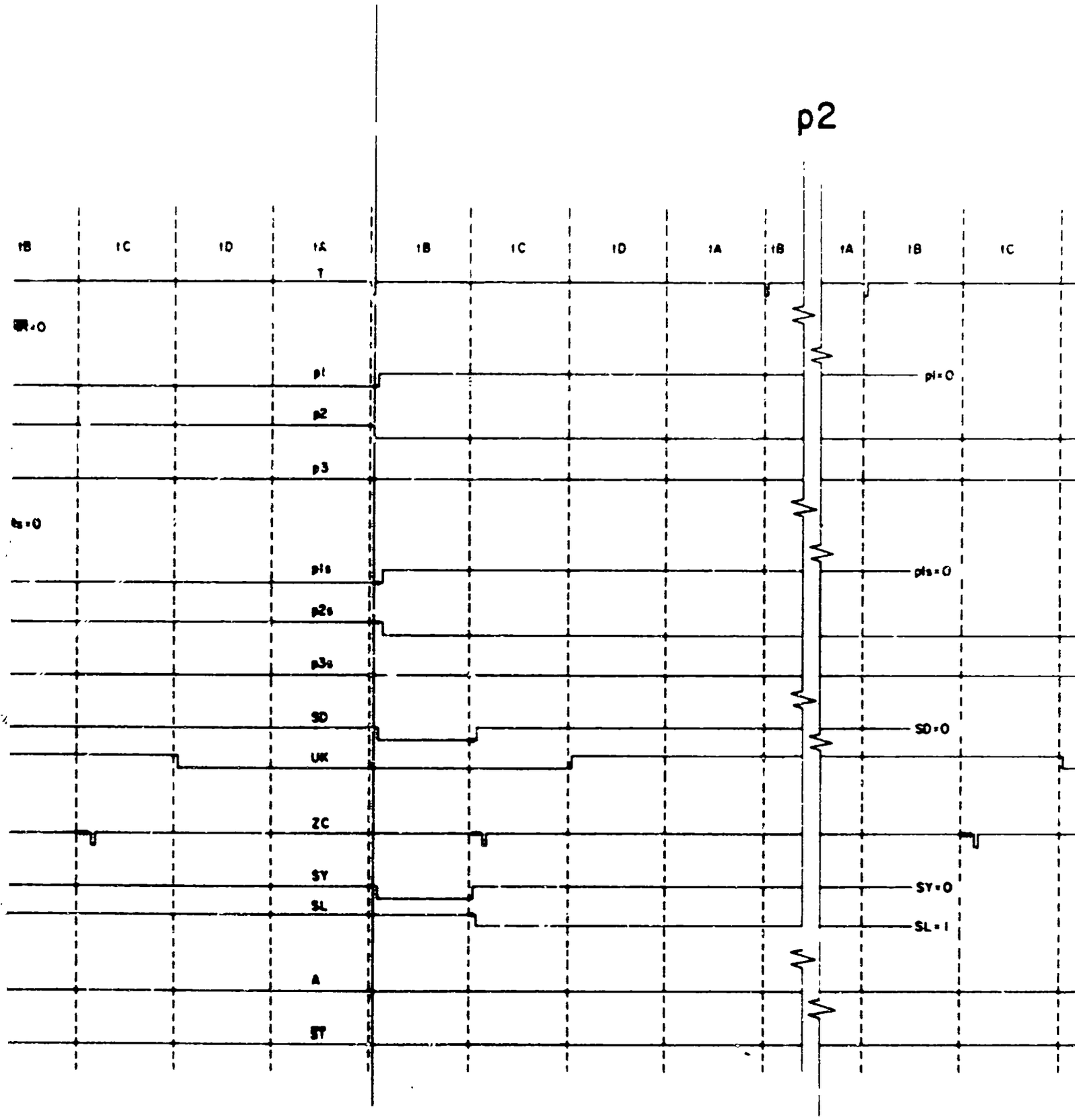
APOLLO RANGING DATA SUBSYSTEM

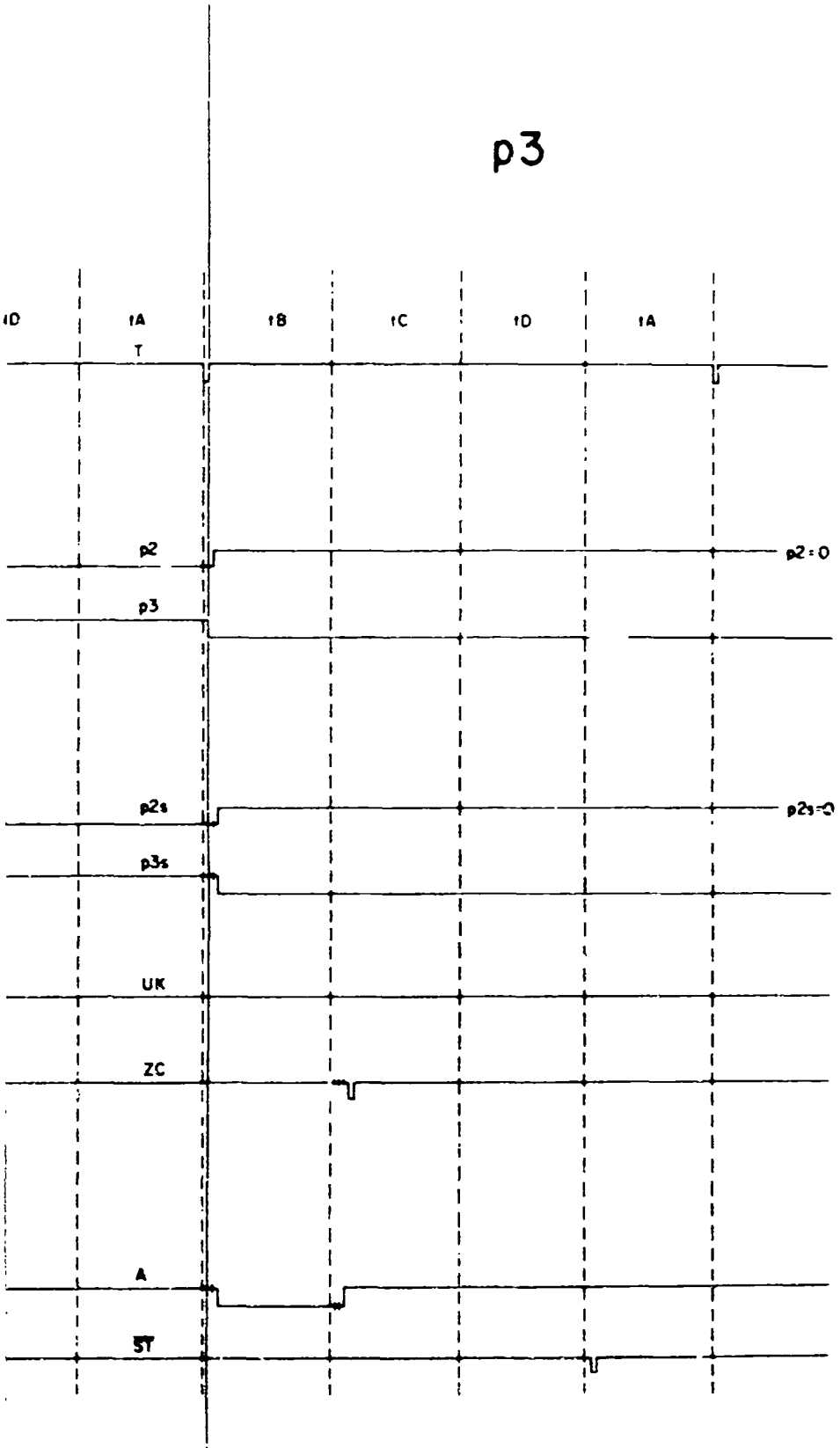
PROGRAM UNIT WAVEFORMS

ASSEMBLY DRAWING NO.	SCALE	DRAWING NO.
		11



NOTE:
Waveforms ⑪ and ⑫ are in opposition unit 1
Waveforms are for negative logic "0" "1"

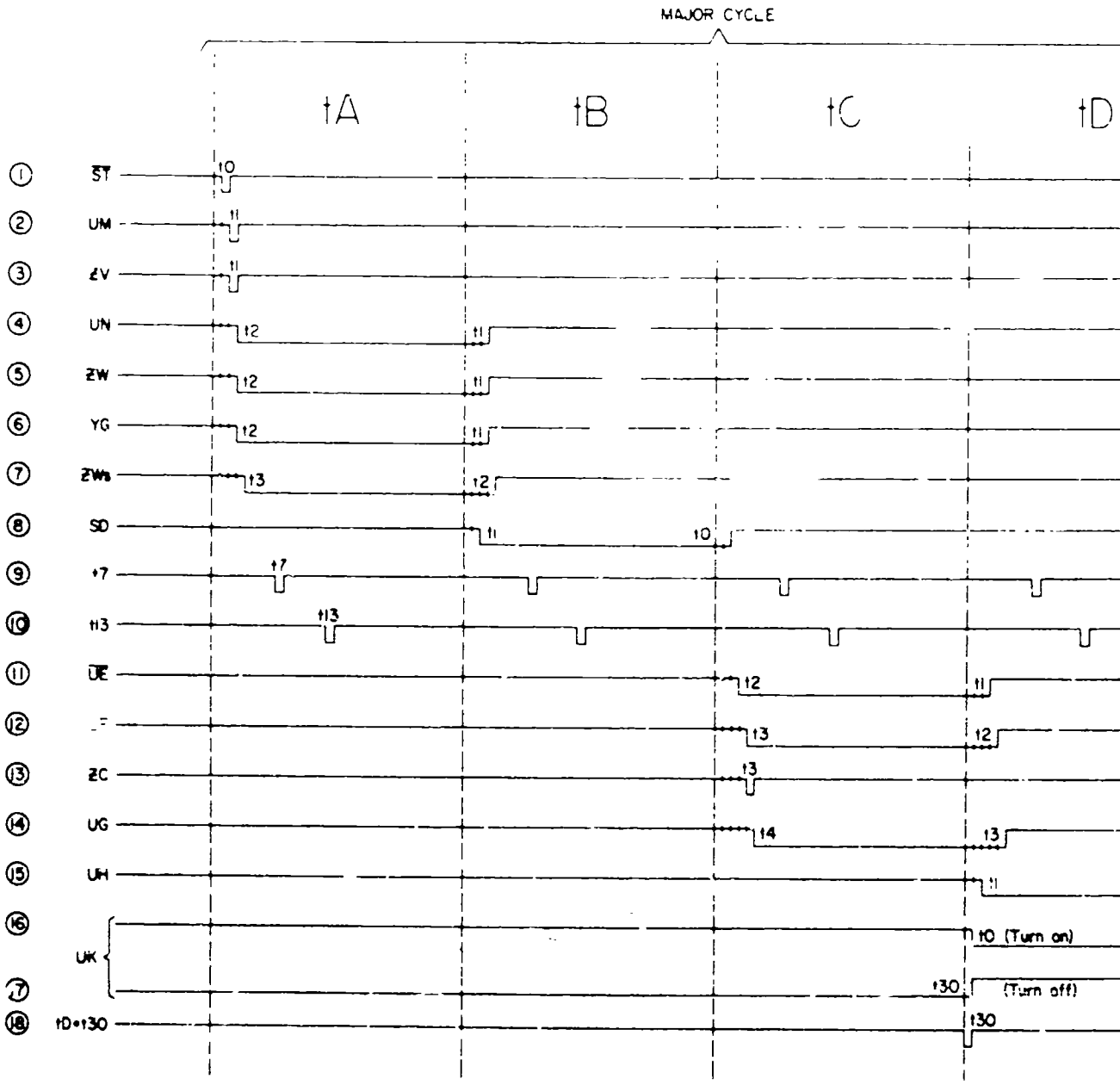

p2
tB
tC
tD
tA
T
pi
p2
p3
pis
p2s
p3s
SD
UK
ZC
SY
SL
A
ST
pi=0
pis=0
SD=0
SY=0
SL=1



APOLLO [illegible] DATA [illegible]

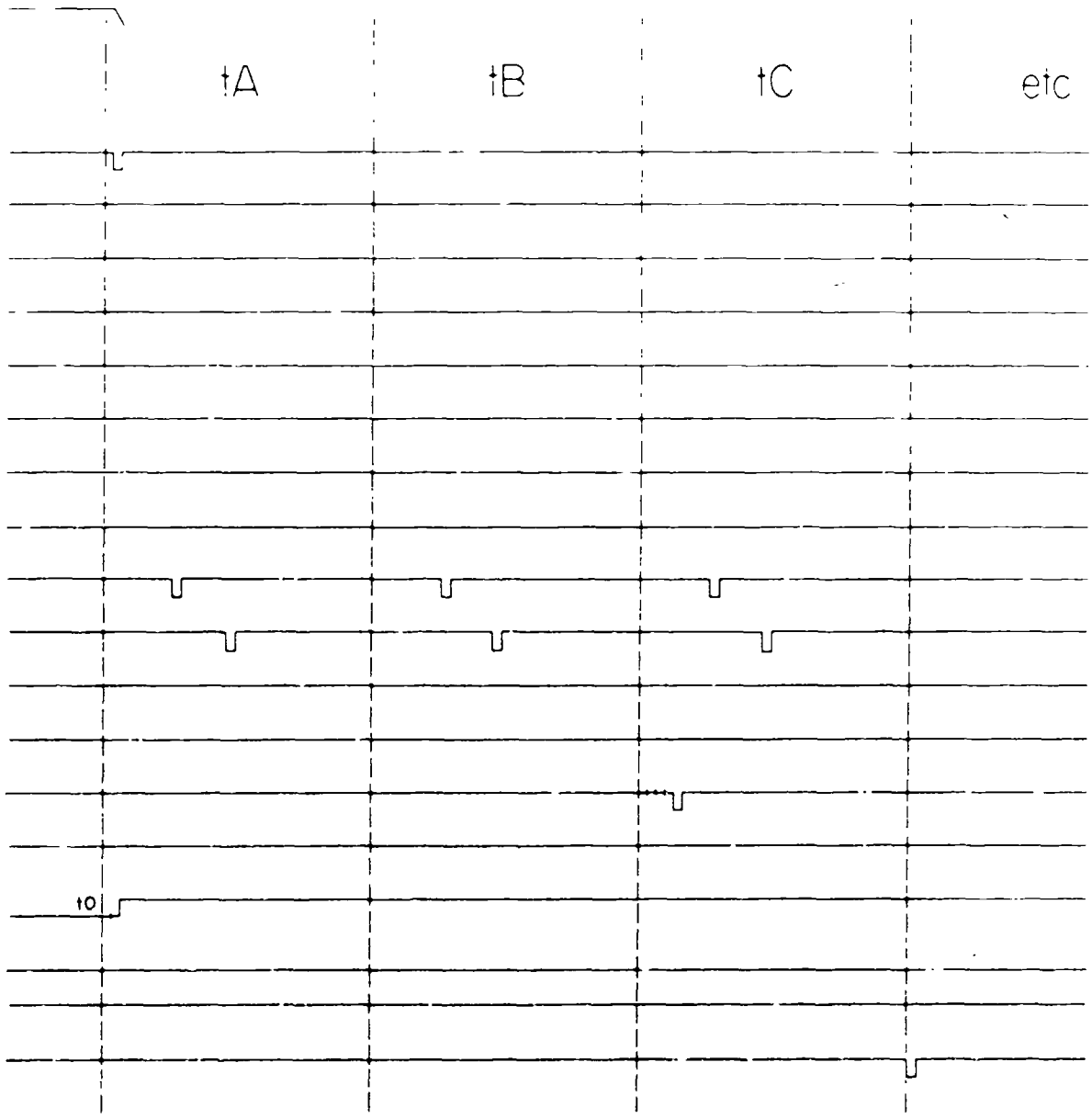
R, P1, P2 AND ASSOCIATED WAVEFORMS

[illegible] - P1 [illegible] - SEC 04
[illegible] - [illegible] - SEC 04
[illegible] 12

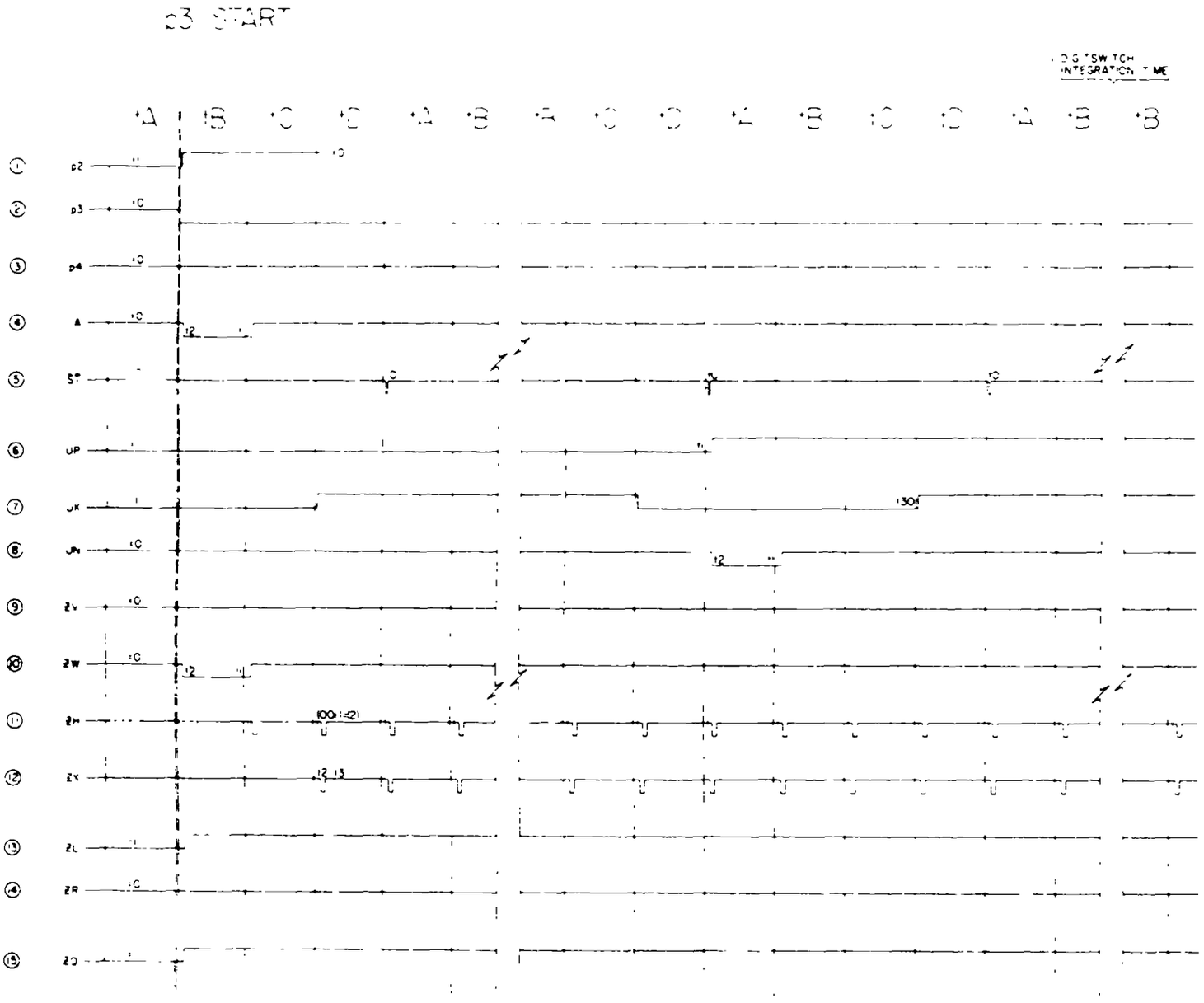


NOTE

1. tA, tB, tC and tD are minor cycles.
2. Waveforms are for negative logic: "0" = ▁, "1" = ▔
3. Waveforms ② through ⑧, ⑯ and ⑰ do not necessarily occur during the same major cycle
4. Waveforms ① through ⑮ show the timing of a 31 bit number (1's and 0's not shown) relative to the unit subtract pulse ⑮

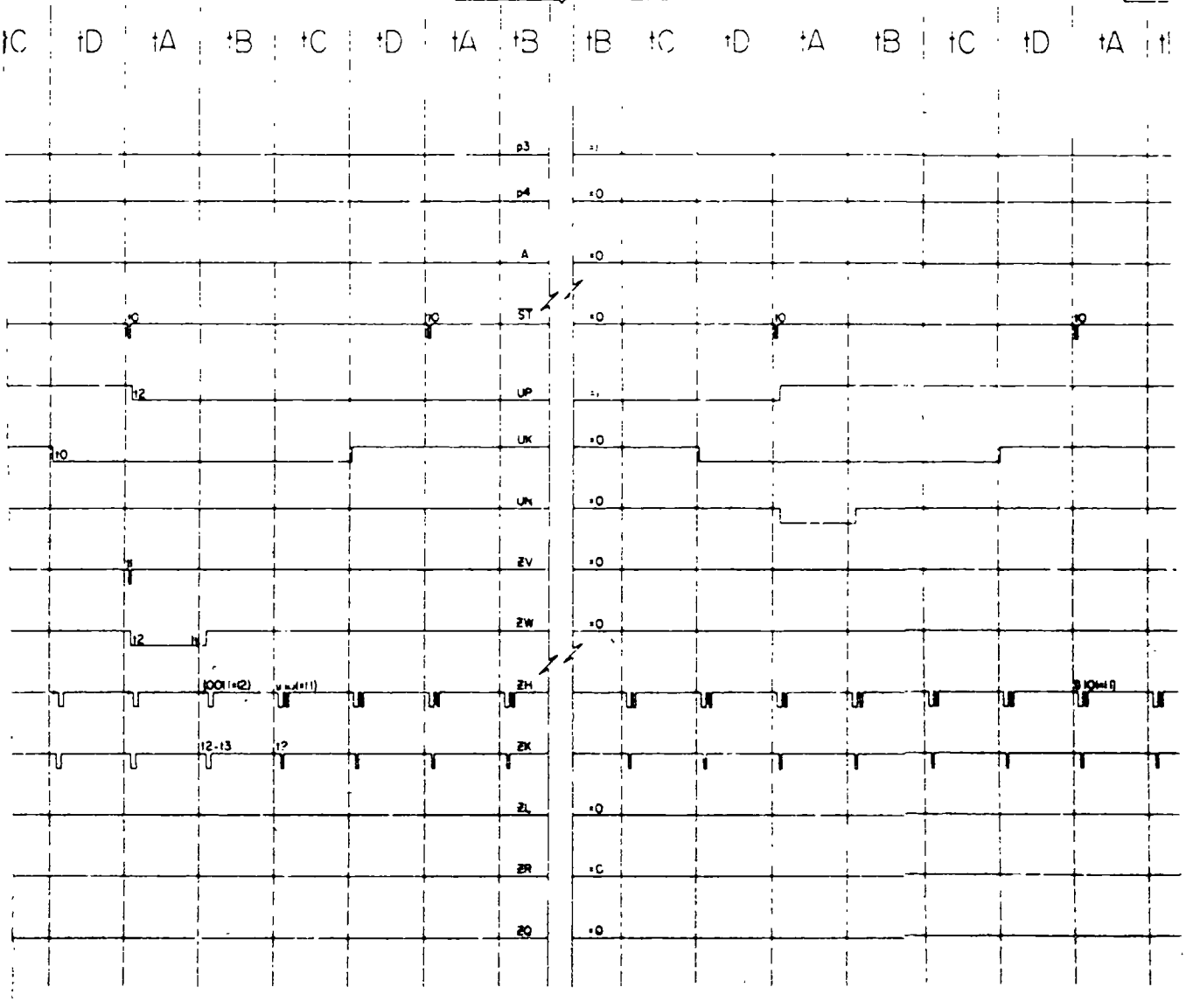


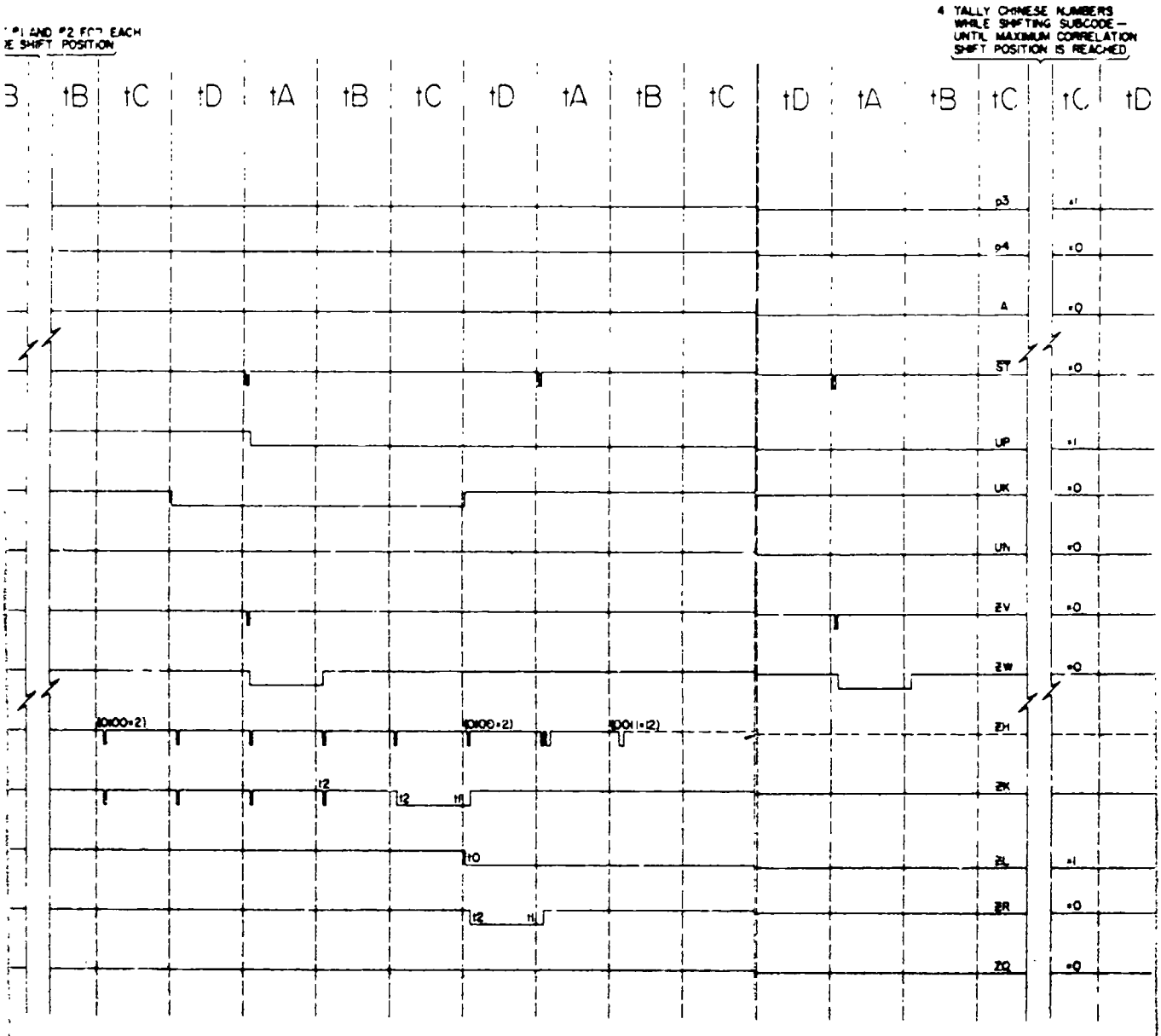
DESIGNED			DATE
DRAWN	TIBBEL	3/15/65	NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
APPROVED	SHAFFER		GODDARD SPACE FLIGHT CENTER
DIVISION — NET ENGRG & OPNS			GREENBELT, MD
BRANCH — NETWORK DATA SYS			APOLLO RANGING DATA SUBSYSTEM
SIZE: 12	CODE: E-14	PROJECT: 466	ACQUISITION UNIT TIMING
SECURITY CLASSIFICATION			ASSEMBLY DRAWING NO. / SCALE / DRAWING NO. 13


C3 START
A
B
C
D
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
p2
p3
p4
A
ST
UP
UK
UN
ZV
ZW
ZH
ZX
ZL
ZR
ZD

2 SHORT DELAY SO CHINESE NUMBER CAN BE STORED IN RANGE TALLY

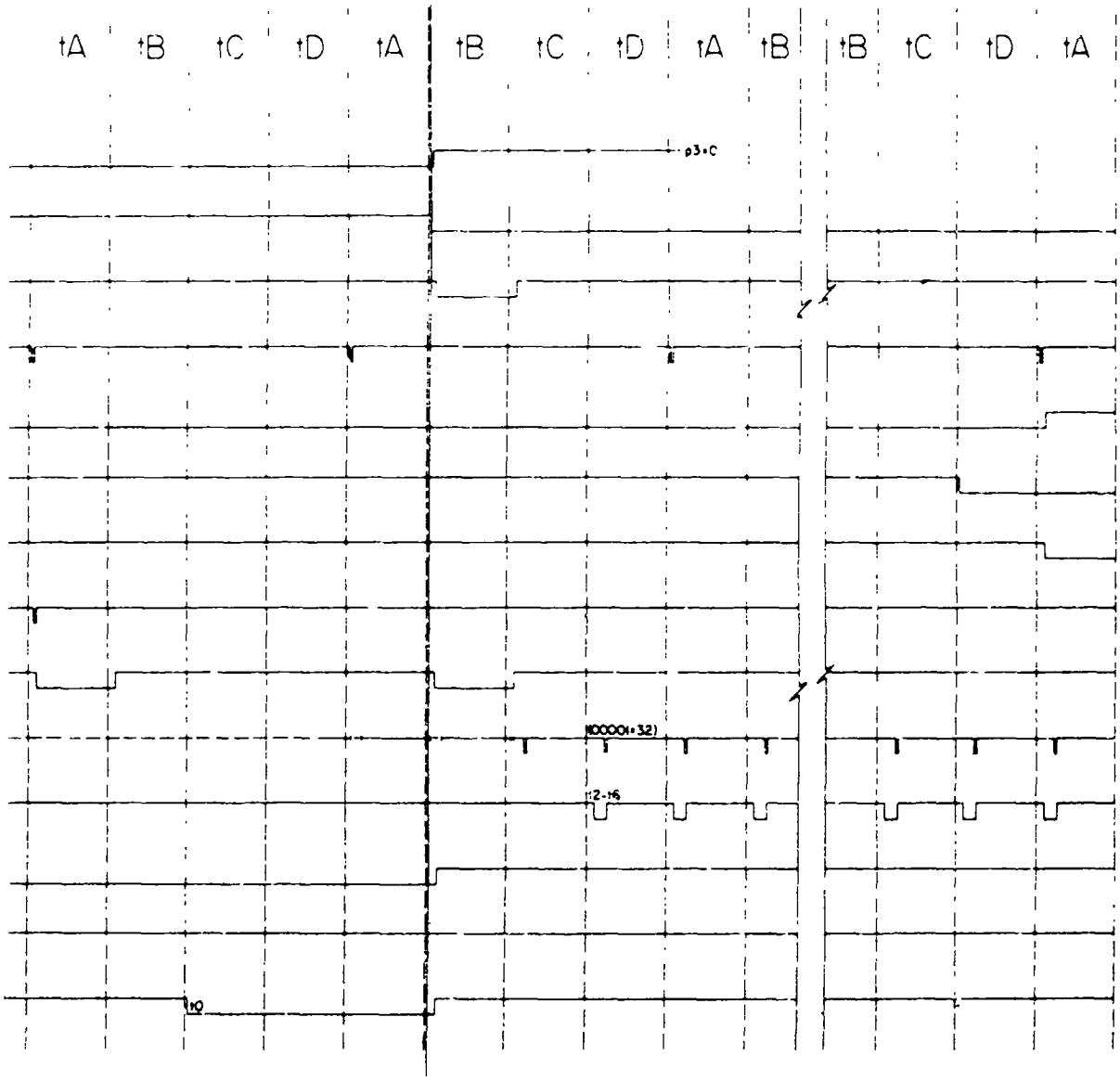
3 REPEAT SUBCC





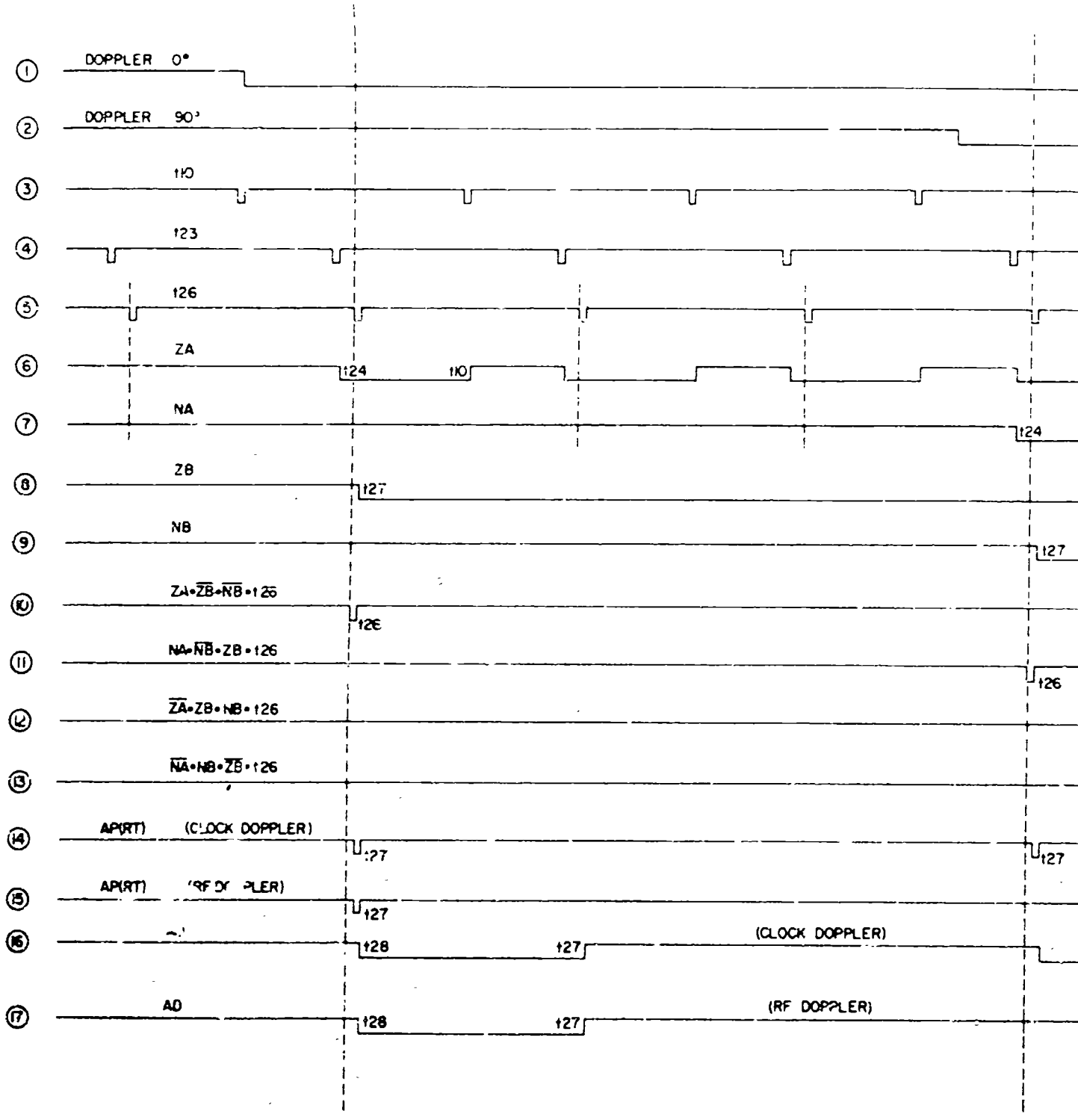
NOTE
WAVEFORMS ARE FOR NEGATIVE LOGIC "0" "1"
BINARY (AND DECIMAL) VALUE OF ZH IS SHOWN IN PARENTHESIS ON WAVEFORM (11)

p4 START

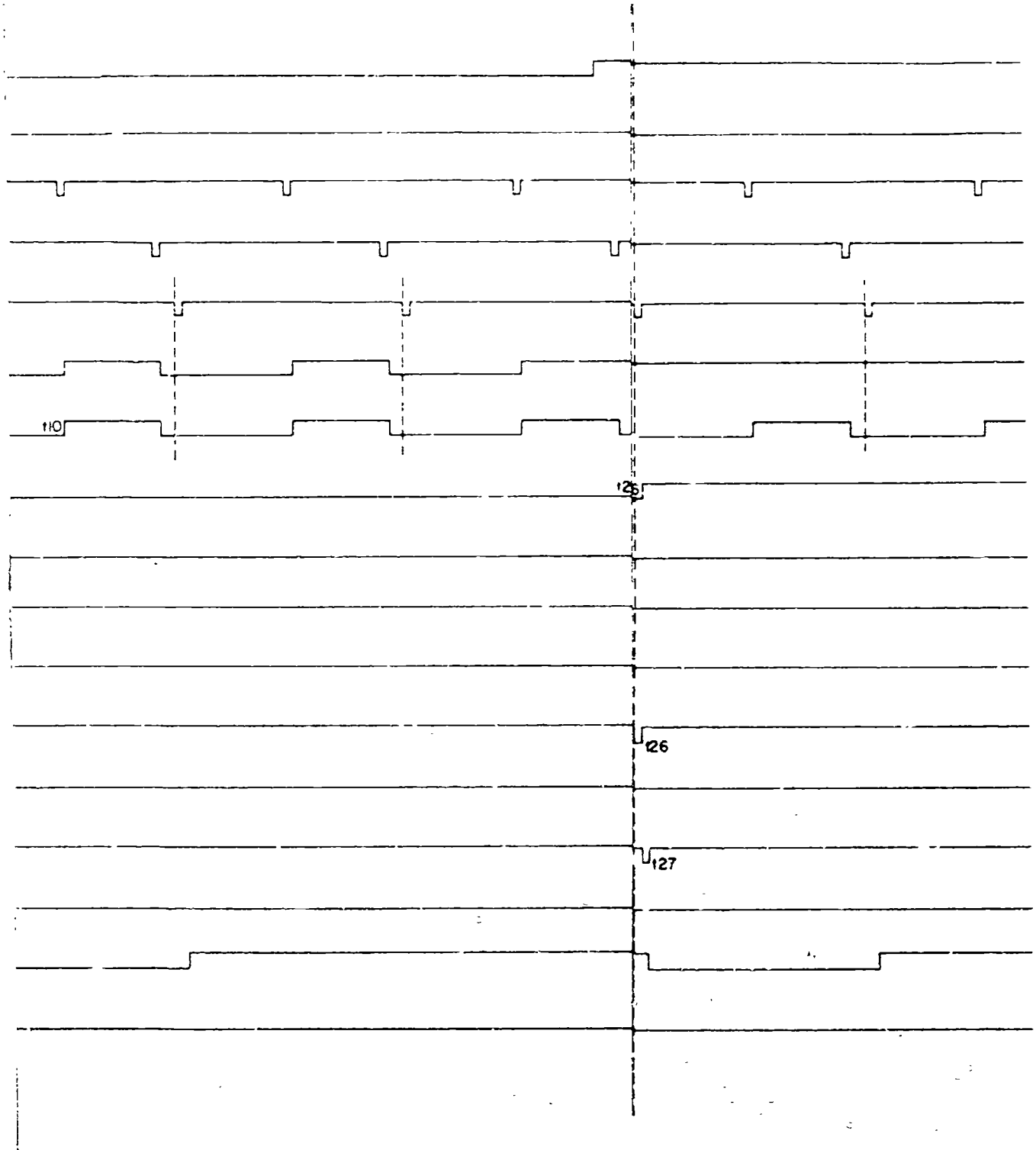


ACOLLA RANGER BETA SUBSYSTEM
p3 AND ASSOCIATED WAVEFORMS
(p4, p5 AND p6 ARE SIMILIAR)

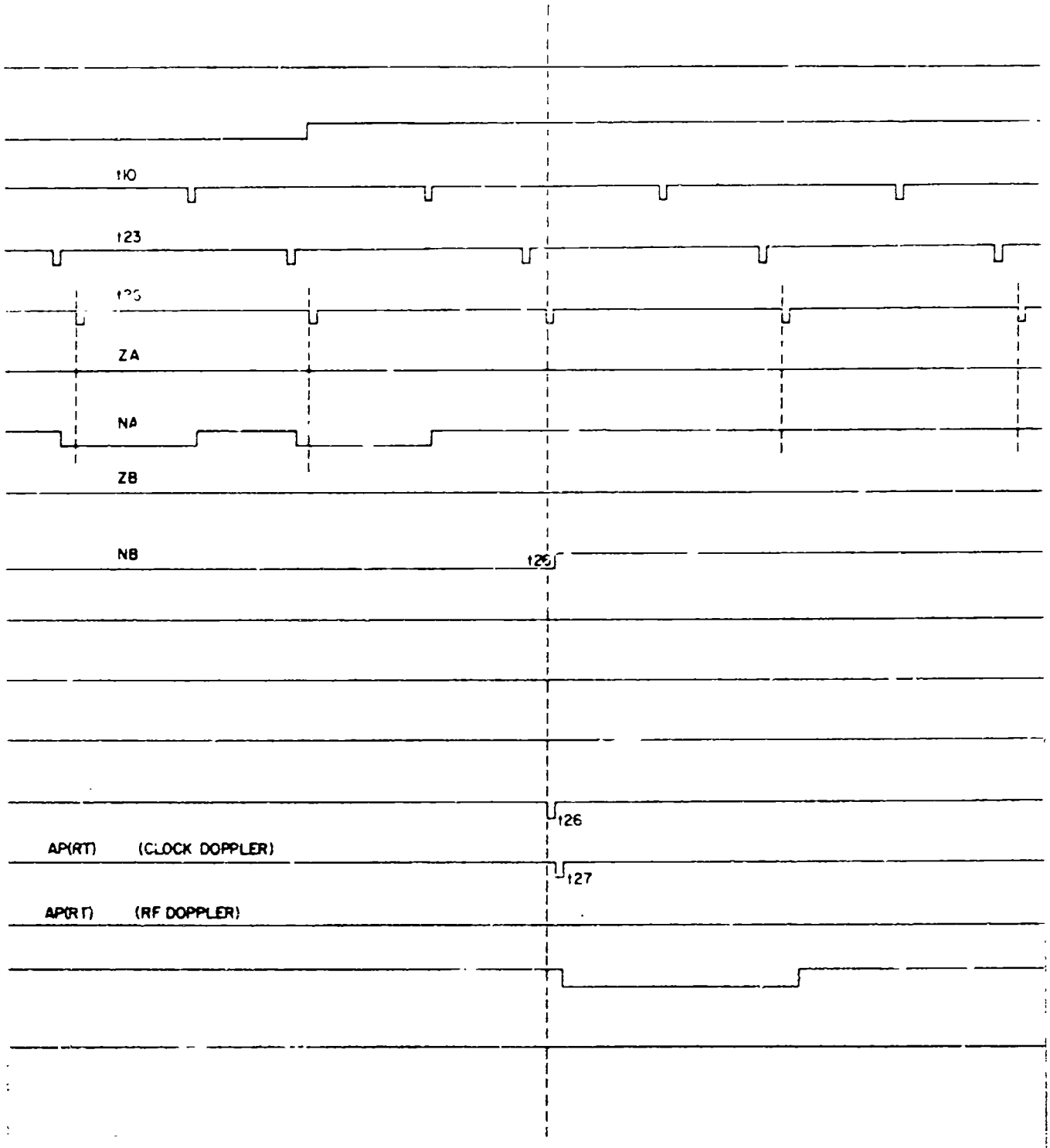
4

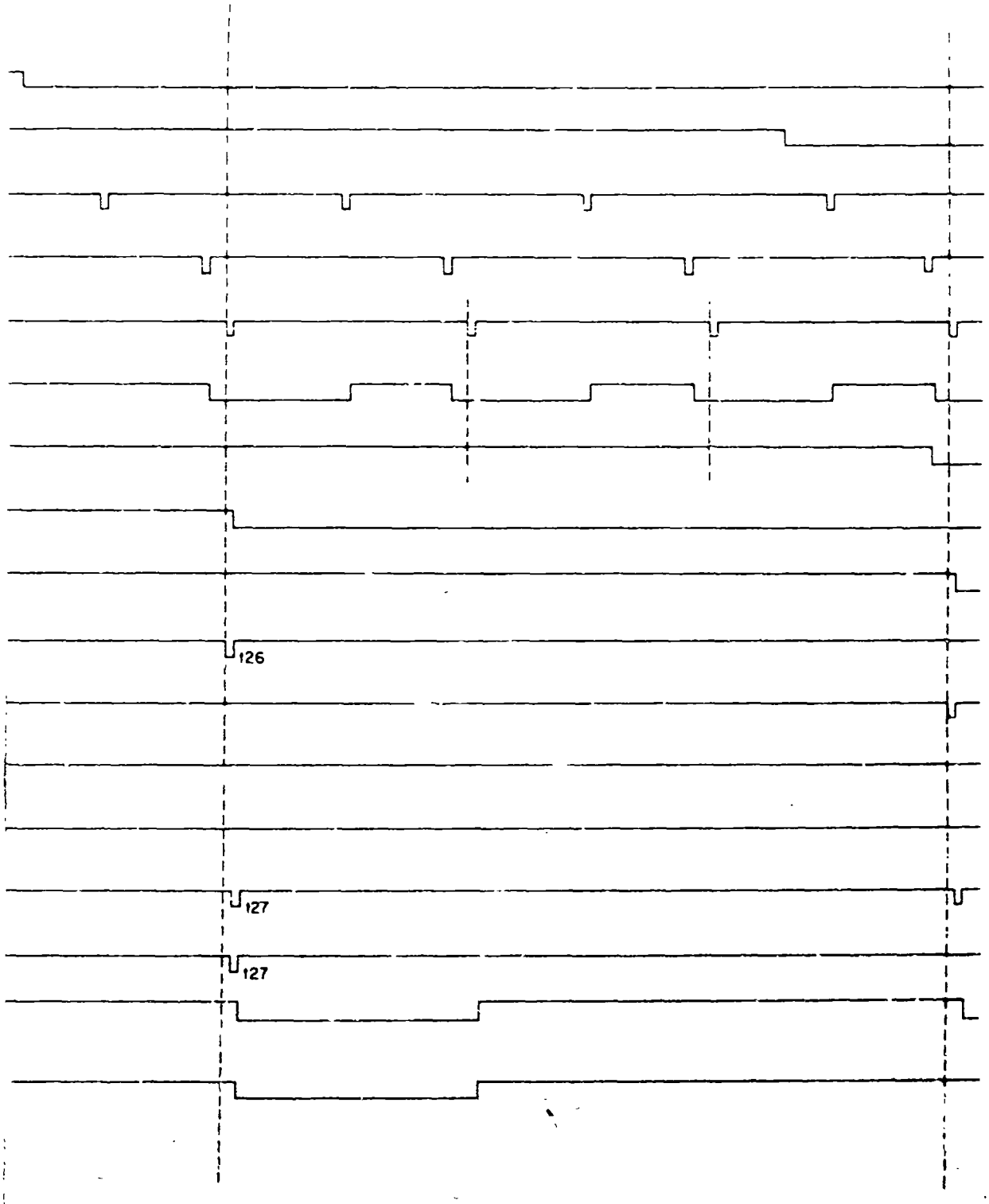


NOTE:
WAVEFORMS ARE FOR NEGA



VE LOGIC. "0" "1"


110
123
ZA
NA
ZB
NB
126
126
AP(RT) (CLOCK DOPPLER)
127
AP(RT) (RF DOPPLER)



APOLLO GUIDANCE & DATA SYSTEM

RANGE TALLY WAVEFORMS

DRAWN: FLANAGAN DEC '64
APPROVED: SHAFFORD DEC '64

DWG NO 15

INPUT & CONTROL RELAYS CABLE

					A		B	C		FUNCT
01		RCVR OPERATIONAL	KA1						41	
10									42	
02		TRANS LOOP TO XMTR	KA2	J1B20	+		TR-51	AUI-11	46	$\overline{t_0}$
20					+		TR-1	AUI-12	47	$\overline{t_1}$
03		TRANS LOOP TO RCVR	KA3						48	
30				J1B09	+		TR-17		49	$\overline{t_{29}}$
04		TRANS LOOP LOCK	KA4	J1B10	+		TR-50	AUI-10	50	$\overline{t_{30}}$
40									51	
05		RCVR IN LOCK	KA5						52	
50									53	
06		CLOCK LOOP IN LOCK	KA6						54	
60									55	
07		SPARE	KA7						56	
70									57	
08		SPARE	KA8						58	
80									59	
									60	
									61	
									62	
									63	
				J1A20	AUI-24		TR-71	+	64	t_0
				J1A04	AUI-25		TR-24	+	65	t_4
									66	
									67	
56		TRANS LOOP SYNC	KC4						68	
59		RELAY SUPPLY COMMON		J1C09			TR-69	+	69	t_{29}
									70	
79		RELAY SUPPLY MINUS							71	
									72	
				J1C03	AUII-29		NG-23	•	73	p_3
				J1C04	AUII-30		NG-24	•	74	p_4
				J1C05	AUII-31		NG-25	•	75	p_5
				J1C06	AUII-32		NG-26	•	76	p_6
					AUI-22			•	77	t_C
					AUI-21			•	78	t_D
									79	
					AUI-23			•	80	$\overline{t_D}$

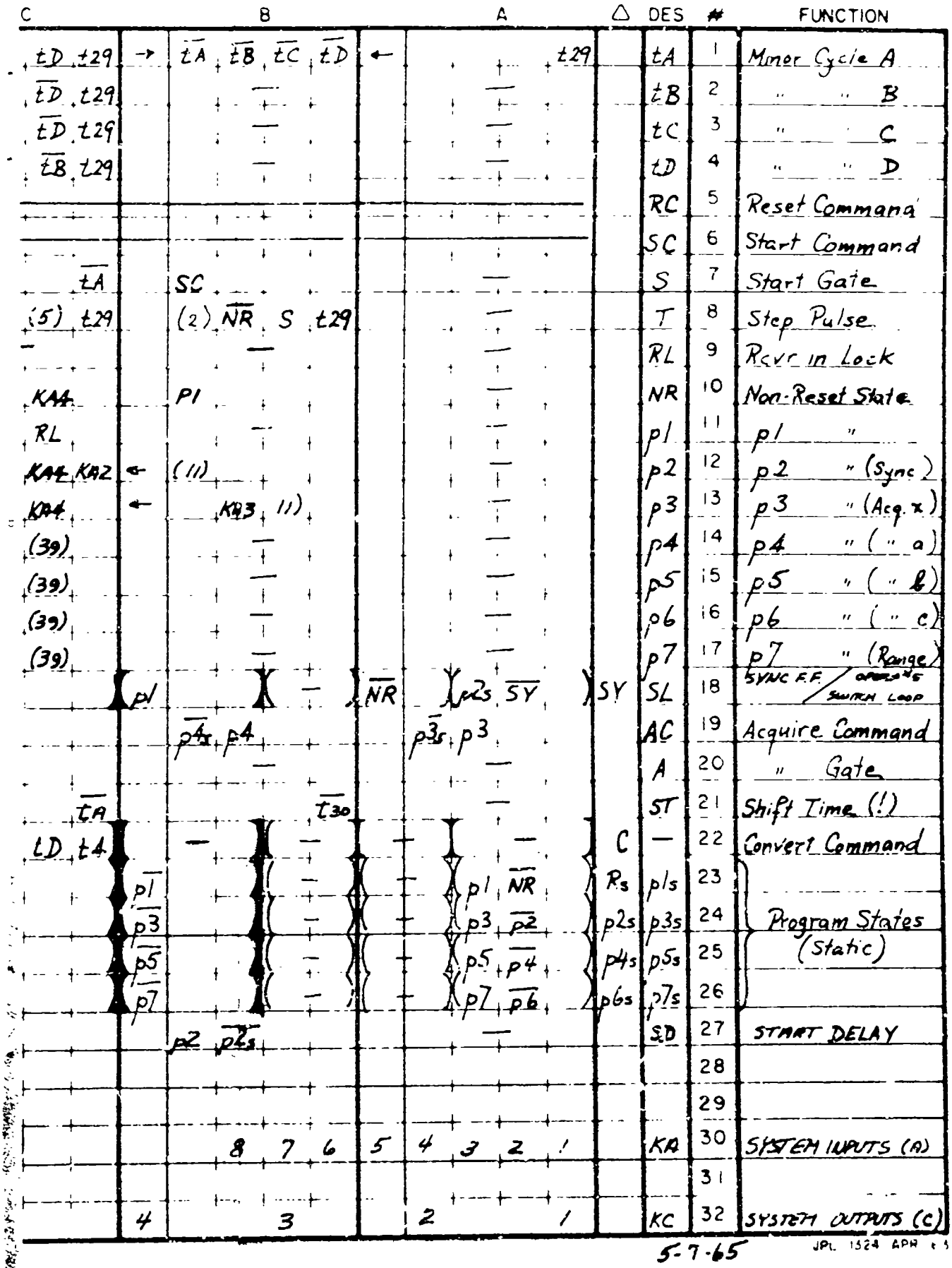
5-7-65 JPL 132

DRAWING 16: PROGRAM UNIT (PU)

		A	B	C		FUNCTION
J3A01	+		J7G			Man. Program
J3A02	+		J7H		2	" " Bar
J3A03	+		J5n		3	Reset Pulse
J3A04	+		J5m		4	Start Pulse
J3C02	+		J7F	AUI-42	5	Man. SHIFT BAR
	•	$\overline{SD}$		AUI-14	6	START DELAY BAR
					7	
					8	
					9	
					10	
	+			AUI-19	11	DELAY COUNT FINISHED
					12	
					13	
					14	
	•	A		AUI-15	15	Acquire Gate
	•	$\overline{A}$		AUI-16	16	" " Bar
					17	
					18	
J3B09	•	$\overline{C}$	J5IN		19	Convert Command Bar
	•	SD		AUI-13	20	START DELAY
J3A10			J6a	p1s	• 21	Prog. State (Static) 1
J3A11			J5b	p2s	• 22	" " " 2
J3A12		RCII-23	J5c	p3s	• 23	" " " 3
J3A13		RCI-24	J5d	p4s	• 24	" " " 4
J3A14		RCI-25	J5e	p5s	• 25	" " " 5
J3A15		RCI-21	J5f	p6s	• 26	" " " 6
J3A16		RCII-27	J5g	p7s	• 27	" " " 7
J3A17			J5z	Rs	• 28	" " " Reset
		RCI-32		SY	• 29	Sync.
J1C02		RCI-33	RT-40	$\overline{SY}$	• 30	" Bar
J3A19			J5-99	KA5	• 31	Rcvr. in Lock
J3A20			J6-34	KA1	• 32	RCVR OPERATIONAL
J3A18			J5-44	KA6	• 33	CLOCK LOOP IN LOCK
					34	
					35	
		AUII-36		AC	• 36	Acquire COMMAND
J1C07			RT-25	p7	• 37	p7
		AUI-61		NR	• 38	NON-RESET STATE BAR
		AUI-39			+ 39	Comp. Acq'd.
		AUI-46		$\overline{ST}$	• 40	Shift Time (1) Bar

INH	D					
		tA $\overline{t29}$				
		tB $\overline{t29}$			tA $\overline{t}$	
		tC $\overline{t29}$			tB $\overline{t}$	
		tD $\overline{t29}$			tC $\overline{t}$	
	(3)				—	
	(4)				—	
	S		$\overline{t29}$		S	
tA	(1) S		t29		(2) N	
	KA6 KA5 KA1 $\overline{RC}$					
RL	NR p2				NR	
	p1 $\overline{p2}$ RL				$\overline{NR}$	
	p2 $\overline{p3}$ NR			→	p1	
	p3 $\overline{p4}$ NR			→	p2	
	p4 $\overline{p5}$ NR				p3	
	p5 $\overline{p6}$ NR				p4	
	p6 $\overline{p7}$ NR				p5	
	p7 NR				p6	
p2	$\overline{p2_s}$	) — (	—		)	
	$\overline{p6_s}$ p6				$\overline{p5_s}$	
	A		$\overline{t1}$		AC	
	$\overline{p3}$ $\overline{p4}$ $\overline{p5}$ $\overline{p6}$					
	tD t0	) — (	—		)	
$\overline{NR}$		) — (	—		)	
p2	p1	) — (	—		)	
4	$\overline{p3}$	) — (	—		)	
p6	$\overline{p5}$	) — (	—		)	
	SD		$\overline{t_0}$		p1	
(C01)	(C02)	(C03)	(C04)	(C05)	(E06)	
		(SL)		$P7_{CS}$	$P7_S$	

APR 63


C
B
A
△
DES
#
FUNCTION
tA 1 Minor Cycle A
tB 2 " " B
tC 3 " " C
tD 4 " " D
RC 5 Reset Command
SC 6 Start Command
S 7 Start Gate
T 8 Step Pulse
RL 9 Rcvr in Lock
NR 10 Non-Reset State
p1 11 p1 "
p2 12 p2 " (Sync)
p3 13 p3 " (Acq. x)
p4 14 p4 " (" a)
p5 15 p5 " (" b)
p6 16 p6 " (" c)
p7 17 p7 " (Range)
SL 18 SYNC F.F. / CARRIER SWITCH LOOP
AC 19 Acquire Command
A 20 " Gate
ST 21 Shift Time (!)
C — 22 Convert Command
p1s 23
p2s p3s 24 Program States (Static)
p4s p5s 25
p6s p7s 26
SD 27 START DELAY
28
29
KA 30 SYSTEM INPUTS (A)
31
KC 32 SYSTEM OUTPUTS (C)
5-7-65
JPL 1524 APR 65

	A		B	C			FUNCTION
J3C01	+		J7-E	AUII-13		41	MAN. SHIFT
	+		PU-5	AUII-14		42	" " BAR
J3A05	+		J7-C			43	MAN. STORE
J3A06	+		J7-D			44	" " BAR
J3A07	+		J7-J			45	"STORE" PULSE
						46	
						47	
						48	
						49	
J3B10	+		J52 F			50	Variation Output 0
J3B11	+		J52 R			51	1
J3B12	+		J52 J			52	2
J3B13	+		J52 J			53	3
J3B14	+		J52 T			54	4
J3B15	+		J52 [illegible]			55	5
J3B16	+		J52 E			56	6
J3B17	+		J52 P			57	7
J3B18	+		J52 [illegible]			58	8
J3B19	+		J52 H			59	9
J3B20	+		J52 HH			60	SIGN
			PU-38		+	61	NON-RESET STATE BAR
J1A01	AUII-35		TR-21		+	62	τ_1
J1A02	AUII-22		TR-22		+	63	τ_2
J3C04			J5-1		+	64	Digital Input No. 0
J3C05			J6-2		+	65	4
J3C06			J5-3		+	66	6
J3C07			J5-4		+	67	7
J3C08			J5-5		+	68	8
J3C09			J5-6		+	69	9
J3C10			J5-7		+	70	10
J3C11			J5-8		+	71	11
J3C12			J6-9		+	72	12
J3C13			J6-10		+	73	13
J3C14			J5-11		+	74	14
J3C15			J5-12		+	75	15
J3C16			J5-13		+	76	16
J3C17			J5-14		+	77	17
J3C18			J5-15		+	78	18
J3C19			J5-16		+	79	19
	AUII-38				+	80	SHIFT Command

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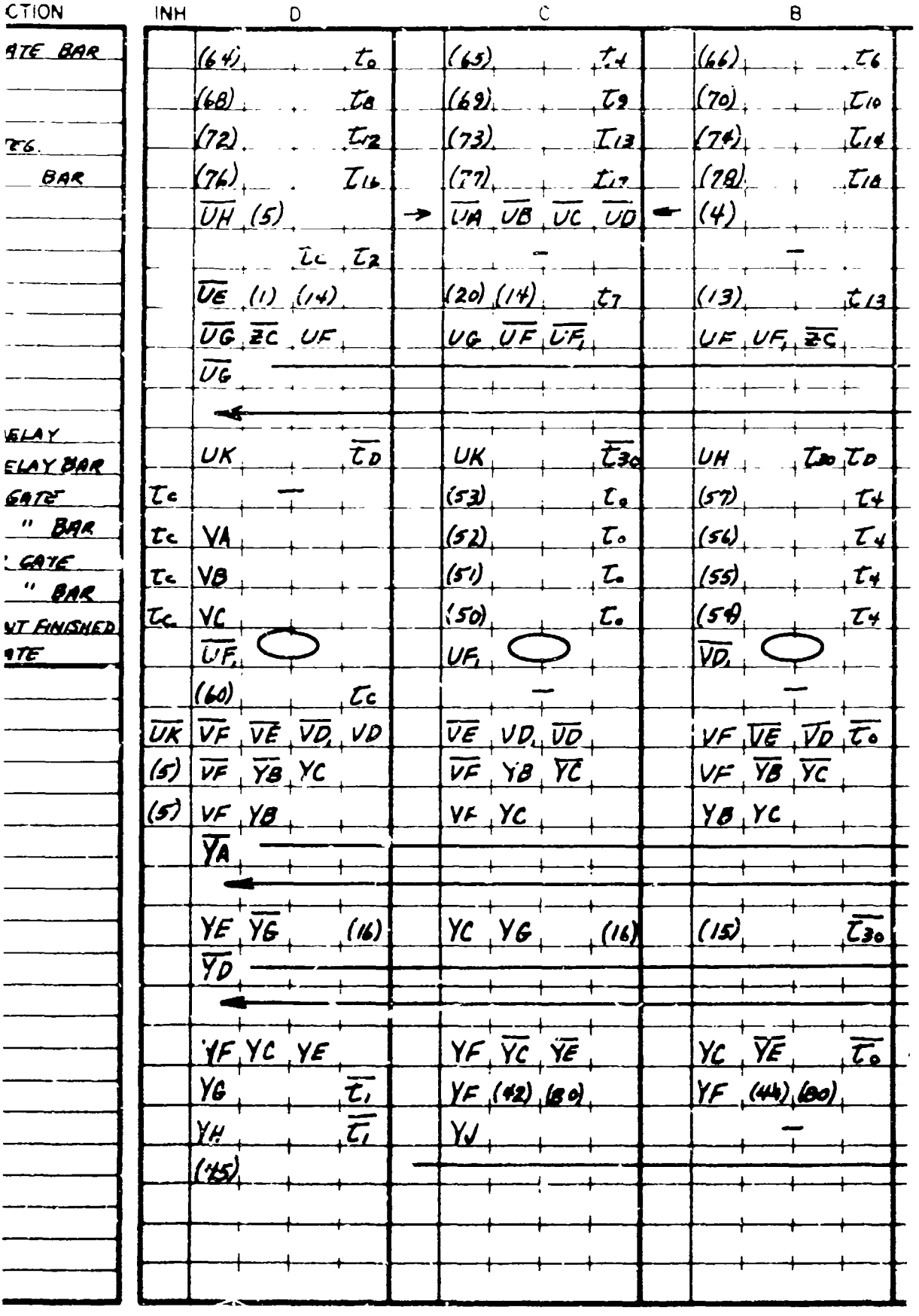
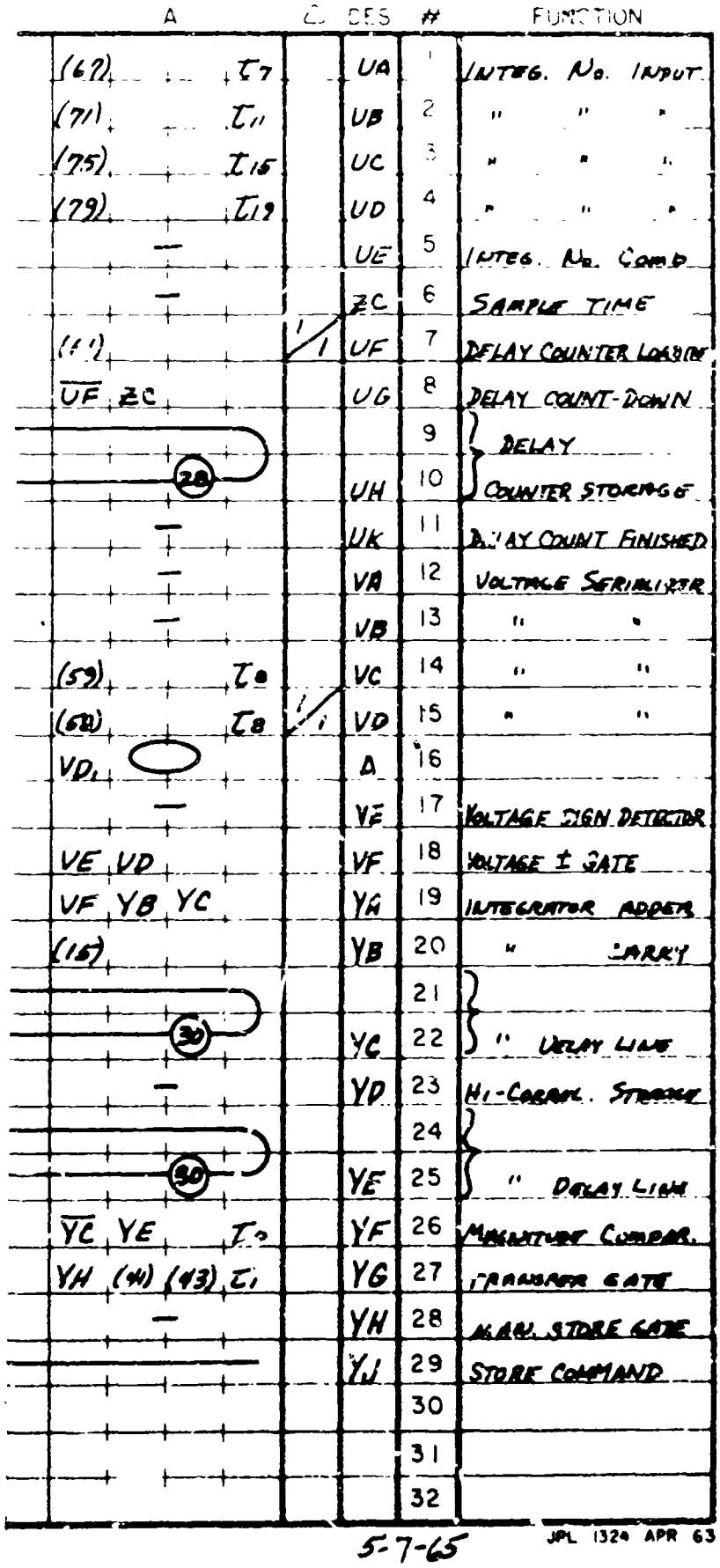
	A		B	C			FUN
	-			AUII-1		1	SHIFT C
						2	
						3	
	+			AU II-4		4	START IN
	+			AUII-5		5	" "
						6	
						7	
						8	
						9	
	+		PU-50	AUII-10		10	$\overline{\tau_{30}}$
	+		PU-116	AUII-11		11	$\overline{\tau_0}$
	+		PU-47	AUII-12		12	$\overline{\tau_1}$
	+		PU-20			13	START D
	+		PU-6			14	START D
	+		PU-15	AUII-15		15	ACQUIRE
	+		PU-16	AUII-16		16	"
	•	YG		AUII-17		17	TRANSFER
	•	$\overline{YG}$		AUII-18		18	"
	•	UK	PU-11	AUII-19		19	DELAY Coil
1B03	+		NG-56	AUII-9		20	SHIFT C
			PU-78		+	21	τ_D
			PU-77		+	22	τ_C
			PU-80		+	23	$\overline{\tau_D}$
	AUII-21		PU-64		+	24	τ_0
			PU-66		+	25	τ_4
J1A06	AUII-25		TR-26		+	26	τ_6
J1A07			TR-27		+	27	τ_7
J1A08			TR-28		+	28	τ_8
J1H09			TR-29		+	29	τ_9
J1A10			TR-30		+	30	τ_{10}
J1A11			TR-31		+	31	τ_{11}
J1A12			TR-32		+	32	τ_{12}
J1A13			TR-33		+	33	τ_{13}
J1A14			TR-34		+	34	τ_{14}
J1A15			TR-35		+	35	τ_{15}
J1A16			TR-36		+	36	τ_{16}
J1A17			TR-37		+	37	τ_{17}
J1A18			TR-38		+	38	τ_{18}
J1A19			TR-39		+	39	τ_{19}
J1C10	AUII-26		TR-70		+	40	τ_{20}

ING 17: ACQUISITION UNIT I (AUI)

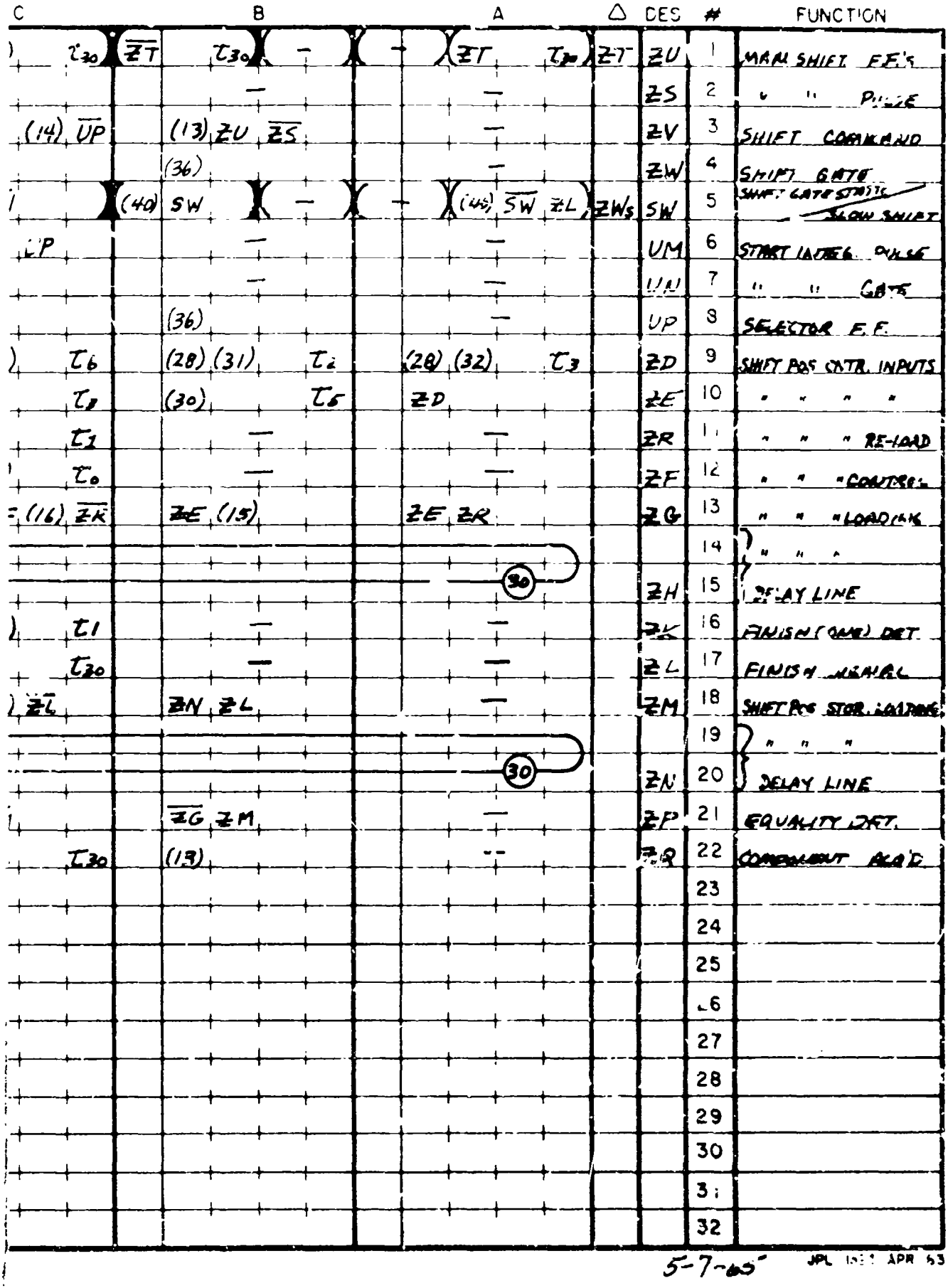



A
C
DES
#
FUNCTION
(67) T_7
(71) T_{11}
(75) T_{15}
(79) T_{19}
(11)
$\overline{UF}$ ZC
28
(59) T_0
(60) T_8
VD
VE VD
VF YB YC
(15)
30
$\overline{YC}$ YE T_0
YH (44) (43) T_1
90
UA 1 INTEG. No. INPUT
UB 2 " " "
UC 3 " " "
UD 4 " " "
UE 5 INTEG. No. COMP.
ZC 6 SAMPLE TIME
UF 7 DELAY COUNTER LOADING
UG 8 DELAY COUNT-DOWN
9 } DELAY
UH 10 } COUNTER STORAGE
UK 11 DELAY COUNT FINISHED
VA 12 VOLTAGE SERIALIZER
VB 13 " "
VC 14 " "
VD 15 " "
Δ 16
VF 17 VOLTAGE SIGN DETECTOR
VF 18 VOLTAGE ± GATE
YA 19 INTEGRATOR ADDER
YB 20 " CARRY
21 }
YC 22 } " DELAY LINE
YD 23 HI-CORRL. STROBE
24 }
YE 25 } " DELAY LINE
YF 26 MAGNITUDE COMPAR.
YG 27 TRANSFER GATE
YH 28 MAG. STORE GATE
YJ 29 STORE COMMAND
30
31
32
5-7-65
JPL 1324 APR 63

		A	B	C			FUNCTION
	•	$\overline{ZW}$	AUI-1			1	SHIFT GATE BAR
J3A08	+		J7U	RCII-19		2	SHIFT RT. MANUAL
J3A09	+		J7P	RCII-20		3	" " " BAR
	•	UN	AUI-4			4	START INTEG. GATE
	•	$\overline{UN}$	AUI-5			5	" " " BAR
						6	
						7	
						8	
	•	ZW	AUI-20			9	SHIFT GATE
	+		AUI-10			10	$\overline{T_{30}}$
	+		AUI-11			11	$\overline{T_0}$
	+		AUI-12			12	$\overline{T_1}$
	+		AUI-41	RCII-11		13	MAN. SHIFT
	+		AUI-42	RCII-12		14	MAN SHIFT BAR
	+		AUI-15			15	ACQUIRE GATE
	+		AUI-16			16	" " BAR
	+		AUI-17			17	TRANSFER GATE
	+		AUI-18			18	" " BAR
	+		AUI-19			19	DELAY COUNT FINISHED
	•	ZW_S		RCII-10		20	SHIFT GATE STATIC
			AUI-24		+	21	T_0
			AUI-63		+	22	T_2
J3A03			TR-23		+	23	T_3
J3A05			TR-25		+	24	T_5
			AUI-26		+	25	T_6
			AUI-40		+	26	T_{30}
J3B01		XC-21	J7A		+	27	NORMAL CODE
J3B02		XC-22	J7B		+	28	" " BAR
			PU-73		+	29	p3
			PU-74		+	30	p4
			PU-75		+	31	p5
			PU-76			32	p6
						33	
						34	
			AUI-62		+	35	T_1
			PU-36		+	36	ACQUIRE COMMAND
						??	
			AUI-80	ZV	•	38	SHIFT COMMAND
			PU-39	ZV	•	39	COMP. ACQ'D
			PU-40		+	40	SHIFT TIME (1) BAR

INH	D			
(2)	T_{30}	–	+	(3.
	ZS	ZU		(13) ZV
(40)	ZL $\overline{ZQ}$	(14) $\overline{SD}$		(19) $\overline{ZL}$
	ZW	$\overline{T_1}$		ZV
$\overline{ZW}$		–	+	$\overline{ZW}$
(19)	–			(19) $\overline{ZL}$
	UN	$\overline{T_1}$		UM
	UP $\overline{UM}$			ZV
	(27) (31)	T_5		(27) (32
	(29)	T_2		(29)
	ZR (16)	$\overline{T_3}$		ZK
	ZF $\overline{ZH}$	$\overline{T_0}$		ZW (16)
	ZH $\overline{ZF}$	(16) $\overline{ZR}$		$\overline{ZH}$ ZA
	$\overline{ZG}$			
	ZK $\overline{ZH}$			$\overline{ZL}$ (16
	ZL (16)			ZK
	ZN (18) $\overline{ZL}$			ZH (17
	$\overline{ZM}$			
	ZP	$\overline{T_{30}}$		ZG $\overline{ZM}$
	ZQ (16)			$\overline{ZP}$ ZL

TION UNIT II (AUII)

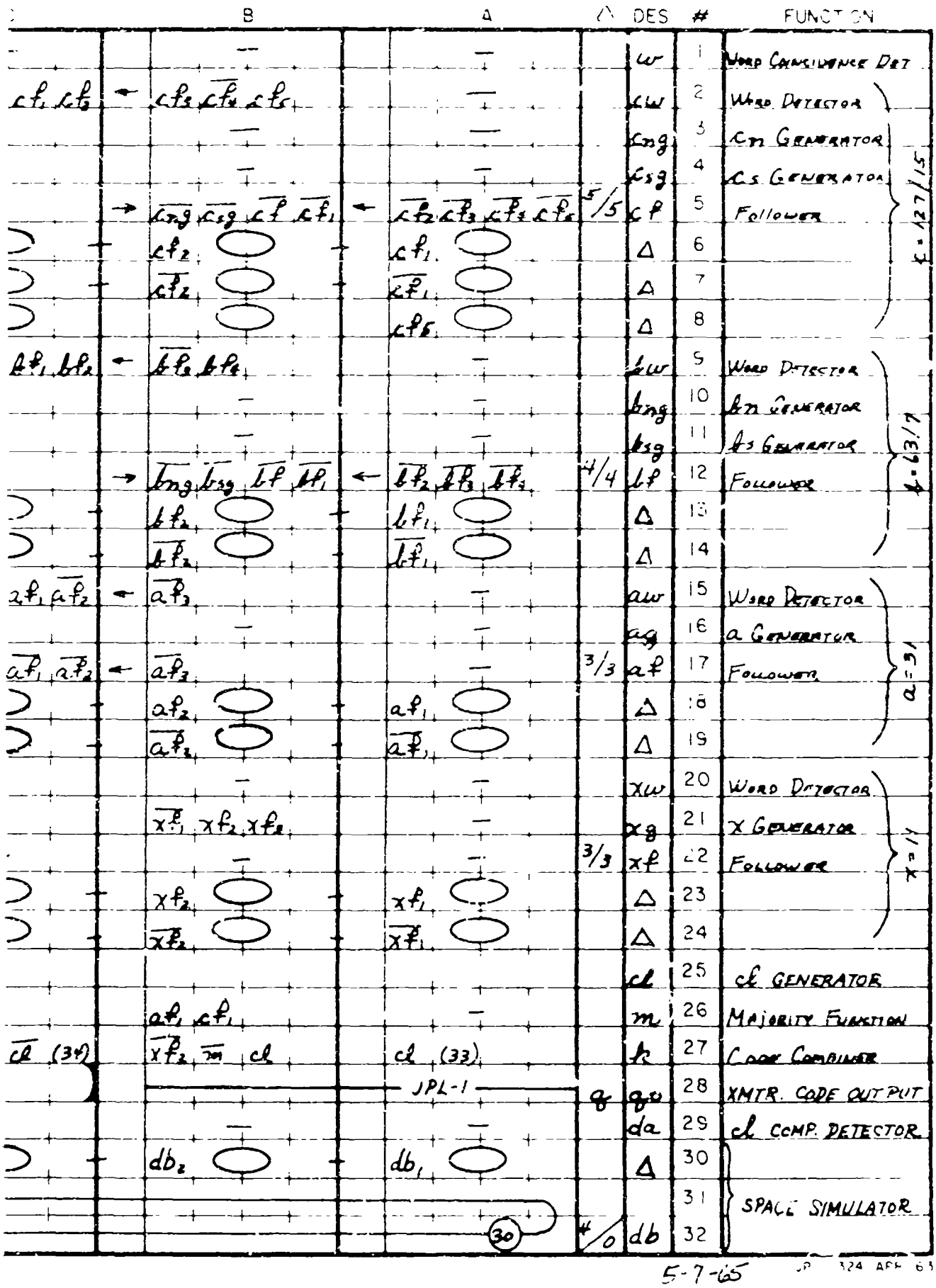


2

	A	B	C			FUNCTION
	• da_4		RCII-1		1	DELAYED XMIR CODE
					2	
					3	
					4	
					5	
					6	
					7	
	• cn_g		RCI-3		8	Cn GENERATOR
	• c_{sg}		RCI-9		9	c_s "
	• b_{ng}		RCI-10		10	b_n "
	• b_{sg}		RCI-11		11	b_s "
	• a_g		RCI-12		12	a_n "
	• x_g		RCII-13		13	x_n "
					14	
					15	
					16	
					17	
					18	
					19	
					20	
	RCI-21	AUII-27		+	21	NORMAL CODE
	RCI-22	AUII-28		+	22	" " BAR
					23	
					24	
					25	
					26	
					27	
					28	
					29	
					30	
					31	
					32	
J3B03		J5-21		+	33	CLOCK CODE
J3B04	RCII-35	J5-22		+	34	" " BAR
J3B05		J5-38		+	35	XC CN
					36	
					37	
					38	
					39	
J1C20		TR-73	QW	•	40	"31" WORD DETECTOR

INH	D		
	$cw\ \overline{cw}\ qw\ \overline{xw}$		–
	$c_{sg}\ cf\ \overline{cf_1}\ cf_2$	→	$c_{ng}\ cf$
(21)	$cf_4\ \overline{cf_5}$		$\overline{cf_4}\ \overline{cf_5}$
(22)	$cf_1\ \overline{cf_2}$		$\overline{cf_1}\ cf_2$
	c_{ng}		c_{sg}
	cf_4 ⬭	+	cf_2 ⬭
	$\overline{cf_4}$ ⬭	–	$\overline{cf_3}$ ⬭
	⬭		$\overline{cf_5}$
	$b_{sg}\ \overline{bf}\ bf_1$	→	$b_{ng}\ bf$
(21)	$bf_3\ \overline{bf_4}$		$\overline{bf_3}\ bf_4$
(22)	$bf\ \overline{bf}$		$\overline{bf}\ bf_1$
	b_{ng}		b_{sg}
	bf_4 ⬭	–	bf_2 ⬭
	$\overline{bf_4}$ ⬭	–	$\overline{bf_3}$ ⬭
	–	→	$a_g\ af$
	$af_1\ \overline{af_3}$		$\overline{af_1}\ af_3$
	a_g	→	$\overline{a_g}\ \overline{af}$
	⬭		af_2 ⬭
	⬭		$\overline{af_3}$ ⬭
	$x_g\ xf_2\ xf_3$		–
	$\overline{x_g}\ \overline{xf_2}$		$\overline{xf}\ xf_2$
	x_g		–
	⬭		xf_2 ⬭
	⬭		$\overline{xf_3}$ ⬭
			[O]
	$af_1\ bf_1$		$bf_1\ cf_1$
	$xf_2\ cl$		$\overline{xf_2}\ m$
[k	(35)	k	(33)]		–	[$\overline{k}$
	$k\ cl$		$\overline{k}\ \overline{cl}$
	db_4 ⬭	–	db_3 ⬭
	$\overline{da}$		

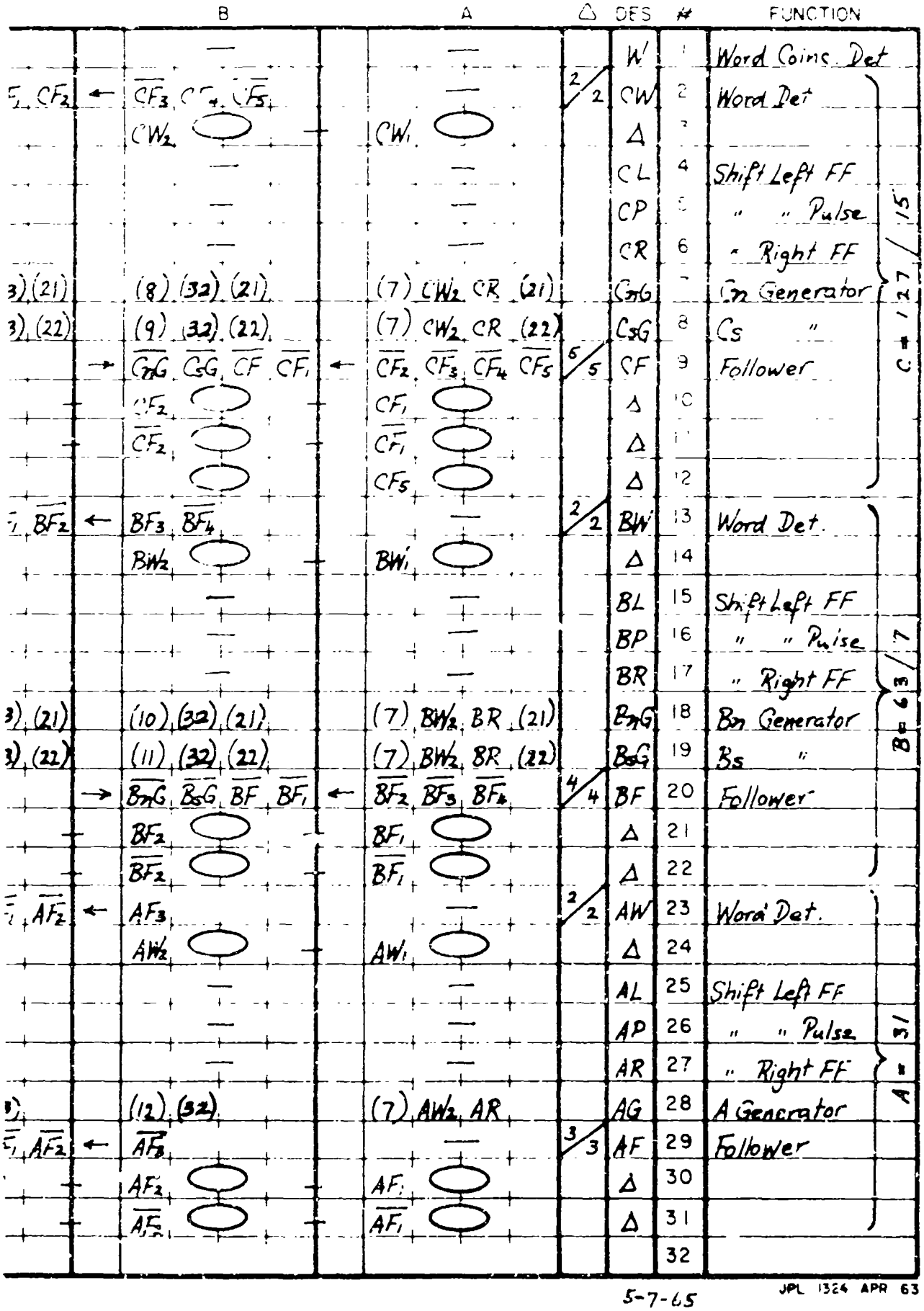
SMITTER CODER (XC)



A		B	C			FUNCTION
					1	
					2	
+			RC II - 3		3	"11" Word Detector
+			RC II - 4		4	Left Shift Cond
+			RC II - 5		5	" " " Bar
+			RC II - 6		6	Right "
+			RC II - 7		7	" " " Bar
+		XC - 8			8	α_n Generator
+		XC - 9			9	α_s Generator
+		XC - 10			10	β_n Generator
+		XC - 11			11	β_s Generator
+		XC - 12			12	α Generator
					13	
•	CF		RC II - 14		14	C Comp. Foll.
•	BF		RC II - 15		15	B " "
•	AF		RC II - 16		16	A " "
					17	
					18	
					19	
					20	
		XC - 21		+	21	Normal Code
		XC - 22		+	22	" " Bar
					23	
RC II - 24		PU - 24		+	24	$p4_S$
RC II - 25		PU - 25		+	25	$p5_S$
RC II - 26		PU - 26		+	26	$p6_S$
					27	
					28	
					29	
					30	
					31	
RC II - 33		PU 29		+	32	Sync.
RC II - 34		PU - 30		+	33	Sync. Bar
					34	
					35	
					36	
					37	
RC II - 38			AW	•	38	"31" Word Detector
					39	
					40	

INH	D		C
	CW, BW, AW (3)		—
	$C_SG, \overline{CF}, CF_1, \overline{CF_2}$	→	C_rG, CF, C
	$\overline{CW_2}$ ⬭		$\overline{CW_1}$ ⬭
	$CL, \overline{CW}$		(4) (26)
	(5) CW, CL		—
	$CR, \overline{CW_2}$		(6) (26)
$\overline{CP}$	$CF_4, \overline{CF_5}$ (33) (21)		$\overline{CF_4}, CF_5$ (3
$\overline{CP}$	$CF_1, \overline{CF_2}$ (33) (22)		$\overline{CF_1}, CF_2$ (3
	C_nG		C_sG
	CF_4 ⬭		CF_3 ⬭
	$\overline{CF_4}$ ⬭		$\overline{CF_3}$ ⬭
	⬭		$\overline{CF_5}$ ⬭
	$\overline{B_sG}, BF, \overline{BF_1}$ (22)	→	B_rG, BF, B
	$\overline{BW_2}$ ⬭		$\overline{BW_1}$ ⬭
	$BL, \overline{BW_1}$		(4) (25)
	(5) BW, BL		—
	$BR, \overline{BW_2}$		(6) (25)
$\overline{BP}$	$BF_3, \overline{BF_4}$ (33) (21)		$\overline{BF_3}, BF_4$ (3
$\overline{BP}$	$BF, \overline{BF_1}$ (33) (22)		$\overline{BF}, BF_1$ (3
	B_nG		B_sG
	BF_4 ⬭		BF_3 ⬭
	$\overline{BF_4}$ ⬭		$\overline{BF_3}$ ⬭
	—	→	$AG, AF, \overline{A}$
	$\overline{AW_2}$ ⬭		$\overline{AW_1}$ ⬭
	$AL, \overline{AW}$		(4) (24)
	(5) AW, AL		—
	$AR, \overline{AW_2}$		(6) (24)
$\overline{AP}$	$AF_1, \overline{AF_3}$ (33)		$\overline{AF_1}, AF_3$ (3
	AG	→	$\overline{AG}, \overline{AF}, \overline{A}$
	⬭		AF_3 ⬭
	⬭		$\overline{AF_3}$ ⬭

ER CODER I (RCI)



5-7-65

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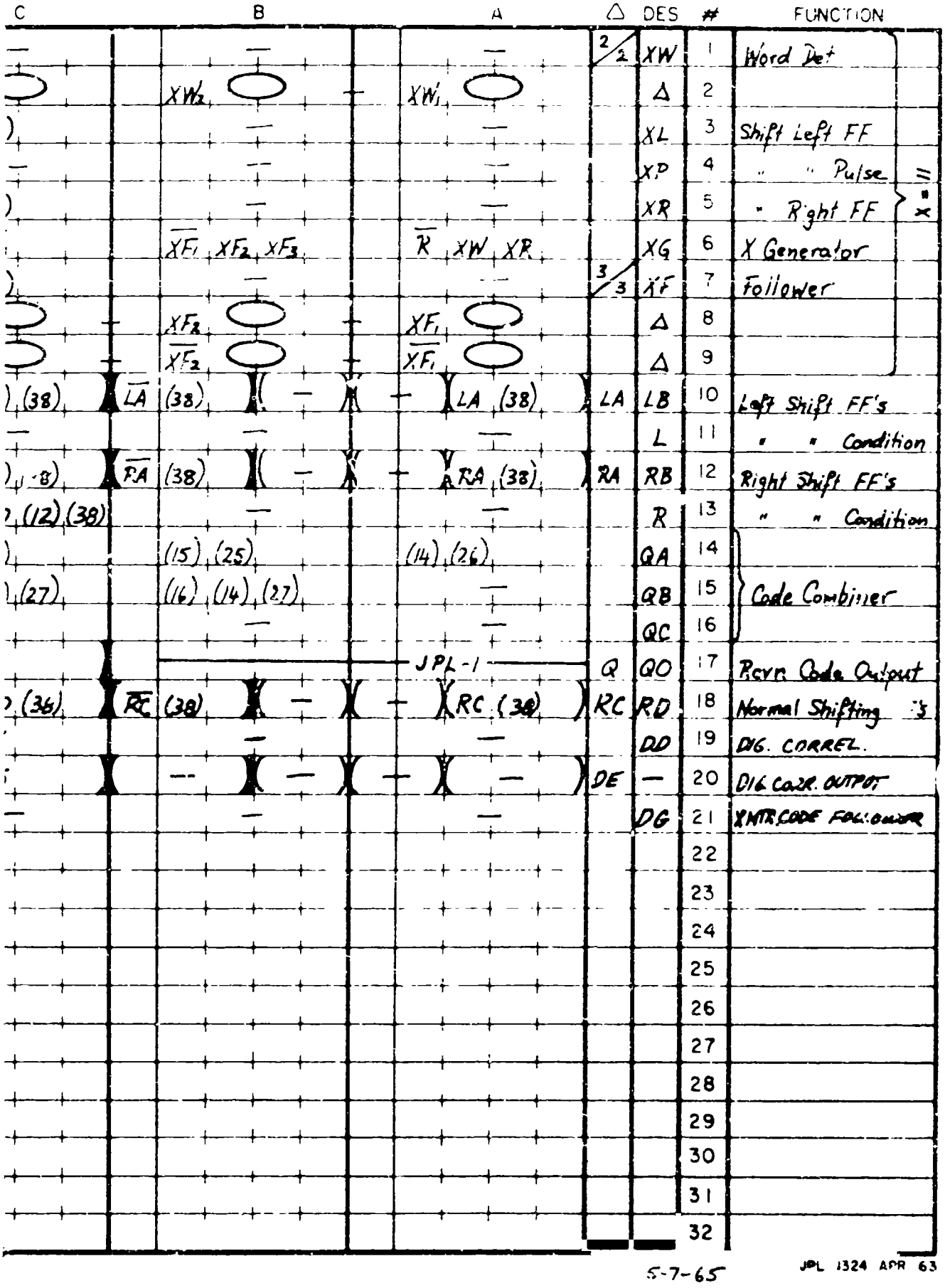
	A		B	C			FUNCTION
	+		XC-1			1	Delayed Xmtr Code
	•	$\overline{DE}$				2	DG. CORREC. OUT
	•	XW	RCI-3			3	"1" Word Det.
	•	L	RCI-4			4	Left Shift Cond
	•	$\overline{L}$	RCI-5			5	" " " Bar
	•	R	RCI-6			6	Right "
	•	$\overline{R}$	RCI-7			7	" " " Bar
						8	
						9	
	+		AUE-20			10	Shift Gate Static
	+		AUH-13			11	Man Shifting
	+		AUK-14			12	" " Bar
	+		XC-13			13	X Generator
	+		RCI-14			14	C Comp. Follower
	+		RCI-15			15	B " "
	+		RCI-16			16	A " "
J3B06	+		J7L			17	Man. Shift Left
J3B07	+		J7M			18	" " " Bar
	+		AUT-2			19	" " Right
	+		AUU-3			20	" " " Bar
						21	
						22	
			AUE-29		+	23	p3s
			RCI-24		+	24	p4s
			RCI-25		+	25	p5s
			RCI-26		+	26	p6s
			PU-27		+	27	p7s
JB04			NG-28	LA	•	28	Shift Left FFA
J1B05			NG-29	$\overline{LB}$	•	29	" " FFB Bar
J1B06			NG-30	RA	•	30	" Right FFA
J1B07			NG-31	$\overline{RB}$	•	31	" " FFB Bar
						32	
			RCI-32		+	33	Sync.
			RCI-33		+	34	" Bar
			XC-34		+	35	CLOCK BAR
						36	
						37	
			RCI-38		+	38	"31" Word Det.
						39	
						40	

INH	D		
	XG, XF_2, XF_3		
	$\overline{XW_2}$		$\overline{XW_1}$
	XL, $\overline{XW_2}$		L (23
	$\overline{L}$, XW_2, XL		
	XR, $\overline{XV}$		R (23
$\overline{XF}$	$\overline{XG}$, $\overline{XF_2}$		$\overline{XF}$, $\overline{XF_3}$
	XG (34)		(13) (33
			XF_3
			$\overline{XF_3}$
(17)	(38)		(18
	LA, $\overline{LB}$, (11) (38)		
(19)	(38)		(20
	RA, $\overline{RB}$, (11) (38)		$\overline{RC}$, RL
	(16) (23)		(16) (24
	(16) (15) (27)		(15) (14
$\overline{XF_2}$	QA		QB
QC	(35)		$\overline{QC}$
(10)	$\overline{RC}$		RL
	QC, DG		$\overline{QC}$, $\overline{DG}$
DD			$\overline{DD}$
	(1)		

ER CODER II (RCII)



	A	B	C			FUNCTION
	• $\overline{I21}$		NG-41		41	
	$\overline{I22}$		NG-42		42	
	• $\overline{I23}$				43	
	• $\overline{I24}$		NG-44		44	
	• $\overline{I25}$				45	
	• $\overline{I26}$		NG-46		46	
	• $\overline{I27}$		RT-3		47	
	• $\overline{I28}$		RT-4		48	
J2B09	• $\overline{I29}$	PU-49	UG-49		49	
J2B10	• $\overline{I30}$	PU-50	UG-50		50	
J2B20	• $\overline{I0}$	PU-46	UG-51		51	
					52	
					53	
					54	
					55	
					56	
					57	
					58	
					59	
					60	
			I21	•	61	
			I22	•	62	
	RT-36		I23	•	63	
			I24	•	64	
			I25	•	65	
	NG-38		I26	•	66	
	RT-38		I27	•	67	
	RT-39		I28	•	68	
J2C09	RR-25	PU-69	I29	•	69	
J2C10	RR-26	AUI-40	I30	•	70	
J2A20		PU-64	I0	•	71	
					72	
J2C20		XC-40		+	73	"31" Wire Diversion
					74	
					75	
					76	
					77	
					78	
					79	
					80	

	A	B	C		
J2B01	• $\overline{I1}$	PU-47	NG-1		1
	• $\overline{I2}$		" 2		2
	• $\overline{I3}$		" 3		3
	• $\overline{I4}$		" 4		4
	• $\overline{I5}$		" 5		5
	• $\overline{I6}$		" 6		6
	• $\overline{I7}$		" 7		7
	• $\overline{I8}$		" 8		8
	• $\overline{I9}$		" 9		9
	• $\overline{I10}$		" 10		10
	• $\overline{I11}$		" 11		11
	• $\overline{I12}$		" 12		12
	• $\overline{I13}$		" 13		13
	• $\overline{I14}$		" 14		14
	• $\overline{I15}$		" 15		15
	• $\overline{I16}$		" 16		16
	• $\overline{I17}$		" 17		17
	• $\overline{I18}$		" 18		18
	• $\overline{I19}$		" 19		19
	• $\overline{I20}$		" 20		20
12A01		AUI-62	I1	•	21
12A02		AUI-63	I2	•	22
12A03		AUI-23	I3	•	23
12A04		PU-66	I4	•	24
12A05		AUI-24	I5	•	25
12A06		AUI-26	I6	•	26
12A07		AUI-27	I7	•	27
2A08		AUI-28	I8	•	28
2A09		AUI-29	I9	•	29
2A10		AUI-30	I10	•	30
12A11		AUI-31	I11	•	31
12A12		AUI-32	I12	•	32
12A13		AUI-33	I13	•	33
12A14		AUI-34	I14	•	34
12A15		AUI-35	I15	•	35
12A16		AUI-36	I16	•	36
12A17		AUI-37	I17	•	37
12A18		AUI-38	I18	•	38
12A19		AUI-39	I19	•	39
			I20	•	40

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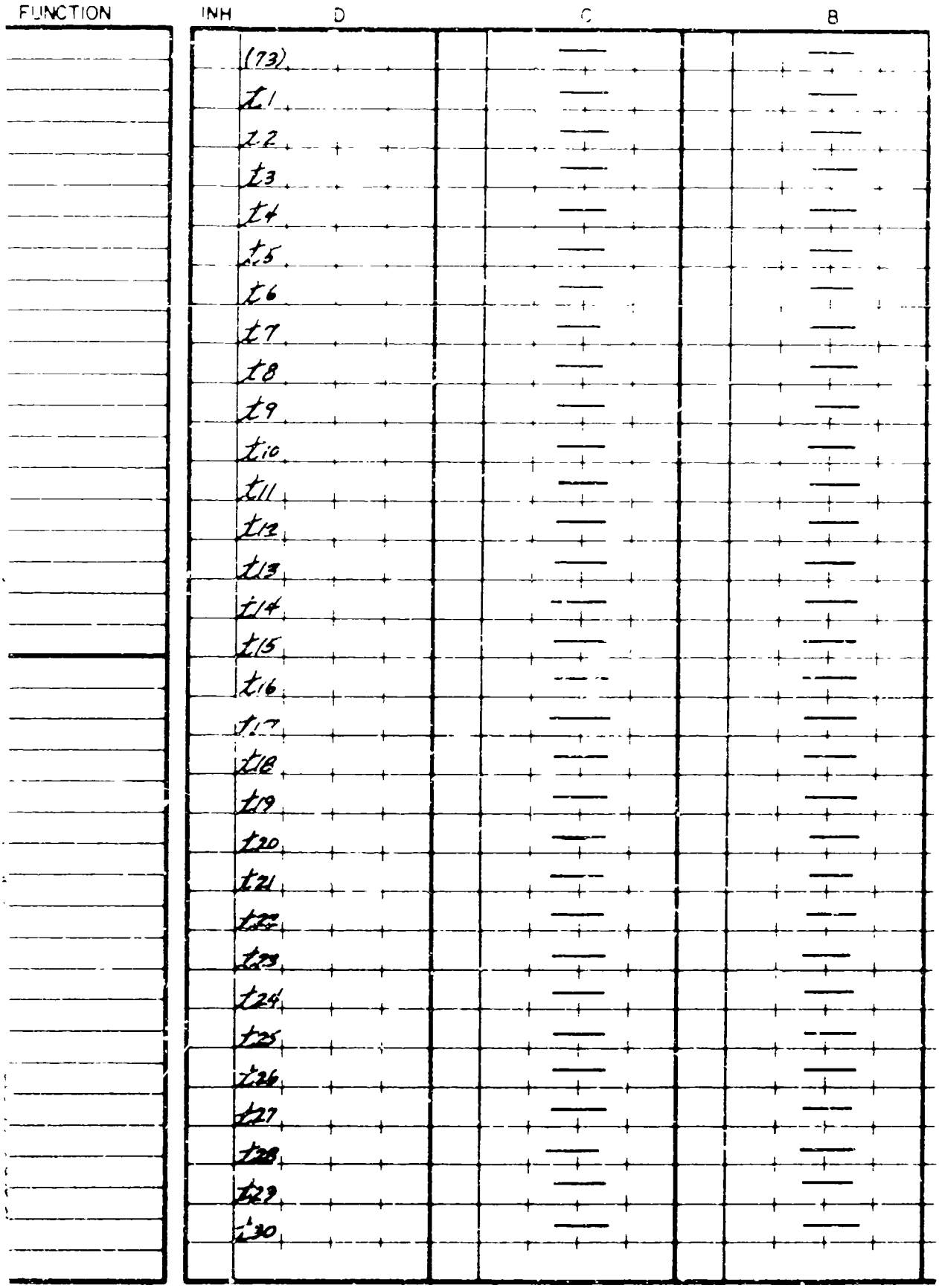
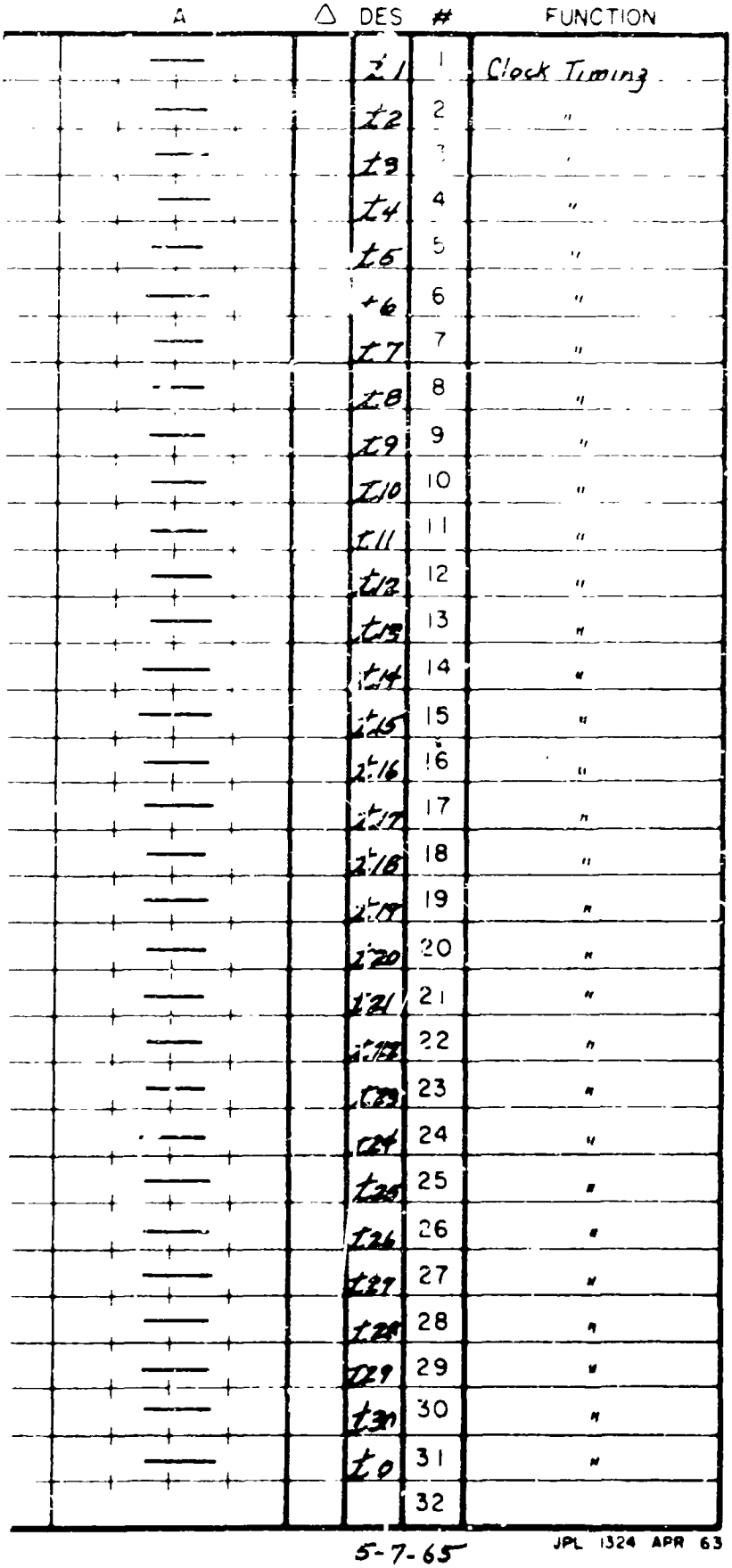
DRAWING 22: TIMER (TR)





A	△	DES	#	FUNCTION
		ϕ_1	1	Clock Timing
		t_2	2	"
		t_3	3	"
		t_4	4	"
		t_5	5	"
		t_6	6	"
		t_7	7	"
		t_8	8	"
		t_9	9	"
		t_{10}	10	"
		t_{11}	11	"
		t_{12}	12	"
		t_{13}	13	"
		t_{14}	14	"
		t_{15}	15	"
		t_{16}	16	"
		t_{17}	17	"
		t_{18}	18	"
		t_{19}	19	"
		t_{20}	20	"
		t_{21}	21	"
		t_{22}	22	"
		t_{23}	23	"
		t_{24}	24	"
		t_{25}	25	"
		t_{26}	26	"
		t_{27}	27	"
		t_{28}	28	"
		t_{29}	29	"
		t_{30}	30	"
		t_0	31	"
			32	

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		A	B	C		FUNCTION
	+		TR-41		41	$\overline{\pm 21}$
	+		TR-42		42	$\overline{\pm 22}$
					43	
	+		TR-44		44	$\overline{\pm 24}$
					45	
	+		TR-46	RT-2	46	$\overline{\pm 26}$
					47	
					48	
	+		TR-49	RT-5	49	$\overline{\pm 29}$
	+		TR-50	RR-1	50	$\overline{\pm 30}$
	+		TR-51		51	$\overline{to}$
					52	
					53	
J4C01	+		J7-E		54	Man Shifting
J4C02	+		J7-F		55	" " Bar
J2C03	+		AUI-20		56	Shift Gate
					57	
					58	
					59	
	•	Scope			60	Dopp Test Pulse
					61	
J4C08			J7Z	DZ	• 62	Clock Dopp. 0°
J4C09			J7a	DN	• 63	" " 90°
J4C10			J7V	RZ	• 64	RF Dopp. 0°
J4C11			J7U	RN	• 65	" " 90°
					66	
					67	
					68	
					69	
					70	
					71	
					72	
					73	
					74	
					75	
					76	
					77	
					78	
					79	
					80	

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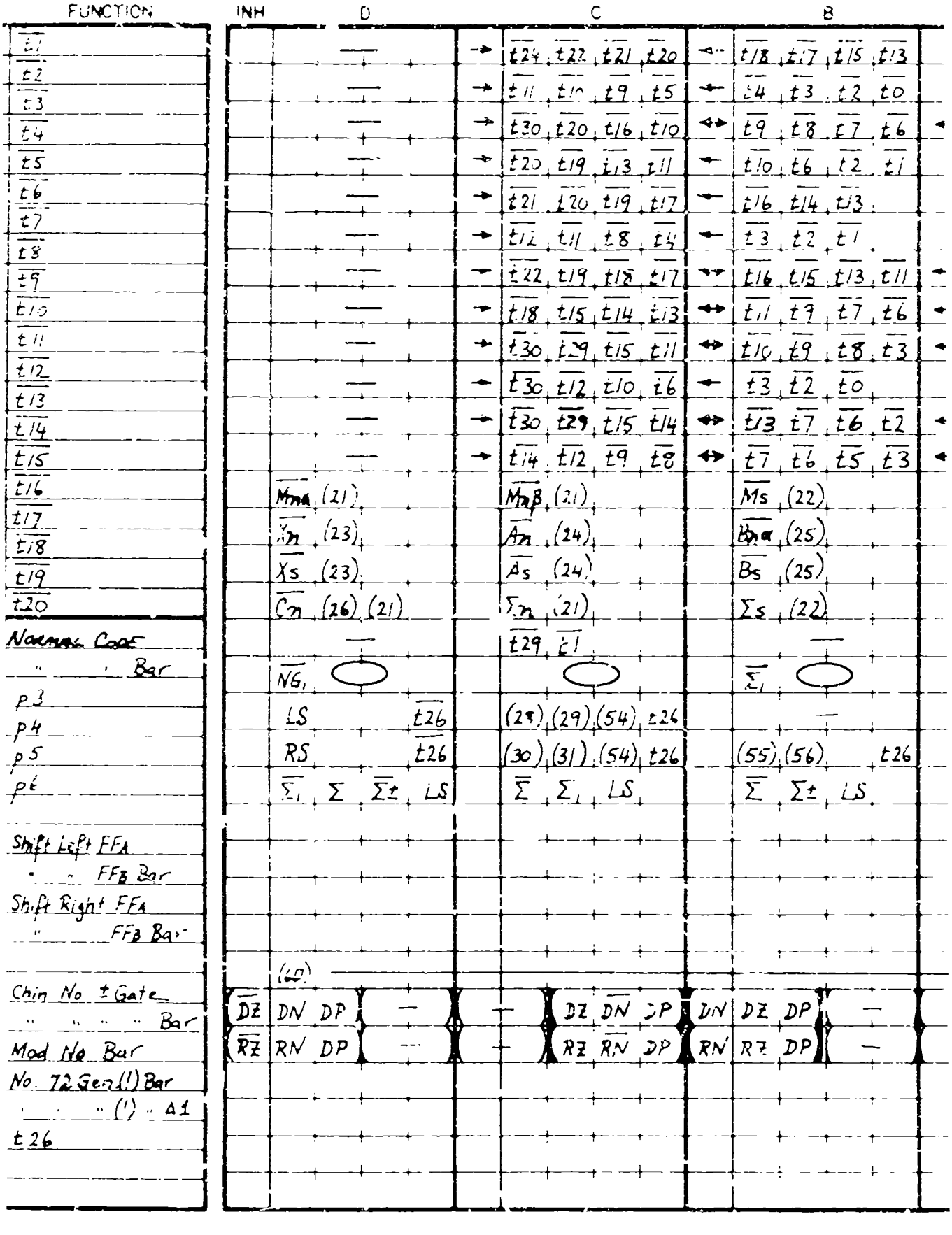
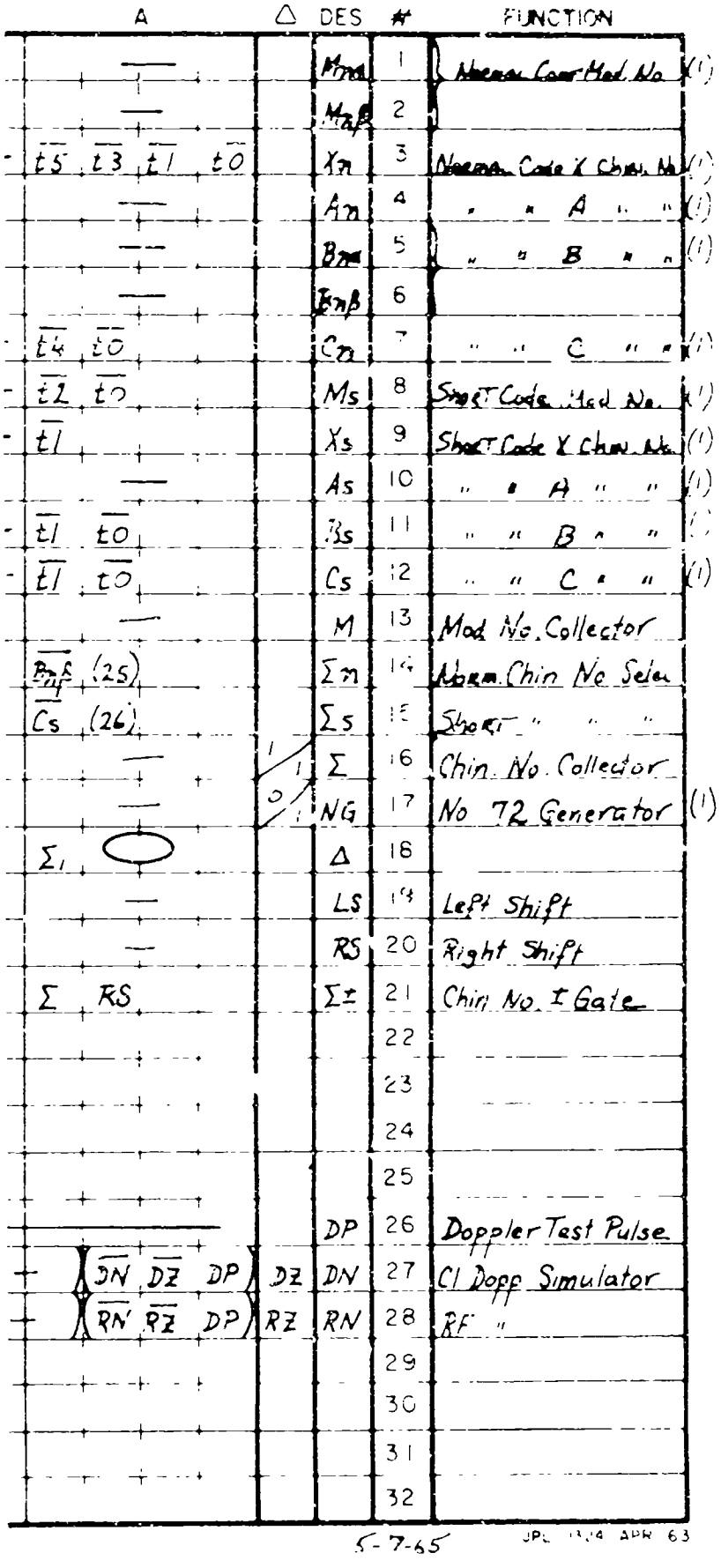
	A	B	C		
+		TR-1			1
+		TR-2			2
+		TR-3			3
+		TR-4			4
+		TR-5			5
+		TR-6			6
+		TR-7			7
+		TR-8			8
+		TR-9			9
+		TR-10	RT-1		10
+		TR-11			1
+		TR-12			12
+		TR-13			13
+		TR-14			14
+		TR-15			15
+		TR-16			16
+		TR-17			17
+		TR-18			18
+		TR-19			19
+		TR-20			20
		J7 A		+	21
		J7 B		+	22
		PU-73		+	23
		PU-74		+	24
		PU-75		+	25
		PU-76		+	26
					27
		RC II-28		+	28
		RC II-29		+	29
		RC II-30		+	30
		RC II-31		+	31
					32
RT-27			$\Sigma \pm$	•	33
RT-28			$\overline{\Sigma \pm}$	•	34
RT-29			$\overline{M}$	•	35
RT-34			$\overline{NG}$	•	36
RT-35			$\overline{NG_1}$	•	37
RT-37		TR-66		+	38
					39
					40

MC01
14C02
14C03
4C04
14C05
14C06

12B04
12B05
12B06
12B07

DRAWING 23: NUMBER GENERATOR (NG)





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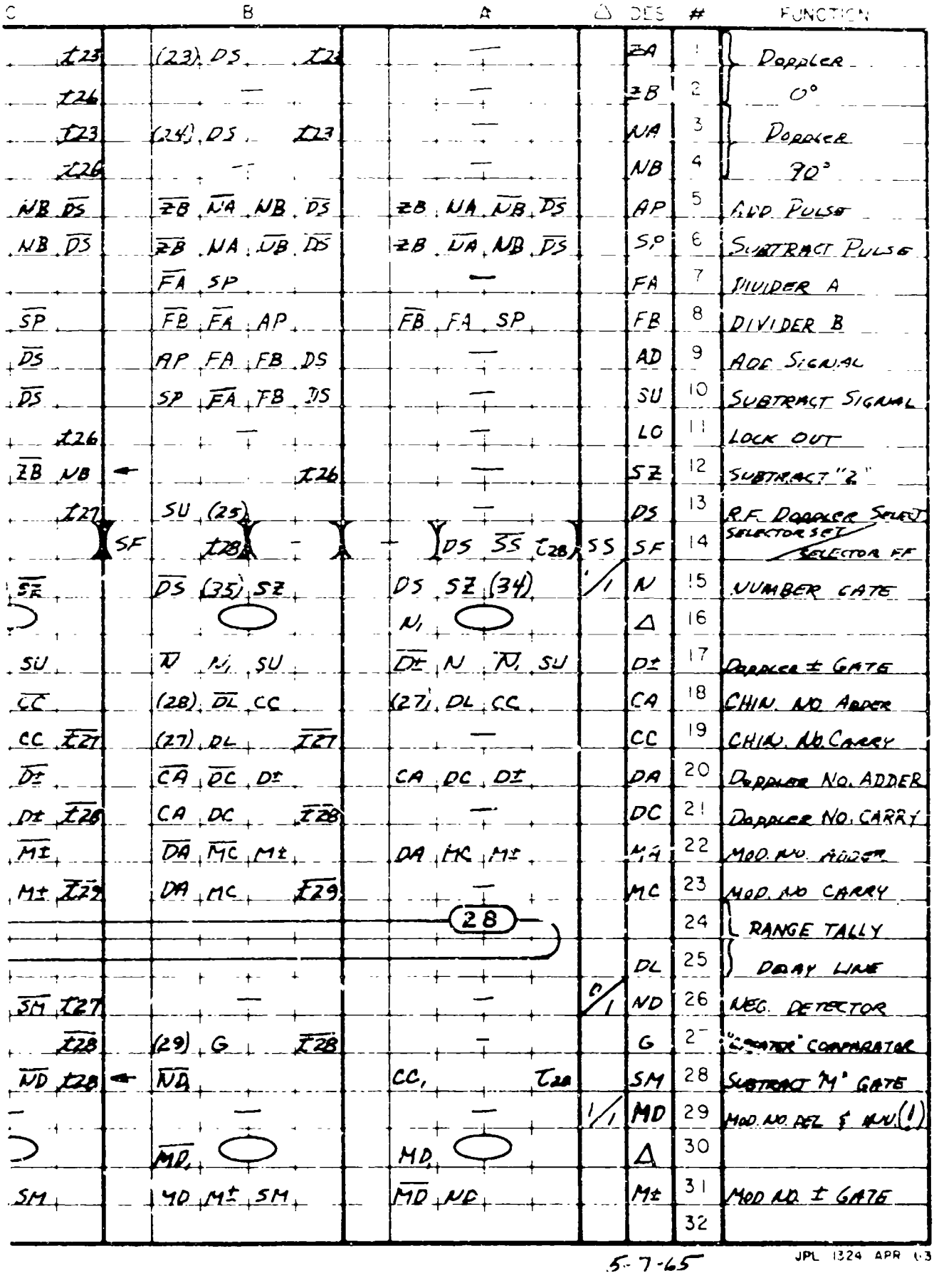
3

	A		B		C			FUNCTION
	+		NG-10				1	$\overline{I10}$
	+		NG-46				2	$\overline{I26}$
	+		TR-47				3	$\overline{I27}$
	+		TR-48				4	$\overline{I28}$
	+		UG-49				5	$\overline{I29}$
							6	
							7	
							8	
							9	
							10	
							11	
							12	
							13	
							14	
							15	
							16	
							17	
							18	
							19	
							20	
J4A03						+	21	CL DOPPLER 0°
J4A04						+	22	" " 90°
J4A05						+	23	RF " 0°
J4A06						+	24	" " 90°
J2C07			PU-37			+	25	P7
	RR-34				$\overline{SS}$		26	SELECTOR SET BAR
			NG-33			+	27	CHAN NO. ± GATE
			NG-34			+	28	" " " BAR
			NG-35			+	29	MOD AC BAR
	RR-30				MA	-	30	MOD. NO. ADDER (RANGE NO.)
	RR-31				$\overline{MA}$	-	31	" " " BAR (RANGE NO. BAR)
	RR-32				$\overline{DS}$	-	32	RF DOPP. SELECT BAR
	RR-33				DS	-	33	RF DOPP SELECT
			NG-36			+	34	NO. 72 COU BAR
			NG-37			+	35	NO 72 COU BAR DEL.
			TR-63			+	36	I23
			NG-38			+	37	I26
			TR-67			+	38	I27
	RR-24		TR-68			+	39	I28
J2C02			PU-30			+	40	SYNC. BAR

INH	D						
	ZA			$\overline{I10}$			(21) $\overline{DS}$
	ZB			$\overline{I26}$			ZA
	NA			$\overline{I10}$			(22) $\overline{DS}$
	NB			$\overline{I26}$			NA
I26	ZA	ZB	NB				$\overline{ZA}$ $\overline{ZB}$
$\overline{I26}$	$\overline{ZA}$	ZB	NB				ZA $\overline{ZB}$
	FA	$\overline{AP}$	$\overline{SP}$				$\overline{FA}$ AP
	FB	$\overline{FA}$	$\overline{AP}$				FB FA
$\overline{SF}$	AD			$\overline{I27}$			AP
$\overline{SF}$	SU			$\overline{I27}$			SP
	LO	(40)					ZA $\overline{ZB}$
	SZ			$\overline{I26}$	→		$\overline{LO}$ ZA
LO	DS	(25)					AD (25)
DS		$\overline{I28}$					$\overline{DS}$
LO	DS	$\overline{SL}$		$\overline{I27}$			$\overline{DS}$ (34)
	CC,	⬭					$\overline{N}$, (
	N	AD	$\overline{SU}$				D± $\overline{N}$
(40)	(27)	DL	$\overline{CC}$				(28) DL
(40)	(28)	DL	CC	$\overline{I27}$			(27) $\overline{DL}$
	CA	$\overline{DC}$	$\overline{DI}$				$\overline{CA}$ DC
	$\overline{CA}$	DC	DI	$\overline{I28}$			CA $\overline{DC}$
(40)	DA	MC	$\overline{M\pm}$				$\overline{DA}$ MC
(40)	$\overline{DA}$	MC	M±	$\overline{I29}$			DA $\overline{MC}$
	$\overline{MA}$						
	ND			$\overline{I27}$			DL $\overline{ND}$
	DL	(29)					DL G
	SM			$\overline{I28}$	→		G $\overline{SM}$
	(29)						
		⬭					$\overline{ND}$, (
	MD,	$\overline{MD}$	$\overline{M\pm}$	SM			MD $\overline{MD}$

NGE TALLY (RT)


C
B
A
△ DES
#
FUNCTION
ZA 1 DOPPLER
ZB 2 0°
NA 3 DOPPLER
NB 4 90°
AP 5 ADD PULSE
SP 6 SUBTRACT PULSE
FA 7 DIVIDER A
FB 8 DIVIDER B
AD 9 ADD SIGNAL
SU 10 SUBTRACT SIGNAL
LO 11 LOCK OUT
SZ 12 SUBTRACT "2"
DS 13 R.F. DOPPLER SELECT
SF 14 SELECTOR SET / SELECTOR FF
N 15 NUMBER GATE
Δ 16
D± 17 DOPPLER ± GATE
CA 18 CHAN. NO. ADDER
CC 19 CHAN. NO. CARRY
DA 20 DOPPLER NO. ADDER
DC 21 DOPPLER NO. CARRY
MA 22 MOD NO. ADDER
MC 23 MOD NO CARRY
24 RANGE TALLY
DL 25 DELAY LINE
ND 26 NEG. DETECTOR
G 27 "0" GATE COMPARATOR
SM 28 SUBTRACT "M" GATE
MD 29 MOD NO. DEL & ADV. (1)
Δ 30
M± 31 MOD NO. ± GATE
32
28
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OUTPUT RELAYS CABLE A

01	DATA BIT	28	KD4
10	" "	"	KD4
02	" "	27	KD3
20	" "	"	KD3
03	" "	26	KD2
30	" "	"	KD2
04	" "	25	KD1
40	" "	"	KD1
05	" "	24	KE4
50	" "	"	KE4
06	" "	23	KE3
60	" "	"	KE3
09	" "	22	KE2
90	" "	"	KE2
12	" "	21	KE1
21	" "	"	KE1
15	" "	20	KF4
51	" "	"	KF4
23	" "	19	KF3
32	" "	"	KF3
24	" "	18	KF2
42	" "	"	KF2
25	" "	17	KF1
52	" "	"	KF1
26	" "	16	KG4
62	" "	"	KG4
29	" "	15	KG3
92	" "	"	KG3
35	" "	14	KG2
53	" "	"	KG2
45	" "	13	KG1
54	" "	"	KG1
56	" "	12	KH4
65	" "	"	KH4
59	" "	11	KH3
95	" "	"	KH3
79	" "	10	KH2
97	" "	"	KH2

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OUTPUT RELAYS CABLE B

01	DATA BIT	10	KH1
10	" "	"	KH1
02	" "	9	KJ4
20	" "	"	KJ4
03	" "	8	KJ3
30	" "	"	KJ3
04	" "	7	KJ2
40	" "	"	KJ2
05	" "	6	KJ1
50	" "	"	KJ1
06	" "	5	KK4
60	" "	"	KK4
09	" "	4	KK3
90	" "	"	KK3
12	" "	3	KK2
21	" "	"	KK2
15	" "	2	KK1
51	" "	"	KK1
23	" "	1	KL4
32	" "	"	KL4
24	" "	0	KL3
42	" "	"	KL3
25	DATA GOOD BIT		KL2
52	" "	"	KL2
26	ODD EVEN BIT		KL1
62	" "	"	KL1
29			
92			
35			
53			
45			
54			
56			
65			
59			
95			
79			
97			

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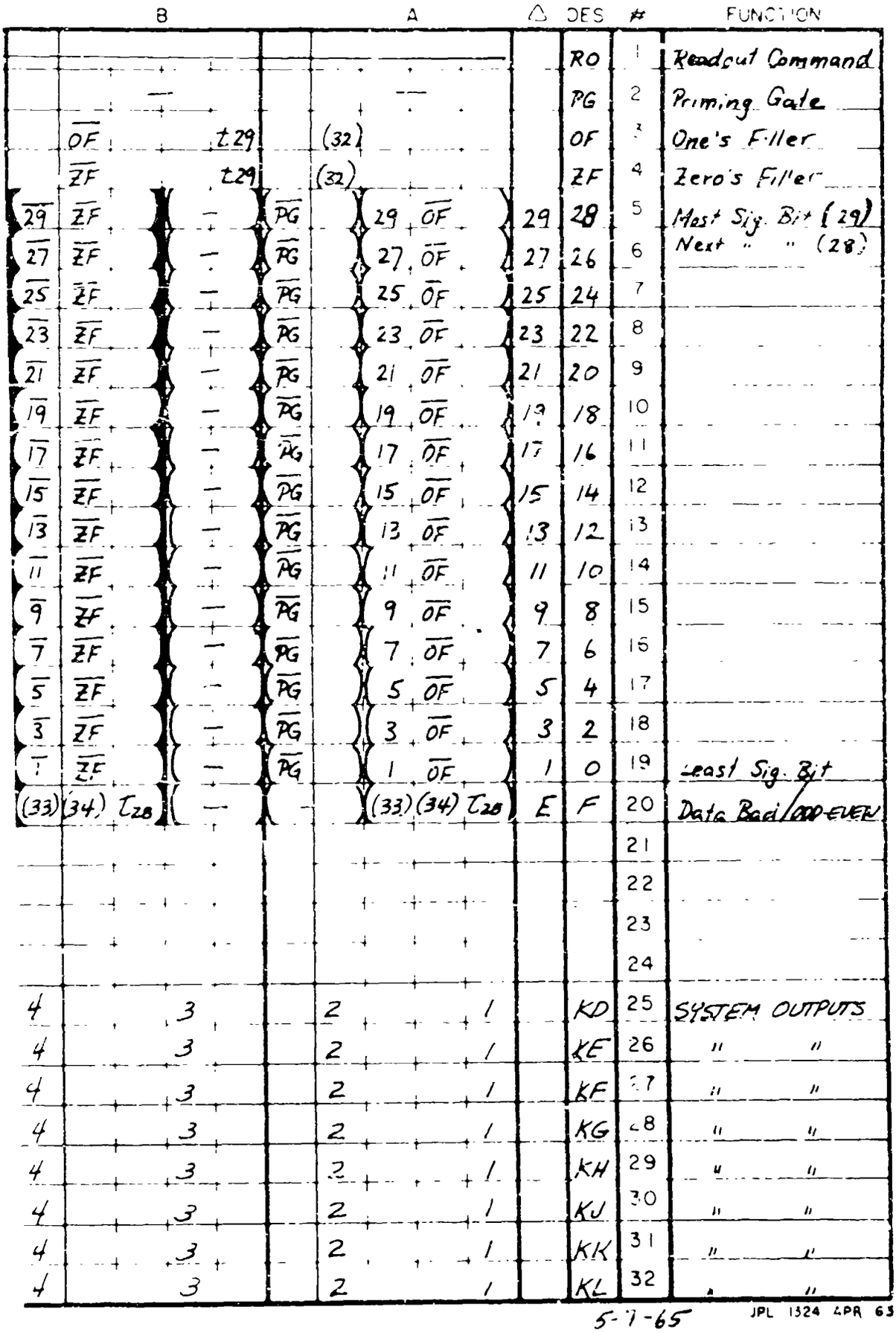
DRAWING 25: READ OUT REGISTER (RR)

A	B	C			FUNCTION
+		NG -50		1	$\overline{t30}$
				2	
				3	
				4	
				5	
				6	
				7	
				8	
				9	
				10	
				11	
				12	
				13	
				14	
				15	
				16	
				17	
				18	
				19	
				20	
				21	
				22	
				23	
	RT-39		+	24	t 28
	TR-69		+	25	t 29
	TR-70		+	26	t 30
				27	
				28	
				29	
	RT-30		+	30	Mod No Adder (Range No.)
	RT-31		+	31	" " " Bar (Range No. Bar)
	RT-32		+	32	RF Dopp Select Bar
	RT-33		+	33	RF Dopp. Select
	RT-26		+	34	Selector Set Bar
				35	
				36	
				37	
				38	
				39	
				40	

INH	D		C	
	PG	$\overline{R0}$	$\overline{PG}$	$\overline{t30}$
	OF	PG	OF	$\overline{t30}$
	ZF	PG	ZF	$\overline{t30}$
(31)	$\overline{OF}$	$\overline{PG}$	(30) $\overline{ZF}$	
28	$\overline{OF}$	$\overline{PG}$	28 $\overline{ZF}$	
26	$\overline{OF}$	$\overline{PG}$	26 $\overline{ZF}$	
24	$\overline{OF}$	$\overline{PG}$	24 $\overline{ZF}$	
22	$\overline{OF}$	$\overline{PG}$	22 $\overline{ZF}$	
20	$\overline{OF}$	$\overline{PG}$	20 $\overline{ZF}$	
18	$\overline{OF}$	$\overline{PG}$	18 $\overline{ZF}$	
16	$\overline{OF}$	$\overline{PG}$	16 $\overline{ZF}$	
14	$\overline{OF}$	$\overline{PG}$	14 $\overline{ZF}$	
12	$\overline{OF}$	$\overline{PG}$	12 $\overline{ZF}$	
10	$\overline{OF}$	$\overline{PG}$	10 $\overline{ZF}$	
8	$\overline{OF}$	$\overline{PG}$	8 $\overline{ZF}$	
6	$\overline{OF}$	$\overline{PG}$	6 $\overline{ZF}$	
4	$\overline{OF}$	$\overline{PG}$	4 $\overline{ZF}$	
2	$\overline{OF}$	$\overline{PG}$	2 $\overline{ZF}$	
$\overline{0}$	$\overline{OF}$	$\overline{PG}$	0 $\overline{ZF}$	
	$\overline{29}$	$\overline{28}$	$\overline{27}$	$\overline{26}$
	$\overline{25}$	$\overline{24}$	$\overline{23}$	$\overline{22}$
	$\overline{21}$	$\overline{20}$	$\overline{19}$	$\overline{18}$
	$\overline{17}$	$\overline{16}$	$\overline{15}$	$\overline{14}$
	$\overline{13}$	$\overline{12}$	$\overline{11}$	$\overline{10}$
	$\overline{9}$	$\overline{8}$	$\overline{7}$	$\overline{6}$
	$\overline{5}$	$\overline{4}$	$\overline{3}$	$\overline{2}$
	$\overline{1}$	$\overline{0}$	$\overline{E}$	$\overline{F}$


B
A
△ DES
#
FUNCTION
RO 1 Readout Command
PG 2 Priming Gate
OF 3 One's Filler
ZF 4 Zero's Filler
29 ZF PG 29 OF 29 28 5 Most Sig. Bit (29)
27 ZF PG 27 OF 27 26 6 Next " " (28)
25 ZF PG 25 OF 25 24 7
23 ZF PG 23 OF 23 22 8
21 ZF PG 21 OF 21 20 9
19 ZF PG 19 OF 19 18 10
17 ZF PG 17 OF 17 16 11
15 ZF PG 15 OF 15 14 12
13 ZF PG 13 OF 13 12 13
11 ZF PG 11 OF 11 10 14
9 ZF PG 9 OF 9 8 15
7 ZF PG 7 OF 7 6 16
5 ZF PG 5 OF 5 4 17
3 ZF PG 3 OF 3 2 18
1 ZF PG 1 OF 1 0 19 Least Sig. Bit
(33)(34) t28 (33)(34) t28 E F 20 Data Bad/00 EVEN
21
22
23
24
4 3 2 1 KD 25 SYSTEM OUTPUTS
4 3 2 1 KE 26 " "
4 3 2 1 KF 27 " "
4 3 2 1 KG 28 " "
4 3 2 1 KH 29 " "
4 3 2 1 KJ 30 " "
4 3 2 1 KK 31 " "
4 3 2 1 KL 32 " "
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