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FINAL REPORT

OPTIMIZATION STUDY OF HIGH POWER STATIC INVERTERS AND CONVERTERS

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TRW EQUIPMENT LABORATORIES

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SUMMARY

The purpose of this study program was to develop high performance static inverter and converter conceptual designs that will fulfill the present and projected requirements for various space applications. High efficiency, high power to weight ratios, and high reliability were the three design goals that were used to optimize these conceptual designs. Since optimizing one or two of these design goals usually degrades the third, a reasonable compromise must be made among the three design goals. The most feasible circuit techniques and advanced circuit components were used to obtain an optimum mix for these three design goals so that high performance static inverter and converter conceptual designs can be realized for the various space applications.

The power range that was to be examined covered the range of 100 watts to 10,000 watts with operating frequencies of 400 cps to 3200 cps. However, a program redirection was instituted later in this program which directed all efforts toward the development of an optimum design for a 3200 cps - 10 KW inverter and a 400 cps - 10 KW inverter in place of the low and medium power inverter and converter requirements that were originally specified. Certain ground rules and a Methodology Plan were established so that the multitude of performance parameters for these inverters and converters could be correlated in order to obtain these optimum conceptual designs. With the basic set of performance specifications for these conceptual designs established, the first phase of this study was directed toward a selection of the most feasible approach for each inverter application. The primary consideration was a selection of the inverter power stage. Therefore, an investigation was conducted on existing designs for both series and parallel inverters so that their operating ranges and their inherent advantages and limitations could be established. Both these inverter types were designed to use transistors or silicon controlled rectifiers as their switching elements with the series inverters using the silicon controlled rectifiers almost exclusively. The maximum useful load range for the series inverter was limited to approximately 3 to 1. Therefore, no further effort was devoted to these series inverters.

The basic parallel inverter designs were investigated next. A typical parallel inverter of the McMurray-Bedford type was analyzed in detail in order to show that it will start and operate under a wide range of load magnitudes and power factors. A detailed mathematical analysis of this parallel inverter is included in the Appendix in order to verify these results and to allow the reader to fully understand the complex sequence of operations which occur in inverter circuits. A general review of various methods of voltage regulation were discussed with the purpose of defining which method of voltage regulation was most suitable for a specific application. Design problems encountered with the different methods of regulation were also included. Various methods of reducing

harmonic distortion are outlined in this section in an attempt to determine which method would offer the least circuit complexity and minimum filter weight and size.

Two general design approaches were obtained from this preliminary investigation that would satisfy the requirements for high performance static inverters. They were high frequency pulse width modulation techniques and stepped wave techniques. These approaches were considered for the 3200 cps - 10KW inverter and 400 cps - 10KW inverter designs.

The second section of this report concentrated on the problems of the 3200 cps - 10KW static inverter since its design appeared to be the most difficult and neither of the two design approaches seemed to offer a clear advantage.

Many switching devices (silicon and germanium transistors, SCR's, and gate controlled switches) were investigated to determine their compatibility when used with either design approach. The results of this investigation revealed that the stepped waveform approach using silicon power transistors would be the most practical means of making a 3200 cps - 10KW inverter. The pulse width modulation techniques had to be disregarded because switching devices of sufficient current capacity and switching speeds could not be found that would make this approach feasible at this operating frequency of 3200 cps.

An analysis was performed on various stepped waveforms in order to obtain a maximum amount of harmonic reduction for a minimum amount of circuit complexity. The suitability of each waveform for this three-phase inverter was investigated from the standpoint of the number of inverter stages required; the applicability to Delta connections; and the number of different transformers required. The results of this analysis revealed that a twelve step waveform requiring six inverters per phase would be an optimum choice.

The magnetic components for this 3200 cps - 10KW static inverter approach were considered after the selection of this multi-stepped waveform in order to obtain optimum component designs. The loading characteristics of fixed transformers were considered in order to develop a general set of equations that can be used to scale optimum transformer designs to different power levels without resorting to extensive calculations. In addition, relationships between the size, weight, and loss of both single-phase and multi-phase transformer designs were established. The analysis of transformer optimization was expanded to include its associated circuitry when the three-phase power output transformers were considered. Flux cancellation was used wherever possible in the design of this multi-phase output transformer in order to minimize its weight and losses. The resulting output transformer design contained twelve windows arranged in two rows of six for use with the twelve-step waveform.

Using this information the design of the 3200 cps - 10 KW power output transformer was detailed. The advantages and disadvantages of various transformer configurations, core materials, use of shunts for current limiting, and use of holes in the transformer core for current balancing were considered. Three optimum output power transformers using Square Permalloy 80, Orthonol, and Supermendur core materials were designed.

The rest of the 3200 cps - 10 KW inverter power stages were then considered in detail with emphasis being placed on the transistor switch drive scheme and the AC output filter configuration that will be used.

Current feedback was selected to minimize the power transistor base drive losses while a timing core was used in each transistor switch pair to eliminate their "turn on" losses. A total savings of 392 watts was realized with the use of these two schemes. The resulting AC output filter configuration contained a series tank circuit in series with the load and a parallel tank shunting the load. The four filter components were determined so that no harmonic would exceed 2%.

A complete theoretical design of the low level logic circuitry was made for this 3200 cps - 10 KW inverter including schematics and parts lists. This completed the detailed theoretical design for this 3200 cps - 10 KW static inverter. Its component weight and overall efficiency were estimated to be 41.5 pounds and 92% at full load.

A reliability study was performed on the electrical circuitry and their parts for the proposed 3200 cps - 10 KW static inverter design. The results of this reliability study could only be used as a guide since this circuitry was created from a theoretical design with no actual stress measurements being taken. These results indicated that this inverter design would have a reliability of .963506 and .718930 for one month and one year continuous operation respectively. The reliability figures of merit can be improved with the use of redundant circuitry and components that have larger derating factors.

The last area of investigation for this static inverter involved scaling its weight, losses, and reliability with respect to reduced power level, DC input voltage, harmonic distortion, output phase separation, voltage regulation, and DC input variations. The effects of scaling this inverter with respect to reduced power level and DC input voltage were of primary interest since a multitude of circuit and component changes will occur. The AC filter components were effected most by scaling this inverter with respect to harmonic distortion, output phase separation, voltage regulation and DC input variations. No large component changes were observed for this scaling except when separate voltage regulators were required for each phase when the voltage regulation tolerance was reduced below ±2%.

The last section of this report was devoted to the design of the 400 cps - 10 KW static inverter. Both the multi-stepped waveform techniques and the pulse width modulation techniques were considered for this inverter design. The information obtained for the selection of the 3200 cps - 10 KW inverter approach was used again as an aid toward selecting the best approach for this 400 cps - 10 KW static inverter. The pulse width modulation scheme was selected for this inverter because an estimated weight savings of 54 pounds could be realized with only a slight sacrifice in efficiency as compared with an equivalent multi-stepped waveform inverter. In addition, the pulse width modulation approach does not require a bulky power output transformer. The elimination of the power output transformer allows the power output stages to be readily adaptable to modular construction. The modular construction techniques allow these power output stages to be easily scaled to any power capacity by adding or removing the transistor switch leg modules which are connected in parallel for each half phase.

A detailed investigation of the various high frequency pulse width modulation techniques was made to determine which one would produce waveforms with low total harmonic content with relatively simple inverter circuitry. The results of this investigation revealed that classical pulse width modulation with natural sampling required the least amount of circuit complexity and would use a simple and light-weight AC filter. The other pulse width modulation techniques (Classical PWM with uniform sampling, commutated PWM with uniform sampling, and commutated PWM with natural sampling), required either large AC filters with comparable circuit complexity or more complex circuitry with comparable AC filter size and weight. The classical pulse width modulation with natural sampling required a minimum practical carrier frequency of twenty-five times the fundamental or 10 KC so that the frequencies of the carrier and its harmonics and sidebands would be high enough to allow lightweight filter components to be used. Therefore switching components with high voltage, high current, and very fast switching times were required for these output stages. Fast switching times were essential in order to minimize the switching losses that will occur at this 10 KC carrier frequency. Medium power silicon transistors (10 A) with high voltage ratings and extremely fast switching times ($\sim 2\ \mu s$) were available and were found to be the most efficient switching components for these power output stages. Because a minimum safety factor margin of two was used for a design goal, two of these switching transistors must be connected in series to provide an adequate voltage safety margin. In addition, fifteen pairs of these series connected transistors must be connected in parallel for each half phase in order to supply the necessary capacity for 250% overload conditions. (There are a total of six half-phases that will be used to make up the three phase wye connected output for this inverter).

In order to build a transformerless inverter, the input voltage to the power stages must be bi-polar and have sufficient magnitude to produce the required three-phase output voltages. Therefore, a DC-DC converter will usually be required for relatively low voltage sources to step-up the voltage to this desired bi-polar DC voltage level. In addition, this DC-DC converter will be used to regulate the source voltage.

A complete theoretical design for the low level logic circuitry, the power stages, and the DC-DC converter was made for this 400 cps - 10 KW static inverter. Both schematics and parts lists were generated from this theoretical design. The overall component weight and efficiency were then determined for this proposed conceptual inverter design. Its total component weight was found to be 147.54 pounds while its total full load efficiency was estimated to be 80.4%.

A reliability study was performed on the electrical circuitry and their parts for the proposed 400 cps - 10 KW static inverter design. Again, the results of this reliability study could only be used as a guide since the stress levels of each electrical component were calculated with no actual stress measurements being taken. The same generic failure rates, derating factors, and environmental conditions used for the electrical components for the 3200 cps - 10 KW reliability analysis were used again. A certain amount of redundancy was found in the power output stages depending on its mode of failure and the permissible maximum current allowed. Therefore, the reliability figure of merit for the proposed conceptual inverter design was determined for each of these power stage failure modes. Using a suitable protective device such as fuses in each of the transistor switch legs will eliminate the worst failure mode. (Both switching transistors connected in series for one switch leg that fails in the shorted mode, thus shorting out a half phase and causing possible damage to the DC-DC converter.)

The use of redundant circuitry in circuits with the largest failure rates will considerably improve the reliability of this proposed 400 cps - 10 KW static inverter.

The results of this "Optimization Study of High Power Static Inverters and Converters" has produced two conceptual designs for both 400 cps and 3200 cps 10 KW static inverters. A complete set of schematics and parts lists have been generated from these theoretical designs. In addition, reliability, efficiency, and weight have been calculated for these two designs. A more detailed discussion and analysis of these inverter designs is given in the introduction and body of this report.

INTRODUCTION

The overall objective of this high power static inverter optimization study program was to develop conceptual designs for efficient, lightweight and highly reliable static power conversion units up to ratings of 10 kilowatts. These inverters would be used for auxiliary electric power systems required for present and future space applications. The considerations which entered the design of these inverters included the performance requirements of the load, the regulation of the DC source, the method of inversion, the environment with its thermal and radiation problems, and weight restrictions. When the general technique had been determined, the resultant circuit designs for the inverters were developed with efficiency, power to weight ratio, and reliability as key criteria.

High efficiency was desired in order to provide maximum power transfer between the source, which usually has a limited amount of power, and the load. An increase in efficiency will also allow a decrease in the amount of heat sink weight and volume required for a particular inverter design. High power to weight ratios for these space inverters must be a major design objective in order to obtain more useful payload weight for a given launch vehicle thrust. A high reliability figure is manditory in order to provide long trouble-free service under the most adverse environmental conditions. However, for space applications where it is usually impossible to carry spare units or to perform routine maintenance for unmanned missions, the aspect of inherent reliability must be weighted heavily against efficiency, and power to weight ratios in order to achieve an optimum inverter design. It was a purpose of this study to explore the interrelations of these various aspects of the space power conditioning problem in an effort to determine the most feasible techniques to fulfill the present and projected requirements for high power space static inversion and conversion equipments.

In order to correlate the multitude of performance parameters for the inverters and their interrelationship with the components and the circuitry required for an optimum design, certain ground rules were established. These ground rules determined the best methods of evaluating the components and techniques so that the wide range of choice could be narrowed to a few selected approaches. The quantities of primary concern in this optimization study are listed below in three groups of the Methodology Plan.

METHODOLOGY PLAN

GROUP I Nominal Description of the Inverter

a) Full load volt-amperes (va) in a specified power factor range.
b) Frequency
c) Number of phases
d) DC input voltage

GROUP II Performance Specifications

a) Harmonic distortion
b) Variation of DC input voltage around nominal
c) High frequency transients on DC input
d) Output voltage
e) Output voltage regulation, steady state and transient
f) Output phase separation
g) Output short circuit protection
h) Overload capability
i) Unbalanced load capability
j) Output frequency regulation

GROUP III Parameters to be Optimized

a) Weight
b) Efficiency
c) Reliability

This list, while not all inclusive, does contain the quantities which are of primary concern to the electrical design of an inverter. They were split into three separate groups. These particular groups were selected in conjunction with the proposed ground rules which are discussed next.

Group I determines the nominal requirements of the inverter. At the beginning of this program it was proposed that these characteristics be limited to the following ranges for three inverter types:

GROUP I	TYPE A	TYPE B	TYPE C
Watt range	100 to 500 at 1.0 to .7 lag power factor	500 to 2000 1.0 to .7 lag power factor	2000 to 10,000 1.0 to .7 lag power factor
Frequency	400	400	3200
Number of Phases	3	3	3
Range of DC Input Voltage	15 to 100	15 to 100	15 to 100

A program redirection was instituted later in this program which directed all efforts toward the development of an optimum design for (a) a 3200 cps, 10 KW inverter and (b) a 400 cps, 10 KW inverter, in place of the low and medium power 400 cps inverter requirements that were originally specified.

The range of 15 to 100 volts was selected as the probable limits of DC voltage sources that would become standard in the future. For the conceptual designs 56 VDC was selected as the most feasible input voltage. Scaling techniques were developed which then allowed the system designer to see the variations in weight and efficiency that attended a change in VDC nominal. The selected inverter techniques will be capable of accepting a nominal (+10%, -20%) voltage within these DC limits without a change in the general configuration. The choice of specific components was directly related to the DC voltage level under consideration.

Inverters which operate from DC sources of one volt and under were considered to be outside the scope of this study. Studies indicated that this type of inverter is not especially suited for space applications because of its low power to weight ratio. Inverters which operate from high sources of DC voltage (1000 V DC and Higher) were also considered to be outside the scope of this study. However, because of the low currents involved, this type of inverter offered a potentially high power to weight ratio if suitable switching components and techniques could be developed.

The Group II performance specifications are listed next.

Harmonic Distortion:	Not to exceed 5% on total distortion with any single harmonic not to exceed 2%.
DC Input Voltage Variation:	+10%, -20%
High Frequency Transients on DC:	±200% of nominal for 10 microseconds or less
Output Voltage:	115/208 VAC
Output Voltage Regulation:	±2% for steady state, upper limit of transients during load switching to be +50% of normal envelope with recovery to steady state in 20 cycles.
Output Phase Separation:	120 ±2 degrees
Short Circuit:	Automatic recovery to normal operation when short is removed.
Overload:	200% for 5 seconds with ±4% regulation.
Unbalanced Load:	Up to 1/3 the total maximum VA between highest and lowest phases.

One additional area which is difficult to treat as an exact specification but is nevertheless important is the effect of the DC source impedance. Solid state inverters use switching techniques to condition the raw DC power. This rapid switching causes the DC input current to contain AC components at multiples of the switching frequency. These AC components can cause transmission line disturbances as well as disturb the source itself. While these disturbances are essentially a detailed application problem, it is desirable to know approximately the time profile of the input current so as to ascertain the probable magnitude of the problem. Calculation of the input current to a transistorized inverter (under the assumption of zero source impedance) is relatively straight forward. The input current to typical SCR circuits was explored in enough detail to show the complexity created by the commutation currents involved in SCR circuits.

Group III, (weight, efficiency and reliability) represents those parameters which must be optimized for any specific mission. It was the primary purpose of the study to select the methods and components which would allow the Group III parameters to be optimized for the given inverter types. These Group III parameters are usually interrelated in such a way that optimizing one of them will generally degrade the others. For instance, an extremely lightweight inverter might be designed to reduce the design margins on wound iron components. However, this would result in more heat loss in these components. This additional heat loss would reduce the efficiency and push the semiconductor components closer to their maximum operating temperatures thereby reducing reliability. The Group III parameters also interact with the Group II specifications. For instance, the lightweight inverter described above might also sacrifice harmonic distortion. These interrelations between Group II and Group III as well as the interactions of the Group III parameters with each other are analyzed in the main body of this study.

The weight estimates of these conceptual designs were defined as the weight of the electrical components only. It will not include the weight of such things as heat sinks, outside case and other structural supports, connectors, etc. The weight of these additional items is closely related to the type of heat sinking that is available and the shock and vibration levels to be encountered. While it was beyond the scope of this study to determine the packaging configuration and hence total weight, a reasonable engineering estimate is that the weight of the electrical components will comprise 50% to 70% of the total weight in an aerospace type inverter.

The reliability of any inverter is obviously very important. However, the number attached to the concept of reliability is a quantitative expression of

the effect of such factors as the number of components used to perform a certain function; the temperature, voltage and current stress on these components; the intrinsic reliability and failure modes of the components themselves; and the number of redundant circuits or components that are used; and the required life of the mission. Most of the above information can be obtained from a theoretical analysis. However, the actual stress levels must be measured on breadboards, etc., before a number can be assigned to the actual circuit reliability. Moreover the temperatures of the components, especially the semiconductors, are a function of the packaging and cooling of the final unit. These factors combine to make any discussion of absolute reliability strictly an academic discussion if the stress levels existing in the final package are unknown. During the initial phases of this study the voltage and current stress levels were approximated by analysis and judgment based on the behavior of similar circuits. This analysis together with the relative number of parts in the various circuits guided the selection of the techniques to be studied intensively. In the later phases of the study an absolute reliability analysis was performed. This analysis will be based on assumed voltage and current stress levels in the conceptual designs. The temperature of the components, especially semiconductors, was also assumed to remain within a specified band. The effect of radiation on the reliability of an inverter was beyond the scope of this study. However, in selecting the components, radiation of Van Allen Belt intensity was assumed.

Having established a basic set of performance specifications consistent with the reliable operation of an inverter in a space environment, the first phase of this study was directed toward a selection of the most feasible approach for each projected application. The primary consideration was a selection of the power stage for the inverter. Toward this end an investigation was conducted on existing designs for both series and parallel inverters in an effort to determine their operating ranges and their inherent strengths and weaknesses in regards to these established ground rules.

I. INVESTIGATION OF EXISTING INVERTER DESIGNS

A general description of present inverter configurations was examined next. These inverters were designed almost exclusively around two types of switching elements; silicon controlled rectifiers (SCR's) and transistors. The difference between these, of course, was the lack of ability to turn off the SCR at the gate. An external means must be provided to reduce the current in the SCR to zero.

Series type inverter circuits were investigated first. These circuits used SCR's almost exclusively thus requiring additional circuitry to turn these SCR's off. The results of this investigation revealed that the series type inverters were limited in useful load range to approximately 3 to 1. No

simple circuit modifications appeared to be available to extend this useful load range ratio, therefore, no further effort was devoted to these series inverter circuits. Instead, parallel type inverter circuits were studied. The basic parallel inverter circuits used either transistors or SCR's as their switching elements. Again additional circuitry was required to turn off these SCR's that were used as the switching elements. Technical information for parallel inverter operation with both resistive and inductive loads were available in the literature and were studied extensively. However, the technical information did not include the operation of the inverter under unloaded or switched conditions.

Therefore, a detailed analysis (See Appendix 4-I) was performed for this unloaded or switched condition with the results that this parallel inverter would not operate properly because the only current path for the reactive current to flow was through the commutating capacitor under these conditions. Improvement of this basic parallel inverter circuit was realized with the addition of "reactive" diodes to provide an alternate path for this reactive current (the McMurray-Bedford Circuit). This allowed the inverter to operate at all load power factors. These "reactive" diodes also limited the voltages under no-load conditions, thus making inverter operation under no-load conditions possible. However, should the load current become too large, resulting in excessive currents at the time of commutation, the turn-off time of the inverter is decreased causing the inverter to malfunction. A comparison was made between the various types of SCR inverters with respect to several parameters such as weight, efficiency, etc., (see Table 4-I). These parameters were based on 400 cps inverters with 5% total harmonic distortion and operating at the 1 KW level. The results showed that for fixed load operation, the series inverter was superior, but for large load variations, the McMurray Circuit was favored.

The output voltage of all the inverters mentioned previously was a direct function of the D. C. input voltage and could be varied by changing this input voltage. Thus, some type of voltage regulator will be required to regulate the inverter output voltage. Different types of voltage regulators were investigated in order to determine their individual merits when they were used with these inverters. The simplest type of D. C. regulator was the series proportional D. C. regulator which used a series transistor in the input of the inverter to be regulated. This type of regulator was only efficient when the input voltage to the regulator was very close to its output voltage in order to minimize the power loss in this series transistor. The input voltage excursions to this regulator must be kept small in order to maintain this high efficiency. Thus, the series proportional D. C. regulator could only be used to regulate low power inverters whose input voltage variation is small.

A modification of this series proportional type of voltage regulator was the series switching D. C. regulator. Here the series transistor was used as a switch that could be turned full "on" or full "off" depending on how the output voltage compared with a reference. This type regulator required an LC filter to smooth out these D. C. output pulses. The size and weight of this LC output filter was depended on the switching frequency of this regulator which in turn was determined by the maximum switching times of the series transistor chosen. The efficiency of this regulator was good under all load conditions within the rating of its series switching element. This regulator could accept large input voltage excursions which were only limited by the conduction angle swing of the series switching element. The size and weight of the LC output filter required to smooth these D. C. output pulses to an acceptable level limited its use for regulating high power inverters.

Both these series switching type regulators had one disadvantage in common in that their output voltages could be no greater than their input voltages. It becomes desirable in some circuit applications to have the regulator output voltage larger than its input voltage. Such step-up in voltage levels were required in inverter schemes that do not employ transformers in their output power stages such as the pulse width modulated type of inverter. A shunt switching type of D. C. regulator developed by Bedford[1] will produce a regulated D. C. output voltage that is greater than its input voltage. This type of circuit depended on the controlled energization of a series inductor through a shunt switching transistor whose switching time was controlled by an error signal in the same manner as was used for the series switching regulator approach. The operation of this circuit was highly dependent on the values of inductance and capacitance used for a given load range. These reactive elements could become quite large for large load requirements.

A common method that was used to obtain a step-up or step-down in the D. C. voltage level of the D. C. source was to first change it to an A. C. square wave with a simple parallel inverter. The A. C. output of this parallel inverter could then be stepped up or down by simply varying the turns ratio of the inverter transformer. Regulation was obtained by either controlling the amplitude or turn "on" and turn "off" time of this A. C. waveform. The regulated output D. C. voltage level was obtained by rectifying and filtering the A. C. waveform output of this inverter.

A modification of this basic inverter-regulator-rectifier circuit was to provide only the difference voltage between the D. C. source and the desired D. C. output voltage. This was accomplished by connecting the output of this regulator circuit in series with the source to provide this regulated difference output. Therefore, the inverter-regulator was required to pass only the error

[1] Quarterly Progress Report #4 on "Voltage Regulation and Power Stability in Unconventional Electrical Generator Systems" (AST1A #AD265158) page 87.

power instead of the total D. C. source power making it less complex and more efficient than the basic inverter-regulator-rectifier circuit approach.

In the above discussion separate regulator circuit approaches were considered in order to regulate these high power static inverters.

It was possible with certain types of high power static inverter designs that required output transformers to incorporate voltage regulation as part of their power output stages. Regulation could be accomplished by phase shifting one square wave with respect to a fixed square wave, both generated by this power stage, to produce a simple quasi-square wave whose resultant amplitude could be varied to provide this regulation. Suitable output filtering was required to suppress the harmonics generated by this quasi-square wave. More sophisticated approaches could be taken by generating multi-stepped waveforms with less harmonics that could be phase shifted in order to reduce the size of the output filter components required to suppress the resultant harmonics that were generated.

Two basic regulator approaches have been presented that could be used to regulate these high power static inverters. The first regulator approach required a separate regulator that either steps up or steps down the D. C. source voltage to the power stages of static inverters which usually do not have output transformers. The second regulator approach was included as part of the static inverter power output stage which usually has an output transformer. Regulation was usually accomplished by phase shifting one A. C. waveform with respect to a fixed A. C. waveform. In either approach, the harmonic distortion of the unfiltered outputs of these high power static inverters was usually too large. Thus, these harmonics must be removed by either filtering them or by using circuits which will produce harmonic cancellation. The optimum design was usually a combination of these two.

II. 3200 CPS - 10 KW STATIC INVERTER DESIGN CONSIDERATIONS

With this background of the type of basic inverter circuits available, along with their significant characteristics, such as output voltage waveforms, allowable loads, and methods that could be used to regulate their output voltages, a study was made of the possible approaches to any of the inverter groups described in the Methodology plan. Since this Methodology plan had been revised to eliminate the investigation of both the low and medium power -400 cps Static Inverters, all efforts were directed toward determining optimum circuit configurations for both the 400 cps and 3200 cps high power (10 KW) static inverters. The problem of the 3200 cps - 10 KW static inverter was considered first as it appeared to be the most difficult and no specific approaches appeared to offer a clear advantage. A survey of inverter configurations and switching devices was undertaken and representative inverter

circuits analyzed. It was felt that there were two basic design decisions to be made. One was the selection of the basic power switching stage and its power switching elements. The second was the technique of combining these basic elements to obtain a three phase, voltage regulated sinusoidal output whose characteristics would conform as close as possible to the specifications outlined in the Methodology plan.

The various switching devices were investigated first to determine their merits and disadvantages when used in different high power static inverter configurations. They were germanium and silicon power transistors, silicon controlled rectifiers, and gate controlled switches. Two basic power inverter approaches were considered for this 3200 cps - 10 KW inverter design. They were high frequency pulse width modulation techniques and quasi-square wave or stepped wave techniques. The pulse width modulation scheme was found to be impractical at this operating frequency since its minimum practical carrier frequency would be approximately five times the fundamental or 16,000 cps. Neither the silicon controlled rectifiers nor the gate controlled switches had fast enough turn "on" and turn "off" times to handle these switching speeds. Germanium transistors of sufficient current capacity to minimize the number of parallel transistors required per half phase to a reasonable number could not be obtained with sufficient switching speeds to accommodate this carrier frequency. Medium power silicon transistors (10A) were found with extremely fast switching times that could accommodate this carrier frequency. However, the resulting switching losses of 130 watts per transistor at 16,000 cps and 200% load were found excessive for a reasonably efficient power stage. Thus, the pulse width modulation approaches were considered to be impractical at this operating frequency of 3200 cps.

The second approach to this problem would be to perform the inversion at the fundamental frequency of 3200 cps, thus reducing the switching losses that were obtained for the pulse width modulation schemes. Again the various switching devices were compared with the results that both the silicon controlled rectifiers and gate controlled switches were found unsuitable for high power inverter applications. The gate controlled switches were limited by their low current ranges (6A maximum) and their rather long switching times. The silicon controlled rectifiers were available in ratings up to 400 amps rms and voltage ratings up to 1300 volts. However, the fact that the silicon controlled rectifiers must be commutated off by an external source adds circuit complexity and additional losses at these high power levels. From a weight point of view, this additional weight required by the many transistors over a few silicon controlled rectifiers would be compensated by the elimination of the commutating capacitors and chokes required by the SCR circuitry. The higher efficiency of the transistorized devices and absence of the high peak currents

associated with the silicon controlled rectifier commutation would reduce the size and weight of the output transformers and heat sinks of the proposed power inverter.

Comparing the germanium and silicon transistors for this stepped wave inverter approach at 3200 cps revealed that for a given transistor current capacity the silicon transistor would have approximately 1.5 times the losses as an equivalent germanium transistor. The major loss in the silicon transistor was contributed by its forward losses. In the germanium transistor, however, the major loss was due to its switching losses. It would appear that the germanium transistor would offer a better choice. However, its maximum junction temperature was limited to 100°C while the silicon transistor junction temperature was good to 200°C, thus requiring less heat sink capacity. In addition, silicon transistors were available in ratings up to 150 amps rms with ratings to 150 V_{CE}. These were much larger ratings than could be obtained for germanium transistors at this time. Thus, fewer silicon transistors would be required to perform the same switching function. The selection of silicon transistors for the power stage switching elements were made because of these two reasons.

In order to reduce the silicon transistor losses in this power inverter, possible circuit changes including techniques for optimizing the switching pattern, reducing the current and/or voltage at the time of switching, or reducing the effective switch resistance by connecting additional transistors in parallel could be utilized. Transistor drive losses could be reduced by providing a current feedback drive control which would be proportional to the instantaneous collector current rather than a voltage square wave drive whose output was fixed for the largest collector current.

Since the stepped wave approach was decided upon for the 3200 cps - 10KW static inverter, an analysis was performed on various stepped waveforms to obtain a maximum number of harmonic cancellations for a minimum amount of circuit complexity. The more harmonics that could be effectively cancelled would in turn reduce the size and weight of the filter components required. The method of voltage regulation would be a major factor in selecting the stepped waveform to be used. It was found that adding together two multi-stepped waveforms with a variable phase difference in the power stages would produce the most efficient and lightweight means of regulation which would produce a minimum harmonic distortion. A variety of stepped waveform characteristics that have been proposed by contributors to the field of static

inverters were investigated. The various waveforms were classified as to the number of horizontal steps that could be counted in a full cycle, whether the steps occurred at equal or unequal time intervals and whether the step heights had equal or unequal amplitudes. The stepped waveforms examined were broadly classified into two groups. The first group were waveforms that could be divided by the smallest time increment step into an integral even number of parts. These waveforms had steps of optimum height that specifically reduced the number of lower harmonics. The second group of stepped waveforms were those which had been specifically designed to have either the minimum total harmonic distortion possible for a waveform having a particular number of steps or designed specifically to eliminate certain harmonics.

The application of the stepped waveforms to static inverters required certain characteristics of the waveform for three phase operation. In some of the waveforms examined, a single square wave inverter could supply two or even three phases with a required step and therefore was given additional considerations. Thus, waveforms requiring no increase in the number of basic square wave inverters to generate three phases compared to the number required by a single phase inverter were chosen. From these waveforms, the ones whose phase voltages could be connected in a delta configuration were given special consideration. This narrowed the choice of multi-stepped waveforms down to three choices using the above criteria. They were:

1) Six steps per phase requiring three inverters per phase with the fifth harmonic being the lowest.
2) Twelve steps per phase requiring six inverters per phase with the eleventh harmonic being the lowest.
3) Eighteen steps per phase requiring nine inverters per phase with the seventeenth harmonic being the lowest.

Of these three, the waveform containing twelve steps requiring six inverters per phase was chosen. This required an output filter capable of suppressing the eleventh harmonic and its complement, the thirteenth. Although the selection of the eighteen step waveform would permit a further decrease in filter size, the increase in circuit complexity required with the use of nine inverters per phase would not justify the increase in weight and loss in efficiency that would occur. Thus, the waveform containing twelve steps per phase was considered an optimum choice for this 3200 cps - 10KW static inverter.

Having established the type of stepped waveform that would be used in the power output stages for the 3200 cps - 10KW static inverter, a concentrated

effort was devoted to the magnetic components that would be used in this static inverter. A detailed study was undertaken to obtain optimum magnetic component designs. Optimum magnetic designs required not only optimization of the individual magnetic components for a given inverter design, but also provided an optimum choice of the overall system that would eventually be used. An optimum magnetic component design would depend on the specific application since, in general, weight and losses could not be minimized together.

Optimum loading of a fixed transformer was investigated first. The general rule regarding the optimum loading of a transformer was that maximum efficiency occurred when the core and copper losses were equal. However, this rule was based on the conditions of a constant input voltage and a variable load. If both, the input voltage and maximum design load were fixed, which was usually the case, then the only parameters that could be varied were its physical size and its relative losses in the windings and core. Maximum transformer efficiency for this case was found when the core loss was not quite equal to the copper loss. However, the actual differences in these losses were not very large so the general rule mentioned previously still applied. A general set of equations were developed next to permit an optimum transformer design for a given power level to be scaled to a different power level with respect to volume, weight, and losses. This would enable new transformer designs to be obtained without extensive calculations. These general set of equations could only be used to compare transformers of similar construction operating at the same core flux density and copper current density levels. They were used extensively when the final 3200 cps - 10 KW static inverter design was scaled to lower power levels.

An analysis was made on the losses of transformers delivering constant power as their size and weight were varied. The results of this analysis indicated that for a fixed power level, a transformer with a minimum weight loss product could be obtained when its core material was operated as close to its maximum flux density as possible.

The analysis of transformer optimization was expanded to include its associated circuitry when the three phase power output transformers were considered. Various possible power switching stages which could be used for this 3200 cps - 10 KW static inverter were investigated. It was found that some required the use of three single phase transformers, some required one three phase transformer, and some required more complex transformer construction. Since a twelve step, six inverter per phase waveform was decided upon, a comparison of the many possible transformer configurations that would be compatible with this waveform was undertaken. It immediately became clear that the three phase transformer had less volume and weight than three single phase transformers with equivalent three phase capacity. However, the circuit complexity

required to drive this three phase transformer more than offset these advantages obtained in both weight and volume reduction. A more complex transformer suitable for operation with this twelve step waveform had been described in the literature.[2] This transformer contained six windows whose outer legs supported both the primary and secondary windings. This transformer was referred to as a "hexadic" transformer because it contains six windows. This "hexadic" transformer obtained its weight savings by using less iron in those portions of the magnetic circuit where flux cancellation occurred. It was estimated that the "hexadic" transformer was approximately 20% lighter than its six single phase counterparts. This analysis was extended to include several possible complex transformer designs similar to the "hexadic" transformer. Again, the same basic technique of flux cancellation was utilized in different portions of the magnetic circuit to reduce the weight of these transformers. Additional flux cancellation was also obtained when the phase shift between the two sets of multi-stepped output voltage waveforms was varied to obtain voltage regulation. A transformer suitable for use with this twelve step waveform was conceived. It contained twelve windows arranged in two rows of six and was designed for minimum core weight. The primaries for both the reference twelve step waveform and the phase shifted twelve step waveform were wound on the six outer legs of each side of the transformer respectively while the secondary windings were wound on the six inner legs which were common to the twelve windows. Two "hexadic" transformer cores would be required to provide this twelve step waveform phase shifting regulation scheme.

A comparison between this proposed transformer and the two "hexadic" transformers based on the same core cross-sectional area and window area per winding revealed that the two "hexadic" transformer cores have 96.5% of the weight of the proposed transformer core. However, when the winding weights were factored in, the total weight of the two "hexadic" transformers became 1.63 times the weight of the proposed transformer. Both these designs were too heavy in winding weight as compared with their respective core weights, and improvements in both could be expected with a more detailed design effort. Thus, the proposed flux adding transformer design with twelve windows was the choice for this 3200 cps - 10 KW static inverter.

The core material and operating flux density were considered next for this transformer. Three types of core material were considered. They were Square Permalloy 80, Orthonol, and Supermendur. A sample transformer

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[2] "Static Inverter with Neutralization of Harmonics", A. Kernick, J. Roof, T. Heinrich, AIEE Transactions, May, 1962, pp 59-68.

was designed using each of these core materials. They were theoretically operated at various frequencies and power levels. These sample transformers were simple two winding toroidal units with equal copper and core weights. The maximum flux density that the transformers could support was considered the design limit. The results of this investigation were tabulated for five selected frequencies and were used to optimize the output transformer design at 3200 cps.

A final 3200 cps transformer design was made for each of the three core materials. All three transformer designs were obtained by operating the core materials at their maximum flux density levels. The results of their weight loss products and efficiencies were:

DESIGNS	I Sq. Perm-80 (2 mil) (79% Nickel) (17% Iron) (4% Molybdenum)	II Orthonol (2 mil) (50% Nickel) (50% Iron)	III Supermendur (2 mil) (49% Iron) (2% Vanadium) (49% Cobalt)
WT-LOSS PRODUCT	1860 lb-watts	1300 lb-watts	975 lb-watts
EFFICIENCY (at 10 KW load)	99.16%	98.37%	96.32%

From these results, the Orthonol core material was selected for the final transformer design since it was in between the two extremes of weight and efficiency. The silicon transistor switching elements that would be used for these output power stages were determined next. Calculations indicated that the peak load current that would have to be carried by any one side of a power switching stage would not exceed 88 amps for a 200% overload condition. The peak voltage appearing across any of the power switches would occur at turn-off and would not exceed 133 volts. Both these current and voltage requirements could be satisfied by one power transistor whose ratings were 150 amps and 150 volts. Although this transistor had sufficient current capacity, its voltage level did not offer much safety margin. Larger voltage ratings for this transistor are expected in the near future which will improve this safety margin. If larger voltage safety margins were desired than could be provided by this transistor, then it was possible to series two of these transistors per switch leg or to parallel a number of lower current higher voltage transistors. In either case, the circuit complexity and losses would present additional design problems; thus, the one 150V - 150 amp power transistor was tentatively

used for these switching elements and would be replaced with their higher voltage counterparts as soon as they become available.

Having established the power stage output transformer design and the silicon transistor switches that were to be used with it, further means of improving the power stage efficiency were investigated. The results of this investigation revealed that the power stage efficiency would be improved in two ways. The first improvement would utilize a timing core in the collectors of each of the power transistor switching pairs which would reduce their "turn on" losses to a negligible value. The resulting savings of 6 watts per output stage or a total of 72 watts for the entire inverter would be realized with the use of these delay cores. The second improvement would employ current feedback as a means of supplying the required transistor base drive in place of the more conventional voltage base drive scheme. A base drive proportional to the transistor collector current was obtained in this current feedback scheme. The transistor base drive transformers in this case would be used as current transformers. In order to turn off a transistor it was necessary in this scheme to provide enough turn-off current on a pulse basis from an external driving source to completely cancel the positive drive signal from the collector feedback winding. The power wasting base current limiting resistors required for the conventional voltage base drive scheme were also eliminated. A savings of 320 watts total at full load had been estimated for this current feedback scheme. Thus, a total savings of 392 watts had been realized with the use of these two schemes.

The A. C. output filter circuit configuration and component values were determined for the three phase outputs. Because of the widely varying load impedance encountered, conventional filter design techniques were not applicable for use with static inverters. The AC output filter must have a nearly constant phase shift and voltage transfer ratio over a wide variation in load impedance. Thus, a four element filter circuit was decided upon which contains a series tank circuit in series with the load and a parallel tank circuit shunting the load. The series tank resonance frequency was tuned to the fundamental frequency so no attenuation or phase shift would be encountered. This filter must reduce the eleventh and thirteenth harmonics to less than 2% each and the filter components were calculated accordingly.

A D. C. filter was placed on the input terminals of this inverter in order to make the D. C. source appear "stiffer" to the inverter and to help attenuate the radio frequency noise impressed on the supply lines caused by the inverter current pulses. This D. C. filter consisted of a large capacitor ($\sim$ 100 ufd) that was shunted by a small ($\sim$ .01 ufd) mica capacitor.

The resultant weights and losses were determined for this complete 3200 cps - 10 KW power stage and were found to be 29.55 pounds and 635.9 watts full load loss.

The low level logic and power stage circuitry was tentatively designed for this 3200 cps - 10 KW static inverter. A complete set of schematics and parts lists were generated for this design. Since this circuitry and their parts were created from a theoretical design, they could only be considered as representative of the actual circuitry that would be needed since much bread-boarding of the individual circuitry will be required in order to finalize this design. The low level logic circuitry necessary to control the power stages will be described briefly. A master crystal controlled oscillator and pulse shaper circuit was used to provide a series of pulses at twelve times the fundamental frequency of 3200 cps to one six phase ring counter that was used as a reference, and a phase shifter circuit that was used as part of the phase shifter regulator scheme. The reference ring counter consisted of six interconnected flip-flops whose outputs produce 6 square waves which were displaced 30° from each other and have a frequency of 3200 cps. The outputs of this reference ring counter were used to control six pre-buffer drive stages which were composed of push-pull center tap transistor drive circuits. These six pre-buffer drive stages in turn controlled the six power stages which were used to generate the twelve step, three phase reference waveform in the inverter output transformer.

The phase shifter circuit was made up of six cascaded stages each of which was capable of producing a maximum phase shift angle of 30°. A typical phase shifter stage consisted of an input flip-flop, two linear ramp generators, a level sensing Schmitt trigger, and an output flip-flop.

The Schmitt triggers had their voltage trip levels set for a pre-determined value. The input error signal from the output voltage sensing circuitry was introduced into the inputs of these Schmitt triggers. This input error signal current biased the linear ramps that appear on the input of these Schmitt triggers, shifting them up or down with respect to the preset trigger levels. This caused the Schmitt triggers to fire at different points on the ramps as a function of the magnitude and polarity of this input error signal. A relative phase shift angle of up to 180° was obtained between the output pulses of the master crystal controlled oscillator and the resultant output pulses of the phase shifter. The phase shifted output pulses of this phase shifter were introduced into the input of a six phase ring counter that was identical in construction and operation to the reference ring counter. The outputs of this phase shifted ring counter were used to control six pre-buffer drive stages. These pre-buffer drive stages in turn controlled the six power stages which were used to

generate the phase shifted twelve step, three phase waveforms in the inverter output transformer to provide the necessary voltage regulation.

A short circuit current limiting circuit was provided to protect the inverter against overload currents exceeding 215%. This was accomplished by turning off the power stages for a finite time and then turning them back on. This cycling would continue as long as the short remains, thus protecting the inverter components.

A reliability study was performed on the electrical circuitry and their parts for the proposed 3200 cps static inverter. This reliability study could only be used as a guide since this circuitry was created from a theoretical design and the stress levels assigned to each component were based on this theoretical design with no actual stress measurements being taken. Packaging techniques and electrical connections were not included in this reliability study. The parts failure rate approach was used to analyze each component in this electrical system. A reliability block diagram was used to represent the overall circuit configuration. Each major circuit was represented by one of these blocks. A series of sub-blocks were assigned to each major block to represent the individual circuits or components that were required to create a major circuit. This reliability block diagram was used with the representative circuits for each sub-block to establish an overall Reliability Figure of Merit R for the 3200 cps - 10 KW Static Inverter. The generic failure rates, derating factors, and environmental operating modes for the electrical components were obtained from:

> "Reliability Engineering Data Series Failure Rates" by D. R. Earles, M. F. Eddins. Avco Corporation - Research & Advanced Development Division.

The operating time for each component was determined. From this information the overall Reliability Figure of Merit R was computed for a 20-minute missile launch combined with one month and then one year continuous operation as a Satellite in an earth orbit. The results of this study indicated that this inverter would have a reliability of .963506 and .718930 for the one month and one year continuous operation respectively. There were no redundant circuits in this proposed inverter. In order to improve its overall Reliability Figure of Merit, redundant circuitry should be used with circuits that contain the largest failure rates. Components with larger de-rating factors could also be used to improve these reliability numbers.

The last area of investigation for the 3200 cps - 10 KW Static Inverter involved scaling its weight, losses, and reliability with respect to reduced power level,

D. C. input voltage, harmonic distortion, output phase separation, voltage regulation, and D. C. input variations. The effects of scaling this inverter with respect to reduced power level and D. C. input voltage were of primary interest. As the power level was reduced below 10 KW, there were a multitude of changes which occurred in the inverter components and circuitry. Components such as transformers, inductors, etc., which must be especially designed for a given inverter could be scaled for loss and weight on a continuous basis. However, components such as transistors and diodes which were not made specifically for a given size inverter but were selected because their parameters met or exceeded those required for a particular application would vary in a step component change. There were also certain components and circuits which were independent of the power level such as the master crystal controlled oscillator and pulse shaper circuit. Weight and loss curves as a function of power level were obtained for these magnetic and semiconductor components. The total weights and losses for all these components were added together to obtain the anticipated weight and loss of the entire inverter as a function of the power level. The weight and loss of the magnetic and semiconductor components were determined as the D. C. input voltage was varied. The power stage transistors were found to be the components most affected by these voltage changes. When the D. C. input voltage was dropped below 41 volts, the current in the power stage transistors became excessive, thus requiring paralleling techniques to reduce these currents to an acceptable level. The paralleling of these power stage transistors modified the power output transformer so that a split transformer technique was required. As the nominal D. C. input voltage exceeded 68 volts, the power stage transformers were connected in a bridge configuration to allow each transistor to support half the D. C. input voltage. Again, the total weights and losses for all the inverter components were added together to obtain the anticipated weight and loss of the entire inverter as a function of the D. C. voltage input level.

The scaling involving harmonic distortion, output phase separation, voltage regulation and D. C. input variations revealed that the A. C. output filter parameters were the components most effected. The output power transformer copper loss and leakage inductance were reflected as part of the filter parameters. Also, the load impedance was considered as part of these filter parameters. Weight and loss curves were determined for each of the filter components as the above four parameters were varied. The worst condition that was encountered was the effects of unsymmetrical loading on the voltage regulation. If the voltage regulation tolerance was reduced below ±2%, an individual voltage regulator would be required for each phase which would require three separate power flux-adding transformers with an increase of weight and losses over the present system of 2.32 lb and 55.5 watts. In addition, three times the power switching transistors and pre-drive circuitry

would be required along with two additional ring counters, two phase shifters, and two voltage sensing circuits. This added circuit complexity did not justify reducing the voltage regulation tolerance below ±2%.

A detailed design study had been completed for the 3200 cps - 10 KW Static Inverter. A conceptual design was created using the Methodology plan as a design guide. Many inverter designs, circuit approaches, and component optimization studies were investigated in regards to efficiency, weight, and reliability as well as other design parameters listed in the Methodology plan before this inverter design was established. Improvements in efficiency, weight, and reliability should be realized if this conceptual design is fabricated since new circuit approaches and more optimum component designs will develope as experience is gained with the various circuits. Assuming that the 3200 cps - 10 KW design is performing to the Methodology plan, a detailed reliability analysis may then be instigated in which the electrical and thermal stresses of each circuit component are carefully measured. The overall reliability can then be computed with a high degree of confidence. Reliability recommendations may be incorporated into the circuitry wherever possible to improve the inverter's reliability figure of merit. The component weights and sizes may also be computed accurately. Such items as heat sinks, terminals, connectors, etc., which were intangible items in the theoretical design may now be accurately determined in order to obtain a final package configuration. Shock, vibration, and other environmental conditions must also be considered for this final package design.

At present, the conceptual design offers a lightweight ($\sim$41.5 lb total component weight) and an efficient ($\sim$92% overall at full load and .9 P.F.) inverter. However, its overall reliability figure of merit (R$\sim$.71893 for one year continuous operation as a Satellite in an earth orbit) will have to be improved considerably either through the use of redundant circuitry or with less complex circuit designs.

A minimum safety factor margin of two was used for a design goal in this theoretical design wherever possible. Circuits which employ components that cannot meet this design goal should be thoroughly investigated in order to determine alternate approaches that can be used. For example, the power switching transistors that are presently available only allow for a safety factor of 1.125. Thus, either higher voltage units of 150 amp capacity must be found or lower current transistors with higher voltage ratings must be paralleled. Overvoltage circuit protection may also be used to protect these transistors. Therefore, the conceptual design that was determined, will require more design considerations coupled with extensive breadboard testing of the individual circuitry before an optimum 3200 cps - 10 KW static inverter design can be realized whose electrical parameters will either conform or exceed those defined in the Methodology plan.

III. 400 CPS - 10 KW STATIC INVERTER DESIGN CONSIDERATIONS

The 400 cps - 10 KW Static Inverter Design was investigated. Both the Multi-Stepped Waveform techniques which were described in detail for the 3200 cps inverter design, and the Pulse Width Modulation techniques were considered for this 400 cps - 10 KW inverter design. The Pulse Width Modulation techniques consisted basically of switching bi-polar high voltage D. C. to produce duty cycle controlled pulses at the carrier frequency to synthesize the 400 cps sinewave. (The carrier frequency of 10 KC has been selected for this inverter design.) These two approaches were capable of producing an output waveform that contained only the higher harmonics therefore requiring a simple and light weight A. C. filter. The most predominant frequency for the Pulse Width Modulation approach was the carrier frequency.

The first harmonic pair for the Multi-Stepped Waveform approach was predominant with their frequencies determined by the number of steps selected. The Multi-Stepped Waveform approach required a multi-phase output transformer and its associated switching transistors connected in push-pull pairs which must be capable of producing 10 KW at an operating frequency of 400 cps.

The Pulse Width Modulation approach departed from the more conventional Multi-Stepped Waveform approach by not using any form of power transformer in its output stages. Instead, the D. C. source voltage was stepped up to a bi-polar high voltage level by a rather simple DC-DC converter which used a light weight output power transformer. This bi-polar high voltage D. C. was then sent to the power stages which consisted of power transistor switches that were connected in parallel for each half phase to obtain the required current capacity. Six of these half phases were required to produce the necessary four wire, three phase output. The power transistors were connected directly to the load with their "on" and "off" times controlled by the driver stages. The resultant output voltage waveform, before the A. C. filters, was a series of pulses whose "on" and "off" times synthesized a 400 cps sinewave with the carrier frequency being the predominant harmonic that must be eliminated.

The Pulse Width Modulation scheme was selected for this 400 cps - 10 KW inverter. This selection was based primarily on a preliminary comparison of weight, efficiency, and reliability between the Pulse Width Modulation scheme and an equivalent inverter using the multi-stepped waveform approach. The results of this preliminary comparison indicated that a weight savings of 57.4 pounds would be realized with the use of the Pulse Width Modulation scheme (PWM $\sim$150 lbs and Stepped Waveform $\sim$207.4 lbs). However, the efficiency of this Pulse Width Modulation approach was slightly less (PWM $\sim$82.4% and Stepped Waveform $\sim$83.5%).

The reliability figures were not known at this time since the detailed designs had not been performed. Thus, for selection purposes, the reliability of the two approaches were assumed to be the same. The selection of the Pulse Width Modulation scheme was then based on the apparent weight savings of 57.4 pounds since the efficiency variations between the two approaches appeared to be negligible. An examination of the electrical parameters (Group II) of the Methodology plan did not reveal any characteristics which might be better in one system rather than the other with the exception of short circuit protection. The Pulse Width Modulation approach would provide faster short circuit protection by changing its index of modulation because the output filter requirements were less.

A DC - DC converter was required for this Pulse Width Modulation scheme to step up the source voltage to a bi-polar high voltage output that was required for the output power stages. The efficiency of this DC - DC converter was calculated to be 88% while the efficiency of the actual inverter was calculated to be 93.5%. If the converter was eliminated by using a bi-polar high voltage source, then the overall inverter efficiency would then become 93.5% making this inverter approach even more attractive.

A detailed investigation of the various high frequency Pulse Width Modulation techniques was undertaken in order to determine which one would produce waveforms with low total harmonic content with relatively simple inverter circuitry. All these Pulse Width Modulation techniques operated by modulating the width, phase, or frequency of a high frequency carrier signal with a power frequency and then demodulating the resulting waveform to obtain the modulating frequency power.

The Classical Pulse Width Modulation technique was examined first. Its output voltage consisted of a number of pulse duration modulating pulses having their trailing edge modulated by a power frequency. The method of analyzing these complicated waveforms was developed by W. R. Bennett[3] and consisted of a double Fourier series that represented this waveform. This method of analysis was applicable to both uniform and natural sampling techniques with modifications. In the uniform sampling technique, the pulse width was proportional to the instantaneous value of the modulating wave at uniformly spaced sampling times. An analysis of its waveform spectra revealed that the method of uniform sampling had a carrier and its harmonics and sidebands that diminished rapidly. In addition, this waveform contained second, third, fourth, fifth and sixth harmonics of the power frequency which would require a rather large and heavy filter to eliminate them. Thus, the method of uniform sampling would not produce a waveform with low harmonic content that would allow a lightweight filter to be used.

3 W. R. Bennett, "New Results in the Calculation of Modulation Products", the Bel System Technical Journal, New York, Vol. 28, No. 3, pp 490-595.

Natural sampling was investigated next. In this case the pulse width was a function of the average value of the modulating waveform during the sampling interval. Examining the natural sampling spectra revealed that the carrier and its harmonics and sidebands were identical to those of the uniform sampled technique. However, there were no lower harmonics of the power frequency as occurred for the uniform sampled technique. Thus, a simple lightweight low pass filter could be used to filter the carrier and its sidebands. The method of natural sampling produced a waveform with low harmonic content with rather simple inverter circuitry.

The Commutated Pulse Width Modulation techniques were also examined. Both natural and uniform sampling could be used with this technique. In this technique, the modulating wave was first rectified and then operated on by the modulator. The resulting pulse width modulated waveform was then commutated by a square wave which was in synchronism with the modulating waveform. A triple Fourier series expansion was required to analyze this waveform. The results of this analysis revealed that the harmonic spectrum of both the uniform and natural sampling for this Commutated Pulse Width Modulation Technique was nearly identical to the harmonic spectrums obtained for the Classical Pulse Width Modulation technique. The choice of Modulation technique was based on the complexity of the circuits required for each method. Each modulation technique required a logic stage, a power inversion stage, DC - DC converter, and an output filter. However, the Commutated Pulse Width Modulation techniques required a demodulator stage and its associated logic circuitry. The modulating techniques employing uniform sampling were disregarded because of the heavy output filters required. The Classical Pulse Width Modulation technique employing natural sampling was selected for this 400 cps - 10 KW inverter because it had less circuit complexity than the Commutated Pulse Width Modulation technique using natural sampling. It was felt that the additional weight and loss obtained for the Commutated Pulse Width Modulation technique did not justify the slight, if any, reduction in output filter weight that could be obtained.

Having selected the Classical Pulse Width Modulation technique with natural sampling for the 400 cps - 10 KW static inverter, the various switching devices were investigated. The Pulse Width Modulation scheme required a minimum practical carrier frequency of twenty-five times the fundamental or 10,000 cps so that the frequencies of the carrier and its harmonics and sidebands would be high enough to allow lightweight filter components to be used. The results of this investigation revealed that neither the silicon controlled rectifiers or gate controlled switches have fast enough switching times. Germanium transistors of sufficient current capacity for reasonable parallel operation also had switching times that were too slow for efficient operation. However,

medium power silicon transistors (10A) with high voltage ratings had been found with extremely fast switching times that could accommodate this carrier frequency (10,000 cps) with a minimum amount of switching losses. In addition, transistors with high switching speeds would allow a maximum value for the modulating wave component to be obtained since the modulation index M could be made very close to its optimum value of one. This was desirable since the fundamental component would decrease and the carrier frequency amplitude would increase as the modulation index was made less than one thus requiring a progressively larger output filter.

In order to build a transformerless inverter, the input voltage to the power stages must be bi-polar and be high enough to produce the required three-phases output voltages specified in the Methodology plan. Therefore, a DC - DC converter was required to provide these voltage requirements from the source.

A detailed theoretical design for the 400 cps - 10 KW PWM inverter was undertaken to obtain tentative circuits and parts lists in preparation for the breadboarding phase. In addition, typical values of efficiency, weight and reliability were obtained from this theoretical design. A conceptual circuit design was obtained for the 400 cps - 10 KW PWM inverter which was considered as representative of the actual circuitry that would be needed since much breadboarding of the individual circuitry would be required in order to finalize the design. This circuit design contained a three phase square wave reference generator that produced the low frequency (400 cps) modulating signals which were square waves displaced 120 degrees apart. The reference signals were passed through controllable attenuators which had a normal attenuation of zero. These attenuators were used for overcurrent protection by attenuating the size of the modulating signal which in turn reduced the voltage of the overloaded line. The fundamental frequency of the output square wave from the attenuators was extracted by tuned amplifiers which had unity voltage gain at 400 cps. The 400 cps sine waves produced by these tuned amplifiers were then mixed with the sweep wave in the three summing networks. The sweep wave was a generator which produced a sawtooth sweep wave at the carrier frequency. The resulting waveform that came out of these summing networks was a sinusoidally modulated sawtooth wave which was sent to the slicer circuits. The slicer circuits sensed the absolute level of these waveforms, thus producing pulses which had their widths proportional to the modulating signal level during the sampling interval. The variable pulse width signals were then amplified and sent to the driver stages which transformed these signals into a form suitable for use by the power stages. The power stages converted the low level drive signals into the required high power levels. The high voltages required for the power stage was supplied by a DC - DC converter from the low voltage source. The DC - DC converter was also used as a voltage

regulator to maintain the voltage across the power stages constant. The output filters were used to extract the carrier and its sidebands from the output voltage leaving only the power frequency voltage.

Both the power stage and DC - DC converter were given special design attention since they were the circuits that were required to control this high power. The power stage contained six half phases which were required for a transformerless output. Each half phase contained a number of transistor switch legs that were connected in parallel to handle the required load current. The number of these switch legs would be determined by the current capacity of the individual transistors selected. The maximum voltage across the half phases was found to be 380 volts for a 115 V rms output. This was rather a high voltage, making it difficult to find a transistor that had both high voltage and current ratings along with very high switching speeds. An RCA developmental type TA2110 transistor with a V_{CEX} of 400 volts and 10 amp current capacity was found that had very fast switching speeds. However, its voltage rating only provided a 5% safety factor which was below the minimum design goal of 200%. This design goal could be satisfied by connecting two of these transistors in series producing a safety factor of 211%.

Voltage divider resistors were required to equally divide the supply voltage across the power transistors connected in series when they were in the "off" condition since their collector leakage currents could be unequal. These resistors were connected in parallel with each transistor. The maximum switch current that each half phase must be able to supply could be as high as 250 percent of rated current at .7 P.F. or a maximum current of 147 amps. Since the RCA developmental TA2110 was rated for 10 amps, a total of fifteen of these transistors must be connected in parallel for each half phase. Thus, the series-parallel transistor combination netted a total of 30 transistors per half phase or a total of 180 transistors for the power stages. Because the saturation voltage could vary for the switching transistors, some sort of current balancing technique will be required. This balancing technique must be simple and have a high efficiency. Two non-dissipative current balancing techniques, one using split transformers and the other using balancing reactors, were examined in detail. The results of this study indicated that balancing reactors connected in a closed chain for each half phase would be the lightest and most efficient approach to balance the transistor load currents for this nominal D.C. voltage of ±200 VDC. The balancing reactors must be designed to support the maximum voltage unbalance that could exist between the saturated transistors.

Blocking diodes were connected in series with each half phase to prevent reverse current from flowing through the power transistors. The blocking diodes must have a very fast recovery time to reduce its switching losses when the switch legs were being commutated "on" and "off". Reactive diodes

must also be connected across the input to each half phase to provide a current path for the reactive current when the blocking diodes were in the circuit.

The power stage weight and efficiency were found. The power stage weight was 55.239 pounds for 1059 parts while the full load power stage efficiency at .7 P.F. was calculated to be 89.14%.

The DC - DC converter was used to provide a regulated bi-polar high voltage to the power stages from the unregulated low voltage source. The DC - DC converter must be capable of supplying the 250% overload capacity to these power stages. A number of converter techniques were investigated with the result that a pure square wave system with pulse width modulated riders was selected. The output filter for this converter was very small since pure square waves were being rectified and the switching stage used to control the DC input to this stage had only to handle the power required to raise the source voltage up to its maximum level. Therefore, at the high source voltages, the switch handles no power, while the maximum power it controls was at the low source voltages. This means that the transformer used in the switching section could be smaller for the voltage stepup system. Both of these factors contributed to a lower overall system weight. A tentative operating frequency of 1000 cps was selected to provide an optimum design between efficiency and weight for this converter. The slow switching speeds of the 150 amp power transistor and hence their switching loss was the major deterrent in going to higher operating frequencies. The DC - DC converter weight could be reduced substantially while still retaining its high operating efficiency if higher operating frequencies could be used if and when 150 amp transistors with higher switching speeds become available.

The DC - DC converter weight and efficiency could now be found. The converter weight was 50.3 pounds while the full load efficiency at .7 P.F. was calculated to be 91.4%.

A reliability study was performed on the electrical circuitry and their parts for the proposed 400 cps - 10 KW PWM static inverter. This reliability study could only be used as a guide since the circuitry was created from a theoretical design and the stress levels assigned to each component were based on this theoretical design with no actual stress measurements being taken. Packaging techniques and electrical connections were not included in this reliability study. The parts failure rate approach was used to analyze each component that would represent the overall circuit configuration. Each major circuit was represented by one of these blocks. Sub-blocks were assigned to each major block to represent the individual circuits or components that were required to create a major circuit. An overall Reliability Figure of Merit R could be found for this 400 cps - 10 KW PWM Static Inverter from the

representative circuits for each sub-block in the reliability block diagram. Examining the block diagram revealed no redundant circuitry was used in the low level logic, DC-DC converter, and the pre-driver stages. However, the power output stages can contain redundant circuitry depending on the mode of failure and the permissible maximum current allowed. Power transistors usually fail in the shorted mode of operation. Thus, a maximum of one transistor in each switch leg or a total of 15 transistors, one in each switch leg for each half phase, could fail in the shorted mode without degradation of the output waveforms. The voltage safety factor across the unshorted transistors, however, was reduced from 211% to 5%. A catastrophic failure would occur if both transistors that were connected in series in one switch leg should fail in a shorted mode causing the loss of a half phase. The use of fuses in each switch leg would prevent this catastrophic failure by clearing the shorted switch leg. However, the current capacity of the half phase would be reduced. If the power transistors should fail in an open mode, then a maximum of nine switch legs would be lost per half phase with the inverter load capacity being reduced from 250% to 100% of full load. The same generic failure rates, derating factors and environmental operating modes used for the electrical components for the 3200 cps - 10 KW reliability analysis were used here. The operating time for each component was determined. The reliability figure of Merit R was then determined from this information for the three possible modes of failure in the power stages. Again, a 20-minute missile launch combined with one month and then one year continuous operation was used. The results of this study indicated that the lowest reliability figure of merit for one year (R = .498263) was obtained for the catastrophic failure of two power transistors in the same switch leg without fuse protection. The highest reliability figure of merit for one year (R = .808652) was obtained for the failure in the open mode of nine switch legs per half phase. These reliability figures of merit could be improved especially in the DC-DC converter circuitry and low level logic by the use of redundant circuitry. The reliability of the power stages could be improved by using more redundant switch legs.

A detailed design study had been completed for the 400 cps - 10 KW static inverter using classical pulse width modulation and natural sampling. A conceptual design was created using the Methodology plan as a design guide. Complete electrical circuits and their parts lists, and all reliability numbers, weights, and losses were based on this theoretical design and should only be used as a guide for this conceptual design. Improvements in efficiency, weight, and reliability should be realized if this conceptual design is fabricated and tested. Assuming that the 400 cps - 10 KW static inverter design is performing to the Methodology plan, a detailed reliability analysis may be conducted in which the electrical and thermal stresses of each circuit component are carefully measured. The overall reliability can then be computed with a high degree of confidence. Reliability recommendations may be incorporated into

the circuitry wherever possible to improve the inverter's reliability figure of merit. Intangible items such as heat sinks, connectors, terminal boards, fuses, etc., in the theoretical design may now be accurately determined in the breadboard phase so that a final package configuration can be established. Shock, vibration, and other environmental conditions will also be considered for this final package design.

The present conceptual design does not use a bulky power output transformer. The elimination of the power output transformer allows the power output stages to be readily adaptable to modular construction. Therefore, each switch leg in each half phase can be constructed as a simple module that can be easily replaced. The modular construction techniques allow these power output stages to be easily scaled to any power capacity by adding or removing switch leg modules which are connected in parallel for each half phase. For example, the present 10 KW inverter with a 250% overload capacity can be reduced to a 4 KW inverter with a 250% overload capacity with the removal of nine of these switch leg modules per half phase. The driver stages, output filter components, DC-DC converter, and current feedback circuitry will also require modifications in order to be compatible with the power output stages. Modular construction will be used in these circuits where possible to simplify these modifications.

At present, the conceptual design offers a lightweight (147.54 lbs. total component weight) and a fairly high efficient (80.4% overall at full load and .7 P.F.) inverter. However, its overall reliability figure of merit will have to be improved considerably either through the use of redundant circuitry or with less complex circuit designs.

A minimum safety factor margin of two was used for a design goal in this theoretical design wherever possible. Circuits which employ components that cannot meet this design goal will be thoroughly investigated in order to determine alternate approaches that can be used. Thus, the use of two power transistors in series per switch leg can be eliminated if an equivalent transistor with an 800 V_{CE} voltage rating could be found. This would eliminate divider resistor losses (144 watts) and cut the base driver power requirements in half (save 270 watts) making a more efficient inverter.

Therefore, the conceptual design will require more design considerations together with extensive breadboard testing of the individual circuitry before an optimum 400 cps - 10 KW static inverter design can be realized whose electrical parameters will either comply with or exceed those defined in the Methodology plan.

BODY OF REPORT

GENERAL INFORMATION

I. DESCRIPTION OF INVERTER TYPES

A. Introduction

Solid state inverters are designed almost exclusively around two types of switching elements: silicon controlled rectifiers (SCR's) and transistors. The difference between these, of course, is the lack of ability to turn off the SCR at the gate; an external means must be provided to reduce the current in the SCR to zero. Provision must be made for this in all circuits using SCR's. In some circuits, this turn-off is an inherent part of the circuit; in others it is inherent for some load ranges, while in still others extra components must be added to provide this turn off. Series type inverter circuits which are used almost exclusively with SCR's are of the first two types. Their permissible load change, however, is limited to approximately 3 to 1. Parallel inverters (which are used with both SCR's and transistors) generally belong to the last class.

B. Parallel Inverters

a) Simple Parallel Inverter

The basic parallel circuit is shown in Figure 4-1. Here the switching elements are shown as switches, since both transistors and SCR's are used in this circuit. For use with SCR's the components shown dotted must be included to provide for proper commutation of the SCR's.

The transistorized circuit puts out a square wave voltage into a resistive load; the output voltage of the SCR inverter, because of the resonant effects of L and C is a complex function of the value of L, C, the operating frequency, and the load. For the graphical presentation of the results of a steady state analysis of this type of inverter, the reader is referred to the literature "Parallel Inverter with Resistive Load"[4], and "Parallel Inverter with Inductive Load"[5].

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4 "Parallel Inverter with Resistive Load", C.F. Wagner, A.I.E.E. Transactions, V54, November, 1935, pp. 1227-1235.

5 "Parallel Inverter with Inductive Load", C. F. Wagner, A.I.E.E. Transactions, V55, September, 1936, pp. 970-980.

Unfortunately, these papers do not investigate the operation of the inverter under unloaded or switched conditions. It can be shown as follows that this inverter will not operate under no load conditions.

Consider any one half cycle of inverter operation. The equivalent circuit of Figure 4-1, under no load conditions, is shown in Figure 4-2. If we assume that the SCR's are alternately gated on at a frequency w_o lower than the resonant frequency of the commutating components $w_c = \frac{1}{4\sqrt{LC}} > w_o$ then, at the time of the closing of S, there is no current in the circuit. When S is closed, the following differential equation applies to this circuit:

$$L\frac{di}{dt} + \frac{1}{4C}\int_o^t i\,dt = E + v_o \qquad \left[\begin{array}{l} i_{/t=0} = 0 \\ \frac{di}{dt}_{/t=0} = \frac{E+v_o}{L} \end{array}\right. \quad (4-1)$$

This has the solution:

$$i = 2\sqrt{\frac{C}{L}}\,(E+v_o)\,\sin\,\frac{t}{2\sqrt{LC}}$$

The solution, however, is only valid for $i \geq 0$, since S only conducts in one direction. Thus, this solution is valid only for $0 \leq t \leq 2\pi\sqrt{LC}$. During this time, the capacitor voltage changes from v_o to

$$v_o - \frac{1}{4C}\int_o^{2\pi\sqrt{LC}} i\,dt = v_o - \frac{1}{4C}\int_o^{2\pi\sqrt{LC}} 2\sqrt{\frac{C}{L}}(E+v_o)\,\sin\frac{t}{2\sqrt{LC}}\,dt$$
$$= -v_o - 2E.$$

Thus, in each half cycle, the equivalent capacitor (4C) voltage increases by 2E, or the voltage on the actual capacitor C_c increases by 2 (2E) = 4E. Therefore, either the output transformer will soon saturate from the overvoltage or one of the SCR's will conduct, in either case resulting in a double fire or latch-up condition where both SCR's are conducting simultaneously. This is indicated in the waveform drawing of Figure 4-3, where the voltages are shown building up from the starting condition of $v_o = 0$. For very light loads, a similar situation occurs at start, except an equilibrium condition may eventually be reached if the voltage ratings of all the components are high enough. To handle inductive loads, the commutation capacitance C_c must be large enough to absorb the reflected load current for that part of the cycle during which the load is returning energy to the inverter (i.e. the load voltage and current are of opposite sign) without having the capacitor voltage rise to a destructively high value. This is also discussed in the literature previously cited in "Parallel Inverter with Inductive Load".[5]

[5] op. cit.

For an inverter which must operate over a wide range of (lagging) power factors, this can result in a considerable excess of commutation capacity at normal or light loads, giving rise to a condition similar to the no load case described. Thus, this type of inverter is not suited for general purpose applications where the load is of variable magnitude and power factor. This inverter, like all SCR parallel inverters also will not operate if the load impedance becomes too small. A detailed discussion of the reasons for this limitation in the case of the McMurray-Bedford circuit is found in Appendix 4-I; the same reasoning can be applied to this configuration. Depending on the values of L, C, load, and operating frequency, an SCR which has been conducting may either be turned off by the attempt of the current in it to reverse its direction, or by the action of the commutating capacitor in pulling the anode voltage of one SCR negative when the other SCR is first turned on.

b) The McMurray-Bedford Parallel Inverter

Improved operation of this circuit can be realized by the addition of so-called "reactive" diodes to provide a path for reactive currents which formerly went into the commutating capacitor (for the SCR circuit). This allows operation for all load power factors. The reactive diodes also serve to limit the voltages under no-load conditions, (the capacitor voltage is held to 2E) so that operation under no-load is now possible. The new circuit is shown in Figure 4-4; again, the additional parts required for an SCR inverter over a transistor inverter are shown. A detailed analysis of the operation of the SCR parallel inverter with reactive diodes (the McMurray-Bedford circuit) is given in Appendix 4-I. Waveforms of the SCR inverter at startup and steady state are given in Figures 4-I-11 and 4-I-12.

C_c is chosen according to Equation 4-I-15 to provide the desired minimum turn-off-time (e.g. 20 usec) for the SCR's under the worst condition of commutating the maximum current at the minimum capacitor voltage. L_C is generally chosen to resonate with C_C at a frequency with half period approximately twice the turn-off-time. This is only a guide and L_C may be varied as desired, keeping in mind the following effects:

For a constant C_C, source voltage, and current to be commutated:

1) As L is decreased, the available turn-off time is decreased because the commutating capacitor can be discharged more rapidly. Refer to Equation 4-I-29.

2) As L is decreased, the peak charging current to the capacitor is increased (Equation 4-I-2) although the average value (which determines the energy delivered to the capacitor) remains approximately constant; thus, the rms value of the current is increased, resulting in increased i^2R losses in the choke and output transformer.

3) As L is increased, the circuit is more affected by suddenly changing loads. A sudden increase in load currents results in a voltage developed across L in such a direction as to cause the commutating capacitor C_C to partially discharge into the load. If L is too large, this effect can cause circuit failure upon load switching.

Because of the action of the reactive diodes in providing a path for reactive currents and limiting the capacitor voltage under light loading, this circuit will operate and start under a wide range of load magnitudes and power factors; however, should the load become too heavy, resulting in excessive currents at the time of commutation, then according to Equation 4-I-15, the circuit provided turn-off time is decreased and the inverter malfunctions.

c) Gate-Controlled Switch Parallel Inverter

Idealized waveforms for a transistorized or gate controlled switch (GCS) parallel inverter operating with a resistive load are shown in Figure 4-5. These are much less complex than those of the SCR inverter as shown in Figure 4-I-11 because of the absence of the commutating choke and capacitor from the circuit of Figure 4-5. Table 4-I compares the various types of SCR inverters with respect to several parameters such as weight, efficiency, etc. These ratings are based on 400 cps inverters with 5% total harmonic distortion and operating at the 1 KW level. This table shows that, in general, for fixed load operation, the series inverter is superior, but for large load variations, the McMurray circuit is favored.

II. VOLTAGE REGULATION

The output voltage of all the inverters mentioned previously was a direct function of the D.C. input voltage and could be varied by changing this voltage. A series or phase shift A.C. output regulator or a D.C. voltage regulator may be used to regulate the output voltage of these inverters. These regulators are controlled by an error signal that is developed by comparing the A.C. output voltage with a reference to provide a closed loop control of the inverter output voltage. The following discussion will deal in detail only with the D.C. voltage regulators.

A. Series Proportional D.C. Regulator

The simplest type of d.c. regulator (and the lightest, if heat sink requirements are not considered) is the series regulator, shown schematically in Figure 4-6 and equivalently in Figure 4-7.

For a load current I, the power input to the regulator (neglecting the power required by the low level control and sensing circuits) is VI, and the power output of the regulator is $V_o I$. Thus, the maximum efficiency is

$$\eta = \frac{P_o}{P_i} = \frac{V_o I}{VI} = \frac{V_o}{V} .$$

Thus, for greatest efficiency, the output voltage should be as close as possible to the input. However, the regulated output can never be greater than the least value of the input; therefore, for any but small variations in voltage, this regulator becomes rather inefficient. Furthermore, the power lost in the regulator, $(V - V_o) I$, is all dissipated in the series control element which must then be adequately heat-sinked.

B. Series Switching D.C. Regulator

One of the first switching type d.c. regulator circuits used the same series transistor as the simple series regulator, but turned it full on or full off depending on how the output voltage compared with a reference. A simple LC filter smoothed out the large voltage variations caused by this switching, and a flyback diode was added to provide a path for the choke current during the periods when the series switch was off. The resulting circuit is shown in Figure 4-8, and the waveforms in such a circuit in Figure 4-9. The losses in this circuit are less than those of Figure 4-6, for most cases and can be analyzed as follows:

Assuming a switching period of τ and a choke large enough so the current is approximately constant, the "on" time t_1 is approximately related to the period and the input and output voltages by the equation

$$V_o = \frac{t_1}{\tau} V_{in} \qquad (4\text{-}2)$$

Therefore for a load current I_o, the losses in the circuit will be:

1. $I_o^2 R_L$ in the series choke
2. $I_o V_S \frac{t_1}{\tau}$ in the series switch
3. $I_o V_D \frac{(\tau - \tau_1)}{\tau}$ in the flyback diode

where V_D is the forward drop across the flyback diode, V_S is the forward drop across the series switching element and R_L is the resistance of the filter choke. It can be seen that these losses are independent of the input and output voltages. This is strictly true only for the case where $V_S = V_D$; otherwise the losses will vary slightly as the ratio of input to output voltage changes, because the time ratios t_1/T and $\frac{T-t_1}{T}$ will vary as this ratio changes. Thus, this circuit is suitable in applications where the input and output voltage of the regulator may differ by large amounts. Because of the choke, it is heavier (for a given current) than the circuit of Figure 4-6, but this difference can be minimized by performing the switching at as high a frequency as possible (consistent with transistor switching losses) to reduce the choke size. Since this is a switching type regulator, it is also possible to use SCR's or GCS's in place of the transistor. With SCR's the circuits become more complex, again because of the necessity of having some method for turning the SCR off. A typical circuit (the Morgan Chopper) and its waveforms are shown in Figures 4-10 and 4-11. The operation of this circuit is discussed in the literature.[6]

Both the transistor and SCR series type switching regulators provide an output voltage which can be no greater than the input.

C. Shunt Switching D.C. Regulator (Bedford Step-up Circuit)

The newly developed Bedford circuit shown in Figure 4-12 removes this restriction by providing an output not less than the input voltage.[7] It operates in the following manner: (refer to Figure 4-12 and the waveform Drawing 4-13). Transistor S performs the same function as a single pole - single throw switch. When transistor S is turned on (saturated) the only current path provided for the source is through the inductor L and the saturated transistor S, thus making $I_i = I_s$. During this time the current through the inductor is building up. When the transistor S is turned off (unsaturated), the current Is through this transistor drops to zero. However, the charging current I_i through the inductor L is maintained by flowing through diode D into capacitor C and the load. Capacitor C is charged up causing a decay in the inductor current (because the output voltage becomes greater than the input voltage) until the transistor S turns on again. Diode D is used

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6 "Silicon Controlled Rectifier Manual", General Electric Company, p. 149-151.

7 "Quarterly Progress Report No. 4 on Voltage Regulation and Power Stability in Unconventional Electrical Generator Systems" (ASTIA #AD265158), p. 87.

to isolate the capacitor C and load from the charging circuit composed of indicator L and transistor S thus preventing the capacitor from being discharged through transistor S when it is turned on. While transistor S is turned on and current is building up in L, the load current is supplied entirely by capacitor C. With an input of V_i volts and I_i amps, and an output of V_o volts ($V_o > V_i$) and I_o amps ($I_o < I_i$) the average current carried by the switching element is $I_i - I_o$, and the average current carried by the diode is I_o.

Assuming an inductor resistance of R_L, diode drop of V_{D_2} and switching element drop of V_S, the losses in this circuit are then $I_i^2 R_L + (I_i - I_o)V_S + I_o V_D$. Again, this is independent of the input and output voltage to the same degree as the losses of the series switching inverter.

Figure 4-13 shows the waveforms in the Bedford circuit for a step-up ratio of 2:1.

D. Inverter-Rectifier D.C. Regulators

Other circuits for d.c. regulation involve changing the d.c. to square wave a.c. with a simple parallel inverter, and then operating on this a.c. with various types of modulators and rectifiers. Though more complex than the previous techniques described, this method is of advantage where the raw d.c. input is not near a value that can be readily used by the inverter; any desired amount of step-up or step-down in voltage can be obtained with this technique by simply varying the turns-ratio of the inverter transformer. Since this incorporates inverter stages, which will be discussed in great detail later, and furthermore could not be advantageously used to provide a more optimum d.c. voltage level to drive an inverter (since it itself is an inverter and would have to work at the least optimum voltage), this method will not be discussed further.

E. Buck Boost D.C. Regulators

A modification of the above technique is the use of a square wave inverter-modulator-rectifier to provide only the difference voltage between the raw d.c. input and desired d.c. output. Its output is then connected in series with the d.c. input to provide the regulated output. The advantage of this system is that the inverter-modulator is required to pass only the error power instead of the total d.c. load. The output rectifiers still pass the full load current, however, so the losses here are not decreased. The circuitry used in this technique is shown in Figure 4-14. This circuit can be designed to subtract from as well as add to the raw d.c. input voltage; if this is done, the maximum error power required is reduced by a factor of

two, since the maximum output voltage of the regulator can be halved when its output can assume either polarity.

F. Quasi-Square Wave Regulation Techniques

a) Quasi-Square Wave Power Stage

Another method for voltage regulation involves increasing the complexity of the basic inverter circuit to provide for changing the output waveform of the inverter as required. One of the simplest outputs resulting from this is called a quasi-square wave and is illustrated in Figure 4-15.

Harmonic analysis of the resultant wave (shown in Figure 4-15) indicates the variation of the fundamental component of this wave with the dwell angle ϕ.

$$v(t) = \frac{4V}{\pi}\left[\sin wt \cos \phi + 1/3 \sin 3 wt \cos 3\phi + 1/5 \sin 5 wt \cos 5\phi + \frac{1}{2m-1} \sin (2m-1) wt \cos (2m-1)\phi\right] \qquad (4\text{-}3)$$

Where the harmonic number (2m-1) is determined by m which ranges from one (1) to infinity (∞). (m=1, 2, 3, 4 ----∞).

Hence, by changing ϕ, the peak amplitude of the fundamental component of the above wave can be varied between $\frac{4V}{\pi}$ and 0.

With transistors and a resistive load, this can be easily accomplished by only turning them on when an output is desired, instead of always having one on. This is indicated in the waveform drawings of Figure 4-5. When using SCR's the problem is more complex, since in all the circuits for parallel inverters discussed so far, the only way one SCR is turned off is to turn the other one on. Hence, in SCR inverters, additional circuitry is required to produce the output waveforms of Figure 4-5.

III HARMONIC REDUCTION

In general, the harmonic distortion of the unfiltered output of these switching circuits is too high for many applications. Two obvious solutions are to either filter the output to remove the undesired harmonics or to use circuits which produce less harmonics. The optimum design is usually a combination of these two, since it is not too difficult to construct an inverter that suppresses the lower harmonics in the switching stages, and the higher ones are readily attenuated by simple filters.

A. Single Step Waveforms (Quasi-Square Wave)

The simple quasi-square wave, with $\phi = 30°$ has no third harmonic;

three such waves each displaced by 120°, can be generated in a simple 3 phase bridge circuit as shown in Figure 4-16. This can provide a good start for a three phase inverter; however, holding ϕ at 30° (or any other fixed value) means giving up the voltage regulation capability of the quasi-square wave. Thus, some additional means is required for voltage regulation in situations where ϕ is held fixed for harmonic reduction purposes.

B. Multi-Stepped Outputs

Another method for reducing the distortion produced by the switching stage is to use a more complicated switching arrangement which is capable of providing intermediate values of output. Such a circuit is shown in Figure 4-17. Here the switches (either transistors or SCR's may be used) are closed in the proper sequence to provide the stepped waveform also shown in Figure 4-17. In this scheme, the switches farthest from the center tap provide the lowest output voltage, etc. Providing for reactive current in a scheme such as this can be a problem unless certain switches can be made bi-directional. It is also possible to produce such a waveform by adding a number of square waves of proper phase relationship in a technique which is an extension of that shown in Figure 4-18. These more advanced switching techniques become more advantageous in multiphase inverters because several gating signals will be common to two phases; the control section for a three-phase multistepped inverter cannot be appreciably more complex than that for a single phase unit. Voltage regulation in these more complex techniques may be obtained by a d.c. input regulator, by varying the width of some step in the waveform, or by adding together two such waveforms with a variable phase difference.

C. Constant Voltage Transformer Techniques

A combination of voltage regulation and harmonic suppression can be obtained through the use of special ferro-resonant transformers designed for this purpose (e.g. the Sola transformer). These, however, have fairly high no-load losses and an output voltage somewhat sensitive to load power factor. They afford a very simple and reliable means of voltage regulation and harmonic suppression and also provide short circuit protection. When starting unloaded or operating under switched loads, they sometimes draw large spikes of magnetizing current, successful operation of an SCR inverter power stage under these conditions required a large commutation capacity when compared to normal demands.

D. Static Tap Changing

One technique of voltage regulation which can be useful under certain conditions is static tap changing. As shown in the diagram of Figure 4-19, this uses semiconductors acting as switches S_1, S_2.... to connect one of several possible taps on the output transformer to the load. Two representative techniques for utilizing SCR's and transistors in a.c. (bidirectional) static switches are shown in Figure 4-20. Which tap is selected will depend on the load and input voltage to the transformer. This technique has the advantage that it allows voltage regulation of a complex multistepped waveform without introducing distortion or phase shift as would be the case with a conventional on-off output modulator. This would be especially useful in a situation where the input voltage was very low so that an additional semiconductor in series with the input side (as would be the case with a conventional d.c. input regulator) would result in excessive losses, but where the output voltage of the switching stage transformer was high enough so that the drop in the static tap changing switching elements would represent a negligible fraction of the output power. The disadvantage is the large number of taps, and hence semiconductors required when either the d.c. input voltage to the power switching stage varies over a wide range (compared to the permissible variation in output) or the output voltage tolerance is so stringent that variations in output due to changes in load require a large number of taps.

E. High Frequency Techniques

SCR's could also be used to modulate a high frequency square wave to obtain a pulse-width modulated output like that of Figure 4-21. A block diagram of such a system is shown in Figure 4-22. Other techniques for low order harmonic reduction are the various types of pulse modulation. The switched output and fundamental component of such a circuit is shown in Figure 4-21. These waveforms would be generated by circuits similar to those already discussed for square waves; the only difference being that the circuit is switched several times in each cycle. In these circuits, switching losses become much more significant, and components designed especially for high frequency use become a necessity. Figure 4-23 corresponds to a high frequency version of the quasi-square wave and can be generated by circuits similar to those used for the usual quasi-square waves. The advantage of the waveform of Figure 4-21 over that of Figure 4-23 is discussed further in a following section (Section II-A, B, of 400 cps - 10 KW P.W.M. Inverter Design).

The advantages of these high frequency techniques lie in the size and weight reductions possible both from high frequency operation and from the fact that the harmonics present in the unfiltered output are of a very high frequency compared to the fundamental, simplifying filtering. The main disadvantage is the increased switching loss. There is also presently a rather limited selection of semiconductors in the high power high frequency field. It might also be mentioned that unlike inverters of the quasi-square wave plus brute force band-pass filter design, which are restricted to sine-wave outputs, pulse width modulation inverters, which can efficiently use low-pass filters, are capable of providing any desired waveforms with highest frequency harmonic below the cut-off of the particular filter used.

F. Passive Filters

Filters used for the outputs of the simpler inverter circuits generally consist of a series element (which is generally series resonant at the fundamental frequency) and a shunt path (which is capacitive at high frequencies and may be tuned to parallel resonance at the fundamental frequency). The series section may also have impedance poles at those frequencies of greatest harmonic magnitude. The shunt section may likewise have impedance zeroes at appropriate harmonics. The basic filter concept is shown in Figure 4-24. In general, it is desirable to have the series element provide a low impedance path for the fundamental and a high impedance to harmonics. This first allows the fundamental current to pass without voltage drop from the inverter switching stage to the load, while the high harmonic impedance prevents harmonic currents from flowing in switching stages, thus reducing dissipation. Similarly, the shunt path ideally presents an open circuit to the fundamental and a nearly short circuit to harmonic currents. (These harmonic currents may be the small amount that get through the series filter section, along with any due to load non-linearily.) As mentioned previously, pulse width modulation filters can be of the low pass type since the pulse width modulation waveform is essentially free of the lower order harmonics.

One proposed method for harmonic reduction in polyphase systems involves the use of a distributed transformer to couple the switching stage to the load. This can best be described as a wound rotor induction motor with locked rotor and having fractional pitch windings and skew selected to eliminate specified harmonics.

G. Active Filters

Another method of harmonic reduction is the use of active filtering. This involves using an error amplifier to make up the difference

between the switching stage output and the desired sine wave output as provided by a sine wave reference source. A block diagram of such a system is shown in Figure 4-25.

3200 CPS - 10 KW INVERTER DESIGN

I. INTRODUCTION

Two basic power inverter approaches were considered for this 3200 cps - 10 KW Inverter Design. The first approach utilized the Pulse Width Modulation techniques while the second approach employed the Multi-Stepped Waveform techniques. The Pulse Width Modulation approach was found to produce excessive switching losses when operating at the power frequency of 3200 cps. This resulted because switching devices with reasonable current capacities could not be found with the necessary switching speeds ($t_s < .1$ us) to minimize these switching losses when switching at the minimum modulating frequency of 16,000 cps. Therefore, the Multi-Stepped Waveform approach was chosen for this 3200 cps - 10 KW inverter design.

A preliminary comparison between two 10 KW - 3200 cps inverters, one using SCR's and the other using transistors was made on the basis of the calculated weights, efficiencies, and parts count. The results indicate that although the SCR inverter has only half the parts count as the transistor inverter, its efficiency is less (64% versus 70%) and its parts weight is higher (62.25 lbs versus 50 lbs) than its transistor counterpart. (Tables 4-2 and 4-3 are used to compare efficiency, weight, and parts count of both inverters.) Because of the higher efficiency and lower parts weight offered by the transistor inverter, the circuit design was concentrated on the multi-stepped transistorized output inverter approach. The following sections are used to establish this 3200 cps - 10 KW Inverter Design.

II. STEPPED WAVEFORMS

The basic requirements of Stepped Waveforms on the reduction of Harmonic Distortion outlined in Section III-B (Multi-Stepped Outputs) are examined in more detail in this section. A variety of stepped waveform characteristics that have been proposed by contributors to the field of static inverters were investigated in an effort to reduce the size of the filter requirements for an allowable harmonic distortion level and yet maintain complexity of the inverter circuitry to a minimum.

The waveforms evaluated here are classified first as to the number of horizontal steps that can be counted in a full cycle. Therefore, a wave can be classified simply as an "eight" step or a "six" step waveform merely by counting the steps. Further subclassification is then made by determining if the steps occur at equal or unequal time intervals and are called either equal time or unequal time waveforms respectively. The next subclassification made is whether the step heights are equal or not

equal in amplitude and are called equal height or unequal height waveforms respectively. We now have a system that can classify any stepped waveform that is used to synthesize a sine wave.

Table 4-4 lists the waveforms that will be evaluated here. The numbers in the second column signify the number of steps in the waveform.

The stepped waves examined here can be broadly classified into two groups for discussion. The first group are waveforms (phase voltages) that can be divided by the smallest time increment step into an integral even number of parts. (Refer to Figures 4-26 through 4-40.) These waveforms have steps of uniquely optimum height, as some authors put it, that specifically reduce the number of lower harmonics and the harmonics that appear do so at predictable points. Several authors [8, 9] have come upon this relationship which can be made applicable to waveforms fitting this description.

The relationship is that harmonics only appear in pairs according to the equation

$$h = N n \pm 1 \qquad (4\text{-}4)$$

where h is the harmonic number, N is the integer arrived at by dividing the waveform by the smallest time increment step and n is any integer from 1 to infinity. This test can be applied to the waveforms numbered 1, 2, 3, 5, 6, 7, 9, 11, 12, 14 and 15 illustrated in Figures 4-26 to 4-40. A proof of the validity of this relation can be made by selecting a waveform and expressing it as a Fourier series and then examining the harmonics. Waveform 6-P will be used as an example (refer to Figure 4-31).

The waveform is described as a six step-unequal time-unequal height waveform. However, by dividing the waveform by the smallest time increment between steps (45°), the integer eight is obtained which fits the basic requirement previously stated. The harmonic numbers are then:

$$h = 8 n \pm 1 \qquad (4\text{-}5)$$

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8 "Methods For Optimizing the Waveform of Stepped - Wave Static Inverters", P.D. Corey, A.I.E.E. Paper No. CP-62-1147.

9 "Static Power Inverter Utilizing Digital Techniques and Harmonic Cancellation", D. L. Anderson, A. E. Willis, C. E. Winkler, A.I.E.E. Paper No. CP-62-1148.

according to this equation the only harmonics will be

n	=	1,	h	=	7, 9
n	=	2,	h	=	15, 17
n	=	3,	h	=	23, 25
n	=	n,	h	=	8 n ± 1

This can be proved by examining the Fourier series expansion of the waveform which is:

$$e = \frac{4V}{\pi}\Big[(1+\sqrt{2}\cos 45^\circ)\sin wt + 1/3(1+\sqrt{2}\cos 135^\circ)\sin 3wt + 1/5(1+\sqrt{2}\cos 225^\circ)\sin 5wt + 1/7(1+\sqrt{2}\cos 315^\circ)\sin 7wt + 1/9(1+\sqrt{2}\cos 45^\circ)\sin 9wt + 1/11(1+\sqrt{2}\cos 135^\circ)\sin 11wt + 1/13(1+\sqrt{2}\cos 225^\circ)\sin 13wt + 1/15(1+\sqrt{2}\cos 315^\circ)\sin 15wt + 1/17(1+\sqrt{2}\cos 45^\circ)\sin 17wt + 1/19(1+\sqrt{2}\cos 135^\circ)\sin 19wt + 1/21(1+\sqrt{2}\cos 225^\circ)\sin 21wt + 1/23(1+\sqrt{2}\cos 315^\circ)\sin 23wt + 1/25(1+\sqrt{2}\cos 45^\circ)\sin 25wt + \ldots + \frac{1}{(2n-1)}(1+\sqrt{2}\cos(2n-1)45^\circ)\sin(2n-1)wt\Big] \qquad (4\text{-}6)$$

By examining the harmonic coefficients it can be seen that the third, fifth, eleventh, thirteenth, nineteenth, and twenty-first are equal to zero. The only harmonics present are the seventh, ninth, fifteenth, seventeenth, twenty-third, twenty-fifth, and the (8 n±1)th as predicted by the relationship. The magnitude of the harmonic can also be derived by inspection as (1/h) times the magnitude of the fundamental.

The second group of stepped waveforms are those which have been specifically designed to have either the minimum total harmonic distortion possible for a waveform having a particular number of steps, or designed specifically to eliminate certain harmonics. Waveforms fitting this description are shown in Figures 4-29, 4-33, 4-35, and 4-38.

Figures 4-29, 4-35 and 4-38 were derived by Mr. Paul Vergez[10] of Texas Instruments. Mr. Vergez used a digital computer to determine the proper

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10 "Electronic Design", April 26, 1964, pp. 36-42 by Paul Vergez.

time increments and step heights that yield the waveform with the minimum total harmonic distortion for a particular number of steps. Figures 4-29, 4-35 and 4-38 shown in this report have been normalized to conform with the method established for constructing waveforms, namely the first step is of unit height V.

Figure 4-33 is also in the second group and has been specifically designed to eliminate the third and fifth harmonics and all multiples of the third and fifth harmonics. This characteristic is evident by examining the Fourier series expansion of the waveform which is:

$$e = \frac{4V}{\pi}\Big[(\cos 12^\circ + \cos 48^\circ)\sin wt + 1/3(\cos 36^\circ + \cos 144^\circ)\sin 3wt + 1/5(\cos 60^\circ + \cos 240^\circ)\sin 5wt + 1/7(\cos 84^\circ + \cos 336^\circ)\sin 7wt + \ldots + \frac{1}{(2n-1)}(\cos(2n-1)12^\circ + \cos(2n-1)48^\circ)\sin(2n-1)wt\Big] \quad (4\text{-}7)$$

From the expansion it can be seen that the coefficients of the third and fifth harmonics are zero (cos 36° = -cos 144° and cos 60° = -cos 240°). The multiples of the third and fifth harmonic are also equal to zero;

$$\cos n\,36^\circ = -\cos n\,144^\circ$$

and

$$\cos n\,60^\circ = -\cos n\,240^\circ$$

The application of the stepped waveforms to static inverters demands certain characteristics of the waveform for three phase operation. The waveforms discussed in this report have their characteristics tabulated in Table 4-4 and the item of interest here are the columns listing the number of square wave inverters required to generate a single phase voltage and a three phase voltage.

In some of the waveforms, a single square wave inverter may supply two or even three phases with a required step and therefore be a more optimum choice. Waveforms requiring no increase in the number of basic square wave inverters to generate three phases compared to the number required by a single phase are obviously the most optimum choices. Waveforms having this desirable characteristic are shown in Figures 4-30, 4-37, and 4-40.

Waveforms which are complementary to Figures 4-37 and 4-40 are shown in Figures 4-36 and 4-39 respectively. In these waveforms, the number of inverters required to generate a three phase voltage are the same as those in Figures 4-37 and 4-40, but one less square wave is required to generate a phase voltage. This feature is an advantage in single phase inverters but of no particular advantage in a three phase inverter because

the phase loads are less equally distributed among the square wave inverters.

Figure 4-33 is the next most optimum waveform based on the criteria established above. For use in a three phase inverter, no other feature of this waveform appears to be any advantage except perhaps the fact that all the secondary windings required to generate the waveform are equal.

The only other waveforms useful for three phase inverters based on the criteria are illustrated in Figures 4-28 and 4-30 which are complementary.

The other waveforms (Figures 4-26, 4-27, 4-29, 4-31, 4-32, 4-34, 4-35, and 4-38) are totally unsuitable for three phase inverters based on the criteria of multiple base use of a single square wave. Each of these waveforms require three times the number of square wave inverters for three phase use as compared to single phase use.

Another consideration, while not pertinent to the ground rules which established a four wire three phase connection, is whether the phase voltages can be connected in delta. In order to be connected in delta, the instantaneous voltage sums of the phases must be equal to zero. Waveforms which meet this requirement are shown in Figures 4-28, 4-30, 4-36, 4-38, 4-39, and 4-40.

When using stepped waveforms to synthesize a sine wave, it is usually necessary to filter the output voltage to reduce the total harmonic distortion. If harmonic elimination filters (LC tanks) are used to reduce the harmonic distortion, the new total harmonic distortion can be approximated by using the following equation:

$$\text{T.H.D.} = 100 \sqrt{\left(\frac{e_t}{e_f}\right)^2 - \left(1 + \sum \frac{1}{h^2}\right)} \qquad (4\text{-}8)$$

where

T.H.D. = total harmonic distortion

e_t = root-mean-square value of waveform before filtering

e_f = root-mean-square value of fundamental component of waveform

h = order of the harmonic to be removed by filtering

Example: (4-1)

Assume Waveform in Figure 4-33 is used in an inverter. What is the new

total harmonic distortion if a filter is used to eliminate the 7th and 11th harmonics ?

$e_t = 1.5055$ V

$e_f = 1.483$ V

$h = 7$ and 11

Therefore

$$T.H.D. = 100 \sqrt{\left(\frac{1.5055}{1.483}\right)^2 - \left(1 + \frac{1}{7^2} + \frac{1}{11^2}\right)}$$

$$= 100 \sqrt{(1.0152)^2 - (1.0287)}$$

$$T.H.D. = 4.36\%$$

or a reduction of

$$\frac{17.4 - 4.36}{17.4} \times 100 = 74.9\%$$

This method will determine what harmonics must be removed to meet a particular T.H.D. Specification.

A. Note on Stepped Wave Analysis

In the course of analyzing the stepped waves presented in this report, a useful mathematical method was developed. This method permits the user to write the Fourier series expansion of periodic stepped waves having axis symmetry and half wave symmetry by simple inspection methods described here.

The waveform must first be normalized by setting the amplitude of the first step to a unit quantity and the amplitude of all the other steps as a function of this unit quantity. See Example 4-2.

The series expansion is then written as a sum of sine terms with cosine coefficients as follows:

$$e = \frac{4V}{\pi}\Big[(1\cos\theta_1 + a\cos\theta_2 + b\cos\theta_3 + \ldots + \propto \cos\theta_N)\sin wt +$$
$$1/3(1\cos 3\theta_1 + a\cos 3\theta_2 + b\cos 3\theta_3 + \ldots + \propto \cos 3\theta_N)\sin 3wt +$$
$$\ldots\ldots + \frac{1}{(2n-1)}(1\cos(2n-1)\theta_1 + a\cos(2n-1)\theta_2 + b\cos(2n-1)\theta_3 +$$
$$\ldots\ldots + \propto \cos(2n-1)\theta_N)\sin(2n-1)wt\Big] \qquad (4-9)$$

From this expansion it is possible to determine by elementary manipulation which harmonics cancel, the amplitude of any harmonic, and what step amplitudes or angular division must be varied to eliminate a particular harmonic.

Example: (4-2)

Assume the normalized waveform e(t) in Figure 4-41.

The following equation may be written for this waveform (Figure 4-41).

$$e = \frac{4V}{\pi}\Big[(\cos\Theta_1+a\cos\Theta_2-b\cos\Theta_3)\sin wt$$
$$+1/3(\cos 3\Theta_1+a\cos 3\Theta_2-b\cos 3\Theta_3)\sin 3wt$$
$$+1/5(\cos 5\Theta_1+a\cos 5\Theta_2-b\cos 5\Theta_3)\sin 5wt$$
$$+1/7(\cos 7\Theta_1+a\cos 7\Theta_2-b\cos 7\Theta_3)\sin 7wt$$
$$+\ldots \frac{1}{(2n-1)}(\cos(2n-1)\Theta_1+a\cos(2n-1)\Theta_2$$
$$-b\cos(2n-1)\Theta_3)\sin(2n-1)wt\Big] \qquad (4-10)$$

Notice that the steps may be negative. Steps that descend rather than ascend are negative.

If it is desired, for example, to eliminate the third harmonic from the waveform the coefficients (a) and (-b) can be changed to cancel the coefficient of $\cos 3\Theta$, thereby eliminating the third harmonic.

III. MAGNETIC COMPONENT STUDIES

An optimum magnetic design requires not only optimization of the individual magnetic components (transformers, inductors, etc.) of any given system but also, of equal importance, an optimum choice of the overall system to be used to perform the specified function. (For example, it will be shown that for purposes of paralleling transistors, under some conditions the use of the split transformer technique is superior to the balancing reactor approach from a weight and loss viewpoint. Clearly, when these conditions are encountered, regardless of how well the balancing reactors are designed, their use will result in a poorer overall system than could be obtained by other means.) What is optimum will depend on the specific application since in general, weight and losses cannot be simultaneously minimized.

To obtain quantitative means for optimizing a system of magnetic components, it is first necessary to determine the characteristics of each component in the system as one or more of its parameters are varied. Accordingly, the transformer (as a typical and common magnetic component) was analyzed to see how its weight and efficiency varied with the size and design. In particular, analyses were made of:

1) The optimum design of a transformer of fixed size to operate at a given power rating.

2) The variation of the size, weight, and losses of such a transformer as its rating is varied.

3) The relationship between the size and losses of a transformer operated at constant power.

4) Multi-phase transformers and circuits utilizing them.

The results obtained from these analyses were then used to investigate the relative merits of several common inverter circuit techniques. The areas investigated were:

1) The weight and loss penalties for using switching elements that must be paralleled.

2) A comparison between different techniques for paralleling. (Balancing reactors versus the split transformer technique.)

3) The use of multiphase transformers to provide simultaneous weight and harmonic reduction.

These analyses and the results obtained from them follow. The mathematically more involved sections are found in the Appendices 2-I through 2-III of Quarterly Report No. 2 of the "Optimization Study of High Power Static Inverters and Converters" - NASA - CR-54021.

A. Optimum Loading of a Fixed Transformer

The general rule regarding the optimum loading of a transformer is that maximum efficiency occurs when the copper loss and core loss are equal.

This result, which is derived in Quarterly Report No. 2 - Appendix 2-I (NASA-CR-54021) under the assumption that the primary copper loss due to transformer magnetization current may be neglected, can be expressed mathematically as

$$\frac{P_c}{P_r} = 1 \qquad (4\text{-}11)$$

where P_c is the total core loss (hysteresis, eddy current, interlaminar and stray losses) and P_r is a total copper loss (and includes, where applicable proximity and skin effects but not, as indicated above, the copper losses due to the component of the primary current which serves to magnetize the core). This derivation, however, was based on the conditions of a constant input voltage and variable load. In practice, however, both the input voltage and maximum design load are generally fixed, and all that the transformer designer can vary is the overall size and/or shape of the transformer and the relative losses in the coil and core.

To start, it will be assumed that the size and shape of the tranformer are fixed, and only the relative core and coil losses can be varied. For a core of fixed size, given material, lamination loss, induction level, and operating at a constant frequency, the only way in which the core losses can be reduced is to reduce the induction level to which the core material is operated. With a fixed size and voltage input, this can only be accomplished by increasing the number of turns on the primary (and hence, in order to maintain the required turns ratio, the secondary turns must be correspondingly increased).

A decrease in core loss in a constant size transformer is thus obtained at the expense of increased copper losses, since not only is the number of turns increased (increasing the winding resistance) but also with the total area available for winding remaining constant, the available cross-sectional area for each turn decreases.

Taking these effects into account, and making use of the approximate empirical relationship

$$P_c = c_1 B^a \qquad (4\text{-}12)$$

where P_c is the core loss/unit volume, B = maximum flux density the core reaches, and c_1 and a are constant (for any given core material and operating frequency), it was shown in Quarterly Report No. 2 - Appendix 2-I (NASA-CR-54021) that the optimum ratio between core loss and copper loss is given by the equation

$$\frac{P_c}{P_R} = \frac{2}{a} \qquad (4\text{-}13)$$

where P_c and P_R are defined as for Equation 4-11.

The relative losses in equal size and weight transformers carrying the same VA with one designed according to Equation 4-11 and the other designed according to Equation 4-13 are computed in Quarterly Report No. 2 - Appendix 2-I and the results plotted in Figure 4-42. From this it can be seen that except for the case where a = 2 (where the two designs are equivalent), the losses in a transformer designed with equal copper and core loss will be greater than those in a transformer designed for a core loss 2/a times the copper loss. The actual differences in loss are not very great, however, as can be seen from Figure 4-42. When these loss variations are translated into efficiency variations, the difference is further suppressed.

B. Scaling of Transformers

Once an optimum transformer is designed at a given power level, and its weight and losses determined, it is often useful to be able to scale the size of the transformer up and down over the power level and thus obtain new designs without extensive calculations. A decision on the various possible methods of paralleling can only be answered with a knowledge of the total transformer weights and losses in the different schemes. Therefore, some useful equations for the scaling of transformers will be developed here. These equations are strictly true only when used to compare transformers of similar construction operating at the same core flux density and copper current density levels.

Consider a transformer with linear dimension L. The window area available for the coils, A_W, is given by $A_W \sim L^2$. For operation at any fixed current density, the cross-sectional area of each turn, A, is directly proportional to A_W and inversely proportional to N, the total number of turns. Also, the current, I, that can be carried in each wire is proportional to the cross-sectional area of that wire. Writing these relations in equation form there results:

$$A_W \sim L^2, \quad A \sim \frac{A_W}{N}, \quad I \sim A \quad = \quad I \sim \frac{A_W}{N} \sim \frac{L^2}{N} \tag{4-14}$$

Therefore, the ampere turn (NI) capability of the coil is given by

$$NI \sim N\left(\frac{L}{N}\right)^2 \quad = \quad L^2 \tag{4-15}$$

When operating at any fixed value of maximum flux density, the volt/turn which the transformer can support is directly proportional to the core cross-section, which is proportional to L^2. Therefore

$$\frac{V}{N} \sim L^2 \tag{4-16}$$

The volt-ampere rating of the transformer is thus given by:

$$VI = \frac{V}{N}(NI) \sim L^2 (L^2) = L^4 \qquad (4\text{-}17)$$

In other words, the rating of a transformer is proportional to the fourth power of its linear dimension. Its weight, W, on the other hand, is directly proportional to the volume which is proportional to the cube of its linear dimension

$$W \sim \text{volume} \sim L^3 \quad \text{or} \quad W \sim L^3 \qquad (4\text{-}18)$$

(Actually, the weight equals (volume of iron x density of iron) + (volume of copper x density of copper), but under the assumptions of the problem, the ratio of the volume of iron to volume of copper remains constant, hence the weight is proportional to the overall volume, even though this volume contains substances of different densities.)

One possible figure of merit for a transformer, its power/weight ratio, is then given by

$$\frac{\text{power}}{\text{weight}} = \frac{VI}{W} \sim \frac{L^4}{L^3} = L \qquad (4\text{-}19)$$

Thus, the figure of merit for a transformer is proportional to its linear dimension.

By combining 4-17 with 4-18, the relationship between weight and power rating may be determined as follows:

$$VI \sim L^4 \sim (W^{1/3})^4 = W^{4/3}$$

or

$$W = K(VI)^{3/4} \qquad (4\text{-}20)$$

Or, the power handling capability of a transformer is proportional to the 4/3 power of its weight, where k is a constant of proportionality.

For the conditions under which the previous equations were derived (namely, constant current density in the windings and constant flux density in the core) the loss per unit volume (or weight) remains constant in all transformer sizes; thus, the total losses are directly proportional to the weight. Or rewriting Equation 4-20 after substituting losses for weight, there results

$$\text{Loss} \sim (VI)^{3/4} \qquad (4\text{-}21)$$

The relationship between the size, weight, and losses of scaled transformers have thus been derived. It should be mentioned that in order for these relations to hold, the scaled transformers should all be similar - that is, all their (linear) dimensions should be changed in the same ratio. This is not a difficult restriction to meet in practice since, for example, all transformers made from a square stack of scrapless E-I laminations (which are all constructed with the same ratios) and having the available window area completely filled with wire would fall into this category. Of course, the conductor and core material must be the same for all the transformers. This analysis holds for either toroidal or laminated cores, single or three phase transformers, as long as the similarity condition is met.

In general, smaller transformers may be designed with higher current and flux densities than larger ones due to the fact that it is easier to get the heat out of a smaller unit. This would reduce the weight of the small transformers but increase the losses still further.

C. Relationships Between Size, Weight and Losses

Quarterly Report No. 2 - Appendix 2-II of the "Optimization Study Of High Power Static Inverters And Converters" - NASA - CR-54021 contains an analysis of the losses in transformers delivering constant power as their size (and hence weight) is varied, thus indicating quantitatively the trade-offs involved in transformer designs. The results of this analysis indicate that to obtain a transformer which operates at a fixed power level and has a minimum weight-loss product, the smallest transformer designed according to Equation 2-I-20 of Quarterly Report No. 2, (NASA - CR-54021) in which the required core flux density is low enough so that Equation 4-12 is valid, should be used. In other words, the core material should be operated as close to its maximum flux density as possible without violating Equation 4-12.

D. Multi-Phase Transformers and Circuits Utilizing Them

Up to now, the analysis of transformer optimization has not had to involve any considerations outside the transformer, since the circuitry associated with the transformer would not be affected by the optimization. This ceases to be the case when three-phase transformers are used, as will be brought out in the following discussion.

Of the various possible power switching stages which may be used for three-phase static inverters, some require the use of three single phase transformers, some work only with three-phase transformers and some may be used with either type. More complex transformer construction than the three-phase is also possible and sometimes useful.[11] In order to be able to use a three-phase transformer, the instantaneous sum of the voltages applied to the three windings must equal zero at all times. This condition is imposed by the flux requirements of three phase transformer core design. This requirement is met, of course, by three equal amplitude sine waves each displaced by 120°. It is also met by three equal amplitude quasi-square waves with an "on" time of 120°. Three square waves, even though separated in phase by 120°, do not fulfill this requirement; thus, inverter power stages which produce square waves cannot use conventional three-phase transformers. The weight savings possible with three-phase transformers will now be investigated.

The core geometry of a single phase transformer made from conventional scrapless E-I laminations is shown in Figure 4-43. If three of these would be combined into a single transformer, keeping the same coil dimensions and core cross-section, the three-phase transformer would have the core geometry as shown in Figure 4-44. If it is assumed that the stack thickness of the original transformer is x (i.e. the stack is square), then the thickness of the three-phase transformer stack will also be x. Since the coils used on the two transformers are identical, the only weight savings will be in the core. The volume of three single-phase cores of the type illustrated in Figure 4-43 will be 18 x^3. The volume of one three-phase core is shown in Figure 4-44 and will be 14.5 x^3. Thus, a saving of approximately 20% in core weight is achieved by the use of a three-phase unit. If, for a rough estimate, the core weight is taken equal to the copper weight, the overall weight savings will be about 10%.

The core configuration of Figure 4-44 is not the only possibility, any more than the single phase core shown in Figure 4-43 is the only one available; variation of the dimension ratios are possible and under some conditions quite desirable. (For example, because of the poorer primary copper utilization in static inverter transformers operating with the center-tapped primary scheme it is advantageous

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11 Design Manual Featuring Tape Wound Cores, Magnetics, Inc. TWX-300, pp. 45-55

to have a larger window area than provided by the conventional scrapless laminations). It is also possible to take advantage of the flux relationships existing in a three-phase system and arrive at a third type of core structure, shown in Figure 4-45. The manufacturer [12] of this type of core claims a 10% weight saving over a conventional three-phase core configuration for this design as well as elimination of magnetic, electrical and physical unbalances caused by the unsymmetrical design of the conventional three-phase core. The drawback of this system is the added complexity of winding coils for it, particularly if it is desired to make maximum utilization of the window area.

It has already been mentioned that, because of their special magnetic construction, three-phase transformers

1) are lighter than equivalent single phase units,

2) require that the instantaneous sum of the voltages applied to them be always zero.

This first item, is of course, an advantage. Single square waves cannot be used with the three-phase transformers since their instantaneous voltage summations do not equal zero. Thus, in order to satisfy the second item, a more complex waveform must be used such as a quasi-square wave. To generate a quasi-square wave usually requires more components and more complex circuitry than a square wave, especially if zero clamping (refer to Quarterly Report No. 1, pp. 30 ff of the "Optimization Study Of High Power Static Inverters And Converters") is required, thus offsetting the weight reduction obtained for the three-phase transformer in item one.

However, the voltage requirement of the three-phase transformer can be used to provide zero clamping without the use of additional components. Consider the circuit and waveforms shown in Figure 4-46. If switches S_1 - S_6 are turned on as indicated, it will be observed that

1) There are always two and only two switches on at the same time.

2) Whenever both switches of any phase are off, the sum of the voltages being produced by the other two phases is zero.

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12 Gulow Transformer Company, Inc.

Thus, whenever any phase has both power switches off (and hence its output voltage would, under normal single phase conditions, be undefined) in this three-phase system, the output voltage of that phase must necessarily be zero. Thus, zero clamping is provided by the power switches of the other two phases, working in conjunction with the three-phase transformer. Because this circuit produced 120° quasi-square waves without the need for any additional zero-clamping components, it appeared quite useful and was investigated further.

One item of interest is how the circuit handles load current which is flowing in the secondary of any phase during the dwell (or zero output voltage) time of that phase. This secondary current cannot be balanced by primary current from the same phase, since the only way that primary current can flow is either through the power switch or reactive diode, neither of which can occur when the output voltage is zero. Examination of the circuit and the magnetic relationships required by the transformer showed that any such secondary current in one phase gave rise to equal currents in the primaries of the other two phases; (for convenience, a 1:1 primary to secondary turns ratio was assumed) one of these induced currents was of such a direction as to represent an energy flow from the d.c. source (and hence went through a reactive diode). Since the two currents were equal, no net energy was transferred through the inverter to the output of that phase, a condition which must necessarily exist since no energy can be transferred under a zero output voltage condition.

Because this extra current in the power switching elements does not contribute to providing any output power, it results in a less effective utilization of the switching devices than would be possible with a simple square wave inverter. This problem of decreased switch utilization is not limited to this particular circuit, however, as a similar effect will occur in any circuit where the final output voltage is a result of the summation of individual voltage waveforms which are not all in phase. Thurs, any of the circuits which provide for harmonic reduction and/or voltage regulation by adding different phased square waves will be subject to the same problem. However, due to the new way in which the proposed circuit (Figure 4-46) operates, it was deemed advisable to actually compare the switching element currents in this circuit to those in the more conventional circuits which use phase shifted square waves for harmonic reduction.

The two circuits compared are shown in Figures 4-48 and 4-49. The line to neutral output voltage of each of these circuits is the same, both in amplitude and waveform, and is shown in Figure 4-47. In this waveform, the first harmonic is the 11th, making for relatively easy filtering.

Regardless of whether SCR's or power transistors are used as the power switching element in these circuits, it is the peak value of the current through the switch which is of interest. This is because in the case of transistors, the transistors themselves must have a current rating greater than the peak current, and with SCR's, the commutating circuit must be capable of turning the SCR's off under peak load current conditions. Hence, an attempt was made to determine the peak currents which would occur in the power switching elements in the two circuits. For the case of the conventional circuit utilizing single phase transformers as shown in Figure 4-48, it is quite easy to put an upper bound on the peak current since, with a peak current of I amperes flowing in each of the three phases, it is obvious that, with the turns ratios as given, the peak current in any primary could not exceed $I(.67 + .5 + .16) = 1.33\ I$ amperes. (The number associated with each secondary of the transformers is the turns ratio of that secondary referred to the primary; the angle given with each switch is the phase angle of the output of that switch section compared to the first, which serves as the reference.)

Due to restrictions on the phase angles of the impedances which may (according to specifications as outlined in the methodology plan), serve as loads on this unit, it is impossible for the peak current in all three phases to occur simultaneously. Thus, the 1.33 I value is in excess of the actual maximum peak current which the switching elements may encounter.

For the three-phase transformer circuit (shown in Figure 4-49), because of the complex fashion in which currents are transferred from one phase to the other two during the zero voltage periods, it is very difficult to see how to choose the individual phase loads (within the permissible load range) in order to maximize the peak current in any one switching element. However, one attempt to do this yielded a peak primary current of 2.7 I amperes, which is over twice that obtained using the phase shifted square waves.

Since both circuits provide the same output voltage, and require the same number of switches, it is obvious that only half the peak current capability is required of the switching elements in the conventional scheme as compared to those in the three-phase transformer circuit. Since the three-phase transformer circuit also requires a more complex driving circuit, it appears that the 10% transformer weight advantage would be more than offset by the additional weight of the extra switch current capacity needed for operation with the three-phase transformer.

A more complex transformer suitable for operation with an input set consisting of six square waves, each shifted by 30°, has been described in the literature.[2] This transformer contains six windows whose outer legs contain both the primary and secondary windings required for each of the six phases. This transformer will be referred to as a "hexadic" transformer because it contains all six-phase primary and secondary windings.

Preliminary investigation of the magnetic paths in this "hexadic" transformer indicates that it would not create the type of circuit problems that the three-phase transformer does. Like the three-phase transformer, the "hexadic" transformer obtains its weight savings by using less iron in those portions of the magnetic circuit where flux cancellations occur. It is estimated that the "hexadic" transformer is 20% lighter than its six single-phase equivalents. This general area of multiple inverters in connection with multiple transformers to produce stepped waveforms approximating sinusoids will be pursued in more detail in the following sections.

E. 3200 CPS Inverter (10KW) Power Stage Transformer Analysis

a) Transformer Analysis

An analysis was made of several possible transformer designs of a complex nature similar to the "hexadic" transformer described by Kernik, Roof & Heinrich.[2] The results of this analysis are given below.

The basic technique used to reduce the weight of these transformers is to utilize the fact that the fluxes in different portions of the circuit are sometimes in such a direction as to cancel one another part of the time. Thus, some sections of the magnetic

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path may be made smaller than would be the case if the fluxes could not be depended upon to cancel. This cancellation generally occurs in inverter circuits which synthesizes a multi-stepped waveform from the addition of several square waves. Some cancellation will also occur in those inverters which vary the phase shift between two sets of output voltage to obtain voltage regulation.

Consider the simple transformer for phase shift regulation shown in Figure 4-50. The total volume occupied by the core of this transformer is $x(4x)(3x)+2(x^2)(8x) = 12x^3+16x^3 = 28x^3$.

If this transformer is utilized in an inverter circuit where, for example, the input square wave to each outside winding varies between 25 and 31 volts, then, if the phase difference between the two input square waves is always adjusted to provide the same average value in the output (center leg) then the center leg does not have to be any wider than $25/31\ (2x)=1.6x$. If the phase shift between the two input square waves, when the input voltage is 25 volts, is still greater than zero, the center leg may be reduced still further. This is due to the fact that in a quasi-square wave (which is the output voltage of the center leg) the ratio of the rms value of the fundamental component of the wave to its half-cycle average increases with increasing dwell angle as shown in the graph of Figure 4-52. Even assuming that the largest center leg (1.6x) will be required, the amount of core material saved by this reduction is $(0.4x)(x)(5x)=2x^3$ which is 7% of the original weight of $28x^3$.

This weight reduction was obtained by utilizing the known flux cancellation between the two phase shifted square waves. It is also possible to utilize the flux cancellation between the several square waves which go into making the multi-stepped output from each inverter set. For example, in the three-phase transformer shown in Figure 4-53, the fact that the instantaneous sum of the voltages applied to the three windings is always zero means that $\phi_1+\phi_2+\phi_3=0$ and hence there is no need for a separate magnetic return path. However, as mentioned before, the requirement that $\phi_1+\phi_2+\phi_3=0$ precludes the use of three square waves as the input to this device. Since square waves are the most naturally obtained output of switching type inverters, this presents a difficult application problem. A similar problem exists with the improved three-phase transformer as shown in Figure 4-54.

A combination transformer which simultaneously allows the addition of the outputs from two separate inverter groups and also provides for flux cancellation between inverters of the same three-phase set is shown in Figure 4-55. It should be noted that this transformer will perform the same function as three of the flux adding transformers of Figure 4-50. However, three of these transformers have a core volume of $3(28x^3)=84x^3$. Even if the center leg is reduced to 1.6x, their total volume is still $3(28x^3-2x^3)=78x^3$. On the other hand, the core volume of the transformer of Figure 4-55 is less than this by the amount saved by joining the interior flux paths and

allowing for flux cancellation. This savings is $2(I\,2/3x^2)(7.6x)=25.3x^3$. Thus, a core weight savings of 32.5% over the best design of a single phase flux-adding transformer is possible. This savings in core weight is accompanied by a corresponding decrease in core losses over the single phase transformer approach.

A transformer suitable for use with the six square wave approximation to a sine wave is shown in Figure 4-56. As in the case of the transformer of Figure 4-55, the window length and depth (3x and 2x respectively) have not been optimized but were chosen only to keep the individual sections of the transformer on an equal basis with a single phase transformer as shown in Figure 4-51. Since the transformer of Figure 4-56 replaces six of the single phase transformers of Figure 4-51 (which have a core volume of $6(26x^3)=156x^3$,) and allows a savings in core volume of $5(15/6x^2)(7.6x)=69.7x^3$, its core weight (and losses) will thus be over 45% smaller than those of the equivalent single-phase transformers. Thus, this represents a considerable savings over conventional techniques. In addition, the magnetic paths in these two transformers (Figures 4-55 and 4-56) do not require any special instantaneous voltage conditions to be met as do the conventional three-phase transformers.

Clearly, the concepts embodied in the transformer designs of Figures 4-55 and 4-56 may be extended to handle any number of input square waves.

However, all the transformers discussed so far have been extensions of the conventional design in only two dimensions. Accordingly, investigations were started to determine if any significant advantages could be had by using core configurations that were basically three dimensional. Although most of these would be impractical to construct out of conventional laminated core materials, the use of ferrites, powdered iron, or similar materials capable of being moulded could render such designs feasible.

Two configurations which were investigated and found to possess no apparent advantages over more conventional designs are shown in Figures 4-57 and 4-58. A configuration for the three dimensional replacement for Figure 4-56 is shown in Figure 4-59. This configuration is obtained by bending the two ends of Figure 4-56 around until they meet. Savings are obtained by this maneuver because the path formed from the two ends can be made smaller than the algebraic sum of their cross-sections because of the flux cancellation that will occur. The amount saved in this configuration over the flat one of Figure 4-56 is

$$7.6x\left[5\left(\frac{x^2}{6}\right)+2x^2-6\left(\frac{x^2}{6}\right)\right]=7.6x\left(\frac{5x^2}{6}\right)=6.34x^3$$ which

is 8.35% of the weight of the equivalent single-phase transformer system. However, not only the constructional difficulties but

also the heat transfer and mechanical stability problems encountered with this type of construction are considerably increased. Thus, based on the relatively small improvement obtained by using this system over the "two-dimensional" transformer of Figure 4-56, this technique does not appear practically useful.

A comparison between this technique and the use of two "hexadic" transformers, as described by Westinghouse,[2] will now be attempted. The total core volume of the core of Figure 4-56 amounts to $86.3x^3$.

If a "hexadic" transformer core is designed so that it provides the same core cross-sectional area and window area/winding as the six phase-flux adding unit of Figure 4-56, it will have a core as shown in Figure 4-60 and a total core volume of $42\ 1/9x^3$. Since two of these are required to provide the same output as a single unit of the type of Figure 4-56, their total core weight will be $84\ 2/9x^3$, still less than the six-phase flux adding technique. However, when the winding weights are factored in, the total weight of the two "hexadic" transformers becomes $4267x^3$, whereas the total weight of the six-phase flux adding transformer is only $2635x^3$, making the six-phase flux adding transformer more desirable from the standpoint of reduced weight and less copper loss. Both of these designs yield a transformer with much more weight in copper than iron; an improvement in both could be expected with a detailed design effort, but it is expected that the flux adding transformer would still come out ahead, basically because its design permits splitting up the secondary from the primary, yielding more but smaller coils having a lower mean length per turn for the same volt-ampere capability. Hence, the flux-adding construction depicted in Figure 4-56 has been chosen as the type of output transformer that will be used.

b) Core Material Considerations

Besides the core configuration used, other very important parameters are the core material to be used and the flux density at which it will be operated. In general, those types of core

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materials having low losses (Molybdenum Permalloy) also have low saturation flux densities, and materials having high saturation flux densities (Supermendur) also have high losses. The 50% nickel-iron alloys (such as 48 alloy) have saturation flux densities and core losses which are between the two extremes mentioned. Which one will make the best transformer core depends on what is an acceptable weight-loss distribution. (This, of course, will vary from system to system and hence no one answer will be satisfactory for all cases.)

As an aid in visualizing the trade-offs involved, a sample transformer was designed and (theoretically) operated at various frequencies and power levels. This was done for three different types of core material: Square Permalloy 80 (which is representative of the low-loss, low saturation flux density materials); Supermendur (which represents the high loss, high saturation flux density materials); and Orthonol (which is representative of the medium loss, medium saturation flux density materials). The transformers were all simple two-winding toroidal units with equal copper and core weights (1 lb. core and 1 lb. copper, for a 2 lb. total weight), and the excitation was varied in such a way that the core loss and copper loss were always maintained equal (unless it was impossible to obtain the desired core loss because of core saturation). In this case (core saturation), the applied voltage and hence, core loss was limited to a maximum value as determined by the saturation flux level and further increase in output power was obtained by increasing the output current only, holding the input voltage (and hence flux level) constant. The results of this investigation are shown in Table 4-5 which shows the core flux density, core loss, output voltage, current and power and total loss for the three different core materials operated at five selected frequencies and many different power levels. The indicated frequencies were chosen because manufacturers' data on core losses were available at these frequencies. The power levels at which each transformer was operated at any given frequency were selected to give the desired values of copper loss (between 0.3 and 50 watts) and to result in equal core and copper losses whenever possible (i.e., core loss not limited by saturation). The results shown in Table 4-5 are also plotted on the graphs of Figures 4-61, 4-62 and 4-63. The points at which the core losses can no longer be increased to keep up with the copper loss (because of core saturation) are indicated on these graphs by a circle (O).

For example, these graphs indicate that at 400 cycles for this particular transformer weight (two pounds), if only low power is required ($<$ 82 watts) then the core material which will yield the lowest loss is the square Permalloy 80. In the medium power range (82 to 480 watts), Orthonol is best, while for high powers (480 to 1100 watts) at this weight level, Supermendur is best.

As a specific example, at the 300 watt level, a two pound transformer of this design would have a loss of 8.5 watts with an Orthonol core, 28 watts with a square Peramlloy 80 core, and 13.5 watts with a Supermendur core. Thus, at this power and weight level (and at 400 cycles), the Orthonol design would be best. However, if any of the three parameters (frequency, weight, power level) changes, the optimum core material might also change. As the last example shows, the curves in Figures 4-61, 4-62 and 4-63 can be readily used directly to determine the optimum core material for a two pound transformer (of the specific toroidal design arbitrarily assumed for purposes of this example) at any of the five selected frequencies.

To obtain the optimum designs at other weights, the graphs of Figures 4-61 through 4-63 can still be used, but appropriate modifications must be made according to the scaling equations developed in a previous section. (See Section III-B - Scaling Of Transformers). As an example of the application of these equations, consider the problem of making an optimum choice for the core material of a 300 watt transformer weighing 10 lbs. (again operating at 400 cycles). By Equation 4-23 of this report, this is equivalent in core flux density and winding current density to a $300(\frac{2}{10})^{4/3}$ = 35.1 VA transformer that weighs two pounds. Checking the 400 cycle curves for the lowest loss 35.1 VA transformer, the square Permalloy 80 design is superior, with a total loss of 0.7 watts. Since the loss is directly proportional to the weight, the losses in the 10 lb. 300 VA transformer are $(\frac{10}{2})(0.7)$ = total 3.5 watts. Thus, it can be seen that the proper (lowest loss) choice of transformer core material depends on the weight and power rating of the transformer in question; the 2 lb. 300-watt transformer used Orthonol core material, while the 10 lb. 300-watt transformer used square Permalloy 80 core material and had 5 watts less loss than the 2 lb. Orthonol design.

By repeating this scaling process as described above for several different weights at constant power, a curve of minimum loss versus weight can be obtained. Such a curve is shown in Figure 4-64 for 2800 VA at 3000 cycles and shows that the lighter the transformer, the greater the change in losses for a given change in weight.

On this curve, the point at which the optimum core material changes turns out to be at 28.8 pounds, and is so indicated on Figure 4-64. Which of the designs represented by this curve should be selected will depend on the weight penalties, additional losses placed on the DC power supply, and heat sink assembly.

c) Use of Shunts for Current Limit

A very simple technique for providing current limiting is the incorporation of magnetic shunts between the input and output windings of the output power transformer. These are merely pieces of iron of the same laminated material as the core and located so that the flux setup in the core by the primary winding may pass through the shunt without linking the secondary.

An example of this is shown in Figure 4-65. In order to avoid having all the flux pass through the shunt, thus preventing any power from being delivered to the secondary, an air gap is inserted in the shunt path. This air gap determines the way the flux divides between the shunt and the secondary winding under any given loading condition. A detailed analysis of the operation of the magnetic shunt (given in Quarterly Report No. 3 - Appendix 3-II of the "Optimization Study Of High Power Static Inverters and Converters" - NASA - CR-54122), indicates that as long as the shunt (or rest of the transformer core) does not saturate, the transformer with an internal magnetic shunt can be represented by an equivalent circuit consisting of an ordinary transformer with a linear inductor in series with its secondary. This is indicated in Figure 4-66. If the magnetic shunt of Figure 4-65 is selected so that under short circuit conditions, the transformer output current is 200% of the rated (full load) load impedance, then the value of the series inductor in Figure 4-66 will be one-half of the rated load impedance. If the magnitude and phase of the load voltage provided by this transformer are plotted as a function of the (resistive) load, the results are as shown in Figure 4-67. As can be seen from this graph, when the load is up to full rated, the output is about 10% lower than it

would be without the shunt, and the phase shift is 26.6°. Thus, for three-phase applications with unbalanced loads, the use of magnetic shunts for current limiting introduces serious voltage regulation and phase shift problems. However, since by specification the battery supply usually varies over a 30% range, in a single phase system where the phase shift would not be important, the additional 10% change in output voltage over the load range could be compensated for by operating the voltage regulating system over a slightly larger range. Detailed design procedures for current limiting transformers may be found in the literature.[13]

d) Use of Holes in the Iron Core for Current Balancing

Although it is not expected to be needed in this inverter because of the input voltage decided upon (56 volts) and the increasing availability of silicon power transistors with very high current ratings, a technique for incorporating the balancing reactors into the output transformer core, as suggested by the NASA technical manager, was investigated and will be described below.

Figure 4-68 indicates the configuration that was investigated - a section of the transformer core in which three (assuming three transistors are to be paralleled) holes are placed. The common current Bus A is split into three Wires B, C, and D each of which is passed through one of the holes in the core. A second Wire E is looped through all three holes in such a way that as one travels along this wire, the core material is always traversed in the same direction. Currents flowing in Wires B, C and D set up magnetic fields as indicated in the core; these link with the loops of Wire E causing a current to flow in it. This current is in a direction opposite to the current in Wires B, C and D, tending to cancel the magnetic fields that the currents in those wires originally set up. Since the same current must flow in all parts of the Wire E, only if the three currents in Wires B, C and D are equal will all the magnetic fields be cancelled. Otherwise, they will not, and the uncancelled fields will cause voltages to be induced between the common and

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13 "Design Procedures For Special Type High Temperature Transformers - II". Irving Remis, Electrical Manufacturing, August, 1957, pp. 119ff.

separate ends of Wires B, C and D, in such a polarity as to tend to equalize the currents in the three wires. Thus, this system acts in the same fashion as the closed chain balancing reactor scheme discussed in "Paralleling Techniques and Problems" - Section IV- B-b of this report. (In order to avoid interactions between the flux setup by this balancing scheme and that produced by the main power windings on the transformers, these holes should be located out of the main flux path, possibly in little nibs incorporated in the transformer lamination punching. For those materials having a high retentivity (Orthonol and Supermendur), it may also be necessary to introduce an air gap into the magnetic circuit by slitting the core from an edge to each hole.)

IV. PARALLELING TECHNIQUES AND PROBLEMS

Regardless of the exact nature of the inverter transformers, the switching elements can be considered as an entity.

When the output required of any power switching stage is greater than can be handled with one switching device on each side, the power handling capability of the switch must be increased by paralleling. The simplest method of paralleling is to connect additional power switching elements in parallel with the original one. Although simple, this method suffers from the drawback that, because of the unavoidable differences in internal impedance of the switching elements, the load current will not be shared equally. Two non-dissipative paralleling techniques, the split transformer technique and the balancing reactor technique, can be used to force current sharing between the parallel power switching elements. These will now be analyzed in turn to determine their relative merit.

A. The Split Transformer Technique

The essentials of the split transformer technique are shown in Figure 4-69. Here, the original (unparalleled) circuit requires a power switching device with a capability of VI watts. The lower circuit indicates the technique used to split the load up into N equal parts, with each power switching stage being required to handle only VI/N watts. Because all the transformer secondaries are connected in series, the same current flows in each, and thus, through transformer action, the primary currents are forced to be identical. This method achieves exact load sharing at the expense of splitting up one large transformer into N smaller ones. The weight and loss penalties that this entails are obtained from the following analysis.

It will be assumed that all of the smaller transformers are identical to one another and similar (in the geometrical sense) to the single large transformer; that is, with all dimensions scaled in the same ratio, the smaller transformers can be made congruent with the large one. The smaller transformers will also be operated at the same core flux density and winding current density as the larger ones. The analysis proceeds as follows:

Let the large transformer have a power rating of P_I. Then each of the smaller transformers has a rating of P_I/N. If the weight of the large transformer is W_I, then, by Equation 4-20, W_N, the weight of each of the smaller ones can be obtained as follows:

$$W_I = k\, P_I^{3/4} \qquad W_N = k\left(\frac{P_I}{N}\right)^{3/4} = \frac{W_I}{N^{3/4}} \tag{4-22}$$

Thus, the weight of N of the smaller transformers will be

$$N\left(\frac{W_I}{N^{3/4}}\right) = W_I N^{1/4} \tag{4-23}$$

which is $N^{1/4}$ times as much as the weight of the single large transformer. Since, under the operating conditions assumed above, the losses are directly proportional to the weight, the losses in the N smaller transformers will be $N^{1/4}$ times the losses in the larger transformer.

B. Balancing Reactor Techniques

The weight (and loss) penalties incurred in using the split transformer paralleling technique have already been analyzed (Equation 4-23). Those due to another current balancing scheme, the use of balancing reactors, will now be investigated.

A comparison of using a balancing reactor to equalize the currents in two switching units versus the use of a split output transformer to achieve balance will be examined first. The two methods are shown schematically in Figures 4-70 and 4-71. The balancing reactor technique operates on the principle that, unless the currents in the two halves of the reactor are equal, a voltage is developed across the inductor in such a direction as to increase the current in that switch tending to carry the least current. Because the same switch will always tend to slack, the balancing reactor must always provide the same polarity voltage when load currents are flowing in it. Thus, an air gap is required in the core to allow the flux to return to zero during the non-conducting halves of each cycle when no current flows and

the core must reset itself for the following half-cycle. This air gap, coupled with the relatively few turns required to support the small unbalance voltage results in the balancing reactor having a fairly high magnetizing current. (This could be reduced by over-design of the voltage capability of the unit). The magnetizing current flows through the switch which normally tends to carry more than its share of the load. Therefore, unlike the case of the split transformer technique, in the balancing reactor technique the currents in the switching elements are never perfectly balanced, the unbalance being due to the magnetizing current of the balancing reactor.

In the simple scheme shown in Figure 4-70, the output transformer is rated at $2\ I_o\ V$ volt-amperes (where V is the supply voltage and $2\ I_o$ is the DC current taken by the switching stage), and the balancing reactor is used at $I_o\ \frac{v_o}{2}$ volt amperes, where v_o is the maximum voltage difference required across the switching elements to obtain the desired current balance. However, because of the unidirectional nature of the reactor current, only one-half of the B-H loop of the core of the balancing reactor can be utilized; thus, since only one-half of the voltage capability of the reactor can be utilized, its size and weight will be comparable to one of twice its normal VA rating. Therefore, for purposes of weight and loss estimates, the VA rating of the balancing reactor will be taken as $2\ (I_o\ \frac{v_o}{2}) = I_o v_o$. From Equation 4-20, the weight of the single output transformer plus two balancing reactors for the balancing reactor technique will be

$$W_1 = k\left[2\ (I_o v_o)^{3/4} + (2\ I_o V)^{3/4}\right] \qquad (4\text{-}24)$$

Similarly, the weight of the two split transformers will be

$$W_2 = 2\ k\ (I_o V)^{3/4} \qquad (4\text{-}25)$$

The ratio of these weights is:

$$\frac{W_1}{W_2} = \frac{k\left[2(I_o v_o)^{3/4} + (2 I_o V)^{3/4}\right]}{2k\ \ (I_o V)^{3/4}} = \frac{1}{4\sqrt{2}} + \left(\frac{V_o}{V}\right)^{3/4} \qquad (4\text{-}26)$$

This ratio is plotted in Figure 4-73 for different values of $\frac{V_o}{V}$, and will be less than I (i.e., the balancing reactor technique will be lighter) for

$$\left(\frac{V_o}{V}\right)^{3/4} < 1 - \frac{1}{4\sqrt{2}} \quad \text{or} \quad V > \frac{v_o}{\left[1 - 4\sqrt{2}\right]}^{4/3} \qquad (4\text{-}27)$$

For a typical V_o of 1.5 volts for a silicon transistor, the cross-over supply voltage for the two techniques (from Equation 4-27 or Figure 4-73) is 18 volts. Above this value, the balancing reactor circuit of Figure 4-70 is lighter (and has smaller losses); below it the split output transformer technique is best.

For balancing more than two switching elements at a time, there are several methods that may be used. The split transformer technique as shown in Figure 4-69 may be used. Balancing reactors of the type shown in Figure 4-70 may be connected in cascade; an example of this for the case of balancing four units is shown in Figure 4-72.

Although this technique (Figure 4-72) requires a minimum number of reactors for the number of transistors to be paralleled, it has the disadvantage that if any one of the paralleled elements develops a fault and is cleared from the circuit, the current in the remaining elements is no longer balanced, accelerating failure in the remaining switches.

a) Reference Balancing Technique

One method of avoiding this problem is shown in Figure 4-74. Here the balancing reactors serve to maintain a constant ratio between the current in the reference switch and the current in each of the paralleled power switches. Should one of the power switches be cleared from the circuit, all the switches, including the reference, will pick up proportional shares of the load. (If the reference switch fails, the balancing scheme becomes inoperative; for this reason, the reference switch is generally operated at a reduced power level to enhance its reliability.) As an example of this operation, consider the circuit of Figure 4-74 and assume

1) All the switches are operating

2) The total load current is I

3) The turns ratio of the comparison reactor is 5:1 so that the reference switch current is 1/5 of the power switch current.

Let the power switch current be x. Then, the total current is

$$5(x) + x/5 = I \qquad (4\text{-}28)$$

which has the solution $x = .192I$. Thus, each power switch carries .192I amps and the reference switch carries .0385 I. If one of the power switches opens, the equation for current division becomes

$$4(x_1) + \frac{x_1}{5} = I \qquad (4\text{-}29)$$

This has the solution $x_1 = .238\ I$; each power switch now carries .238 I amperes and the reference switch carries .0476 I. The currents are still balanced, although they are, of course, higher than when all switches were operating. As in the case of the simple circuit using only one balancing reactor, the actual switch currents will deviate from the ideal due to the magnetizing currents of the balancing reactors.

An analytical investigation of the weight penalties inherent in the reference balancing technique will now be undertaken. If there are n power switches and the current through the reference element can be neglected, the current in each reactor will be I/n, where I is the total current carried by the parallel switch bank. Since two switching banks are used for each inverter stage, the total number of reactors needed is 2n. Each reactor must be able to support v_o volts (where v_o, as before, is the maximum unbalance voltage between switch units when all are carrying equal current). Thus, the rating of each reactor (again inserting a factor of two to account for the reduced use of the core capability brought about by the unidirectional current), will be $2\ v_o I/n$ amperes. The ratio of the weight of this system to one consisting of n split transformers if then

$$\frac{\text{wt. of reference balancing technique}}{\text{wt. of split transformer technique}} = \frac{(VI)^{3/4} + 2n\left(2v_o\frac{I}{n}\right)^{3/4}}{n\left(\frac{VI}{n}\right)^{3/4}}$$

$$= n^{-1/4} + 2\left(\frac{2v_o}{V}\right)^{3/4} \qquad (4\text{-}30)$$

where Equation 4-20 was used to evaluate the relative weights. Thus, it can be seen that the weight (and loss) advantages of this system increase as the number of elements to be paralleled increases and as the supply voltage increases.

As a specific example, with $v_o = 1.5$, $V = 28$ and $n = 6$, using Equation 4-30 yields a ratio of

$$\frac{\text{wt. of reference balancing technique}}{\text{wt. of split transformer technique}} = 6^{-1/4} + 2\left(\frac{3}{28}\right)^{3/4}$$

$$= 1.013 \qquad (4\text{-}31)$$

Thus, under these conditions the split transformer technique is only marginally better than the reference balancing reactor technique and other considerations would probably be the deciding factors.

b) Closed Chain Balancing Reactors

Still another technique using balancing reactors is shown in Figure 4-75. Here, each switch has its current balanced with the two elements on each side of it (and the outside ends are compared with each other, to form a closed chain). With the loop closed, the balancing obtained by this technique is very good; when one of the switches is opened, the loop is opened and the unbalance increases, although the circuit still operates to maintain the balance. If the current carried by the reference transistor in the previous method is neglected, this shceme has the same weight as the reference balancing scheme. It does have the advantage that all of the switches are treated equally; anyone can fail and the circuit will still operate somewhat. (In the case of the reference balancing scheme (Figure 4-74) failure of the reference switch means complete loss of balance, although balance will be maintained even though one or more of the power switches fail).

As the example worked out in Equation 4-31 shows, neither technique (split transformer or balancing reactor) offers any great weight advantage over the other in the power level and voltage range under consideration. However, weight (and losses) are not the only items of significance. But when multi-aperature transformers are used, splitting them is better than using balancing reactors.

In conclusion then, the selection of a certain balancing reactor technique versus the split output transformer technique in regard to weight savings can be found for any given switching element voltage unbalance v_o by using the cross-over graph of Figure 4-73.

V. GENERAL DESCRIPTION OF PROPOSED 3200 CPS - 10KW INVERTER DESIGN

The overall block diagram of the complete inverter is shown in Figure 4-76. The master crystal oscillator-pulse shaper provides a series of output pulses at 12 times the inverter output frequency. These are fed to two places: 1) a six-phase transistorized flip-flop reference ring counter which provides an output consisting of six squares waves, (at the inverter output frequency) each displaced from the next by 30°, and 2) a phase shifter, which is capable of delaying the pulses from the crystal oscillator by any amount from (approximately) 15° to 175° as measured at the fundamental frequency. The pulse output of the phase shifter pulse shaping network , which has the same appearance as the pulse output directly out of the master crystal oscillator-pulse shaper, is then fed to another six-phase transistorized flip-flop phase shifter ring counter identical to that mentioned above. Its output is another set of six square waves at the inverter fundamental output frequency with each displaced from the next by 30°, and the entire square-wave output set displaced from the corresponding ones provided by the reference ring counter by an amount depending on the delay provided in the phase shifter circuitry((15° - 175°). These outputs (six from each ring counter) are then amplified by their associated pre-drive buffer amplifiers and fed into the input of the square wave power switching stages where they are further amplified and transformed by various ratios on the output transformer to be added in series with one another to yield the composite output. With this technique, the output voltage shown in Figure 4-47 contains no harmonics lower than the 11th. This scheme of utilizing all six square wave output voltages to form part of each phase output voltage was chosen in preference to a similar scheme which generates a comparable waveform with the use of only five of the six available waveforms[11] because the method of using all six square wave voltages gave a more complete distribution of phase loads and allowed all twelve output transformers to be identical. The "hexadic" transformer described in the above-mentioned report could still be used in this scheme. Although the generation of an even more complex waveform than that provided by the six square wave approximation would permit a further decrease in filter size, this was not attempted because a more complex system than the six-step approach could not then be scaled down without becoming overly complex for its function at the lower power levels. (The next possible number of steps in a scheme of the type used here is nine, which would mean a 50% increase in the overall complexity.) It should also be mentioned that the filter in a static

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11 op. cit.

inverter performs two functions; it not only removes unwanted harmonics from the power stage output, but also acts as a buffer between the power switching stage and the load.

The delay of the phase shifter circuitry is controlled by the voltage feedback circuit to maintain the average of the phase voltage outputs at the desired value (or peak current in any or all phases below the 200% overload limit). The individual blocks are discussed in more detail in the following sections.

VI. POWER STAGE

A. Final Transformer Design

Using the information obtained in the Magnetic Component Studies (Section III) of this report, it is now possible to establish final transformer designs for the 10KW - 3200 CPS - Static Inverter. Since the lowest weight-loss products were obtained by operating the transformer core materials at as high induction level as practically possible, the output transformer was designed in this fashion. Three different core materials were used and for simplicity and ease of comparison, the core losses and winding losses were designed to be equal. Aluminum foil is used for the windings, both for weight savings and ease of fabrication, since at 3200 cycles, only a few turns of relatively large cross-section are needed.

The lamination design for use with a low-loss, low saturation flux density material such as square Permalloy 80 is shown in Figure 4-77. The center leg of this core is only 1.3 times the width of the outer legs because of the fact that the phase shift between the two input square waves will never be less than 22°. Thus, while each outer leg must support 61.6 volts of square wave, the inner section only has to have enough volt-second capability to support a quasi-square wave with 22° dwell angle and amplitude of (this is the worst condition) twice the minimum battery voltage (44.8 volts). This has a volt-second equivalent of a square wave of amplitude $2\,(44.8)\left(\frac{180-22}{180}\right) = 78.6$ volts which is only $= 1.28$ times that of the maximum 61.6 volt square wave which will appear across each primary winding when the battery voltage is at its maximum. Although of all rectangular shapes the square provides the least perimeter for a given area and hence is desirable as a core cross-section because it allows the least winding resistance for a given volt-second capability, it is obviously impossible to make both the inner and outer legs have a square cross-section since they are of different widths. As a compromise, the stack thickness was chosen to be the cube root of

the product of the two primary and one secondary widths or $3\sqrt{(1.0)(1.0)(1.3)} = 1.1$. The window length was arbitrarily chosen and the window width was calculated so as to give approximately equal weights of core and winding. The designs for the three different core materials are summarized in the table below.

TABLE 4-6

Designs	I	II	III
Core Material	Sq. Perm-80 (2 mil)	Orthonol (2 mil)	Supermendur (2 mil)
Core Size	As shown in Figure 4-77	As shown in Figure 4-77 X 0.69	As shown in Figure 4-77 X 0.48
Core Loss	42 watts	88 watts	191 watts
Primary Winding (Each of 12)	Wind two coils 16 turns each bifiliar. Aluminum foil cross-section .018" x 1.78"	Wind two coils 20 turns each bifiliar. Aluminum foil cross-section .010" x 1.23"	Wind two coils 25 turns each bifiliar. Aluminum foil cross-section .0057" x 0.85"
Secondary Windings	COIL 1 8 turns COIL 2 5 turns COIL 3 4 turns Aluminum foil cross-section .035"x1.78"	COIL 1 9 turns COIL 2 7 turns COIL 3 3 turns Aluminum foil cross-section 0.21"x1.23"	COIL 1 12 turns COIL 2 9 turns COIL 3 3 turns Aluminum foil cross-section .011"x0.85"
Maximum Operating Flux Density	7 KG	12KG	20KG
Coil Losses (Total)	42 watts	88 watts	191 watts
Core Weight	10.5 lbs.	3.5 lbs.	1.2 lbs.

TABLE 4-6 (continued)

Designs	I	II	III
Winding Weight	10.1 lbs.	3.4 lbs.	1.15 lbs.
Insulation	1.4 lbs.	0.5 lbs.	0.2 lbs.
TOTAL WEIGHT	22.0 lbs.	7.4 lbs.	2.55 lbs.
Total Losses	84 watts	176 watts	382 watts
Wt. - Loss Product	1860 lb-watts	1300 lb-watts	975 lb-watts
Efficiency (at 10 KW load)	99.16%	98.37%	96.32%

It can be observed that going from Design I to Design II allows a weight reduction of 14.6 pounds while increasing the losses only 92 watts, for a trade-off at 6.3 watts/lb. On the other hand, in going from Design II to III, 206 watts must be sacrificed for a reduction of 4.85 lbs., giving a trade-off ratio of 42.5 watts/lb. As indicated earlier, which design would be selected depends on the weight-loss characteristics of the rest of the power system. In order to arrive at a firm design and weight-loss figure, the transformer design using Orthonol (Design II of Table 4-6) will be selected. This represents a middle-of-the-road design, which does not lean too heavily toward either extreme of efficiency or minimum weight.

B. Transistor Configuration

A typical power output stage is represented in Figure 4-78. The power switch transistors are represented by Q9 and Q10 while transformer T1 is part of the power output transformer.

Calculations indicate that in the flux adding 12 step approximation, under the worst possible conditions, (200% load on all three phases and worst combination of load power factors), the peak current which will have to be carried by any one side of a power switching stage will not exceed 88 amps.

With bifiliar primary windings on the output transformer T1, the peak voltage appearing across any of the power switches should occur at turn-off and will be twice the supply voltage plus the di/dt voltage introduced by the delay core T4. The latter will depend on the saturated inductance of the delay core and is not expected to exceed 10 volts. The supply voltage does not exceed 61.6 volts (56 V + 10%) making a maximum switch voltage of 2(61.6) + 10 = 133 volts.

Both these voltage and current requirements can be met by a single transistor appearing recently on the market - the Silicon Transistor Corporation #STC-2501 which has ratings of 150 amps and 150 volts. Although the current rating provides plenty of margin, the voltage rating is rather close. It is expected, however, that it will not be long before the units can be made with voltage ratings to 200 volts, which would provide a considerable margin in the voltage also. Westinghouse can already make 30 ampere units with voltage ratings to 300 volts.

Should higher voltage units not be available and larger safety factors (or higher input voltages) be desired, there are two possible methods which may be used.

1) Several of the existing 30 amp high voltage (300 V) transistors may be paralleled in order to provide the required current carrying capability. At least 3 would be required to be paralleled to handle the 88 ampere peaks; this would require the use of split transformers or some type of balancing reactors thus introducing additional weight, loss and complexity. Provisions would also have to be made in the base drive circuitry to insure proper sharing of the drive power.

2) Two (or more) of the 150 V, 150 A transistors could be connected in series. This permits the high voltage to be divided between them. Since power switching transistors of this type generally fail in the shorted mode, should one fail (short) it would not have to be removed from the circuit.

However, the drive losses and forward losses in this circuit are twice those in the single transistor circuit. Furthermore, any network used to equalize the voltages across the two transistors cannot have very low impedance, because it should not cause a circuit malfunction when one of the transistors shorts and the entire voltage appears across the other one.

Because of the additional problems and losses that these multiple transistor techniques involve, it has been decided to use only one 150A, 150V transistor in each switch. The 150V collector to emitter voltage of this transistor is the largest voltage rating that can be obtained for this size transistor at the present time. Thus, the maximum voltage safety factor is only 10% which is well below the safety design margin of 100%. However, collector to emitter voltage ratings of 200V and higher are expected to be available in the near future therefore increasing this safety factor to 50% and higher. To protect the transistors from voltage spikes of any source, zener diodes are connected across them. The proposed power stage is shown in Figure 4-78.

The delay transformer T_4 serves the purpose of preventing the load current from flowing through the power switches (Q_9 or Q_{10}) until some 10 μ secs. after they have been turned on. This reduces the turn-on losses in the transistors to a negligible value.

This transformer will support 60 volts for 10 μ seconds. It weighs about .06 lbs. and at 100% load has copper losses of 2.4 watts and a core loss of 1.2 watts, for a total of 3.6 watts. This core saves the turn-on losses in Q_9 and Q_{10} which, at full load, are estimated to total 9.6 watts. Thus, the savings are six watts per output stage or 72 watts total for the inverter through the use of the delay cores. This is at the full load case; at lighter loads the savings will be less; at heavier loads, more. For example, at the 200% load point, the savings amounts to 100 watts.

Current feedback is used to provide the necessary base drive current for the power transistors Q_9 and Q_{10}. This type of base drive has the advantage over a more conventional voltage base drive scheme in that a considerable reduction of base drive losses can be obtained. This reduction is obtained for two reasons:

1) The amount of base current supplied is instantaneously and continuously adjusted so that only the required drive is provided; thus excess, unusable drive is avoided.

2) The feedback circuit makes the drive circuit appear as a current source (in the forward direction) to the input (base). Thus, power wasting base current limiting resistors necessary when driving the transistor from a voltage source, are not required.

At full load, the drive requirements for a single transistor is approximately 2.5 watts. (This is actual power delivered to the output transistor.) With a proportional drive, this is approximately the amount of power that the drive would supply. On the other hand, if the drive is furnished by a circuit that always supplies the maximum drive that the transistor would

ever require (whether it is needed or not) the power delivered to the transistor would be about 8 watts. In addition, the current limiting resistance required in order to avoid problems due to the change in input voltage of the output transistor with load and output current would dissipate another 8 watts. Thus, the proportional drive allows savings of about 27 watts/power stage $\tilde{=}$ 320 watts total. In addition, the drive used for this inverter also provides for the turning off of one side of the power stage before the other side is turned on, thus reducing the switching losses.

A base drive proportional to the collector current is obtained by adding to the base drive transformers (T_2, T_3), a winding through which the collector current passes. T_2 and T_3 then act like current transformers in which the primary winding is the collector feedback winding and the secondary (load) winding is the base drive winding. With the proper polarity and turns ratios on the two windings, the result is a large amount of positive feedback which results in the power transistors (Q_9 or Q_{10}) being turned completely on and the current being limited solely by the external load. When it is desired to turn off a transistor which is being held on with this feedback technique, it is necessary to provide enough turn-off current from the external driving source to completely cancel the positive drive signal provided by the collector feedback winding. This is provided by the drive circuitry discussed in the Logic section - Section VII - D of this report.

In order to avoid excessive reverse base voltages on transistors Q_9 and Q_{10}, two diodes are placed in each of these transistor base drive circuits in the reverse direction in order to limit the base to emitter reverse voltages of these transistors to -1.4 V DC maximum. This reverse voltage of -1.4V DC will insure that these transistors will remain cut off over the highest operating ambient temperatures. These diodes also provide an approximate voltage match with the base drive voltages (+1.4V DC) when the transistors Q_9 and Q_{10} are in their respective "on" states.

Short circuit protection for the output stage is described in the Logic Section - Section VII - E of this report.

It is generally desirable to provide additional windings for the reactive diodes on the output transformer primary (T1) as shown in Figure 4-78. If the tap voltage is properly chosen, this provides a slight forward bias on the reactive diodes when their associated power transistors are conducting. This bias, just under that required to cause significant conduction, allows that reactive diode to begin conducting without the output voltage of the stage having to change from the (E-forward switch drop) to

the (E + reactive diode drop) as must occur when the reactive diodes and power switches are connected to the same point. This reduction in output voltage shift with a primary current shift from the power switch (transistor) to the reactive diode results in a lower power stage internal impedance under reactive loading and thus reduces the effect of unbalanced loads on the voltage regulation and phase separation of a three-phase inverter which does not have individual phase voltage or angle regulation (as is the case with the present inverter).

However, because the amount of forward bias required for the reactive diodes is so slight, because of the high values of volts/turn obtained on the power transformers of high power inverters operating at higher frequencies, voltage increments of the size required ($\sim$ 0.5 volts) are too small to be obtained without the use of fractional turns on the output transformer. Although this is possible (by passing the last turn through a hole in the core, thus linking only a fraction of the core flux with that turn), it is not practical, and hence will not be used.

C. AC Filter

Because of the widely varying load impedance encountered, conventional filter design techniques are generally not applicable to the design of filters for use with static inverters. For some special cases where the load magnitude and impedance variations are restricted, special filters can be designed which compensate for the internal regulation of the inverter.[14] However, in the more common situation where the filter phase shift and voltage transfer ratio must be held nearly constant in spite of wide variations in load impedance and power factor, the filter configuration shown in Figure 4-79 is most applicable. Because the series section is tuned to resonance at the fundamental frequency, there is no attenuation or phase shift of the fundamental in passing through this filter. The amount of attenuation of any given harmonic is dependent on the relative impedance of the series and shunt sections at the frequency of the harmonic.

In general, it is desirable to have as small a filter as possible, both from the point of view of weight and efficiency and also transient load regulation.

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14 "OTT" Filter - Westinghouse Silicon Controlled Rectifier Designer's Handbook" - First Edition, 1963 pp. 7-18 to 7-22 and pp. 8-1 to 8-8.

For the twelve-step waveform which will be used in this inverter, the first harmonics present besides the fundamental will be the eleventh and the thirteenth. As the two twelve-step waveforms are varied in phase with respect to one another, the harmonic content of the sum will vary. Since the phase displacement will be varied by the voltage regulator in such a fashion as to maintain the fundamental component of the sum constant as the battery voltage is increased, the phase displacement will increase. The harmonics in each waveform will increase in proportion with the battery voltage. The harmonics in the output will vary in a more complex fashion because for certain phase displacements, some of the harmonics in the two waveforms will cancel one another. The percentage of total harmonic distortion and the percentages of the 11th and 13th harmonics in the sum of two twelve-step waveforms as a function of the phase displacement between the two waveforms is shown in Figure 4-80. Figure 4-81 shows the value of M required of the filter for the 11th and 13th harmonics as a function of the phase displacement between the two input waveforms. The value of M is defined as the ratio of the magnitude of the series reactance of the fundamental over the magnitude of load impedance at full load. These values for M were obtained from the consideration that no single harmonic in the output should have a value in excess of 2% of the fundamental. In the case of the 11th and 13th harmonics, it is this requirement, rather than the 5% maximum on total harmonic distortion which is the most stringent.

Because of the impossibility of obtaining the exact number of turns required on each winding for proper cancellation of the harmonics, there will be some harmonics in the output which would ordinarily be cancelled. However, the actual number of turns on each winding cannot differ from the correct value by more than 1/2 turn, or a total of 2 (1/2) turns out of a possible 19 on the three windings (for Design II in Table 4-6). This is for two of the windings being off by 1/2 turn; thus, the amount of harmonics re-introduced in this fashion should not exceed 1/19 or 5.25% of the value of that harmonic in a square wave. These amounts are shown below.

TABLE 4-7

Harmonic	Percent in Square Wave	Residue in Output
3rd	33%	1.75%
5th	20%	1.05%
7th	14%	0.75%
9th	11%	0.58%

If all three windings were off by 1/2 turn, the half-turn on one winding would cancel the effect of the half-turn on another winding, leaving a net error of only 1/2 turn.

Since none of the 11th and 13th harmonics are cancelled by the interconnections, having the turns ratios inexact neither increases or decreases the magnitude of these harmonics, which are limited by the filter to a maximum of 2% each.

The total harmonic distortion contributed by all the harmonics through the 14th is then given by

$$\text{THD}(\%) = \sqrt{(1.75)^2 + (1.05)^2 + (0.75)^2 + (0.58)^2 + 2^2 + 2^2} \simeq 3.6\%$$

This is considerably less than the 5% total prescribed by the specification, especially when one considers that at no time (except zero phase shift, which is not a region of normal operation) will all of the harmonics reach their maximum values simultaneously.

Since the load may vary in power factor from 1.0 to 0.7 lag, each phase (line-to-neutral) may draw as many as 3300 $\sin(\cos^{-1}0.7)$ = 2300 vars. Since the shunt capacitor of the filter draws only 830 vars, it is actually advantageous to eliminate the shunt inductance and use the load to provide the missing inductive vars for tuning.

In fashion, the full load power factor as seen by the inverter, ranges from .97 lead to .84 lag instead of the 1.0 to 0.7 lag of the load. Also, by using the load inductance as part of the filter, the weight and losses associated with the shunt inductance are completely eliminated.

Since the full load impedance is $R_L = \frac{E^2}{P} = \frac{(110)^2}{3.3\text{x}10^3} = 3.66\,\Omega$ and a value of M (from Figure 4-81) of 0.23 provides adequate attenuation, the required series inductance is $L = \frac{R_L(0.23)}{\omega} = \frac{(3.66)(0.23)}{(6.25)(3.2\text{x}10^3)} =$ $.0419 \times 10^{-3}$ hy = 41.9μhy. Part of this inductance is made up of transformer leakage inductance which is estimated to be approximately 28.2μhy. The maximum current this inductance will be required to carry occurs at the 200% load condition and is $I_{max} = \frac{(3300)\ (2)\ (\sqrt{2})}{110\quad .84}$ = 101 amps (peak). The design current will be 30A rms (100% load). The core design is shown in Figure 4-82.

The series capacitor required for tuning this choke is:

$$C = \frac{1}{\omega X_c} = \frac{1}{(3.66)(0.23)(6.28)(3.2\text{x}10^3)} = 59.2\,\mu\text{fd}$$

A 55μfd ±2% capacitor will be specified; the small additional capacity required to exactly tune the capacitor with the core will be added in parallel. The maximum rms voltage across the capacitor (under the 200% load condition) will not exceed 55 volts; at steady state conditions under 100% load the capacitor will be 27 volts. (rms). The shunt capacitor is related to the series capacitor by the Equation $C_P = M^2 C_S$ and thus has a value of $(59.2)(.23)^2 = 3.12\mu$fd. It is operated at 120 volts rms AC. (Under steady-state conditions, the voltage across the shunt capacitor is independent of the load.)

D. DC Filter

The DC input filter for the +56V supply will consist of a shunt capacitor whose value is tentatively set for 100μfd at 200WVDC. A small mica-capacitor with a rating of .01μfd at 500 WVDC may be placed around this large capacitor for high frequency noise suppression.

The input (DC) filter actually serves several functions:

It helps attenuate the effects on the supply line of the pulses of current drawn by the inverter. In so doing, it not only suppresses a considerable amount of radio frequency noise that would otherwise be imposed on the DC supply lines but also makes the supply appear "stiffer" to the inverter, thus avoiding wild and possibly damaging voltage fluctuations at the inverter input terminals.

It also is capable of suppressing any voltage pulses on the supply line which tend to affect the inverter. It thus decreases both the conducted radio frequency interference produced by the inverter and the inverter's susceptibility to conducted R. F. I. on the input lines.

Because of the relatively slow switching speeds (10μsec) of the large silicon power transistors used in this type of inverter, the amount of radio frequency interference generated above 200KC is expected to be quite small. Therefore, no difficulty is expected in meeting an R. F. I. specification such as MIL-I-26600 which requires suppression down only to 200KC. To suppress any voltage transients of this nature which may get through, as well as any generated internally in the inverter, zener diodes will be connected across all appropriate transistors.

E. Weights and Losses

One of the largest contributors to the total inverter weight is the output transformer. As indicated in a previous section, the output transformer design can be varied to exchange weight for losses; which design would be selected depends on overall system considerations such as the permissible weight, size and cooling capacity of the required heat sinks and the weight and capacity of the external power source which is unknown at this time. For this report the compromise design using Orthonol (Design II) was used.

The trade-offs in the design of the AC output filter inductors follow the same lines as those for the output transformer; variation in the core materials can provide different designs for different applications. Hence, only one AC filter choke will actually be designed; it is to be understood that extensions to other core materials would parallel the output transformer designs. The filter choke was designed to have an inductance of 13.7 microhenries, carry a current of 30A rms (corresponding to full (100)% load current) and to not saturate with peak coil currents as high as 101 amperes (which corresponds to the case of 200% load at .7 power factor).

Since the leakage reactance of the output transformer, calculated to be 28.2μhy (the total effective leakage reactance, referred to and summed up in the series connected secondary windings which make up each of the three phases), can be considered to be effectively in series with the output of the power output transformer (as is the series filter tuning reactor), the series filter reactor was reduced from 41.9μhy by the amount of the leakage reactance (28.2μhy) to only 13.7μhy. The core configuration is shown in Figure 4-82, and the other electrical and physical parameters of the choke are given below:

TABLE 4-8

Core:	2 mil Orthonol, as shown in Figure 4-82
Coil:	Aluminum foil; cross-section 0.025" x 0.900", 13 turns
Coil loss:	1.5 watts (full load, 0.92 P.F. load)
Core loss:	1.2 watts
Core Weight:	0.155 lbs.
Coil Weight:	0.075 lbs.
Total Weight:	0.250 lbs.
Total Loss:	2.7 watts

The remaining items in the power stage which dissipate appreciable power are the delay core, power switching transistors, reactive diodes, and base limiting diodes. Magnetic components such as the delay cores were not designed in detail hence, their weights and overall losses were only estimated. Their dissipation under full load conditions are shown below:

Power Transistors:

Forward current loss: $2(18.6)^2(0.01) = 7$ watts/pair
Turn-on-losses (none, because of delay core)
Turn-off-losses ($T_{fall} = 10\mu sec$) = 13.6 watts/pair
Off-losses = 6 watts/pair
Drive-losses (Proportional drive) = 2.5 watts/pair

Total output transistor loss = 30 watts/pair or 360 watts for the entire inverter.

The losses in the reactive diodes will depend on the battery input voltage as well as the load, because the phase shift between the two input square waves in each phase will be varied by the voltage regulator to compensate for input DC voltage changes. At the nominal input voltage (56 volts) the phase shift between corresponding square waves will be about 80°. Thus, the current in each phase will be out of phase with the voltage by 40°. Hence, the current rhough the reactive diodes will have an average value of 1.9 amperes each. With an average diode drop of 1.0 volt, the total loss in the reactive diodes in each stage will be 3.8 watts, or 46 watts for the entire inverter.

Total weights and losses for all the 3200 cps - 10KW power stages are estimated as:

TABLE 4-9

Delay Cores T_4	.2 lbs.	10.8 watts
Driver Transformers T_2 and T_3	1.5 lbs.	10 watts
Diodes D_{11} - D_{14}	0.4 lbs.	25 watts
Diodes D_{17} - D_{18}	1.0 lbs.	46 watts
Zener Diodes DZ_5 - DZ_6	1.0 lbs.	Neg.

TABLE 4-9 (continued)

Output Transistors Q_9 - Q_{10}	5.3 lbs.	360 watts
AC Filter Capacitors	9.0 lbs.	----------
DC Input Filter Capacitors	3.0 lbs.	----------
AC Filter Inductors	.75 lbs.	8.1 watts
Output Transformer - T_1	7.4 lbs.	176 watts
Total Weights and Losses	29.55 lbs.	635.9 watts

VII. LOGIC

A. Oscillator

The reference oscillator package unit (see Figure 4-83) will contain a crystal oscillator and a squaring circuit. The crystal oscillator will have an output frequency of 38.4 KC or 12 times the output frequency. The frequency accuracy will be maintained at ±.02% over a temperature range of -55°C to +85°C without an oven. This frequency stability of ±.02% is inherent in the quartz crystal design that is used for this crystal oscillator. The squaring circuit shapes the waveform of the crystal oscillator into a square wave whose output will be 5 volts peak into a 5K load. The rise time of this square wave will be no greater than 130 nanoseconds.

An external pulse shaping network (see Figure 4-83) is provided for this oscillator in order to supply the pulse energy necessary to step the reference ring counter and input flip-flop of the phase shifter. The oscillator output square wave is current amplified in the emitter follower circuit Q_3. The resultant square wave output of this emitter follower is differentiated by the network consisting of C_1 and R_3. The leading edge of this differentiated signal turns on the inverter Q_2 which places the base of the output emitter follower at ground momentarily. This allows a pulse current to flow from the flip-flop trigger circuitry to ground through resistor R_1 and logic diodes D_2 and D_3 causing a change of state in the reference ring counter and input flip-flop of the phase shifter. This sequence is repeated for each incoming square wave. The emitter follower Q_1 is required to supply the necessary ground path for the trigger circuits. The logic diodes D_2 and D_3 are used as an "or" circuit to isolate the input flip-flop trigger circuitry of the phase shifter from the trigger circuitry of the reference ring counter.

B. Ring Counter

Two ring counters are required for this inverter. One ring counter is used as a fixed reference to supply the necessary square waves to the reference driver stages. The second ring counter is used as part of the phase shifter circuit for output voltage regulation. Its square wave outputs are phase-shifted with respect to the reference ring counter by delaying its incoming steering pulses. Each ring counter consists of six flip-flops whose output steering resistors are connected such that each incoming pulse will cause the ring to advance one step. Figure 4-84 is a typical flip-flop circuit used in the ring counter. Terminals 13 and 14 and resistors R_9 and R_{10} are used to steer the next flip-flop in the ring. Similar input steering signals are supplied to this flip-flop from terminals 15 and 16. Figure 4-86 helps to illustrate these steering connections.

Because the flip-flop is a bistable device, emitters of transistors Q_1 and Q_2 are biased slightly above ground for the single ended supply. This will allow the bases of transistors Q_1 and Q_2 to be biased slightly negative with respect to their emitters to allow stability over a wide temperature range by minimizing the effects of the leakage current (I_{CO}).

A 3.9 V zener regulated supply consisting of R_{11} and DZ_1 is used for each ring counter to bias the emitters of the flip-flops.

A start preference circuit consisting of resistors R_1, R_2 and capacitor C_1 is used for each ring counter to set the "on" and "off" states of each flip-flop in the ring counter when the DC from the regulator supply is turned on. This insures that both ring counters are "set" with respect to each other so that proper tracking will take place when the pulses from the oscillator are introduced into their steering circuits.

The outputs (3) and (4) are taken from the collectors of transistors Q_1 and Q_2 of each flip-flop circuit. In order to minimize loading effects on the ring counter, their outputs are amplified by the Darlington circuits used in the pre-buffer stages.

C. Phase Shifter

In order to obtain phase control between the two ring counters for voltage regulation, a phase shifting circuit is required. There are a number of approaches that may be used to obtain this phase control; such as:

1) Phase shifting the output square waves of the phase shift ring counter with respect to the reference ring counter.

2) Phase shifting the incoming pulse train to the phase shift ring counter with the use of a voltage controlled-variable frequency oscillator.

3) Phase shifting the incoming pulse train to the phase shift ring counter with a cascaded phase shifting circuit.

The first approach requires the use of a phase shifting circuit such as a push-pull magamp connected to each set of output leads of the phase ring counter. A slave flip-flop will be required on the output of each push-pull magamp to provide square waves of the same frequency (3200 cps) as the ring counter. The square waves generated by the ring counter are delayed by the amount of control signal applied to the magamp control windings. This approach offers the advantage of low operating frequency (3200 cps).

However, it has a major disadvantage in that the gains of all the phase shifting circuits must be closely matched in order to prevent the output square waves from becoming shifted with respect to each other causing an increase in the harmonic distortion. The transient response time must also be very closely matched in order to provide uniform correction.

The second approach utilizes a voltage controlled variable frequency oscillator to produce the second pulse train. Voltage feedback is used to control the frequency of this oscillator and hence the phase relationship between the reference pulse train and the pulse train generated by the oscillator. When the feedback error is corrected, the voltage controlled oscillator is held in frequency synchronism with the master oscillator. This means of phase control has the disadvantages that the voltage controlled oscillator must have a minimum drift with temperature and must be insensitive to transient overshoots during error correction that will cause positive feedback by allowing the square wave of the phase shift ring counter to slip into the 180° to 360° region.

The third approach consists of six controllable delay circuits that are connected in cascade. This is necessary to produce the desired phase shift of up to 180° between the two ring counters at the fundamental frequency of 3200 cps because the reference pulse train must be delayed by six (6) times its period.

This circuit has the following advantages:

1) Response time can be made less than one period of the fundamental frequency.

2) A phase shift greater than 180° cannot be obtained thus preventing the phase shift ring counter from slipping into the 180° to 360° phase shift region.

3) A variance in phase shift in any of the individual cascade stages will accumulate as a resultant output phase shift error which will be corrected by the voltage feedback circuit.

This circuit has a disadvantage in that it must operate at a high frequency of 19.2 KC or six (6) times the fundamental frequency.

The third approach was decided upon as the means of obtaining the required phase shift control because of the advantages it offers over the other two approaches. Because of the high operating frequency (19.2 KC) involved, an all solid-state circuit was considered to have certain advantages over an equivalent magnetic circuit. At these high frequencies, the exciting current increases sharply for magamps, causing a reduction in gain and increasing its rise and fall time.

Figure 4-87 represents a typical stage used in this phase shifting scheme. This typical stage consists of an input flip-flop, two linear ramp generators, a Schmitt trigger, and an output flip-flop.

Linear voltage ramps with a 2.6 μs period are generated by the circuits that contain the PNP transistors Q_1 and Q_2. A constant charging current is established by the voltage regulator circuit consisting of DZ_1 and R_1 which places a fixed voltage of 5.6VDC across resistors R_2 and R_3 through the transistors Q_1 and Q_2 which are connected as emitter followers. This voltage regulator circuit supplies the rest of the ramp generators from Point 18. The constant current is used to charge up the timing capacitors C_1 and C_2, producing linear voltage ramps at their outputs.

These linear ramp generators are synchronized by the input flip-flop which alternately discharges the timing capacitors C_1 and C_2 through transistors Q_3 and Q_4 on each half cycle. Zener diodes DZ_2 and DZ_3 are used to remove the base drive to the clamping transistors on alternate half cycles since the output of the saturated side of the flip-flop is 3.9 volts above ground.

The two linear ramps are introduced into the base circuit of the Schmitt trigger through an "OR" circuit consisting of diodes D_1 and D_2. The input error signal from the differential amplifier is also introduced into this base circuit through resistor R_6 and Point (10). This input error signal current biases the linear ramps which in effect shifts them up or down with respect to the present trigger level of the Schmitt trigger. This causes the Schmitt trigger to fire at different points on the ramp as a function of the magnitude and polarity of the input error signal.

When the ramp voltage is below the trip voltage of the Schmitt trigger, transistor Q_6 is saturated and transistor Q_5 is off. When the ramp voltage exceeds the trip voltage, the Schmitt trigger changes state by regeneration through resistor R_{11}. Transistor Q_5 saturates turning off transistor Q_6. A positive voltage on the collector of Q_6 is placed at the inputs of two "AND" circuits composed of transistors Q_7 and Q_8.

Either transistor Q_7 or Q_8 will saturate when both signals on its input circuit are positive. If one of the signals is at ground, then the transistor will remain cut off. Thus, when the positive signal from the Schmitt trigger is combined with the positive synchronizing signal from the input flip-flop, the transistor in one of the "AND"circuits will saturate causing the output flip-flop to change states. The output flip-flop serves as the input flip-flop to the next stage and will steer the output flip-flop of that stage as it was steered in the previous stage. Since the error signal is applied equally to all the Schmitt triggers in this phase shifting scheme, an accumulative phase shift composed of the individual phase shifts will be obtained.

The output of the last flip-flop in this phase shifting scheme is differentiated into pulses which alternately saturate transistor Q_2 twice a cycle of 6F, (See Figure 4-89). Thus, a train of phase-shifted pulses are obtained at 12F or the same frequency as the input pulses to the phase shifter. These phase-shifted pulses are introduced into the steering circuits of the phase shift ring counter by the emitter follower circuit consisting of transistor Q_1.

Transistors and diodes with very short switching times were used throughout the phase shifting circuit. Metal film precision resistors with low temperature coefficients will be used in the ramp generator and Schmitt trigger circuits for accuracy. Silver mica-capacitors with at least 5% accuracy will be used in the ramp generators.

Additional trimming capacitors and resistors may be required in these ramp generators to obtain the same slope characteristics. The Schmitt triggers may also require a trimming potentiometer to set their threshold levels in order to minimize errors.

D. Driver

The basic driver and its pre-drive circuitry are shown in Figure 4-90.

The function of the power stage and its components are explained in the Power Stage - Section VI-B of this report. Examining this power stage reveals that it requires two basic modes of control.

1) Pulse drive to turn off the power transistor that is saturated.

2) Sustaining drive that is used to supply enough base drive to sustain the power transistor that is conducting and to back bias the power transistor that is off.

The above modes of control must be supplied from the outputs of the ring counters. There will be one Power Stage for each ring counter flip-flop output, thus requiring twelve (12) Power Stages.

In order to match the low level logic of the ring counters to these power stages, a pre-driver stage is required. A typical pre-driver stage is shown in Figure 4-90. The outputs of the ring counters are buffered by the Darlington circuits composed of transistors Q_1, Q_2, Q_3 and Q_4. This circuit is used to minimize loading of the ring counters. The output of transistors Q_3 and Q_4 are connected in a push-pull inverter configuration to output transformer T_7. The secondary of this output transformer is used to supply the two basic modes of control.

Examining the control circuitry for one side of the power stage, Figure 4-90 (Q_9 and T_2) note that the following events happen:

1) At the beginning of the positive half-cycle, transistor Q_9 is turned on (saturated) and transistor Q_{10} is turned off (unsaturated).

2) Transistor Q_5 is driven into saturation for a period of 10 μs by the timing core T_5 at the beginning of this positive half-cycle.

3) During this 10μs time interval a large current, limited by resistor R_{19} ($\sim$ 1.2 A min), passes through a secondary winding N_4 of transformer T_2.

4) The polarity of the current and the turns ratio are such as to set up a flux which will oppose the feedback current required to supply the base drive to power transistor Q_9.

5) Transistor Q_9 is turned off with the cancellation of its base drive.

6) The sustaining drive transistor Q_7 is held off during this time of 10μs since its base is placed at ground through transistor Q_5.

7) The timing core T_5 saturates after 10μs removing the base drive to the shorting transistor Q_5. Its current is limited by resistor R_9.

8) The sustaining drive transistor Q_7 saturates causing a current to flow in the secondary windings N_3 of T_2 and T_3.

9) The polarity of the current and the turns ratio are such as to back bias the base of the power transistor Q9 by $\sim$ -1.4V to insure that the leakage current will not forward bias the power transistor at the maximum operating ambient temperatures.

10) The sustaining drive forward biases the base of power transistor Q_{10} by approximately +1.4V, turning it on.

11) The power stage remains in this state until the beginning of the next half-cycle when steps 1 through 11 are repeated for the opposite side of the power stage (power transistor Q_{10}).

The timing cores T_5 and T_6 are reset on the negative half-cycle respectively. During the first 10μs of the reset half-cycle, a reverse voltage is developed across the base drive circuit of the shorting transistors Q_5 and Q_6. Diodes D_9 and D_{10} are used to insure that the emitter to base voltage limits are not exceeded during this reset interval.

Zener diodes DZ_3 and DZ_4 are used to suppress voltage transients that may exceed the collector to emitter voltage ratings of shorting transistors Q_5 and Q_6. Logic diodes D_5 through D_8 are used to isolate the two sustaining drive windings on transformers T_2 and T_3. The

current in the sustaining drive is limited by resistors R13 and R14 since the base drive of the power transistors Q9 and Q10 represents a non-linear load. Logic diodes D1 and D2 are required to keep the +56 V out of the base circuits for the sustaining drive transistors Q7 and Q8. The voltage drop caused by diodes D1 and D2 and the saturation voltages of Q5 and Q6 will not be enough to turn on these transistors.

E. Short Circuit Current Limiting

The short circuit current limiting feature is used to protect the inverter against overload currents exceeding 215%. This is accomplished by turning off the power stages for a finite time and then turning them back on. The cycling will continue as long as the short remains. This sustained cycling will not be detrimental to the 3200 cps Static Inverter because of its low duty cycle ($Du \sim 10^{-5}$). However, a time delay circuit could be added which would stop the cycling after a predetermined time if the short circuit persisted. A manual reset will be required on this time delay circuit to re-start the inverter. The current overload circuit is shown in Figure 4-92. When the voltage regulator is first turned on, B+ (1) is supplied to the oscillator, ring counters, phase shifting circuitry, and a time delay circuit. This allows enough time for the oscillator and ring counters to stabilize before B+ (2) is applied to the pre-driver stages.

The time delay circuit consists of timing elements R14 and C3 (see Figure 4-92). Capacitor C3 charges up to the threshold voltage of UJT-Q7 (16 V) in approximately two seconds. The UJT-Q7 fires causing transistor Q6 to saturate. The saturation of Q6 pulses transformer T9 whose secondary turns SCR1 (Gate turn-off type) on. The SCR1 switches on the controlled B+ (2) voltage which is used for startup of the pre-drive buffer stage and for current overload protection.

B+ (2) voltage is then applied to the pre-driver transformer T7 (see Figure 4-90). This initiates the drive necessary to turn on the power stages. This B+ (2) also energizes transistor Q8 which clamps the timing capacitor (C3) to ground thus de-energizing UJT-Q7 and transistor Q6. Pulse transformer T9 is current reset by resistor R18. Current transformers T1, T2 and T3 are used to sense the load current in each phase. The core material (HY MU-80) for these current transformers is operated at a very low flux density to prevent core saturation on current overload. Their secondaries are loaded by burden resistors R9, R10 and R11 to maintain the ampere turns relationship between their primary and secondary windings. The

three phase output voltage developed in the secondary windings of these current transformers is bridge-rectified and filtered by resistor R7 and capacitor C1 to 0.6% ripple.

Potentiometer R8 is used to adjust the output voltage by controlling the secondary load impedance of the current transformers. The filtered DC output is current-amplified by the emitter follower Q4. The threshold voltage is adjusted by potentiometer R8 to cause the Shockley diode to switch on at 215% overload. When the Shockley diode DA1 fires, a large positive voltage is introduced into the base circuits of transistors Q3 and Q5 causing them to saturate.

When transistor Q3 saturates, it causes transformer T7 to apply a pulse of 20μs to the base of the Darlington circuit composed of power transistors Q1 and Q2. The saturation of Q1 turns off all twelve power stages through the "OR" circuit composed of twenty-four diodes of which one power stage is represented in Figure 4-90 by diodes D19 and D20. This causes a large current to flow in the secondary windings of T2 and T3 which will oppose the feedback current in whichever side happens to be on thus removing the base drive to the power transistors Q9 and Q10.

At the same time the saturation of transistor Q5 pulses transformer T8 which in turn reverse-biases the gate of the SCR1 thus turning it off. This removes the B+ (2) to the pre-driver stages of Figure 4-90, deactivating the sustaining drive and pulse drive to all twelve power stages. The transistor clamp (Q8) on the timing capacitor C3 is also removed allowing the timing circuit to be initiated again.

As soon as the power stages are turned "off" the overload current drops to zero. This removes the voltage from the emitter follower circuit Q4 which in turn allows the Shockley diode DA1 to reset. Transistors Q3 and Q5 are turned off, removing the current from the pulse transformers T7 and T8. The pulse transformers are current reset through resistors R2 and R19.

After a two-second time delay, the SCR1 is pulsed on again. If the short circuit is still present, the overload cycle will be repeated until the short is removed.

The response time of this circuit should be 312 μs or less. The response time of the current transformers, R-C filter, and pulse transformers will be the major factors contributing to the overall response time of this overload circuit.

In this current overload scheme, the phase shift ring counter was not shifted back to 180°. However, the phase shifting circuitry in Figure 4-87 can be shifted back to 180° to allow for soft starting after an overload to allow for a gradual increase in the output voltage. This soft starting feature was not included in this design since the response of the overcurrent circuit and the time delay before turn-on will be more than adequate to protect the power stage circuitry.

F. Voltage Feedback

The line to neutral voltage of each phase is measured by the potential transformers (Figure 4-92) T4, T5, T6 whose core material (Orthonol) is operated at a sufficiently low flux density to prevent core saturation due to large voltage excursions. The secondaries of these potential transformers are connected in a push-pull rectifier configuration and their center taps connected together and grounded to form a return path. Thus, each diode (D8 - D13) will conduct 60° of its full cycle being biased off the rest of the time. This circuit is a slight departure from the straight three-phase bridge configuration which requires that the secondaries of these transformers be connected in either a Wye or Delta configuration. Each diode only carries one-half the current and offers less effect on the output voltage if it should fail open as compared with its three-phase bridge counterpart. An additional advantage is obtained with this circuit in that the diode voltage drop is less than half of that obtained for the bridge circuit. The output of the rectifier is filtered in the two stage filter composed of resistors R12, R24, and capacitors C2 and C4. The ripple should be attenuated to $\sim$.06% by this filter. Resistor R13 serves as a stabilizing resistor which determines the load current through the diodes and hence controls to some extent the diode drops. The output (9) of this filter is placed into one side of a differential amplifier which has a minimum input impedance of 20K, which is determined by the gain hFE of the transistors Q3 and Q4 and the collector and emitter resistors R1 through R4. (See Figure 4-94).

A compensated reference zener diode DZ1 is used on the base input of Q4 to establish a reference for comparison of the error signal. The gain of the differential amplifier is determined by the ratios of resistor R1 to R2 and resistor R3 to R4, and is tentatively set for 50. The output of the differential amplifier (10) is placed into the base circuits of the six Schmitt trigger circuits (Figure 4-87) in order to bias the linear ramps and obtain a resultant phase shift.

The differential amplifier is compensated for drift caused by variations in ambient temperature with the use of PNP transistors Q1 and Q2. The overall drift should be less than 12μV/°C. A further reduction in drift can be realized by matching the NPN transistors Q3 and Q4 for gain and base to emitter drops. Metal film resistors with low temperature coefficients and ±1% tolerance will be used in this amplifier circuitry. In addition, a separate regulated supply may be required to minimize the effects of B+ variation. An additional stage of filtering may be required on the output of the rectifiers to reduce the ripple by another order of magnitude in order to allow the gain of the differential amplifier to be increased. If higher gains are required to obtain closer tolerances on the output voltage regulation, a second differential amplifier may be used whose inputs are taken from the differential outputs of the first differential amplifier. The response time of the voltage feedback circuit will be determined by the complexity of the R-C filter network used, the potential transformers, the output power filter, and output power transformer.

G. 200 Watt Voltage Regulator

An input voltage regulator is required for the low level logic and pre-buffer drive circuitry specified in Sections A through F. The maximum load requirement for this logic circuitry is approximately 5.5 amps at an operating voltage of +25V ±1%. The unregulated input supply voltage can vary from +61.6V to +44.8V low with a nominal value of +56V. A conventional series or shunt regulator may be used. Because of the large load requirements ($\sim$137 watts) the losses incurred by these regulators become prohibitive. (The conventional series regulator will have a maximum dissipation of 200 watts.)

A switching type regulator was used to minimize these regulator losses. This regulator was designed for 200 watts capacity to provide a satisfactory margin of safety. The maximum projected power loss for this switching type regulator is approximately 20 watts which is a factor of ten (10) less than the conventional series regulator.

Figure 4-96 represents the basic voltage regulator circuitry. The voltage regulator circuitry is discussed in detail in Quarterly Report No. 3 - Page 132 to 137 of the "Optimization Study Of High Power Static Inverters and Converters" - NASA - CR-54122.

VIII. RELIABILITY STUDY AND SCALING FOR 3200 CPS (10KW) STATIC INVERTER

A. Results of Reliability Study

A reliability analysis was performed on the electrical circuitry and their electrical components for the proposed 3200 cps Static Inverter. Packaging techniques and electrical connections were not included in this reliability study. The results of the study can only be used as a design guide to point out the circuits and components that have marginal designs, since the electrical circuitry was created from a theoretical design with no actual stress measurements being taken on the circuit components.

The detailed reliability analysis is given in Appendix 4-II. The reliability block diagram that is used to represent the overall circuit configuration is given in Figure 4-II-1. Each block represents a major circuit while sub-blocks are used to designate the individual circuits or components that are required to create a major circuit. The generic failure rates, derating factors, and environmental operating modes are established for each electrical component along with its operating time. From this information the total failure rate λT is established for each block (see Figure 4-II-1) and its sub-blocks which may be used to determine which circuits need to be improved. The overall Reliability Figure of Merit R for the 3200 CPS - 10KW Static Inverter is then found from this information for each mission profile and is:

1) Twenty-minute missile launch and one month continuous operation as a satellite in an earth orbit.

   a) $\overline{\lambda}_i t_i = .037175$

   b) $R = .963506$

2) Twenty-minute missile launch and one year continuous operation as a satellite in an earth orbit.

   a) $\overline{\lambda}_i t_i = .329858$

   b) $R = .718930$

The overall Reliability Figures of Merit R ($R = .963506$ and $R = .718930$) are rather low and can be improved. Examining Figure 4-II-1 reveals that the power stages (Blocks I and J), the

pre-drive buffer stages (Blocks G and H), and the phase shifter circuitry (Block C) have the largest total failure rates (λT). These large failure rates were caused by the large number of circuit components required, their percent operating duty cycles, and the de-rating factors assigned to each circuit component. These failure rates can be reduced by selecting components with larger de-rating factors, a redesign of the circuitry to reduce its total number of components, or using redundant circuitry. Of these three approaches, the use of redundant circuitry on all circuits with large failure rates will greatly improve the overall Figure of Merit R for this inverter design.

B. Results of Class I Scaling

Class I scaling consists of determining the changes in weight, efficiency and reliability for the conceptual design of the 3200 cps - 10 KW Static Inverter when it is scaled with respect to reduced power level and to changes in the DC source voltage. The detailed analysis of this Class I scaling is given in Appendix 4-III.

A reduction in the power level requirements from 10KW to 2KW for this inverter reveals that many changes will take place in the inverter components. The proposed circuit configuration for the 10KW inverter will remain the same over this output range (10KW to 2KW) requiring no circuit redesign. As the power level is reduced from 10KW the efficiency, size and weight of some components will have a continuous change while certain other components will change in discrete steps. Therefore, those components that must be especially designed for a given inverter such as transformers and inductors will have a continuous change in their parameters while components such as transistors and diodes which are not made specifically for a given size inverter will have a step change in their parameters.

The weights and losses for the magnetic components in the power stages (output transformer, AC filter inductors, drive transformers, and delay cores), the semiconductors in the power stages (power transistors, zener diodes, reactive diodes), AC filter capacitors, and the components in the logic sections are obtained at the lower power levels. These results are plotted in Figures 4-III-1 through 4-III-5 for each group of components. The results of these curves in Figures 4-III-1 through 4-III-5 are added together at the various power levels to obtain the total weight and loss for the entire inverter as a function of the inverter rating. These results are shown in Figure 4-III-6. Examining the weight and loss curves of this graph (Figure 4-III-6) reveals that a reduction

in total loss of 3.88 to 1 (775 watts to 200 watts) and in total weight of 2.51 to 1 (41.5 pounds to 16.5 pounds) will be realized when the total inverter output capacity is reduced from 10KW to 2KW. The reliability of this 3200 cps inverter will remain essentially the same over this power range (10KW to 2KW) because its proposed circuit configuration did not change and the same stress levels, duty cycles and de-rating factors can be assigned to these scaled components.

The weights and losses for the magnetic components and semiconductors of the power stages and for the components in the logic sections were determined at the 10KW power level as the DC input voltage from the source was varied. The power stages were found to be most effected by this scaling of the DC input voltage.

When the nominal DC input voltage is lowered below 41 volts, the transistor collector currents become excessive for the 150 amp transistors (STC-2501) that were chosen for this inverter design. Since transistors with larger current capacities are not available at the present time, the 150 amp transistor must be paralleled to provide the necessary current capacity. The output transformer must be modified so that a split transformer technique can be used to balance the current through these paralleled transistors.

As the nominal DC input voltage is increased above 68 volts, the transistor collector to emitter voltages become excessive for the 150 amp - 150 V transistors (STC-2501) that were chosen for this inverter design. Assuming that these transistors will be available with 200 V collector to emitter voltages, the power stages must be changed to a bridge configuration in order to avoid excessive transistor voltages. The number of power transistors will have doubled while the output transformer size will be reduced. Smaller size power transistors with large collector to emitter voltage ratings (300 and higher) can be used when the nominal DC input voltage is increased above 90 V because the maximum collector current becomes less for this 10KW inverter rating.

The curves in Figures 4-III-7 through 4-III-11 illustrate the changes in the weights and losses for the magnetic components and semiconductors of the power stages and for the components in the logic sections as the DC input voltage is varied. The results of these curves in Figures 4-III-7 through 4-III-11 are added together to obtain the total weight and loss for the entire inverter at 10KW which is depicted in Figure 4-III-12. Examining the weight and loss curves of this graph (Figure 4-III-12) reveals that a reduction

in total loss of 1.85 to 1 (1460 watts to 790 watts) and in total weight of 1.38 to 1 (58 pounds to 42 pounds) will be realized when the DC input voltage from the source is increased from 20 volts DC to 100 volts DC. The inverter with the lowest weight (40.5 pounds) and the lowest loss (720 watts) is obtained when the nominal DC input voltage is 68 volts or just before the inverter power stages are changed to a bridge configuration.

C. Results of Class II Scaling

Class II scaling involves determining the changes in weight, efficiency, and reliability for the conceptual design of the 3200 cps - 10KW Static Inverter when it is scaled with respect to harmonic distortion, output phase separation, voltage regulation, and DC input variations. The detailed analysis of this Class II scaling is given in Appendix 4-V.

The effects of varying the harmonic distortion specification on the inverter components were investigated with the results that only the AC output filter components - weight, size and loss were effected. The present design specification for harmonic distortion allows for a maximum total harmonic distortion of 5% with each individual harmonic not to exceed 2%. The leakage reactance and winding resistance of the output transformer and the phase load impedance are reflected into the AC filters as part of their parameters. The eleventh harmonic which is the predominate harmonic that must be filtered is used to determine the filter component values required for various degrees of harmonic distortion. The harmonic distortion before filtering is found in terms of the relative phase shift angle Θ (see Figures 4-80 and 4-81) required to maintain the proper load output voltage. The eleventh harmonic has several maxima and minima over this relative phase shift region. The amplitudes and phase angles for the maxima are used to determine the values of the filter components necessary to provide a specified harmonic distortion after filtering. These values of filter components may be used to scale their weights, sizes and losses as a function of allowable harmonic distortion for the eleventh harmonic at phase shift angles Θ of 32.7°, 65.5°, 98.2°, 131° at which the maximum harmonic distortion occurs for this eleventh harmonic.

Closing up the tolerances on the total harmonic distortion specification causes the series filter inductance to increase therefore reducing the capacity of the series filter capacitor in order to maintain exact tuning at the fundamental frequency of 3200 cps. This will cause a decrease in the total AC filter weight and an increase in in its total losses as shown in Figures 4-V-6 and 4-V-7.

The following secondary effects will also occur:

a) A reduction in the voltage and current feedback sensing circuit filtering may be possible.

b) An increase in the AC output filter response time.

c) A tighter control on the proper secondary transformer turns ratio must be maintained to suppress the lower harmonics.

d) Improving the source and transformer regulation will reduce the size of the filter parameters required since a smaller relative phase shift angle Θ will be required with a subsequent reduction in the initial total harmonic distortion.

Opposite effects on items a, b, and c, can be realized by relaxing the tolerances on the total harmonic distortion specifications.

The amount of phase separation between the three AC output phases was investigated in order to determine its effects on the inverter components. The present maximum phase displacement tolerance is two degrees. De-tuning of the AC output filters, variations in the transistor saturation resistance, deviations in the output transformer leakage reactance and winding resistance, and unsymmetrical loading are the factors that effect the phase separation between the three AC output phases. De-tuning of the AC output filters with a full reactive load was found to have the most effect on this phase separation and therefore was investigated. The transistor saturation resistance, output transformer leakage reactance and winding resistance, and the phase load impedance are reflected into the AC filters as part of their parameters. Thus the input voltages to the three AC filters can be assumed to be exactly 120° out of phase. The output voltage phase shift on a per-phase basis is then determined with respect to the input voltage as the resultant AC filter resonance circuit is de-tuned at the fundamental frequency of 3200 cps. A representative range of nominal series filter inductors and capacitors at a maximum regulation phase shift angle of 131° were chosen from the Class II Scaling of harmonic distortion outlined in Appendix 4-V, Section A of this report. The initial phase shift angle $\angle\alpha_o$ and gain were calculated first with the AC filters perfectly tuned in order to establish a reference point. The reactive elements composing the series filter branch of one of the phases were then de-tuned to produce both positive and negative reactances whose magnitudes are determined by the percent of de-tuning desired. The AC filters in the other two phases were left

tuned at the fundamental frequency to establish a reference point. The amount of relative phase shift angle $\angle\alpha_R$ was determined by subtracting the phase shift angle $\angle\alpha$ obtained as a function of de-tuning from the reference phase shift angle $\angle\alpha_o$. The relative phase shift angle $\angle\alpha_R$ is then plotted as a function of the percent of filter de-tuning for four equivalent series filter component combinations as illustrated in Figures 4-V-8 and 4-V-9. The necessary trimming inductors and capacitors can now be found to re-tune this AC filter to the fundamental frequency (3200 cps.)

The weight and loss of these trimming components may then be found as a function of the amount of corrective re-tuning required with the help of the scaling techniques used in Appendix 4-V, Section A of this report. The weights and losses for these trimming components can be added to the weights and losses of the AC filter components to obtain a complete AC filter weight and loss for each phase. The total weights and losses for all three phase AC filters are plotted as a function of the percent output filter de-tuning as shown in Figures 4-V-10 through 4-V-13. The four curves in each of these figures represents the four combinations of series filter inductors and capacitors that were used. Examining the curves in these figures reveals that the greatest changes in weight and loss contributed by the trimming inductors for re-tuning occurs in curve 4 for an equivalent filter inductance of 321μH while curve 1 represents the largest change in weight contributed by the trimming capacitor for an equivalent filter capacitance of 88μfd. Since the losses in the filter capacitors were assumed to be negligible, the curves in Figure 4-V-13 willhave constant AC filter losses.

The following secondary effects will occur when the permissible relative phase shift tolerance on all three phases is reduced below the present angle of 2 degrees:

a) A tighter tolerance will be required for the series filter inductors and capacitors as well as the load shunt capacitor for each of the three phases for a prescribed harmonic distortion level.

b) A more exact tuning between the series filter components for each of the three phases will require some trimming components which will increase the weight and loss of the AC output filters.

c) The series filter components may have to be temperature compensated over the required operating temperature range to insure proper matching.

d) The output power transformer design will have to be given more careful consideration in order to minimize its leakage reactance and winding resistance and to provide a close balance between its three output phases.

e) The power transistors and reactive diodes should be matched for forward voltage drop and saturation resistance.

The tolerances requirements on items a through e can be relaxed with the relaxation of the permissible relative phase shift tolerance.

The effects of varying the voltage regulation tolerance on the inverter components can be directly related to the results obtained for the phase separation study in Appendix 4-V, Section B of this report. The present design specification for output voltage regulation allows for a ±2 percent tolerance for steady state load conditions with the source voltage held constant. Again, the transistor saturation resistance and transformer winding leakage reactance and resistance can be combined with the series elements of the AC filters. De-tuning of the AC filters with a full reactive load was found to be the major factor in contributing to the voltage regulation problem. The same range of AC filter components and load conditions that are used to specify the relative phase shift angle as a function of de-tuning in Appendix 4-V, Section B of this report are used again. The input voltage to the AC filters was assumed to be fixed. The magnitude of the voltage across the load can then be determined with respect to the input voltage as the resultant AC filter was de-tuned from the fundamental frequency of 3200 cps. For the unloaded conditions, the AC filter output voltage can be considered equal to its input voltage for a tuned filter. Therefore, the output regulation as a function of the percent de-tuning for positive and negative reactances can be found for the four representative AC filter component combinations as shown in Figures 4-V-14 and 4-V-15. The total 3Ø AC filter weight and loss including trimming inductors and capacitors required for retuning can be related to the permissible percent output voltage regulation by relating similar curves in Figures 4-V-10 through 4-V-13 with those in Figures 4-V-14 and 4-V-15. Therefore for a given curve in Figure 4-V-14 or 4-V-15 for positive or negative reactive filter detuning, the percent of output filter de-tuning can be found for a given voltage regulation tolerance. This percent of output filter de-tuning combined with the type of trimming component required (shunt capacitor or shunt inductor) can be used in Figures 4-V-10 through 4-V-13 to find the total AC filter weight and loss for all three phases.

The secondary effects (a) through (e) discussed for the effects on Phase Separation tolerance (Appendix 4-V, Section B) will apply for the effects of varying the voltage regulation tolerance on the inverter components. In addition, the following secondary effects will occur when the permissible voltage regulation tolerance is reduced below the present value of ±2 percent.

a) An increase in the voltage feedback gain will be required with a decrease in voltage regulation tolerance. This may require another differential amplifier stage which will require the following additional parts:

Part	Quantity
Transistors	4
Resistors	5

b) Unsymmetrical loading may place too large a requirement on the averaging type of voltage regulator that is presently proposed. This will require that each phase be independently voltage regulated. The resultant circuit changes for the same 10KW inverter are as follows:

1) Three separate power output flux-adding transformers will be required, one for each phase with an increase in weight of 2.32 pounds, and in total losses of 55.5 watts using the Orthonol transformer design as reference.

2) The pre-drive reference phase can remain the same. However, three times the power switching transistors and pre-drive circuitry will be required for the flux-adding phase shifting stages.

3) A substantial increase in the complexity of the low level logic will be encountered. Two additional ring counters containing six flip-flops each, two complete phase shifting networks, and two differential amplifiers will be required. This will increase the parts count as follows for the above items.

Part	From	To
Transistors	80	240
Resistors	209	627

Part	From	To
Diodes	66	198
Capacitors	72	216
Zener Diodes	24	72

The relaxation of the allowable output voltage regulation will eliminate the requirement of a second differential amplifier stage in item a and allow an averaging type voltage regulator to be used with a large reduction in circuit complexity in item b.

The present design specification for the DC variations caused by the internal source impedance is +10%, -20% about the nominal voltage of +56 volts. The averaging type of voltage feedback circuit allows the phase shifted stepped waveform to swing from $\angle\Theta \sim +16°$ at 44.8 V DC for its full load case to $\angle\Theta \sim 90°$ at 61.6 V DC for its no-load case. If the allowable DC variations on the source is reduced, then the required corrective phase shift angle will also be less. Therefore, the number of phase shifting stages can be reduced to a minimum of one for a minimum source regulation of 1.6%. Each phase shifting stage will provide a maximum phase shift of 30°.

A maximum weight reduction of 18.8% for the output transformer can be expected for this reduction in source regulation to 1.6%. The reliability of the phase shifting circuits is improved with the reduction of the source regulation to 1.6% (R = .976765/year for three-phase shifting stages to R = .989511/year for one-phase shifting stage). The switching losses for the input voltage regulator that is used to provide the necessary voltage to all the low-level logic circuitry will also be reduced by 17.3% when the source regulation is reduced to 1.6%.

If the tolerance on the source regulation is allowed to increase, then its limit is determined by the maximum flux density that the output transformer can support for this particular transformer design. The switching transistor's collector to emitter voltage rating before a bridge configuration is required will also limit the increase in regulation tolerance.

The absolute no-load voltage limit appears to be about 70 V before the output transformer has to be redesigned to support this voltage for a bridge configuration required for the present switching transistor (150 V_p - 150A power transistors). This increase in the input

voltage tolerance to 70 V_p will require no load voltage regulation in the phase shift region between 90° and 120°. Therefore, four phase shifting stages are required to provide the 0° to 120° phase shift range necessary for a maximum source regulation of 58.4%. A maximum weight increase of 9.2% for the output transformer will occur while the reliability of the phase shifting circuits will be reduced (R = .976765/year for three-phase shifting stages to R = .970454/year for four-phase shifting stages) with the increase in the source regulation to 58.4%. The switching losses for the input voltage regulator that is used to provide the necessary voltage to all the low-level logic circuitry will be increased by 8.69% when the source regulation is increased to 58.4%.

DESIGN OF A 400 CPS PULSE WIDTH MODULATION INVERTER

I INTRODUCTION

Multi-Stepped Waveform techniques and Pulse Width Modulation techniques were both considered for this 400 cps - 10 KW Inverter. The Pulse Width Modulation scheme was selected for this 400 cps - 10 KW Inverter because this approach appeared to offer a substantial weight savings without sacrificing efficiency or reliability. Examining the various Pulse Width Modulation Techniques revealed that classical (not commutated) Pulse Width Modulation with natural sampling would require the least amount of inverter circuit complexity and AC filter weight. Therefore, this approach was chosen so that an optimum trade-off between reliability, efficiency, and weight could be obtained for this 400 cps - 10 KW Inverter.

The design of an inverter utilizing classical Pulse Width Modulation with natural sampling can be directed by examining the spectra of the output waveform (Figure 4-98). This spectra represents the maximum amplitude that the carrier frequency and its sidebands as well as their harmonics can obtain relative to the power frequency for a modulation index M of .9. The first indication as to direction is the large number of high frequency components in the spectra. If a conventional parallel output stage and transformer is used, a very large hysteresis and eddy current loss component can be expected. Therefore, the inverter should be a power transformerless device in order to maintain a high operating efficiency.

In order to build a transformerless inverter, the input voltage must be high enough to produce a usable output voltage. Therefore, a DC - DC converter must be used at the inverter input. Since the output voltage of the inverter must be alternating, three phase and four wire, the DC - DC converter must be bipolar. The following sections are used to establish this 400 cps - 10 KW Pulse Width Modulation inverter design.

II PULSE WIDTH MODULATION

Certain types of pulse modulation techniques outlined in Section III-E (High Frequency Techniques of this report) were considered to produce waveforms that would contain a low total harmonic content with relatively simple inverter circuitry. It is the purpose of this section to further explore the various types of pulse width modulated inverter techniques in an effort to determine which method of modulation will produce the least total harmonic distortion.

There is a general class of static inverters called "Pulse Width Modulation" inverters. These inverters operate by modulating the width, phase, or frequency of a high frequency carrier signal with a power frequency and then demodulating the resulting waveform to obtain the modulating frequency power. The expected advantages of a system such as this are:

1) Higher efficiency
2) Lower weight
3) Lower harmonic distortion

There are several forms this inverter can assume, each form has its advantages and disadvantages. These forms will be discussed here with respect to waveform and circuitry.

A. Classical Pulse Width Modulation

The classical pulse width modulation static inverter is the inverter proposed by A. A. Sorensen in 1960. The inverter output voltage consists of a number of pulse duration modulating pulses having their trailing edge modulated by a power frequency (see Figure 4-21).

The analysis of this type of waveform is extremely complicated by ordinary methods because of the non-integral relation of the modulating and carrier frequencies. However, by using a double Fourier series, the waveform can be analyzed. The method developed by W. R. Bennett and explained by H. S. Black [15] is a very useful explanation of the double Fourier series analysis technique. Black's treatment of the subject yields two equations describing the spectra of a pulse width modulating waveform; one for natural sampling and one for uniform sampling.

a) Uniform Sampling

The difference between natural and uniform sampling is quite subtle and undetectable by visual examination of the resulting waveform, but is readily seen by examining the spectra of the waveforms. Basically, uniform sampling is the modulating technique whereby the pulse width is proportional to the instantaneous value of the modulating wave at uniformly spaced sampling times. This is shown in Figure 4-99. The top waveform is the

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[15] "Modulation Theory", D. Van Nostrand Company, Inc., 1953, by Harold S. Black

modulating signal. Superimposed on the modulating signal are lines representing uniform sampling times. Superimposed on this waveform is the resulting pulse amplitude modulated waveform representing the value of the modulating signal at the uniform sampling times. Added to this waveform is the sweep wave from the synchronizer from which the pulse width modulated waveform is obtained. The width of the resulting pulse is equal to the width of the summed sweep and PAM wave when intersected by the control value. A typical block diagram of a Uniform Sampling PWM Inverter is shown in Figure 4-100.

The spectra of a pulse width modulating waveform employing uniform sampling can be expressed by the following equation which is a modification of an equation by Black[15].

$$F(t) = \sum_{n=1}^{\infty} \frac{\frac{(n\pi M \omega_v)}{\omega_c}}{\frac{n\pi\omega_v}{\omega_c}} \sin\left(n\omega_v t - \frac{n\pi\omega_v}{\omega_c} - \frac{n\pi}{2}\right)$$

$$- \sum_{n=1}^{\infty} \frac{\sin m\omega_c t - jo(m\pi M)\sin(m\omega_c t - M\pi)}{m\pi} \quad (4\text{-}32)$$

$$+ \sum_{n=1}^{\infty} \sum_{n=\pm 1}^{n=\pm\infty} \frac{jn\left[(m\omega_c + n\omega_v)\frac{\pi m}{\omega_c}\right]}{(m\omega_c + n\omega_v)\frac{\pi}{\omega_c}} \sin\left[(m\omega_c + n\omega_v)\left(t - \frac{\pi}{\omega_c}\right) - \frac{n\pi}{2}\right]$$

where M is the modulation index, which is defined as the amount of excursion of the trailing edges of the modulated pulses.

$M \cos \omega_v$ is the modulating wave.

and ω_c is the carrier wave angular frequency.

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[15] op. cit.

In order to get the maximum value for the modulating wave component, a modulation index of 1.0 will be used. This is contrary to usual practices in communications but expedient for power conversion. A spectrum representing the above equation is shown in Figure (4-101). A ratio of 25 to one was used for the carrier to modulating signal ratio.

If the modulation is decreased from a value of I.0, the fundamental component decreases and the carrier frequency amplitude increases. The unwarranted increase makes it more difficult to filter the output. The spectrum shows the fundamental (ω_v) component having a relative value of one. The carrier and its harmonics and sidebands are seen to diminish rapidly and a filter that cuts off at about $15\omega_v$ will completely eliminate these components. An undesirable aspect of this type of modulation (uniform) is seen by the presence of second, third, fourth, fifth, and sixth harmonics of ω_v. These harmonics are quite close to ω_v and will require a rather large and heavy filter to eliminate them.

The method of uniform sampling has the undesirable property of producing unwanted and hard to remove harmonics. The sampling method which does not produce these fundamental harmonics is natural sampling which will be discussed next.

b) Natural Sampling

Figure 4-102 illustrates the natural sampling method for modulating the width of a train of pulses. It can be seen that the pulse width is a function of the average value of the modulating waveform during the sampling interval and not the value of the waveform at the instant of sampling. A block diagram of a naturally sampled PWM inverter is shown in Figure 4-103. The expression for the spectra of a naturally sampled pulse width modulation is (from Black);[15]

$$F(t) = \frac{M}{2}\cos\omega_v t + \sum_{m=1}^{\infty} \frac{\sin m\omega_c t}{m\pi} \qquad (4\text{-}33)$$

$$- \sum_{m=1}^{\infty} \frac{jo(m\pi M)}{m\pi} \sin(m\omega_c t - m\pi)$$

(continued on next page)

[15] op. cit.

(continued from previous page)

$$- \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{n=\pm \infty} \frac{j\, n(m\pi M)}{m\pi} \sin\left(m\omega_c t + n\omega_v t - m\pi - \frac{n\pi}{2}\right)$$

where M is the modulation index

$M \cos \omega_v t$ is the modulating voltage

ω_v is the carrier angular frequency

The spectra is shown in Figure 4-104. ($\omega_c = 25\omega_v$ for sample calculation.)

It is seen that natural sampling yields a spectra identical to the spectra for uniform sampling with the exception of harmonics of the modulation frequency. The naturally sampled waveform is free of lower harmonics ($2\omega_v$, $3\omega_v$, $4\omega_v$, etc) and the lowest harmonics are sidebands of the carrier frequency.

The above discussion makes a very good case for natural sampling as the type to use for a static inverter since the filtering problem is considerably lessened when compared to the uniform sampling method.

Another type of output voltage that is beginning to gain popularity is a form of pulse width modulation which produces pulses that are commutated. The pulses appear in bunches having a square wave envelope. The next paragraphs will examine this waveform.

B. Commutated Pulse Width Modulation

The commutated pulse width modulated waveform is shown in Figure 4-105. It is obtained by first rectifying the modulating wave as shown in the top waveforms of the figure. This waveform is then operated on by the modulator as before. The resulting pulse width modulated waveform is then commutated by a square wave which is in synchronism with the modulating waveform. The resulting commutated waveform is shown at the bottom of the figure. A block diagram for Uniform Sampling - Commutated PWM inverter is illustrated in Figure 4-106.

The analysis of this waveform is exceedingly difficult. A triple Fourier series expansion can be used to analyze the waveform where the three functions of time are the rectified modulating wave, the sweep wave and the commutating signal. However, the expressions for the modulating wave and the commutation wave make the triple Fourier series extremely complicated. A simple method of analysis, while not as accurate, has been used to analyze the waveform.

The method of analysis used was to break the waveform down into a number of simple quasi-square waves, each having an on-time equal to the width of an individual pulse in the waveform. Each quasi-square was then given a phase-shift and analyzed. The harmonic components of like frequency in all the quasi-square waves were then summed. The result was a number of harmonics of various amplitudes and is shown on the spectra of the waveform seen in Figure 4-107.

The commutated waveform spectra reveals that a large number of undesirable harmonics are present; namely, the third, fifth, seventh and eleventh. These harmonics are the result of the sampling method used (uniform) and will diminish if natural sampling is used. It is important to notice that the spectrum of this waveform is nearly identical to the classical pulse width modulated waveform and is clearly no improvement of that waveform.

The choice of waveform to be used by an inverter can be decided by comparing the circuit complexity required for each method (classical or commutated). Each inverter requires a dc-dc converter if a high voltage DC input is not available, a logic stage, a power inversion stage, and an output filter. Regulation is accomplished for each inverter by either controlling the index of modulation M, by incorporating regulation in the DC - DC converter, or using some type of AC regulator. However, the commutated waveform inverter will require a commutator or demodulator stage and its associated logic circuitry. The size and weight of this additional circuitry will more than offset the reduction in output filter size and weight that will be obtained for this commutated waveform inverter. Additional inverter power loss will also be contributed by this demodulator. Therefore, the classical Pulse Width Modulation approach with natural sampling is best by virtue of simplicity.

III GENERAL DESCRIPTION

The block diagram of the complete inverter is shown in Figure 4-108. The three phase square wave reference generator produces the low frequency (400 cps) modulating signal. These three signals are displaced 120 degrees with respect to each other to establish the three phase

relationship of the output voltage. The reference waves are then passed through controllable attenuators which have a normal attenuation of zero, but when an overload current is detected at an output line, the proper attenuator is activated to attenuate the size of the modulating signal which in turn reduces the voltage of the overloaded line. After passing through the attenuator, the fundamental frequency of the output square wave is extracted by the tuned amplifier which has a unity voltage gain at 400 cps. The purity of this resulting sinewave is as high as practical because it determines the waveshapes of the output voltage. The modulating sine-waves are then mixed with the sweep wave in the three summing networks. The resulting waveform is a sinusoidally undulating sawtooth wave which is then sent to the slicer circuit. The slicer circuit is an absolute level detecting system that produces pulses having a width proportional to the modulating signal level during the sampling interval. The sampling interval is determined by the sweep wave generator which produces a sawtooth sweep wave at the carrier frequency. The variable pulse width signal is then amplified and sent to the driver stage which transforms this signal into a form suitable for use by the power stages. The power stages convert the low level drive signals into the required high power level output. The power source for the power stage is the regulated DC - DC input converter. The input converter raises the input voltage to the required voltage level for use by the power stages. The high power output voltage of the inverter is then filtered to eliminate the carrier and its sidebands from the output voltage leaving only the power frequency voltage. The voltage regulator and reference develops an error signal which is fed back to the input regulator to maintain a constant output voltage. Also present at the output lines are three current transformers which detect any overload currents and act on the modulating signal via the current limit and reference circuit to reduce the power frequency output voltage thereby limiting the overload current. The individual blocks will be discussed in more detail in the following sections.

IV POWER STAGE

The circuit of the power stage for the PWM inverter is shown in Figure 4-109. The voltage waveshapes at various points in the power stage are shown in Figure 4-111. Waveshape (a) illustrates the inverter output voltage before filtering. This is a pulse width modulated waveshape that is naturally sampled (see "Pulse Width Modulation" - Section II-A-B of this report) and has a modulation index M less than one. A perfect inverter can have a modulation index M of one but this implies an infinitely narrow pulse width at extremes of the modulating waveform. While this is desirable, since it produces the maximum output voltage, it is impossible to produce in practice because of transistor switching speed limitations.

A modulation index M of 0.9 produces a minimum pulse width of 10 microseconds which can be reasonably reproduced by a transistor which switches in one microsecond.

The input voltage required to produce rated output voltage in the power inverter is a function of the modulation index M and the filter efficiency at the power frequency (400 cps). In our case, the modulation index M is 0.9 and a 5% voltage drop can be expected in the filter at full load. With this information, the input voltage can be determined. The 400 cycle component before the filter is:

$$E_1 = 115\,(1 + 0.05) = 121 \text{ volts rms}$$

since

$$V \text{ (input voltage)} = \frac{e_1}{M} \text{ where } e_1 = \sqrt{2}\,E_1$$

$$V = \frac{121\sqrt{2}}{M} = 190 \text{ volts}$$

The voltage across one of the half phases is shown in waveform (b) of Figure 4-111. This voltage has a magnitude of 2V or

$$V_{CE_{max}} = 2 \times 190 = 380 \text{ volts.}$$

This rather high voltage can be effectively switched by one high voltage transistor. An RCA developmental type TA 2110 has a V_{CEX} of 400 volts with a V_{EB} of 8 volts. However, this voltage rating is too low when a voltage safety factor is considered. A 400 volt transistor permits only 20 volts or a 5% safety factor. This situation is improved by using two transistors in series which yields a safety factor of 800/380 or 211%.

The next problem to be solved is to equally divide the supply voltage across the power transistors when they are in the "off" condition. Due to the possibility of unequal I_{CEX} currents (I_{CEX} is the collector leakage current when the base emitter junction is reverse biased) in the two series transistors, the effective resistive equivalent of the two transistors may vary widely and cause an unequal voltage distribution across them. Any voltage unbalance automatically reduces the safety factor. In order to reduce the possibility of voltage unbalance, a voltage divider resistor (R_d) is included in parallel with each transistor.

The value of the divider resistor is a function of the maximum unbalance in I_{CEX} in the power transistors and the maximum tolerable voltage

unbalance allowed between the two "off" transistors. In order to determine what size Rd should be the series power transistors can be thought of as resistors having a resistance equal to V_{CE} divided by the leakage current I_{CEX}.

$$R = \frac{V_{CE}}{I_{CEX}} \tag{4-34}$$

The value of R will vary from transistor to transistor because of the spread of I_{CEX}. This spread will produce two values of R, a maximum and a minimum value, Namely R_M and R_m respectively. The ratio of R_M to R_m is called (a).

$$R_M = a\, R_m \tag{4-35}$$

An equivalent circuit can be drawn of the series transistors and divider resistors combination and is shown on Figure 4-112.

The equation for the circuit is:

$$I\left[\left(\frac{R_d R_M}{R_d+R_M}\right) + \left(\frac{R_d R_m}{R_d+R_m}\right)\right] = V \tag{4-36}$$

Let k equal a voltage unbalance factor such that:

$$I\left(\frac{R_d R_M}{R_d+R_M}\right) = I\,k\left(\frac{R_d R_m}{R_d+R_m}\right) \tag{4-37}$$

cancelling I and solving for Rd;

$$R_d = \frac{R_M R_m (k-1)}{(R_M - k\,R_m)} \tag{4-38}$$

But since $R_M = a\, R_m$ the equation becomes:

$$R_d = \frac{a\, R_m (k-1)}{(a-k)} \tag{4-39}$$

The values of R_d are plotted in Figure 4-112 for values of (a) from 2 to 20 and for values of k from 1.1 to 2.4.

From the graph of R_d on Figure 4-112, it can be seen R_d varies from 0.1 R_m to ∞R_m. This is a very large range, but it can be narrowed by limiting the maximum voltage across any transistor to twice the voltage across its series partner which determines a value of k equal to two (2.0). (A value of k equal to 2.0 yields a safety factor of 150%.) Also, since a very large number of transistors are to be used, it should be a simple matter to arrange them in groups of two which have a maximum R_M to R_m ratio of 10. With these restrictions (k=2.0 or less and a = 10 or less), a value R_d can be found from the graph which is 1.25 R_m.

Since we are using a TA 2110 transistor which has a I_{CEX} maximum of 10 ma. at 400 volts ($R_m = \frac{400}{10^{-2}}$ = 40 K), then R_d is equal to 1.25 R_m or 50 Kilohms.

The power rating of the resistor is equal to the maximum voltage across any divider resistor squared divided by R_d or

$$P = \frac{E^2}{R_d} \tag{4-40}$$

where $$E = \left(\frac{k}{k+1}\right) V \tag{4-41}$$

therefore $$P = \frac{\left(\frac{k}{k+1}\right)^2 V^2}{R_d} \tag{4-42}$$

in our case $$P = \frac{\left(\frac{2}{(2+1)}\right)^2 (380)^2}{50 \times 10^3} = 1.28 \text{ watts} \tag{4-43}$$

The voltage divider resistors R_d will be of the wire wound type whose temperature coefficient will be matched as close as possible to that of the power transistors in order to minimize the change in voltage balances as the ambient temperature changes. During the time when the power transistors are turning "off", the voltage dividing resistors are useless because the turn-off or fall times of the two series connected transistors are not exactly equal. The unequal fall times cause a situation in which the full supply voltage is developed across the fastest transistor to turn off. In order to prevent damage to the transistor by these unwanted voltage transients, a zener diode clamp with a value of less then V_{CEX} and greater than 2V is shunted across each transistor. In our case a zener diode rated between 380 and 400 volts is required. A diode with a value of 395 volts can be easily obtained by a series connection of two standard zener diodes. The current

rating of the zener diode should be at least ten times $I_{CEX_{max}}$ in order to provide maximum effectiveness which means the zener diodes must have a power rating of about 20 watts each. The nearest zener diode rating to 20 watts is 50 watts which will provide a good safety margin.

The current rating of the TA 2110 power transistor is 10 amperes while the rated load current is:

$$I_L = \frac{10 \text{ KW}}{.7 \text{ PF} \times 115\text{V} \times 3 \text{ phases}} = 41.4 \text{ amps}$$

The peak current is:

$$I_{peak} = \sqrt{2} \times 41.4 = 58.6 \text{ amps}$$

The waveshape of the transistor power switch current is shown in Figure 4-111 for unity power factor load. With overload and short circuit considerations, the power switch current may be as high as 250 percent rated current or a maximum current of:

$$I_m = 2.5 \times 58.6 = 147 \text{ amps}$$

In order to switch this large amount of current at least fifteen power transistors must be connected in parallel in each half phase using a closed chain balancing reactor system. The power stage circuit complexity can be reduced by reducing the number of paralleled transistor switch legs required if larger current capacity power transistors with compatible switching times and V_{CE} voltage ratings can be found. The balancing reactors assure the equal distribution of current between the paralleled transistors.

The balancing reactors must be designed to support V_o per coil at a current of 10 amperes and a frequency of 10 kilocycles. V_o is the total unbalance voltage that may be presented by the transistor switches and is equal to difference between the maximum and minimum saturation voltage of the series connected transistors or

$$V_o = (2\, V_{CEmax} - 2\, V_{CEmin}) \qquad (4\text{-}44)$$

The coefficient 2 is used because two transistors are connected in series. The maximum and minimum saturation voltage for the type TA 2110 power transistor is:

$\frac{I_C}{10 \text{ amp}}$	$\frac{V_{CE\ sat\ max}}{1.0 \text{ volts}}$	$\frac{V_{CE\ sat\ min}}{0.6 \text{ volts}}$

The voltage V_o that the balancing reactor must support is equal to:

$$V_o = (2 \times 1.0) - (2 \times .6) = 0.8 \text{ volts}$$

The wire for the balancing reactor must have a cross section of 5,000 circular mils based on a 500 c.m. per amp rating. A number twelve conductor will be quite sufficient (5184 c.m.).

Since the operating frequency is quite high and the supporting voltage of the coil (V_o) is quite low, a very small core may be used. In order to determine the core size (cross sectional area) the number of turns is fixed first. In this case assume that each coil will have three turns. The required core area can then be determined if the maximum flux density is known. Assume here that Hy Mu 80 is used which has a B max of 7 KG. Therefore, from the equation

$$N = \frac{V_o \times 10^8}{2\ BmfA}$$

From Quarterly Report No. 2, page 107 of the "Optimization Study of High Power Static Inverters and Converters" -NASA-CR-54021) (4-45)

The required area is

$$N = \frac{V_o \times 10^8}{2BmFA} \qquad (4\text{-}46)$$

where

A = the core area in square centimeters
V_o = the unbalance voltage
B_m = maximum flux density in Gauss
f = frequency of operation in cycles per second
N = number of turns per coil.

Therefore

$$A = \frac{0.8 \times 10^8}{2 \times 7 \times 10^3 \times 10^4 \times 3} = 0.191 \text{ sq. cm.}$$

or

$$A = \frac{0.191}{(2.54)^2} = 0.0296 \text{ square inches}$$

A suitable lamination to use for the core is the 34-E size which has an outside dimension of 0.75 x 0.82 inches and a center leg width of 0.249 inches. If .014 in. thick laminations are used, a total of 9 laminations will provide the required cross sectional area. The weight of 9 laminations is 0.0199 pounds. The resulting core loss is about 1 watt per pound or about 0.02 watts per core. The copper weight is about 15 gms or .033 pounds and will be practically lossless. The total weight of the reactor will be .053 pounds and have a constant loss of .02 watts. Figure 4-113 shows this reactor.

In order to prevent reverse current from flowing through the power transistors, a blocking diode is connected in series with each half phase. When the blocking diode is in the circuit the reactive current has no path so a reactive current diode is placed across each half phase. The current through the reactive diode is shown in waveshape (d) of Figure 4-111.

The rating of the blocking diode and the reactive diode is determined by the maximum rms current that they are required to conduct. The blocking diode is required to conduct almost a complete half cycle of current which has a full cycle rms magnitude of 104 amps for the 250% overload case. This means the rating of the blocking diode is one half the maximum peak current or

$$I_{rating} = 1/2 \sqrt{2} \times 104 = 73.6 \text{ amps (average over one cycle of 400 cps.)}$$

Another characteristic which must also be considered when choosing a blocking diode is the recovery or commutation time. Most rectifiers have a construction directed toward low forward drop and current handling ability and are quite efficient at 60 to 400 cps operation. When operated at frequencies such as those encountered in this inverter they become quite inefficient. The inefficiency is due to the rather long commutation time required to return the diode to its blocking state, this time usually runs from 1 to 5 microseconds.

In order to overcome this difficulty a fast recovery type diode must be used. Diodes are available that recover their blocking state less than 200 nanoseconds. The only difficulty with these diodes is the low current handling ability. At present, the maximum current rating of fast recovery diodes is 30 amps.

Paralleling of the 30 amp rectifiers is necessary to meet the 73.6 amp required rating. This is accomplished by dividing the paralleled power transistors in each half phase into groups of three and connecting one 30 amp fast recovery diode to each group. With this technique, the balancing reactors used for dividing the current equally among the power transistors also divides the current equally through the blocking diodes. This arrangement is shown in Figure 4-109.

The reactive current diodes must also be of the fast recovery type because of the very high operating frequency. The rating of the reactive diode is about 30 amps. This rating can be met with one rectifier.

A. Power Stage Efficiency

The power stage efficiency will be calculated here for half load, full load, and twice rated load. (The power factor of the load is 0.7.) The losses will be classified into three categories; "on" losses, "off" losses, and switching losses. The items that dissipate power are power transistors, balancing reactors, blocking diodes, reactive current diodes, base-drive resistors, and the divider resistors.

The first item of power loss calculated will be the transistor "on" losses. The current waveform through the power transistors is shown in (c) of Figure 4-114. The rms value of the current is

$$I_{rms} = \frac{1}{\sqrt{2}} I_L \times M \qquad (4\text{-}47)$$

where I_L = rms load current

M = index of modulation

The "on" losses in the transistors are

$$P_{ton} = (I_{rms})^2 R_{sat-eq} \qquad (4\text{-}48)$$

where $R_{sat-eq.} = \frac{2R_{sat}}{15}$

where R_{sat} = saturation resistance of one power transistor

$R_{sat-eq.}$ = Equivalent saturation resistance of the series-parallel combination of 30 transistors.

therefore

$$P_{ton} = \left(\frac{1}{\sqrt{2}} I_L M\right)^2 \frac{2 R_{sat}}{15} \text{ (transistor "n" losses)} \qquad (4\text{-}49)$$

In our case, the factor M and R_{sat} remain constant so the transistor "on" losses can be tabulated as follows. (It must be remembered that this table and others like it are the losses computed for one half phase containing 30 series - parallel transistor combinations. The total power losses will be collected later.)

TABLE 4-10

	I_L Amps	M	$\left(\frac{1}{\sqrt{2}} I_L M\right)^2$	$\frac{2R_{sat}}{15}$ *	$P_{t\text{-}on\text{-}watts}$
Half rated load	20.7	.9	173	.0133	2.3
Full rated load	41.4	.9	693	.0133	9.24
Twice rated load	82.8	.9	2775	.0133	36.9

* Maximum R-sat for TA 2110 is 0.1 Ω

The transistor "off" losses will now be calculated. This loss will be calculated together with the divider resistor loss because of their intimate relationship in a four element network.

Previous calculations determined an equivalent resistance for the transistors of 400 K and 40 K (maximum difference assumed) and a divider resistor value of 50 K. The equivalent two terminal network has a resistance of:

$$R = \left[\left(\frac{R_d R_m}{R_d + R_m}\right) + \left(\frac{R_d R_M}{R_d + R_M}\right)\right] \frac{1}{15} \qquad (4\text{-}50)$$

where R_d = divider resistance
R_m = minimum transistor resistance
R_M = maximum transistor resistance
15 = number of paralleled combinations

$$R = \left[\frac{(50\text{x}10^3 \text{x} 40\text{x}10^3)}{(50\text{x}10^3 + 40\text{x}10^3)} + \frac{(50\text{x}10^3 \text{x} 400\text{x}10^3)}{(50\text{x}10^3 + 400\text{x}10^3)}\right] \frac{1}{15}$$

$$R = 4.45\text{x}10^3 \Omega$$

The transistor-divider resistor "off" losses remain constant regardless of the inverter load.

$$P_{t\text{-}R_d}\text{-off} = \frac{(2V)^2}{R} \qquad (4\text{-}51)$$

$$P_{t\text{-}R_d}\text{-off} = \frac{(380)^2}{4.45\times10^3} = 32.4 \text{ watts}$$

The transistor - divider resistor "off" losses ($P_{t\text{-}R_d}$-off) are computed for each half phase containing 30 series - parallel transistor combinations. The total transistor - divider resistor "off" losses will be collected later.

The power loss in the blocking diode is proportional to the load current and is

$$P_{BD} = \left(\frac{1}{\sqrt{2}}\ I_L M\right) V_d \qquad (4\text{-}52)$$

where V_d = the diode voltage drop

V_d = 1 volt

TABLE 4-11

	$P_{B\text{-}D}$-watts
Half rated load	13.17
Full rated load	26.4
Twice rated load	52.7

The power loss in the balancing reactors is principally core loss and this will remain constant over the load range. Previous calculations have indicated a power loss of .02 watt per reactor. The total balancing reactor loss is:

$$P_{BR} = 15 \times .02 = .30 \text{ watts}$$

The reactive current diodes conduct only during the spaces between the power switch pulses. The current they conduct is approximately

$$I = \frac{1}{(2\sqrt{2})}\ I_L M, \quad P_{RD} = V_d I \qquad (4\text{-}53)$$

TABLE 4-12

	I-amps	P_{RD} - watts
Half rated load	6.57	6.57
Full rated load	13.14	13.14
Twice rated load	26.28	26.28

The only remaining semiconductors are the zener diodes. During normal operation of the inverter, these diodes should not conduct for more than 1/2 microsecond. This conduction occurs during the switching transient that occurs at the rise and fall time of each power pulse or at a 20 KC rate. The current should be less than 100 milliamps.

The power dissipated by the zeners is:

$$P_{ZD} = (f \times t \times I \times V_z) N \qquad (4\text{-}54)$$

where

f = rep rate of transient
t = length of transient
I = current
V_z = zener voltage
N = number of zeners per half phase.

$$P_{ZD} = 20\times10^{3} \times .5\times10^{-6} \times .100\times200\times60 = 12 \text{ watts}$$

The rather low average power dissipation of the zener diodes infers that small zener diodes may be used. This is not the fact, however, because the zener must be able to support rather high instantaneous power pulses. It is this rather high power pulse that raised the power level of the zener diodes to fifty watts each. Probably the best way to size the zener diode rating is to build the circuit and measure the actual transient current for a number of cases and rate the zener according to the highest current pulse detected.

The switching losses in the power transistors will be calculated next. Because of the continuously varying magnitude of collector current that must be switched, a discreet calculation for each switching instant must be made. The transistor switching power loss may be expressed as follows:

$$P_{t-s} = \frac{1}{T} \int_{o}^{ts} eidt \qquad (4\text{-}55)$$

where

T = period of power cycle $(\frac{1}{f_v})$

e = transistor voltage during switching

i = transistor current during switching

ts = length of transistor switching transient for either "rise" or "fall" times.

The switching transient of current and voltage are assumed to be linear functions with respect to time. The voltage transient e is:

$$e = V_{CE\ max} \left[1 - \frac{t}{ts} \right] \qquad (4\text{-}56)$$

where $V_{CE\ max}$ = maximum collector voltage

t = incremental switching transient time

The current i during the switching transient is:

$$i = \frac{I_L \sqrt{2}\ t\ \gamma}{ts} \qquad (4\text{-}57)$$

Where γ is the percent of peak load current $\sqrt{2}\ I_L$ at the instant of switching.

The switching power dissipation per switching instant may be expressed as:

$$P_{t-s} = \frac{1}{T} \int_{o}^{ts} \gamma V_o \frac{t}{ts} \left[1 - \frac{t}{ts} \right] I_L \sqrt{2}\ dt \qquad (4\text{-}58)$$

which becomes

$$P_{t-s} = \frac{V_o I_L \sqrt{2}\ ts\ \gamma}{6T} \qquad (4\text{-}59)$$

The total transistor switching power for n switching instants per power cycle may be expressed as:

$$P_{t-s}\ \text{Total} = \frac{V_o \sqrt{2}}{6T}\ I_L \sum_{k=1}^{k=n} \gamma\ ts$$

where the $\sum_{k=1}^{k=n} \gamma\ ts$ represents

the summation of the percentage of peak load current times the transistor "rise" and "fall" times. These products are determined alternately and then summed.

Because an arbitrary value of voltage unbalance of two was chosen for the voltage division across the two series transistors, two power calculations were made for each load current value. The values of P_{t-s} are tabulated below.

TABLE 4-13

	Half Rated Load	Rated Load	Twice Rated Load
$P_{t-s}{}^1$	6.53 watts	13.06 watts	26.12 watts
$P_{t-s}{}^2$	3.26 watts	6.52 watts	13.04 watts
P_{t-s} Total watts	9.79 watts	19.58 watts	39.16 watts

The transistor base drive requirements are 1.7 $V_{BE\ max}$ at one amp. A three volt output will be supplied from each secondary drive winding. The base drive resistor required for each transistor is 1.3 ohms with a 10 watt dissipation capacity. The total base drive loss per transistor circuit is 3 watts and is 90 watts loss per half phase. The total base drive loss per transistor circuit will remain constant independent of the transistor load because it is a constant voltage base drive scheme.

B. Power Stage Weight Breakdown

The following is a list of the PWM static inverter power stage parts. The part quantity and weight are listed to provide a total parts weight and count. There may be a certain degree of inaccuracy in the total weight due to certain unknowns. The unknowns are items like the weight of terminals required on the balancing reactors or the weight of the insulation required on this component.

TABLE 4-14

Item	Quan	Wt. Ea.	Total Wt.
Power Transistors - Type TA 2110	180	0.143 lb	25.8 lb
Zener Diodes - Type 1N3350	360	.0264	9.52
Reverse Blocking Diode Type 1N3918	18	.03125	0.562
Reactive Current Diode Type 1N3918	6	.03125	0.187
Balancing Reactors	90	.053	4.770
Divider Resistor - 50K - 10W	180	.0125	2.25
Base Drive Resistor- 1.3Ω -10W	180	.0125	2.25
Drive Transformer	45	.22	9.9
	1059 parts		55.239 lb

Total Power Stage Losses:

TABLE 4-15

Dissipating Item	Half Rated Load	Rated Load	Twice Rated Load
Transistor "on" losses	13.8	55.4	221.5
Transistor** "off" losses	194.4	194.4	194.4
Transistor Switching Losses	58.8	117.6	235.2
Transistor Base Drive Losses	540	540	540
Blocking Diode Losses	79	158	316
Reactive Diode Loss	39.4	78.8	157.6
Zener Diode Loss	72	72	72
Balancing Reactors	1.80	1.80	1.80
Total Watts Loss	999.2 W	1218.0 W	1738.5 W
Power Output	5000 W	10000 W	20000 W
Power Stage* Efficiency	83.34%	89.14%	92.0%

* Efficiency $= \left(\frac{P_{out}}{P_{out}+P_{loss}} \right) \times 100$ (4-60)

** Transistor "off" losses are composed of leakage losses and divider resistor losses.

V DC-DC CONVERTER STUDY

A. Introduction

While many of the problem areas associated with inverters are also found in the design of DC-DC converters, there are many aspects in which they differ. Hence, a separate study of converters is worthwhile.

Converters come in many different configurations as can readily be appreciated. Some are used to convert to DC at a higher potential than the primary source, and some are used to convert to a lower potential. Many have only one output voltage, while others provide many different outputs. The power handled varies over wide ranges. It follows, therefore, that the choice of a particular conversion method and the optimization of it depends on the application.

For the purpose of this study, it has been decided to concentrate on a converter which could be used in the Pulse Width Modulation scheme decided in Section II - "Pulse Width Modulation" of this report. This means we are directing the effort toward the design of a converter which has two outputs, both having the same potential and power ratings, although one voltage is positive, with respect to ground, while the other is negative. The total required output power is slightly in excess of 10 KW. Inasmuch as our specification dictates a substantial step-up in voltage, the use of a transformer switching stage is indicated.

Because of the high power involved, and the necessity of providing well regulated and well filtered power, systems utilizing other than push-pull outputs were disregarded. Those systems which were considered worthy of study are discussed next.

B. Inversion Methods

While most inversion modes use basically square wave generation for high efficiency operation, a number of modifications are possible in order to provide regulation. These methods unfortunately, in general, provide voltage regulation capability only at the expense of a need for more filtering and less efficient utilization of switches and transformers.

Since our requirement is for two separate outputs, both producing the same magnitude of voltage, it was felt that the use of two separate output regulators would add unnecessary complexity to the system.

This leaves us with the choice of using either inherent regulation in the conversion stage or an input regulator.

Methods which were considered were:

1) Pure Square Wave Generation with external regulation
2) Quasi-Square Wave Generation using

   a) One Power Stage

   b) Two Phase Shifted Power Stages

a) Pure Square Wave Generation with External Regulation

This method of conversion has much to recommend it. It utilizes two power switch elements connected in a push-pull configuration, and generates pure square waves, which are transformed to the power output voltage and then rectified and filtered. Because the rectifier operates on pure square waves, very little filtering is necessary. However, voltage regulation must be provided by amplitude modulation through control of the DC input to this stage. This control can be provided by a switching type of regulator. Two variants are possible: 1) the use of a "Morgan" chopper or similar circuit, or 2) the use of a pulse width modulated rider on top of the DC battery voltage. Both of these systems are usable here because no restraint is placed on their output voltage, other than what is reasonable from the standpoint of the power switch voltage specifications. Obviously, too low an output voltage requires that larger currents be handled.

b) Quasi-Square Wave Generation

Whereas the previous method had no inherent regulation capability, the generation of quasi-square waves does provide this function. Two different methods of generating these waves are possible. First, the conduction time of the power switches can be controlled, so that quasi-square waves rather than pure square waves are generated. Alternatively, two stages, both generating pure squares, can be used. By phase shifting one with respect to the other, and adding their outputs, quasi-square waves can also be formed.

The use of two stages is preferable for two reasons: (1) since high power is being handled, paralleling of transistors will probably be required. The necessity of using a minimum of four transistors in this system is thus not a serious drawback, in fact it may be considered to be beneficial since this system yields extra benefits other than simple higher power capability: (2) two of the four power switches are always "on" - there never is a period when the transformer looks like a high impedance. This is highly desirable, especially since our load is not a pure resistance.

c) Selection of a System

Because we are somewhat limited in frequency due to the necessity of using high current devices, it behooves us to select a system which uses a minimum number of magnetic components.

The pure square wave system with pulse width modulated riders has a distinct advantage in this respect. The output filter can be very small since pure square waves are being rectified, and the switching stage used to control the DC input to this stage need handle only the "boost" power, i.e. the power needed to raise the battery voltage up to its maximum. It follows, therefore, that at the high battery input voltage the switch handles no power, while the maximum power it handles is at the low battery condition. All of the other systems handle full power regardless of the input voltage. This means that the transformer used in the switching section can be smaller for the boost system than for the other approaches. Both of these factors contribute to a lower overall system weight, so this was the type of regulator selected.

C. Weight and Efficiency Versus Frequency Tradeoffs

One of the major problems confronting the designer in DC to DC converters is the selection of an operating frequency.

It is a problem since it has such a major effect on losses and weight. Barring other restraints, the selection will normally be a high frequency for low magnetic component weight or a low frequency for low transistor switching losses and low transformer losses; hence high efficiency, or a medium frequency as a compromise.

Since we are confronted with the problem of handling high power, our selection of a switching transistor is somewhat limited unless large

scale paralleling is used. The use of a high current transistor rather limits the choice of frequency, since they are restricted in their switching speed. For this reason, a frequency of one kilocycle was arbitrarily picked as the operating frequency. This appears to represent a reasonable compromise between extremely low weight and very high efficiencies. A more detailed analysis will be required to determine the most optimum operating frequency in regards to weight, reliability, and efficiency tradeoffs.

D. Detailed Design

The complete regulator design is shown in Figures 4-115 and 4-116. A parts list is included, showing representative values (Figure 4-117).

a) Power Stage

To step up the regulated DC voltage to the desired ±200 V DC, a push-pull stage comprising transistors Q_{3a} - Q_{3b} - Q_{4a} and Q_{4b} and transformer T_2 is used. This stage generates pure square waves at a frequency on 1 KC. Zener diodes D_5, D_6, D_7 and D_8 are used to protect the transistors against overvoltages.

Because of the high currents being switched, it was necessary to parallel two transistors per switch. Silicon Transistor Corp. type 2501 transistors will be used and balancing reactors (T_3 and T_4) will be provided to force current sharing.

b) Rectifier - Filter

The rectifier circuit comprising diodes D_9-D_{10}-D_{11} and D_{12} converts the generated square waves to DC. In actuality while this rectifier resembles a bridge circuit, it actually operates as two full wave circuits in tandem. One produces the positive output, and the other the negative. This turns out to be a very efficient usage of the transformer. The filter consists of a very small filter choke (L_2) and capacitors C_4 and C_5. Resistors R_{12} and R_{13} are bleeders.

c) Input Regulator

To amplitude modulate the square wave power circuit a DC input regulator is used.

This circuit, comprised of controlled rectifiers, SCR_1 and SCR_2, transistors Q_1 and Q_2, transformer T_1 and filter L_1 and C_3 works by adding width modulated pulses on top of the battery voltage.

These pulses are actually parts of pure square waves being generated by transistors Q_1 and Q_2. The pulse width is modulated by controlling the firing point of the two SCR's. At maximum battery voltage the SCR's will not conduct at all, so the DC current flows from the battery through diode D_3 to the output. At a battery potential less than maximum but greater than minimum, the DC current will flow along this same path until the SCR is fired sometime during the square wave half cycle. The initiation of SCR conduction automatically commutates the diode D_3 and a higher voltage "pulse" is added to the battery potential through the SCR. The SCR's are themselves automatically commutated by the reversal of voltage from the transformer. By using the SCR's from an AC source, the need for external commutating circuitry is avoided. The RC network shunting the SCR's are used to alleviate dv/dt problems since we are operating at a moderately high frequency and using square waves. The SCR's should also be selected for high dv/dt capability.

The transistors Q_1 and Q_2 form a square wave push-pull generator. It should be noted that this stage provides only the boost power, that is, the difference between the minimum and maximum battery voltage. The closer these two figures are to each other, the less power this stage has to handle. Zener diodes D_1 and D_2 act as overvoltage surpressors to protect the transistors.

The output filter of the regulator is comprised of choke L_1 and capacitor C_3. Note that since the "raw" input voltage to the filter does not have the large voltage swing which is common to most types of switching regulators, that the required filter elements are small. Diode D_4 acts as a free-wheeling diode. Resistor R_3 is a bleeder on the filter.

d) Oscillator and Driver

A Jensen type two core square wave oscillator is used as the basic frequency reference. Frequency is held to within ±5% by the zener voltage regulator on the DC input to this stage.

Power is taken from this stage to drive both the transistorized output and regulator stages, and also to provide drive for the magnetic amplifier MA-1. This mag amp is used to control the

firing angle of the SCR's in the regulator. The positive output voltage of the DC-DC converter is returned to the control winding of the SCR control magamp MA-1. When the battery voltage is high, the current in the control winding reduces the magamp conduction angle which in turn reduces the SCR firing angles. When the battery voltage becomes low, the current in the control winding increases the magamp's conduction angle which in turn increases the SCR firing angles. The amount of feedback control is determined by the ampere-turns that is set by potentiometer R_{24} on the bias winding. To provide fast rising gate drive waveforms for these SCR's, Shockley diodes D_{18} and D_{21} are used as fast switching wave shaping devices. The output voltage from this circuitry is stepped down to the required gate voltages by transformer T_7. Fast rising gate waveforms are necessary if excessive SCR power loss is to be avoided.

Because the frequency tolerance is not hypercritical, it is not expected that any buffering of the oscillator will be needed. This can be provided if it proves necessary, however.

e) Input Filter

Since this regulator is basically a switching type system, an input filter will undoubtedly be required. A simple Pi type should be sufficient.

E. Expected Weights and Losses

TABLE 4-16

	Weight	Losses
Transformer T_1	13.0	66.4
Transformer T_2	26.9	124.1
Diodes $D_9 \rightarrow D_{12}$	0.5	60.2
Balancing Reactors	0.5	26.0
SCR_1 - SCR_2	0.5	200.0
Choke L_1	2.4	80.0

TABLE 4-16 (continued)

	Weight	Losses
Transistors Q_1 Q_2	0.5	126.9
Transistors Q_{3a}, Q_{3b}, Q_{4a}, Q_{4b}.	1.0	278.4
Miscellaneous	5.0	50.0
TOTAL	50.3 lbs	1012.0 watts

Efficiency = 10,700/10,700 + 1012

$\eta \cong 91.4\%$

VI LOGIC

A. 2.4 KC Clock

The 2.4 KC Clock is a multivibrator oscillator (Figure 4-118 and 4-119) that runs at six times the output frequency of the inverter or 2.4 KC. This clock triggers the three phase square wave oscillator which divides the clock frequency by six to yield the required 400 cps control signal. The frequency accuracy of the clock will be maintained at ±0.5 percent over a temperature range of -55°C to +85°C without an oven. Also, any variation in input voltage (15V) up to ±20% will not change the frequency accuracy or stability. The good stability is obtained by clamping the collector voltage of transistors Q67 and Q68 with the zener diode D58 and also clamping the timing RC network supply voltage. Temperature compensation is obtained by virtue of the fact that the diodes D48, D60 and D58 have temperature coefficients that cancel over the temperature range.

The output voltage of the oscillator is a square wave with a rather slow rise time of approximately 20 to 30 microseconds and very sharp fall time of less than one microsecond. The falling edge of the square wave is used by the three phase square wave oscillator. The sharp fall time is differentiated by the input circuit of the oscillator and amplified to produce a negative pulse of approximately 12

volts magnitude and 1/2 microsecond duration to provide a reliably acting trigger pulse for the oscillator.

B. Three Phase Square Wave Oscillator

The three phase square wave oscillator produces the basic three phase time reference for the inverter. The output voltage of the oscillator is three square wave voltages displaced exactly 120 degrees in time. The amplitude of the square wave output voltage is approximately 10 volts peak to peak and has a frequency of one-sixth of the clock frequency or 400 cps.

The oscillator is constructed of three interconnected flip-flops (see schematic diagram on Figure 4-120), an input pulse shaper, and an "and" gate. The input pulse shaper circuit has a 2.4 KC clock output for its input. The clock output voltage is differentiated and amplified by the circuit to produce a very sharp negative pulse which is used to trigger the three flip-flops.

The three flip-flops are connected by the steering resistors R_6, R_7, R_{15}, R_{16}, R_{24} and R_{25} to form a turn "off" mode ring counter. These steering resistors serve to control the counting sequence of this ring counter with the introduction of each negative trigger pulse. Assume that transistors Q_3, Q_5 and Q_8 of the ring counter are put in a saturated state from a previous negative trigger pulse. Examining the voltages across the base circuit steering diodes reveals that diodes D_2, D_5, and D_7 have large reverse bias voltages across them while diodes D_3, D_4, and D_6 have small reverse bias voltages across them. However, only the saturated transistor Q_5 has a small reverse bias voltage across its steering diode D_4. Thus the next incoming negative trigger pulse will turn "off" transistor Q_5 which in turn will cause transistor Q_6 to saturate changing the state of the ring counter. The flip-flops will continue to change state sequentially with each negative trigger pulse. Thus six negative trigger pulses will be required to make a complete count on the ring counter. Therefore, the output frequency of each flip-flop is one half of the frequency of the effective input pulses or 400 cps since the clock frequency is 2.4 KC.

The "and" circuit consisting of the diode-resistor-capacitor-transistor network on the right side of Figure 4-120 insures that the three flip-flop sequencing network does not lock into an undesirable mode of operation. The undesirable mode of operation is when all three

flip-flops act as one and the output voltages are in phase and at the wrong frequency.

The accuracy of the phase separation of the three square waves is maintained to less than one-sixth of a degree and is a function of the stability of the 2.4 KC clock.

C. Current Reference Circuit and Attenuators

The current reference portion of this circuit is shown in the lower section of Figure 4-122. The circuit consists of a current transformer, a burden resistor, a full wave rectifier bridge, and a small filter section. The load current in the output lines produces a proportional voltage at the output of this circuit. This voltage is then compared with reference diode D24. The polarities are arranged such that the potential of Point X is always negative with respect to ground until the load current exceeds twice the rated load current. When twice the rated load current is exceeded the potential of Point X becomes positive and begins to turn on the shunt blocking transistor Q19.

The shunt blocking transistor acts as a variable resistor which shunts the output current from the three phase oscillator to ground thereby reducing the voltage at the output of the emitter follower. This portion of the circuit is called the attenuator.

The function of the current reference and attenuator circuit is to vary the amplitude of the modulation signal to the following stages of the inverter which will reduce the amplitude of the fundamental voltage at the inverter output terminals. The reduction of the output voltage will reduce the output current thereby stabilizing the maximum load current to approximately 200 percent of the rated load current. When the inverter is operating in this mode, it appears to be a constant current generator and when the overload is removed the inverter returns instantaneously to its correct operating mode of a constant voltage generator.

D. Tuned Amplifiers

The tuned amplifiers operate on the square wave reference voltages and transforms them into ultra-pure sine waves. The amplifier , consisting of transistors Q_{10}, Q_{11}, Q_{12}, is used as a very sharp band pass amplifier as shown in Figure 4-124. This is accomplished by using a twin - T, R-C filter network in the feedback of this amplifier. The twin-T null frequency is adjusted to 400 cps which

is the fundamental frequency of the square wave that is introduced into this amplifier. At this null frequency of 400 cps, the output of the twin-T filter network is zero, thus making the amount of negative feedback zero causing the gain of the amplifier to be the same as the gain of this amplifier without any feedback. On either side of this null frequency (400 cps), the amount of negative feedback increases sharply which causes the amplifier gain to decrease sharply. Thus, only the fundamental frequency of 400 cps will be passed by this band pass amplifier while the odd harmonics of this input square wave will be suppressed and will not appear at the amplifier output.

The output voltage of the tuned amplifier is proportional to the input voltage which comes from the three phase square wave oscillator via the current reference and attenuator circuits. In the event of an overload the amplitude of the sine wave voltage out of the tuned amplifier decreases. The output of the amplifier is then mixed with a sawtooth carrier frequency sweep voltage in the summing networks.

E. Sawtooth Sweep Wave Generator

The sawtooth sweep wave generator is a circuit that produces the sweep wave required to accomplish pulse width modulation. The circuit diagram is shown in Figure 4-126. The ramp generation portion of the circuit is built around Q25. This transistor is a current generator which generates a current having a value equal to the emitter voltage divided by the emitter resistor. Since the emitter voltage is held constant by the zener diode (D25) in the base circuit the emitter current (and therefore the collector current) is held constant. The constant current flow through C36 charges the capacitor up in a linear fashion.

The maximum voltage the capacitor can charge to is the supply voltage, less the collector voltage minimum, which is approximately the zener diode voltage. Once this voltage is reached the capacitor voltage stops increasing and the ramp of voltage ends. In order to produce a repetitive sawtooth voltage, the capacitor must be discharged; this is accomplished with a discharge transistor (Q26) across the capacitor. The discharge transistor gets its drive signal from the Schmitt Trigger circuit consisting of Q27, 28 and 29.

The Schmitt Trigger produces a signal before the collector voltage of Q25 approaches its minimum value and in turn causes the capacitor to discharge while it is still charging linearly. In operation, this

circuit produces an ultralinear sawtooth sweep wave with a frequency of 10 kilocycles.

The output is taken off the collector of Q_{25} and passed through a Darlington emitter follower. The high input impedance of the emitter follower prevents loading of the constant current charging circuit which would affect the linearity of the sawtooth sweep wave.

The sweep wave is then connected to one of the inputs of the summing networks and is common to all three phases of the inverter.

F. Summing Networks

The summing networks mix the sine wave output of the tuned amplifiers and the sawtooth voltage output of the sweep wave generator. The network consists basically of a difference amplifier (see Figure 4-128); one input is the sine wave and the other is the sweep wave whose output is the difference between the two input signals. Summing is accomplished by inverting the sense of one of the signals but is not necessary in this case because the signal which must be inverted is the sine wave. The inversion of this sine wave merely imparts a 180 degree phase shift to the output signal and, as long as all three phases are shifted equally, no defect is imparted to the system.

The emitter follower input circuit seen on each difference amplifier prevents loading of the tuned amplifier circuits.

G. Slicer-Amplifier

The slicer-amplifier circuit is shown in Figure 4-130. This circuit is a high-gain switching amplifier that turns on when the input voltage exceeds the reference voltage established by zener diode D32. The output of this circuit is a train of pulse width modulated pulses having a spectrum as seen on Figure 4-98. The modulation index M is adjusted by trimming the magnitude of the modulation signal at the input of the attenuators. This can be accomplished by adjusting the value of the attenuator input resistors R_{59}, R_{64}, and R_{69} of Figure 4-122.

The output pulses from this circuit are then amplified by the driver stages.

H. Driver Stages

The driver stages are shown in Figure 4-132. This circuit amplifies the pulses out of the slicer-amplifier to a level sufficient to drive the power transistors of the power stages into saturation. Each driver must supply one ampere at a three volt level to each power transistor input circuit and there are thirty power transistors to be turned "on" at once by each drive stage. The total power delivered by each driver is then 90 watts.

The driver transformer that must transform the power from the drive stage to the power transistor is quite special because each power transistor in the power stage requires a separate drive winding. This means that each transformer (one per phase) must have sixty secondaries. Also, the leakage inductance of the transformer must be quite low because excessive leakage inductance will reduce the rise-time of the drive voltages and therefore increase switching losses and produce unwanted distortion. Unfortunately, at present, it is not possible to construct a transformer like this, the largest problem being the excessive leakage reactance between the primary and the sixty secondaries.

A reasonable way out of the driver transformer dilemma is to divide the transformer into fifteen small transformers having four secondaries each and their primaries connected in parallel. By using this approach, the driver transformer can have its secondary and primary windings interleaved in a practical manner to reduce the leakage reactance to a minimum. Figure 4-133 illustrates a method by which all coils (primary and secondary) are wound at once creating a multifilar coil with very close coupling between every wire. This technique can reduce the overall leakage inductance considerably.

Another advantage of using the incremental approach on the drive transistor is the more equal distribution of lead lengths when assembling the inverter. This will reduce the possibility of unwanted lead inductance differences and power drops in long wires.

The driver circuit itself is quite unusual by the fact that the output transistors (Q_{54} and Q_{55}, for example) are not driven into saturation. The reason for this is that if these transistors are saturated, the large number of carriers in the junction region causes a large storage time. If the transistor is not saturated, the number of carriers is less and

therefore the storage time is shorter than in the saturated case. The reduction of storage time to a minimum implies that the switching time is decreased, which is a desirable feature.

The clamping of the collectors of transistors Q_{54} and Q_{55} is accomplished with diodes D_{33} and D_{34}. The base drive current turns on the transistor but when the transistor begins to approach saturation, the collector voltage tries to go below the base-emitter voltage. Before this can happen the diodes (D_{33} and D_{34}) become forward biased and divert the base drive current into the collector. Since the base current required to drive the collector into saturation is diverted, the transistor does not saturate. The circuits preceeding the drive transistors are merely amplifiers and phase shifting circuits to provide drive signals for the main drive transistors.

I. Voltage Regulator Sense Circuit

This circuit is a simple transformer-rectifier-filter circuit (Figure 4-135) which produces a direct-current output voltage proportional to the average output voltage of all three phases of the inverter. This direct-current voltage is fed into the control winding of the mag-amp phase-shift firing circuit of the dc-dc input voltage converter. When the inverter output voltage rises or falls, the variable voltage from the sense circuit causes the input converter to reduce or increase its output voltage thereby maintaining a constant inverter output voltage.

J. Output Filter

The output filter is a simple LC low pass filter section. An examination of the spectrum (Figure 4-98) indicates that the maximum harmonic is the twenty-fifth and the lowest significant harmonic is the twentieth. A permissible voltage drop of 5% was allowed for full load operation which helps to determine the size of the inductor. The resultant reactance at 400 cps, that allows for a 5% voltage drop at full load current, becomes .146 ohms. The filter inductance can then be found and is equal to 58.3 microhenry at 400 cps. The size of the filter capacitor in this LC section shall be such that the largest harmonic is attenuated to less than two percent of the fundamental voltage. The largest harmonic frequency is the carrier which is approximately 51% of the fundamental. A reduction to two percent or less of the fundamental requires an approximate reduction of twenty-five to one in the amplitude of this frequency. In order to perform the reduction, an impedance ratio of twenty-five to one between the inductor and capacitor at this carrier frequency (10 KC)

is required. The inductive reactance at this carrier frequency of 10 KC becomes 3.65 ohms. Therefore, the capacitive reactance should be .146 ohms. The resultant value of capacitance becomes 109.2 ufd.

VII TOTAL WEIGHTS AND EFFICIENCIES

A. Estimated Weight

The complete inverter, less package and heat sinks, is estimated to weigh 147.539 lbs. This weight is distributed as follows:

Power Stages	55.239
DC-DC Converter	50.3
Output Filters	36.0
Logic	6.0
	147.539 lbs

The logic weight is composed of the following elements:

Transistors and Diodes	1.9 lbs
Capacitors	1.3
Transformers	1.2
Resistors and Potentiometers	1.3
Input Filter Components	.3
	6.0 lbs

It is estimated that three 10 lb capacitors and three 2 lb chokes will be required for the three AC filters, hence the overall weight of 36 lbs for the output filter components.

B. Estimated Efficiency

The overall system efficiency is estimated to be 80.4% at full load. The losses are distributed as follows:

Logic	100 watts
DC-DC Converter	1012
Power Stages	1218
Output Filters	105
	2435 watts

$$\text{Efficiency} = \frac{10,000}{12,435} = 80.4\%$$

The major losses, contributed by the DC-DC converter and the power stages, are detailed in Tables 4-15 and 4-16.

VIII RESULTS OF RELIABILITY STUDY FOR 400 CPS - 10 KW PULSE WIDTH MODULATION INVERTER

A reliability analysis was performed on the electrical circuitry and their electrical components for the proposed 400 cps - 10 KW PWM Static Inverter. This detailed reliability analysis is given in Appendix 4-VI. The formulas, ambient temperatures, de-rating factors, and reference material described for the reliability study of the 3200 cps - 10 KW static inverter (Appendix 4-II of this report) were used for this reliability analysis. The results of this reliability analysis can only be used as a design guide to point out circuits and components that have marginal designs, since the electrical circuitry was created from a theoretical design with no actual stress measurements being taken on the circuit components.

The basic approach to the analysis of each component in the electrical system was made from the part failure rate point of view. The reliability block diagram that is used to represent the overall circuit configuration is given in Figure 4-VI-1. Examining this block diagram reveals that no redundant circuitry was used in the low level and pre-drive stage logic (block A through I). However, the Power Output Stages (block J) can contain redundant circuitry depending on the mode of failure and the permissiable maximum current allowed. If the power transistors should fail in the shorted mode, a maximum of one transistor in each switch leg or a total of 15 transistors in each half phase can short out without degradation of the output waveform. However, a catastrophic failure resulting in the loss of one half phase will occur if both transistors in one switch leg should fail in a shorted mode. If the transistors should fail in an open mode, a maximum of nine switch legs can be lost per half phase before the output capacity of the inverter drops below 100% of its full load rating.

The overall reliability figure of Merit R for this 400 cps - 10 KW PWM static inverter is then found for each of the three possible failure modes for the power output stages as follows:

A. Castrophic failure of two power transistors in the same switch leg for any of the six half phases.

   1. Twenty minute missile launch and one month continuous operation as a satellite in an earth orbit.

a. $\overline{\lambda}$ iti = .078517
b. R = .924484

2. Twenty minute missile launch and one year continuous operation as a satellite in an earth orbit.

a. $\overline{\lambda}$ iti = .696529
b. R = .498263

B. Failure in the shorted mode with a maximum of 15 transistors per half phase (one for each switch leg) for all three phases.

1. Twenty minute missile launch and one month continuous operation as a satellite in an earth orbit.

a. $\overline{\lambda}$ iti = .024997
b. R = .975313

2. Twenty minute missile launch and one year continuous operation as a satellite in an earth orbit.

a. $\overline{\lambda}$ iti = .221829
b. R = .801014

C. Failure in the open mode with a maximum of 9 switch legs removed per half phase for all three phases.

1. Twenty minute missile launch and one month continuous operation as a satellite in an earth orbit.

a. $\overline{\lambda}$ iti = .024036
b. R = .97625

2. Twenty minute missile launch and one year continuous operation as a satellite in an earth orbit.

a. $\overline{\lambda}$ iti = .213389
b. R = .808652

These overall Reliability Figures of Merit R are rather low and can be improved. Examining Figure 4-VI-1 reveals that the power switches (block J), driver stages (block I), and the input voltage regulator (block A) have the largest total failure rates (λ T). These large failure

rates were caused by the large number of circuit components required, their percent operating duty cycles, and the de-rating factors assigned to each circuit component. These failure rates can be reduced by selecting components with larger de-rating factors, a re-design of the circuitry to reduce its total number of components, or using redundant circuitry. The use of redundant circuitry on all circuits with large failure rates will greatly improve the overall figure of Merit R for this inverter design.

If overload protection such as fuses is used in each switch leg then no catastrophic failure can occur for any of these switch legs. Therefore, the reliability figures of Merit R obtained for parts B-1, 2 and C-1, 2 will be more representative of the actual reliabilities of this inverter design.

APPENDIX 4-I - Analysis of the Parallel Inverter

This appendix contains an analysis of the McMurray - Bedford parallel inverter circuit shown in Figure 4-I-1. Analytical expressions are obtained for the voltages and currents in different parts of the circuit. The effect of load on circuit operation is indicated, as well as the action of the reactive diodes.

This analysis is carried out for the circuit of Figure of 4-I-1, using SCR's. Furthermore, since the parallel inverter has a square wave output (unlike the nearly sinusoidal output possible with the series inverter) a filter is generally necessary. Since this modifies the operation of the inverter somewhat, the analysis was performed for the inverter with a filter. The filter will be assumed ideal in the sense that it presents an infinite impedance to all harmonics of the inverter output but passes the fundamental without loss or phase shift. The generalized load impedance is:

$$Z_L = |Z_L| \angle \theta$$

A1:1:1 ideal transformer is assumed, with taps at a fraction K of each of the primary windings as shown. Again, at t = o the capacitor is uncharged and both SCR's off. When SCR 1 is turned on, the equivalent circuit becomes that of Figure 4-I-2 which can be further simplified to that of Figure 4-I-3. This transformation from Figure 4-I-2 to Figure 4-I-3 requires the assumption that the transformer of Figure 4-I-2 is ideal and thus transforms the capacitor C by the square of its turns ratio from the C of Figure 4-I-2 to the $2^2C = 4C$ of Figure 4-I-3. Because the filter allows only fundamental current to flow, the high frequency of the initial charging current i results in its being effectively decoupled from the load during this first switching interval.

The equation for the current in this circuit (Figure 4-I-3 is)

$$L\frac{di_1}{dt} + \frac{1}{4C}\int_0^t i_1\,dt + \frac{v_o}{2} = E \qquad (4\text{-I-1})$$

subject to the initial conditions

$$i_1\Big|_{t=0} = 0, \quad v_c\Big|_{t=0} = v_o, \quad v_{4c}\Big|_{t=0} = \frac{v_o}{2}$$

For a general solution, it has been assumed that an initial voltage of V_o is present on the capacitor of Figure 4-I-2 (or an initial voltage of $V_o/2$ on the capacitor of Figure 4-I-3). In the specific case of the first half cycle, V_o will be set equal to zero in the general solution.

This has the solution : $$i_1 = 2\left(E - \frac{v_o}{2}\right)\sqrt{\frac{C}{L}}\,\sin\frac{t}{2\sqrt{LC}} \qquad (4\text{-I-2})$$

This equation is valid only when $i_1 \geq 0$ (because the SCR can be represented by a closed switch only in the region where it is carrying forward current) which holds for

$$0 \leq t \leq 2\pi\sqrt{LC}$$

During the period when SCR 1 is conducting, the capacitor 4C will be charged up by the current i to a value $\frac{V_c}{2}(t)$ (where V_c is the voltage across the actual capacitor C) which is given by the equation:

$$\frac{V_c}{2}(t) = \frac{V_o}{2} + \frac{1}{4C}\int_0^t i_1\,dt \qquad (4\text{-I-}3)$$

Again, this is a general expression for $\frac{V_c}{2}$ for arbitrary values of V_o; as before, for the special case of the first half cycle, we will set $V_o = 0$.

Because of the presence of the reactive diodes (D_1 and D_2) the voltage across the capacitor cannot rise to more than 2E/K, since if it did, it would require that one of the diodes would be forward biased. Thus, what happens is that the current i_1 flows into the capacitor until the capacitor voltage equals 2E/K; the current then flows in the reactive diodes. This is shown on the waveform drawing of Figure 4-I-11 which shows the startup and steady state operation of this inverter with a resistive load.

Substituting the known value for the current (eq 4-I-2) into the general equation 4-I-3 for the capacitor voltage results in an explicit expression for $\frac{V_c}{2}$:

$$\frac{V_c}{2} = \frac{V_o}{2} + \frac{1}{4C}\int_0^t i_1\,dt \qquad (4\text{-I-}4)$$

$$= \frac{V_o}{2} + \frac{1}{4C}\int_0^t 2\left(E - \frac{V_o}{2}\right)\sqrt{\frac{C}{L}}\,\sin\frac{t}{2\sqrt{LC}}\,dt$$

$$= E - \left(E - \frac{V_o}{2}\right)\cos\frac{t}{2\sqrt{LC}}$$

Equating $\frac{V_c}{2}(t)$ with the maximum value of $V_c/2$, namely E/K; one obtains the equation for the time τ_2 when the maximum voltage is reached:

$$E - \left(E - \frac{V_o}{2}\right)\cos\frac{\tau_2}{2\sqrt{LC}} = \frac{E}{K} \qquad (K \leq 1) \qquad (4\text{-I-}5)$$

Therefore

$$\tau_2 = 2\sqrt{LC}\,\cos^{-1}\left[\frac{\frac{E}{K} - E}{-\left(E - \frac{V_o}{2}\right)}\right] \qquad (4\text{-I-}6)$$

Since,

$$\frac{\frac{E}{K} - E}{-\left(E - \frac{\sqrt{o}}{2}\right)} < 0 \text{ , THEN } \frac{1}{2\sqrt{LC}}\tau_2 > \frac{\pi}{2} \qquad (4\text{-I-}7)$$

When t reaches this value, the current in the inductor is:

$$i_\Delta = 2\left(E - \frac{\sqrt{o}}{2}\right)\sqrt{\frac{C}{L}}\,\text{SIN}\left[\text{Cos}^{-1}\left[\frac{\frac{E}{K} - E}{-\left(E - \frac{\sqrt{o}}{2}\right)}\right]\right] \qquad (4\text{-I-}8)$$

$$= 2\left(E - \frac{\sqrt{o}}{2}\right)\sqrt{\frac{C}{L}}\sqrt{1 - \left[\frac{\frac{E}{K} - E}{-\left(E - \frac{\sqrt{o}}{2}\right)}\right]^2}$$

The currents in the circuit immediately before the capacitor C reaches its maximum voltage of 2E/K are shown in Figure 4-I-4. The currents immediately after are shown in Figure 4-I-5. The current i_2 is now forced around the SCR 1 - D1 loop by the inductor L; the current i_3 flows in order to maintain the NI relationship in the output transformer. The voltage across the fraction of the transformer between D1 and the battery is E; therefore the voltage across that part of the transformer winding between D1 and SCR 1 is given by $E\,\frac{(1-K)}{(K)}$. Assuming the diodes and SCR's have no internal drops, this voltage is the only one opposing the change of current in L, and this current thus decreases at a rate of $\frac{E}{L}\,\frac{(1-K)}{(K)}$ amp/sec. (4-I-9)

The time required for the current to die to zero is thus given by

$$\frac{I}{\frac{di}{dt}} = \frac{LK}{E(1-K)}\,2\left(E - \frac{\sqrt{o}}{2}\right)\sqrt{\frac{C}{L}}\sqrt{\left[1 - \frac{\frac{E}{K} - E}{-\left(E - \frac{\sqrt{o}}{2}\right)}\right]^2} = \tau_3 \text{ seconds} \qquad (4\text{-I-}10)$$

and the current i_2 during this interval is given by:

$$i_2 = 2\left(E - \frac{\sqrt{o}}{2}\right)\sqrt{\frac{C}{L}}\sqrt{1 - \left[\frac{\frac{E}{K} - E}{-\left(E - \frac{\sqrt{o}}{2}\right)}\right]^2}\left[1 - \frac{t - \tau_2}{\tau_3}\right] \qquad (4\text{-I-}11)$$

where t = o is the time of initial gating on of SCR 1. (This is just a linear decay in τ_3 seconds from the initial value of the current as given by equation 4-I-8.)

The current i_3 which must flow to maintain the NI relationships in the output transformer is given by

$$i_3 = i_2 \left(\frac{1-K}{K}\right) \qquad (4\text{-I-}12)$$

and the integral

$$\int_{t_2}^{t_3} E\, i_3\, dt = \frac{E(1-K)}{K} \int_{t_2}^{t_3} i_2\, dt \qquad (4\text{-I-}13)$$

represents the excess energy stored in the inductor being returned to the battery. These currents are also shown in the waveform drawing of Figure 4-I-10.

From these equations can be seen the reasons for having $K < 1$; if $K = 1$, (i.e., the diodes D_1 and D_2 were connected to the ends of the transformer where SCR 1 and SCR 2 respectively are) the current i_2 would continue to circulate in the L, SCR 1, D_1 loop indefinitely. (Of course, the resistance in these elements would tend to damp the currents, but all the excess energy stored in the inductance L would be dissipated in the circuit elements instead of being returned to the battery.)

The smaller K is made, the faster the energy stored in the choke is returned to the battery. However, as K is made smaller, the higher the voltage across the transformer must rise in order for the reactive diodes to become effective, and the higher the internal impedance of the inverter during reactive current periods becomes. A practical minimum value for K is 0.8.

At the end of this period of returning energy to the battery (during which the capacitor voltage has been maintained at 2E/K volts,) the commutating capacitor discharges into the load until its voltage drops to 2E volts.

If the load current at this time is I_1, then the capacitor current is $\frac{I1}{2}$ (the transformer has a 1:1:1 turns ratio) and its voltage then changes at a rate of

$$\frac{dv}{dt} = \frac{i}{C} = \frac{I_1}{2C} \quad \frac{\text{VOLTS}}{\text{SEC.}} \qquad (4\text{-I-}14)$$

The change in voltage is $\frac{2E}{K} - 2E = 2E\left(\frac{1}{K} - 1\right)$ volts; thus the time required is

$$\Delta t = \frac{\Delta V}{\frac{dv}{dt}} = \frac{2E\left(\frac{1}{K}-1\right)}{\frac{I_1}{2C}} = \frac{4CE\left(\frac{1}{K}-1\right)}{I_1} \text{ seconds} \qquad (4\text{-I-}15)$$

When this discharge has been completed, the load current is again carried by SCR 1. For a resistive load, nothing further happens until SCR 2 is gated on.

When SCR 2 is turned on, then the cycle as started with Figure (4-I-2) is repeated, only now SCR 1 must be turned off and the initial voltage on the capacitor is -2E. Equations 4-I-1 through 4-I-15 can thus be used to describe the action that occurs in the steady state, if $\sqrt{}_0$ is set equal to -2E. A complete cycle of operation is shown in Figure 4-I-11. This diagram is for the case of a pure resistive load with the output frequency of the inverter low enough so that it can be assumed that the reflected load current is constant (and zero) during the switching interval.

The time scale on this diagram is not constant; the switching intervals are expanded to show in detail the waveforms at commutation while the later period of operation is shown more to scale. Values of current and voltage are indicated and are obtained from formulas developed previously. At higher frequencies where the expanded portion of the waveform (the switching interval) becomes an increasing fraction of the total cycle, exact analysis becomes more difficult, however, for most regions of interest, the current due to switching and the load may be superimposed, because the SCR forward drop is substantially independent of current.

When load current is non-zero during the commutation period, (as will occur for reactive loads) the circuit operation becomes more involved but can be analyzed as follows: Since it has been assumed that the filter passes only fundamental current, the load current can be written.

$$i_L = A \sin(\omega_0 t - \theta_z) \qquad (4\text{-I-16})$$

where W_0 is the fundamental (output) angular frequency of the inverter (and filter) and θ_z is the angle of the combined load and filter impedance as seen by the power stage. Under the assumption that the commutation time is small compared to the period of the fundamental frequency, the load current during the commutation interval is approximately constant. This value may be anywhere between -A and +A depending on the phase angle of the load impedance as seen by the inverter output transformer. Furthermore, with the operating frequency much less than the natural resonant frequency of L and C (which will be on the order of 20 KC), the voltage developed across the inductor L by the changing current at the fundamental frequency is negligible. Under these assumptions the voltages and currents during the commutation period will be examined.

Immediately prior to the turning on of SCR 2, the voltages and currents in the circuit are as shown in Figure 4-I-6. (For this discussion, an inductive load has been assumed, so at the time of commutation of SCR 1, there is a current flowing in it from the load.) SCR 1 (about to be commutated) is carrying i_4 the (1:1) transformed load current i_L.

$$\text{AT } t = \frac{\pi}{\omega_0}, \; i_4 = i_L = A \sin(\pi - \theta_z) = A \sin\theta_z = \frac{I_0}{} \qquad (4\text{-I-17})$$

At the instant after SCR 2 is turned on, the voltages and currents are as shown in Figure 4-I-7.

Since the filter maintains the load current constant at I_o at the time of switching, the transformer, in order to maintain the relation $\Sigma NI = 0$, must carry a primary current of I_o as shown. Since the current must also be maintained in the commutating choke, the current path shown for i_5 is the only one possible. (Any current in the now unused half of the primary which would be in the proper direction to maintain the transformer NI relationship would have to flow in the reverse direction through SCR 2; this is not allowed.) SCR 1 will be reverse biased until the capacitor voltage reaches zero. If this were the only current flowing, the capacitor would reach zero volts at

$$\Delta t = \frac{C\,\Delta E}{I} = \frac{2EC}{I_o} \qquad (4\text{-I-}18)$$

However, there will also be a current flow into the capacitor as SCR 2 attempts to charge it up to 2E through the transformer. The current directions for this action are shown in Figure 4-I-8.

An exact solution for the available turn-off-time (under the assumption that the load current does not change during the commutation interval) can be obtained as follows: Figure 4-I-9 represents the circuit as SCR 1 is turned on. Here I_o is the reflected load current (assumed constant, as shown) and i is the capacitor charging current.

Under the assumption that the transformer is ideal and that the load current remains constant during commutation, the equivalent circuit of Figure 4-I-9 becomes as shown in Figure 4-I-10.

The equations for this circuit are

$$\frac{v_c}{2} = \frac{v_o}{2} + \frac{1}{4C}\int_o^t (2I_o + i)\,dt \quad , \quad L\frac{di}{dt} = E - \frac{v_c}{2} \qquad (4\text{-I-}19)$$

Eliminating VC/2, there results

$$E - L\frac{di}{dt} = \frac{v_o}{2} + \frac{1}{4C}\int_o^t (2I_o + i)\,dt \qquad (4\text{-I-}20)$$

Differentiating this and rearranging terms yields:

$$\frac{d^2 i}{dt^2} + \frac{i}{4LC} = -\frac{2I_o}{4LC} \qquad (4\text{-I-}21)$$

Subject to the initial conditions:

$$\left.\frac{di}{dt}\right|_{t=0} = \frac{E-\frac{v_0}{2}}{L} \qquad \left. i \right|_{t=0} = 0 \tag{4-I-22}$$

This has the solution:

$$i = -2I_0 + 2I_0 \cos\frac{t}{2\sqrt{LC}} + 2\sqrt{\frac{C}{L}}\left(E-\frac{v_0}{2}\right)\sin\frac{t}{2\sqrt{LC}} \tag{4-I-23}$$

The total current into the capacitor is then i + $2I_b$ or

$$i_{CAP} = 2I_0 \cos\frac{t}{2\sqrt{LC}} + 2\sqrt{\frac{C}{L}}\left(E-\frac{v_0}{2}\right)\sin\frac{t}{2\sqrt{LC}} \tag{4-I-24}$$

The voltage on the equivalent capacitor 4C will then rise from $v_0/2$ (where v_0 will actually be a negative number) through 0 towards its final value E/K. However, once the capacitor voltage passes through the zero point, the SCR being commutated (in this case SCR 1) is again forward biased, ending the available turn-off-period. The charge that must be added to the capacitor to accomplish this voltage change is

$$\Delta q = C\,\Delta v = 4C\left(0-\frac{v_0}{2}\right) = -2Cv_0 \tag{4-I-25}$$

but

$$\Delta q = \int_0^t i_{CAP}\,dt = \int_0^t \left[2I_0\cos\frac{t}{2\sqrt{LC}} + 2\sqrt{\frac{C}{L}}\left(E-\frac{v_0}{2}\right)\sin\frac{t}{2\sqrt{LC}}\right]dt \tag{4-I-26}$$

Equating these two values of Δq (and performing the integration) there results

$$4I_0\sqrt{LC}\sin\frac{t}{2\sqrt{LC}} - 4C\left(E-\frac{v_0}{2}\right)\cos\frac{t}{2\sqrt{LC}} = -4CE \tag{4-I-27}$$

Combining the sines and cosines trigonometrically results in the equation:

$$\sin\left[\frac{t}{2\sqrt{LC}} + \tan^{-1}\frac{C\left(E-\frac{v_0}{2}\right)}{I_0\sqrt{LC}}\right] = \frac{-4CE}{\sqrt{\left[4I_0\sqrt{LC}\right]^2 + \left[4C\left(E-\frac{v_0}{2}\right)\right]^2}} \tag{4-I-28}$$

which has the solution: (4-I-29)

$$t = 2\sqrt{LC}\left[\sin^{-1}\left[\frac{-CE}{\sqrt{I_0^2LC + C^2\left(E-\frac{v_0}{2}\right)^2}}\right] - \tan^{-1}\frac{-C\left(E-\frac{v_0}{2}\right)}{I_0\sqrt{LC}}\right]$$

For the case of a very large current to commutate, this expression reduces to (using the approximations $\sin\theta \cong \theta$, $\tan^{-1}\theta \cong \theta$ for θ very small and assuming that $v_0 = -2E$)

$$t = 2\sqrt{LC}\left[\frac{-CE}{I_0\sqrt{LC}} - \frac{-2CE}{I_0\sqrt{LC}}\right] = \frac{2CE}{I_0} \quad \text{which agrees} \qquad (4\text{-I-}30)$$

with this limiting case value obtained from other reasoning (equation (4-I-18)).

The voltage across the capacitor is then (for an initial voltage of -2E):

$$\frac{v_c}{2} = \frac{v_0}{2} + \frac{1}{4C}\int_0^t i\,dt = E + I_0\sqrt{\frac{L}{C}}\sin\frac{t}{2\sqrt{LC}} - 2E\cos\frac{t}{2\sqrt{LC}} \qquad (4\text{-I-}31)$$

Clearly, the value of v_c at any time t will vary as I_0 varies, so, as a limiting case, the situation where I_0 is very large will be investigated. For this case the equation for v_c can be written approximately (using the small angle trigonometric relations $\sin\theta \cong \theta$, $\cos\theta \cong 1$ for θ very small)

$$v_c = -2E + \frac{I_0 t}{2C} \qquad (4\text{-I-}32)$$

and t_4 the time at which $v_c = \frac{2E}{K}$

is given by $t_4 = \frac{4CE}{I_0}\left[1 + \frac{1}{K}\right]$ (4-I-33)

When t reaches this value, the load current, which previously went into the capacitor, now flows into the reactive diode. Because the capacitor was charged up so rapidly, the amount of extra current built up in the commutating inductor is negligible.

The current trapped in the commutating choke (the sum of the load and capacitor charging currents at the instant when the capacitor voltage reached E/K, although in this case the capacitor charging current has been taken as negligible compared to the load current) then decreases at the rate of

$\frac{E}{L}\frac{(1-K)}{K}$ amps/sec until it reaches zero.

For accurate results, the actual final current in the inductor should be used as the starting point of this linear decay. From equation 4-I-23 and Figure 4-I-9, it can be seen that the current in the inductor at any time t for which these equations are valid (which is the time from the start of commutation until the reactive diodes start to conduct) is given by

$$i_L = I_o + i = -I_o + 2I_o \cos\frac{t}{2\sqrt{LC}} + 2\sqrt{\frac{C}{L}}\left(E - \frac{\Delta E}{2}\right)\sin\frac{t}{2\sqrt{LC}} \quad (4\text{-I-}34)$$

and the largest value of t for which this is valid is given by the solution of equation 4-I-26 for the case where

$$\Delta Q = 4C\left[\frac{E}{K} - \frac{V_o}{2}\right]$$

The reactive load current continues to flow through diode D_1 however, resulting in a back bias of $\frac{E(1-K)}{K}$ volts on SCR 1 through the action of the transformer windings. This reactive current is in a direction so as to charge the battery, indicating that, in this portion of the cycle, reactive energy stored in the load during a previous cycle is being returned to the d.c. supply. Sometime before the half-cycle is half over, the load current must reverse its direction, and energy once again flows from the battery to the load via current through SCR 1 and the commutating choke. When the half cycle is over, SCR 2 is turned on and the process repeats, but with the load current reversed and SCR 1 and D1 changing places with SCR 2 and D2. This is shown on the waveform drawing of Figure 4-I-12 which, like the previous one for a resistive load (Figure 4-I-11) has the first portion of the cycle expanded to show the commutation process in detail.

From previous equations (4-I-18, 4-I-29, 4-I-30) it can be seen that for the parallel inverter there is a maximum load current that can be commutated; exceeding this value will result in inadequate turn-off time.

For this reason, the simple parallel inverter will not operate with a short circuit or under any other condition which would result in an excessive current flow at the time of commutation. Excessive current not due to the load can occur on starting a parallel inverter if the residual flux levels in the output transformer are not considered. For example, Figure 4-I-13A shows (dashed line) a typical hysteresis loop for a toroidal core, and (solid line) a B-H curve on which it would be desirable to operate, from the point of view of making maximum use of the core material. However, because the initial flux level in the transformer could be anywhere between $-B_r$ and $+B_r$ where B_r is the residual flux resulting from the maximum flux level at which the transformer is operated, the first half cycle of applied voltage could easily result in saturating the core. Should the resulting excessive magnetizing current exceed the maximum commutatible load current, the circuit would malfunction. Also, because toroidal transformers have a very high ratio of B_r to B_{max}, and because of their high permeability tend to drift towards one end of the hysteresis loop under any slight unbalance in the drive, even in a core designed for operation at a low flux density it is possible to end up at a flux level very near to the B_{max} of the core material. This is shown in

Figure 4-I-13B, where the dashed line again represents the B-H characteristic of the material and the solid line the desired (and expected) hysteresis loop. The dotted line indicates the loop that would be obtained in the steady state with a slight unbalance in the drive to the transformer, as could occur due to differences in the voltage drops across the switching elements. If an inverter were shut off while operating in this mode, and the next time it was started, the first cycle was of such a polarity so as to further increase the magnitude of this flux, the core would be driven far into saturation and the resulting excessive magnetizing current would cause failure. Thus, unless special precautions are taken to eliminate these problems, toroidal (gapless) transformers should not be used for SCR inverter output transformers. For further discussion and one solution to this problem, the reader is referred to the literature.[2] (As long as the transistors can handle the momentary high peak dissipation, inverters using transistors as the switching element will not be harmed by this occurance.) The SCR's themselves would not be damaged either, but would fail to be commutated, resulting in system failure. When using ordinary transformer cores, the air gap inherent in the construction of these units results in a residual flux of approximately zero. If a transformer with gap is then so designed that the maximum operating flux density is less than 1/2 of the saturation flux density, then the application of a full half cycle of voltage at the start will not result in saturation. However, it is not a very efficient use of the core materials to operate them at only 1/2 of their maximum flux levels. This starting problem can be overcome by making the first half cycle of only 1/2 the duration as a normal half cycle. Starting under these conditions is shown in the B-H loop of Figure 4-I-13C. Figure 4-I-14 shows the relationship between the output voltage and core flux level for this starting technique. If it is assumed that $B_r = 0$, this will result in the core being in the proper dynamic hysteresis loop from the start, and the transformer can be designed to operate near the saturation flux level of the core material. Another variation of this half cycle start idea is to use a high frequency starting technique, where the inverter is started out at least twice the normal operating frequency and the frequency gradually lowered to the operating frequency. This results in a B-H loop which "spirals" out to the steady state condition; again avoiding saturation while operating the transformer at near maximum flux levels in steady state operation. The B-H loop for this condition is shown in Figure 4-I-13D; the relationship between the flux and output voltage for this starting mode is shown in Figure 4-I-15.

During the commutation period, two parameters of the SCR being commutated are of particular importance: the turn-off-time and the dv/dt rating. The turn-off-time has been already discussed. The dv/dt rating is simply the maximum rate at which the anode voltage of the SCR can be increased without causing the device to switch into its conducting state. This turning on of the SCR due to rapidly rising anode voltage is actually due to the displacement currents in the gate region induced by the internal anode - gate capacitance of the SCR. For the simple parallel circuit, the value of dv/dt is given

[2] op. cit.

approximately by $dv/dt = i_c/C$ where i_c is the current into the commutating capacitor, and is given by

$$i_c = I_o \cos \frac{t}{2\sqrt{LC}} + \sqrt{\frac{C}{L}}\left(E - \frac{V_o}{2}\right) \sin \frac{t}{2\sqrt{LC}} \qquad (4\text{-I-}35)$$

(This is one-half the current into the equivalent capacitor of Figure 4-I-12.)

The dv/dt on the commutated SCR is thus given by

$$\frac{dv}{dt} = \frac{i_{CAP}}{C} = \frac{I_o}{C} \cos \frac{t}{2\sqrt{LC}} + \frac{\left(E - \frac{V_o}{2}\right)}{\sqrt{LC}} \sin \frac{t}{2\sqrt{LC}} \qquad (4\text{-I-}36)$$

for values of t such that the capacitor voltage is less than 2E/K. For other values of t, the values of dv/dt are less severe than this. Besides this source of dv/dt, the shock excitation of various stray circuit inductances and capacitances which occur at commutation may give rise to very high frequency oscillations which yield high dv/dt's. These oscillations can be effectively damped by putting a series RC stub across the SCR (anode to cathode). This stub will only be effective for the shock induced dv/dt's described; it will have no value in reducing the I/C component of the dv/dt; if this is too large it must be reduced by a major parameter change. (i.e. increasing C). In general, however, SCR's are available which have dv/dt ratings sufficiently high that they are not a limiting factor in the application of the SCR.

An important rating of the SCR just being turned on at this time which must be observed is its di/dt rating. When an SCR is first turned on, the current it carries is localized in a small area where it was first turned on. Thus, if the initial current allowed by the circuit is too high, the current densities in that portion of the SCR just turned on can cause degrading or destructive local heating. Methods used to minimize this problem are:

1. To turn on as much of the SCR as possible as soon as possible. This means the use of fast rising gate signals with a peak power capability approaching that of the allowable gate dissipation.

2. To limit the anode current of the SCR during the turn on to as low a value as possible.

Some circuits, for example the series inverter, have small initial currents (see equation 2c, Appendix 1-I of QR-1 of the "Optimization Study of High Power Static Inverters and Converters") while others, like the parallel inverter, require the SCR to carry a substantial initial current (I_o). In this case, the initial current is limited to a low value for the first few microseconds by putting a small saturating reactor in series with each anode lead.

APPENDIX 4-II - Reliability Study For The 3200 CPS-10 KW Static Inverter

A reliability study was performed on the electrical circuitry for the proposed 3200 cps Static Inverter. The study was based on electrical components used in the low level logic circuitry and power stages. Packaging techniques and electrical connections were not included in this reliability study. Thus, reliability of connectors, terminal boards, wire, solder joints, standoff insulators, buss bars, fuses, circuit breakers, etc., were not considered because a tentative package configuration has not been established at this time.

The basic approach to the analysis of each component in the electrical system was made from the part failure rate point of view. A reliability block diagram for the 3200 cps inverter was established in order to describe pictorially the mission of the various circuits and their components (See Figure 4-II-1). As can be seen from this block diagram, no redundant circuits were used.

Each major circuit is represented by a large block that is identified by a letter ranging from A to O. A series of sub-blocks are assigned to each major block to represent the individual circuits and/or components that are required to create a major circuit. Each sub-block is assigned an identification number. The reliability block diagram may now be used in conjunction with the representative circuits for each sub-block to establish an overall Reliability Figure of Merit R for the 3200 cps 10 KW Static Inverter.

In order to determine this Reliability Figure of Merit R, failure rates for the various components of the sub-block circuitry must be established. The operating time for each component must also be known. When these two requirements are obtained, the Reliability Figure of Merit R may be found from the following formula:

$$R = e^{-\sum_{i=1}^{N} \overline{\lambda}_i t_i} \qquad (4\text{-II-1})$$

where:

R = Overall Reliability Figure of Merit for the 3200 cps -10 KW Static Inverter.

$\overline{\lambda_i}$ = Failure rate of the i^{th} component.

ti = Operating time of the i^{th} component in hours.

$\sum$ = Symbol for summation.

e = Base for the natural logarithms.

Now the Failure Rate $\overline{\lambda}_i$ is derived from the following relationship:

$$\overline{\lambda}_i = \lambda_i K_A K_E = \lambda_i' K_E \qquad (4\text{-II-}2)$$

where:

$\lambda_i' = \lambda_i K_A$

λ_i = is the Generic Failure rate of each component in failures per 10^6 hours or 10^6 cycles.*

λ_i' = is the resultant Generic Failure Rate.

K_A = is the application or derating factor for each component.

K_E = is the environmental operating modes that will be encountered in the assigned mission for the 3200 cps Static Inverter.

*(The Generic Failure rate is a frequency function. It has a statistical connotation as it is relative to the number of failures that would be expected to occur over a large number of cycles or a long period of time. Thus two types of operations are considered as failure rate bases for this analysis. They are time dependent operations and cycled operations.)

Two mission profiles were established for the 3200 cps Static Inverter as follows:

1) 20 minute missile launch and 1 month (720 hours) continuous operation as a Satellite in an earth orbit.

2) 20 minute missile launch and 1 year (8750 hours) continuous operation as a Satellite in an earth orbit.

The maximum operating ambient temperature was established at +40°C. Temperature rises of logic components such as resistors, diodes, and capacitors above this maximum ambient temperature were assumed to be negligible with the use of appropriate derating factors and heat sinking. Low level logic transistors were given a maximum junction temperature rise of 20°C above the worst ambient. The transistors (STC2501) used as switches in power stages were given a maximum junction temperature rise of 40°C. A maximum hot spot temperature of 80°C was assigned to the pulse transformers and pre-drive transformers while hot spot temperatures of 100°C and 120°C were assigned to the output filter inductors and power transformers respectively.

Parts application data sheets were used to assemble the various pertinent information required for each component in the electrical system. The coding established from the Reliability Block Diagram and part numbers from the various circuit schematics were used on these data sheets to identify each part and its function in relationship to the blocks and sub-blocks. Wherever possible, the type and manufacture of the various components were obtained from the JPL preferred parts list (JPL Specification No. ZPP-2061-PPL-D). Deviations were recorded on the parts application data sheets. In order to obtain the generic failure rates λ_i, de-rating factors K_A, and environmental operating mode factors K_E for the various components the following reliability data was used:

"Reliability Engineering Data Series Failure Rates"

by D. R. Earles
M. F. Eddins

Avco Corporation - Research and Advanced Development Division

From this data the values for K_E can be established for each mission as follows:

1) K_E = 900 for Missile Equipment (In Flight)

2) K_E = 1 for Satellite Equipment In An Earth Orbit

Three generic failure rates (Lower Limit, Mean, Upper Limit) are given for each type of component in the Failure Rates - Life Expectancies tabulation tables provided in the above reference. The Mean generic failure rate was used since a more realistic result was felt to be obtained. These Mean generic failure rates λ_i were recorded in the parts application data sheets. The de-rating factors K_A were obtained from graphs provided in the above reference. Pertinent electrical information such as percent of operating power and operating temperatures were used to determine the de-rating factor K_A for each component from the appropriate graphs.

The resultant Mean failure rate λ' for each component may now be found by multiplying the de-rating factor K_A by the mean Generic Failure rate λ for each component in the parts application data sheets.

Typical parts application data sheets for the input flip-flop that is used in the Phase Shifter circuitry are shown in Tables 4-II-1 through 4-II-3. This input flip-flop is included as part of block C-1 illustrated in the Reliability Block Diagram for the 3200 CPS - 10 KW Static Inverter (Figure 4-II-1). Its actual circuitry and parts list are shown in Figures 4-87 and 4-88. The parts application data sheets are divided into three main categories for convenience.

These categories are solid state components, capacitors, and resistors. The mean generic failure rate λ is first determined for each of these components. The de-rating factor K_A is then found for each of these components after their operating parameters have been established. The resultant mean generic failure rate λ' for each of the components can then be found by multiplying K_A by λ .

The operating time of each component in the electrical system is expressed on a percent duty cycle basis. Thus, a 100% duty cycle would indicate that a component would be operating at its rated output for the full mission time.

Multiplying the duty cycle by the time 't' required for various parts of the mission, such as missile launch (20 minutes) or Satellite orbit, (1 month and/or 1 year) produces the exact time that the component is in use ti.

So

$$ti = t' \times \text{duty cycle} \qquad (4\text{-II-}3)$$

The product $\overline{\lambda}t$ may then be found for each component for every phase of the assigned mission. The total $\overline{\lambda}i\ ti$ product may be found for all the electrical components in the 3200 cps Static Inverter by summing the individual products $\overline{\lambda}t$ to the i^{th} component.

The overall Reliability Figure of Merit R was found from Equation (4-II-1) for each mission profile. Their results are as follows:

1) 20 minute missile launch and 1 month continuous operation as a Satellite in an earth orbit.

   a) $\overline{\lambda}i\ ti = .037175$

   b) $R = .963506$

2) 20 minute missile launch and 1 year continuous operation as a Satellite in an earth orbit.

   a) $\overline{\lambda}i\ ti = .329858$

   b) $R = .718930$

Total failure rates λT were determined for each of the major circuit blocks that appear in the Reliability Block Diagram for the 3200 CPS - 10 KW Static Inverter Figure 4-II-1. In order to obtain these total failure rates, the resultant mean generic failure rate λ' for each circuit component was first multiplied by its respective percent operating duty cycle in order to establish

a common base for all the circuit component mean generic failure rates. The establishment of this common base will then allow all these mean generic failure rates to be summed together in order to obtain a total failure rate λ T for each of the major reliability circuit blocks in Figure 4-II-1. This information was helpful in determining which circuit blocks and their sub blocks were contributing most to the reduction of the overall system reliability. Examining these reliability blocks in Figure 4-II-1 reveals that the pre-drive buffer stages (Blocks G and H, power stages (Blocks I and J) and the phase shifter circuitry (Block C) have the largest total failure rates (λ T). Their large failure rates were caused by the large number of circuit components required, the percent operating duty cycles, and the de-rating factor κ A assigned to each of the circuit components. These failure rates can be reduced by selecting components with larger de-rating factors κ A. Thus using a 300 amp power transistor in place of the present 150 amp power transistor for Q9 and Q10 in the power stages (Blocks I and J) will reduce the power transistor mean generic failure rate by more than half. (At present the 150 amp power transistor is the largest available.)

A redesign of the circuitry in Blocks G, H, I, J, and C that would result in the elimination of a large number of their electrical components would also reduce their total failure rates. If it is found that the number of circuit components cannot be reduced significantly with a complete circuit redesign, then the use of redundant circuitry can be employed to reduce these total failure rates. To illustrate the reduction of these total failure rates with redundancy, Block G for example is made completely redundant with the use of two complete and independent pre-drive buffer stages for each power stage. Its total failure rate is reduced from λ T = 6.32×10^{-6} to λ TR = $.35 \times 10^{-6}$. The total failure rate of Block G is reduced by a factor of 18 to 1 with a completely redundant system. Thus the use of redundancy on all circuits with large failure rates will greatly improve the overall Figure of Merit R for this inverter design.

APPENDIX 4-III Scaling - Class I

A. Scaling Down In Power Level

As the power level is reduced from 10 KW, there are many changes which occur in the inverter components and circuitry. The variations which occur can be divided into four types as listed below:

1) Continuous Component Changes

Many components, namely those which must be especially designed for a given inverter (for example transformers, inductors, package and heat sinking, and possibly capacitors, because they are of special manufacture and made to match exactly the requirements of the particular unit being designed) vary their size, weight and losses continuously as the power rating of the complete unit is varied.

2) Step Component Changes

Other components, which are not made specifically for a given size inverter but rather are mass produced for a larger market and are selected because their parameters meet or exceed those required by the particular application posed by a specific inverter, do not vary in a continuous fashion as the power level is decreased, but rather remain constant until the change in requirements is sufficient enough to permit the use of a lower power device, at which time a step change in the weight of the inverter would occur as lighter, lower power units are brought into play.

Transistors and SCR's are excellent examples of this type of component, where (particularly at the higher power levels) the maximum current ratings are not only discrete but fairly widely separated. It should be noted, however, that although the weight and size of these components change in a step fashion with inverter rating, the power dissipation still varies in a continuous fashion (except for the possibility of some discontinuity at places where the components are changed).

3) Fixed Components

Some components in the inverter are completely independent of the power rating of the unit. This is best typified by the master oscillator which, for a given frequency stability, has the same size, weight and loss regardless of the inverter rating. Some of the lowest level sections of the logic (starting circuits, count-down circuits, etc.) would also be in this category.

4) Circuit Changes

As the output level is considerably reduced, it might be possible to eliminate one or more stages of the drive amplifier circuits. If the desired output were very low (say 200 watts instead of 10 KW) it would probably be very desirable to use a completely different circuit. Since this downward scaling will be used only as far down as 2000 watts, (which represents a fivefold reduction in power) at which power level a 56 volt system would still require a peak collector current rating of 20 amperes, it appears that the circuit configuration proposed for the 10 KW unit would still be applicable at the 2000 watt level. Hence, all further discussions of the effects of scaling on weight, efficiency, and reliability will assume that the circuit concept used in the scaled down designs is the same as was used for the 10 KW original design. The scaling of the weight, losses, and reliability of the inverter proceeds as follows.

a) Magnetic Components

The scaling of the magnetic components of the 10 KW inverter downward will be based on the use of the Orthonol transformer and chokes as used for the middle-of-the-road design as outlined in Section VI - "Power Stage" - of this report. The weights and losses for these components for a complete 3 phase inverter are shown in Table 4-III-1.

TABLE 4-III-1

Item	Weight	Loss
Output Transformer	7.4 lbs.	176 watts
A.C. Filter Reactor	0.75 lbs.	8.1 watts
Driver Transformers	1.5 lbs.	10 watts
Delay Core	0.2 lbs.	10.8 watts
TOTAL	9.85 lbs.	205.0 watts

In Section III-B - "Scaling of Transformers" - of this report, it was shown that the weight of a transformer or inductor is related to its power handling capability by the equation

$$W = k\,(VI)^{3/4} \qquad (4\text{-III-1})$$

(where k is a constant of proportionality depending on the type and design of the component). It is shown in Appendix 4-IV that this result can be extended to a collection of transformers (not necessarily having the same k values) and that the weight of the entire group (all those required in an inverter, for example) is still proportional to the 3/4 power of the overall volt-ampere rating (of the inverter).

Using this result, the scaling can be applied to the total transformer weight as given in Table 4-III-1 instead of having to scale each individual transformer and then sum the results.

A graph of total magnetic component weight and loss versus inverter size as obtained from these scaling equations is shown in Figure 4-III-1. These weights and losses include those of the output transformer, a.c. filter reactors, drive transformers and delay cores. These are the magnetic components whose size is determined by the inverter rating. Other magnetic components, such as voltage and current feedback transformers and low level logic drive and pulse transformers, will not vary with inverter rating and hence are not included in the above scaling.

b) Semiconductor Components

1. Transistor Losses

The total losses and weight of the output stage power transistors are shown in Figure 4-III-2. Depending on the size of the inverter, either a 30A, 70A or 150A transistor is used. In all cases, the maximum peak current (under the overload conditions) does not exceed 80% of the rated transistor collector current. The losses in the transistor can be divided into the forward losses (which are proportional to the square of the current and the collector saturation resistance); the turn-off losses (which are proportional to the (constant) supply voltage, the fall time and the load current); the "off" losses (which are proportional to the leakage of any given transistor and hence are independent of the inverter output rating); and the drive losses which are directly proportional to the inverter rating. The sum of these losses as a function of the inverter power rating is shown in Figure 4-III-2.

2. Diode Losses

Figure 4-III-3 shows the losses in the reactive and base limiting diodes as a function of inverter size. These are essentially

linear, with a slight offset in the curve for the reactive diodes where the type of diode used is changed to a lighter one with a lower current rating in order to save weight. The steady state losses in the zener diodes are negligible; at the 4 KW level, a 10 watt diode can be substituted for the 50 watt device used in the 10 KW inverter reducing the weight from 1.0 lbs to 0.6 lbs. This is shown in Figure 4-III-4. Figure 4-III-4 also shows the variation of capacitor weight with the inverter power rating. Because of the nature of capacitors, their VA rating is almost linearly related to their size (for the same type unit). Hence, the capacitor weight versus inverter rating is a straight line as shown in Figure 4-III-4.

c) Logic (Control) Section

The variation in weight and loss of the control section of the inverter is shown in Figure 4-III-5. The variation in weight and loss with inverter rating is due mainly to the reduction in the amount of drive required by the output stage transistors as the output power requirements are reduced. Since the major part of the drive required by the output stage transistors is provided by the feedback windings on the drive transformers, the extra power supplied by the pulse and sustaining drives merely serves to set this feedback in the right direction and hence does not contribute materially to the drive losses in the output transistors. Hence, these losses were not counted in determining the power stage losses and thus may be now considered as part of the logic losses without having been counted twice.

d) Total Weight and Losses

The weight and loss contributions from the different sections of the inverter can now be added to obtain the anticipated weight and loss for (the electrical components of) an entire inverter as a function of the inverter rating. These results are shown in Figure 4-III-6.

B. Scaling for D.C. Input Voltage

As the nominal d.c. input voltage is changed, the inverter components most directly affected are the power output transistors. Assuming that 200 volt transistors will be available in the 150 amp sizes, and operating the transistors so that the actual current and/or voltage applied to the transistor by the circuit never exceeds 75% of the device rating, the circuit as described in Section VI-B - Transistor Configuration - of this report can be used over a nominal input range of 41 to 68 volts without

either the voltage or currents exceeding the limits. (A battery variation of +10%, -20% around the nominal value is assumed.)

When the nominal d.c. input is below 41 volts, the maximum currents required of the transistor are excessive, and they must be paralleled to provide for this. Because of the very effective use that the multiple aperture transformer makes of the iron, the most efficient technique weight and loss-wise for paralleling under these conditions is the split transformer technique. Hence, at 41 volts, the transistor weight and transformer weight undergo a step change. Similarly, for nominal d.c. inputs in excess of 68 volts, the most efficient way of modifying the circuit to avoid excessive transistor voltages is to go to a bridge configuration. This effectively cuts the transistor voltages in half and has the advantage of allowing the output transformer to be reconnected in a bridge configuration, thus allowing more efficient use of it. At still higher input voltage (above 90) the peak forward current has reduced far enough to allow the use of the next smallest size of transistor, thus allowing a slight weight saving.

Figures 4-III-7 through 4-III-11 depict the effects of the variation of the nominal d.c. input voltage on the weights and losses of the various component groups making up the inverter. Figure 4-III-7 and 4-III-8 represent weight-loss curves for the output power switching transistors and base limiting and reactive diodes respectively for the power output stages. The discreet changes in the curves represent a change in component type. The total low level logic loss and weight curves are shown in Figures 4-III-9 and 4-III-10 respectively. The largest loss and weight occur at low nominal d.c. input voltage levels. The combined magnetic component weight and loss curves are depicted in Figure 4-III-11. Again the greatest loss and weight occurs at the lower nominal d.c. input voltage levels. Step changes in the curves represent a change in magnetic component designs.

The total inverter weight and loss curves are shown in Figure 4-III-12. These curves are obtained by combining the curves obtained in Figures 4-III-7 through 4-III-11 for the inverter component groups.

APPENDIX 4-IV

Proof that a Group of Scaled Transformers Follows the Same Weight Versus Power Rating Equation as a Single Transformer

Consider two transformers, A and B, with weights and power ratings as indicated.

	Weight	Power Rating	Equation
Transformer A	W_A	P_A	$W_A = k_A P_A^{3/4}$
Transformer B	W_B	P_B	$W_B = k_B P_B^{3/4}$

Suppose both these transformers are scaled by the same ratio to new power levels P_A' and P_B' (i.e. $\frac{P_A'}{P_A} = \frac{P_B'}{P_B} = \alpha$)

Then the weights of the scaled transformers (A' and B') will be:

$$W_A' = k_A (P_A')^{3/4} \qquad W_B' = k_B (P_B')^{3/4}$$

The combined weight of the old transformers was $W_A + W_B$. The combined weight of the new transformers is

$$W_A' + W_B' = k_A (P_A')^{3/4} + k_B (P_B')^{3/4} = W_A \frac{(P_A')^{3/4}}{(P_A)^{3/4}} +$$

$$W_B \frac{(P_B')^{3/4}}{(P_B)^{3/4}} = (W_A + W_B)(\alpha)^{3/4}$$

Therefore, in the case of two (different) transformers (or reactors) whose ratings are scaled by the same factor, the sum of the weights of the transformers are scaled by this same factor. By induction, this result may then be extended to include any number of transformers.

APPENDIX 4-V Scaling-Class II

A. Harmonic Distortion

The present design specification for harmonic distortion allows for a maximum total harmonic distortion of 5% with each individual harmonic not to exceed 2%. The effects of varying this harmonic distortion specification on the inverter components were investigated with the results that only the AC output filter components weight, size, and loss were effected. The power output transformer leakage reactance and winding resistance along with the phase load impedance are used to make up part of this AC output filter. Thus only a series inductor and series capacitor and a capacitor across the load are required. In order to minimize phase shift the series inductor and capacitor are tuned exactly to the fundamental frequency of 3200 cps. The present design was considered as a point of reference upon which scaling can be accomplished. The series filter inductor consists of the transformer leakage inductance of approximately 28.2 UH in series with a 13.7 UH external inductor. The series and shunt filter capacitors are 59.2 UFD and 3.12 UFD respectively. The 11th and 13th harmonics are the predominant harmonics that must be filtered with the lower harmonics being canceled by the secondary winding turns ratio, (see section VI-C- AC Filter - of this report). The 11th harmonic was used to determine the filter component values required for various degrees of allowable harmonic distortion, since it is the most predominant of the two harmonics.

A relationship between the harmonic distortion before filtering to the harmonic distortion after filtering can be expressed as

$$HD\,(AF) = \frac{|Z_{LH}|\,|Z_{TF}|}{|Z_{LF}|\,|Z_{TH}|} \times HD\,(BF) \qquad (4\text{-}V\text{-}1)$$

where

HD (AF) - Harmonic distortion after filtering

HD (BF) - Harmonic distortion before filtering

$|Z_{LH}|$ = Load impedance at the harmonic frequency in question (including the 3.12 UFD Shunt Capacitor)

$|Z_{LF}|$ = Load impedance at the fundamental frequency (including the 3.12 UFD Shunt Capacitor)

$$|Z_{TF}| = |\overline{Z_{SF}} + \overline{Z_{LF}}|$$

$$|Z_{TH}| = |\overline{Z_{SH}} + \overline{Z_{LH}}|$$

$\overline{Z_{SF}}$ = Series filter impedance at the fundamental frequency.

$\overline{Z_{SH}}$ = Series filter impedance at the harmonic frequency in question.

The harmonic distortion before filtering HD (BF) can be found in terms of the relative phase shift angle (see Figures 4-80 and 4-81) required to maintain the proper load output voltage. The 11th harmonic will have several maxima and minima over this relative phase shift region. The amplitudes and phase angles for the maxima will be used to determine the values of the filter components necessary to provide a specified harmonic distortion level.

The maximum harmonic distortions and phase shift angles for the 11th harmonic are:

$\angle\theta$	HD (11th)
32.7°	.095
65.5°	.108
98.2°	.139
131.0°	.219

Since the series filter components are tuned at the fundamental frequency of 3200 cps, then the series impedance Z_{SF} is composed of the transformer and filter inductor winding resistance and transistors saturation resistance which are small compared with the minimum load impedance. So

$$|Z_{LF}| \sim .992 \quad |Z_{TF}|$$

$$\text{then HD (AF)} \sim 1.01 \frac{|Z_{LH}|}{|Z_{TH}|} \times \text{HD (BF)} \qquad (4\text{-V-}2)$$

$|Z_{TH}|$ may be found by specifying HD (BF) for various phase shift angles and the desired harmonic distortion after filtering. The total series inductance (L_{ST}) and capacitance (C_{ST}) may be found for the 11th harmonic using the relationships:

1. $C_{ST} = \dfrac{.544 \times 10^{-3}}{X_H}$

2. $L_{ST} = \dfrac{2.475 \times 10^{-9}}{C_{ST}}$

where $X_H \sim |Z_{TH}| + X_{LH}$

H is equal to the 11th harmonic and X_{L_H} is the load reactance at this harmonic. The transformer and filter inductor winding resistance is very small compared with the reactance at the 11th harmonic and thus can be neglected. The actual series filter inductance can be found by subtracting off the transformer leakage reactance at this harmonic frequency. The transformer leakage inductance ($L_{ST} \sim 28.2$ UH) will be the limiting case since it must be tuned out at the fundamental frequency (3200 cps). This in turn will place an upper limit on the series filter capacitor of 88 UFD. The inductor weight may be related to its inductance using the following relationship.

$$W_L \sim (1/2\, L_S\, I^2)^{3/4} \text{ pounds} \qquad (4\text{-V-3})$$

This relationship is true only when used to compare inductors of similar construction operating at the same copper current and core flux density levels. The total inductor loss (core and copper loss) and volume are then proportional to the inductor weight. From these relationships the inductor weight, total loss and volume may now be found for each phase as a function of the specified harmonic distortion for various phase shift angles as illustrated in Figure (4-V-1 to 4-V-3). The series filter capacitor weight and volume for each phase can be scaled directly assuming that the same dielectric material and dielectric voltage strength are used. The scaled filter capacitor weight and volume as a function of the allowable harmonic distortion for various phase shift angles are illustrated in Figure (4-V-4 and 4-V-5). The filter capacitor that shunts the load was maintained at 3.12 UFD since it offers a very low impedance to these higher harmonics. ($X_C \sim 1.45 \angle -90°$ under no load conditions). The total 3Ø AC filter weight and loss may be determined from the curves of Figure 4-V-1 through 4-V-5. The total 3Ø AC filter weight curves are shown in Figure 4-V-6. Examining these curves reveals that the overall filter weight increases as the tolerance on the total harmonic distortion is relaxed. This is caused by the increase in series filter capacitor size required to tune out the series filter inductor at 3200 cps. The series filter inductance requirement gets smaller as this total harmonic distortion after filtering is allowed to increase (see Figure 4-V-1). Figure 4-V-7 depicts the total 3Ø AC filter loss as a function of total harmonic distortion after filtering for various relative phase shift angles $\angle\Theta$. The losses will increase as the tolerance is reduced on the allowable harmonic distortion since the size of the series filter inductors must be increased.

Tightening the tolerance on the total harmonic distortion specification causes the series filter inductance to increase consequently reducing the capacity of the series filter capacitor in order to maintain exact tuning at 3200 cps. This will produce the following secondary effects:

a. A reduction in the voltage and current feedback sensing circuit filtering may be possible.

b. An increase in the A. C. output filter response time.

c. A tighter control on the proper secondary transformer turns ratio must be maintained to suppress the lower harmonics.

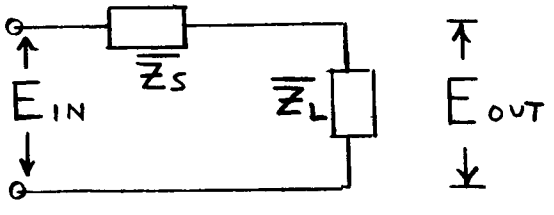
d. Improving the source and transformer regulation will reduce the size of the filter parameters required since a smaller relative phase shift angle $\angle\theta$ between the reference and phase shifted ring counters will be required with a subsequent reduction in the initial total harmonic distortion.

Opposite effects on items a, b, and c, can be realized by relaxing the tolerance on the total harmonic distortion specification.

B. Phase Separation

The present maximum phase displacement tolerance is 2°. The effects of varying this phase separation tolerance on the inverter components were investigated. The results indicate that variations in transistor saturation resistance, deviations in transformer leakage reactance and winding resistance, de-tuning of the A. C. output filters, and unsymetrical loading are the major contributors. The low level logic will provide negligible phase shift since it is composed of digital circuitry.

Of the major contributors to this phase separation, de-tuning of the A. C. output filters with a full reactive load was investigated since the A. C. output filters are composed of both the load and the transformer winding resistance and leakage inductance. The transistor saturation resistance may also be factored in as part of the transformer reflected winding resistance. An equivalent circuit for each phase may be used to determine this filter de-tuning as illustrated.



$$\frac{E_{out}}{E_{in}} = \frac{\bar{Z}_L}{\bar{Z}_T} \qquad (4\text{-V-}4)$$

Where $\bar{Z}_T = \bar{Z}_L + \bar{Z}_S$

$\overline{Z}_S$ is the total series filter impedance including the reflected transformer winding resistance and reactance and the equivalent transistor saturation resistance.

$$\overline{Z}_S = (R_F + R_T) + J(X_{LF} + X_{LT} - X_{CS}) \qquad (4\text{-V-}5)$$

where R_F = inductor winding resistance

R_T = transformer winding resistance and transistor saturation resistance reflected to the secondary side of the transformer.

X_{LF} = inductor reactance

X_{LT} = transformer leakage reactance

X_{CS} = series filter capacitor reactance

$\overline{Z}_L$ = is the load impedance including the shunt capacitor and is equal to 2.24 + 1.76J at F = 3200 cps

An ideal transformer is assumed whose output voltages are exactly 120° out of phase. Thus on a per phase basis E_{IN} will have no phase shift since the transformer parameters are reflected in $\overline{Z}_S$. The output voltage phase shift on a per phase basis was then determined with respect to the input voltage as the resultant filter resonance circuit was de-tuned at 3200 cps. A representative range of nominal series filter inductors and capacitors required to produce various degrees of harmonic distortion (see Scaling Class II - Appendix 4-V-A of this report) at a maximum regulation phase shift angle $\angle\Theta$ of 131° were used. They are: (for $\angle\Theta$ = 131°)

L_{ST} min.	= 28.2 UH	C_{ST} max	= 88 UFD
L_{ST}	= 85.7 UH	C_{ST}	= 28.9 UFD
L_{ST}	= 164 UH	C_{ST}	= 15.1 UFD
L_{ST} max.	= 321 UH	C_{ST} min	= 7.7 UFD

The amount of filter phase shift angle ($\angle\alpha_o$) was first calculated with the A.C. filter perfectly tuned in order to establish an initial phase shift caused by the transformer and filter inductor winding resistance and

transistor saturation resistance. The basic transfer gain for each value of overall filter inductance becomes:

L_{ST}	$\left\lvert\frac{E_{out}}{E_{in}}\right\rvert \angle\alpha_o$
28.2 UH	.996 $\angle\pm$ .4°
85.7 UH	.994 $\angle\pm$ .5°
164 UH	.993 $\angle\pm$ .55°
321 UH	.992 $\angle\pm$ .6°

A variation of the equivalent series resistance in each phase will change this reference phase angle by a slight amount. Thus if the series resistance in phase A should be half of that of the other two phases the corresponding gain and phase shift angle for say the 321 UH equivalent filter inductor will become .996 $\angle\pm$ .4°. The gain has increased from .992 to .996 while the phase shift angle has been reduced by + .2°. The angular relationship between phase A and phase B becomes 120.2° while the angular relationship between phase A and phase C becomes 119.8°.

The reactive elements composing the series filter branch of one of the phases were then de-tuned to produce both positive and negative reactances whose magnitudes are determined by the percent of de-tuning desired, (see Figures 4-V-8 and 4-V-9). The filters in the other two phases were left tuned at the fundamental frequency. The gain and phase shift angle for the de-tuned filter were then determined as a function of the percent of de-tuning. The amount of relative phase shift angle $\angle\alpha_R$ caused by this de-tuning was determined by subtracting the phase angle $\angle\alpha$ obtained as a function of de-tuning from the reference phase angle $\angle\alpha_o$ obtained for this phase before the series filter elements were de-tuned. The relative phase shift angle $\angle\alpha_R$ for each of the four equivalent series inductors and capacitors were then plotted as a function of the percent of filter de-tuning and are illustrated in Figures 4-V-8 and 4-V-9. The filter capacitor (3.12 UFD) that shunts the load was not changed when the filter was de-tuned.

Assuming that the filter components produce an initial amount of de-tuning as shown in Figures 4-V-8 and 4-V-9, the filter can be re-tuned to the fundamental frequency (3200 cps) by placing a suitable inductor or capacitor in shunt with the respective series filter inductor or series filter capacitor. Using the data obtained for the amount of reactive unbalance obtained at

the fundamental frequency as a function of the percent de-tuning, the necessary trimming inductance or capacitance may be found to re-tune the filter. The necessary trimming components (inductor or capacitor) weight and total loss may be found as a function of the amount of corrective re-tuning required. The same weight and loss scaling techniques used for scaling the series filter elements in Scaling - Class II - Appendix 4-V section A of this report were used here. The weights and losses of these trimming inductors and capacitors can now be combined with the weights and losses for the A. C. output filter components to obtain a complete A. C. filter weight and loss for each phase. The total weights and losses for all three phase A. C. filters may now be plotted as a function of the percent output filter de-tuning that must be corrected as shown in Figures 4-V-10 through 4-V-13 for both capacitive and inductive trimming. The four curves in each of these figures represent the total 3Ø A. C. filter weight and loss as a function of percent de-tuning for four combinations of series inductance and capacitance. These four combinations represent a wide range of permissable harmonic distortion at the phase angle $\angle\Theta$ of 131°. Curve 1 represents the extreme case in which only the reflected leakage inductance of the power output transformer is used as the series filter inductance. It is theoretically assumed that a shunt trimming inductor can be placed across this leakage inductance in order to establish a reference curve as shown in Figures 4-V-10 and 4-V-12.

The slopes of the four curves in Figures 4-V-10 and 4-V-11 increase progressively as the equivalent series filter inductance is increased. This is to be expected since the series filter capacitor weight is reduced in order to maintain resonance at 3200 cps. The converse is true for the four curves in Figures 4-V-12 and 4-V-13 for capacitive trimming. Since the dielectric material for the A. C. filter capacitors has not been determined at this time, it is assumed that their losses are negligable compared with the inductive components. Thus the four curves in Figure 4-V-13 have no slope as a function of percent output filter de-tuning. Also the losses attributed by the output power transformer and power transistors were not included as part of the external A. C. filter losses since they have been tabulated elsewhere.

The effects of reducing the permissable relative phase shift tolerance on all of three phases below 2° will require the following measures:

a. A tighter tolerance will be required for the series filter inductors and capacitors as well as the load shunt capacitor for each of the three phases for a prescribed harmonic distortion level.

b. A more exact tuning between the series filter components for each of the three phases will require some trimming components which will increase the weight and loss of the A. C. output filters.

c. The series filter components may have to be temperature compensated over the required operating temperature range to insure proper matching.

d. The output power transformer design will have to be given more careful consideration in order to minimize its leakage reactance and winding resistance and to provide as close a balance between its three output phases as possible.

e. The power transistors and reactive diodes should be matched for forward voltage drop and saturation resistance as close as possible.

The tolerance requirements on items a through e can be relaxed correspondingly with the relaxation of the allowable relative phase shift tolerance.

C. Voltage Regulation

The present design specification for output voltage regulation allows for a tolerance of ±2% for steady state load conditions with the source voltage held constant. The effects of varying the voltage regulation tolerance on the inverter components were investigated. The results indicate that variations in transistor saturation resistance, transformer leakage reactance and winding resistance, de-tuning of the A. C. output filter, Q of the series filter inductor, and unsymmetrical loading are the major contributors.

Since the transistor saturation resistance and transformer winding leakage reactance and resistance can be reflected to the secondary side of the transformer such that they combine with the series elements of the A. C. output filter, de-tuning of the A. C. output filter with a full reactive (. 7 PF) load was investigated as being the major factor in contributing to the voltage regulation problem. This was the same filter and load conditions that were used to specify the relative phase shift angle as a function of de-tuning in Scaling - Class II - Appendix 4-V- Section B of this report. Again an ideal transformer can be assumed whose output voltages are exact in magnitude and do not vary from no load to full load. Thus on a per phase basis E_{IN} will have no magnitude change or phase shift since the transformer and transistor parameters are reflected into the filter. The magnitude of the voltage across the load (Eout) can then be determined with respect to the input voltage as the resultant filter resonance circuit

was de-tuned at 3200 cps for each phase. The same representative range of series filter inductors and capacitors as was used for the Phase Separation investigation (see Scaling - Class II - Appendix 4-V - Section B of this report) were used again.

The percent voltage regulation can be defined as follows:

$$\% \text{ regulation} = 100 \times \frac{|E \text{ no load}| - |E \text{ full load}|}{|E \text{ full load}|} \qquad (4\text{-V-6})$$

The shunt filter capacitor (C_S = 3.12 UFD) is the only output load in the no load case and is equal to $15.92 \angle -90°$ at F = 3200 cps. Using the no load - tuned filter case as reference the following formula may be used

$$\frac{E \text{ (no load) out}}{E \text{ (no load) in}} = \frac{\bar{Z}_L \text{ no load}}{\bar{Z}_T \text{ no load}} \qquad (4\text{-V-7})$$

where

$\bar{Z}_L$ no load = 15.92 Ω

$\bar{Z}_T = \bar{Z}_L$ no load + $\bar{Z}_S$ filter

Z_S filter = R_S + 0 J for a tuned circuit

The resultant no load gain may now be found for the four representative inductors using $\bar{Z}_S$ for each case. The results are as follows for the tuned circuit:

L_S	$\bar{Z}_S$	$\frac{E \text{ out (no load)}}{E \text{ in (no load)}}$
28.2 UH	.01919 + 0J	$\sim$ 1
85.7 UH	.02321 + 0J	$\sim$ 1
164 UH	.0269 + 0J	$\sim$ 1
321 UH	.03293 + 0J	$\sim$ 1

So in all four cases approximately unity gain is obtained. Thus:

E in (no load)$\sim$E out (no load)

But E in (no load) = E in (full load) for the ideal transformer. So substituting these results into the regulation equation produces the following results.

$$\% \text{ regulation} \sim \left[\frac{1}{\frac{(E \text{ out (Full load)})}{E \text{ in}}} - 1 \right] \times 100 \qquad (4\text{-V-8})$$

The resultant transfer function gain data obtained from Scaling - Class II Appendix 4-V - Section B of this report for the four representative filter inductors may now be used to determine the output regulation as a function of the percent de-tuning (see Figures 4-V-14 and 4-V-15). The no load tuned transfer function for each representative inductor was used as a reference. Since Figures 4-V-14 and 4-V-15 and Figures 4-V-10 through 4-V-13 have the same percent of de-tuning scale on their axis of abscissas, the total three phase A. C. filter weight and loss may be found as a function of percent output voltage regulation by using the appropriate curves.

The effects of reducing the voltage regulation tolerance across the phase loads below ±2% will produce the following requirements.

a. A more exact tuning between the series filter components for each of the three phases will require trimming capacitors and/or inductors which will increase the weight and volume of the A. C. output filters.

b. A closer tolerance will be required for the series filter inductors and capacitors as well as the load shunt capacitor to insure balanced outputs for all three phases.

c. The series filter components may have to be temperature compensated over the required operating temperature range to insure proper matching.

d. The output power transformer design will have to be given more careful consideration in order to minimize its leakage reactance and winding resistance with as close a balance between the three output phases as possible.

e. The power transistors and reactive diodes should be matched as close as possible for forward voltage drop and saturation resistance.

f. An increase in the voltage feedback gain will be required with a decrease in voltage regulation tolerance. This may require another differential amplifier stage thus adding the following additional parts:

Part	Number
Transistors	4
Resistors	5

g. Unsymmetrical loading may place too large a requirement on the averaging type of voltage regulator that is presently proposed. This will require that each phase be independently voltage regulated. The resultant circuit changes for the same 10 KW inverter are as follows:

1. Three separate power output flux-adding transformers will be required, one for each phase with an increase in weight of 2.32 lb, and in total losses of 55.5 watts using the Orthonol transformer design as a reference.

2. The pre-drive reference phase can remain the same. However, three times the power switching transistors and pre-drive circuitry will be required for the flux adding phase shifting stages.

3. A substantial increase in the complexity of the low level logic will be encountered. Two additional ring counters containing six flip-flops each, two complete phase shifting networks, and two differential amplifiers will be required. This will increase the parts count as follows for the above items.

	From	To
Transistors	80	240
Resistors	209	627
Diodes	66	198
Capacitors	72	216
Zener Diodes	24	72

Magamps could be used in the output side of one ring counter that would go to the drive stages of each output transformer replacing the cascaded phase shifting circuitry and operational amplifiers. Three times the number of magamps would be required for individual phase voltage control

compared with those that would be used for the averaging voltage control. However, the inaccuracy in the magamps gains would cause additional harmonic distortion and additional filtering problems.

The tolerance requirements on items a through f can be relaxed correspondingly with the relaxation of the allowable output voltage regulation. An averaging type voltage regulator may be used again with a substantial reduction in electrical components compared with the three individual phase voltage regulators proposed in item g.

D. D. C. Variations

The present design specification for the D. C. variations caused by the internal impedance of the source allows for a D. C. variation of +10%, -20% about a nominal voltage V. In the present design V = +56 volts. The averaging type voltage feedback circuit allows the phase shifted stepped waveform to swing from $\angle\Theta \sim +16°$ at 44.8 V for its full load case to $\angle\Theta \sim 90°$ at 61.6 V for the no load case in the present design. However, provisions are made to provide a phase shift of 180° for soft starting if this feature is required. Using the present design as a reference the reduction of the required phase shift angle will consequently reduce the allowable D. C. variations on the source. Thus the following improvements can be realized:

a. Source regulation tolerance is reduced and hence its unloaded voltage must be lowered as a function of phase shift angle Θ.

Max. Source Regulation	Max. No Load Voltage	Max. Phase Shift Angle $\angle\Theta$
37.5%	61.6	90°
12.4%	49	60°
1.6%	44.3	30°

b. Assuming that the same window area and wire size are used for both primary and secondary windings of this output transformer, the weight and weight-loss product will be reduced for these lower source regulation tolerances as follows:

Percent Weight Reduction	Weight Loss Product Lb. - watts	Max. Phase Shift Angle $\angle\theta$
0%	1300	90°
14.5%	1110	60°
18.8%	1055	30°

c. If no soft starting is used then the required number of phase shifting stages can be reduced. Each phase shift stage will provide exactly 30° of phase shift. So the total number of parts that can be saved compared with the present six stages of cascaded phase shift are:

Min. No. of Required Stages	Total No. of Parts Saved	Max. Phase Shift Angle $\angle\theta$
3	153	90°
2	204	60°
1	255	30°

d. Reliability can be improved for the phase shifting circuits with the reduction of the number of stages as follows:

Required No. of Stages	Overall Reliability No. R For the Phase Shifting Circuits		Max. Phase Shift Angle $\angle\theta$
	Month	Year	
6	.995178	.957967	180°
3	.997358	.976765	90°
2	.998087	.983144	60°
1	.998814	.989511	30°

e. The switching losses in the input voltage regulator for the low level logic will be reduced with the reduction of the no-load source voltage:

Reduction in Input Regulator Switching Losses	Maximum Phase Shift Angle $\angle\Theta$
0%	90°
12.8%	60°
17.3%	30°

If the tolerance on the source regulation is allowed to increase, then the limit for this particular transformer design will be determined by the maximum flux density that the output transformer can support and the limit on the switching transistor's collector to emitter voltage ratings before a bridge configuration is required. (At present a 150 VP - 150A power transistor is available for switching.) The absolute voltage limit appears to be about 70V no load across these switching transistors for the present design. At this voltage, the safety margin for the power transistor is zero since the actual voltage seen across this transistor will be 150 VP. (Obtained by adding 2 x 70 VP + 10V, where 10V is obtained from the timing core.)

This increase in the input voltage tolerance to 70 VP will require the voltage feedback in the present design to operate in the phase shift region between 90° and 120°. This increase in phase shift angle and upper voltage tolerance will have the following effects:

a. Source regulation tolerance is increased and hence its unloaded voltage must also be increased as a function of phase shift angle $\angle\Theta$.

Max. Source Regulation	Max. No Load Voltage	Max. Phase Shift Angle $\angle\Theta$
37.5%	61.1	90°
58.4%	70	105°

b. Again assuming that the same window area and wire size are used for both primary and secondary windings of this output transformer, the weight and weight-loss product will be increased for this larger source regulation tolerance.

Percent Weight Increase	Weight Loss Product Lb - watt	Max. Phase Shift Angle $\angle\Theta$
0%	1300	90°
+9.2%	1420	105°

c. The minimum number of phase shifting stages will be increased.

Min. No. of Req. Stages	Total No. of Parts Saved	Max. Phase Shift Angle $\angle\theta$
3	153	90°
4	102	105°

d. Reliability can be improved for the phase shifting circuits with the reduction of the number of stages

Req. No. of Stages	Overall Reliability No. R For the Phase Shifting Circuits		Max. Phase Shift Angle $\angle\theta$
	Month	Year	
6	.995178	.957967	180°
4	.996630	.970454	105°
3	.997358	.976765	90°

e. The switching losses in the input voltage regulator for the low level logic will be increased with the increase in the no-load source voltage.

Increase in Input Regulator Switching Losses	Maximum Phase Shift Angle $\angle\theta$
0%	90°
8.69%	105°

APPENDIX 4-VI

Reliability Study For The 400 cps - 10KW P. W. M. Static Inverter

A reliability study was performed on the electrical circuitry for the proposed 400 cps - 10KW P. W. M. Static Inverter. The formulas, ambient temperatures and reference material described for the reliability study of the 3200 cps - 10 KW Static Inverter (Appendix 4-II of this report) were used again. This reliability study only included the electrical components that were used in the low level logic circuitry, input voltage regulator and power stages. Components such as terminal boards, connectors, wire, standoff insulators, etc., were not included since a tentative package configuration has not been established at this time.

Again, the basic approach to the analysis of each component in the electrical system was made from the part failure rate point of view. Parts application data sheets were used to assemble the various pertinent information required for each component in the electrical system. Typical parts application data sheets for the Sawtooth Sweep Generator (Block F of the Reliability Block Diagram for the 400 CPS - 10KW P. W. M. Static Inverter), are shown in Tables 4-VI-1 through 4-VI-3. Its actual circuitry and parts list are shown in Figures 4-126 and 4-127. The parts application data sheets are catagorized as to the general type of electrical component such as resistors, capacitors, and solid-state components. The mean generic failure rate λ is first determined for each of these components. The de-rating factor K_A is then found for each of these components after their operating parameters have been established. The resultant mean generic failure rate λ' for each of the components can then be found by multiplying K_A by λ . A reliability block diagram for the 400 cps P. W. M. inverter was established in order to describe pictorially the mission of the various circuits and their components (see Figure 4-VI-1). Examining this block diagram reveals that no redundant circuitry was used in the low level and pre-drive stage logic (Block A through I). However, the Power Output Stages (Block J) can contain redundant circuitry depending on the mode of failure and the permissible maximum current allowed. In the present system, the Power Output Stages (Block J) contain fifteen (15) transistor switch legs in parallel for each half phase (see power stage schematic - Figure 4-109). Each of these switch legs contains two transistors in series thus requiring 30 power transistors per half phase and a total of 180 power transistors for all three phases.

Power transistors usually fail in the shorted mode of operation. Thus, a maximum of one transistor in each switch leg or a total of fifteen transistors in each half phase may short out without degradation of the output waveforms. However, if both transistors in one switch leg should fail in a shorted mode,

then the loss of a half phase will occur resulting in a catastrophic failure of the inverter.

Fifteen switch legs are required for each half phase to provide sufficient capacity for a sustained 250% overload. Should some of these switch legs be lost through the failure of the power transistors in the open mode, then a minimum of six switch legs will be required for each half phase to provide 100% load capacity. Thus, three possible failure modes have been presented with the failure of two transistors in the shorted mode in the same switch leg producing a catastrophic failure in the inverter.

The overall reliability Figure of Merit R was found for this 400 cps - 10KW P. W. M. Static Inverter for each of the three possible failures modes for the power output stages using equation 4-II-1 of Appendix II and the data recorded in the parts application data sheets. The equivalent failure rate λ_e was determined for the redundant segments of the output power stages using the following equation:

$$\lambda_e \sim \frac{\left|(\lambda t)^N\right|}{t} \qquad (4\text{-VI-1})$$

where

$$o < \lambda t < .1$$

where λ_e = equivalent failure rate of N redundant circuits
N = number of redundant circuits
λ = resultant failure rate of each switch leg
t = time in hours of switch leg operation

Thus, $N_1 = 1$ was used for the catastrophic failure of two transistors shorted in the same switch leg while $N_2 = 2$ and $N_3 = 2.5$ were used for the failure of fifteen transistors in the shorted mode per half phase and for the removal of nine switch legs due to open transistors per half phase. The three reverse current blocking diodes that are used to supply the DC power to the fifteen parallel switch legs for each half phase may be considered as partly redundant since the loss of one due to an open junction will permit a maximum of ten switch legs to continue to function. A loss of two diodes in the open mode however, will only allow five switch legs to operate which will limit the capacity of the inverter below the 10KW design level. $N_4 = 1.5$ was then used for the loss of one reverse current blocking diode that had failed in the open mode. The overall reliability figure of merit R for this 400 cps - 10KW P. W. M. Static Inverter was then determined for each of the three possible failure modes for the power output stages as follows:

A. Catastrophic failure of two power transistors in the same switch leg for any of the six half phases.

1) 20 minute missile launch and 1 month continuous operation as a satellite in an earth orbit.

a) $\overline{\lambda}_i t_i = .078517$
b) $R = .924484$

2) 20 minute missile launch and 1 year continuous operation as a satellite in an earth orbit.

a) $\overline{\lambda}_i t_i = .696529$
b) $R = .498263$

B. Failure in the shorted mode with a maximum of 15 transistors per half phase (one for each switch leg) for all three phases.

1) 20 minute missile launch and 1 month continuous operation as a satellite in an earth orbit.

a) $\overline{\lambda}_i t_i = .024997$
b) $R = .975313$

2) 20 minute missile launch and 1 year continuous operation as a satellite in an earth orbit.

a) $\overline{\lambda}_i t_i = .221829$
b) $R = .801014$

C. Failure in the open mode with a maximum of 9 switch legs removed per half phase for all three phases.

1) 20 minute missile launch and 1 month continuous operation as a satellite in an earth orbit.

a) $\overline{\lambda}_i t_i = .024036$
b) $R = .97625$

2) 20 minute missile launch and 1 year continuous operation as a satellite in an earth orbit.

a) $\overline{\lambda}_i t_i = .213389$
b) $R = .808652$

Total failure rates λ T were determined for each of the major circuit blocks that appear in the Reliability Block Diagram for the 400 cps - 10 KW PWM Static Inverter - Figure 4-VI-1. Examining these reliability blocks in Figure 4-VI-1 reveals that the power switches (Block J), driver stages (Block I), and the input voltage regulator (Block A) have the largest total failure rates (λ T). These large failure rates were caused by the large number of circuit components required, their percent operating duty cycles, and the de-rating factor K_A assigned to each of the circuit components. These failure rates can be reduced by selecting components with larger de-rating factors K_A or reducing their percent operating duty cycles.

A redesign of the circuitry in Blocks A, I and J would also reduce their total failure rates if a major portion of their electrical components could be eliminated. If it is found that the number of circuit components cannot be significantly reduced with a complete circuit redesign, then the use of redundant circuitry can be employed to reduce these total failure rates. Block J can be used as an example to illustrate this (see Figure 4-VI-1). When no overload protection is provided for each of the 90 transistor switch legs, a minimum total failure rate λ T of 55.2×10^{-6} is obtained. However, the total failure rate λ T is reduced to 2.74×10^{-6} when suitable overload protection such as fuses are placed in each of these 90 transistor switch legs, thus preventing a catastrophic failure from occurring when both transistors in any one of the switch legs should fail in the shorted mode. Thus, the use of overload protection in the switch legs allows more confidence to be placed in the reliability figures of merit obtained for the two mission profiles in parts B-1, 2 and C-1, 2. A further reduction in total failure rates λ T for the rest of the circuitry and hence, an improvement in the overall Figure of Merit R for this inverter design can be obtained with the use of redundant circuitry.

CIRCUIT PARAMETER	BI-DIRECTIONAL SERIES	SIMPLE PARALLEL	MCMURRAY, BEDFORD	MCMURRAY
Permissible Load Variations	3:1 max load changes	3:1 max load changes	Operates from no load to full rated load	Operates from no load to full rated load
Inherent Voltage Regulation with Load Change	Poor	Fair	Good	Very Good
Efficiency	Circuit designed for fixed load 90% Circuit designed for 3:1 load change 70%	Same as Bi-directional Series	85% at rated load	90% at rated load
Weight (Inverter & Filter)	Fixed load circuit 15-20 lbs/KW 3:1 variable load circuit 35-45 lbs/KW	Fixed load circuit 18-21 lbs/KW, 3:1 variable load circuit 25-30 lbs/KW	25-35 lbs/KW	23-27 lbs/KW
Control Circuitry	Simple	Simple	Simple	More Complex
Other Comments	Fail-safe under loss of drive	Not suitable for large variations in inductive loading		

Note: Portions of this table are taken from information presented in: "Quarterly Progress Report #4 on Voltage Regulation and Power Stability in Unconventional Electrical Generator Systems, prepared by General Electric for Bureau of Naval Weapons Contract NOw 60-0824-C, p. 69. (This table is based on operation at 400 $\sim$, 28 VDC in, 115 V out, 1KW power level)

COMPARISON OF INVERTER CIRCUITS

TABLE 4 - 1

Functional Block	No. Per Unit	SCR's Wt.	Loss	Qty.	Signal Transistors Wt.	Loss	Qty.	Diodes Wt.	Loss	Qty.	XFMRS, Chokes Wt.	Loss	Qty.	Resistors Wt.	Loss	Qty.	Capacitors Wt.	Loss	Qty.	Miscell. Wt.	Loss	Qty.
Input Filter	1										1.0	20.0	1				0.5	2.0	1			
Logic DC Reg.	1				3			5			.02		1			15			5	Pwr. Xstr .05	2.0	1
Start Ckt.	1				3			3			.04		2			4			3			
Master Osc. Pulse Shaper	1				4			4			.04		2			10			4			
3Ø Flip-Flop	2				12			18								54			30			
Variable Delay	1				8			14			.3		10			29			15			
Drivers	6				24			48			.5		18	.5	72	64			36	Shockley Diodes 0.3	3	12
Output Stage	6	9.0	3600	36				2.4	672	12	21.0	858	12				12.0	120	6	0.3 Power Xstr.	3	12
Output Filter	3										7.5	240	6				3.3	27	6			
V & I Sense	1				4			14			.5	1	6			15			1			
TOTAL		9.0	3600	36	58			2.4	672	118	30.9	1099	58	.5	72	191	15.8	149	107	.65	8	15

	Weight	Loss	Parts Count
Totals of items listed above	59.25 lbs.	5600 watts	583 components
Allowance for weights & losses not itemized above.	3. lbs.	40 watts	---
TOTAL	62 1/4 lbs.	5640 watts	583 components

$$N = \frac{10000}{10000 + 5640} = 64\%$$

TABULATION OF WEIGHTS, LOSSES, AND PARTS COUNT FOR SCR 10 KW 3200~ INVERTER

TABLE 4-2

	No. Per Unit	Power Transistors Wt.	Loss	Qty.	Signal Transistors Wt.	Loss	Qty.	Diodes Wt.	Loss	Qty.	Transformers Chokes Wt.	Loss	Qty.	Resistors Wt.	Loss	Qty.	Capacitors Wt.	Loss	Qty.	Miscellaneous Wt.	Loss	Qty.
Input Filter	1										0.5	10	1				0.5	2.0	1			
Logic DC Reg.	1	.05	6	1	3			5			.02		1			15			5			
Start Ckt.	1				3			3			.04		2			4			3			
Master Osc. Pulse Shaper	1				4			4			.04		2			10			4			
6Ø Flip-Flop	2				24			36								108			60			
Variable Delay	1				14			26			.5		19			53			29			
Drivers	12	0.5	6	24				24			.7	24	24	.5	72	24			24	Shockley Diodes 0.5	6	24
Output Stage	12	4.4	2260	96				2.4	505	216	29.4	1330	192							.7	48	96
Output Filter	3										3.3	80	6				1.2	10.5	6	Fuses		
V & I Sense	1				4			14			.5	1	6			15			1			
TOTAL		4.95	2272	121	52			2.4	505	328	35.0	1455	253	.5	72	229	1.7	12.5	133	1.2	54	120

	Weight	Loss	Parts Count
Total of items listed above	45.75 lbs	4370 watts	1236 components
Allowance for weights & losses not itemized above.	4.25 lbs	60 watts	------
TOTAL	50.0 lbs	4430 watts	1236 components

$$N = \frac{10,000}{10,000 + 4430} = 70\%$$

TABULATION OF WEIGHTS, LOSSES, AND PARTS COUNT FOR TRANSISTORIZED 10 KW 3200 ~INVERTER

TABLE 4-3

Waveform Number *	Number of Steps Per Phase	Equal-Time, Equal-Height	Equal-Time, Unequal-Height	Unequal-Time, Equal-Height	Unequal-Time, Unequal-Height	Phase Voltage THD %	Line to Line Voltage THD %	Lowest Harmonic (phase)	Number of Inverters Per Phase	Number of Inverters for Three Phase	Number of XFMR Types	Suitable for Delta Connection	Significant Features
1	2	X				48.3	31.09	3	1	3	1	No	
2	4	X				48.3	60.9	3	2	6	1	No	45° Dwell Angle
3				X		31.1	31.1	5	2	3	1	Yes	30° Dwell Angle
4				X		29.1	35.9	3	2	6	1	No	Minimum THD 23.2° Dwell Angle,
5	6	X				31.1	31.1	5	3	3	1	Yes	Complement of No. 3
6					X	22.9	30.05	7	3	9	2	No	
7	8		X			23.1	26.0	7	4	12	2	No	Complement of 6
8				X		17.4	17.4	7	4	6	1	No	"Synchronous Switching" Method
9					X	18.3	13.08	7	4	12	2	No	
10					X	16.6	13.4	3	4	12	2	No	Minimum THD
11	10				X	15.2	15.2	11	5	6	2	Yes	
12	12		X			15.3	15.3	11	6	6	1	Yes	Complement of 11
13					X	11.5	10.6	3	6	18	3	No	Minimum THD
14	16				X	10	10	17	8	9	2	Yes	
15	18		X			10	10	17	9	9	2	Yes	Complement of 14

* Waveform Figures labeled "P" or "L-L" to define phase or line to line voltage.

TABLE OF MULTI-STEP WAVEFORM CHARACTERISTICS

TABLE 4-4

COPPER LOSS (WATTS)	CURRENT (AMPS)	REQ'D CORE LOSS (W/LB.)	400 ~ FLUX DENSITY (GAUSS)	400 ~ OUTPUT VOLTAGE	400 ~ OUTPUT POWER (WATTS)	400 ~ ACTUAL LOSSES (WATTS)	1000 ~ FLUX DENSITY (GAUSS)	1000 ~ OUTPUT VOLTAGE	1000 ~ OUTPUT POWER (WATTS)	1000 ~ ACTUAL LOSSES (WATTS)	3000 ~ FLUX DENSITY (GAUSS)	3000 ~ OUTPUT VOLTAGE	3000 ~ OUTPUT POWER (WATTS)	3000 ~ ACTUAL LOSSES (WATTS)	6000 ~ FLUX DENSITY (GAUSS)	6000 ~ OUTPUT VOLTAGE	6000 ~ OUTPUT POWER (WATTS)	6000 ~ ACTUAL LOSSES (WATTS)	10,000 ~ FLUX DENSITY (GAUSS)	10,000 ~ OUTPUT VOLTAGE	10,000 ~ OUTPUT POWER (WATTS)	10,000 ~ ACTUAL LOSSES (WATTS)	
			-1-				-2-				-3-				-4-				-5-				
50	14.7	52	7000 ①	27	397	50.3	7000 ②	67.5	992	50.77	7000 ③	263	2980	53.1	7000 ④	405	5950	57.5	7000 ⑤	675	9920	64.1	SQUARE PERMALLOY 80
30	11.4	32	" ⑥	"	308	30.3	" ⑦	"	770	26.77	" ⑧	"	2320	33.1	" ⑨	"	4620	37.5	" ⑩	"	7700	44.1	
20	9.3	21.3	" ⑧	"	251	20.3	" ⑧	"	627	20.77	" ⑨	"	1890	23.1	" ⑩	"	3760	27.5	" ⑪	"	6270	34.1	
10	6.6	10.6	" ⑨	"	178	10.3	" ⑨	"	445	10.77	" ⑩	"	1340	13.1	" ⑪	"	2670	17.5	6300	608	4020	20	
5	4.65	5.2	" ⑩	"	125.5	5.3	" ⑩	"	314	5.77	" ⑪	"	945	8.1	5500	318	1480	10	4000	386	1790	10	
3	3.61	3.2	" ⑪	"	97.5	3.3	" ⑪	"	244	3.77	6600	197	772	6	4200	243	878	6	3000	290	1050	6	
2	2.94	2.13	" ⑪	"	79.4	2.3	" ⑪	"	198	2.77	5500	159	465	4	3300	191	559	4	2400	232	679	4	
1	2.09	1.06	" ⑪	"	56.5	1.3	" ⑪	"	141	1.77	3800	110	230	2	2250	130	772	2	1550	149.5	312	2	
0.5	1.47	0.52	" ⑪	"	39.7	0.8	5500	53	77.9	1.0	2600	75.3	110.8	1	1500	86.6	127.2	1	1050	101	148.5	1	
0.3	1.14	0.32	"	"	30.8	0.6	4200	40.5	46.2	0.6	2000	57.9	66	0.6	1150	66.5	76	0.6	770	74.3	84.8	0.6	
			-6-				-7-				-8-				-9-				-10-				ORTHONOL
50	14.7	52	14K ①	54	794	51.2	14K ①	135	1980	55.2	14K ①	385	5950	76.4	12K	694	10,200	100	6500	627	9200	100	
30	11.4	32	" ②	"	615	31.2	" ⑥	"	1540	35.2	" ①	"	4620	56.4	7500	424	4940	60	4100	396	4420	60	
20	9.3	21.3	" ③	"	502	21.2	" ⑦	"	1255	25.2	11.5K	332	3080	40	5200	301	2800	40	2900	270	2510	40	
10	6.6	10.6	" ③	"	366	11.2	" ⑥	"	890	15.2	6500	188	1240	20	2700	156	1030	20	1400	135	890	20	
5	4.65	5.2	" ④	"	251	7.0	17.3K	120	559	10	3600	104	424	10	1400	81	376	10	700	67.5	314	10	
3	3.61	3.2	" ⑤	"	195	5.0	9200	81	392.5	6	2400	69.3	251	6	900	52	188	6	440	425	153.5	6	
2	2.94	2.13	"	"	159	4.0	6400	61.7	281	4	1800	52	153	4	640	37	109	4	300	29	88.4	4	
1	2.09	1.06	8500	32.8	58.5	2.0	3700	35.7	74.6	2	1008	29.95	60.5	2	330	19.1	39.9	2	—	—	—	—	
0.5	1.47	0.52	5000	19.3	28.4	1.0	2700	21.2	31.15	1	550	15.9	23.35	1	—	—	—	—	—	—	—	—	
0.3	1.14	0.32	3500	13.5	15.9	0.6	1500	14.5	16.5	0.6	360	10.4	11.9	0.6	—	—	—	—	—	—	—	—	
			-11-				-12-				-13-												SUPERMENDUR
50	14.7	52	26K ①	77.2	1125	60	20K ①	193	2840	78	7500	275	4040	100	- NOTES -								
30	11.4	32	" ②	"	880	40	" ②	"	2200	58	6400	185	2110	60	ACTUAL CORE LOSS VALUES - WHERE THEY DIFFER FROM THE REQUIRED VALUES.								
20	9.3	21.3	" ③	"	718	30	15K	145	1550	40	4600	133	1238	40									
10	6.6	10.6	"	"	510	20	8600	82	548	20	2700	78	515	20	① 0.32 W/LB				⑥ 30 W/LB				
5	4.65	5.2	11.8K	48	2045	10	4900	47.3	270	10	1508	43.4	262	10	② 2.1 "				⑦ 3.3 "				
3	3.61	3.2	7900	30.5	110	6	3300	31.8	115	6	1040	30	108.5	6	③ 10.6 "				⑧ 28 "				
2	2.94	2.13	4960	18.5	46.5	4	2000	23.2	58.4	4	740	21.4	53.8	4	④ 0.82 "				⑨ 8 "				
1	2.09	1.06	3360	12.7	26.55	2	1400	13.5	28.7	2	440	12.7	26.5	2	⑤ 5.5 "				⑩ 15 "				
0.5	1.47	0.52	1960	7.3	10.72	1	800	7.7	11.3	1	240	6.95	10.2	1									
0.3	1.14	0.32	1360	5	5.7	0.6	580	5.2	5.94	0.6	170	4.91	5.6	0.6									

TABLE OF TRANSFORMER DESIGNS

TABLE 4-5

PARTS APPLICATION DATA SHEET - RECTIFIERS, TRANSISTORS, ETC.

Component Designation 3200 cps - 10 KW Inverter

Table 4-II-1

Circuit Symbol No.	Type No. Mfg. or Mil.	Mfg.	Rating (PWR) or (CURR) Value	% Duty Cycle	T_A or T_C °C	T_A or T_C °C	Maximum Usage Power	Current	Voltage	% Duty Cycle	Operating Time t Hours	Mean Generic Failure Rate λ	De-Rating Factor K_A	Resultant MGFR λ'	Circuit Application	Schematic Diagram	Reliability Block No.
Q9	2N697	T1	2W .2A 0	50	25°C ↓ 150°C	60°	10 MW	10 MA	25	50	720 8750	.7	.03	.021	Phase Shift Input F-F	Fig. 4-87 Fig. 4-88	C-1 of Fig. 4-II-1
Q10	2N697	T1	2W .2A 0	50	25°C ↓ 150°C	60°	10 MW	10 MA	25	50		.7	.03	.021			
D7	1N485	Fair-child	.5W .125A .25W	50	25°C ↓ 150°C	60°	1 MW	1.5 MA	25	50		.2	.02	.004			
D8	1N485	Fair-child	.5W .125A .25W	50	25°C ↓ 150°C	60°	1 MW	1.5 MA	25	50		.2	.02	.004			

PARTS APPLICATION DATA SHEET - RESISTORS

Component Designation – 3200 - 10 KW Inverter

Table 4-II-2

Circuit Symbol No.	Type No. Mfg. or Mil	Mfg.	Res. Value Ohms	Tol. %	Rated Power Watts	Operating Power Watts	% of Operating Power	Maximum Ambient Temp. °C	Operating Time t Hours 720 / 8750	Mean Generic Failure λ	De-Rating Factor KA	Resultant MGFR λ′	Circuit Application	Schematic Diagram	Reliability Block No.
R16	GBT	IRC	2.2K	±5	1	.198	19.8%	40°C		.034	1.2	.049	Input F-F	Fig. 4-87	C-1
R17	GBT	IRC	2.2K	±5	1	.198	19.8%	40°C		.034	1.2	.049	Phase Shifter	Fig. 4-88	of Fig. 4-II-1
R18	GBT	IRC	15 K	±5	1	.03W	3%	40°C		.034	.8	.027			
R19	GBT	IRC	15 K	±5	1	.03W	3%	40°C		.034	.8	.027			
R20	GBT	IRC	22 K	±5	1/2	.0506MW	.01%	40°C		.06	.2	.012			
R21	GBT	IRC	22 K	±5	1/2	.0506MW	.01%	40°C		.06	.2	.012			
R22	GBT	IRC	22 K	±5	1	25 MW	2.5%	40°C		.034	.8	.027			
R23	GBT	IRC	22 K	±5	1	25 MW	2.5%	40°C		.034	.8	.027			

PARTS APPLICATION DATA SHEET - CAPACITORS

Component Designation - 3200 cps - 10 KW Inverter

Table 4-II-3

Circuit Symbol No.	Type No. Mfg. or Mil.	Mfg.	Cap. Value Mfd.	Tol. %	Rated Voltage	Operating Voltage	% of Operating Voltage	Maximum Ambient °C	Operating Time t Hours	Mean Generic Failure Rate λ	De-Rating Factor π_A	Resultant MGFR λ'	Circuit Application	Schematic Diagram	Reliability Block No.
C6	CM20-B	El Menco	100 uufd	±5	300	25	8.33	40°C	720 8750	.045	.1	.0045	Input F-F Phase Shifter	Fig. 4-87 Fig. 4-88	C-1 of Fig. 4-II-1
C7	CM20-B	El Menco	100 uufd	±5	300	25	8.33	↓	↓	.045	.1	.0045			
C4	CM20-B	El Menco	50 uufd	±5	300	25	8.33			.045	.1	.0045			
C5	CM20-B	El Menco	50 uufd	±5	300	25	8.33			.045	.1	.0045			

PARTS APPLICATION DATA SHEET - RECTIFIERS, TRANSISTORS, ETC.

Component Designation = 400 cps - 10KW PWM Inverter

TABLE 4-VI-1

Circuit Symbol No.	Type No. Mfg. or Mil.	Mfg.	Rating (PWR) or (CURR) Value	% Duty Cycle	T_A or T_C °C	T_A or T_C °C	Power	Maximum Usage % of Operating Power	% Duty Cycle	Operating Time t Hours	Mean Generic Failure Rate λ	De-Rating Factor KA	Resultant MGFR λ'	Circuit Application	Schematic Diagram	Reliability Block No.
Q25	2N2218	Ti	3W .8A	100	25° ↓ 150°	60°	15 MW	.5 %	100	720 / 8750	.5	.007	.0035	Sawtooth Sweep Wave Generator 10 KC	Fig. 4-126 Fig. 4-127	F of Figure 4-VI-1
Q26	2N2904A	MOT	.8W .8A	1			25 MW	3.13%	1		.5	.03	.015			
Q27	2N2218	Ti	3W .8A	100			48 MW	1.6 %	100		.5	.016	.008			
Q28	2N2218	Ti	3W .8A	100			20 MW	.66%	100		.5	.009	.0045			
Q29	2N2218	Ti	5W .8A	100			10 MW	.33%	100		.5	.007	.0035			
Q30	2N2218	Ti	3W .8A	100			10 MW	.33%	100		.5	.007	.0035			
Q31	2N2218	Ti	3W .8A	100			225 MW	7.5 %	100		.5	.04	.02			
D25	IN751	Ti	.4W	100			23 MW	5.75%	100		.15	.05	.0075			
D26	IN659	Ti	.25W .32A	1			3 MW	1.2 %	1		.2	.035	.007			
D27	IN659	Ti	.25W .32A	100			5 MW	2 %	100		.2	.04	.008			
D28	IN751	Ti	.4W	100			45MW	11.3%	100		.15	.11	.0165			

PARTS APPLICATION DATA SHEET - CAPACITORS

Component Designation 400 cps - 10KW P. W. M. Inverter

TABLE 4-VI-2

Circuit Symbol No.	Type No. Mfg. or Mil	Mfg.	Cap. Value Mfd.	Tol. %	Rated Voltage	Operating Voltage	% of Operating Voltage	Maximum Ambient Temp. °C	Operating Time t Hours	Mean Generic Failure Rate λ	De-Rating Factor KA	Resultant MGFR λ'	Circuit Application	Schematic Diagram	Reliability Block No
C36	617G	Goodall	.022	±10	100	10	10	40°C	720 / 8750	.083	.2	.0166	Sawtooth Sweep Generator 10KC	Fig. 4-126 Fig. 4-127	F of Figure 4-VI-1
C37	CM-20B	El-Menco	.001	±10	100	10	10	↓	↓	.045	.1	.0045			
C38	CM-20B	El-Menco	.001	±10	100	10	10	↓	↓	.045	.1	.0045			

PARTS APPLICATION DATA SHEET - RESISTORS

Component Designation 400 cps - 10KW P. W. M. Inverter

TABLE 4-VI-3

Circuit Symbol No.	Type No. Mfg. or Mil.	Mfg.	Res. Value Ohms	Tol. %	Rated Power Watts	Operating Power Watts	% of Operating Power	Maximum Ambient Temp. °C	Operating Time t Hours	Mean Generic Failure Rate λ	De-Rating Factor K_A	Resultant MGFR λ'	Circuit Application	Schematic Diagram	Reliability Block No.
R76	GBT	IRC	2.2K	±5	1/2W	4.5 MW	8.9	40°C	720 / 8750	.06	1	.06	Sawtooth Sweep Wave Generator 10KC	Figure 4-126 Figure 4-127	F of Figure 4-VI-1
R77	Bourns	224L	5K pot	±5	1 W	25 MW	2.5	↓	↓	1.4	.07	.098	↓	↓	↓
R78	GBT	IRC	4.7K	±5	1/2W	48 MW	9.6	↓	↓	.06	1	.06	↓	↓	↓
R79	GBT	IRC	47K	±5	1/2W	2 MW	.4	↓	↓	.06	.5	.03	↓	↓	↓
R80	GBT	IRC	4.7K	±5	1/2W	20 MW	4.	↓	↓	.06	.95	.057	↓	↓	↓
R81	GBT	IRC	10K	±5	1/2W	1 MW	.2	↓	↓	.06	.45	.027	↓	↓	↓
R82	GBT	IRC	47K	±5	1/2W	.5 MW	.1	↓	↓	.06	.4	.024	↓	↓	↓
R83	GBT	IRC	4.7K	±5	1/2W	20 MW	4.	↓	↓	.06	.95	.057	↓	↓	↓
R84	GBT	IRC	4.7K	±5	1/2W	20 MW	4.	↓	↓	.06	.95	.057	↓	↓	↓
R85	GBT	IRC	2.2K	±5	1/2W	44.5 MW	8.9	↓	↓	.06	1	.06	↓	↓	↓
R86	GBT	IRC	1K	±5	1 W	.225 Watt	22.5	↓	↓	.034	1.4	.0475	↓	↓	↓

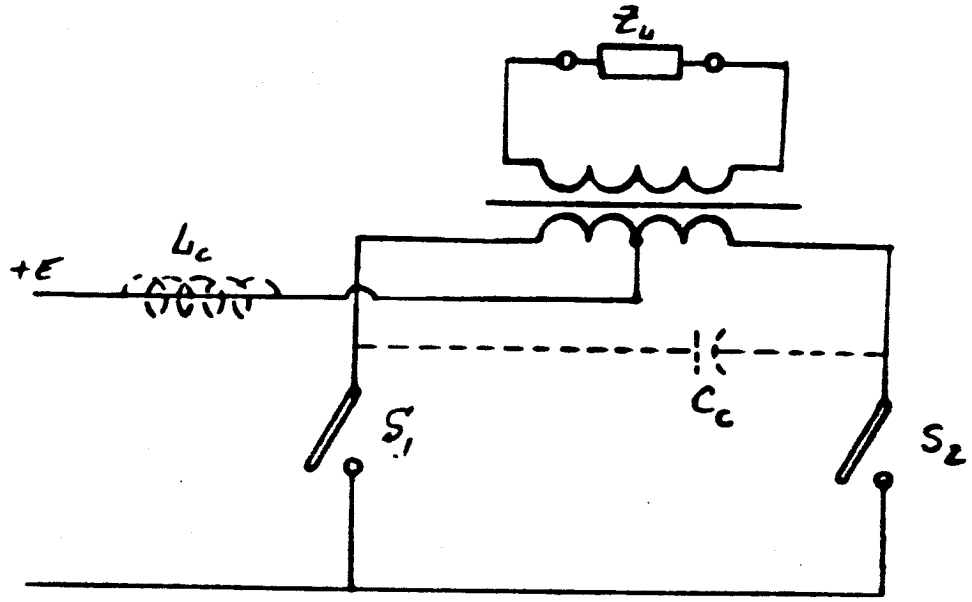
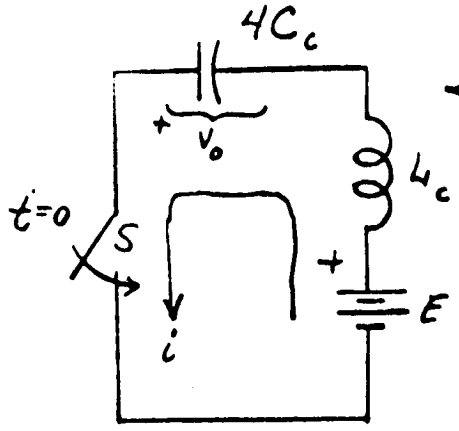
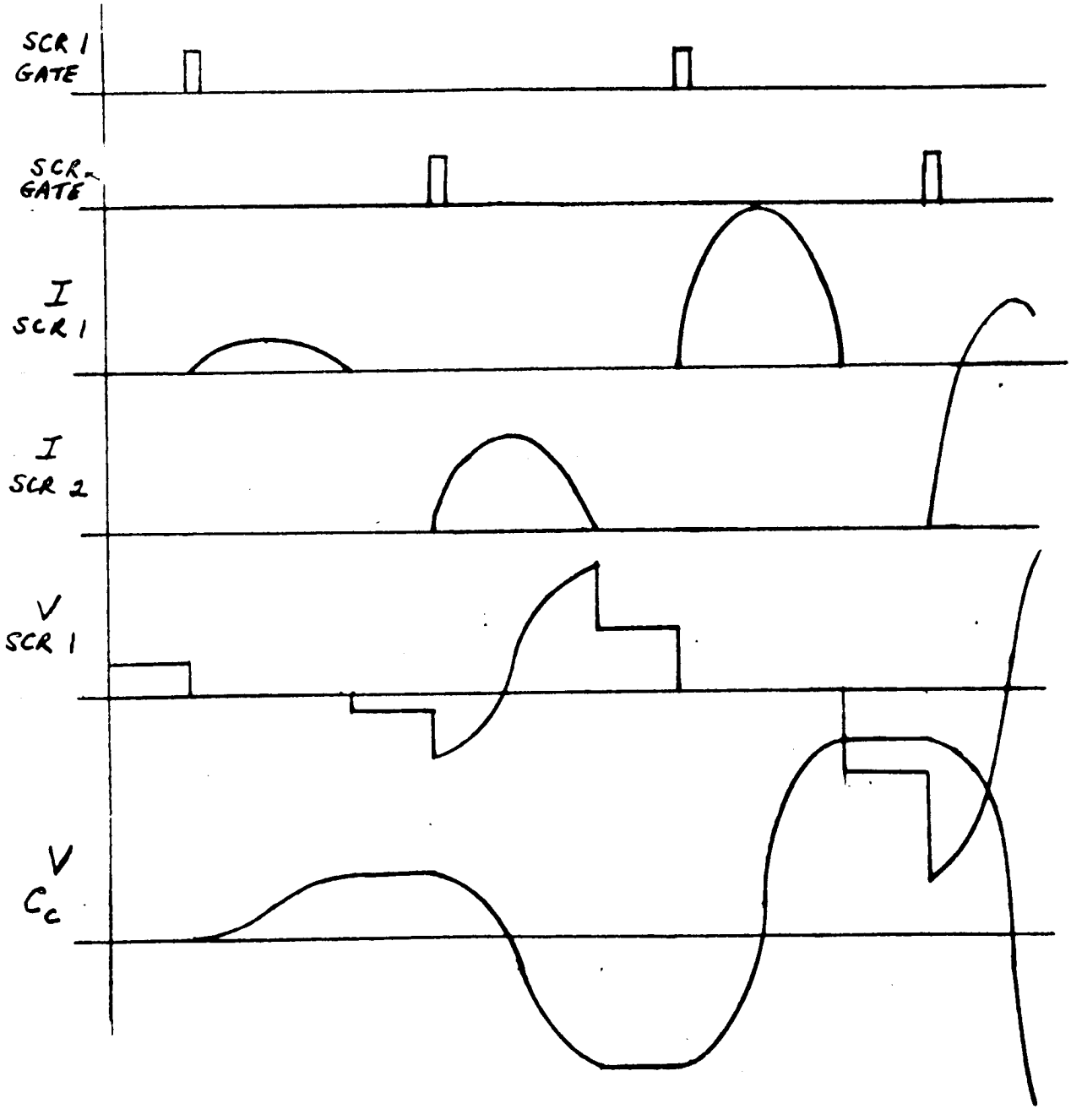


FIG. 4-1 PARALLEL INVERTER



← FIGURE 4-2 EQUIVALENT CIRCUIT OF FIG. 4-1 FOR S_1 BEING CLOSED

FIGURE 4-3 WAVEFORMS FOR STARTING OF FIG. 4-1 WITH NO LOAD.



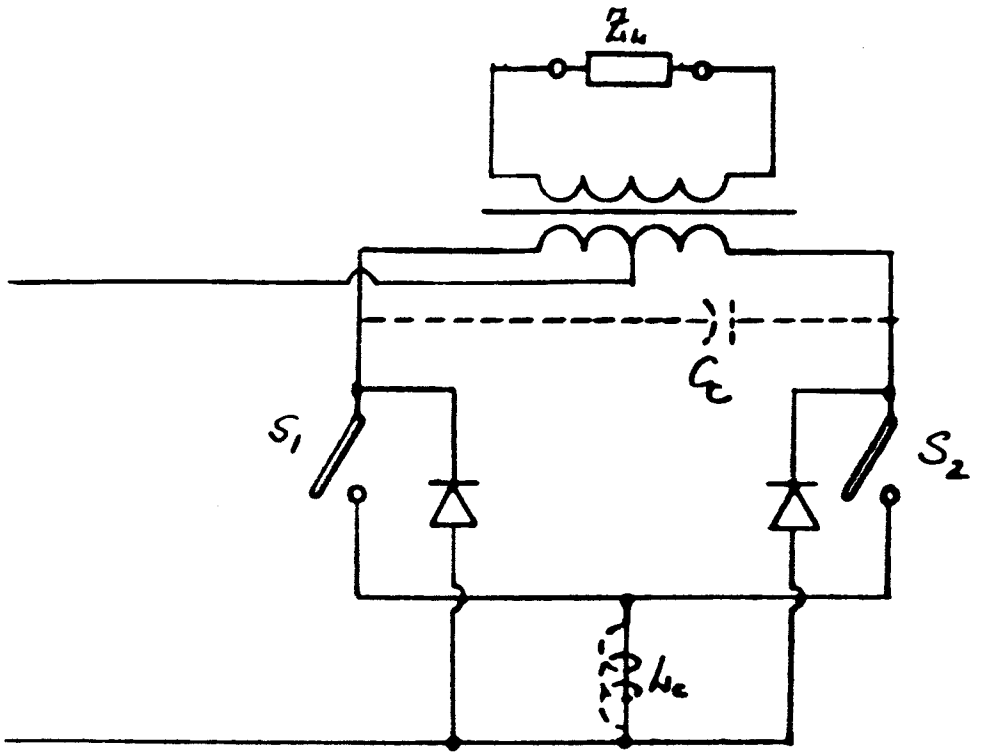


FIG. 4-4 PARALLEL INVERTER WITH REACTIVE DIODES

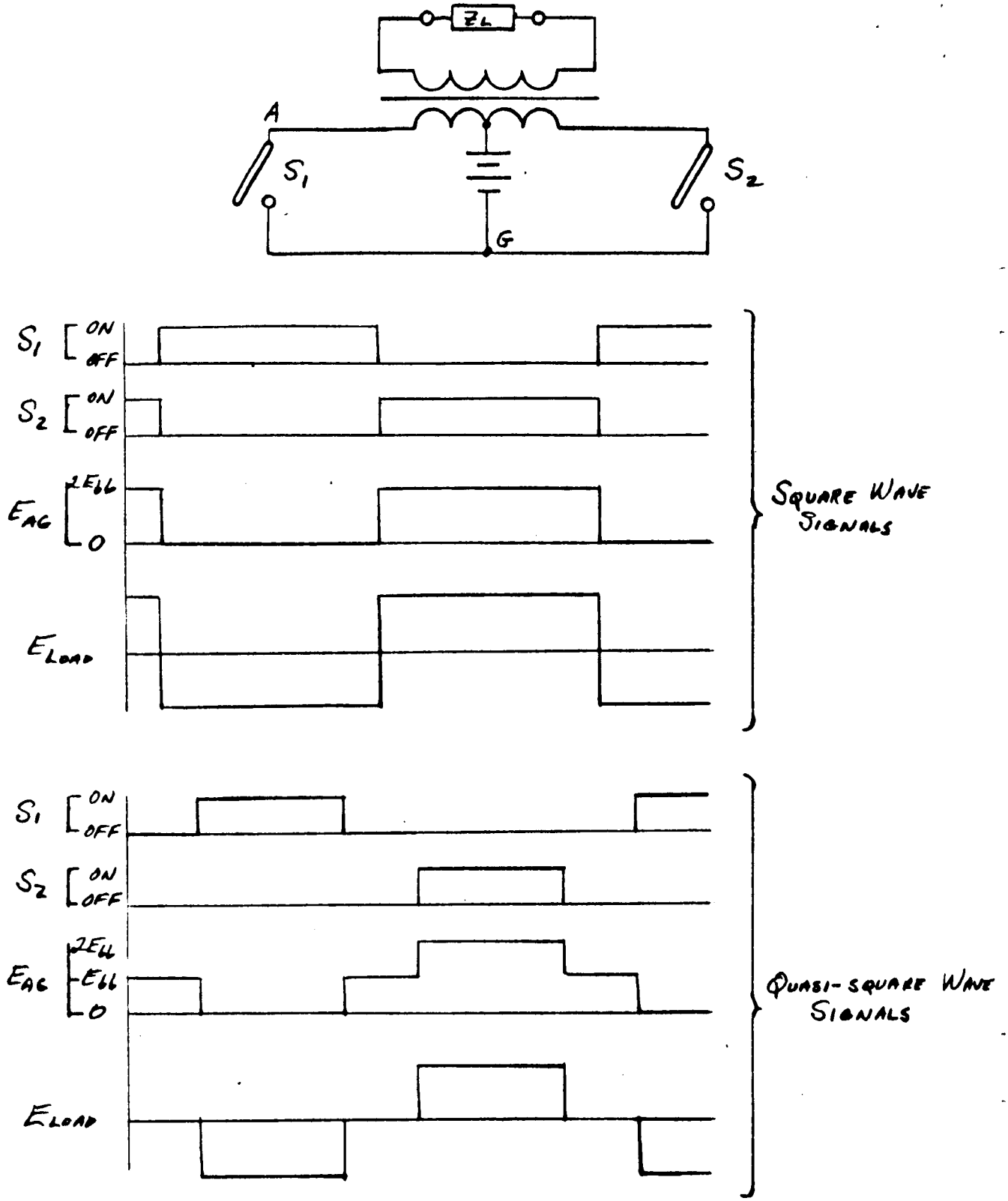
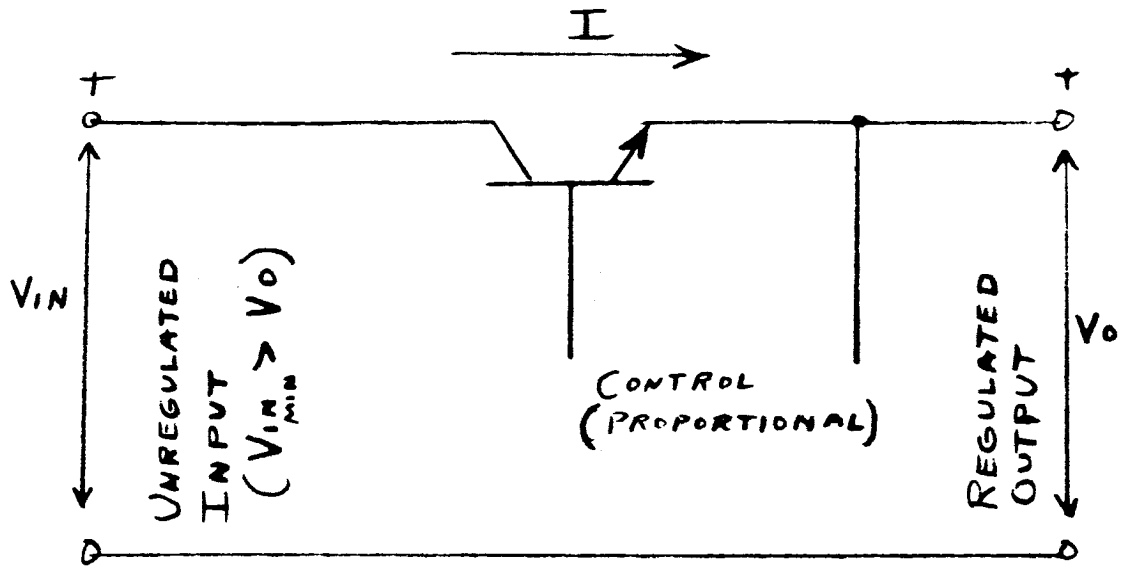
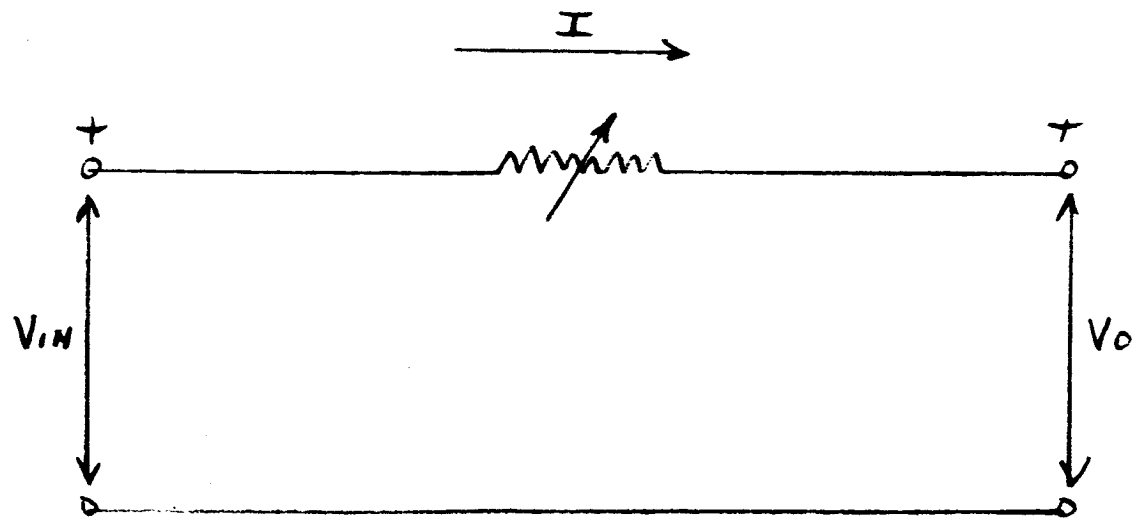


FIG. 4-5 PARALLEL INVERTER WAVEFORMS



SERIES LINEAR REGULATOR

FIG. 4-6



EQUIVALENT CIRCUIT OF FIG. 4-6

FIG. 4-7

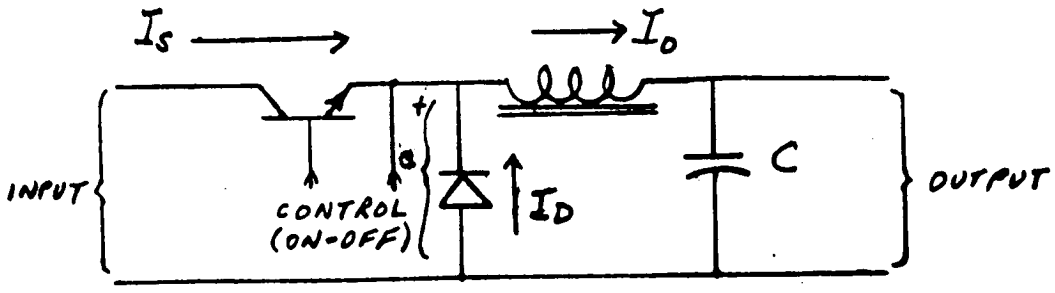


FIGURE 4-8 SERIES SWITCHING REGULATOR

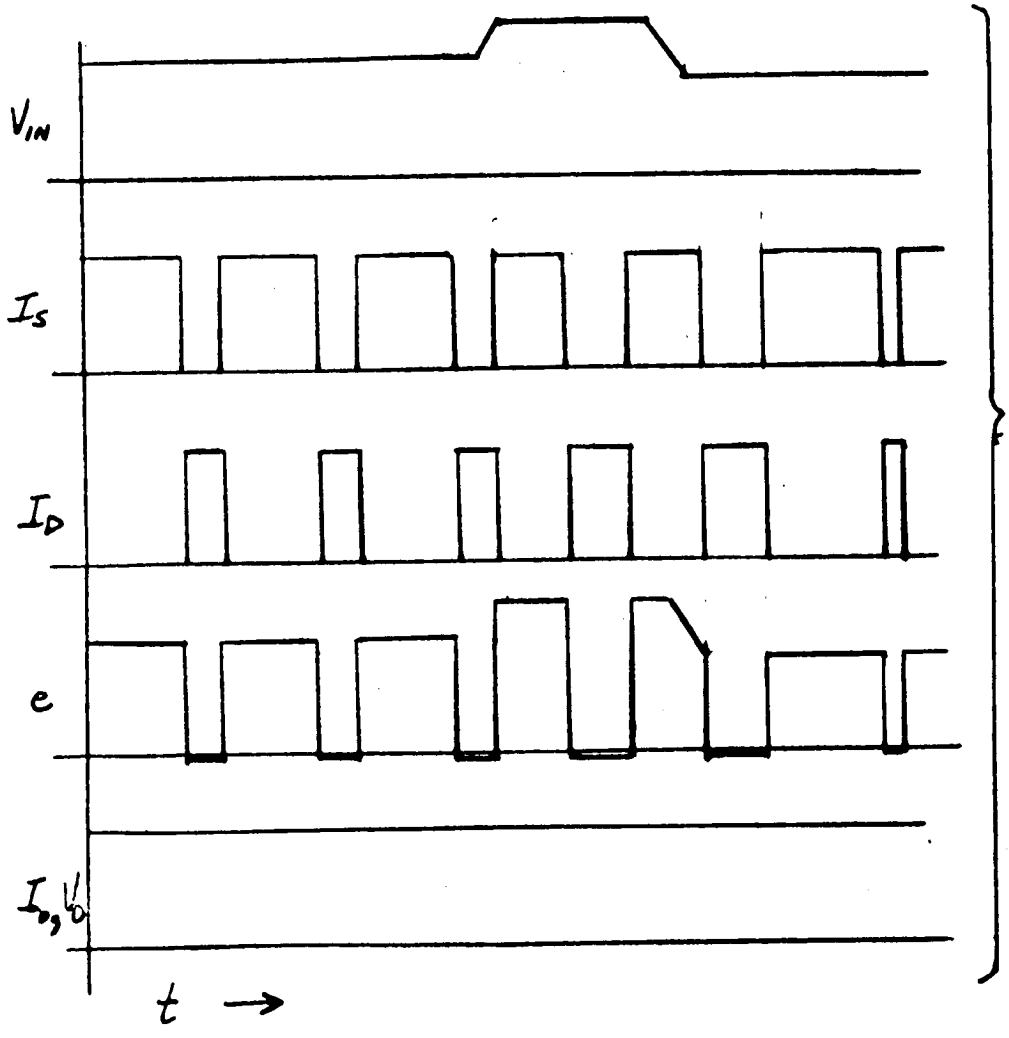


FIG 4-9
WAVEFORMS
FOR 4-8

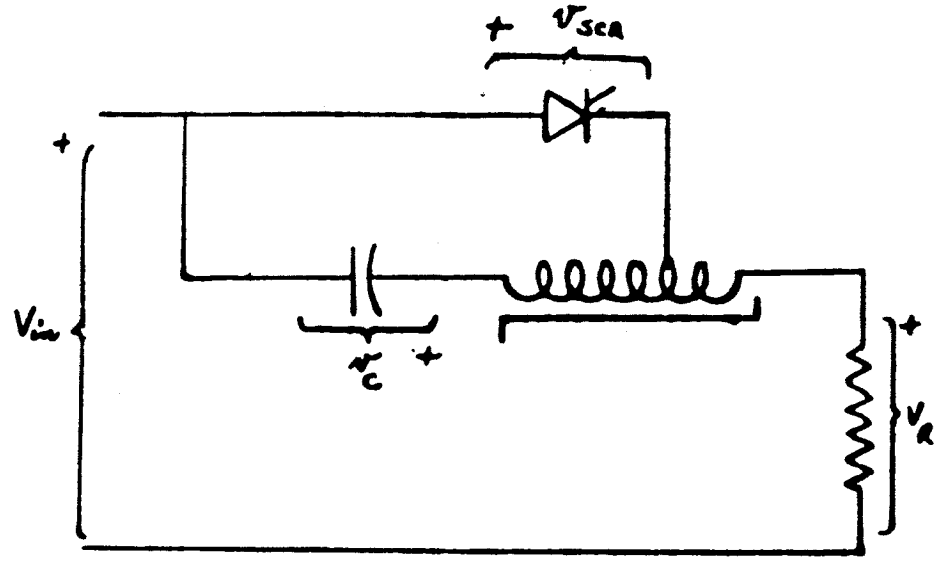


FIG 4-10 MORGAN CHOPPER CIRCUIT

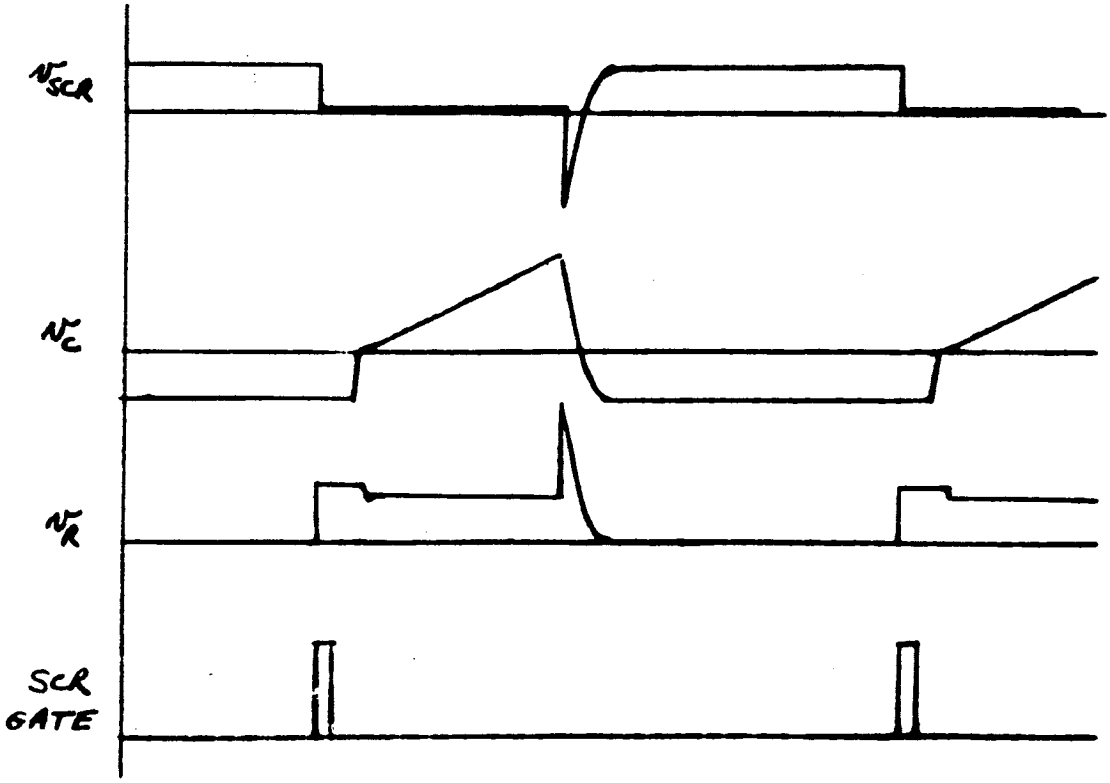


FIG. 4-11 WAVEFORMS FOR FIG 4-10

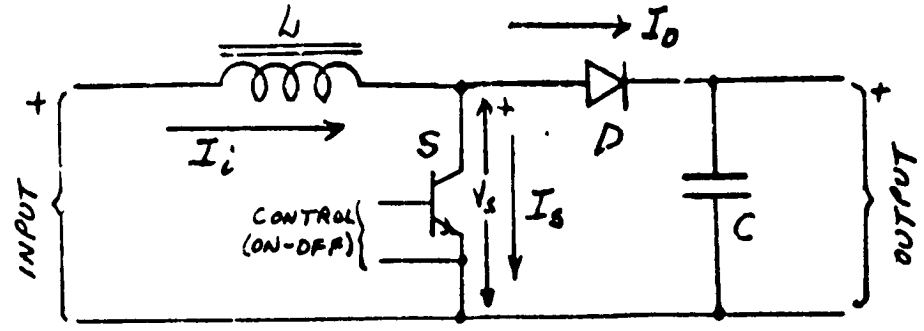
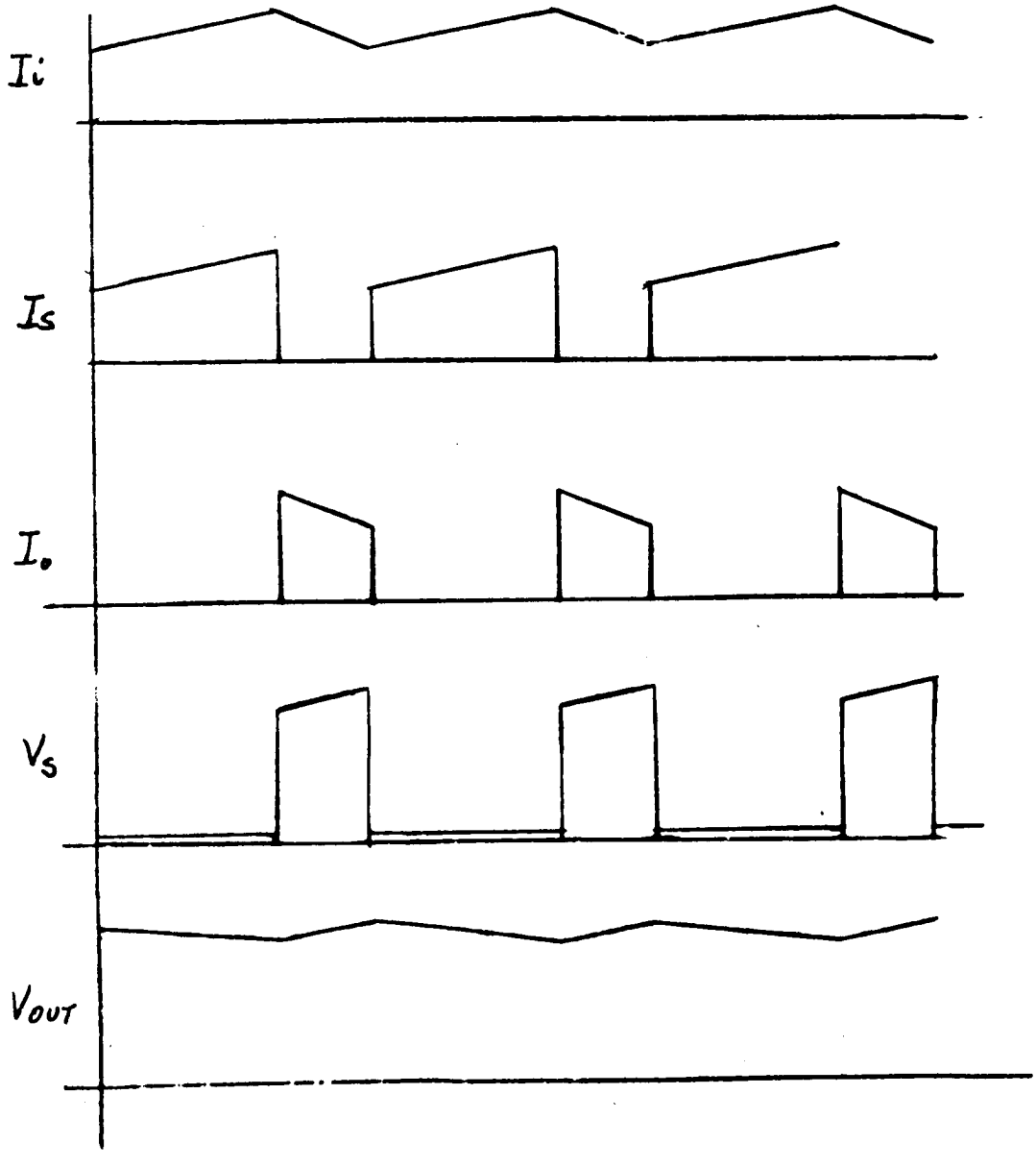
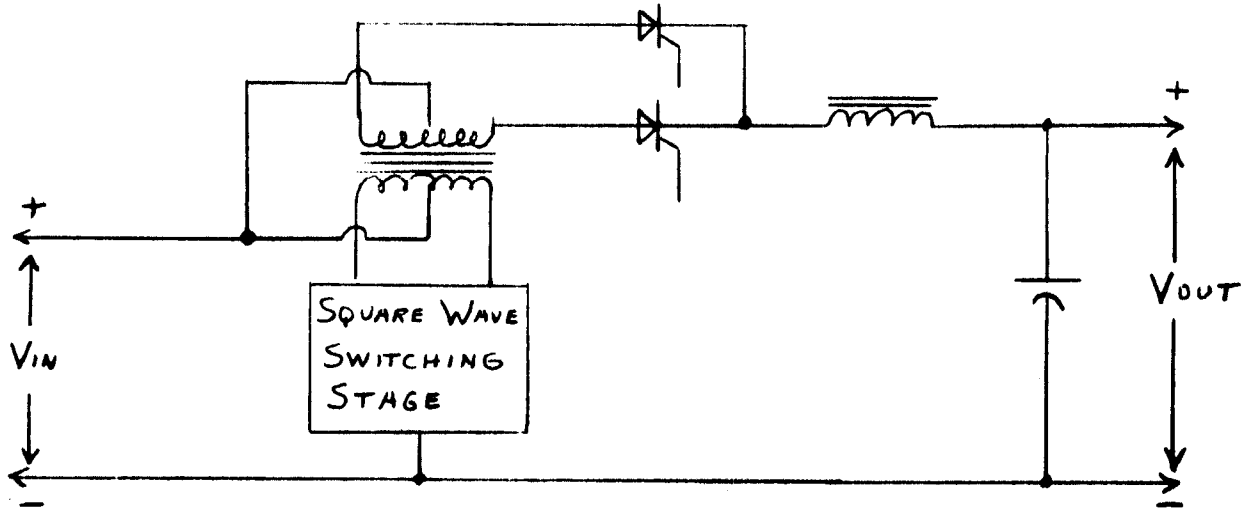


FIG. 4-12 BEDFORD STEP-UP CIRCUIT

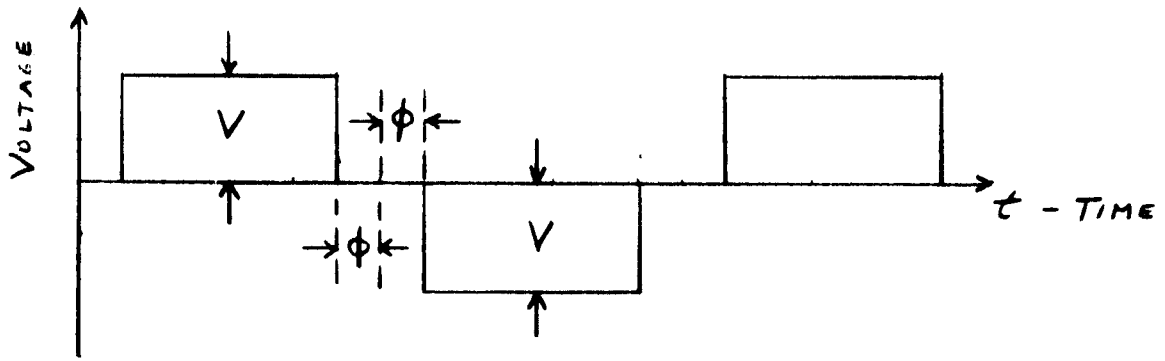
FIG 4-13 WAVEFORMS FOR CIRCUIT OF FIG. 4-12





BUCK - BOOST D.C. REGULATOR

FIGURE 4-14



QUASI-SQUARE WAVE

FIGURE 4-15

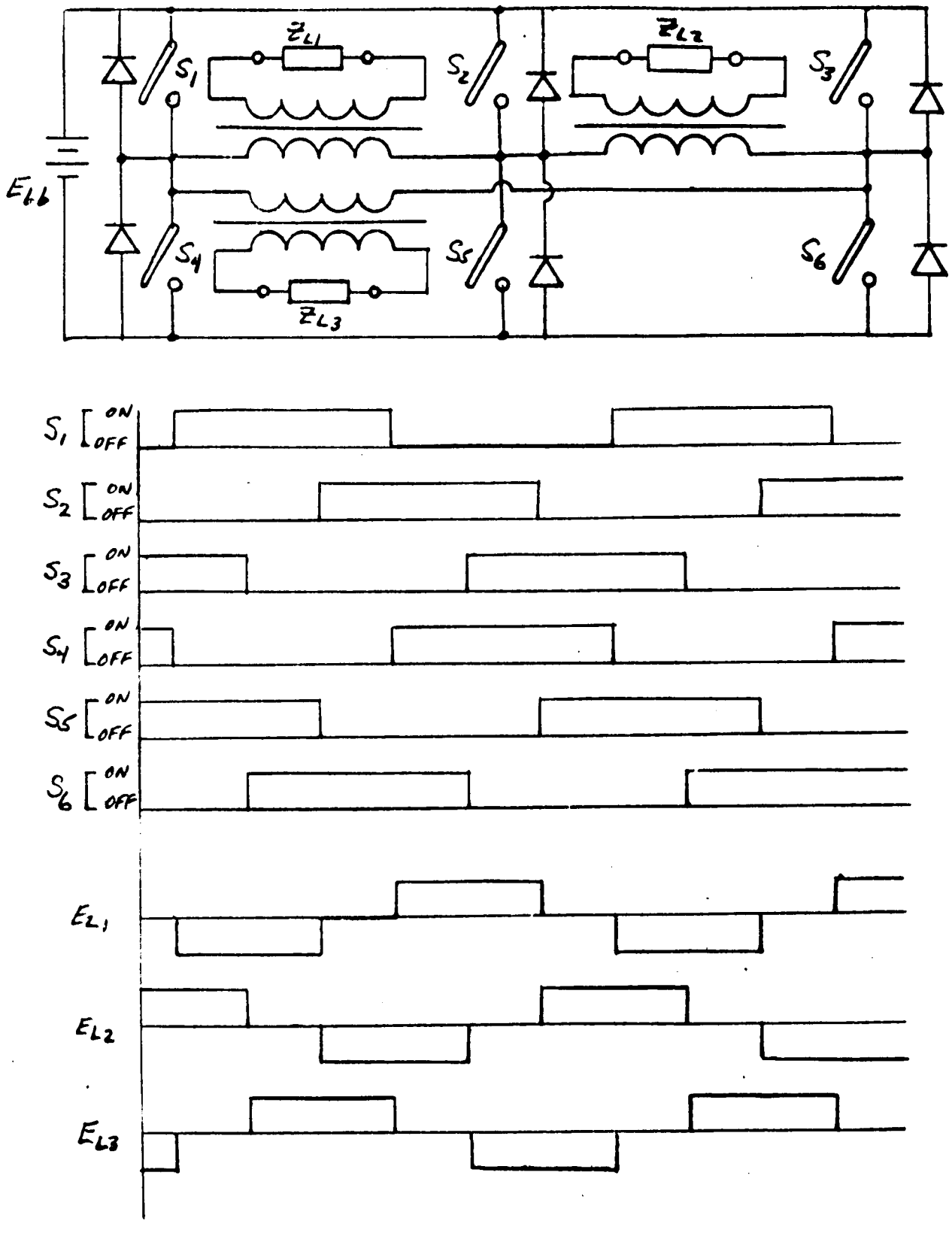


FIG. 4-16 THREE PHASE BRIDGE INVERTER

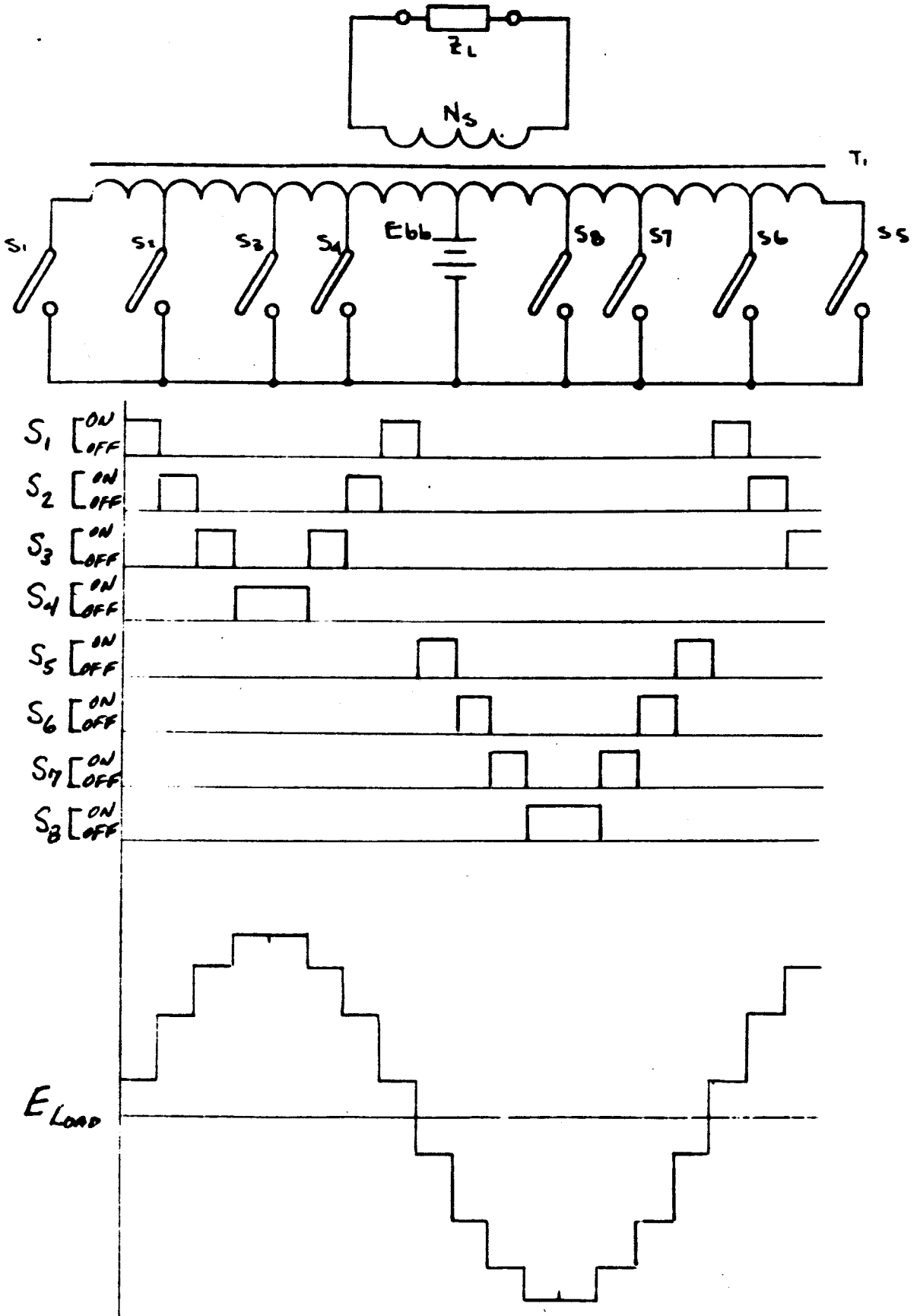


FIG. 4-17 STEPPED OUTPUT WAVEFORMS

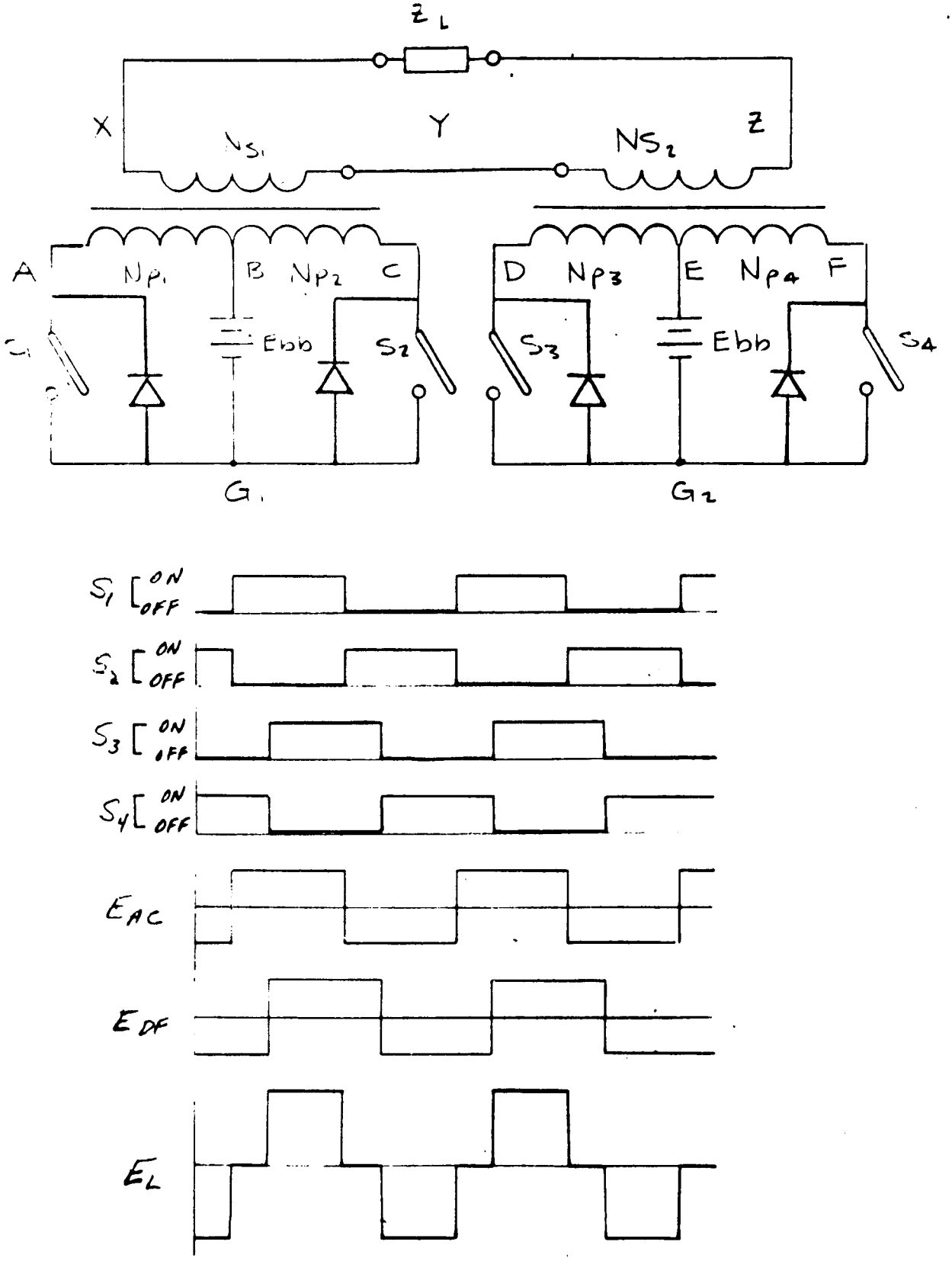


FIG. 4-18 DOUBLE SQUARE WAVE QUASI-SQUARE INVERTER

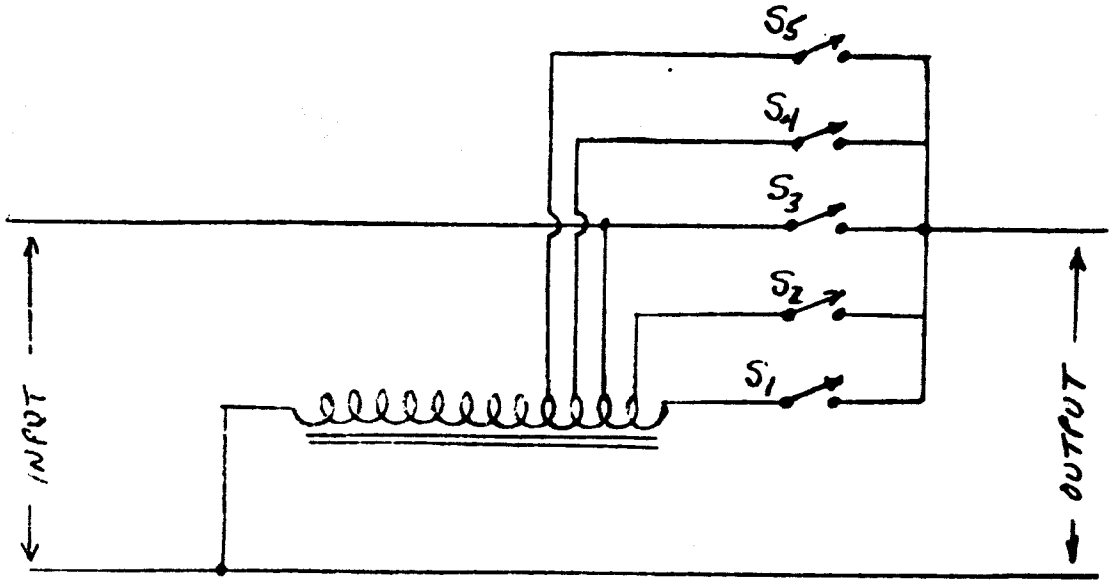


FIG. 4-19 STATIC TAP CHANGING CIRCUIT

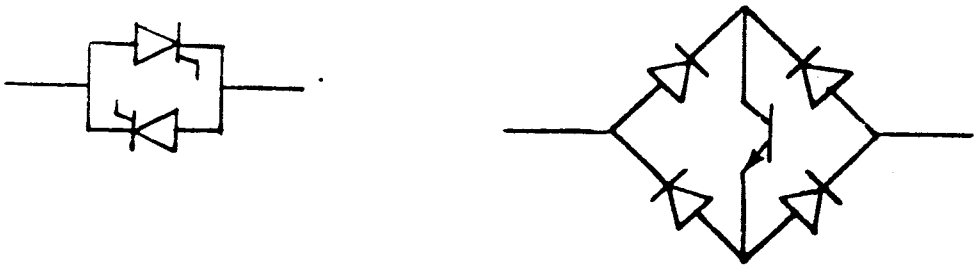


FIG 4-20 TECHNIQUES FOR REALIZATION OF STATIC SWITCHES FOR A-C USE

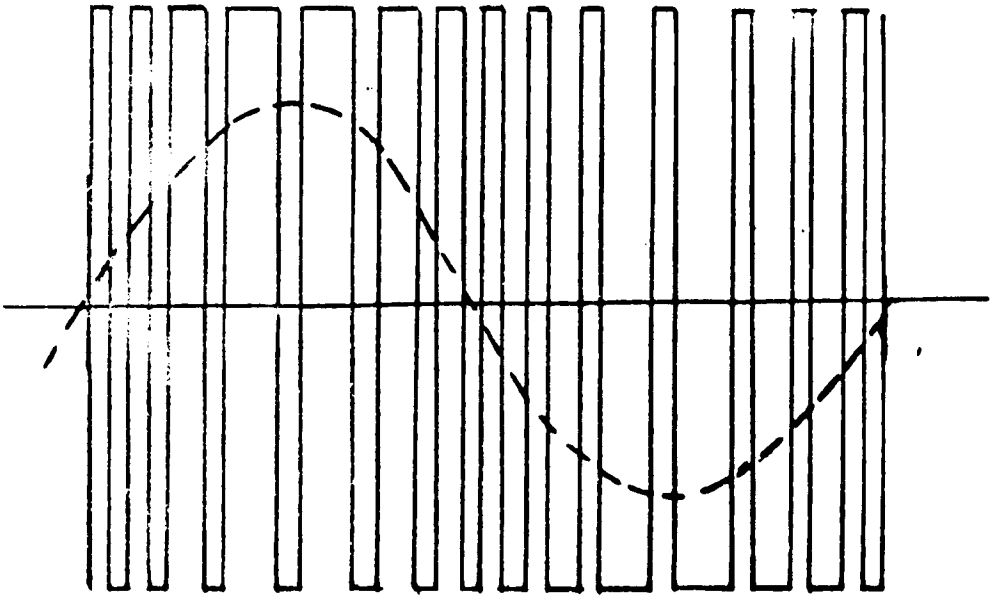
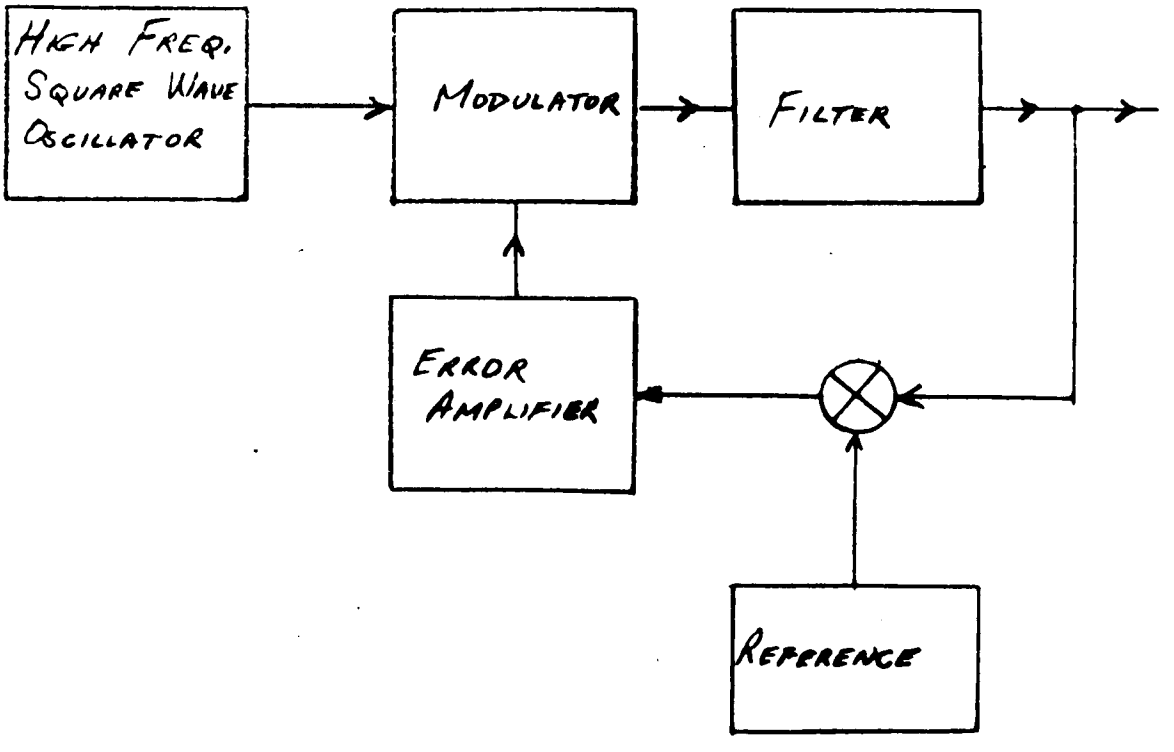


FIG. 4-21 PULSE WIDTH MODULATION WAVEFORM AND ITS FUNDAMENTAL COMPONENT.

FIG. 4-22 PULSE WIDTH MODULATION INVERTER - BLOCK DIAGRAM



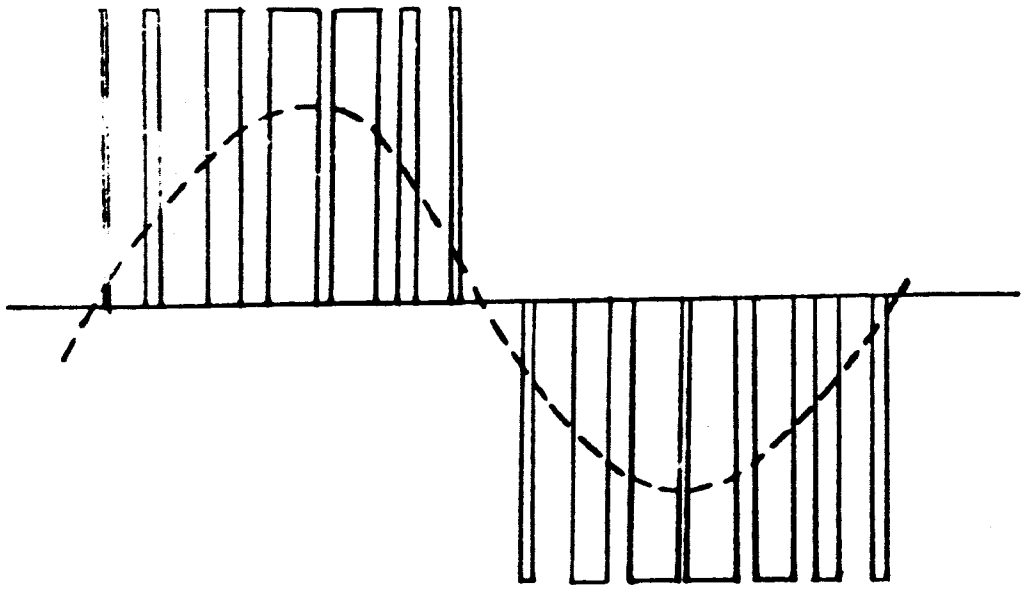


FIG. 4-23 MODIFIED PULSE WIDTH MODULATION WAVEFORM WITH REDUCED HARMONIC CONTENT, ALONG WITH ITS FUNDAMENTAL COMPONENT.

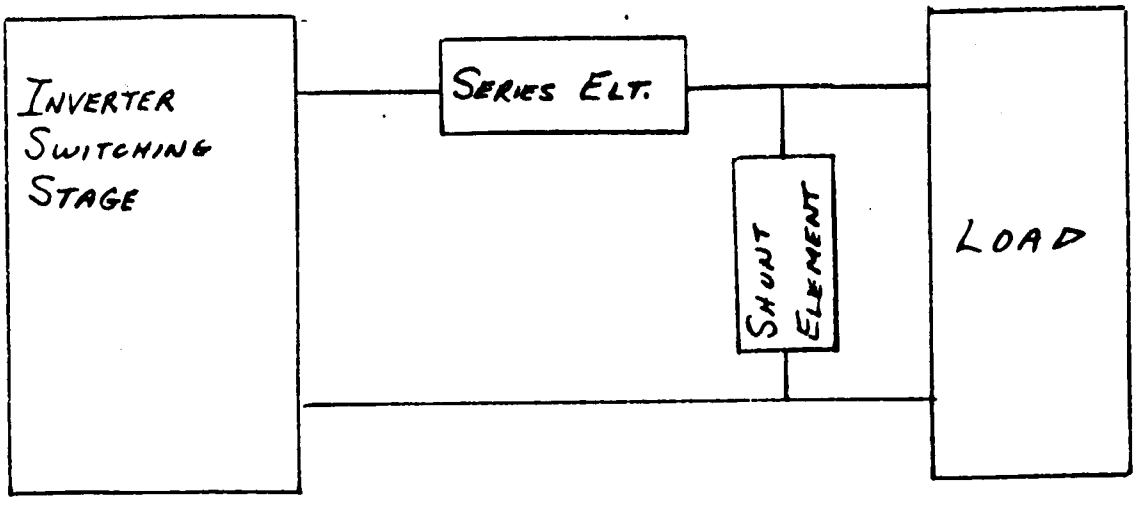


FIG. 4-24 PASSIVE BANDPASS FILTER
BLOCK DIAGRAM

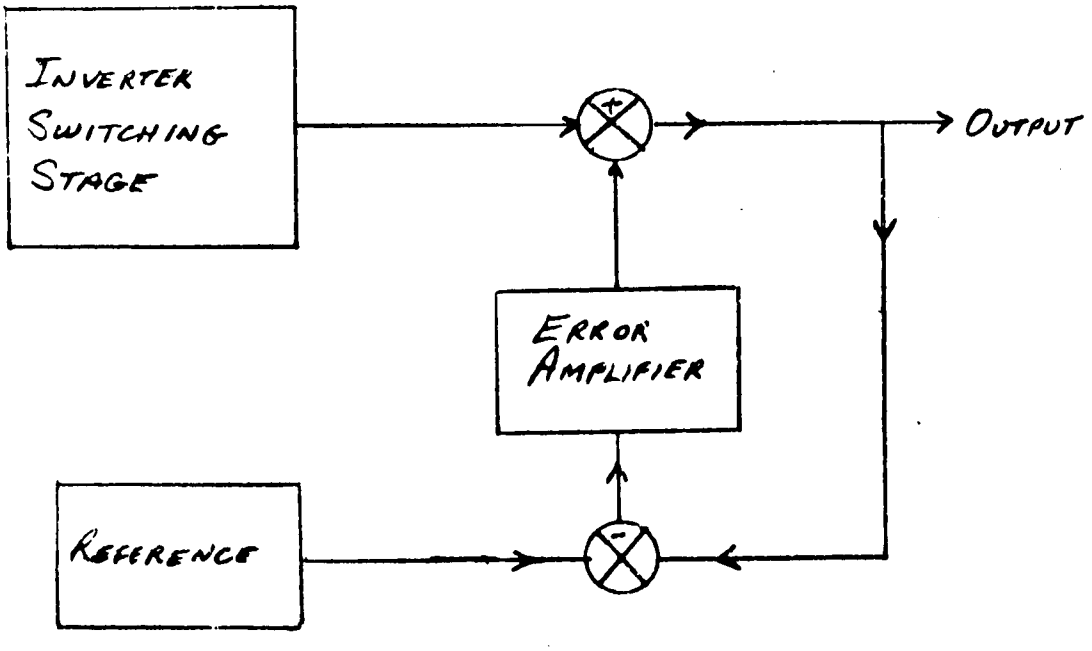


FIG. 4-25 ACTIVE FILTER
BLOCK DIAGRAM

TWO STEP - EQUAL TIME PHASE VOLTAGE

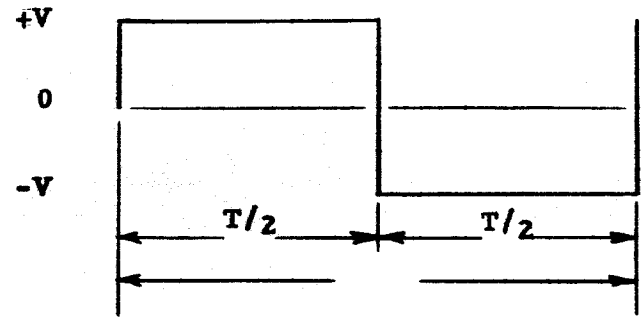


Figure 4-26

Average Value of Waveform = 1.0V
RMS Value of Waveform = 1.0V
RMS Value of the Fundamental = $(1/\sqrt{2} \times \frac{4V}{\pi} = 0.9V$

Total Harmonic Distortion = 48.343%

Harmonic Number	Percent of Fundamental	H. N.	P. of F.
1	100.0	41	2.44
3	33.3	43	2.33
5	20.0	45	2.22
7	14.28	47	2.13
9	11.11	49	2.04
11	9.09	51	1.96
13	7.69	(2N-1)	$\frac{1}{(2N-1)} \times 100$
15	6.67		
17	5.88		
19	5.26		
21	4.76		
23	4.35		
25	4.00		
27	3.70		
29	3.45		
31	3.23		
33	3.03		
35	2.86		
37	2.70		
39	2.56		

Waveform 1 P

FOUR STEP - EQUAL TIME

PHASE VOLTAGE

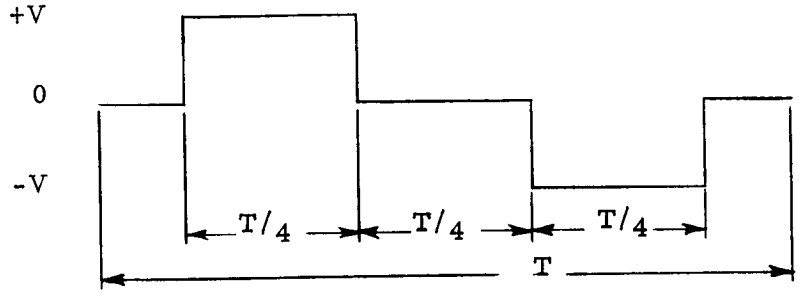


Figure 4-27

Average Value of Waveform = 1/2V
RMS Value of Waveform = $(1/\sqrt{2})$V = 0.707V
RMS Value of Fundamental = $(2/\pi)$V = 0.636V
Total Harmonic Distortion = 48.343%

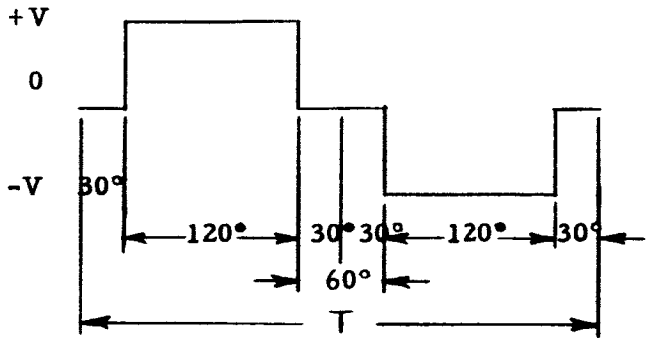
Waveform 2 P

FOUR STEP - UNEQUAL TIME

TYPE A

PHASE VOLTAGE

Figure 4-28



Average Value of Waveform = $(2/3)V$

RMS Value of Waveform = $(\sqrt{2/3})V = 0.8165V$

RMS Value of Fundamental = $\frac{(2\sqrt{3})}{\pi\sqrt{2}} V = 0.5513V$

Total Harmonic Content = 31.09%

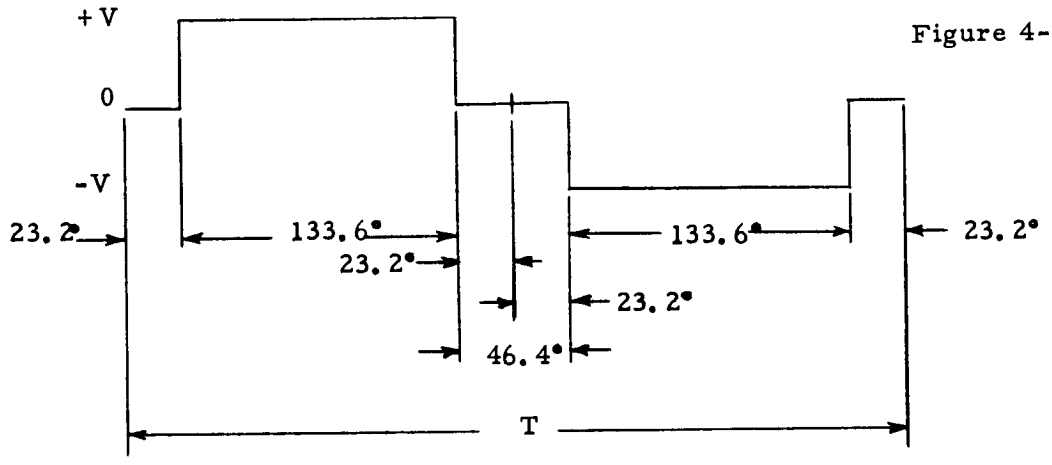
Lowest harmonic is the fifth and all multiples of the third harmonic are zero.

Waveform 3 P

FOUR STEP-UNEQUAL TIME
TYPE B

PHASE VOLTAGE

Figure 4-29



Average Value of Waveform = 0.7422V
RMS Value of Waveform = 0.8615V
RMS Value of Fundamental = 0.8276V
Total Harmonic Distortion = 29.1%

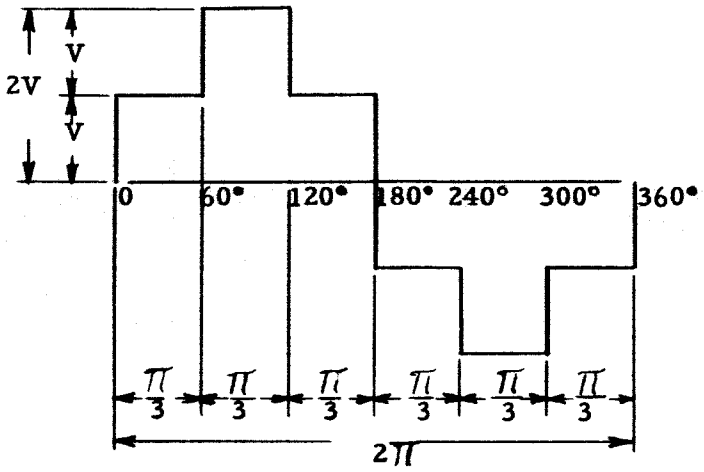
Dwell angle selected for minimum total harmonic distortion.

Waveform 4 P

SIX STEP-EQUAL TIME-EQUAL HEIGHT

PHASE VOLTAGE

Figure 4-30



Average Value of the Waveform = (4/3)V = 1.333V
RMS Value of the Waveform = $\sqrt{2}$ V = 1.414V
RMS Value of the Fundamental = $\frac{(3\sqrt{2})V}{\pi}$ = 1.350V
Total Harmonic Distortion = 31.1%

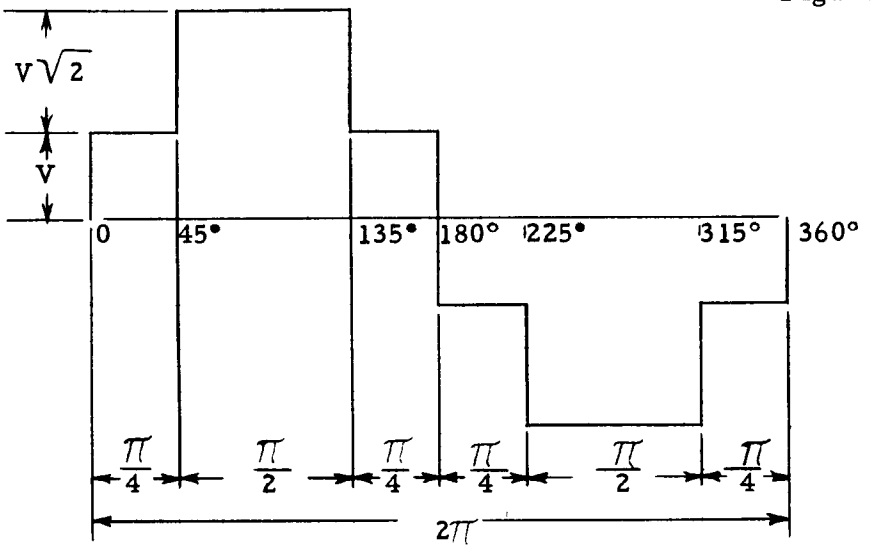
Waveform 5 P

SIX STEP-UNEQUAL TIME -UNEQUAL HEIGHT

TYPE A

PHASE VOLTAGE

Figure 4-31



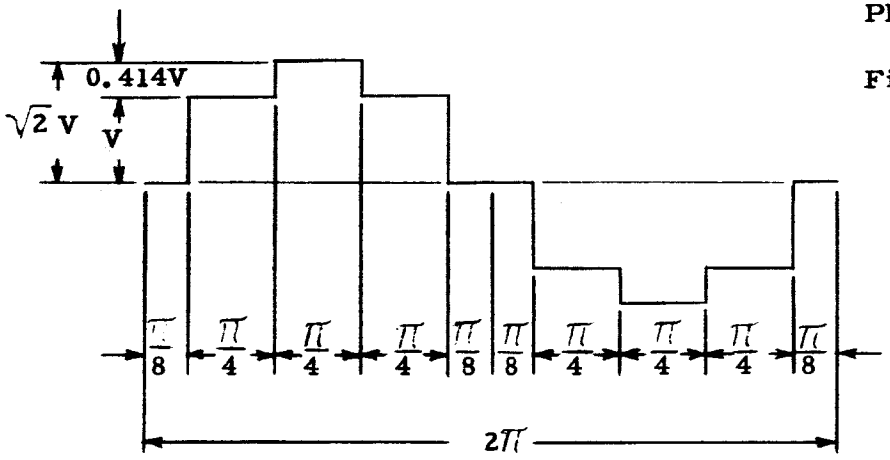
Average Value of the Waveform = 1.707V
RMS Value of Waveform = 1.8477V
RMS Value of the Fundamental = 1.801V
Total Harmonic Distortion = 22.9%

Waveform 6 P

EIGHT STEP-EQUAL TIME-UNEQUAL HEIGHT
TYPE A

PHASE VOLTAGE

Figure 4-32



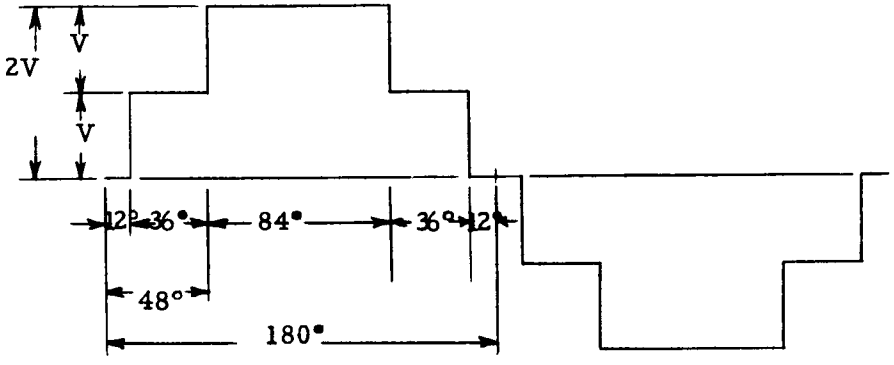
Average Value of the Waveform = 0.8536V
RMS Value of the Waveform = 1.0V
RMS Value of the Fundamental = 0.9743V
Total Harmonic Distortion = 23.1%

Waveform 7 P

EIGHT STEP-UNEQUAL TIME-EQUAL HEIGHT

PHASE VOLTAGE

Figure 4-33



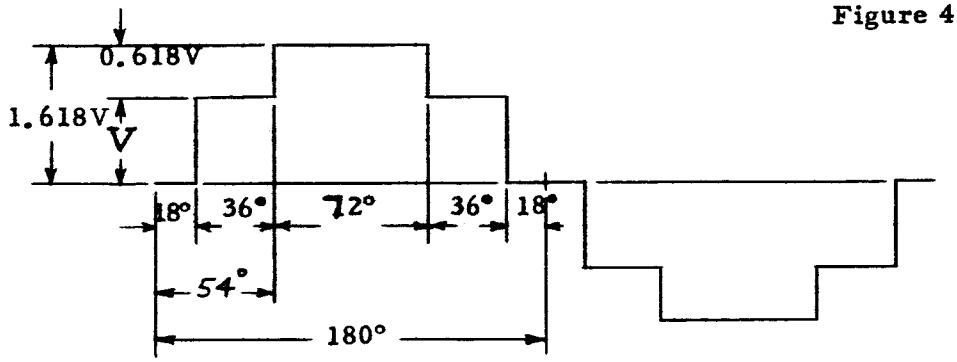
Average Value of Waveform = 1.333V
RMS Value of the Waveform = 1.5055V
RMS Value of the Fundamental = 1.483V
Total Harmonic Distortion = 17.4%

Waveform 8 P

EIGHT STEP-UNEQUAL TIME-UNEQUAL HEIGHT
TYPE A

PHASE VOLTAGE

Figure 4-34



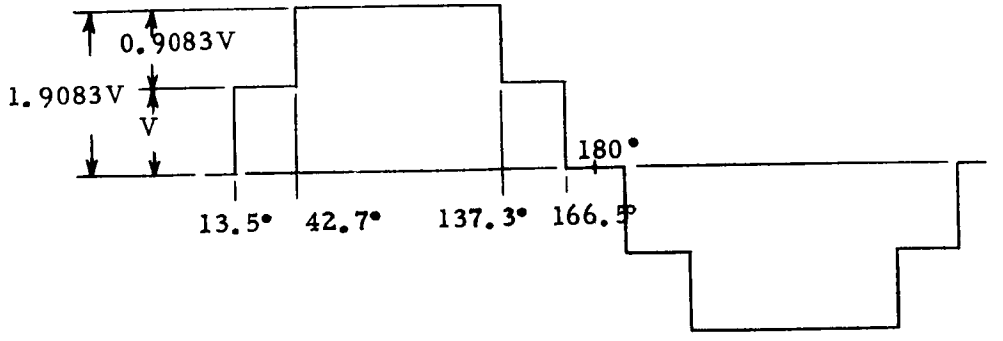
Average Value of the Waveform = 1.0472V
RMS Value of the Waveform = 1.203V
RMS Value of the Fundamental = 1.1835V
Total Harmonic Distortion = 18.3%

Waveform 9 P

EIGHT STEP-UNEQUAL TIME-UNEQUAL HEIGHT
TYPE B

PHASE VOLTAGE

Figure 4-35



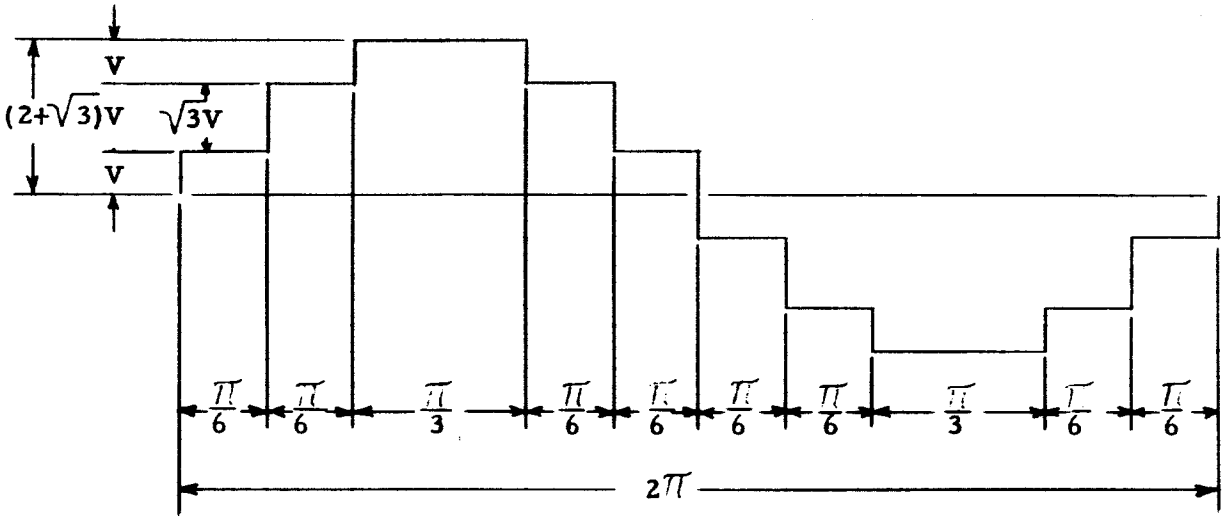
Average Value of the Waveform = 1.325V
RMS Value of the Waveform = 1.496V
RMS Value of the Fundamental = 1.476V
Total Harmonic Distortion = 16.6%

Waveform 10 P

TEN STEP-UNEQUAL TIME-UNEQUAL HEIGHT
TYPE A

PHASE VOLTAGE

Figure 4-36



Average Value of the Waveform = $\frac{(4+2\sqrt{3})V}{3}$ = 2.488V

RMS Value of the Waveform = 2.73205V

RMS Value of the Fundamental = $\frac{6\sqrt{2}V}{\pi}$ = 2.701V

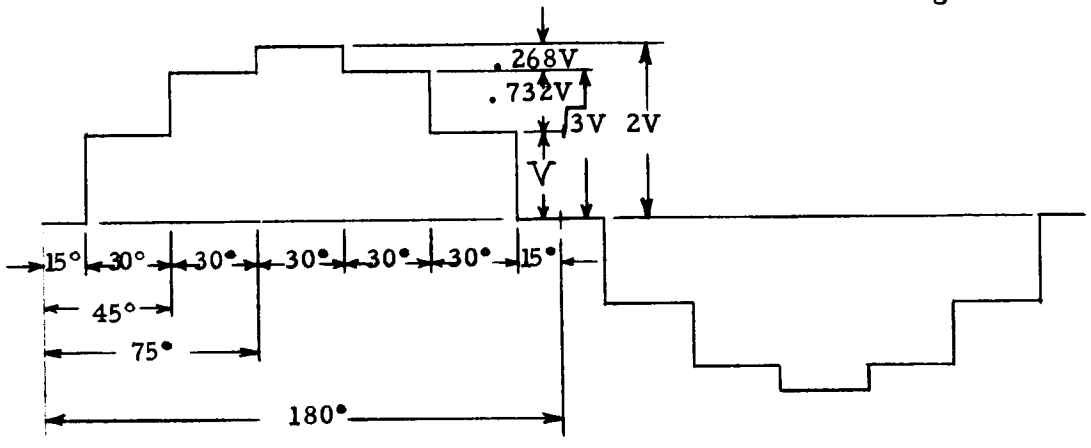
Total Harmonic Distortion = 15.2%

Waveform 11 P

TWELVE STEP-EQUAL TIME-UNEQUAL HEIGHT

PHASE VOLTAGE

Figure 4-37



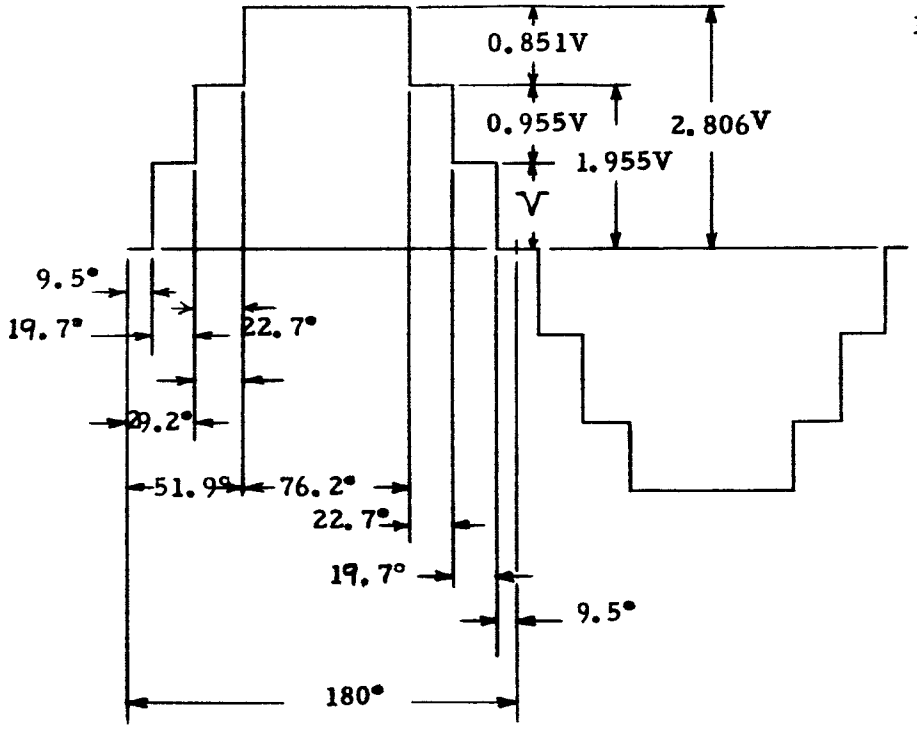
Average Value of the Waveform = 1.244V
RMS Value of the Waveform = 1.414V
RMS Value of the Fundamental = 1.398V
Total Harmonic Distortion = 15.3%

Waveform 12 P

TWELVE STEP-UNEQUAL TIME-UNEQUAL HEIGHT
TYPE A

PHASE VOLTAGE

Figure 4-38



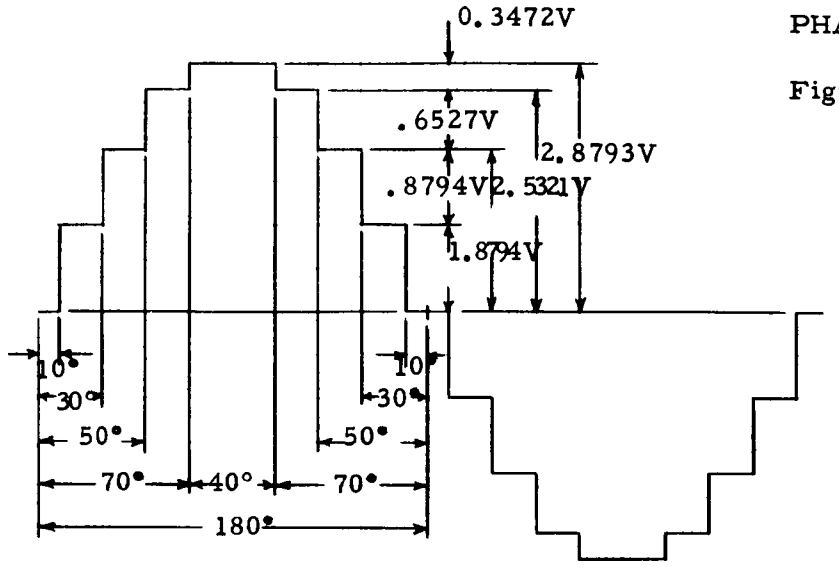
Average Value of the Waveform = 1.889V
RMS Value of the Waveform = 2.125V
RMS Value of the Fundamental = 2.111V
Total Harmonic Distortion = 11.5%

Waveform 13 P

SIXTEEN STEP-UNEQUAL TIME-UNEQUAL HEIGHT

PHASE VOLTAGE

Figure 4-39



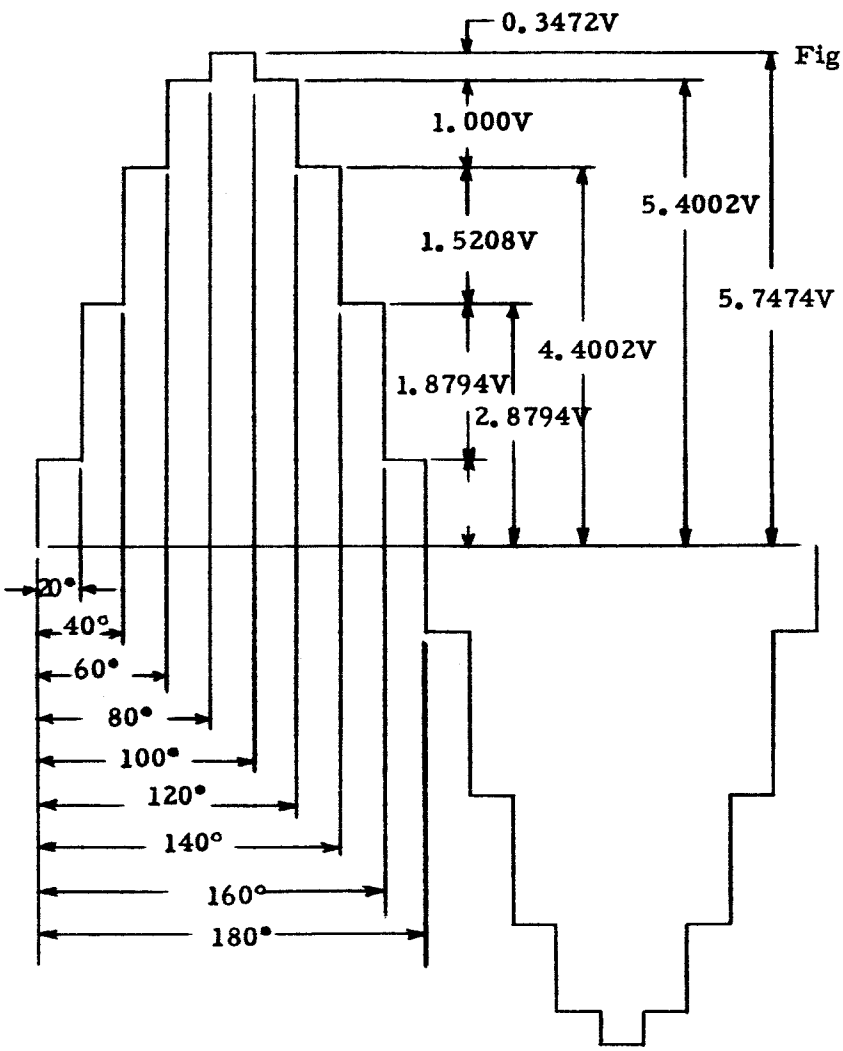
Average Value of the Waveform = 1.8426V
RMS Value of the Waveform = 2.0674V
RMS Value of the Fundamental = 2.0553V
Total Harmonic Distortion = 10%

Waveform 14 P

EIGHTEEN STEP-EQUAL TIME-UNEQUAL HEIGHT

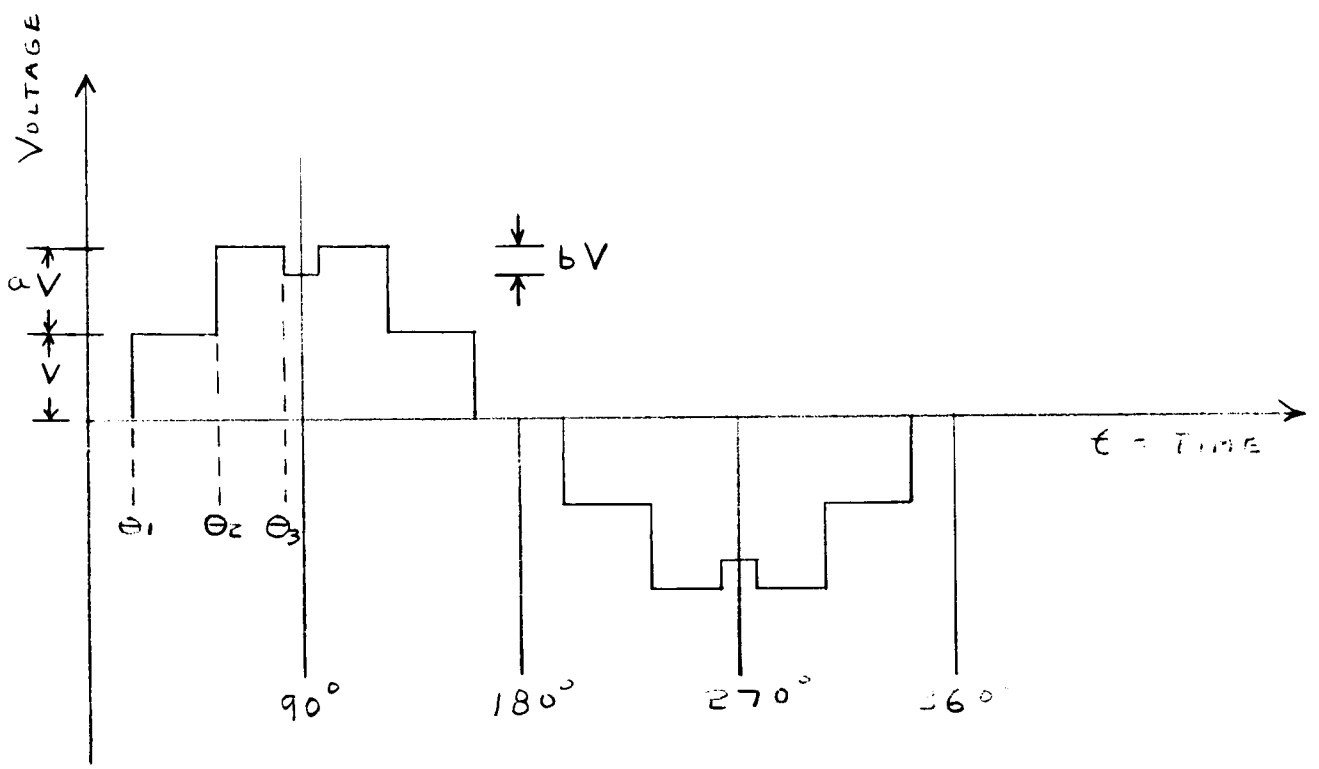
PHASE VOLTAGE

Figure 4-40



Average Value of the Waveform = 3.679V
RMS Value of the Waveform = 4.064V
RMS Value of the Fundamental = 4.036V
Total Harmonic Distortion = 10%

Waveform 15 P



NORMALIZED WAVEFORM e(t)

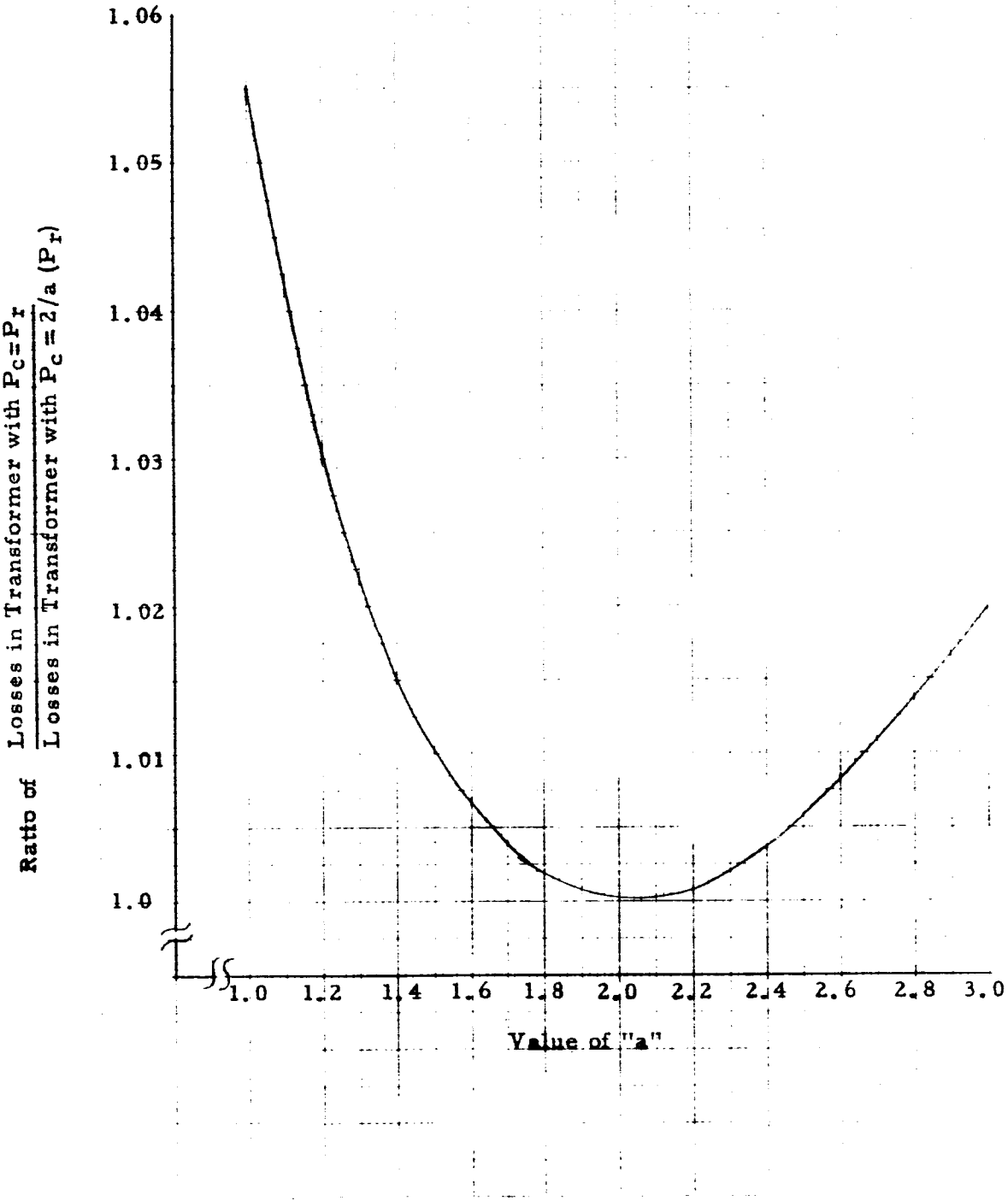
FOR EXAMPLE 4-2

FIGURE 4-41

Figure 4 - 42

Ratio of Losses in Transformers Designed with Equal Copper & Core Loss to Transformers Designed with Core Loss=2/a Copper Loss (where "a" is the exponent in the core loss vs. flux density relationship)

$P = C_1 B^a = \frac{\text{Core Loss}}{\text{Unit Volume}}$



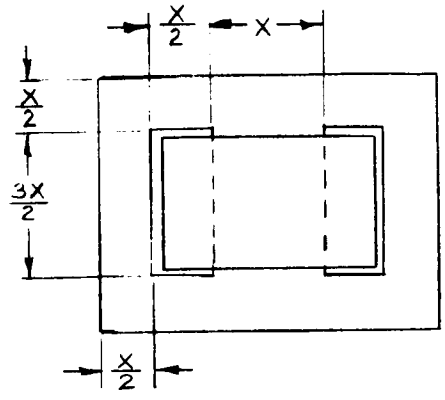


Figure 4 - 43
Conventional Single Phase
EI "Scrapless Lamination"

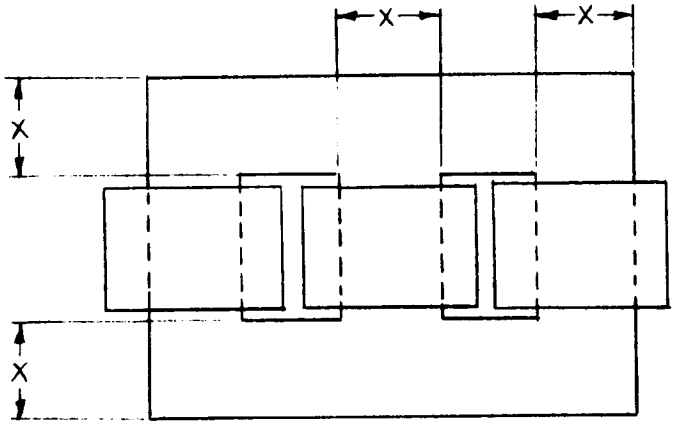


Figure 4 - 44
Three Phase Lamination
which uses same coils
as Figure 4 - 69

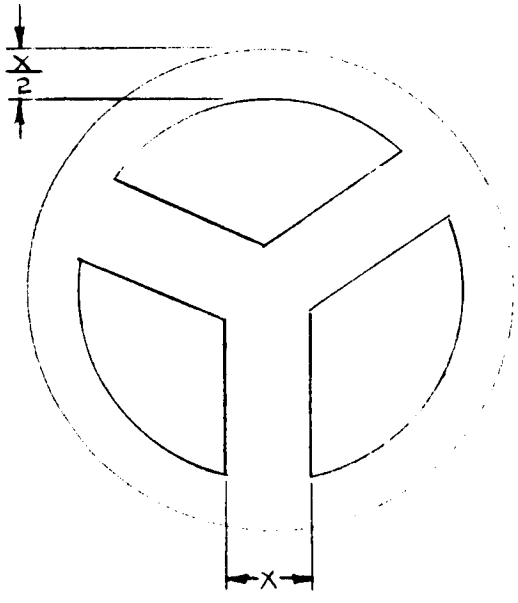
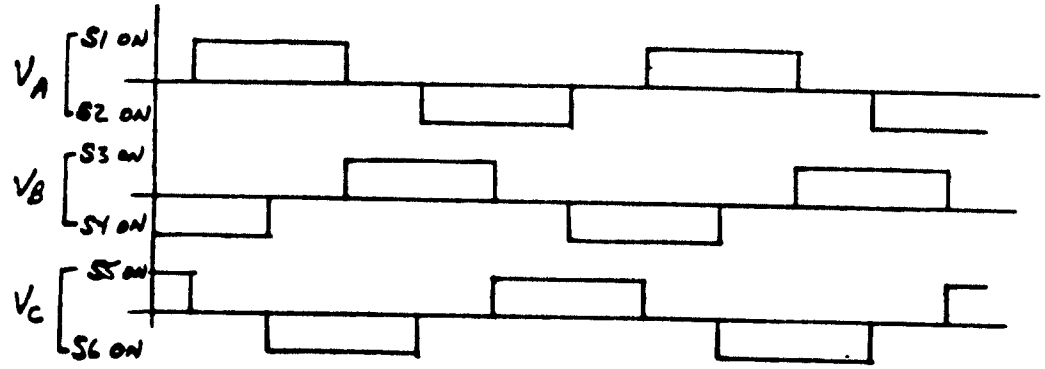


Figure 4 - 45
Circular Three Phase
Lamination



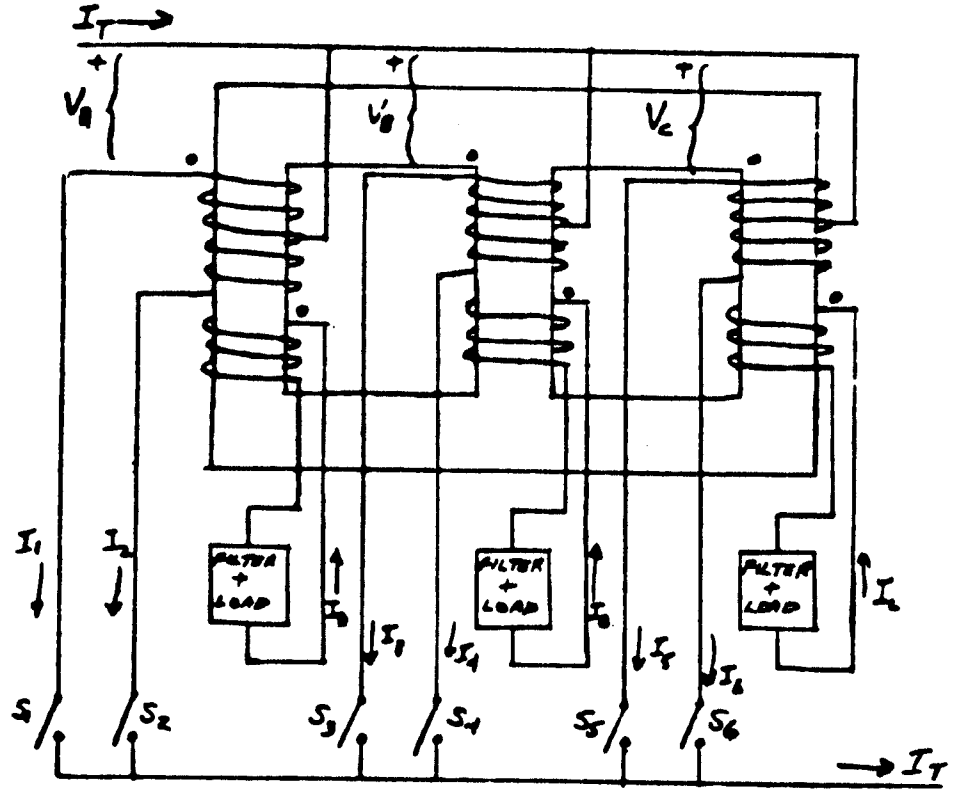


FIG. 4-46

SWITCHING PATTERN FOR THREE PHASE TRANSFORMER WITH 120° QUASI-SQUARE WAVE EXCITATION.

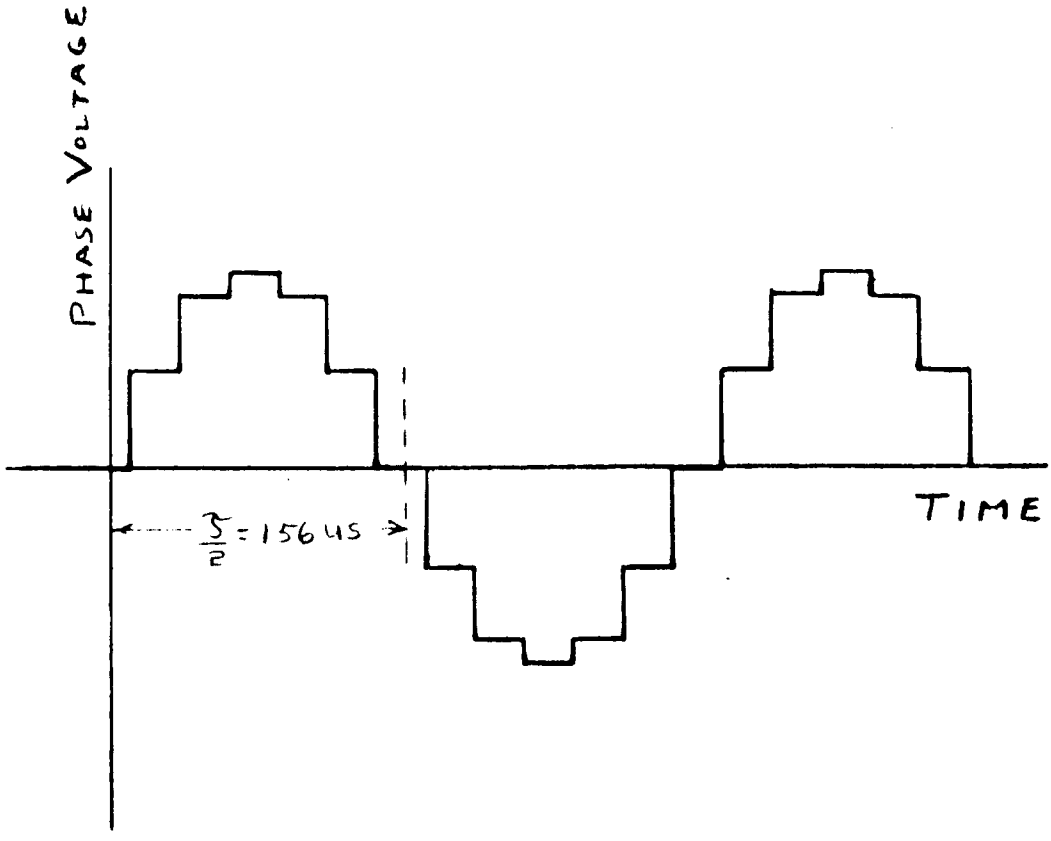


FIG 4-47
MULTI-STEPPED OUTPUT VOLTAGE WAVEFORM
(COMPOSED OF SIX SQUARE WAVES)

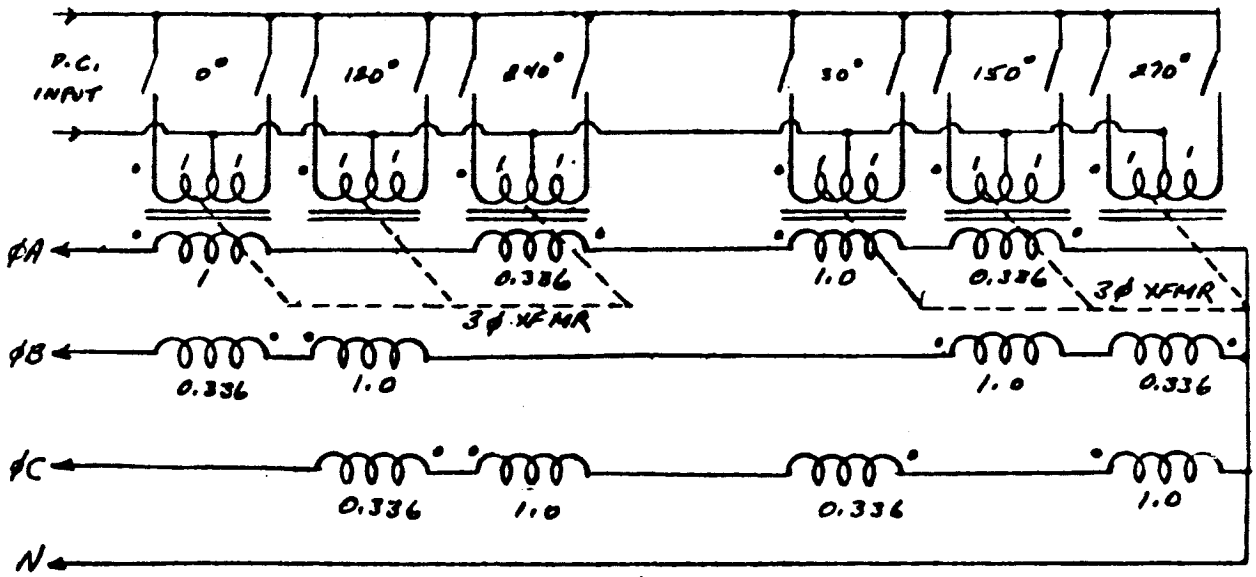
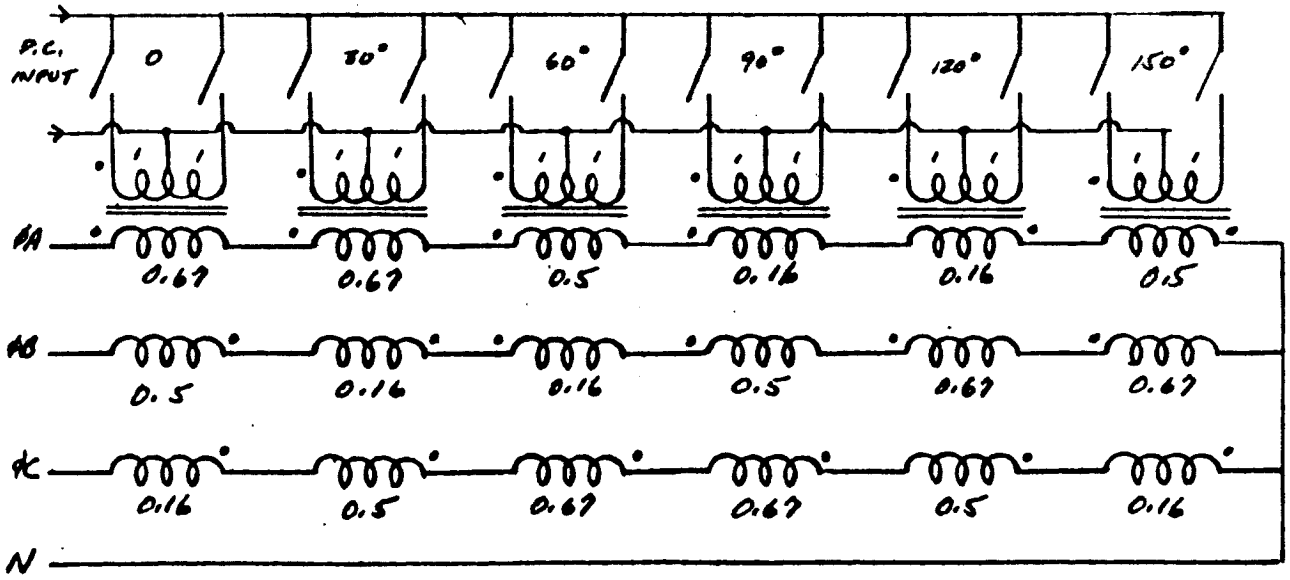
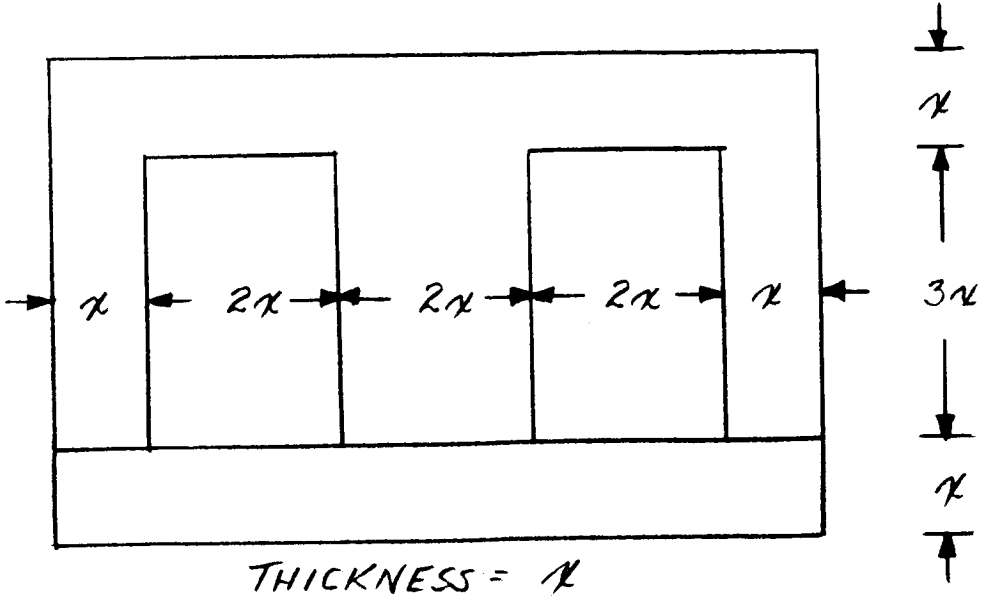


FIG. 4-49 ↑ MULTI-STEPPED WAVEFORM OUTPUT CIRCUIT UTILIZING THREE PHASE TRANSFORMERS

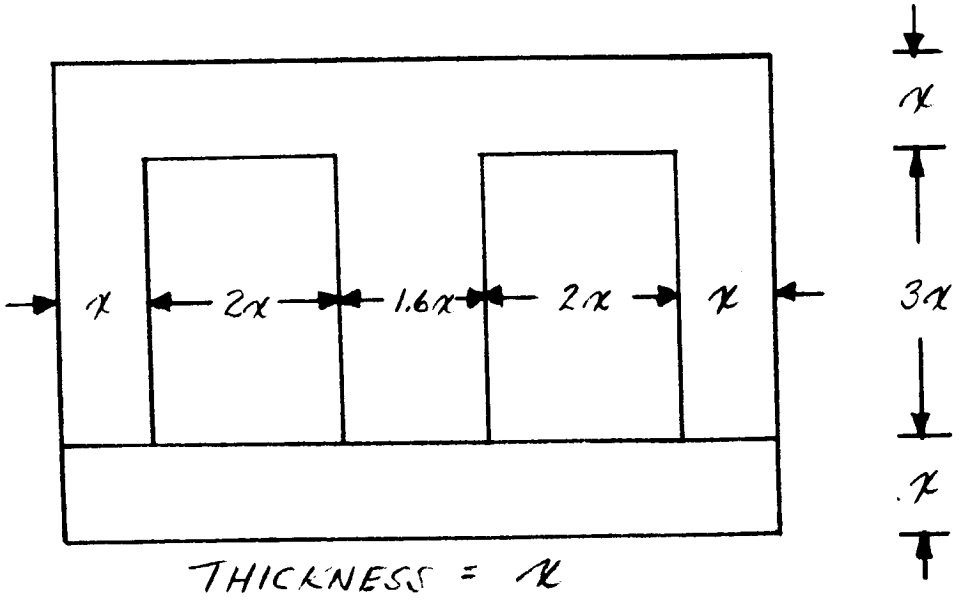
FIG. 4-48 ↓ MULTI-STEPPED WAVEFORM OUTPUT CIRCUIT UTILIZING SINGLE PHASE TRANSFORMERS





CONVENTIONAL FLUX ADDING TRANSFORMER CORE DESIGN

FIGURE 4-50



FLUX-ADDING TRANSFORMER CORE DESIGN WITH REDUCED CENTER L

FIGURE 4-51

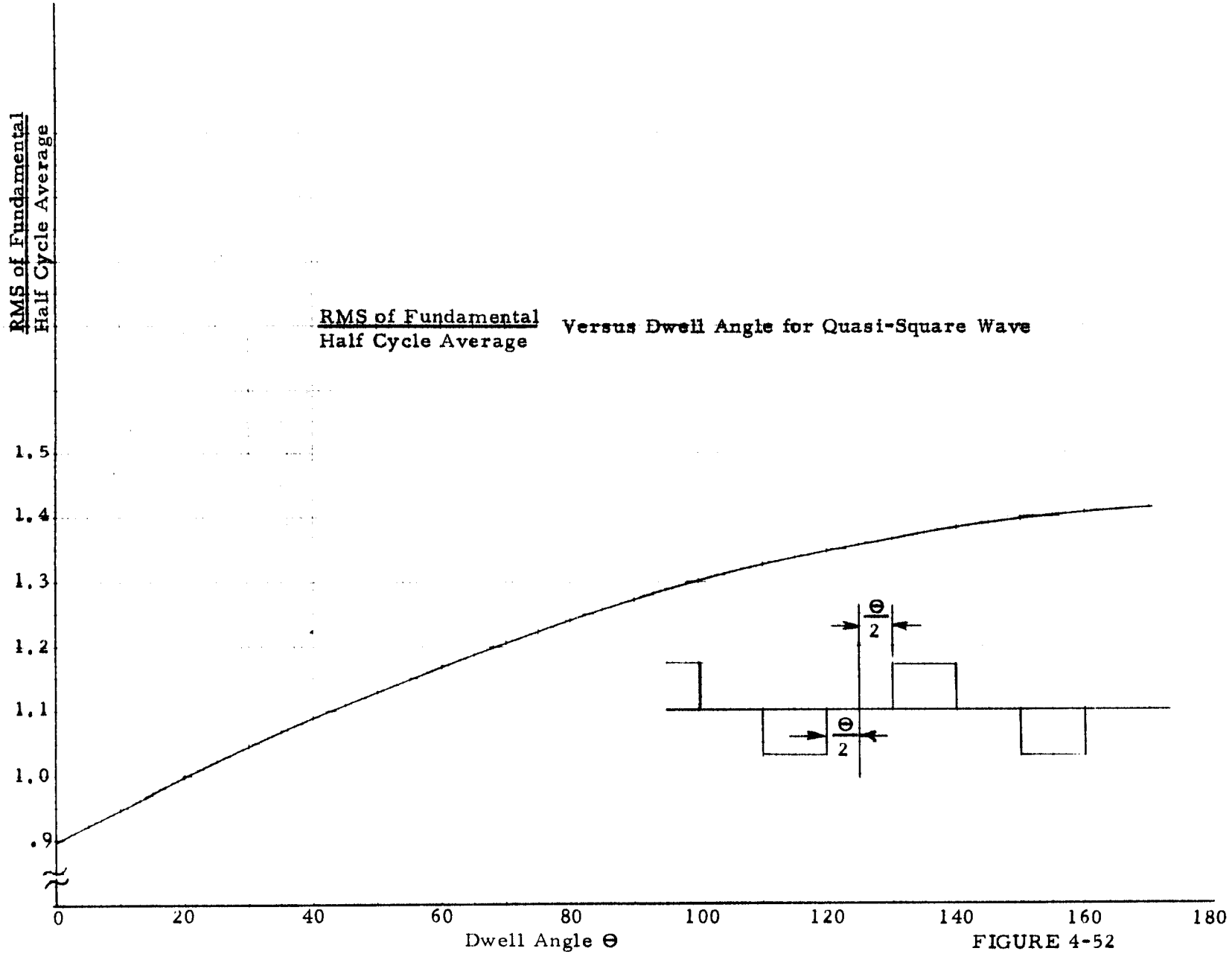
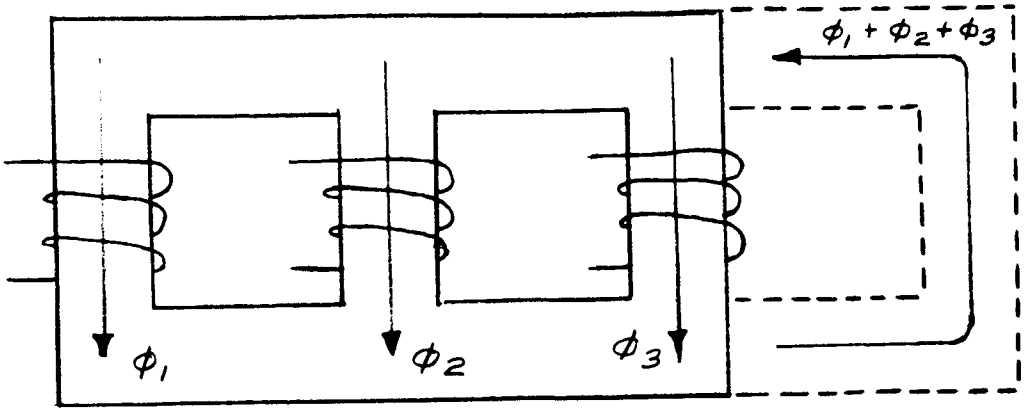
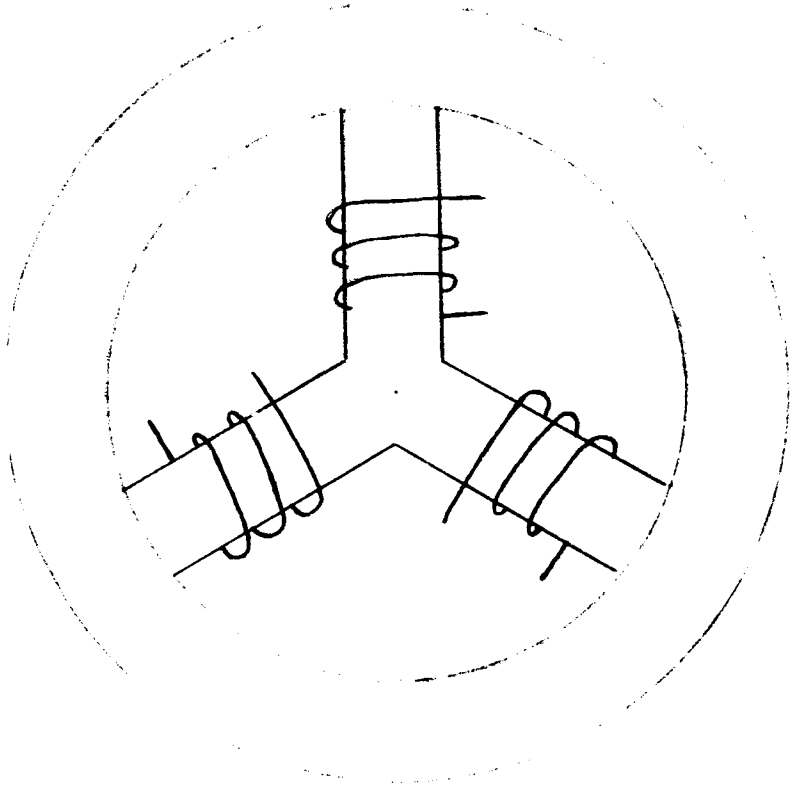

RMS of Fundamental
Half Cycle Average
RMS of Fundamental
Half Cycle Average
Versus Dwell Angle for Quasi-Square Wave
1.5
1.4
1.3
1.2
1.1
1.0
.9
0
20
40
60
80
100
120
140
160
180
Dwell Angle Θ
Θ
2
Θ
2

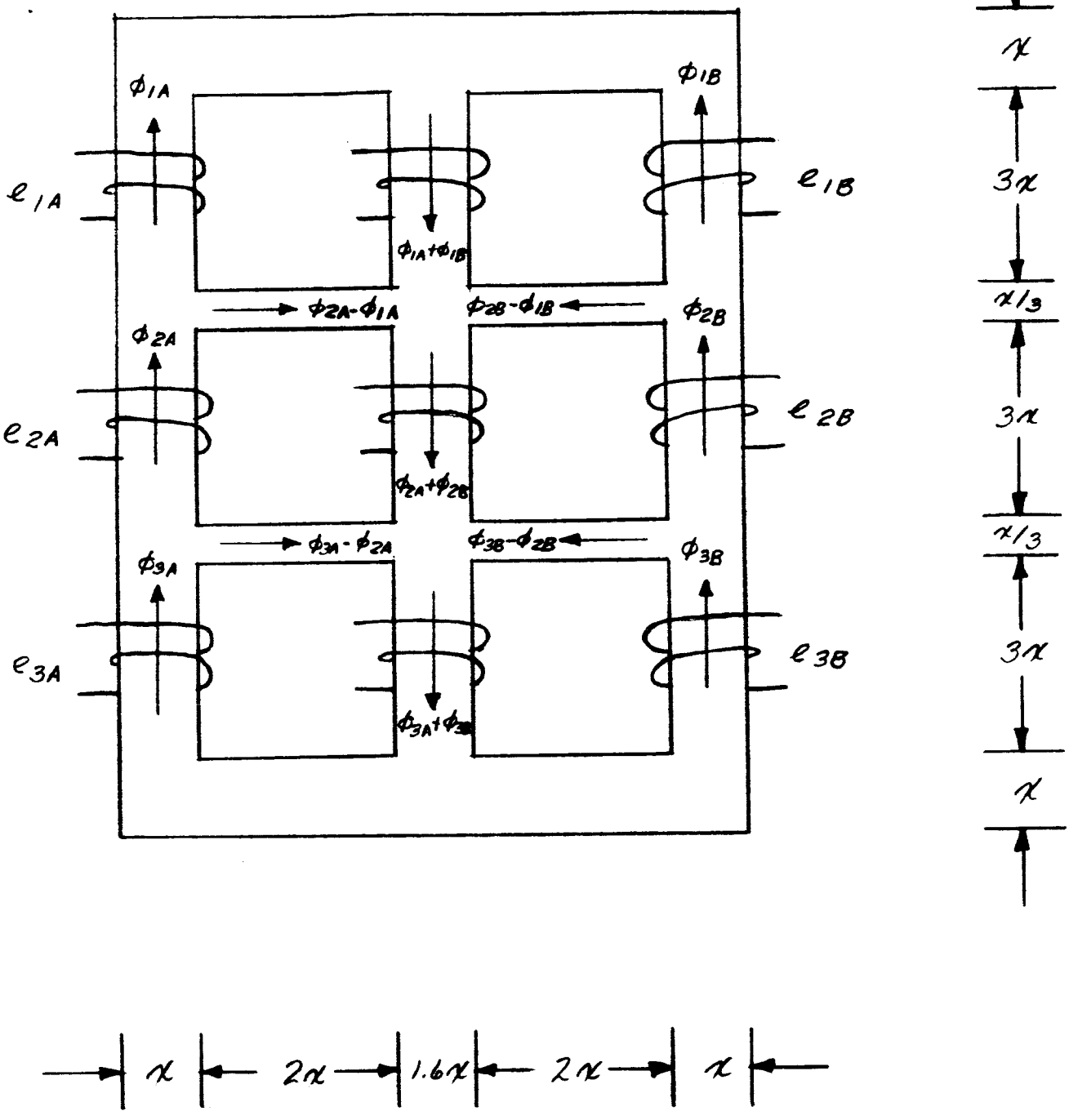
FIGURE 4-52



CONVENTIONAL THREE PHASE TRANSFORMER CORE DESIGN
FIGURE 4-53

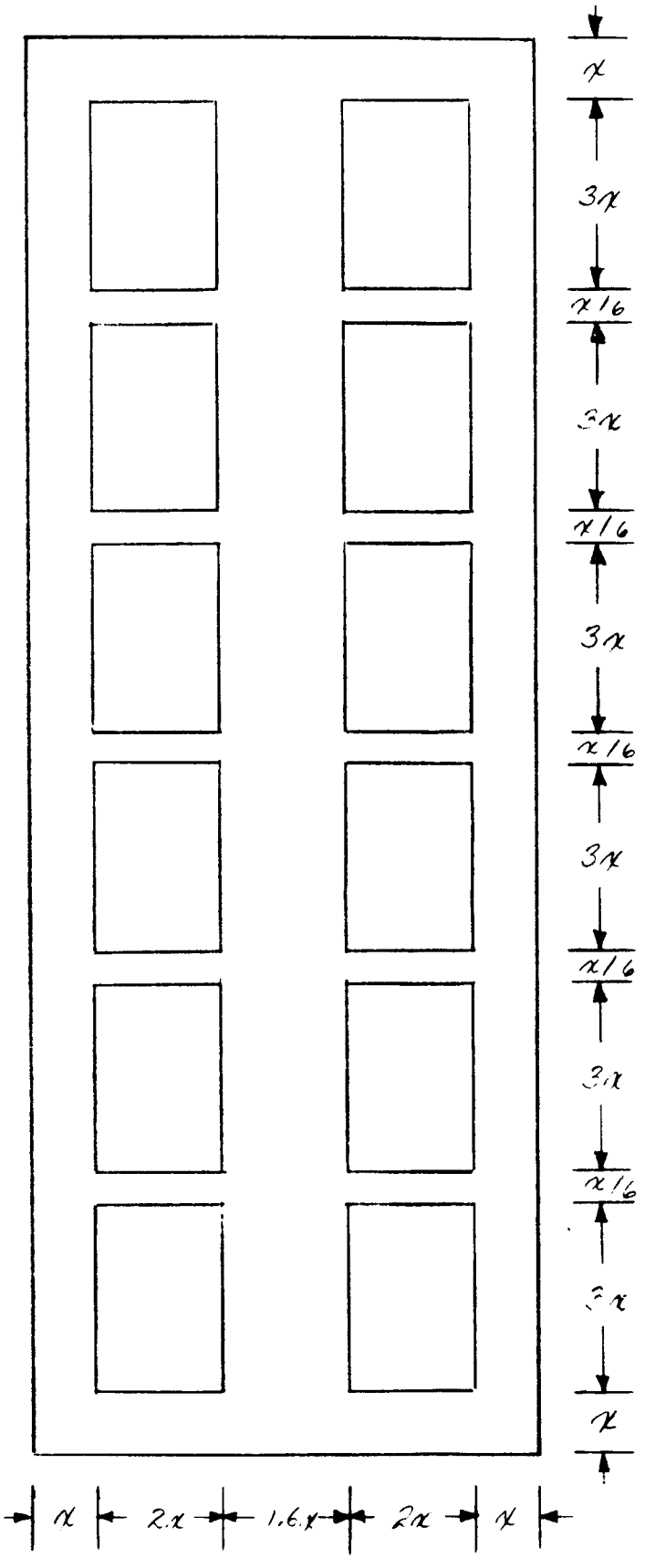


MODIFIED THREE PHASE TRANSFORMER CORE DESIGN (GULOW)
FIGURE 4-54



THREE PHASE FLUX ADDING TRANSFORMER CORE DESIGN

FIGURE 4-55



SIX PHASE FLUX-ADDING TRANSFORMER CORE DESIGN

FIGURE 4-56

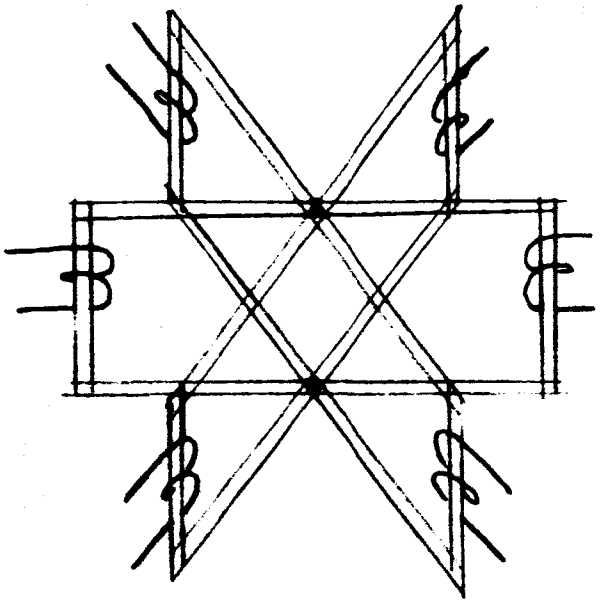


FIGURE 4-57
SIX PHASE THREE DIMENSIONAL CORE DESIGN

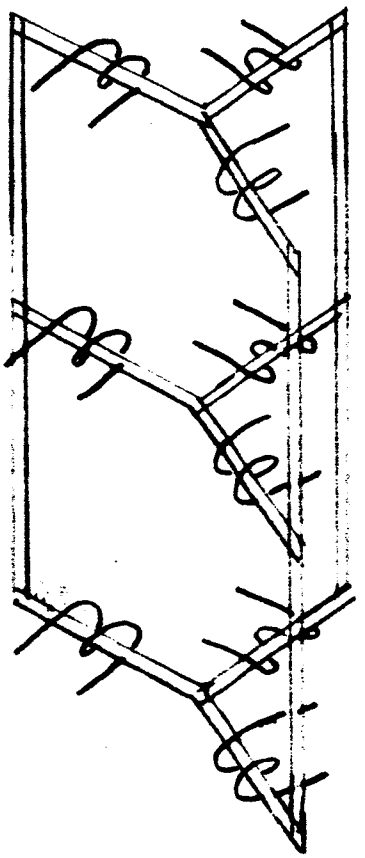


FIGURE 4-58
THREE PHASE FLUX-ADDING THREE DIMENSIONAL CORE DESIGN

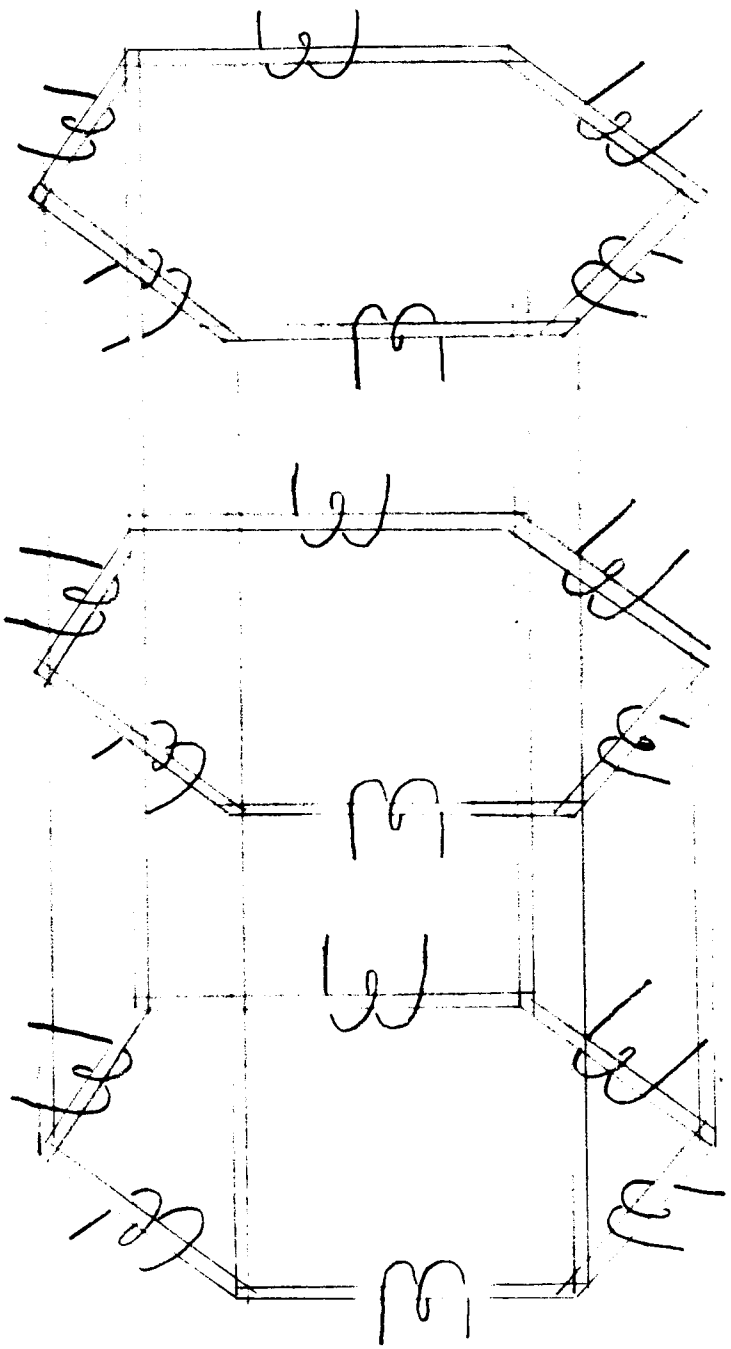
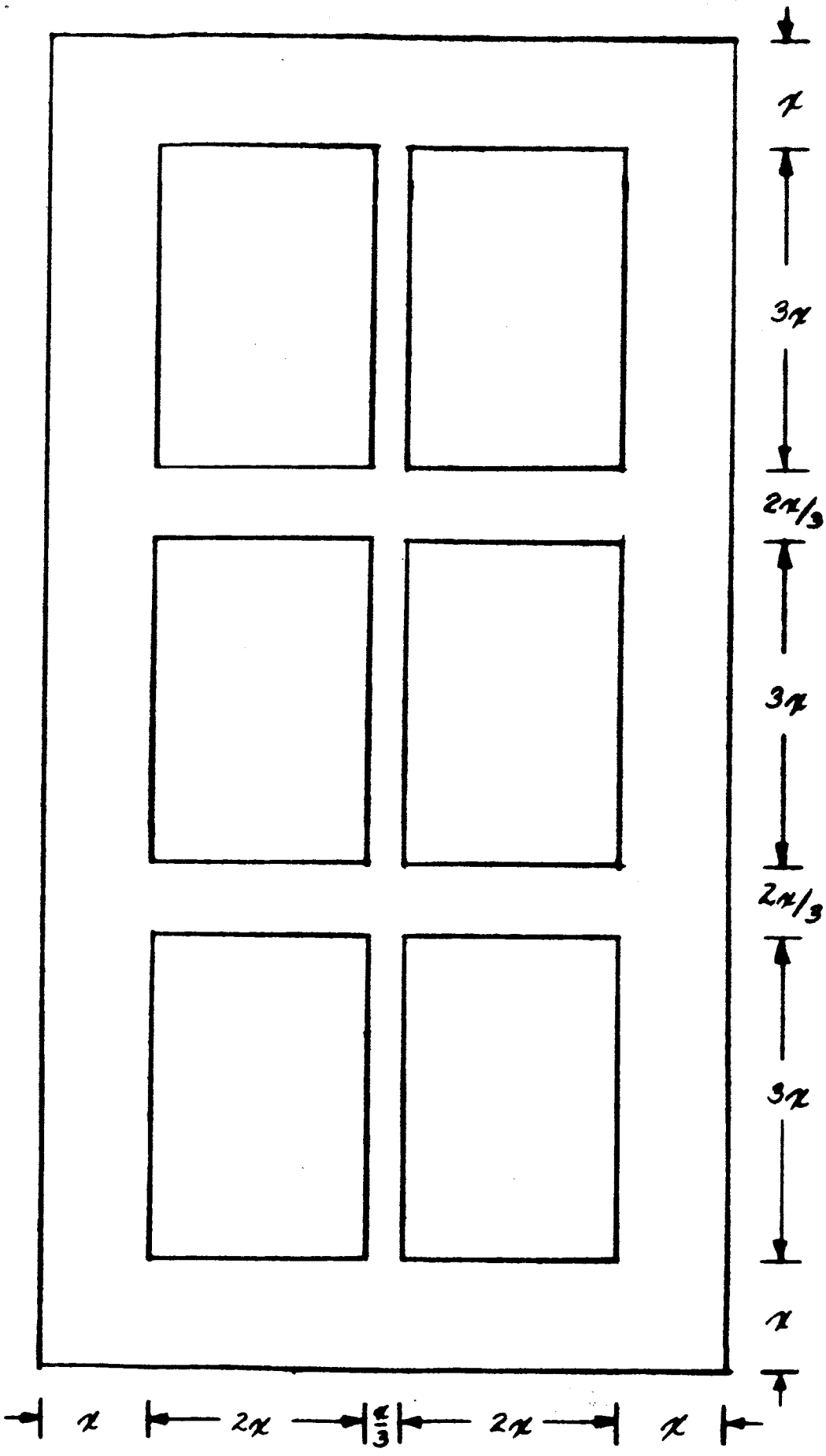


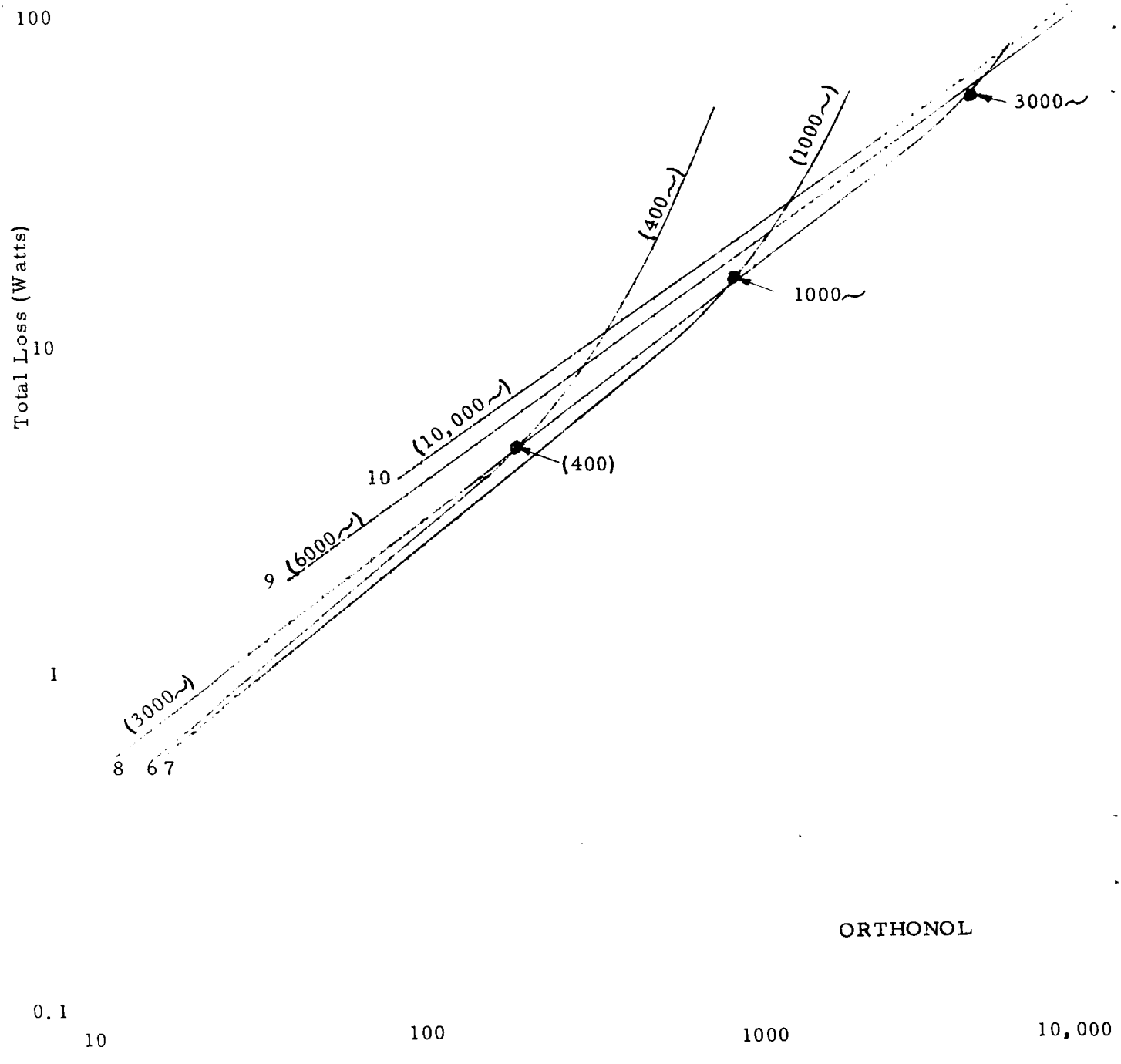
FIGURE 4-59

SIX PHASE FLUX-ADDING THREE DIMENSIONAL CORE DESIGN



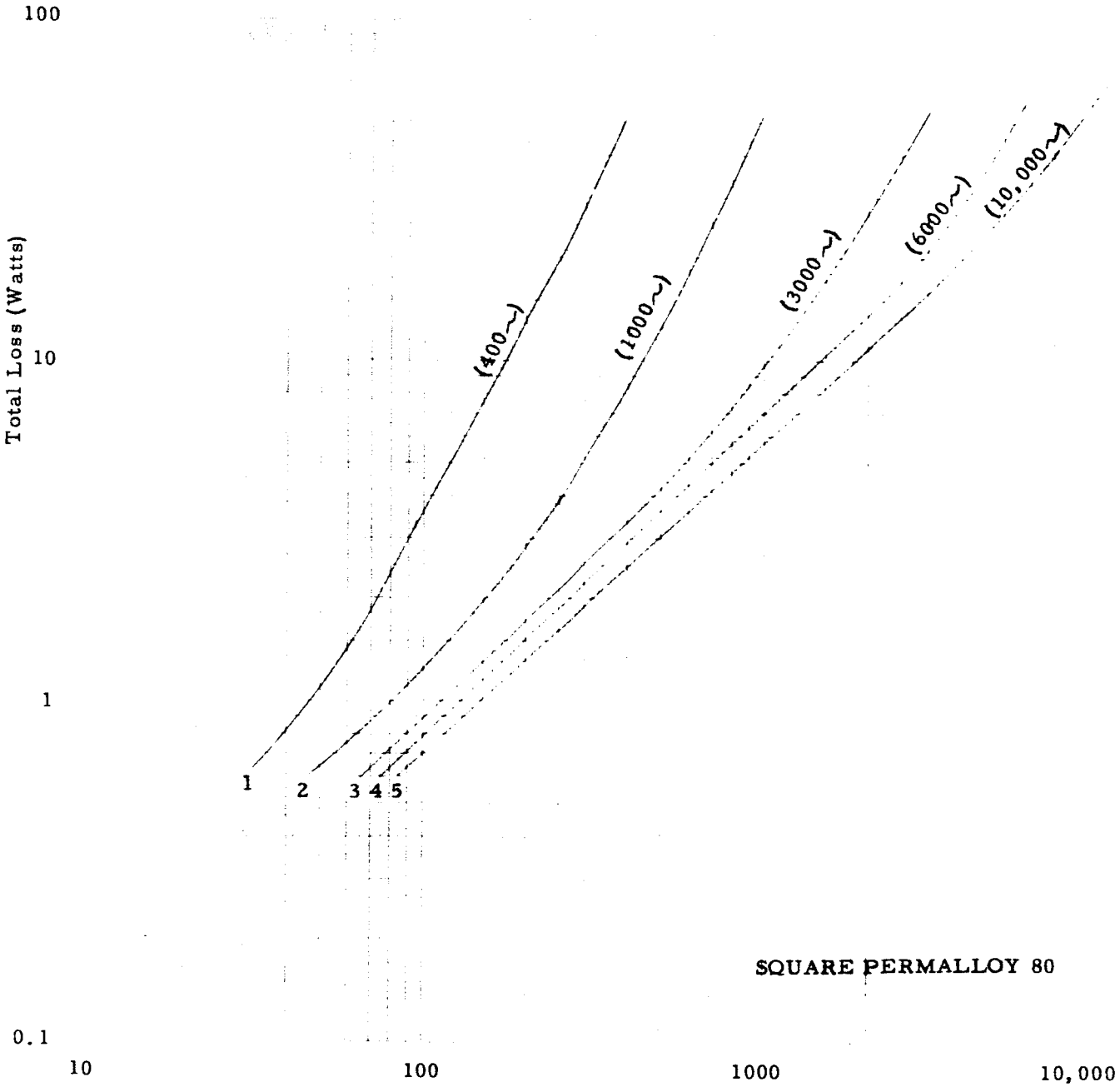
"HEXADIC" TRANSFORMER CORE DESIGN

FIGURE 4-60



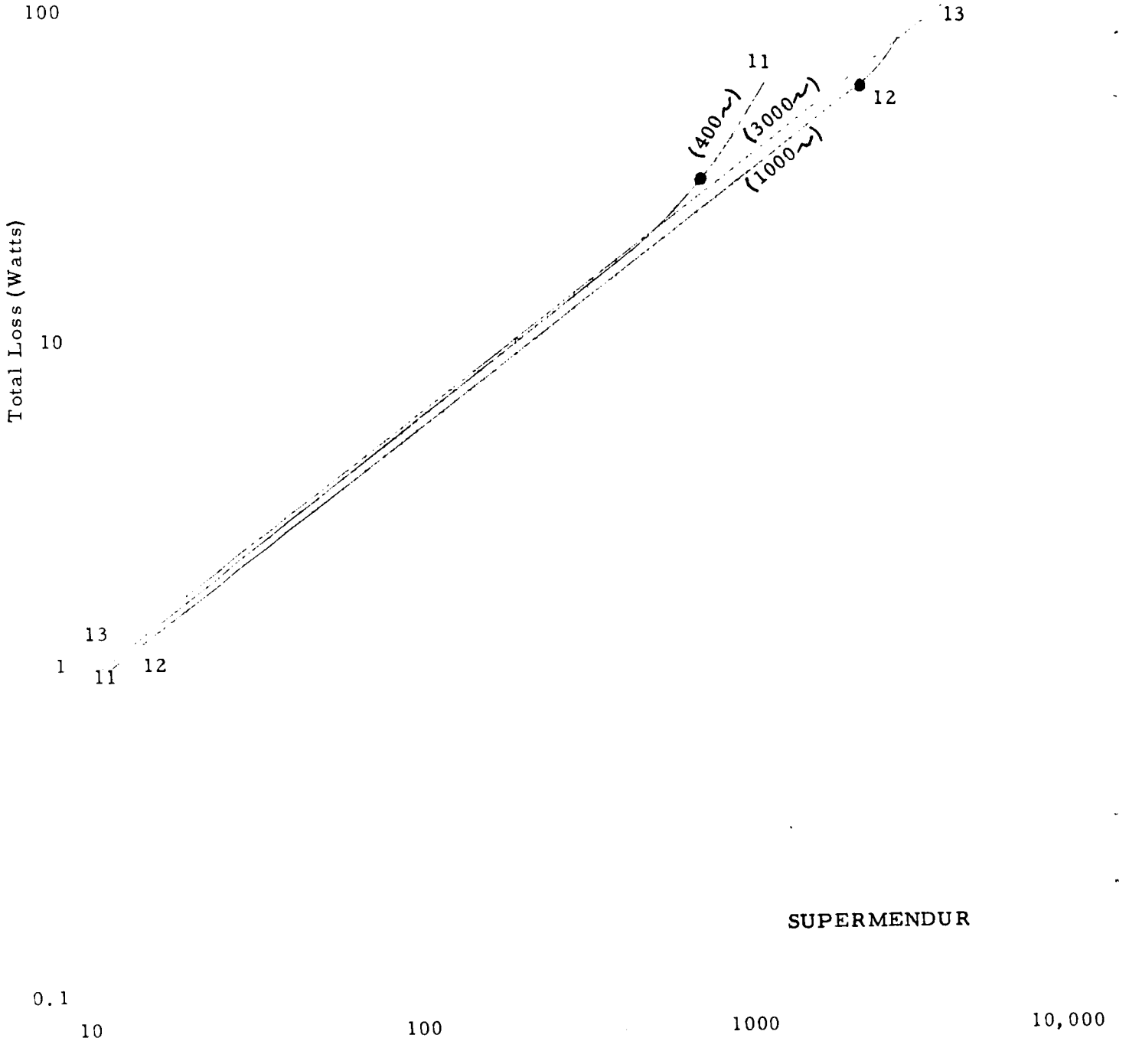
Transformer Designs

Figure 4 - 61



Transformer Designs

Figure 4 - 62



Transformer Designs

Figure 4 - 63

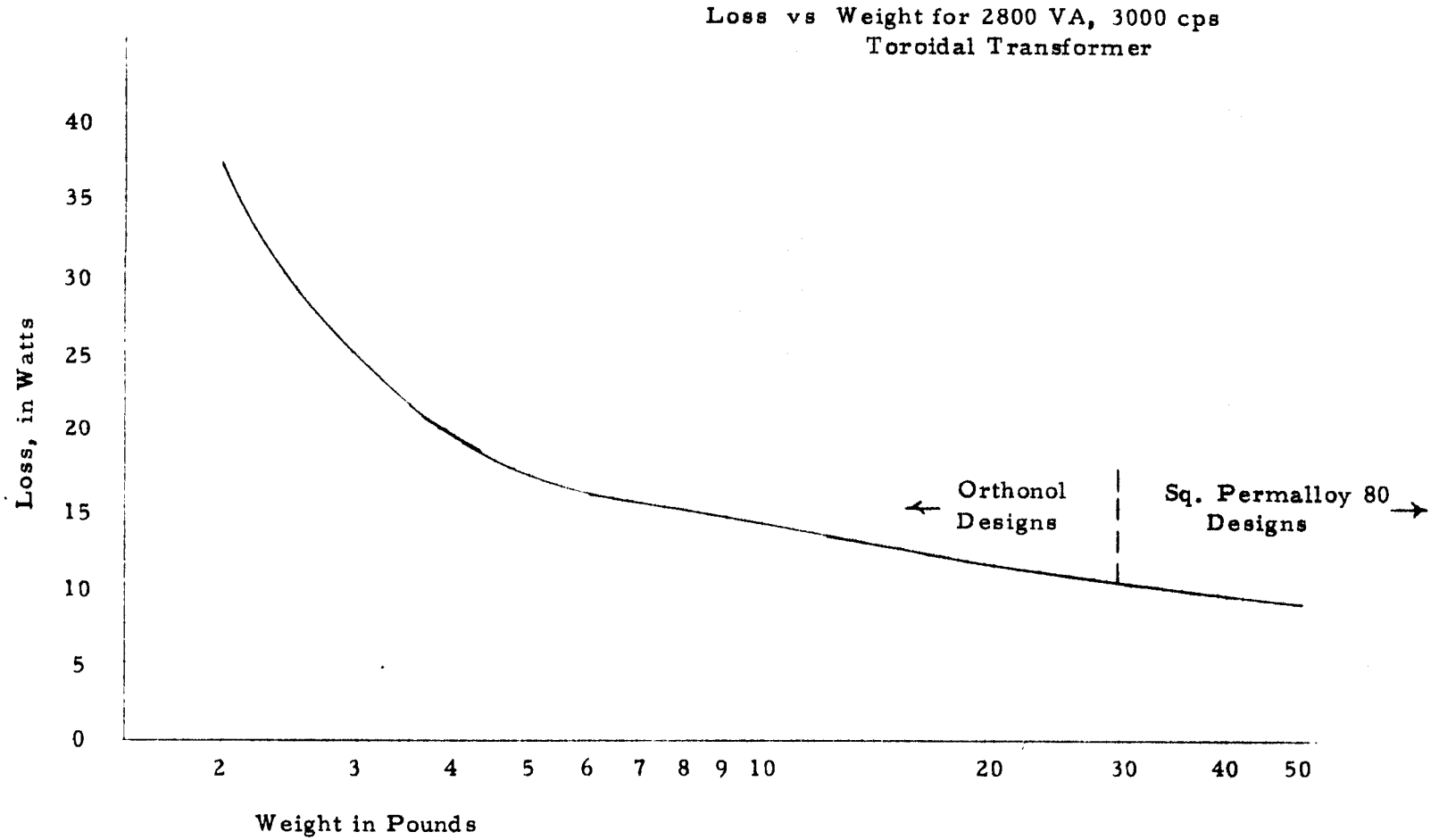
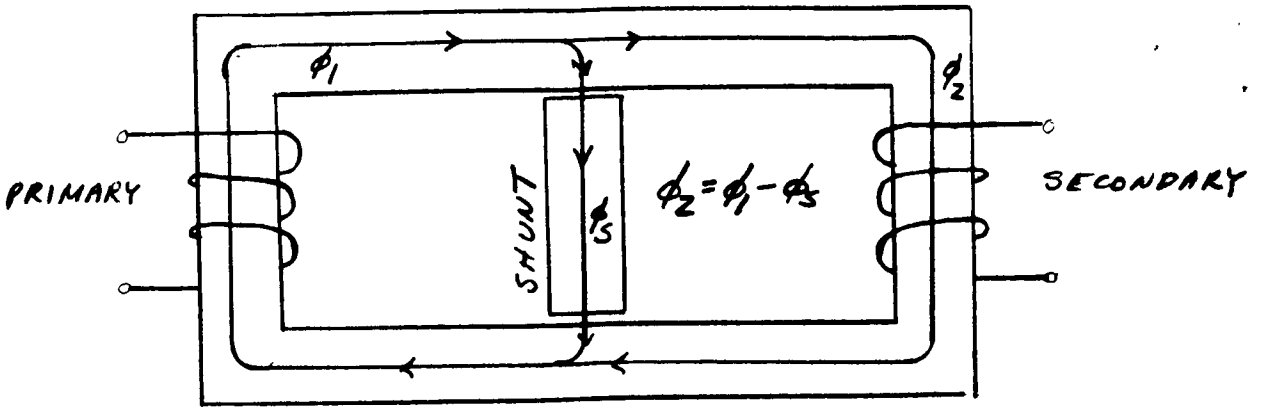
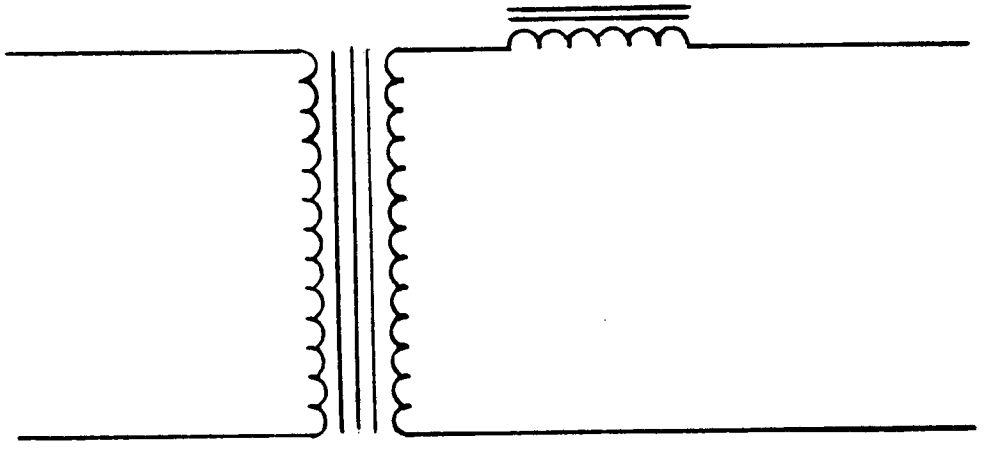

Loss vs Weight for 2800 VA, 3000 cps
Toroidal Transformer
Loss, in Watts
40
35
30
25
20
15
10
5
0
2
3
4
5
6
7
8
9
10
20
30
40
50
Weight in Pounds
Orthonol Designs
Sq. Permalloy 80 Designs

Figure 4 - 64



TRANSFORMER WITH MAGNETIC SHUNT

FIGURE 4-65

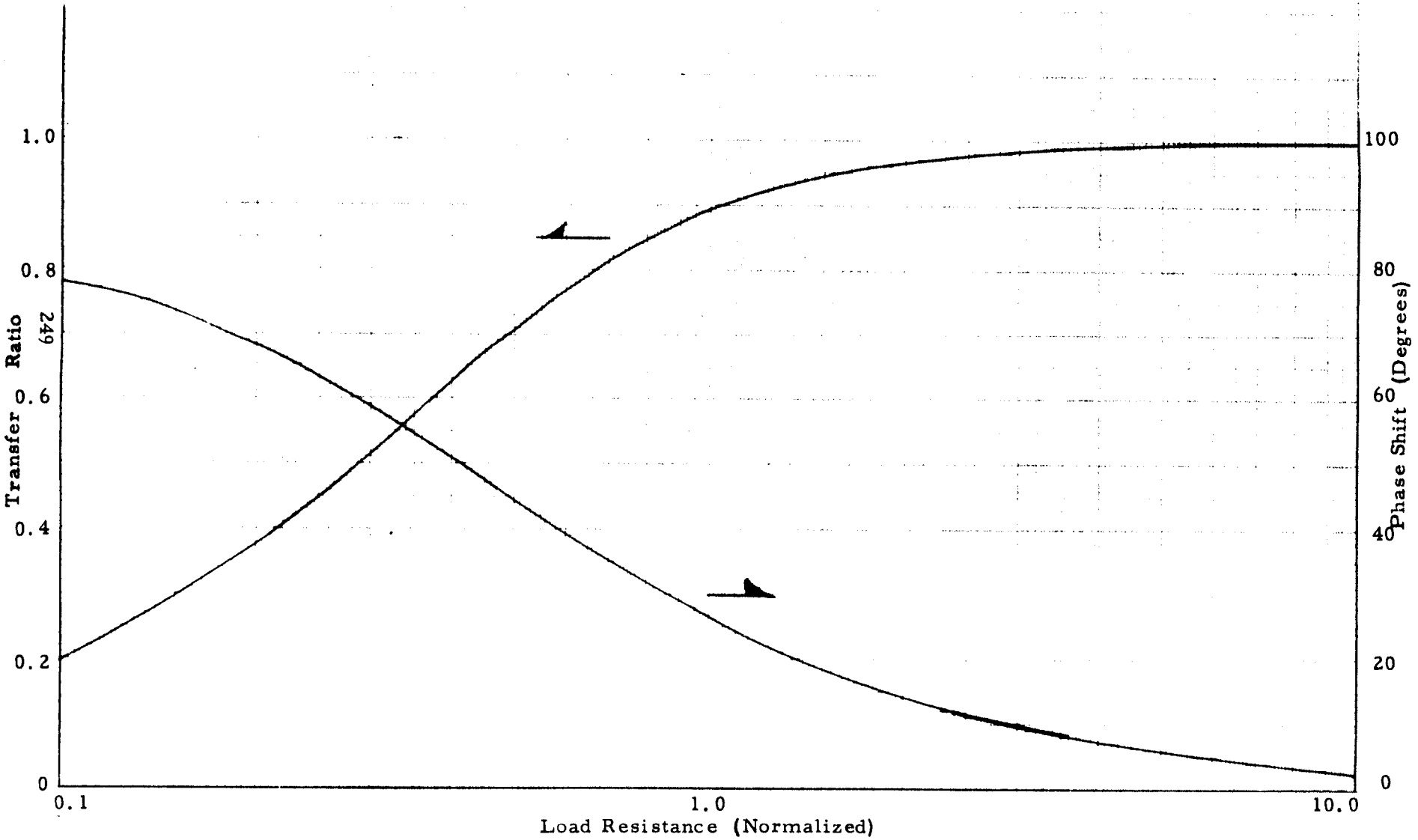


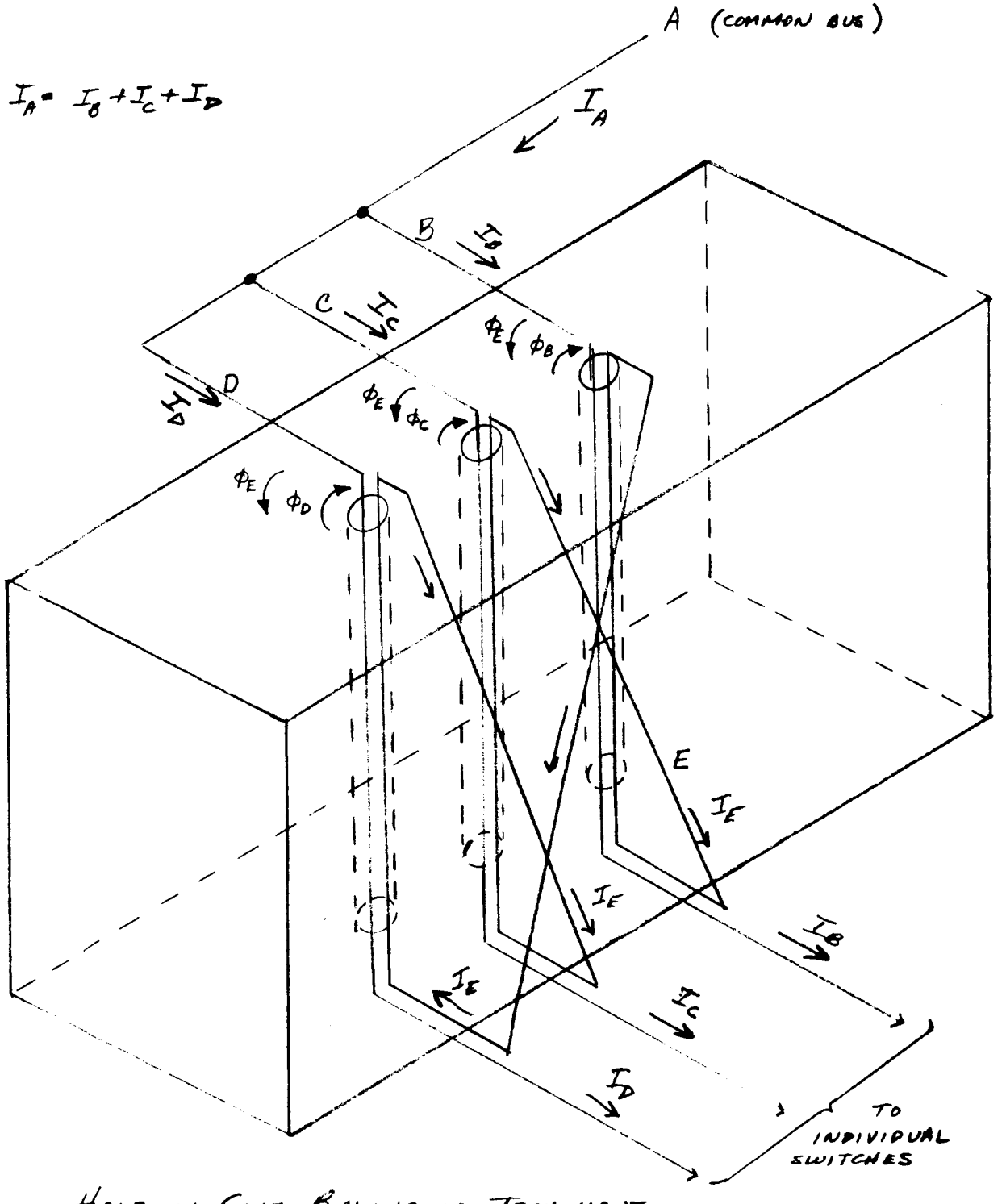
EQUIVALENT CIRCUIT OF TRANSFORMER WITH MAGNETIC SHUNT

FIGURE 4-66

Transfer Ratio and Phase Shift vs Load Resistance

Figure 4 - 67





HOLE-IN-CORE BALANCING TECHNIQUE

FIGURE 4-68

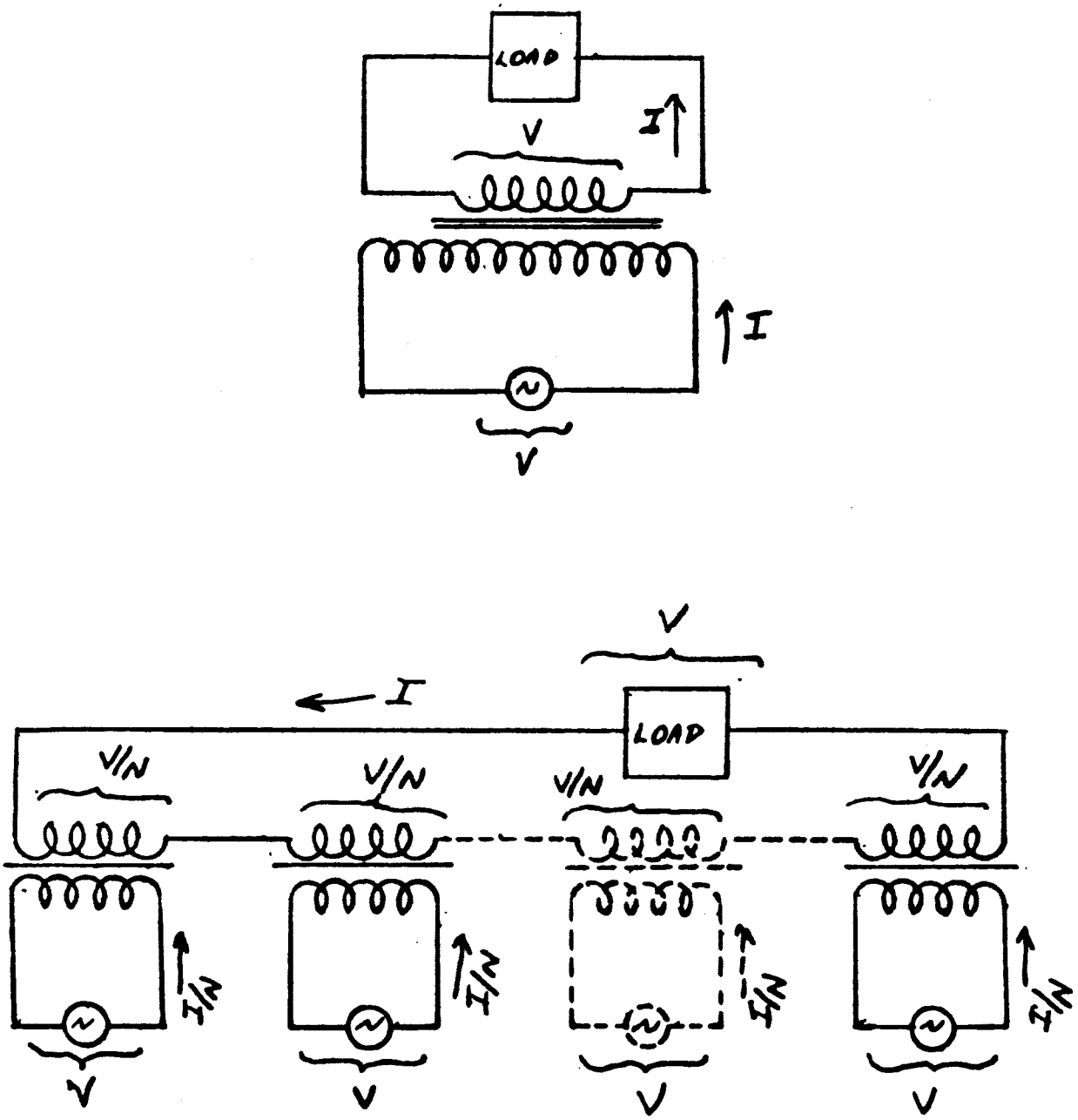


FIG. 4-69 LOAD SHARING BY SPLIT TRANSFORMER TECHNIQUE

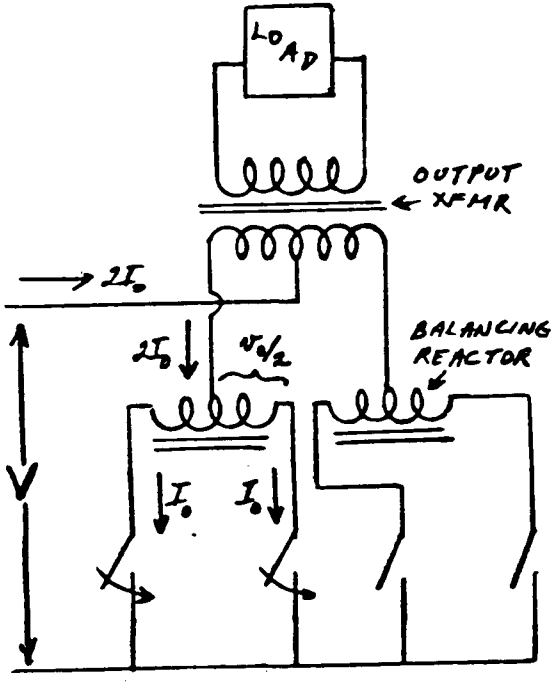


FIG 4-70 LOAD SHARING WITH BALANCING REACTORS

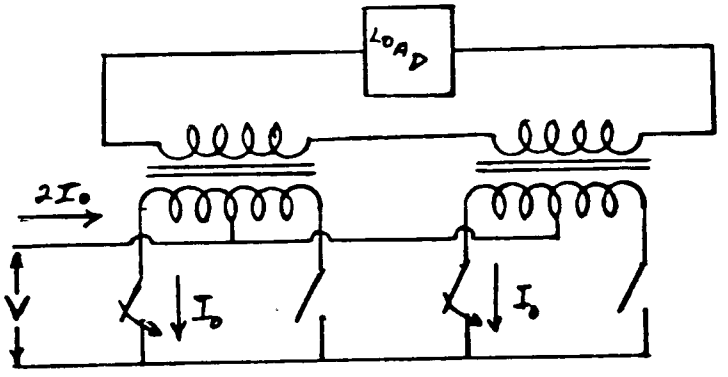


FIG 4-71 LOAD SHARING WITH SPLIT OUTPUT XFMR

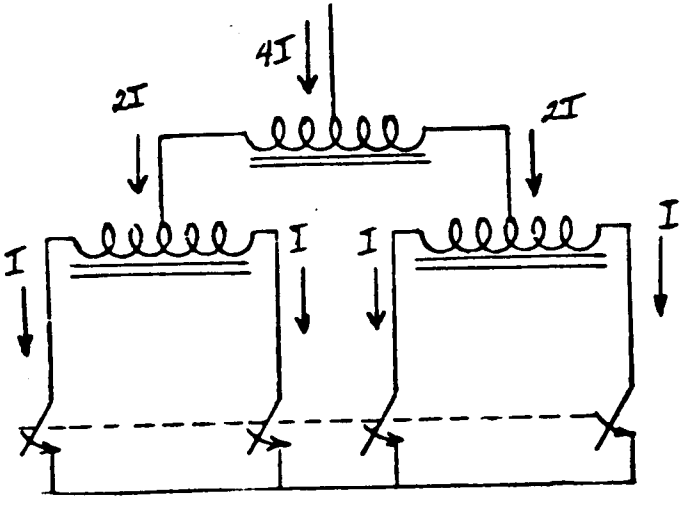


FIG 4-72 LOAD SHARING WITH CASCADED BALANCING REACTORS

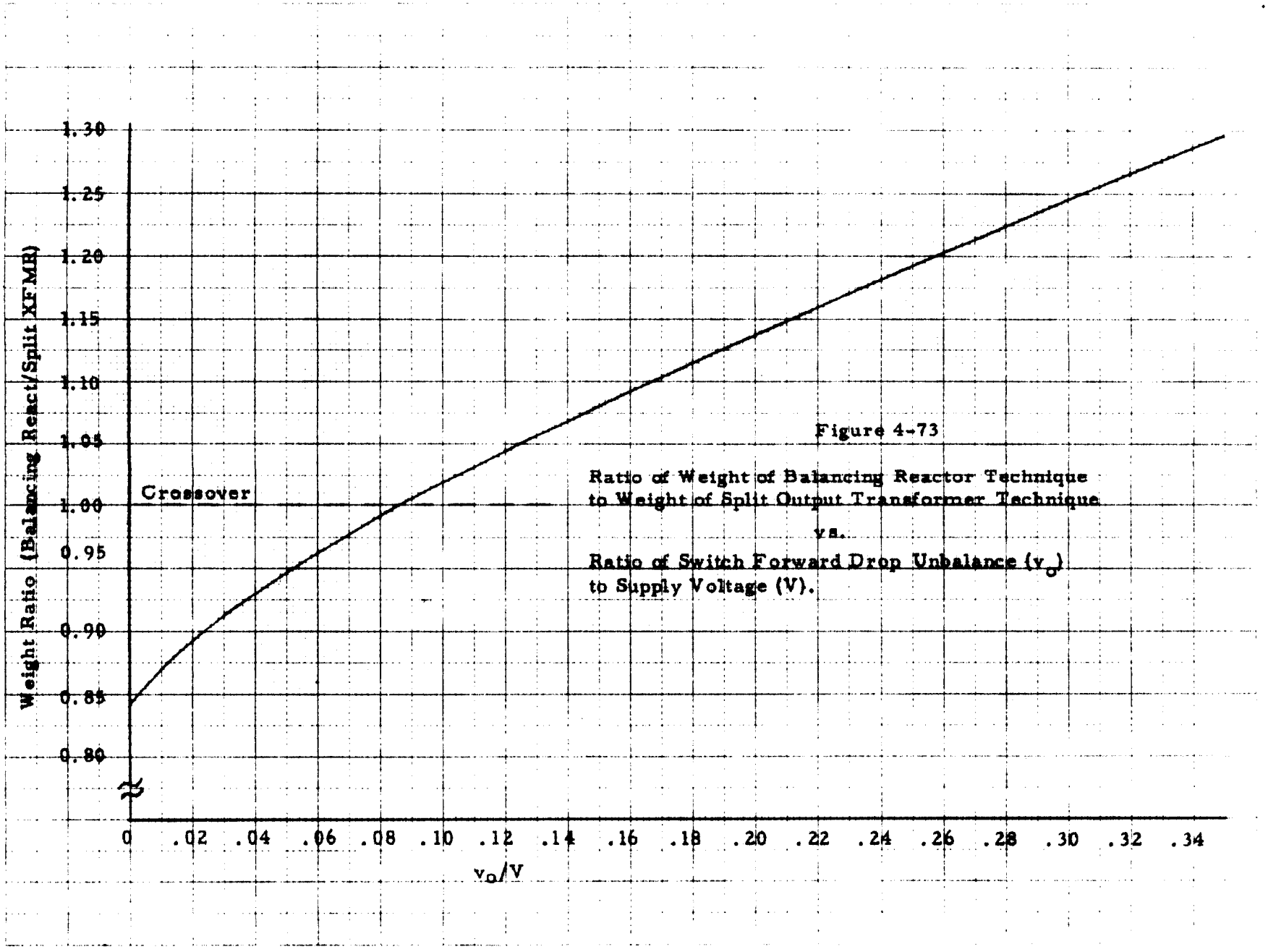


Figure 4-73

Ratio of Weight of Balancing Reactor Technique to Weight of Split Output Transformer Technique vs. Ratio of Switch Forward Drop Unbalance (v_o) to Supply Voltage (V).

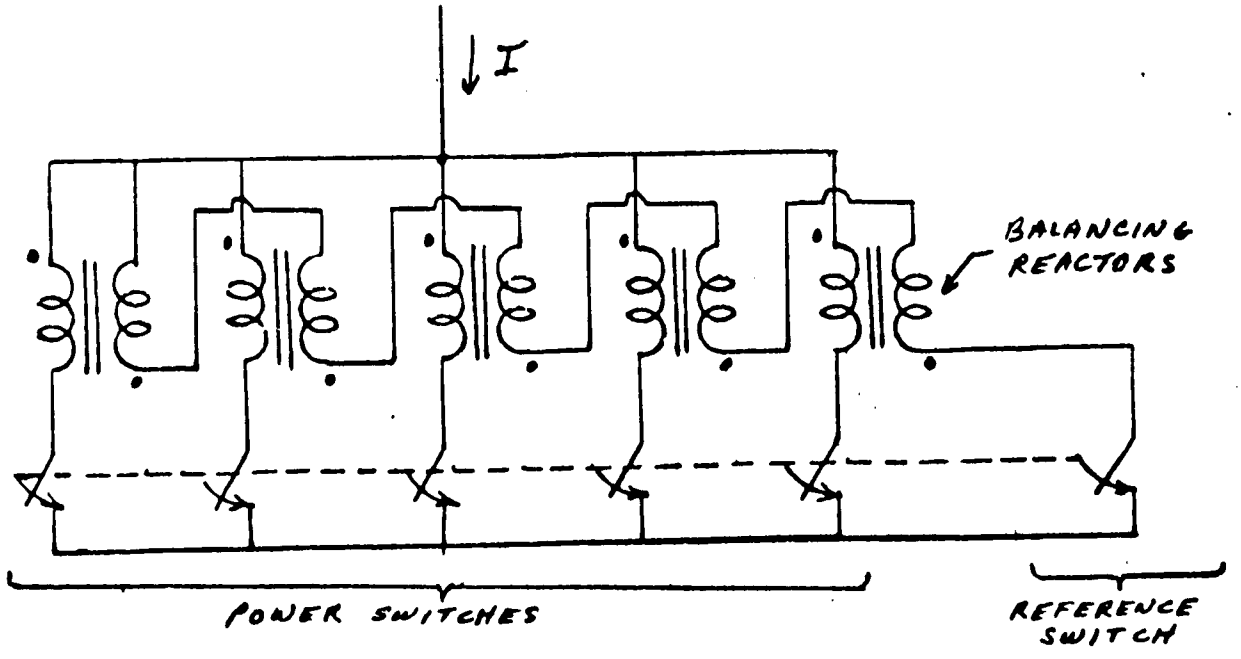


FIG. 4-74 PARALLELING WITH REFERENCE SWITCH AND BALANCING REACTORS

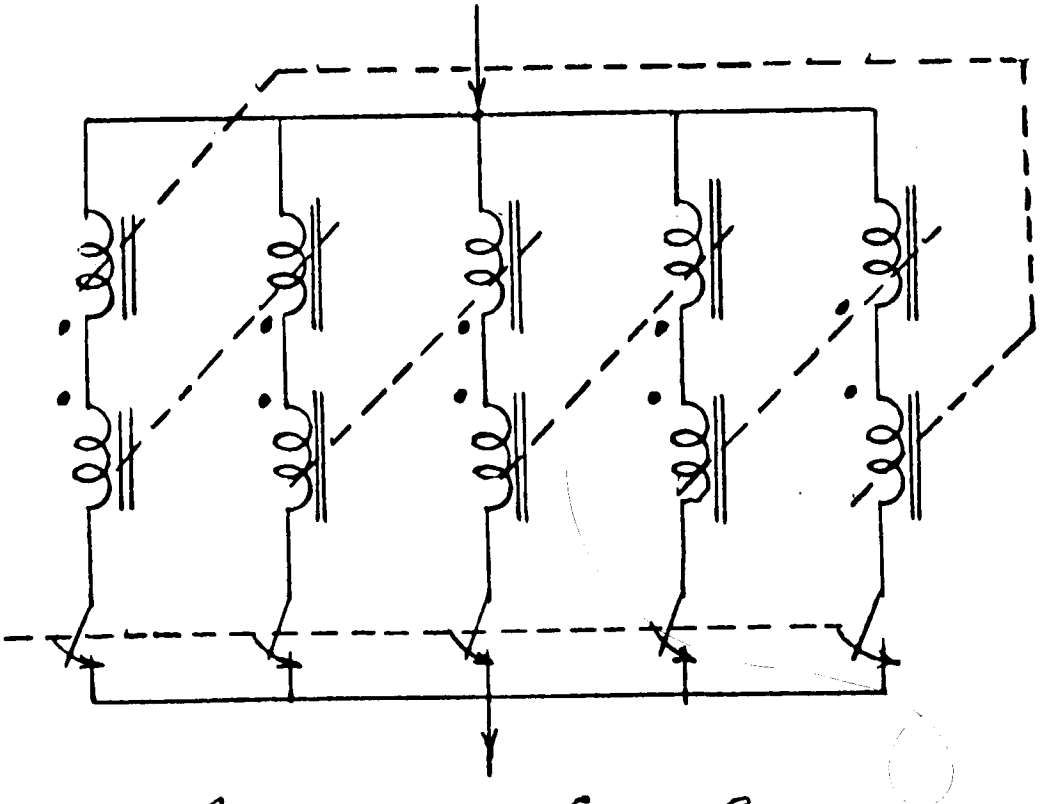
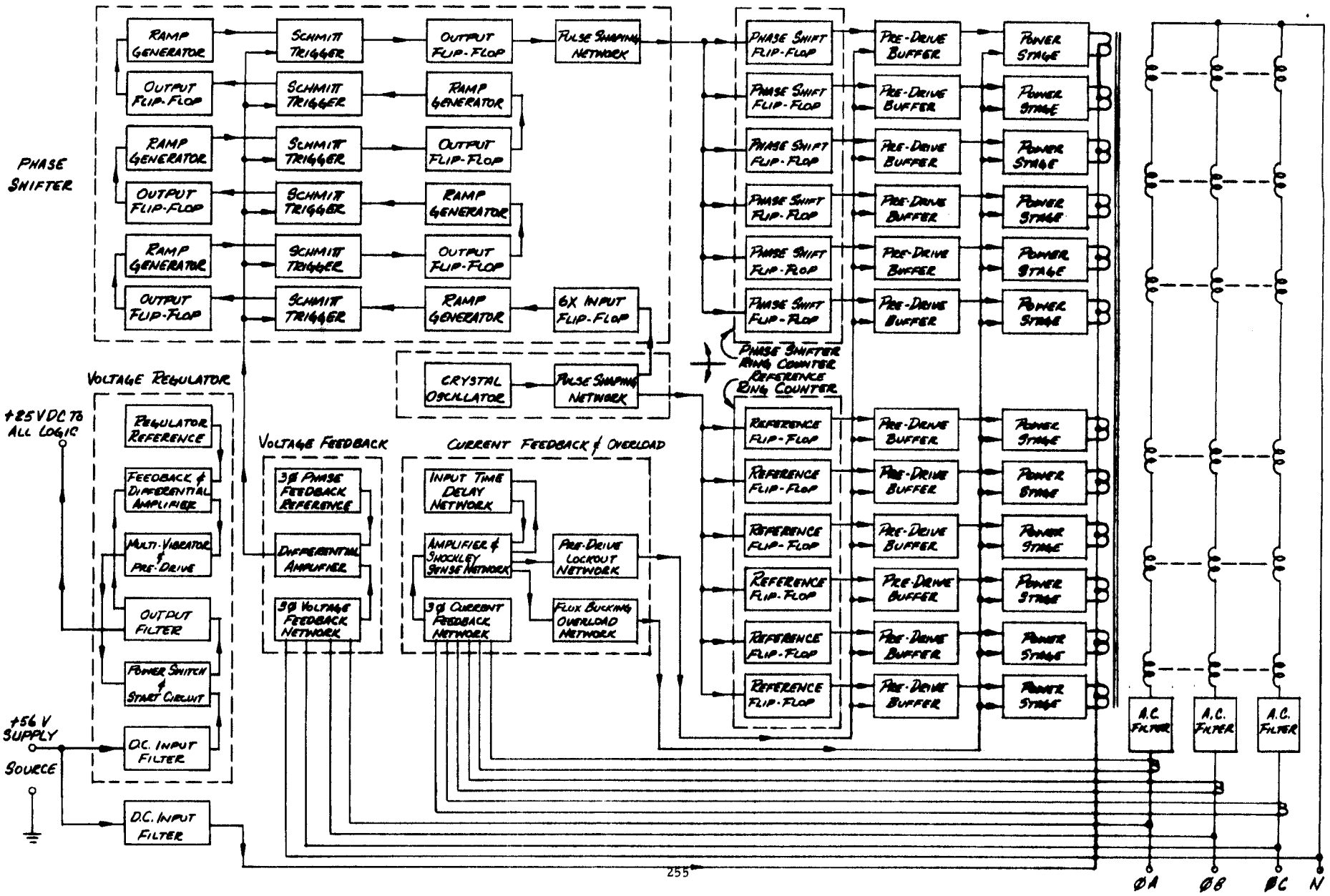


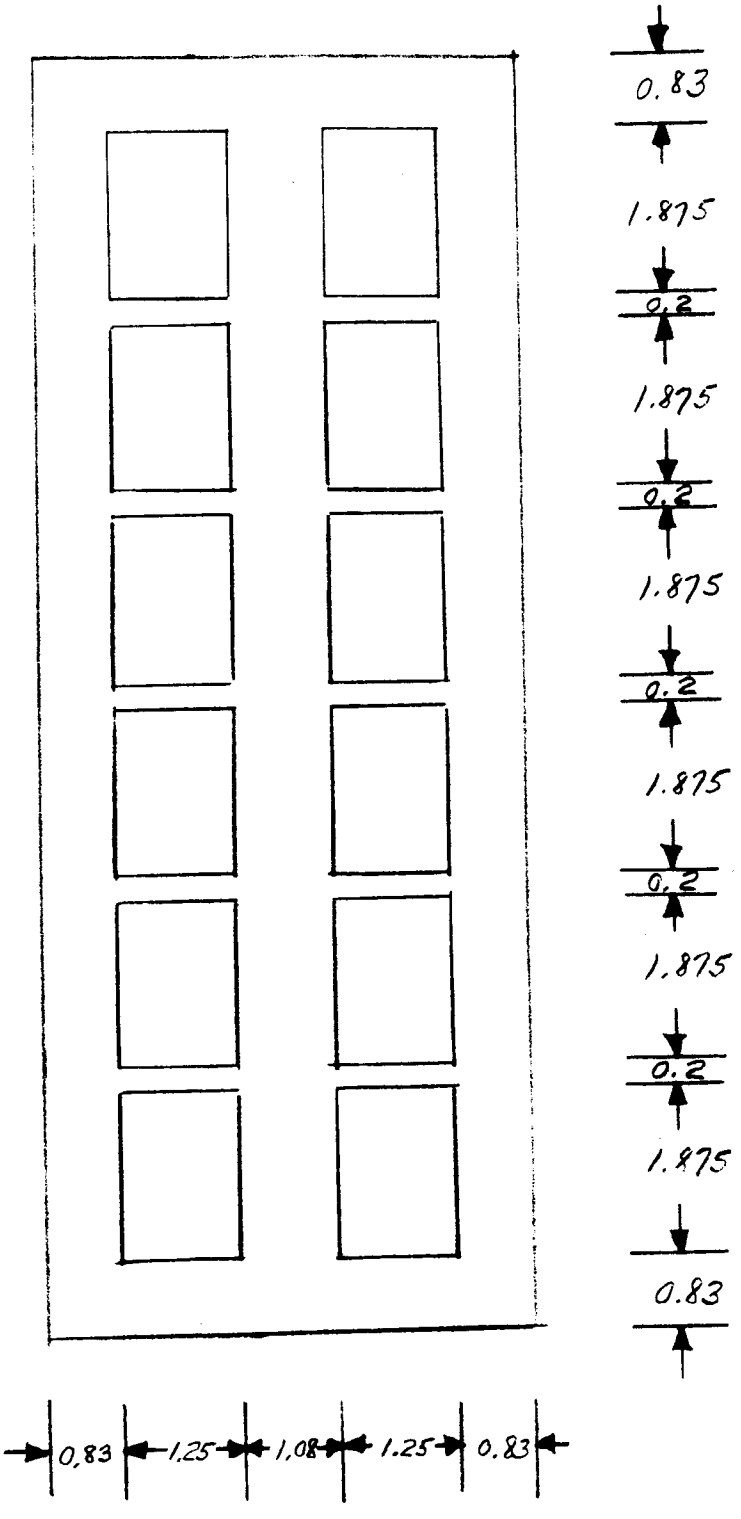
FIG 4-75 PARALLELING WITH CLOSED CHAIN OF BALANCING REACTORS

BLOCK DIAGRAM FOR 3200 CPS INVERTER

FIGURE 4-76



ALL DIMENSIONS IN INCHES.

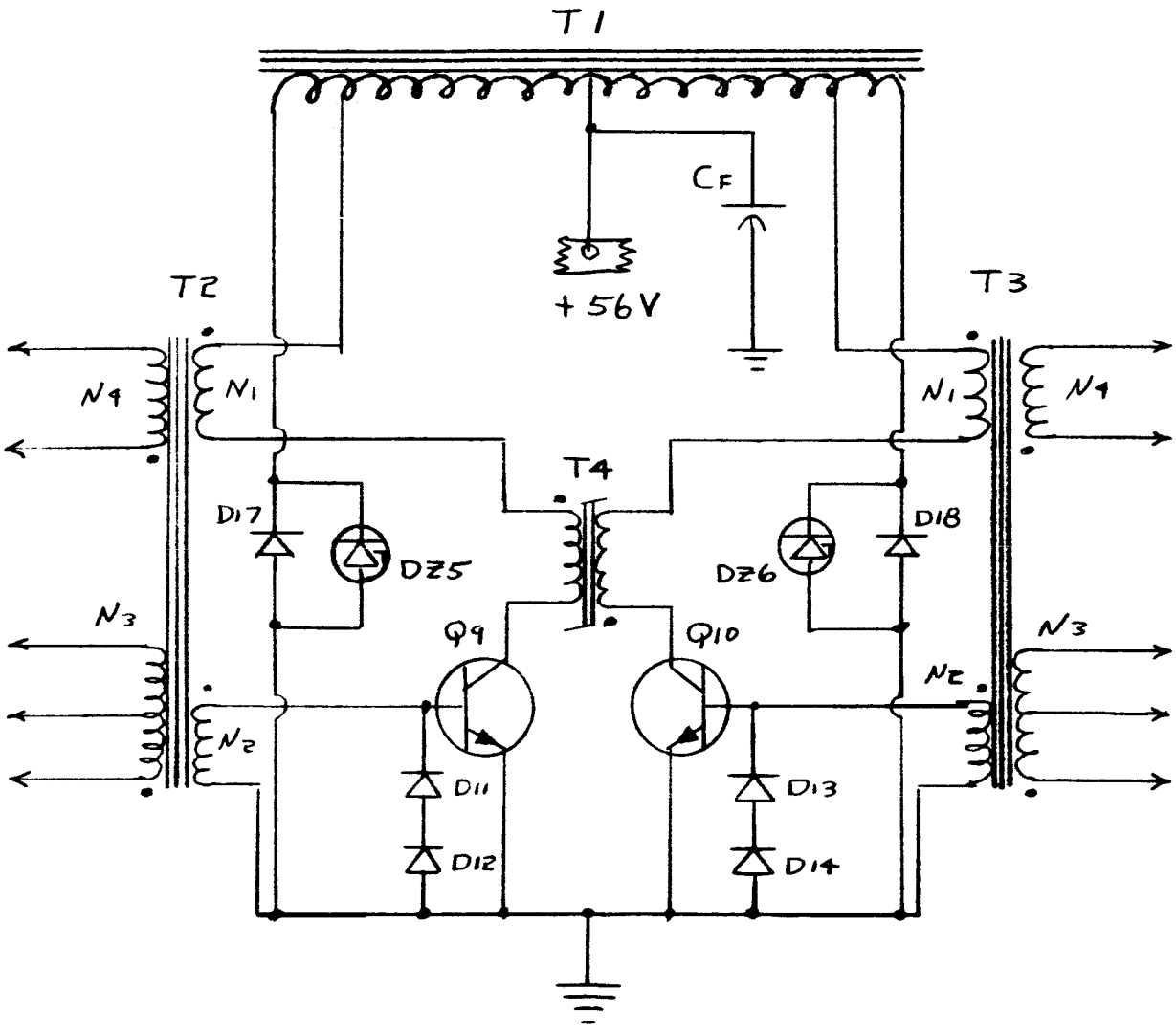


OUTPUT TRANSFORMER CORE CONFIGURATION

FIGURE 4-77

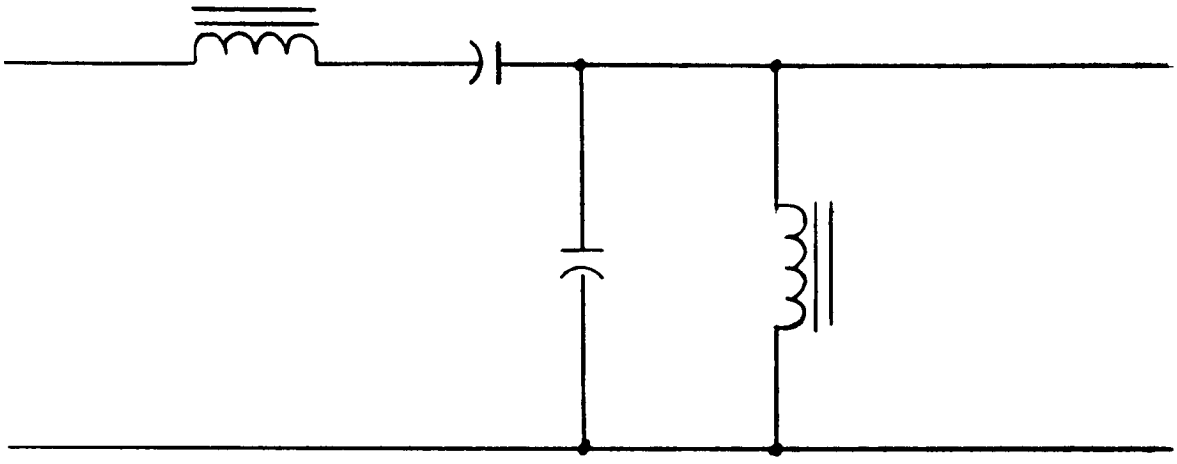
TURNS RATIOS OF DRIVE TRANSFORMERS T2 AND T3

$\frac{N2}{N1} = 10$, $\frac{N3}{N1} = 100$, $\frac{N4}{N1} = 100$



TYPICAL POWER OUTPUT STAGE

FIG. 4-78



A C FILTER

FIGURE 4-79

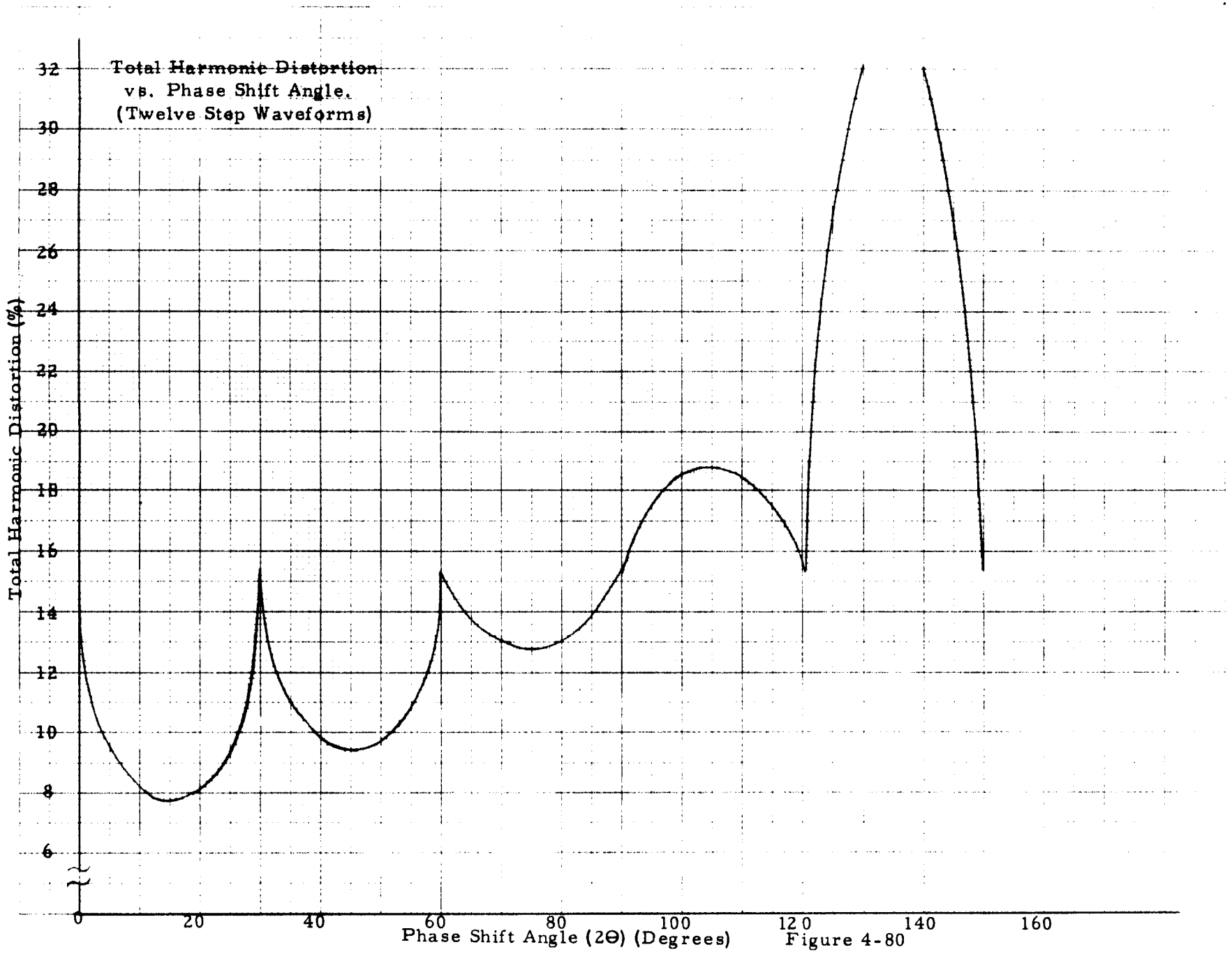

Total Harmonic Distortion
vs. Phase Shift Angle.
(Twelve Step Waveforms)
Total Harmonic Distortion (%)
32
30
28
26
24
22
20
18
16
14
12
10
8
6
0
20
40
60
80
100
120
140
160
Phase Shift Angle (2Θ) (Degrees)

Figure 4-80

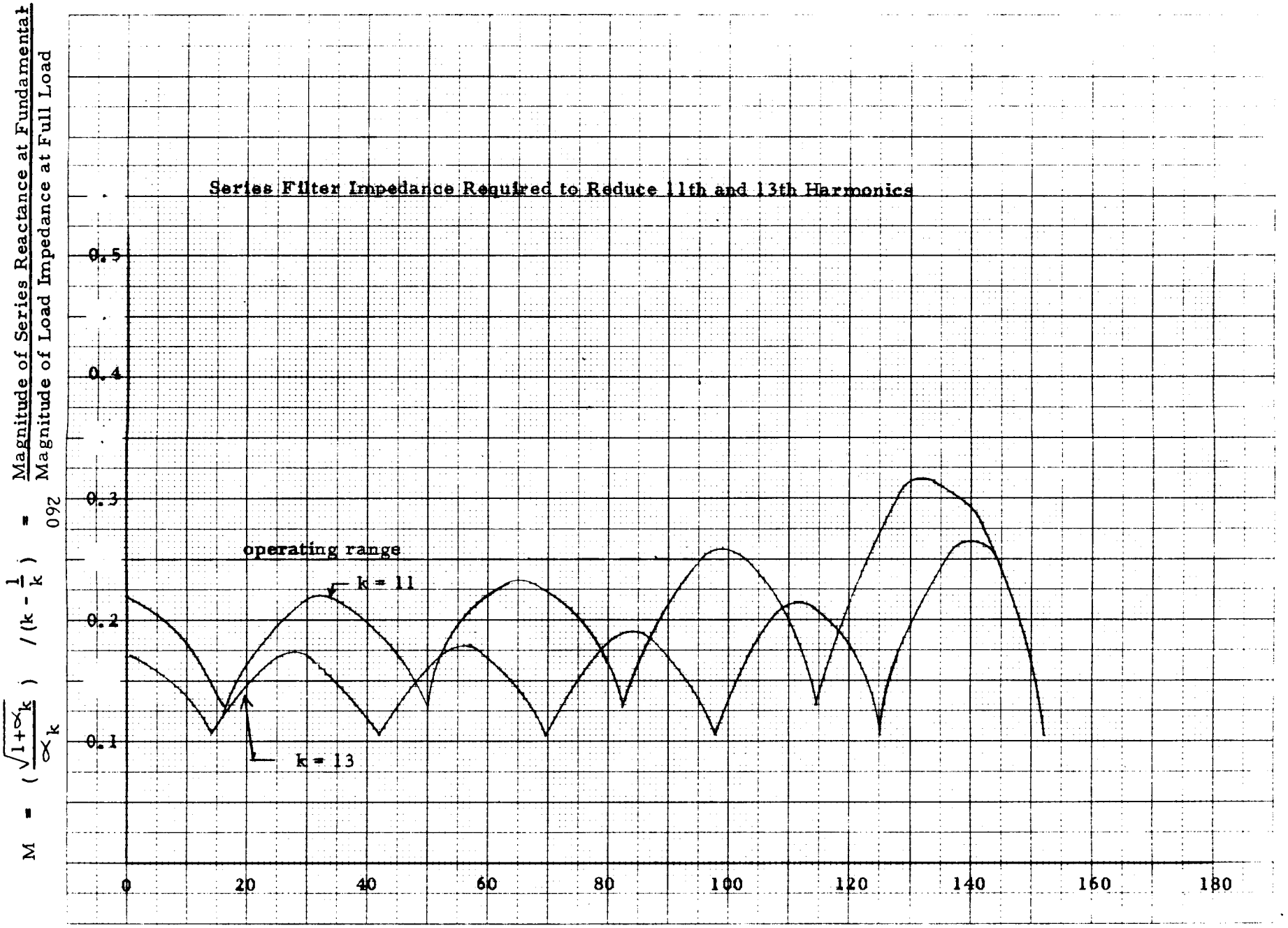
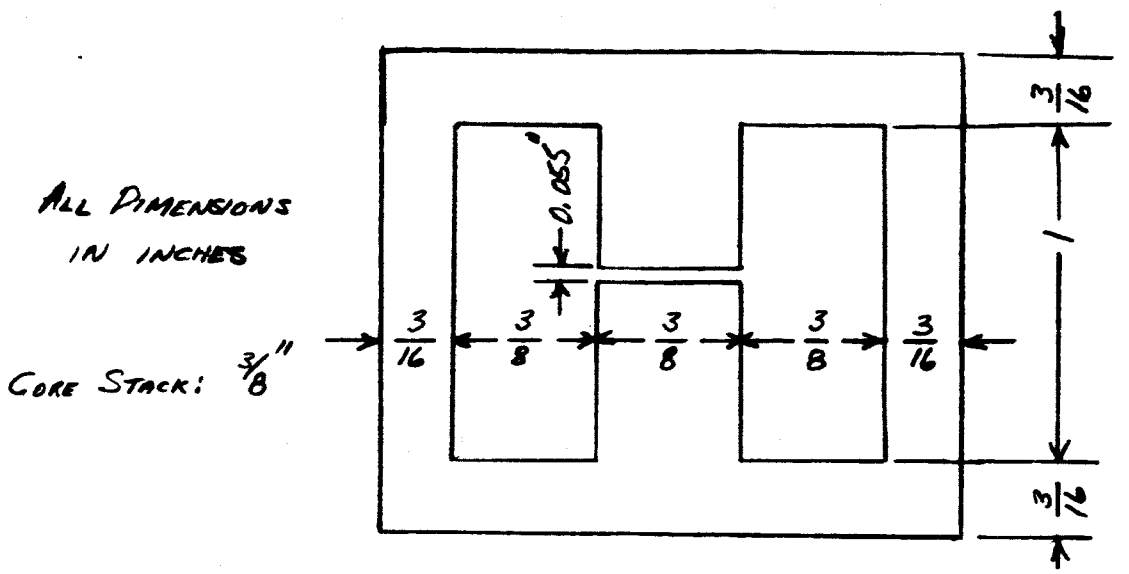
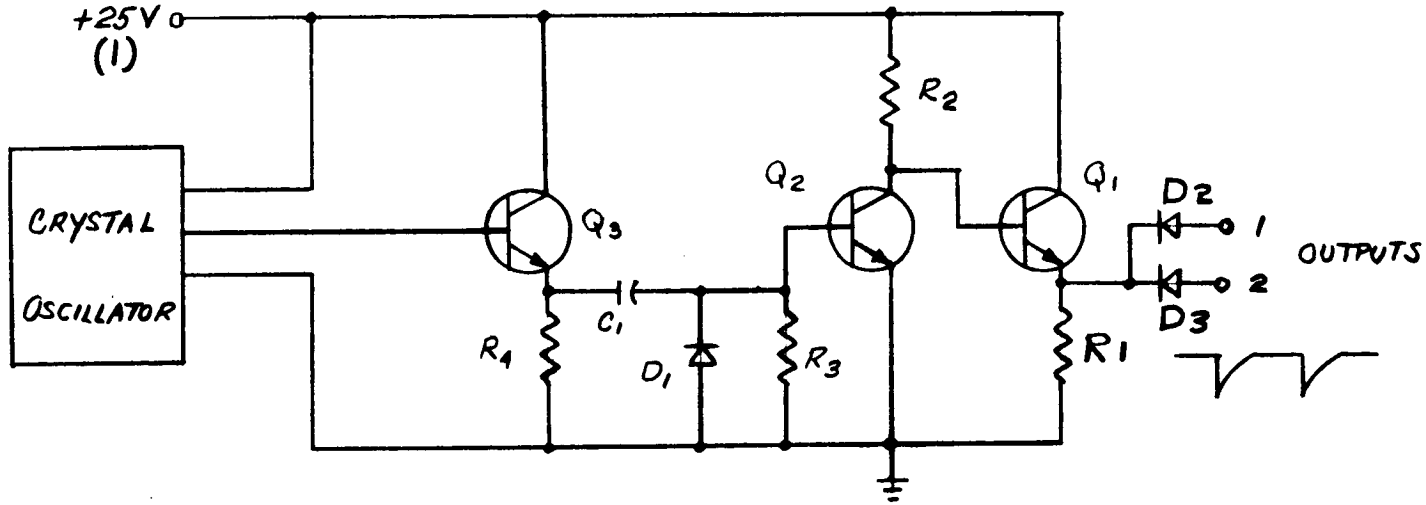

Series Filter Impedance Required to Reduce 11th and 13th Harmonics
M = (√(1+∝k / ∝k)) / (k - 1/k) = Magnitude of Series Reactance at Fundamental / Magnitude of Load Impedance at Full Load
0.5
0.4
0.3
0.2
0.1
operating range
k = 11
k = 13
0
20
40
60
80
100
120
140
160
180
Phase Displacement Between Input Multi-Stepped Waves (Degrees)

FIGURE 4-81



SERIES FILTER INDUCTOR CORE DESIGN

FIGURE 4-82



TERMINAL 1 - TO INPUT OF FLIP-FLOP FOR PHASE SHIFTING NETWORK FIGURE 4-87

TERMINAL 2 - TO FIXED REFERENCE RING COUNTER. FIGURE 4-84

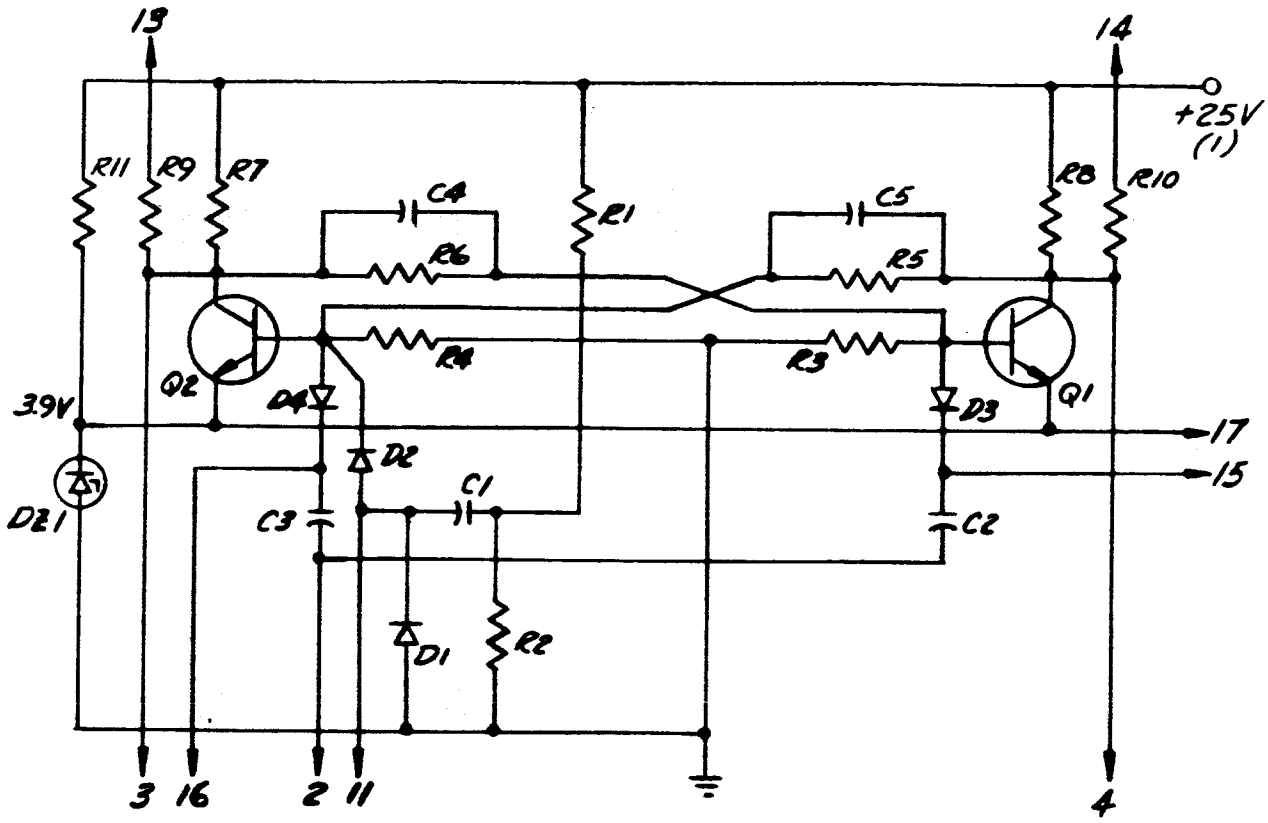
PART	VALUE	TOLERANCE
R_1	560 Ω - 1 WATT	± 5%
R_2	5.6 K - ½ WATT	± 5%
R_3	6.8 K - ½ WATT	± 5%
R_4	1 K - ½ WATT	± 5%
C_1	0.001 μf - 300 WVDC	± 10%
D_1, D_2, D_3	1N916	
Q_1, Q_2, Q_3	2N697	

CLOCK - DELTA F - DFO-10
FREQ. = 38.4 KC SQUARE WAVE
5 VOLT OUTPUT WITH 130 nSEC RISE TIME.

ALL RESISTORS ARE COMPOSITION TYPE

CLOCK OSCILLATOR AND PULSE SHAPER
FIGURE 4-83

TYPICAL FLIP-FLOP FOR BOTH RING COUNTERS (SIX REQUIRED FOR EACH COUNTER)



TERMINAL 2 PULSE SIGNAL FROM CLOCK OSCILLATOR AND PULSE SHAPER. FIGURE 4-83

TERMINAL 3 AND 4 REFERENCE AND PHASE SHIFTER RING COUNTER OUTPUTS TO THE PRE-DRIVE BUFFER STAGES FIGURE 4-90

TERMINALS 13 AND 14 ARE STEERING SIGNALS APPLIED FROM ONE FLIP-FLOP TO ANOTHER IN THE RING COUNTER. FIGURE 4-86

TERMINALS 15 AND 16 ARE THE PLACES WHERE THE STEERING SIGNALS FROM TERMINALS 13 AND 14 ARE APPLIED. 4-86

TERMINAL 11 IS USED TO SET THE RING COUNTER IN THE PROPER MODE WHEN +25V IS APPLIED. FIGURE 4-86

TERMINAL 17 SUPPLIES +3.9VDC TO ALL THE FLIP-FLOPS IN THE REFERENCE AND PHASE SHIFTING RING COUNTERS

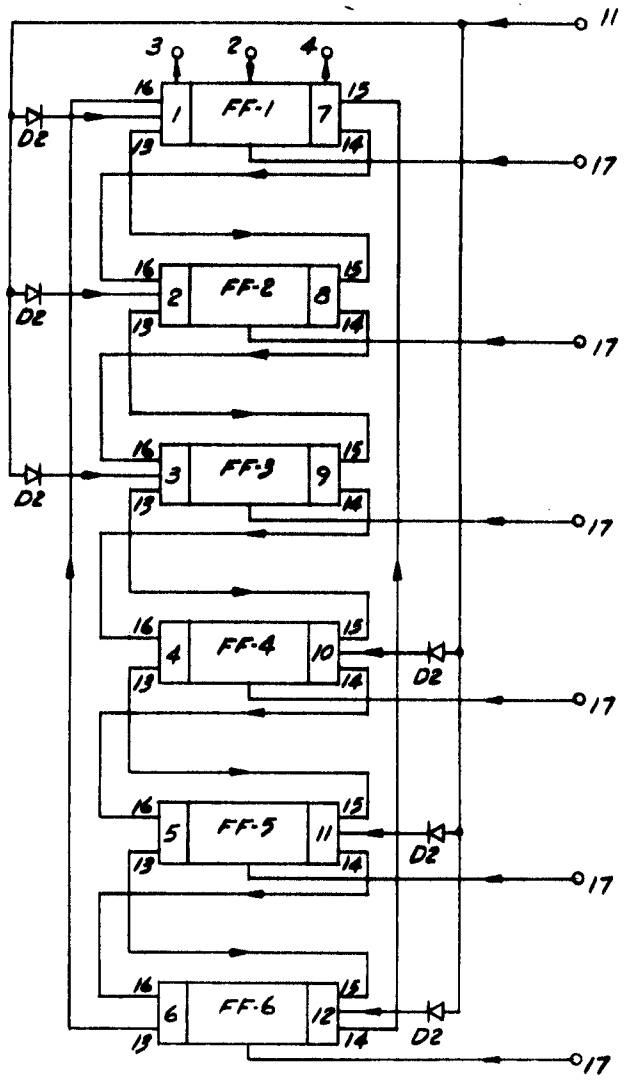
FIGURE 4-84

PARTS LIST FOR TYPICAL FLIP-FLOP FOR BOTH RING COUNTERS (SIX REQUIRED FOR EACH COUNTER)

Part	Value	Tolerance
R1	3.3K - 1/2 watt - composition	±5%
R2	120K - 1/2 watt - composition	±5%
R3, R4	22K - 1/2 watt - composition	±5%
R5, R6	15K - 1 watt - composition	±5%
R7, R8	2.2K - 1 watt - composition	±5%
R9, R10	22K - 1 watt - composition	±5%
R11	270Ω - 10 watt - wire wound	±1%
D1, D2, D3, D4	1N 458A	
DZ1	1N 1518 - 3.9 V DC	±10%
Q1, Q2	2N 657A	
C1	0.22μF - 400 WVDC	±10%
C2, C3	0.001μF - 300 WVDC	±10%
C4, C5	0.001μF - 300 WVDC	±10%

FIGURE 4-85

TYPICAL FLIP-FLOPS RING CONTAINING SIX FLIP-FLOPS WHOSE OUTPUTS ARE STEERED WHICH ARE USED FOR BOTH THE REFERENCE AND PHASE SHIFTER RING COUNTERS



TERMINAL 2 PULSE SIGNAL FROM CLOCK OSCILLATOR AND PULSE SHAPER. FIGURE 4-83

TERMINALS 3 AND 4 REFERENCE AND PHASE SHIFTER RING COUNTER OUTPUTS TO THE PRE-DRIVE BUFFER STAGES. FIGURE 4-90

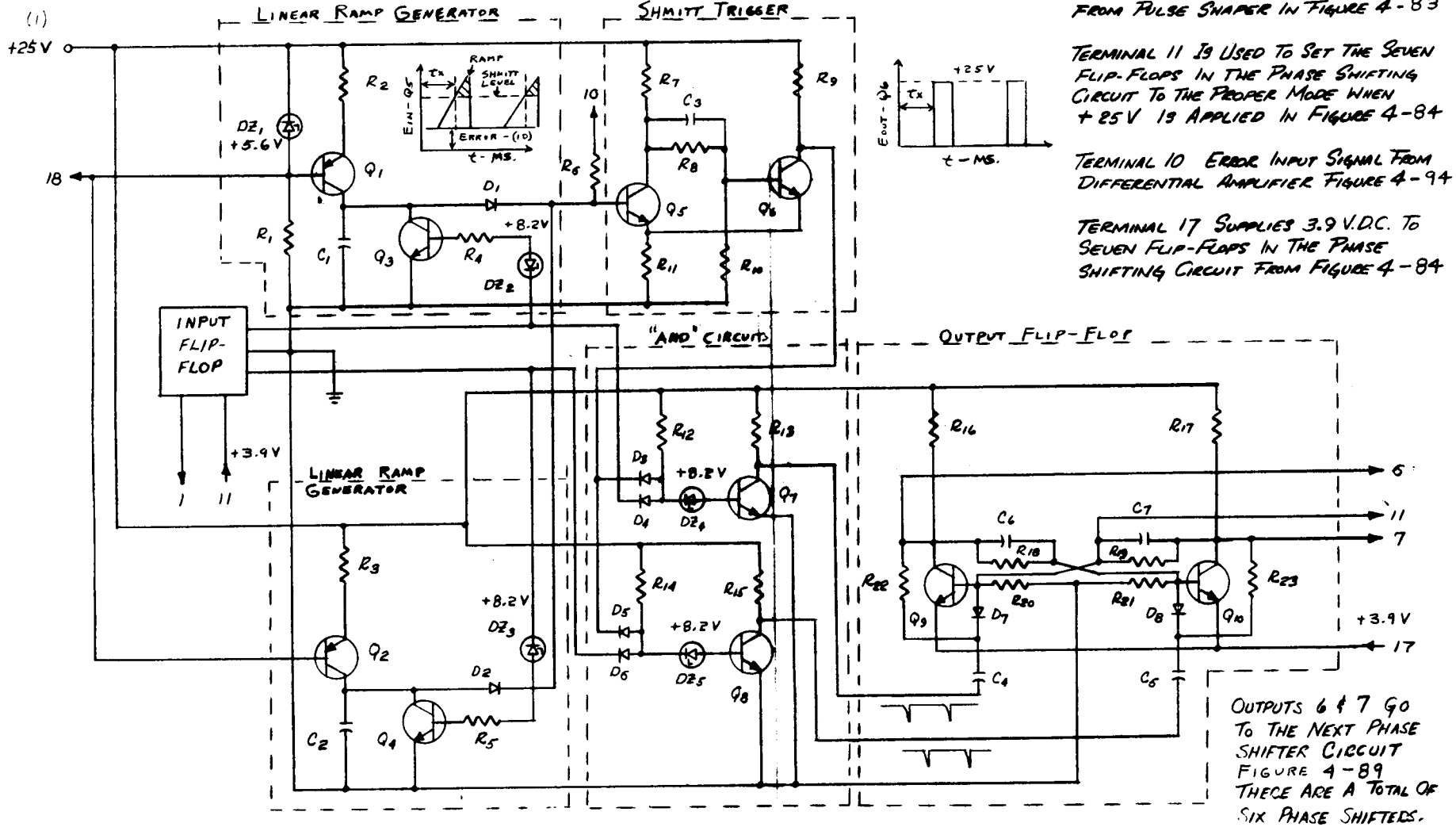
TERMINALS 13 AND 14 ARE STEERING SIGNALS APPLIED FROM ONE FLIP-FLOP TO ANOTHER IN THE RING COUNTER. FIGURE 4-84

TERMINALS 15 AND 16 ARE THE PLACES WHERE THE STEERING SIGNALS FROM TERMINALS 13 AND 14 ARE APPLIED

TERMINAL 11 IS USED TO SET THE RING COUNTER IN THE PROPER MODE WHEN +25V IS APPLIED FIGURE 4-84

TERMINAL 17 SUPPLIES +3.9VDC TO ALL THE FLIP-FLOPS IN THE REFERENCE AND PHASE SHIFTING RING COUNTERS.

FIGURE 4-86



TERMINAL 1 INPUT TRIGGER SIGNAL FROM PULSE SHAPER IN FIGURE 4-83

TERMINAL 11 IS USED TO SET THE SEVEN FLIP-FLOPS IN THE PHASE SHIFTING CIRCUIT TO THE PROPER MODE WHEN +25 V IS APPLIED IN FIGURE 4-84

TERMINAL 10 ERROR INPUT SIGNAL FROM DIFFERENTIAL AMPLIFIER FIGURE 4-94

TERMINAL 17 SUPPLIES 3.9 V.D.C. TO SEVEN FLIP-FLOPS IN THE PHASE SHIFTING CIRCUIT FROM FIGURE 4-84

OUTPUTS 6 & 7 GO TO THE NEXT PHASE SHIFTER CIRCUIT FIGURE 4-89 THERE ARE A TOTAL OF SIX PHASE SHIFTERS.

PHASE SHIFTING CIRCUIT

FIGURE 4-87

PARTS LIST FOR PHASE SHIFTING CIRCUIT

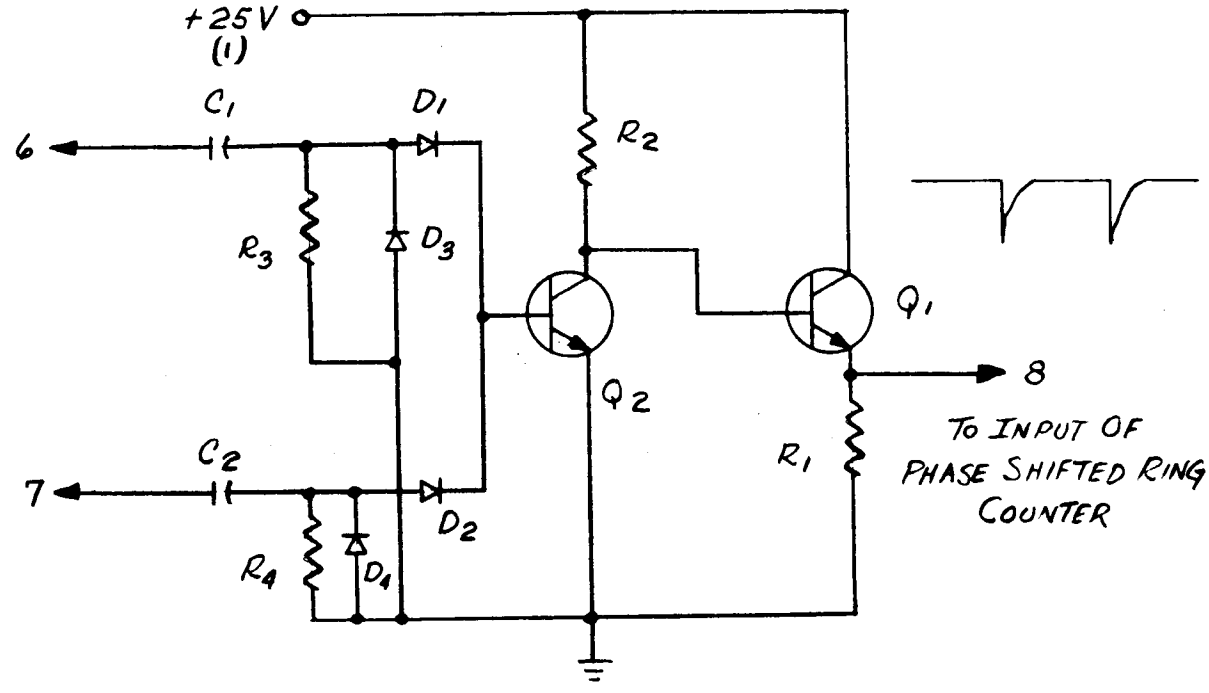
Part No.	Value	Tolerance
R1	1K - 1W Composition	±5%
R2 - R3	10K - 1/2W metal film	±1%
R4 - R5	8.2K - 1/2W Composition	±5%
R6	1K - 1/2W metal film	±1%
R7	2.7K - 1/2W metal film	±1%
R8	15K - 1/2W Composition	±5%
R9	4.7K - 1W Composition	±5%
R10	8.2K - 1/2W Composition	±5%
R11	390Ω - 1/2W metal film	±1%
R12 - R14	22K - 1/2W Composition	±5%
R13 - R15	4.7K - 1W Composition	±5%
R16 - R17	2.2K - 1W Composition	±5%
R18 - R19	15K - 1W Composition	±5%
R20 - R21	22K - 1/2W Composition	±5%
R22 - R23	22K - 1W Composition	±5%
C1 - C2	1000 μμfd - 300 WVDC	±1%
C3	20 μμfd - 300 WVDC	±10%
C6 - C7	200 μμfd - 300 WVDC	±10%
C4 - C5	100 μμfd - 300 WVDC	±10%
D1 - D6	1N916	
D7 - D8	1N458A	
DZ1	1N752A - 5.6 V	±5%
DZ2 - DZ3	1N756A - 8.2 V	±5%
DZ4 - DZ5	1N756A - 8.2 V	±5%
Q1 - Q2	2N1132	Matched
Q3 - Q10	2N697	

Input flip flop represented by block has the same components as output flip flop except the following:

C6 - C7	100 μμfd - 200 WVDC	±10%
C4 - C5	50 μμfd - 200 WVDC	±10%

FIGURE 4-88

OUTPUT PULSE SHAPING CIRCUIT TO PHASE SHIFTED RING COUNTER FROM LAST PHASE SHIFTING FLIP-FLOP

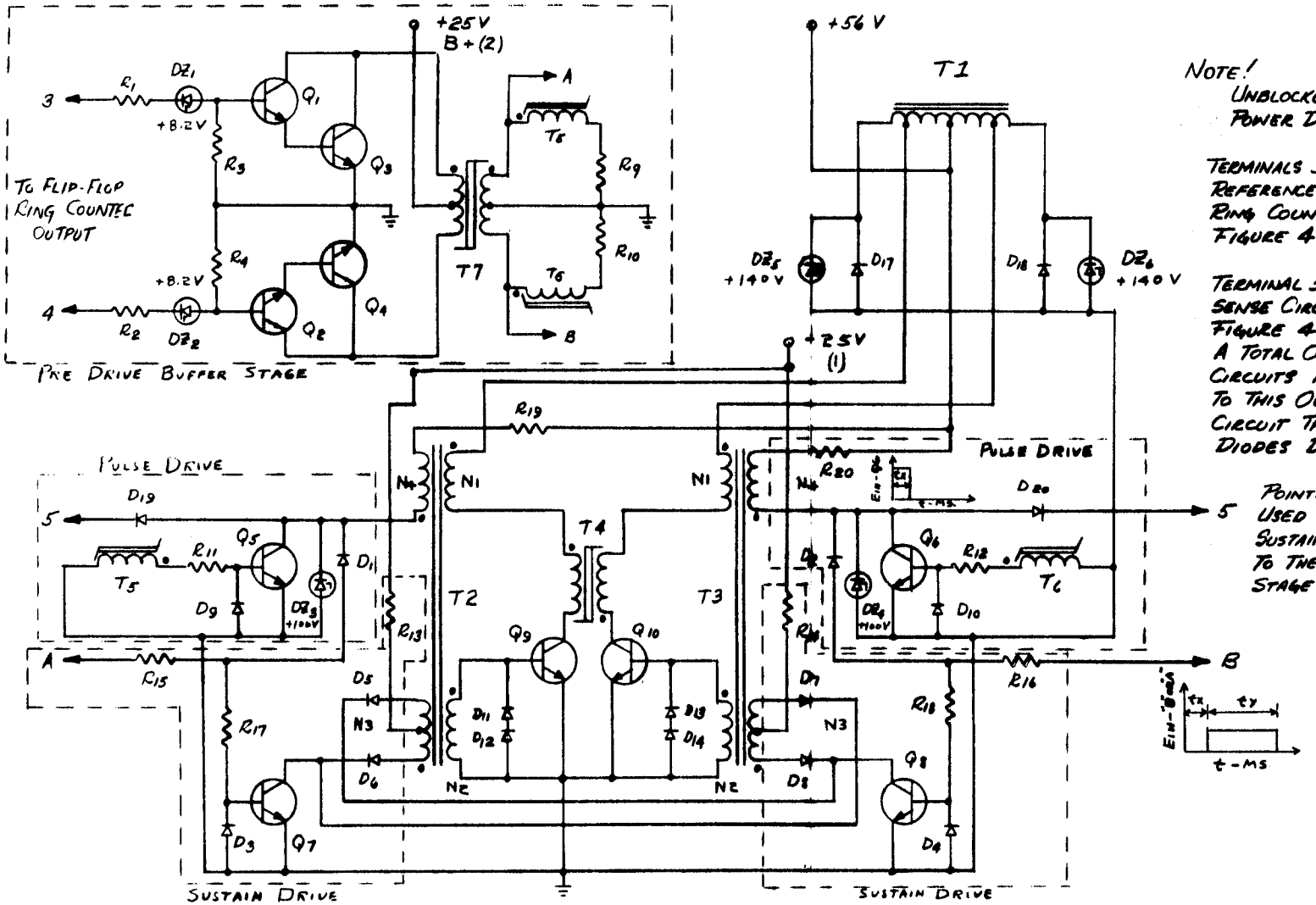


PART	VALUE	TOLERANCE
R_1	560 Ω - 1 WATT - COMPOSITION	± 5%
R_2	5.6 K - ½ WATT - "	± 5%
R_3, R_4	6.8 K - ½ WATT - "	± 5%
D_1, D_2	1N 916	
D_3, D_4	1N 458 A	
C_1, C_2	0.001 μf - 300 WVDC	± 10%
Q_1, Q_2	2N 697	

TERMINAL 6 - FROM OUTPUT OF LAST PHASE SHIFTING FLIP-FLOP FIGURE 4-87

TERMINAL 7 - FROM OUTPUT OF LAST PHASE SHIFTING FLIP-FLOP FIGURE 4-87

FIGURE 4-89



TYPICAL POWER DRIVE CIRCUIT

FIGURE 4-90

PARTS LIST FOR POWER DRIVE CIRCUIT AND PRE-DRIVE STAGE

Part	Value	Tolerance
$R_1 = R_2$	8.2K - 1/2W Composition	±5%
$R_3 = R_4$	22K - 1/2W Composition	±5%
$R_9 = R_{10}$	270Ω 10W Wire Wound	±5%
$R_{11} = R_{12}$	47Ω - 1/2W Composition	±5%
$R_{13} = R_{14}$	130Ω - 10W Wire Wound	±5%
$R_{15} = R_{16}$	1.5K - 1W Composition	±5%
$R_{17} = R_{18}$	330Ω - 1/2W Composition	±5%
$R_{19} = R_{20}$	60 Ω - 25W non inductive Wire Wound	±1%
D1 → D10	1N458A	
D11 → D14	379A (WX)	
D17 - D18	1N1186A	
D19 = D20	1N1615	
DZ1 = DZ2	1N756 - 8.2 V	± 10%
DZ3 = DZ4	1N3340B - 100 V	± 5%
DZ5 = DZ6	1N3345 - 140 V	± 10%
Q1 → Q4	2N657A	
Q5 = Q6	2N1050A	
Q7 = Q8	2N657A	
Q9 = Q10	STC 2501	

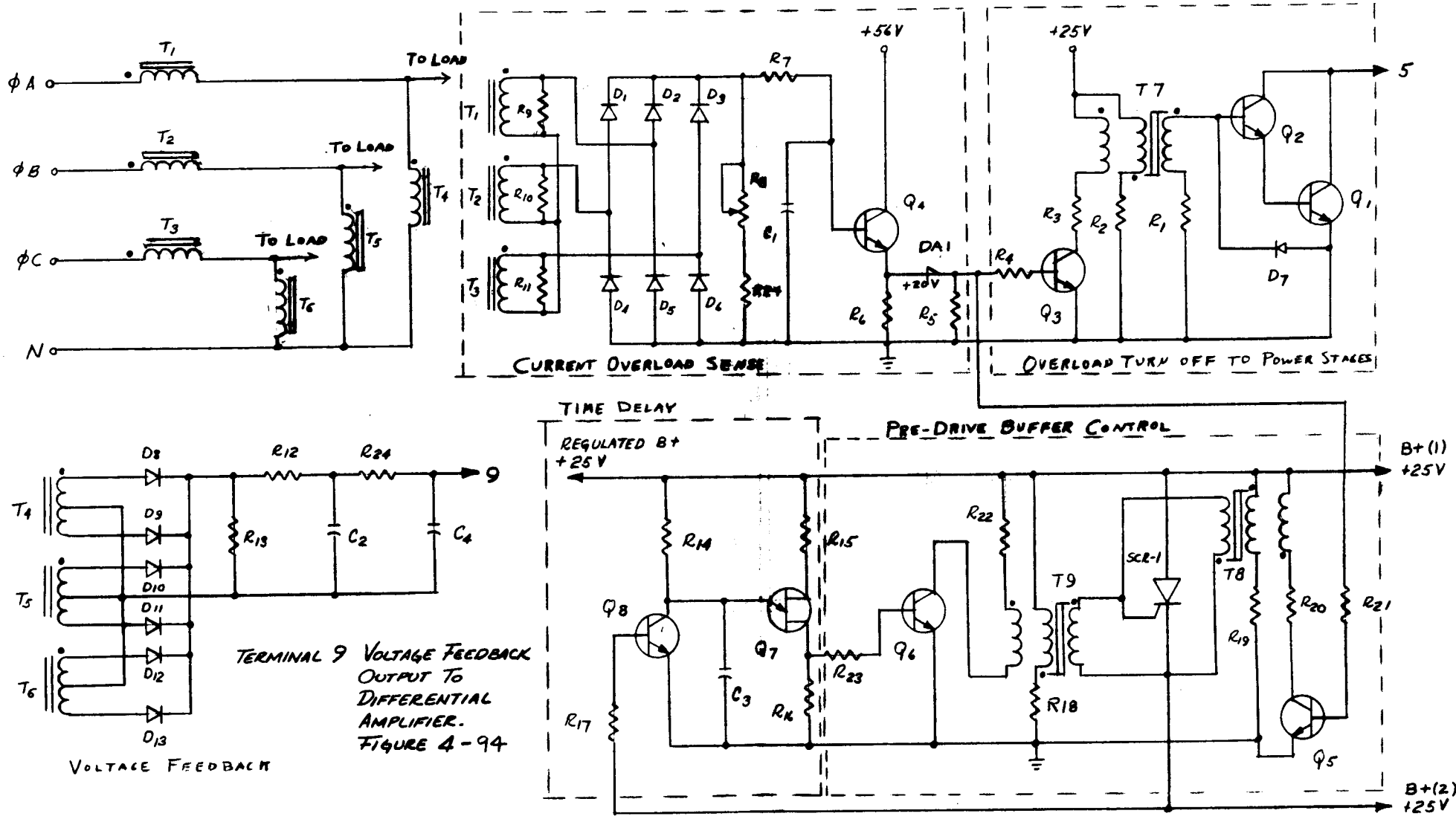
FIGURE 4-91

PARTS LIST (Continued)

T_1 (See Design II - Table 4-6)

T_2 - T_3	Core = AM-1 (Arnold) 1 MIL Silectron
	N_P = 100 turns #30 DFV wire
	N_{S1} = 50/50 turns (Bifilar) #30 DFV wire
	N_{S2} = 10 turns #20 DFV wire
	N_{S3} = 1 turn #10 DFV wire
T_4	Core = 52033 - 1S (Magnetics)
	N_P = N_S = 9 turns #12 DFV wire
T_5 - T_6	Core = 80023 - 1/8A
	N_P = 84 turns No. 30 DFV wire
	N_S = 42 turns No. 30 DFV wire
T_7	Core 50002 - 1A
	N_P = 420 turns No. 30 DFV wire
	Tapped at 210 turns
	N_S = 324 turns No. 30 DFV wire
	Tapped at 162 turns

FIGURE 4-91



OVERLOAD SENSE AND FEEDBACK CIRCUIT

FIGURE 4-92

PARTS LIST FOR OVERLOAD SENSE AND FEEDBACK CIRCUIT

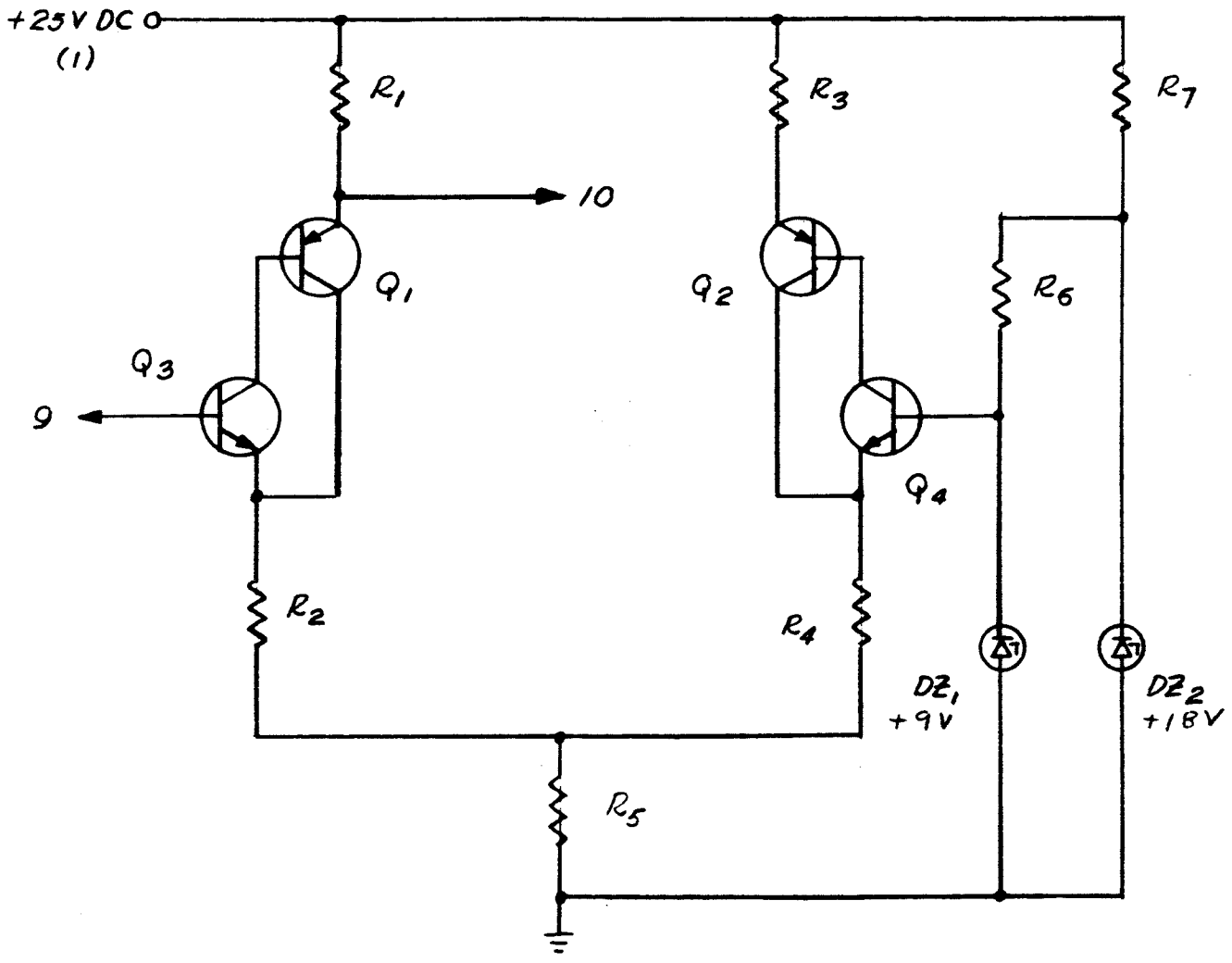
Part	Value		Tolerance
R1	33 1/2W	Composition	±5%
R2	4.7K 1W	Composition	±5%
R3	470Ω - 2W	Composition	±5%
R4	5.6K 1/2W	Composition	±5%
R5	2K - 1/2W	Composition	±5%
R6	3.9 - 1W	Composition	±5%
R7	1K - 1/2W	Composition	±5%
R8	5K - 1W Potentiometer		±10%
R9 → R11	200Ω - 2W	Composition	±1%
R12 - R24	1.5K - 1/2W	Composition	±5%
R13	2.2K - 1W	Composition	±5%
R14	29K - 1/2W	Composition	±5%
R15	1K - 1/2W	Composition	±5%
R16	100Ω - 1/2W	Composition	±5%
R17	22K - 1/2W	Composition	±5%
R18 - R19	4.7K - 1W	Composition	±5%
R20	120Ω - 5W	Wire-Wound	±5%
R21	1.5K - 1/2W	Composition	±5%
R22	240Ω - 2W	Composition	±5%
R23	1K - 1/2W	Composition	±5%
R24	2K - 1W	Composition	±5%
SCR1	241 WA - WM		Westinghouse
D1 - D13	1N458A		
DA1	4E20M-8		20V ±4V
C1	0.1 µfd - 200 WVDC		±10%
C2	.05 µfd - 200 WVDC		±10%
C3	47 µfd - 35 WVDC		±10%
C4	.05 µfd - 200 WVDC		±10%
Q1	STC 1739		
Q2	2N1486		
Q3 - Q6	2N657A		
Q7	2N491		
Q8	2N657A		

FIGURE 4-93

PARTS LIST FOR OVERLOAD SENSE AND FEEDBACK CIRCUIT (Continued)

Part	Value	Tolerance
T1 - T3	50061 - 1D	
	N_P - 1 turn	
	N_S - 1868 turns	No. 30 DFV
T4 - T6	50000 - 1A	
	N_P - 876 turns	No. 40 DFV
	N_S - 132 turns	No. 36 DFV
	Tapped at 66 turn	
T7	80524 1/4A (MA)	
	N_P - 120 turns	No. 30 DFV
	N_S - 50 turns	No. 30 DFV
	N_{reset} - 124 turns	No. 40 DFV
T8	31Z394	Sprague
T9	31Z294	Sprague

FIGURE 4-93



TERMINAL 9 FROM VOLTAGE FEEDBACK OUTPUT. FIGURE 4-92

TERMINAL 10 ERROR SIGNAL FROM DIFFERENTIAL AMPLIFIER TO THE INPUT OF THE SCHMITT TRIGGERS FOR THE SIX PHASE SHIFTING NETWORKS. FIGURE 4-87

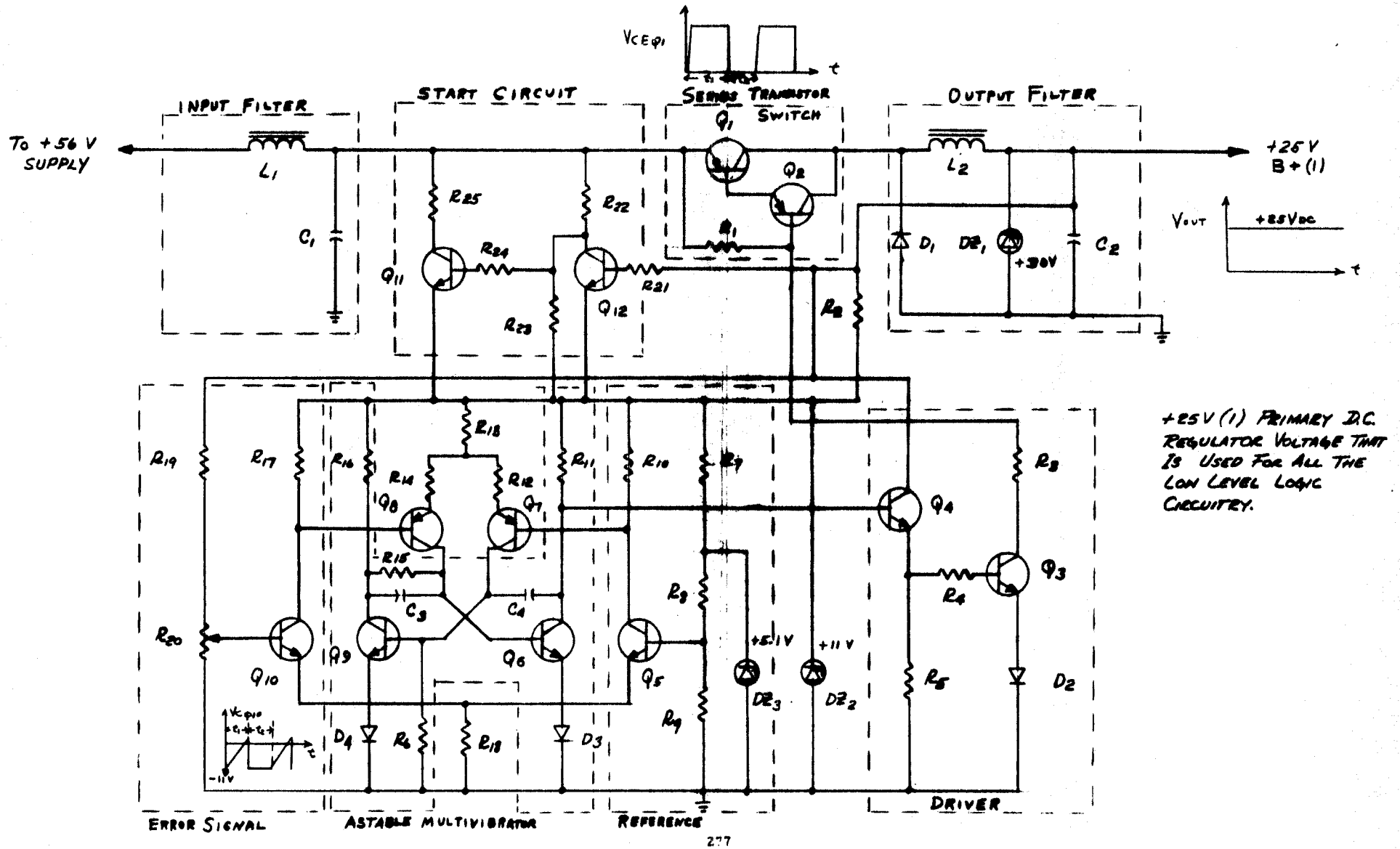
DIFFECENTIAL AMPLIFIER FEEDBACK CIRCUIT

FIGURE 4-94

PARTS LIST FOR DIFFERENTIAL AMPLIER FEEDBACK CIRCUIT

Part	Value		Tolerance
R1	15K	metal film	±1%
R2	300Ω	metal film	±1%
R3	15K	metal film	±1%
R4	300Ω	metal film	±1%
R5	3K	metal film	±1%
R6	900Ω	metal film	±1%
R7	400Ω	metal film	±1%
Q1	2N1132		
Q2	2N1132		
Q3	2N657A	(matched for V_{BE} characteristic)	
Q4	2N657A		
DZ1	1N938B		9V ±5%
DZ2	1N3026B		18V ±5%

FIGURE 4-95



+25V (1) PRIMARY D.C. REGULATOR VOLTAGE THAT IS USED FOR ALL THE LOW LEVEL LOGIC CIRCUITRY.

INPUT VOLTAGE REGULATOR (200 WATT CAPACITY)

FIGURE 4-96

PARTS LIST FOR 200 WATT VOLTAGE REGULATOR

Part No.	Value	Tolerance
R1	270Ω 1/2W Composition	±5%
R2	470Ω 1W Composition	±5%
R3	510Ω 10W Wire Wound	±5%
R4	2.2K 1/2W Composition	±5%
R5	5.6K 1/2W Composition	±5%
R6	47K 1/2W Composition	±5%
R7	680Ω 1/2W Composition	±5%
R8	1.8K 1/2W metal film	±1%
R9	3.3K 1/2W metal film	±1%
R10 = R17	10K 1/2W Composition	±5%
R11 = R16	2.2K 1/2W Composition	±5%
R12 = R14	2.2K 1/2W Composition	±5%
R13	4.7K 1/2W Composition	±5%
R15	39K 1/2W Composition	±5%
R18	3.3K 1/2W Composition	±5%
R19	3K 1/2W metal film	±1%
R20	1K W.W. potentiometer	
R21	47K 1/2W Composition	±5%
R22	10K 1/2W Composition	±5%
R23	2K 1/2W Composition	±5%
R24	1.8K 1/2W Composition	±5%
R25	1.1K 5W Wire Wound	±5%
D1	1N3892	
D2 - D4	1N458A	
C1	100 µfd + 200 WVDC	±10%
C2	1000 µfd + 35 WVDC	±20%
C3	.027 µfd + 400 WVDC	±10%
C4	.015 µfd + 400 WVDC	±10%
Q1	Matched pair 2N3194 With matched hfe, Vbe, Rsat. (can use one 2N2528)	
Q2	STC 5204	
Q3 - Q6	2N697	
Q9 - Q12	2N697	
Q7 - Q8	2N1132A	

FIGURE 4-97

PARTS LIST FOR 200 WATT VOLTAGE REGULATOR (Continued)

Part No.	Value	Tolerance
L1	1MH - 10A cap	
L2	10.2 MH, - 10A cap	
DZ1	1N2823B - 30 V	±5%
DZ2	1N3021B - 11 V	±5%
DZ3	1N751A - 5.1 V	±5%

FIGURE 4-97

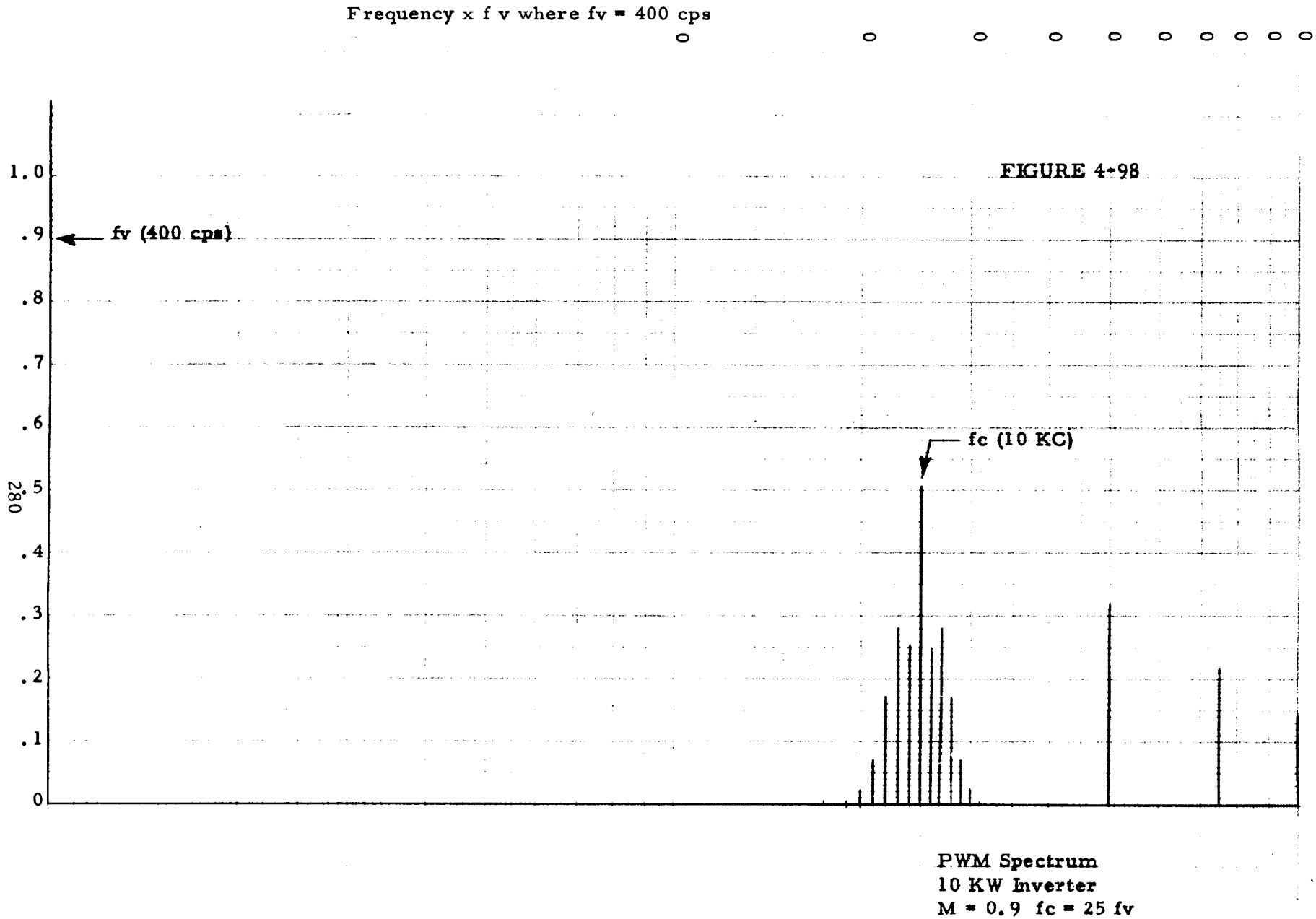
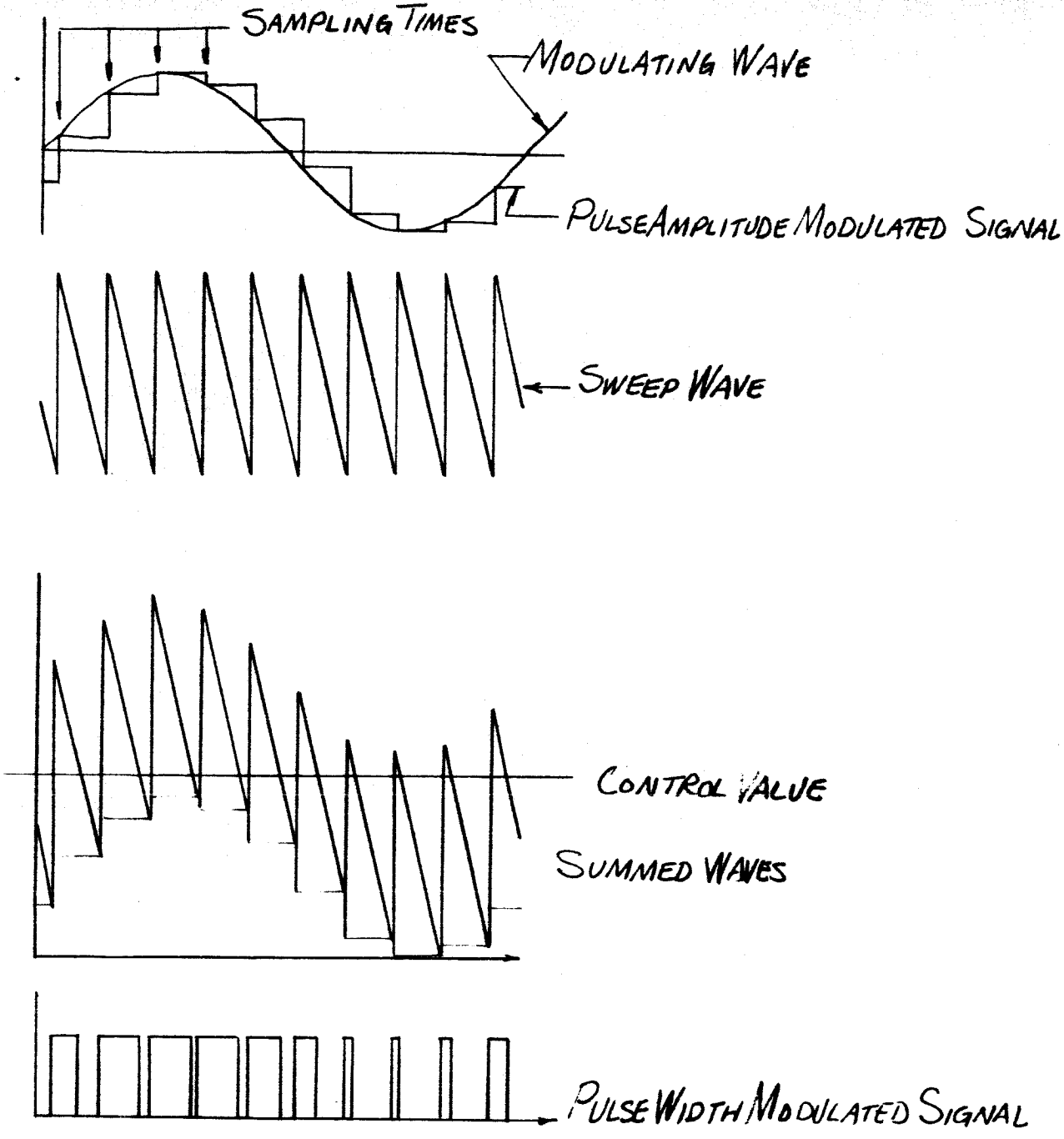


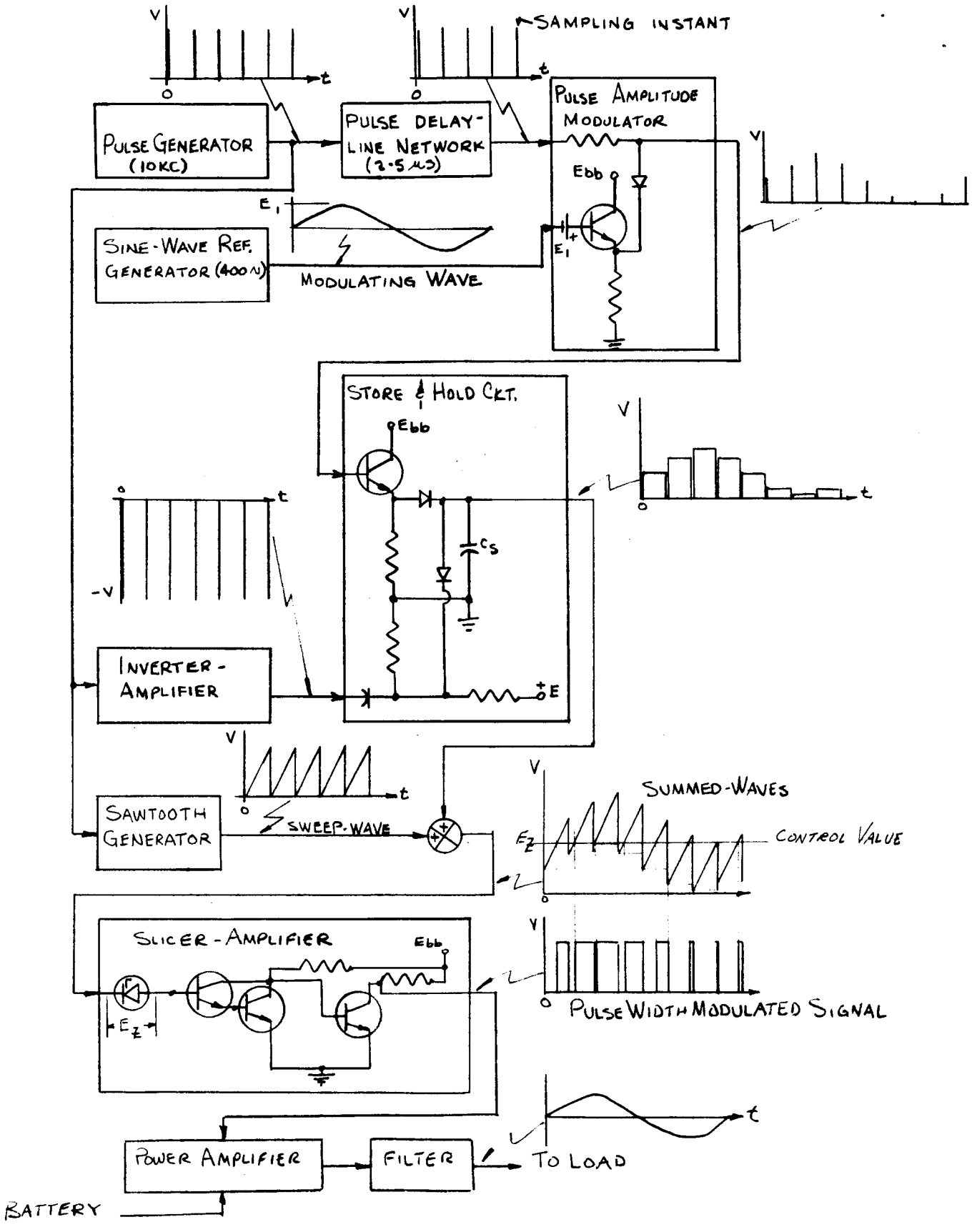
FIGURE 4-98

PWM Spectrum
10 KW Inverter
M = 0.9 fc = 25 fv



UNIFORM SAMPLING

FIGURE. 4-99



BLOCK DIAGRAM - UNIFORM SAMPLING PWM INVERTER

FIGURE 4-100

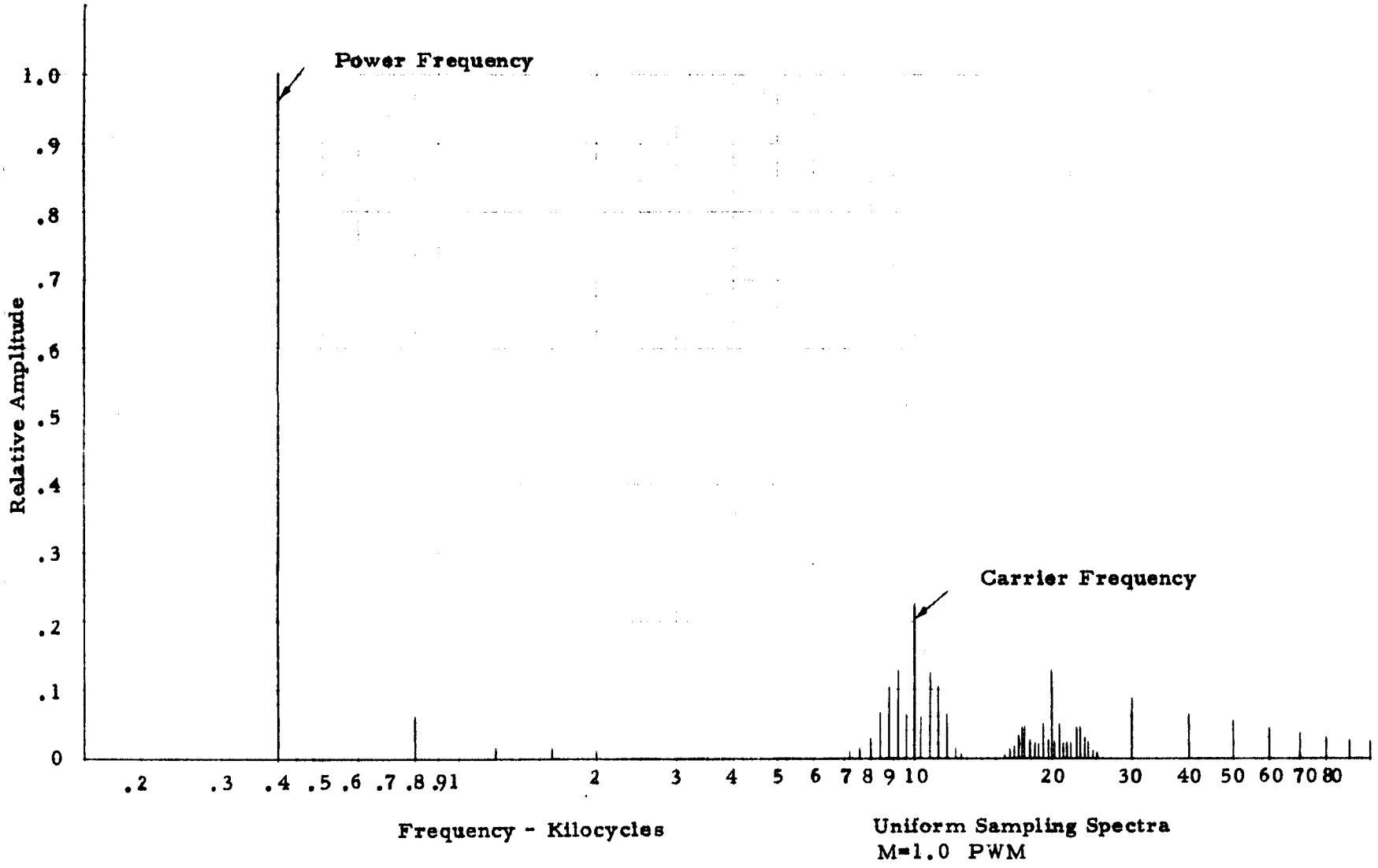
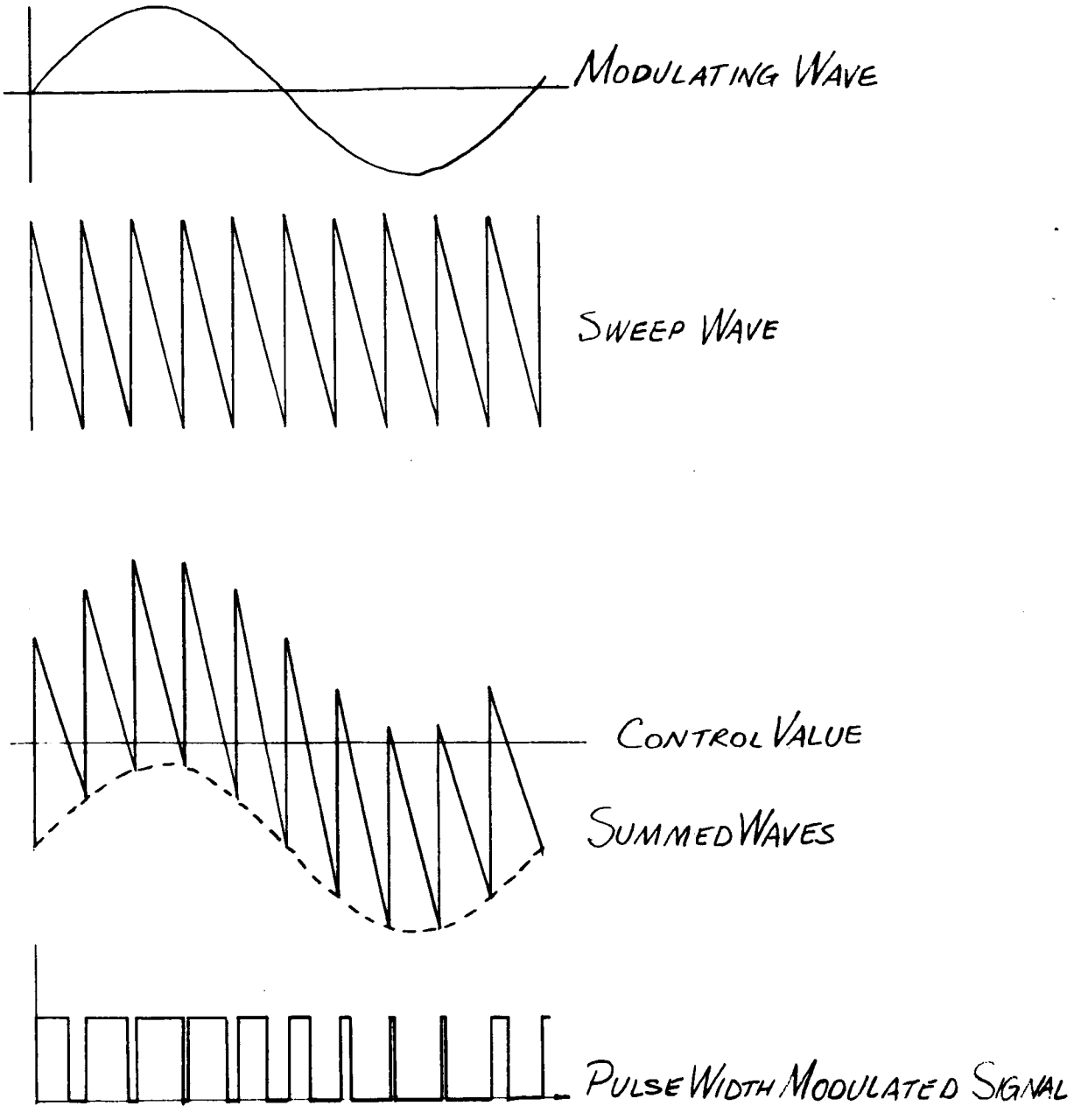
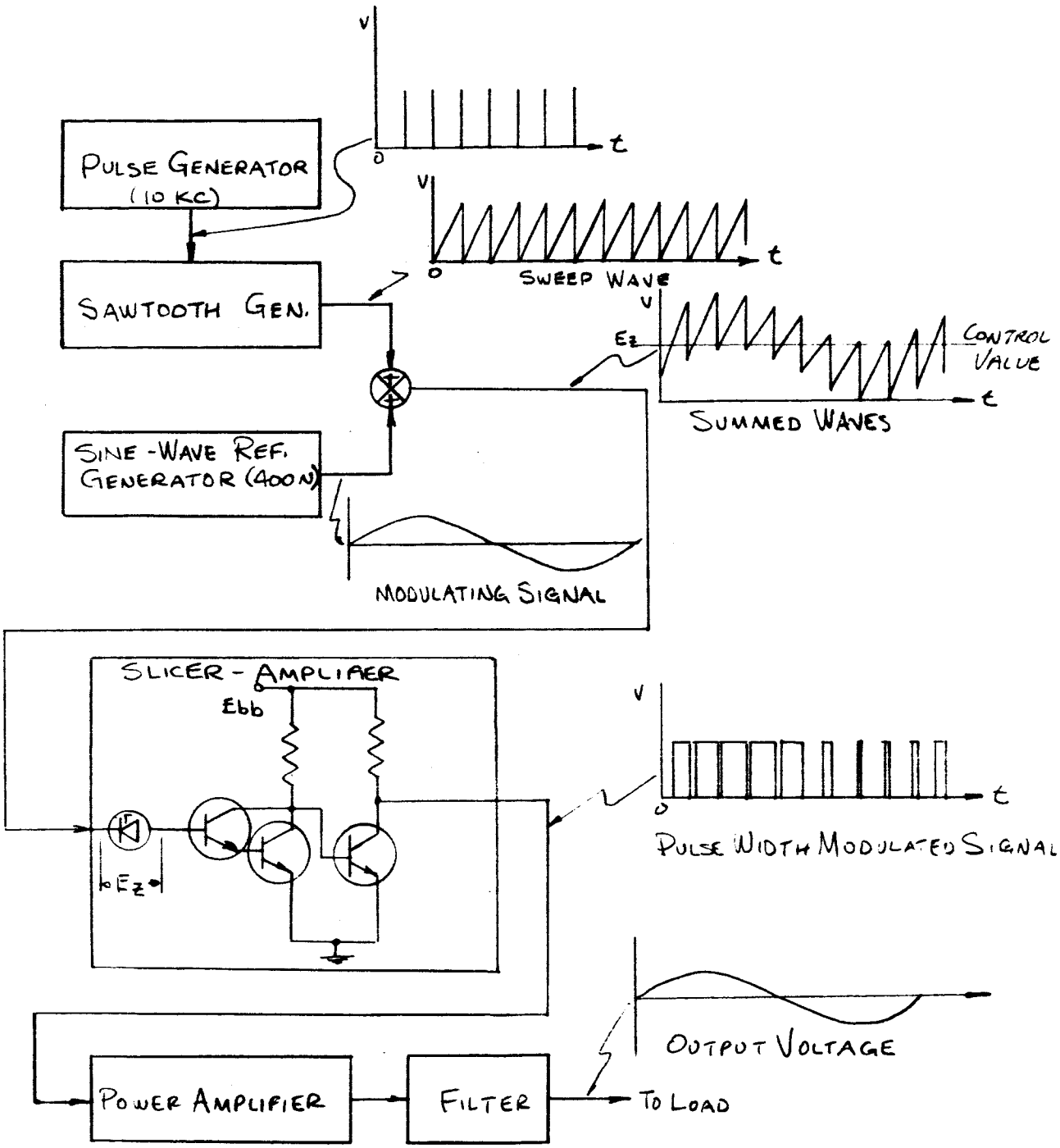

Power Frequency
Carrier Frequency
Relative Amplitude
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
0
.2 .3 .4 .5 .6 .7 .8 .91 2 3 4 5 6 7 8 9 10 20 30 40 50 60 70 80
Frequency - Kilocycles
Uniform Sampling Spectra
M=1.0 PWM

Figure 4-101



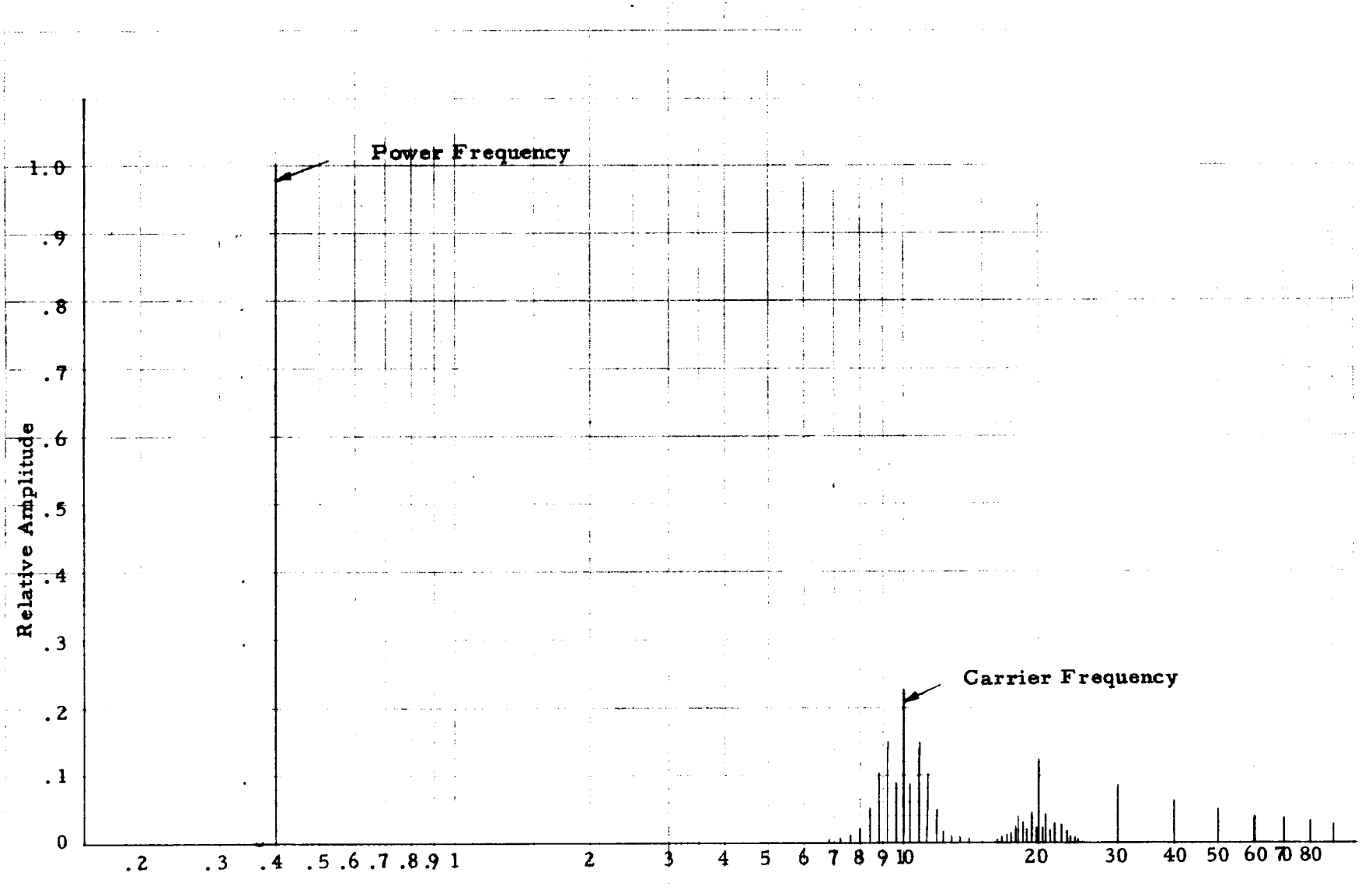
NATURAL SAMPLING

FIGURE 4-102



BLOCK DIAGRAM - NATURALLY SAMPLED PWM INVERTER

FIGURE 4-103



Naturally Sampled Spectra
M=1.0 PWM

Figure 4 - 104

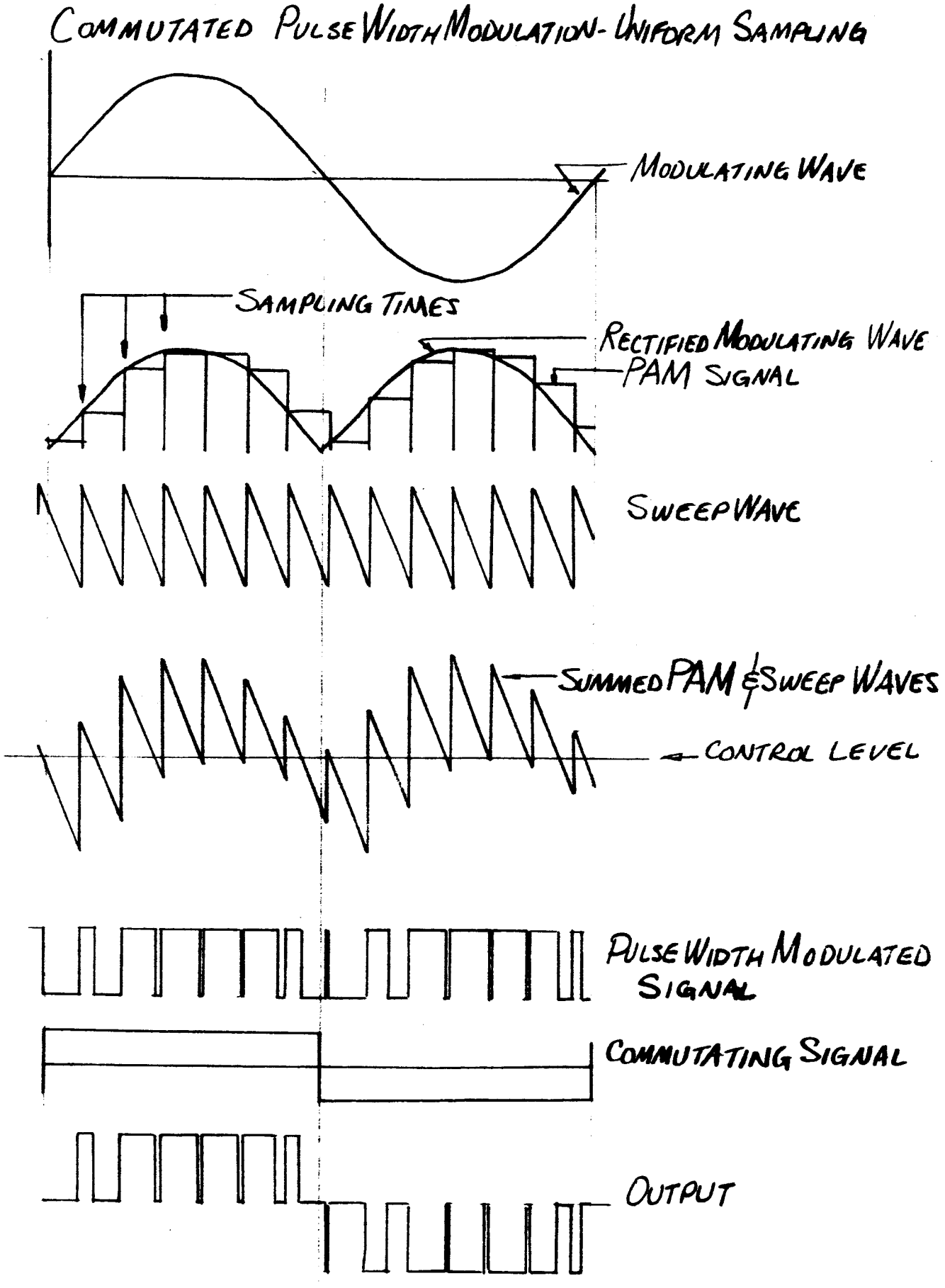
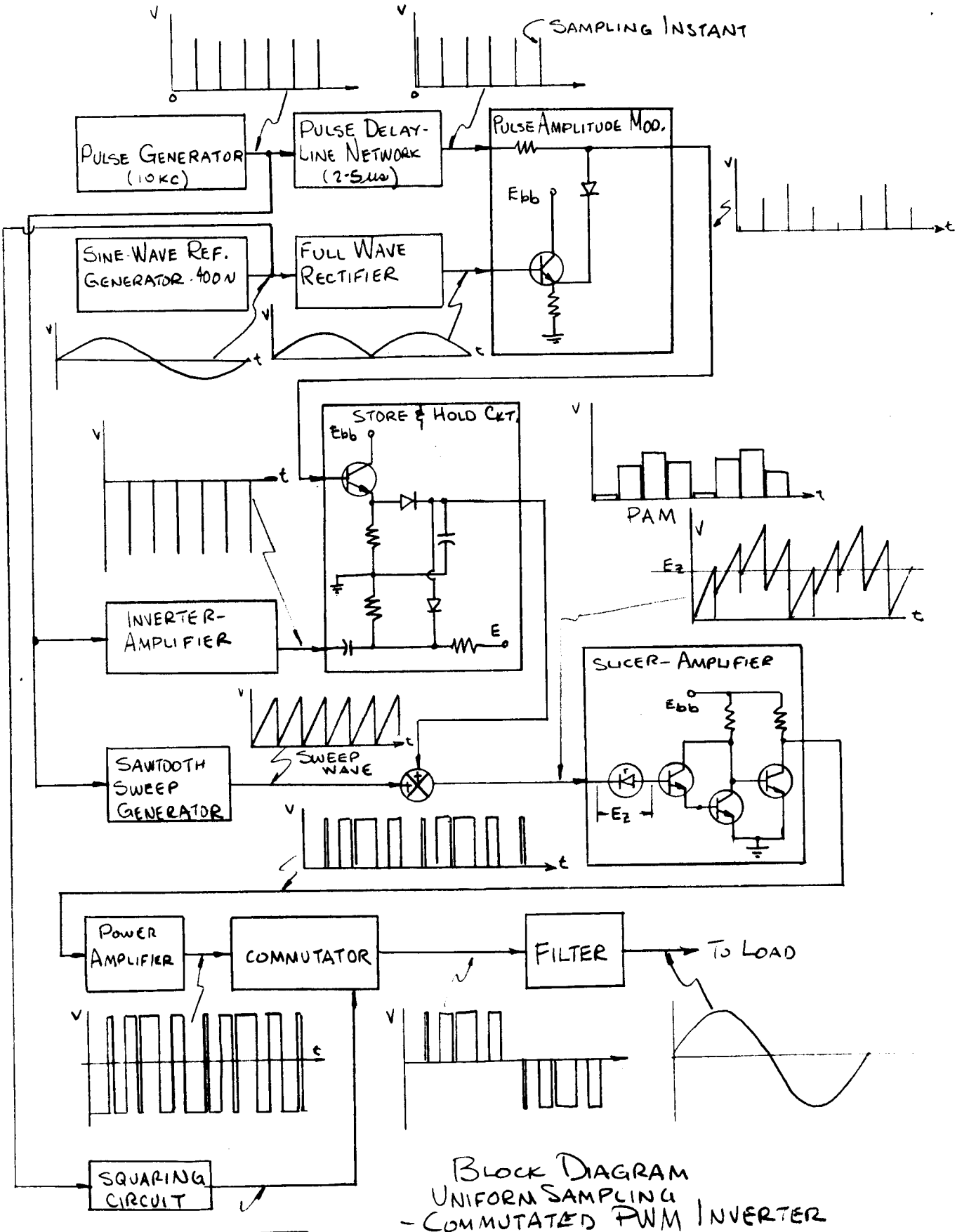

COMMUTATED PULSE WIDTH MODULATION - UNIFORM SAMPLING
MODULATING WAVE
SAMPLING TIMES
RECTIFIED MODULATING WAVE
PAM SIGNAL
SWEEP WAVE
SUMMED PAM & SWEEP WAVES
CONTROL LEVEL
PULSE WIDTH MODULATED SIGNAL
COMMUTATING SIGNAL
OUTPUT

FIGURE 4-105



BLOCK DIAGRAM
UNIFORM SAMPLING
- COMMUTATED PWM INVERTER
FIGURE 4-106

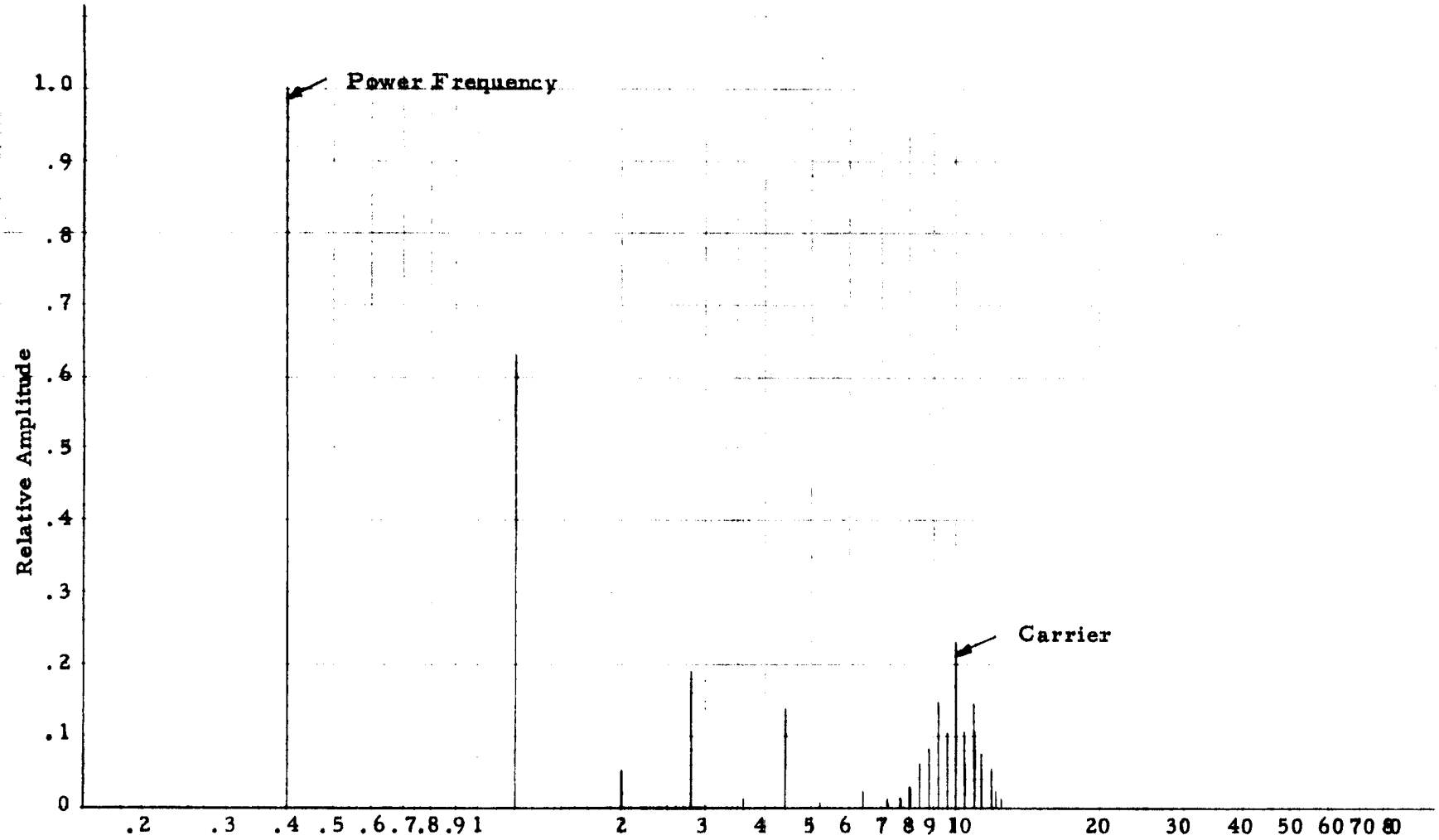
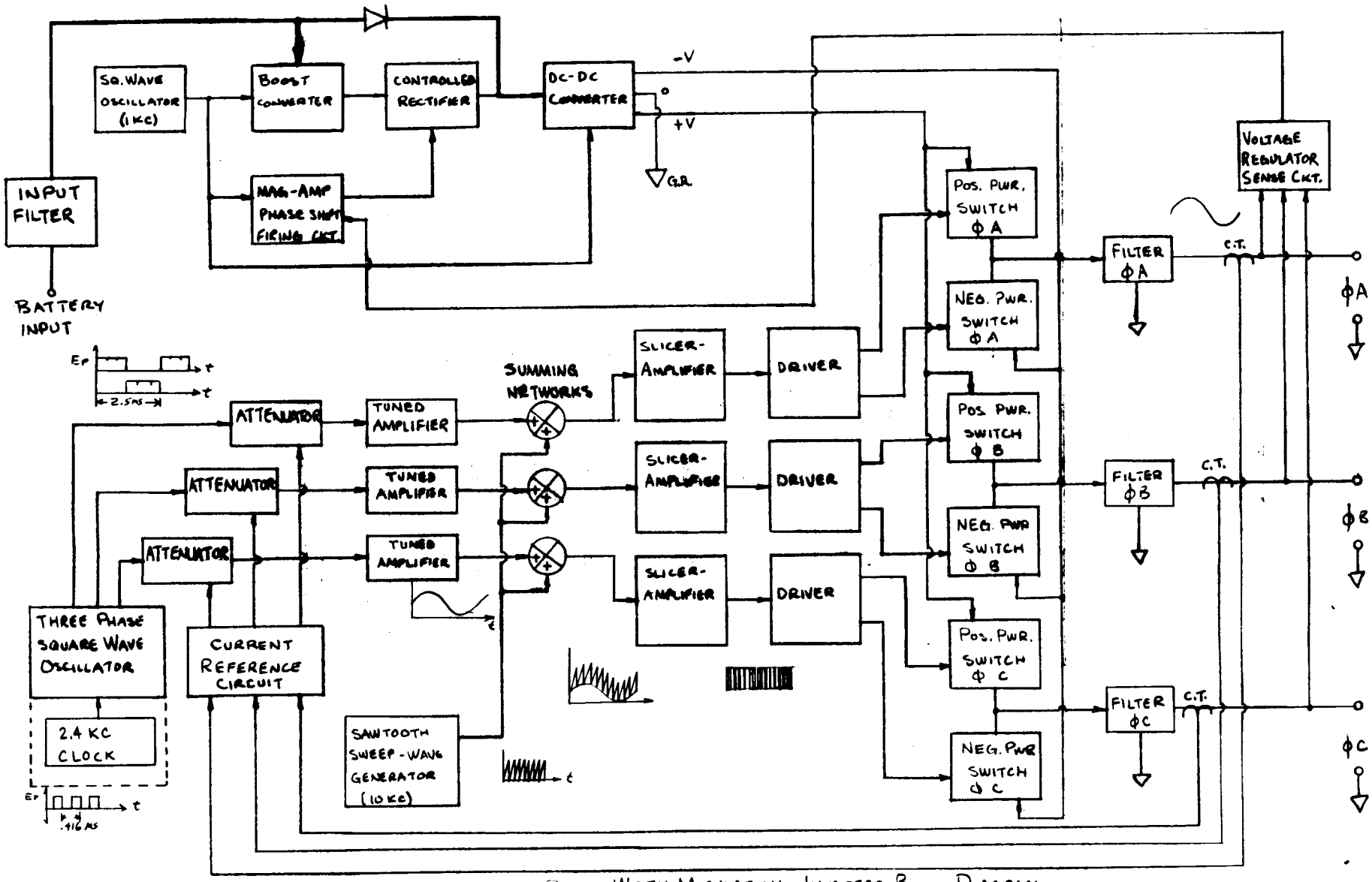


Figure 4 - 107

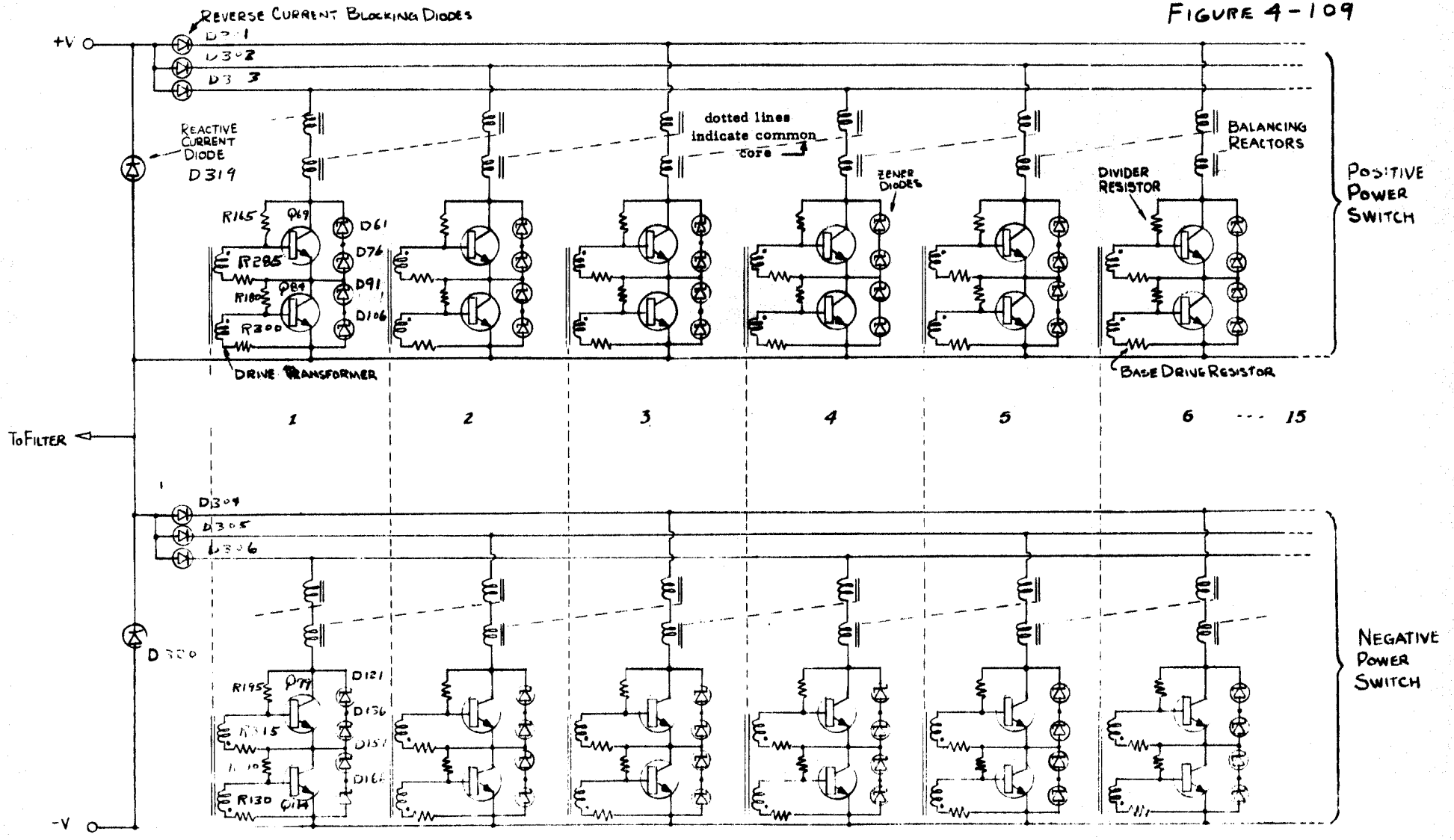
Commutated PWM Spectra
Uniform Sampling
M = 1.0

FIGURE 4-108



PULSE WIDTH MODULATION INVERTER BLOCK DIAGRAM

FIGURE 4-109

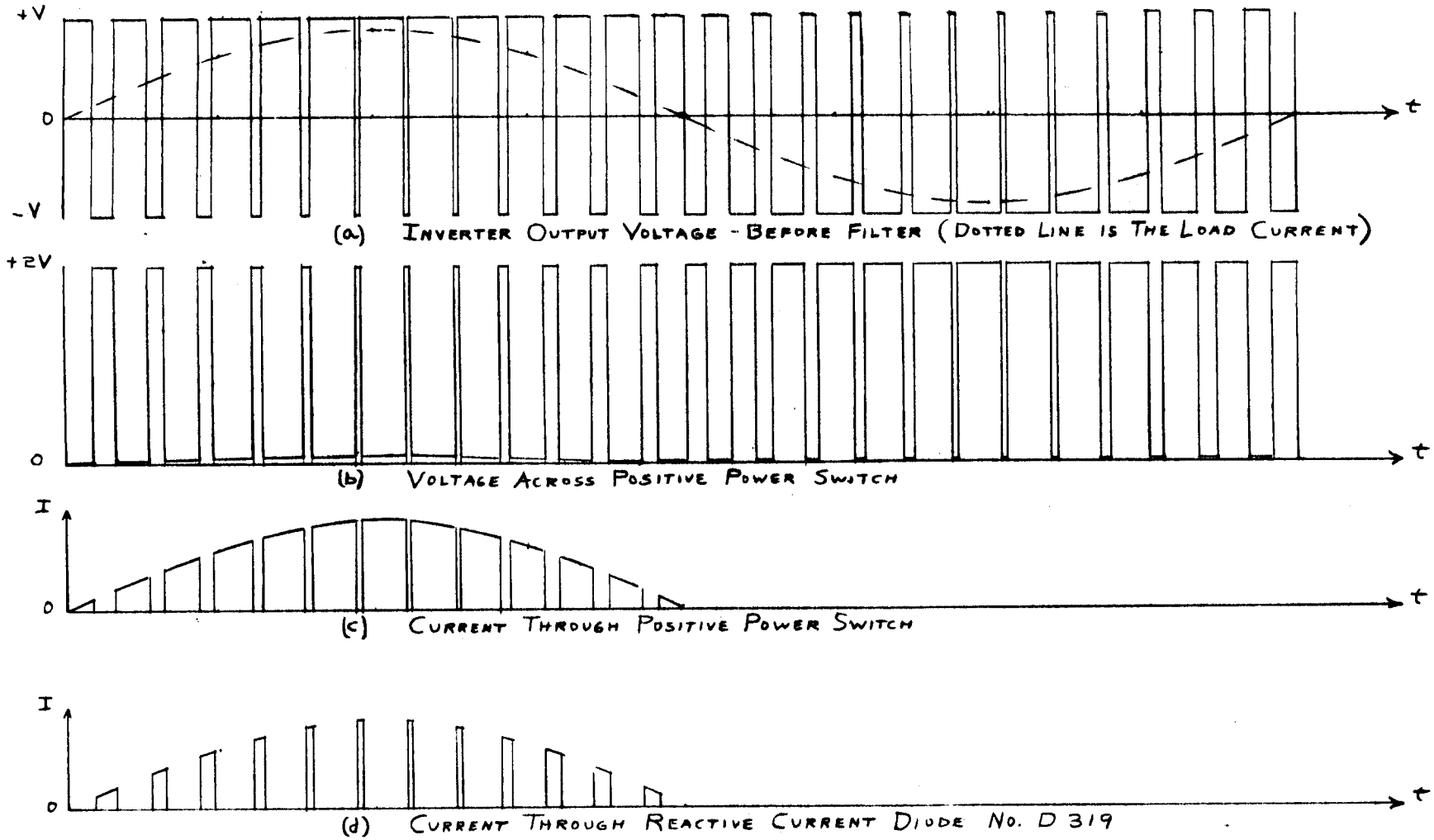


SCHEMATIC DIAGRAM - PWM STATIC INVERTER POWER STAGE (ONE PHASE SHOWN ONLY)

Parts List - PWM Static Inverter Power Stage

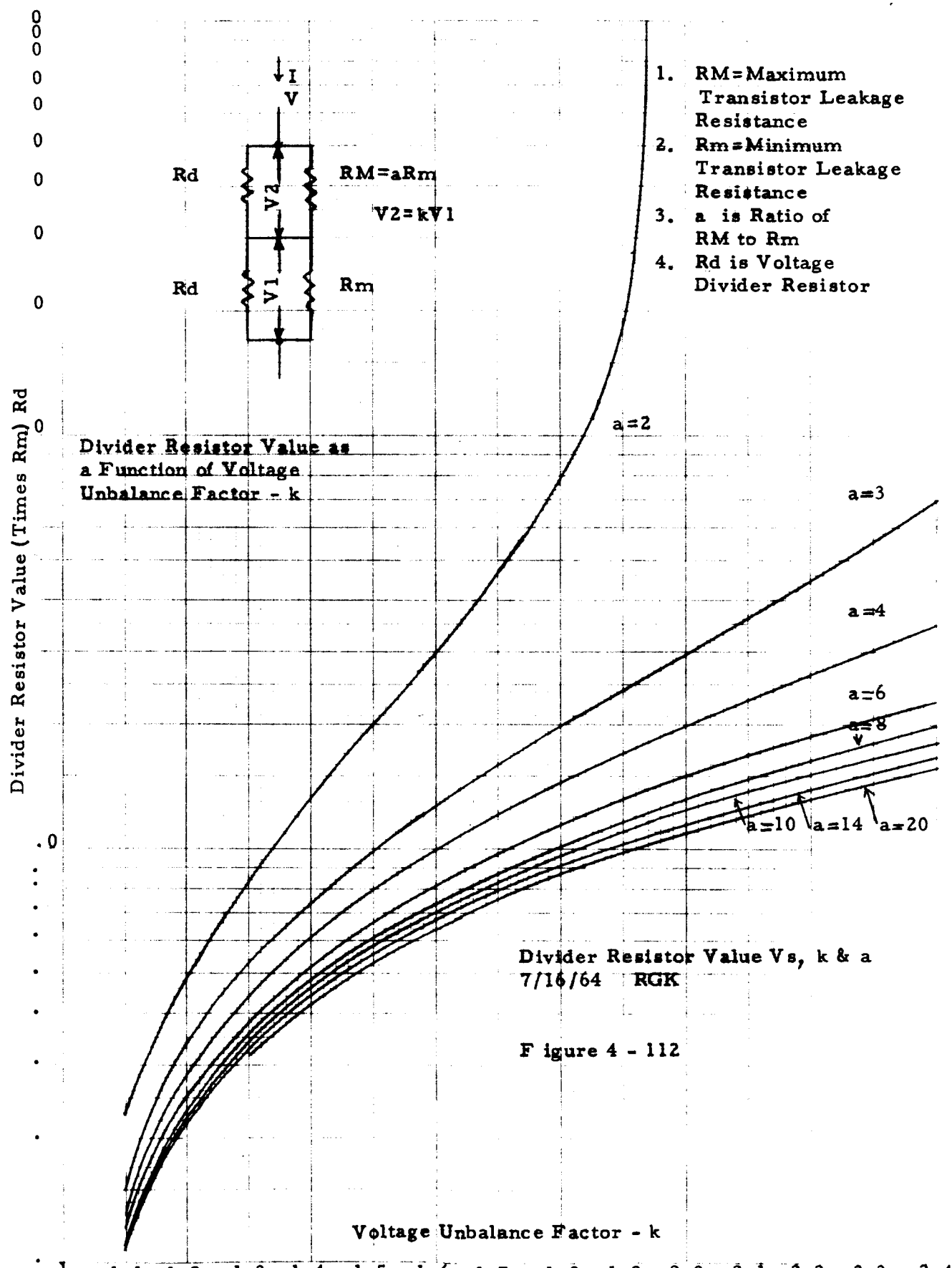
Item	Type	Quantity
Power Transistors	TA2110	180
Reverse Current Block Diodes	1N3918	18
Zener Diodes	1N3350 - 220V - 50W	360
Balancing Reactors	See Figure 4-113	90
Divider Resistors	50K 10W ±5% Wire Wound	180
Base Drive Resistors	1.3Ω-10W ±5% Wire Wound	180
Reactive Current Diodes	1N3918	6

FIGURE 4-110



Voltage and Current Wave Shapes For The Power Stage With A Unity P.F. Load.

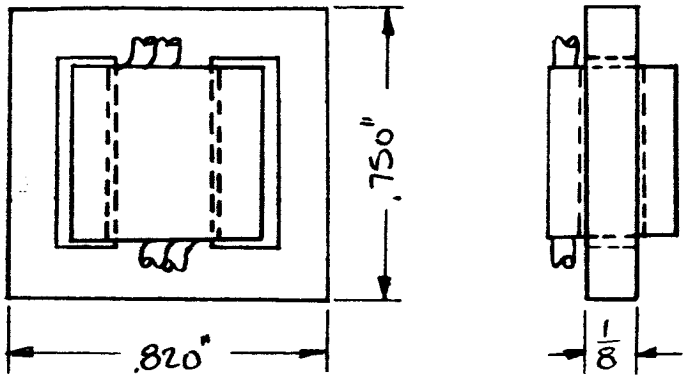
Figure 4-111



Divider Resistor Value Vs, k & a
7/16/64 RGK

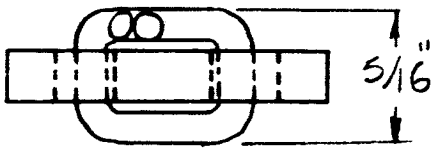
Figure 4 - 112

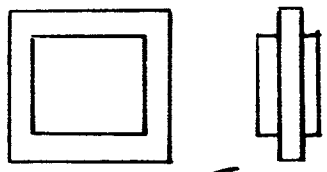
BALANCING REACTOR DESIGN



CORE:
9 LAMINATIONS
.014" x 34E-HyMu80

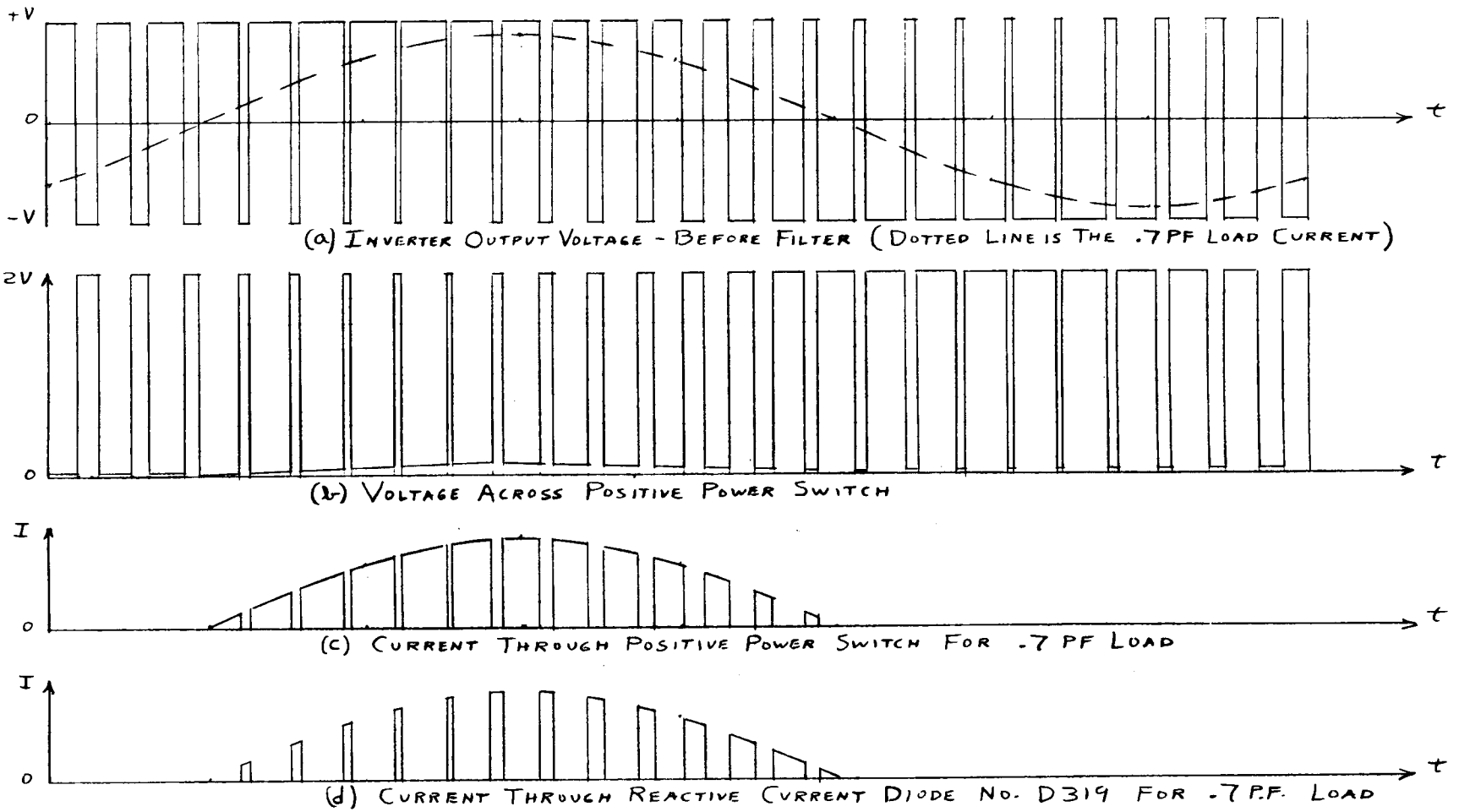
COILS
3 TURNS x 3 TURNS
#12
CLASS H
INSULATION





ACTUAL SIZE

FIGURE 4-113



Voltage and Current Wave Shapes For The Power Stage With A .7 PF Load

Figure 4-114

DC-DC Converter Schematic

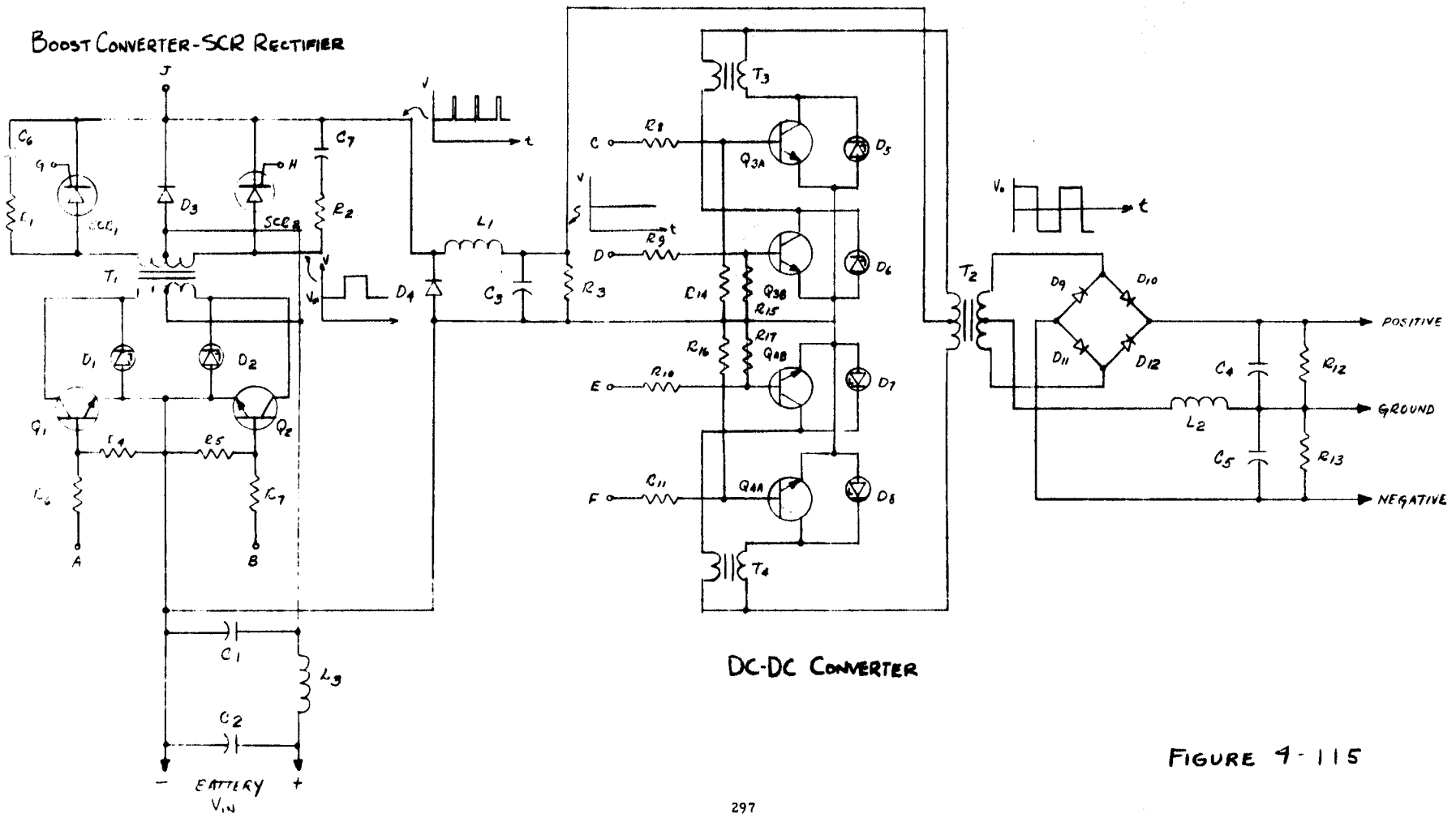


Figure 9-115

DC-DC Converter Schematic

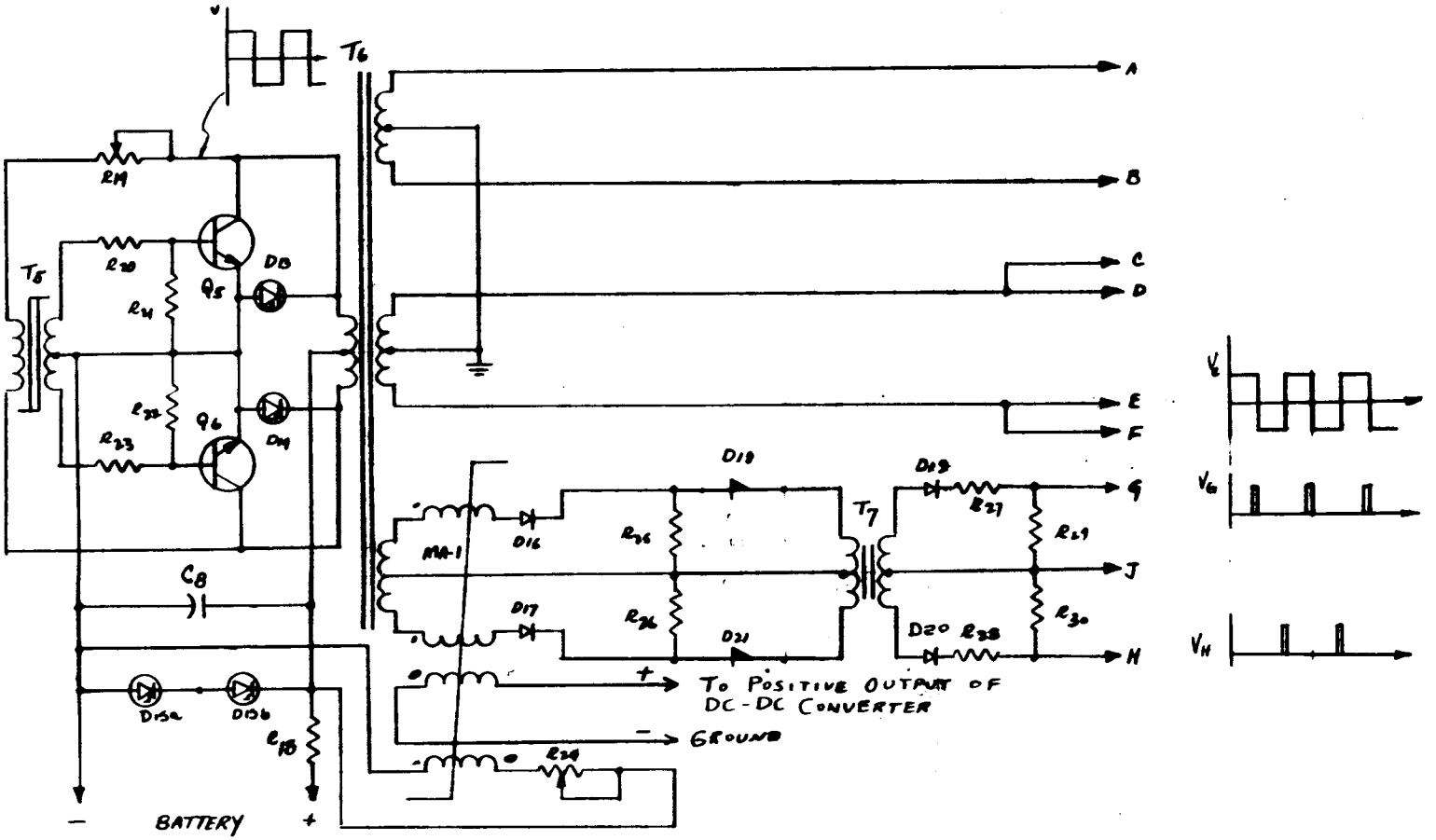


Figure 9-116

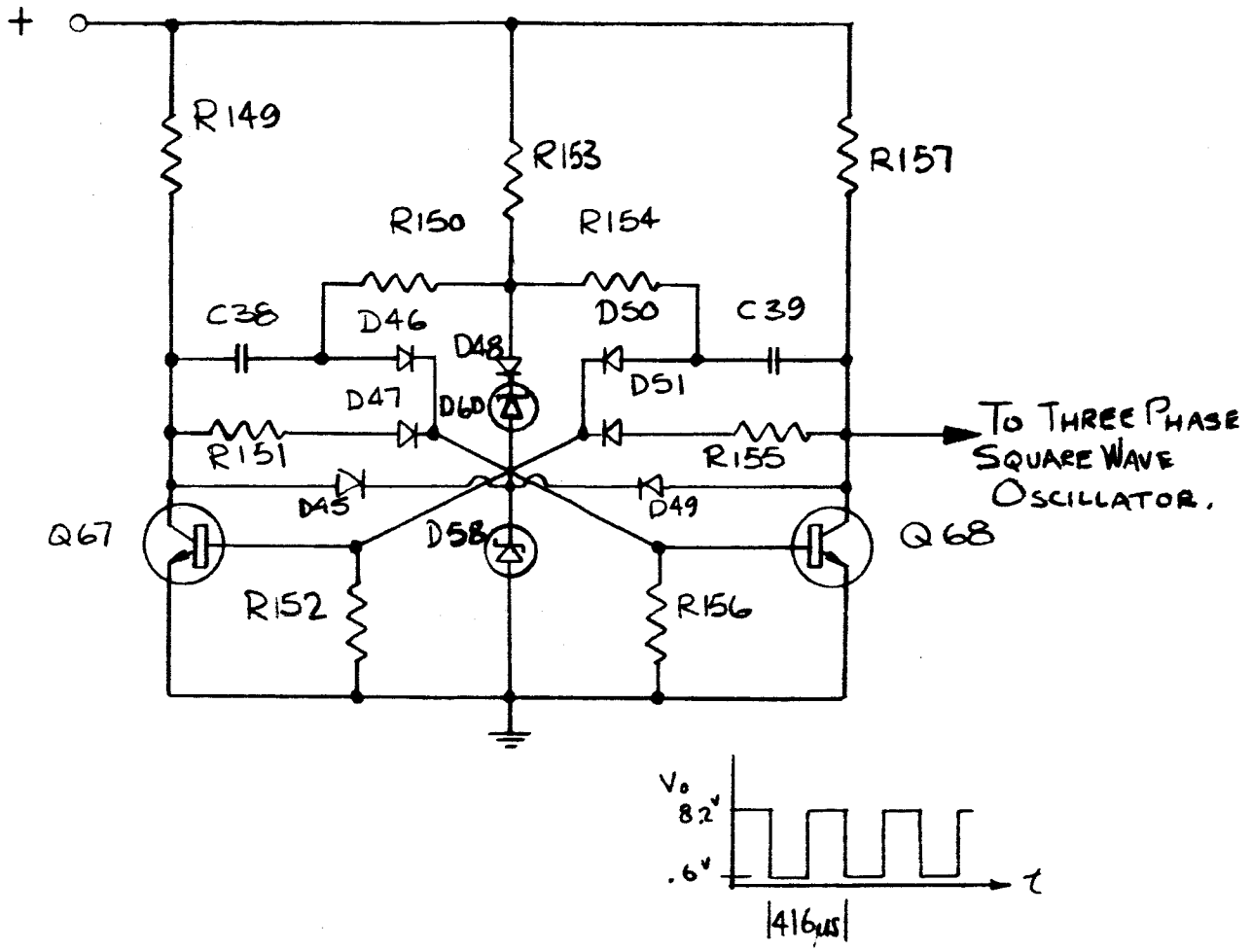
Parts List - DC-DC Converter

$Q_1 = Q_2$	STC 2105
$Q_{3A} = Q_{3B} = Q_{4A} = Q_{4B}$	STC 2501
$Q_5 = Q_6$	2N1486
$SCR_1 = SCR_2$	C80D (selected for high DV/DT)
$D_1 = D_2$	1N3009B - 130V - 10W
D_3	1N4045
D_4	1N1184
$D_5 = D_6 = D_7 = D_8$	1N3009B - 130V - 10W
$D_9 = D_{10} = D_{11} = D_{12}$	1N1190 (or fast recovery equivalent)
$D_{13} = D_{14}$	1N3041B - 75 V - 1W
$D_{15a} = D_{15b}$	1N2913 (50W) 15 V - 50W
$D_{16} = D_{17} = D_{19} = D_{20}$	1N3189
$D_{18} = D_{21}$	4E 20-8
$C_1 = C_2$	16μf - 100 WVDC
C_3	24μf - 100 WVDC
$C_4 = C_5$	0.75μf - 375 WVDC
$C_6 = C_7$	0.5μf - 400 WVDC
C_8	24μf - 100 WVDC
L_1	8 micro hy. - class H
L_2	32 micro hy. - class H
L_3	50 micro hy. - class H
R_1, R_2	100Ω-10W ±5% Wire Wound
R_3	9.1K - 5W ±5% Wire Wound

FIGURE 4-117

R_4, R_5, R_{14}, R_{15}, R_{16}, R_{17}		100Ω - $\frac{1}{2}$ W ±5%	Composition
R_6, R_7		.34Ω-25W ±5%	Wire Wound
R_8, R_9, R_{10}, R_{11},		.195Ω-25W ±5%	Wire Wound
R_{12}, R_{13}		150K - 10W ±5%	Wire Wound
R_{18}		5.9Ω-250W ±5%	Wire Wound
R_{19}		50Ωpot - 1W ±5%	Wire Wound
R_{20}, R_{23}		15Ω-1W ±5%	Composition
R_{24}		5K pot - 1W ±5%	Wire Wound
R_{25}, R_{26}		3.3 K -1W ±5%	Composition
R_{27}, R_{28}		10Ω-1W ±5%	Composition
R_{21}, R_{22}, R_{29}, R_{30}		100Ω -$\frac{1}{2}$ W ±5%	Composition
T_1 - Drive Transformer (Class H)	NP = 21T-CT NS = 6T-CT	-#7 wire -.162" x .410"	Rect. Wire
T_2 - Power Output Transformer (Class H)	NP = 12T-CT NS = 39T-CT	-128" x .410" -#10 wire	Rect. Wire
T_3 = T_4 Timing Core (Class H)	NP = NS = 2T	-.128" x 410"	Rect. Wire
T_5 - Drive Transformer (Class H)	NP = 1275T NS = 59T - CT	-#38 wire -#30 wire	
T_6 - Drive Transformer (ClassH)	NP = 50T-CT NS_1 = 5T-CT NS_2 = 5T-CT NS_3=50T-CT	#18 wire #16 wire #12 wire #28 wire	
T_7- Drive Transformer (Class H)	NP=250T-CT NS=45T-CT	#34 wire #26 wire	
MA-1 Magamp (Class H)	Gate - 1350 T Bias - 1300T Control - 4000T	#30 wire #33 wire #40 wire	

FIGURE 4-117



2.4 KC Clock

FIGURE 9-118

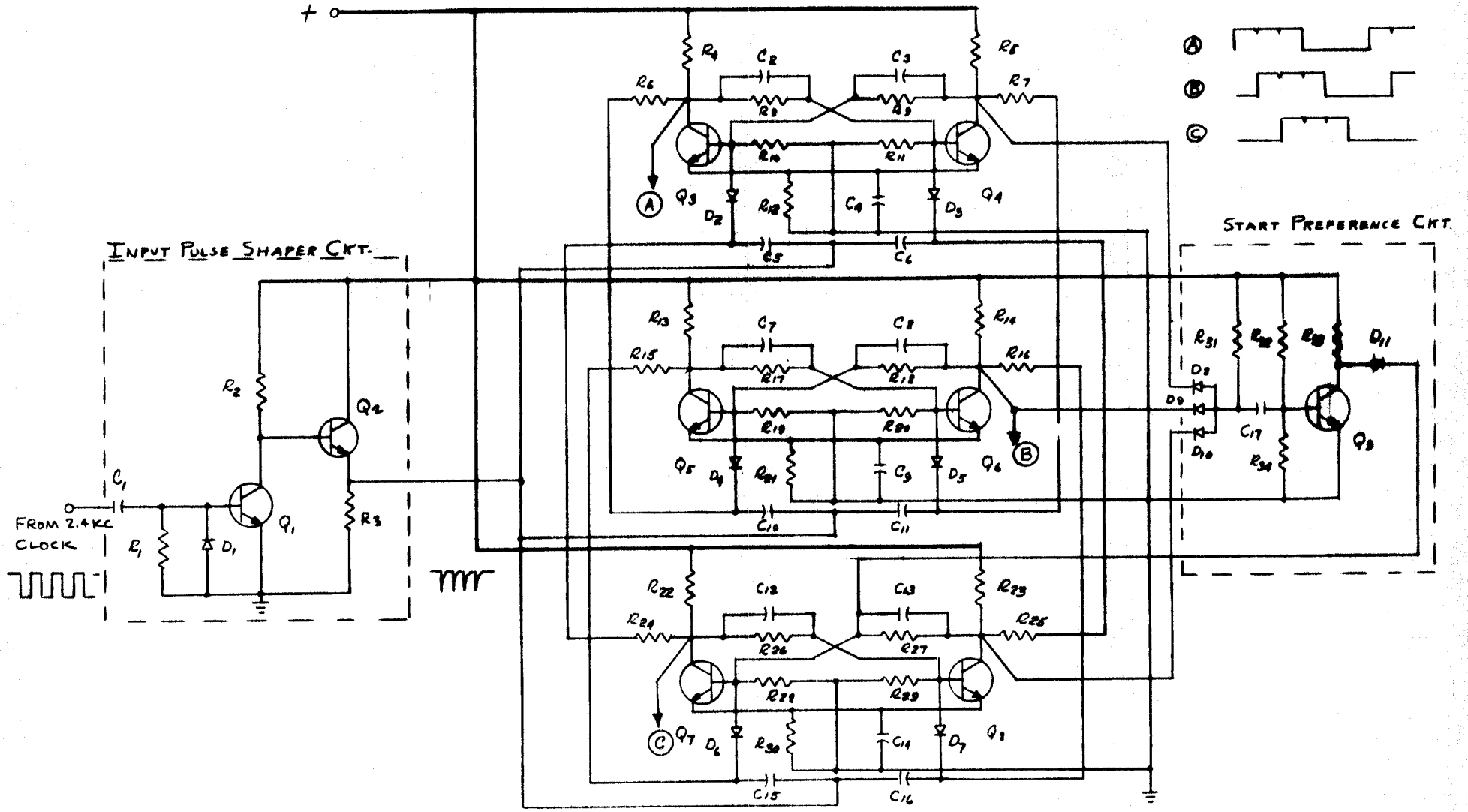
Parts List - 2.4 KC Clock

Q_{67}, Q_{68}	2N2218	
D_{45}, D_{51}	1N659	
D_{58}	1N756	8.2V - .4W
D_{60}	1N747	3.6V - .4W
R_{149}, R_{157}	2.4K -	$\frac{1}{2}$ W ±5% Composition
R_{150}, R_{154}	27K -	$\frac{1}{2}$ W ±1% Metal Film
R_{151}, R_{155}	22K -	$\frac{1}{2}$ W ±1% Metal Film
R_{152}, R_{156}	51K -	$\frac{1}{2}$ W ±5% Composition
R_{153}	330 -	$\frac{1}{2}$ W ±5% Composition
C_{38}, C_{39}	.01μfd - 100 WVDC	

FIGURE 4-119

FIGURE 9-120

3φ RING COUNTER



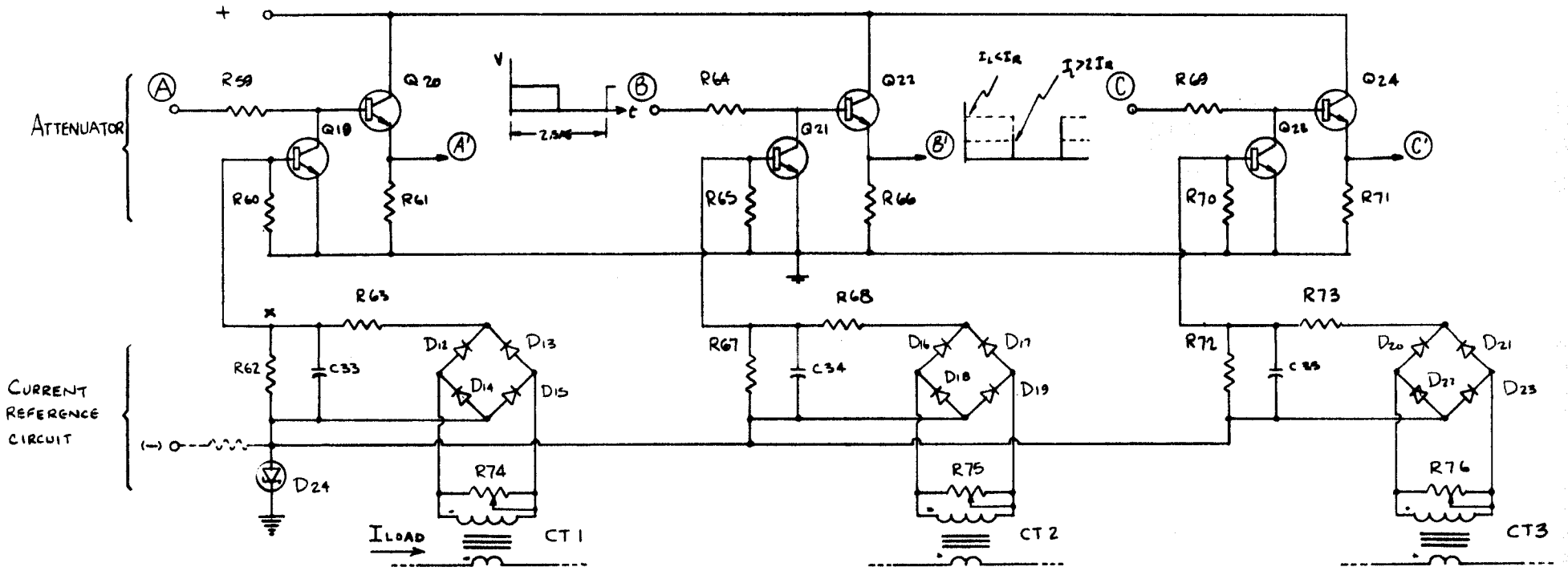
THREE PHASE SQUARE WAVE OSCILLATOR

Parts List - Three Phase Square Wave Oscillator

Q_1, Q_3, Q_4, Q_5, Q_6, Q_7, Q_8, Q_9	2N338A
Q_2	2N656A
$D_1 \longrightarrow D_{11}$	1N659
C_1, C_5, C_6, C_{10}, C_{11}, C_{15}, C_{16}	0.0015 μf - 100 WVDC
C_2, C_3, C_7, C_8, C_{12}, C_{13}	470 pf - 100 WVDC
C_4, C_9, C_{14}	22 μf - 50 WVDC
C_{17}	.001 μfd - 100 WVDC
R_1	91K - $\frac{1}{2}$ W ±5%
R_2	6.8K - $\frac{1}{2}$ W ±5%
R_3	680Ω - 1W ±5%
R_4, R_5, R_{13}, R_{14}, R_{22}, R_{23}	1.3K 1W ±5%
R_6, R_7, R_{15}, R_{16}, R_{24}, R_{25}, R_{34}	22K - $\frac{1}{2}$ W ±5%
R_8, R_9, R_{17}, R_{18}, R_{26}, R_{27}, R_{33}	8.2K - $\frac{1}{2}$ W±5%
R_{10}, R_{11}, R_{19}, R_{20}, R_{28}, R_{29}	6.2K - $\frac{1}{2}$ W ±5%
R_{12}, R_{21}, R_{30}	240 - $\frac{1}{2}$ W ±5%
R_{31}	51K - $\frac{1}{2}$ W ±5%
R_{32}	56K - $\frac{1}{2}$ W ±5%

All resistors are composition.

FIGURE 4-121



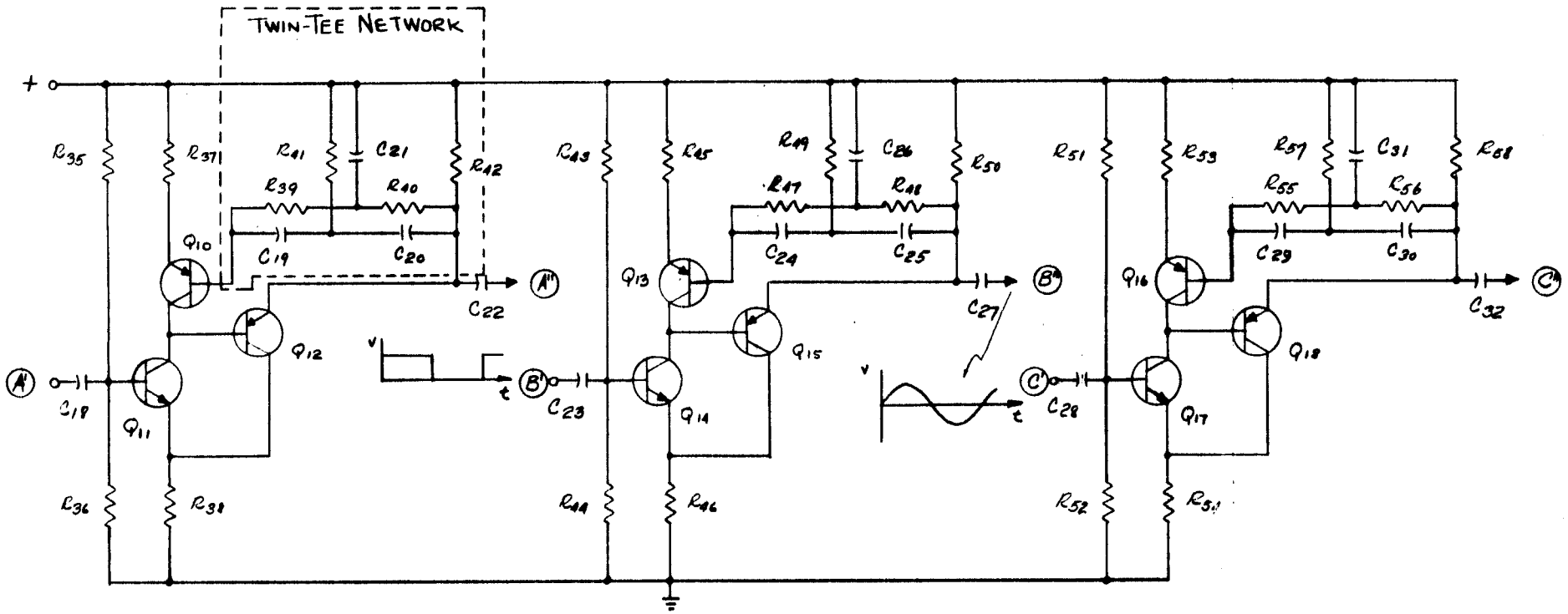
POINT X IS NEGATIVE WHEN $I_{LOAD} < 2 I_{RATED}$
POINT X IS POSITIVE WHEN $I_{LOAD} > 2 I_{RATED}$

CURRENT REFERENCE CIRCUIT
AND
ATTENUATORS

FIGURE 4-122

Q_{19}, Q_{20}, Q_{21}, Q_{22}, Q_{23}, Q_{24}	2N2218
$D_{12} \longrightarrow D_{23}$	1N659
D_{24}	1N751 - 5.1V - .4W
CT_1, CT_2, CT_3	(Class H) Current transformers a = 10,000 : 1
R_{59}, R_{64}, R_{69}	27K - $\frac{1}{2}$ W ±5% Composition
R_{60}, R_{65}, R_{70}	4.7 K - $\frac{1}{2}$ W ±5% Composition
R_{61}, R_{66}, R_{71}	3.9 K - $\frac{1}{2}$ W ±5% Composition
R_{62}, R_{67}, R_{72}	2.7K - $\frac{1}{2}$ W ±5% Composition
R_{63}, R_{68}, R_{73}	56 - $\frac{1}{2}$ W ±5% Composition
R_{74}, R_{75}, R_{76}	1 K potentiometer - 1W ±5% Wire Wound
C_{33}, C_{34}, C_{35}	4.7 micro fd. /10 WVDC

FIGURE 4-123

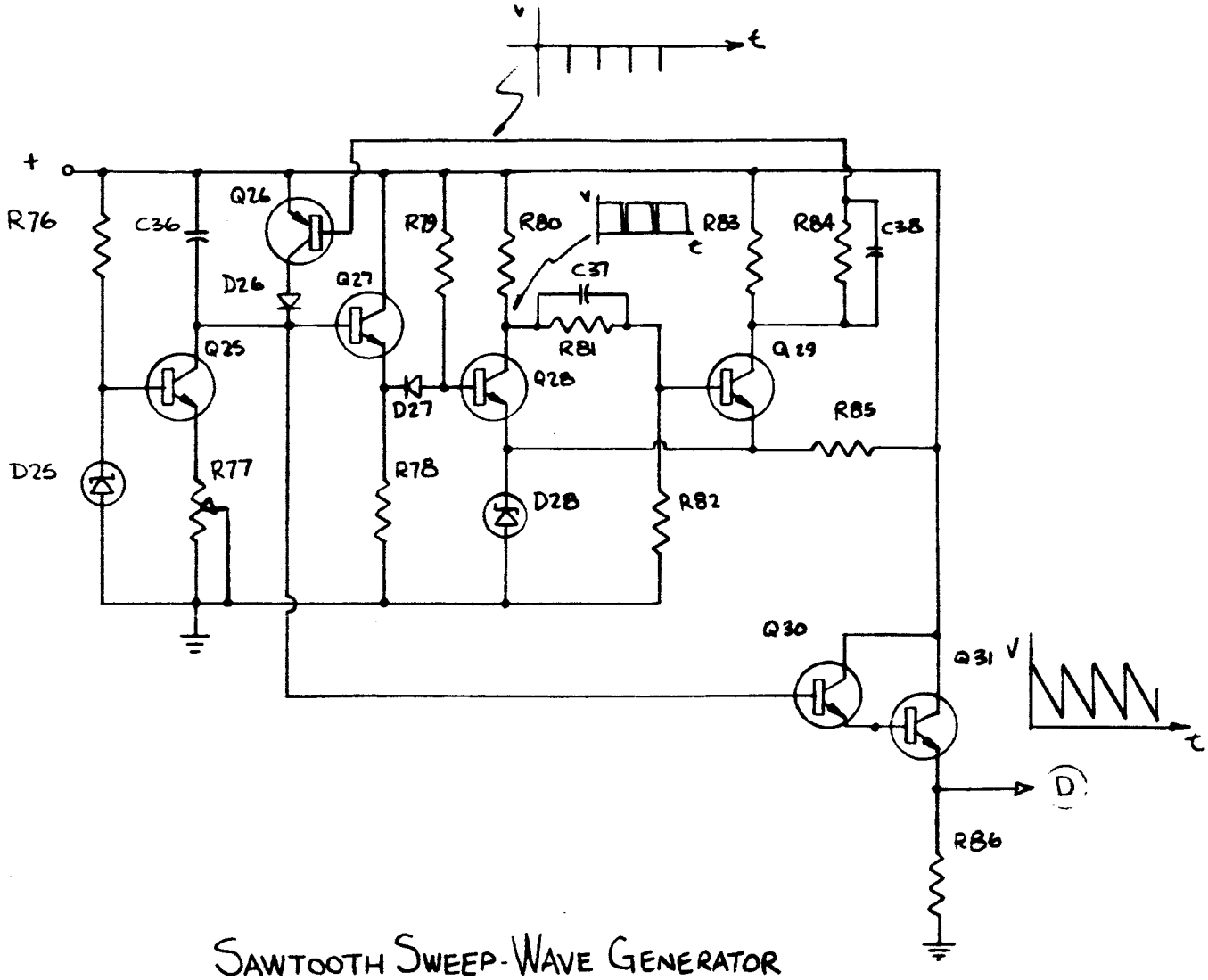


TUNED AMPLIFIERS

FIGURE 4-124

Q_{10}, Q_{12}, Q_{13}, Q_{15}, Q_{16}, Q_{18}	2N2904	
Q_{11}, Q_{14}, Q_{17}	2N2218	
C_{18}, C_{22}, C_{23}, C_{27}, C_{28}, C_{32}	1.0μf - 100 WVDC	
C_{19}, C_{20}, C_{21}, C_{24}, C_{25}, C_{26}, C_{29}, C_{30}, C_{31}	0.0068μf - 100 WVDC	
R_{35}, R_{43}, R_{51}	47K - $\frac{1}{2}$ W ±5%	Composition
R_{36}, R_{44}, R_{52}	4.7K - $\frac{1}{2}$ W ±5%	Composition
R_{37}, R_{38}, R_{45}, R_{46}, R_{53}, R_{54}	1K - 1W ±5%	Composition
R_{39}, R_{47}, R_{55}	57.6K - $\frac{1}{2}$ W ±1%	Metal Film
R_{40}, R_{48}, R_{56}	115K - $\frac{1}{2}$ W ±1%	Metal Film
R_{41}, R_{49}, R_{57}	19.1K - $\frac{1}{2}$ W ±1%	Metal Film
R_{42}, R_{50}, R_{58}	10 meg - $\frac{1}{2}$ W ±5%	Composition

FIGURE 4-125



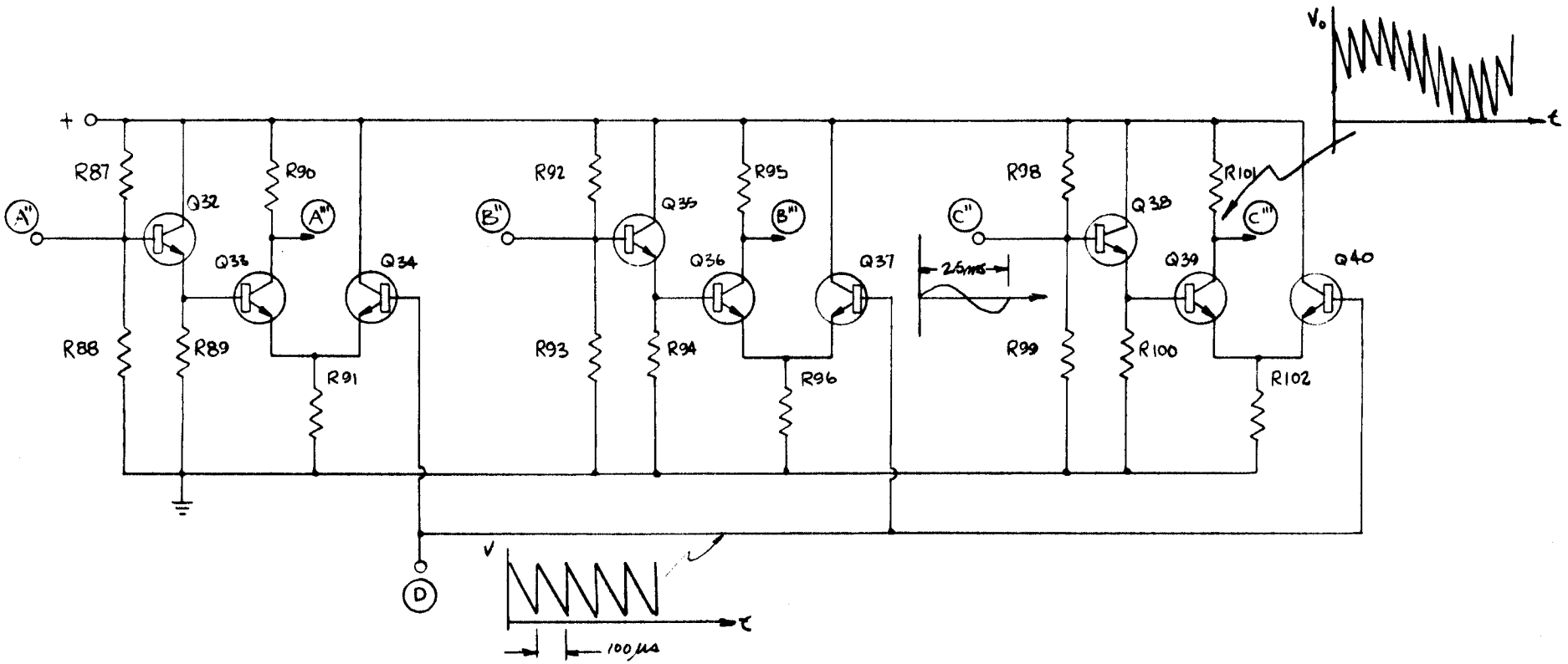
SAWTOOTH SWEEP-WAVE GENERATOR

FIGURE 4-126

Q_{25}, Q_{27}, Q_{28}, Q_{29}, Q_{31}, Q30	2N2218
Q_{26}	2N2904A
D_{25}, D_{28}	1N751 - 5.1V - .4W
D_{26}, D_{27}	1N659
C_{36}	.022μfd - 100 WVDC
C_{37}, C_{38}	.001μfd - 100 WVDC
R_{76}, R_{85}	2.2K - $\frac{1}{2}$ W ±5%
R_{77}	5K pot - 1W ±5%
R_{86}	1K - 1W ±5%
R_{79}, R_{82}	47K - $\frac{1}{2}$ W ±5%
R_{80}, R_{83}, R_{84}, R_{78}	4.7K - $\frac{1}{2}$W ±5%
R_{81}	10K - $\frac{1}{2}$ W ±5%

All resistors are composition.

Figure 4 - 127



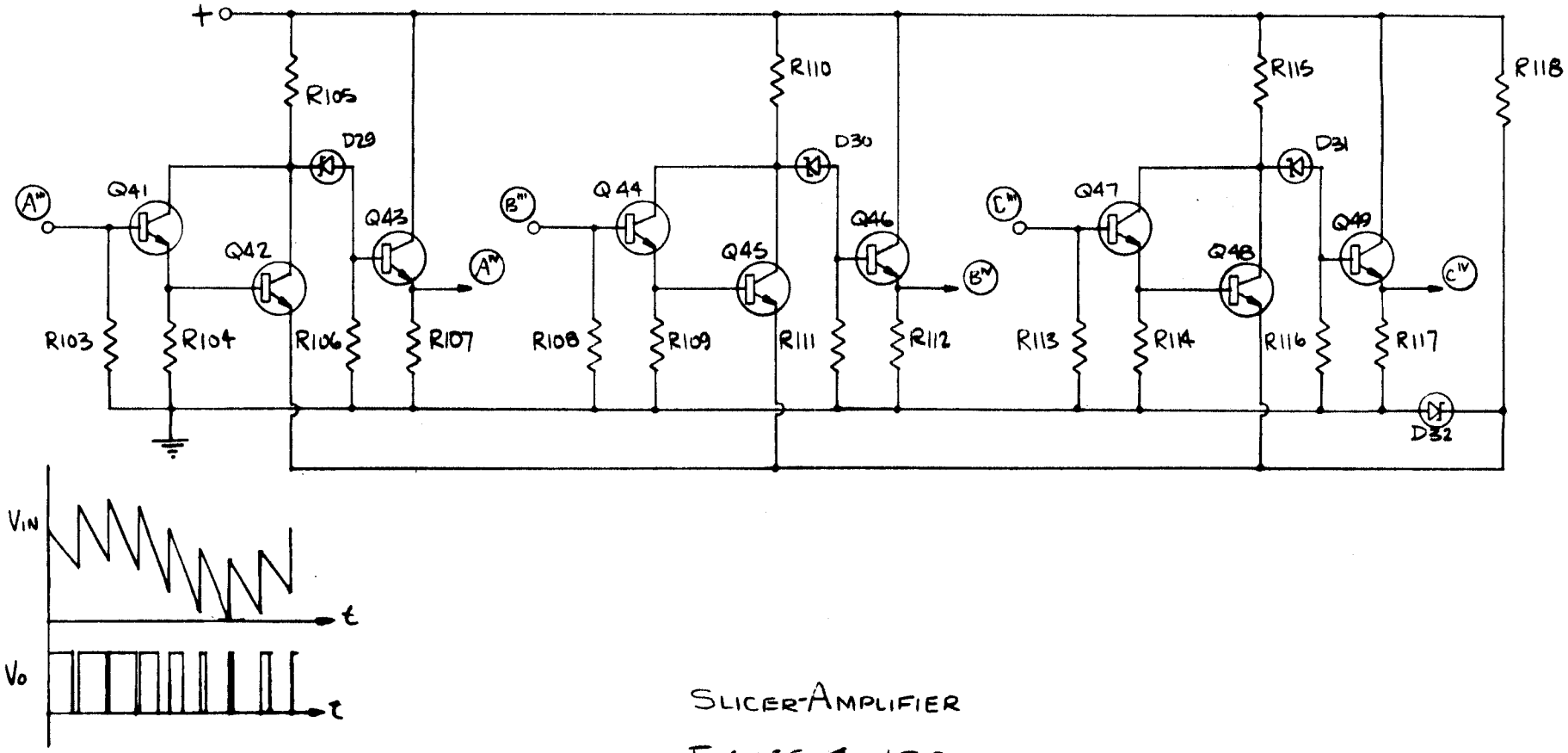
SUMMING NETWORKS

FIGURE 9-128

Parts List - Summing Amplifier

$Q_{32} \rightarrow Q_{40}$	2N2218
R_{87}, R_{92}, R_{98}	68K - $\frac{1}{2}$ W ±5% Composition
R_{88}, R_{93}, R_{99}	27K - $\frac{1}{2}$ W ±5% Composition
R_{89}, R_{94}, R_{100}	10K - $\frac{1}{2}$ W ±5% Composition
R_{90}, R_{95}, R_{101}	4.7K - 10W ±5% Wire Wound
R_{91}, R_{96}, R_{102}	2.7 K - 10W ±5% Wire Wound

FIGURE 4-129



SLICER-AMPLIFIER

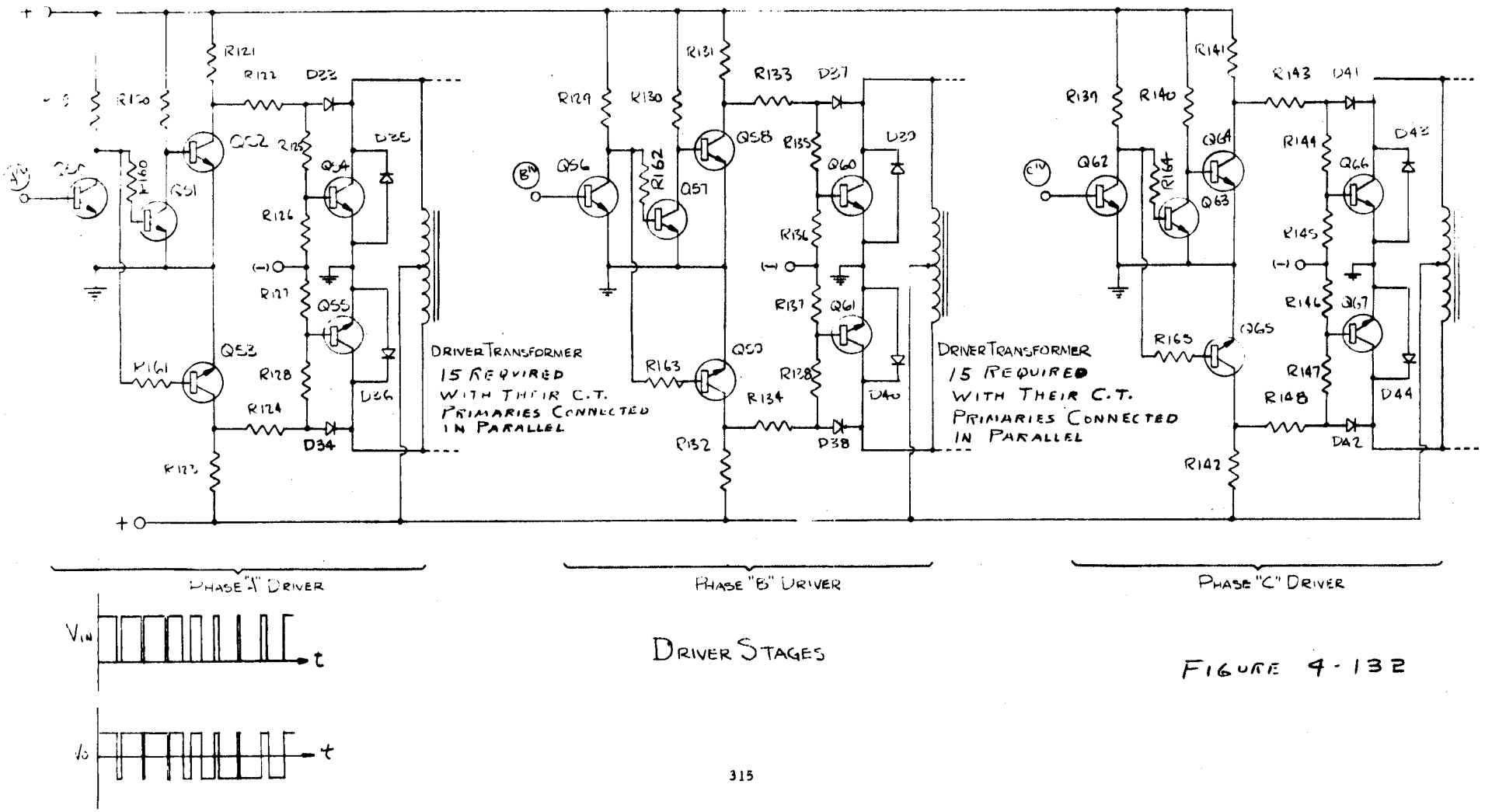
FIGURE 4-130

Parts List - Slicer Amplifier

$Q_{41} \rightarrow Q_{49}$	2N2218
D_{29}, D_{30}, D_{31}	1N756 - 8.2V - .4W
D_{32}	1N751 - 5.1V - .4W
$R_{103}, R_{108}, R_{113}$	27K - $\frac{1}{2}$ W ±5%
$R_{104}, R_{109}, R_{114}$	10K - $\frac{1}{2}$ W ±5%
$R_{105}, R_{110}, R_{115}$	10K - $\frac{1}{2}$ W ±5%
$R_{106}, R_{111}, R_{116}$	47K - $\frac{1}{2}$ W ±5%
$R_{107}, R_{112}, R_{117}$	10K - $\frac{1}{2}$ W ±5%
R_{118}	4.7 K - $\frac{1}{2}$ W ±5%

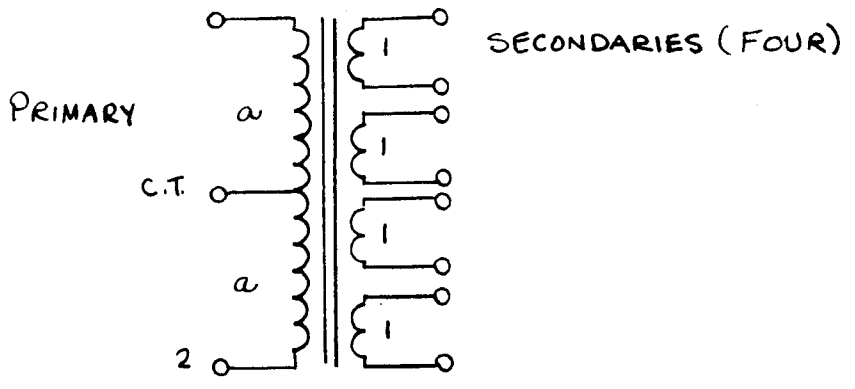
All resistors are composition.

FIGURE 4-131



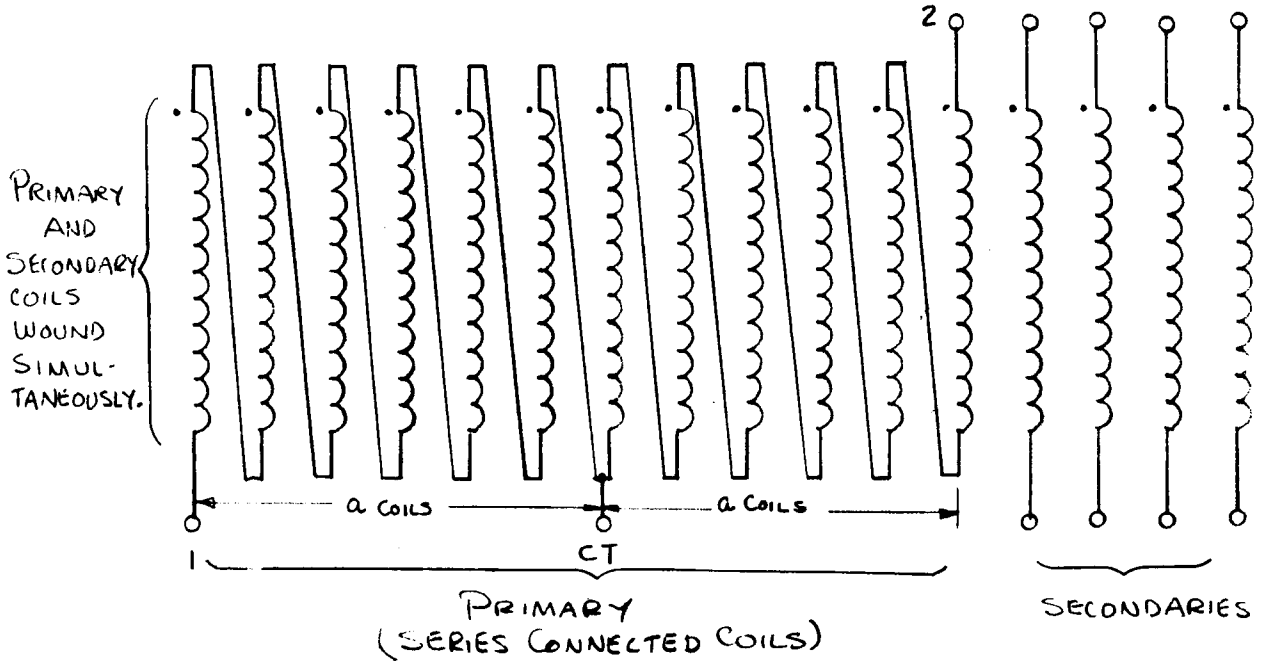
DRIVER STAGES

FIGURE 4-132



TURNS RATIO - a:1

DIAGRAM - REQUIRED TRANSFORMER



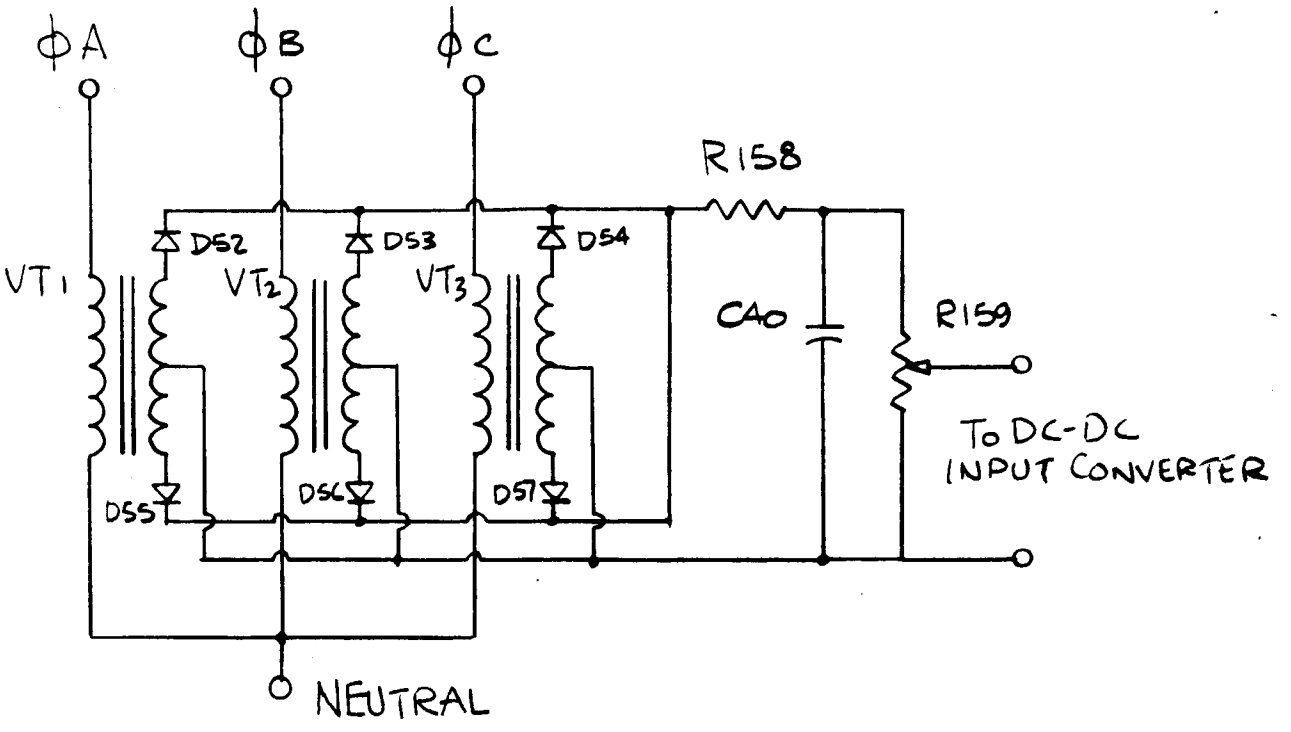
MULTI-FILAR TRANSFORMER COIL CONSTRUCTION TECHNIQUE.

FIGURE 9-133

Q_{50}, Q_{51}, Q_{56}, Q_{57}, Q_{62}, Q_{63}	2N2218	
Q_{54}, Q_{55}, Q_{60}, Q_{61}, Q_{66}, Q_{67}	2N1937	
Q_{52}, Q_{53}, Q_{58}, Q_{59}, Q_{64}, Q_{65}	2N1723	
D_{33}, D_{34}, D_{37}, D_{38}, D_{41}, D_{42}	1N3875	
D_{35}, D_{36}, D_{39}, D_{40}, D_{43}, D_{44}	1N3915	
R_{119}, R_{129}, R_{139}	150Ω-1W ±5%	Composition
R_{160}, R_{162}, R_{164}	1K - $\frac{1}{2}$ W ±5%	Composition
R_{120}, R_{130}, R_{140}	180Ω-$\frac{1}{2}$ W ±5%	Composition
R_{161}, R_{163}, R_{165}	10Ω-$\frac{1}{2}$ W ±5%	Composition
R_{121}, R_{123}, R_{131}, R_{132}, R_{141}, R_{142}	10Ω-10W ±5%	Wire Wound
R_{122}, R_{124}, R_{125}, R_{128}, R_{133}, R_{134}, R_{135}, R_{138}, R_{143}, R_{144}, R_{147}, R_{148}	1Ω-10W ±5%	Wire Wound
R_{126}, R_{127}, R_{136}, R_{137}, R_{145}, R_{146}	100Ω-10W ±5%	Wire Wound

Driver Transformers (45 required) - TA -(Class H)

FIGURE 4-134



VOLTAGE REGULATOR SENSE CIRCUIT

FIGURE 4-135

Parts List - Voltage Regulator Sense Circuit

$D_{52} \rightarrow D_{57}$	1N659
VT_1, VT_2, VT_3	(Class H) Voltage Transformers a = 23 : 1 : 1
R_{158}	180 - $\frac{1}{2}$ W ±5% Composition
R_{159}	1 K pot.- 1 W ±5% Wire Wound
C_{40}	4.7 μfd / 10 WVDC

FIGURE 4-136

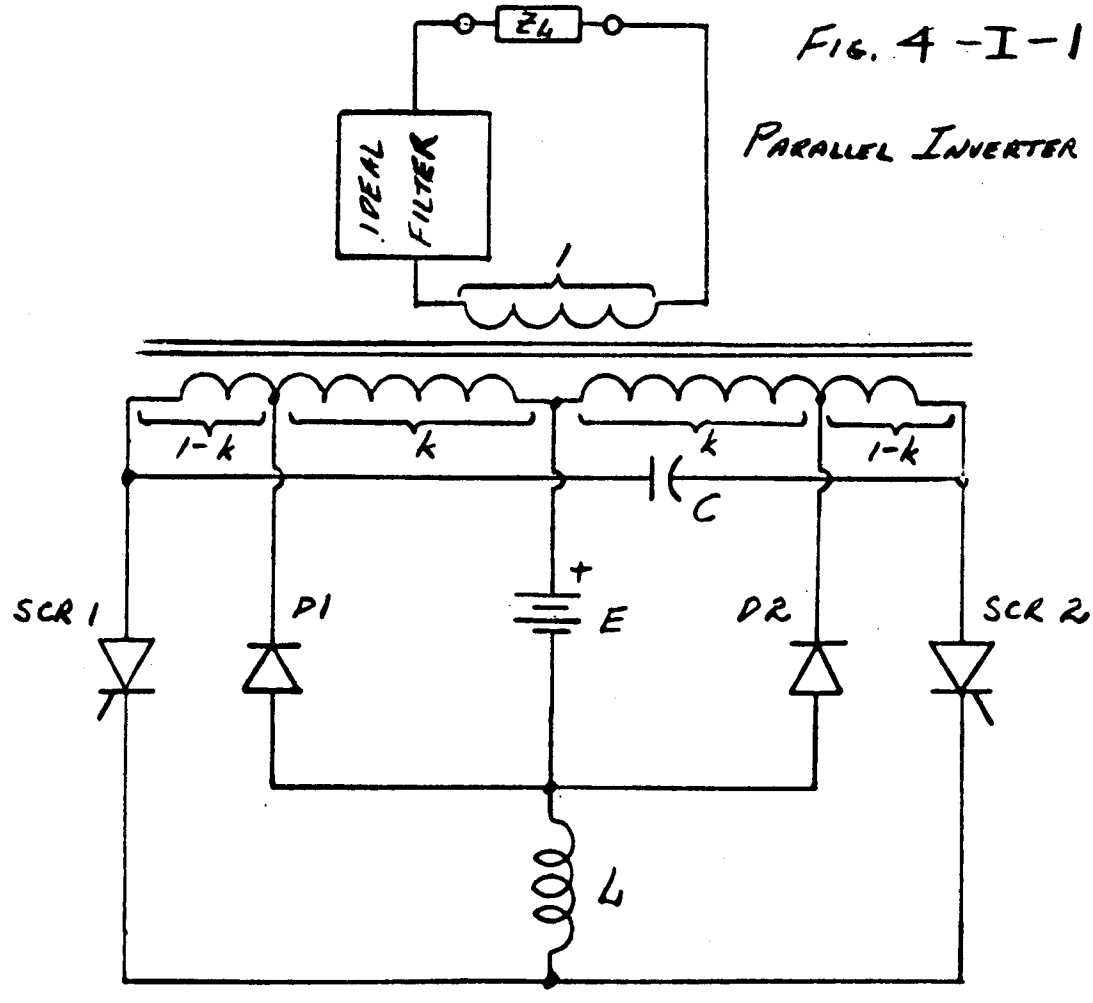


FIG. 4-I-1

PARALLEL INVERTER CIRCUIT

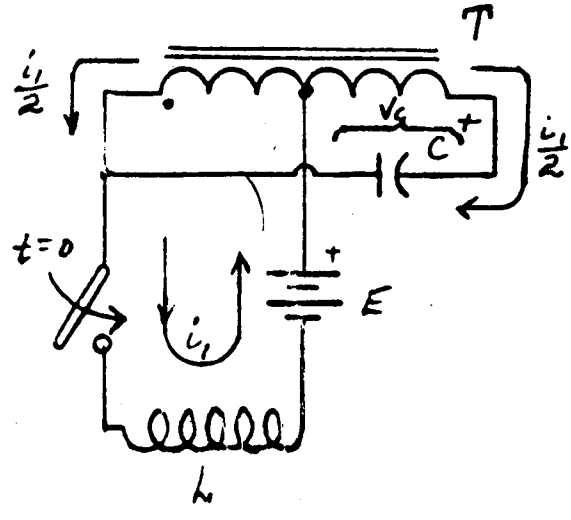


FIG. 4-I-2

EQUIVALENT CKT. OF 4-I-1

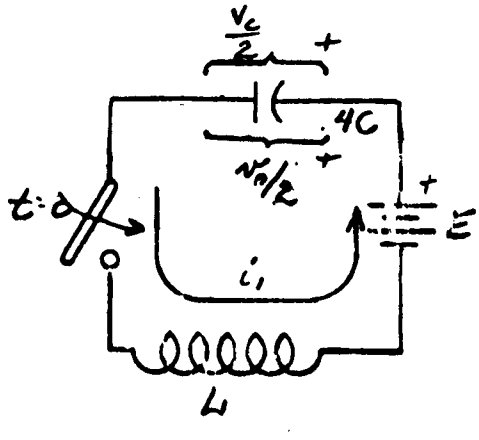


FIG. 4-I-3

EQUIVALENT CKT. OF 4-I-2

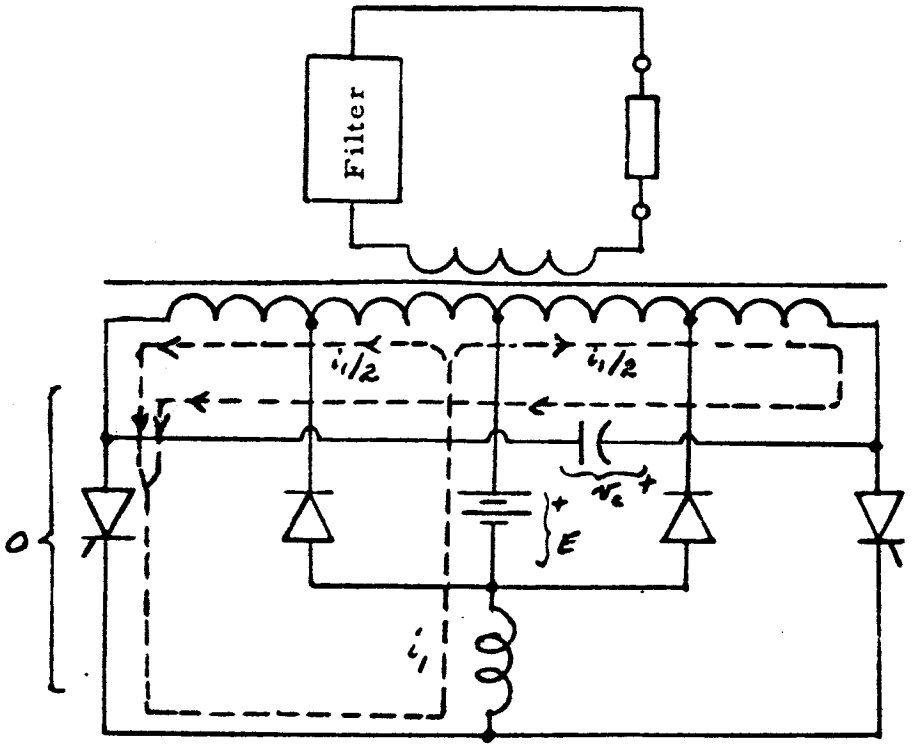


FIG. 4-I-4 CAPACITOR CHARGE CYCLE: $v_c < 2E/k$

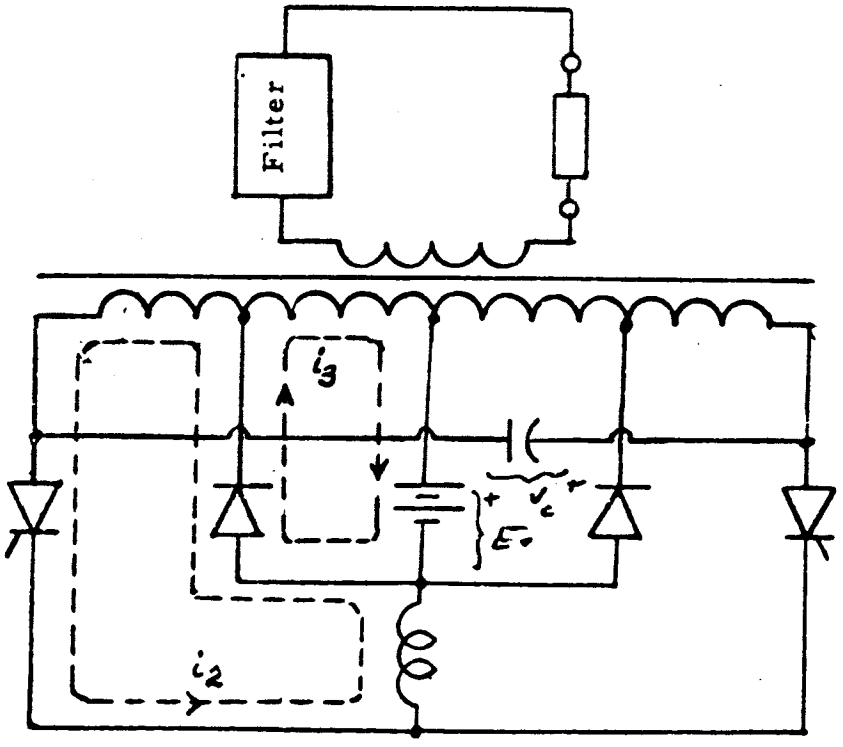


FIG. 4-I-5 CAPACITOR CHARGE CYCLE: $v_c = 2E/k$

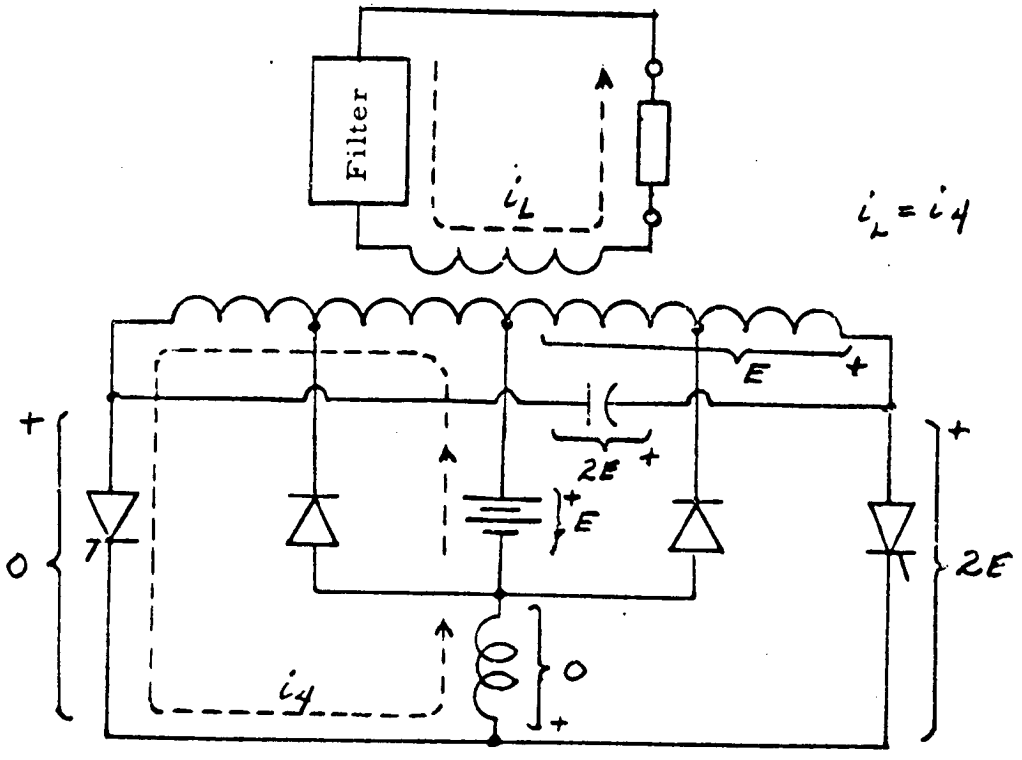


FIG. 4-I-6 CIRCUIT IMMEDIATELY BEFORE COMMUTATION

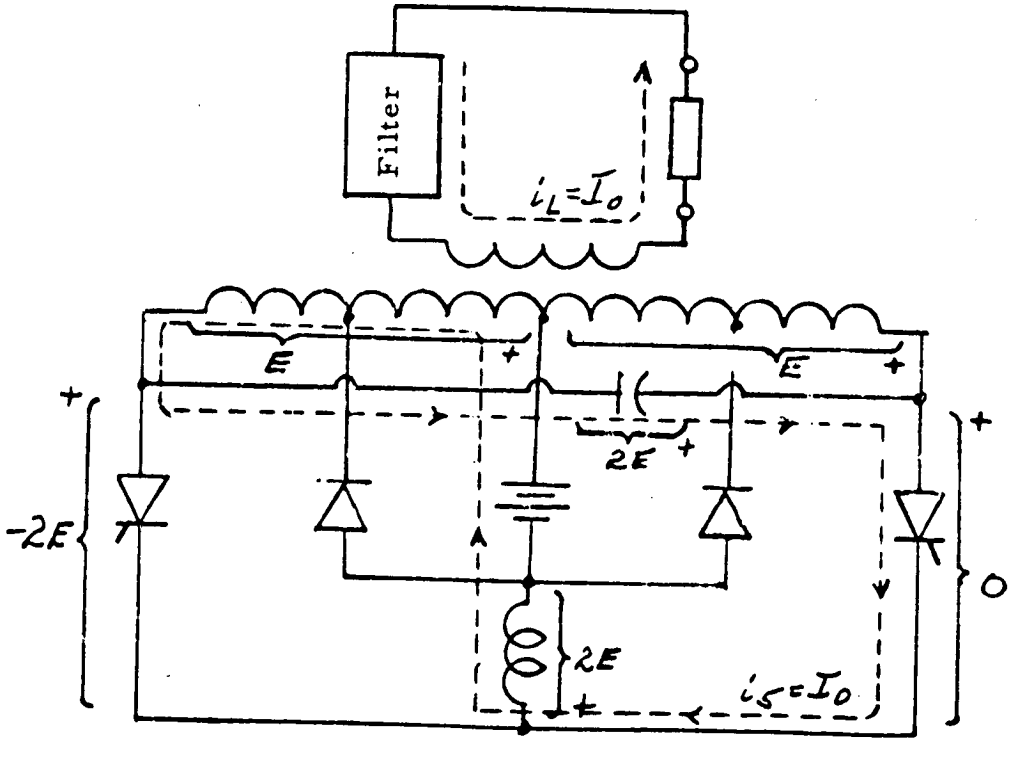


FIG. 4-I-7 CIRCUIT IMMEDIATELY AFTER COMMUTATION

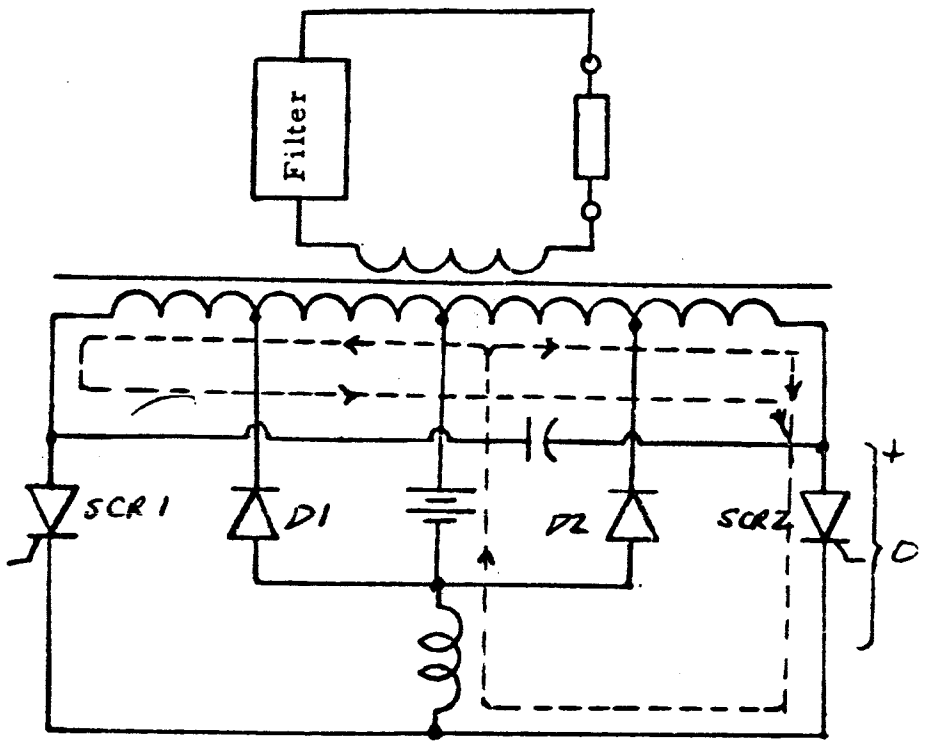


FIG. 4-I-8 CAPACITOR CHARGING CURRENTS IMMEDIATELY AFTER COMMUTATION OF SCR 1 (TURN-ON OF SCR 2)

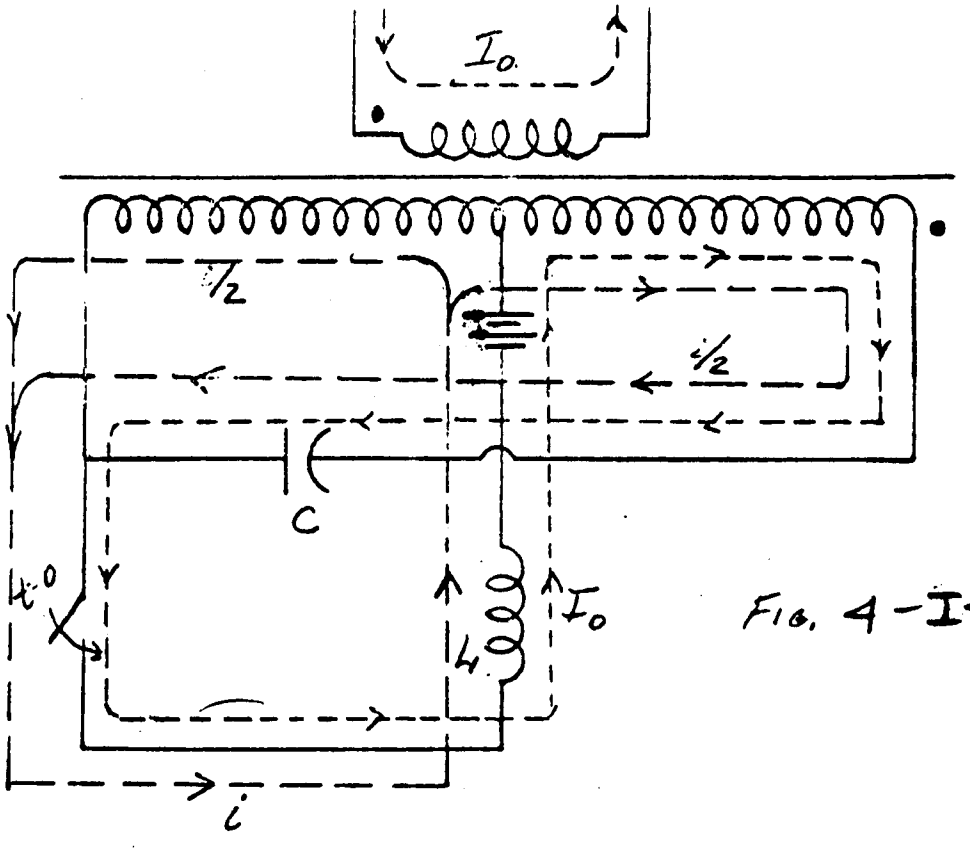


FIG. 4-I-9

CIRCUIT AT INSTANT OF TURNING ON OF SCR 1.

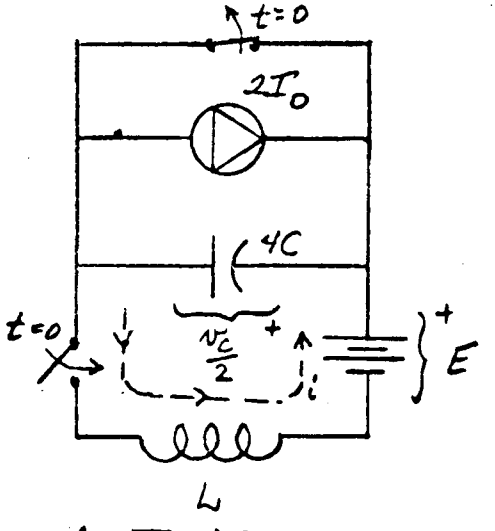


FIG 4-I-10

EQUIVALENT CKT. OF FIG. 4-I-9

STARTING AND STEADY STATE WAVEFORMS
McMURRAY-BEDFORD INVERTER RESISTIVE LOAD (WITH TUNED FILTER)

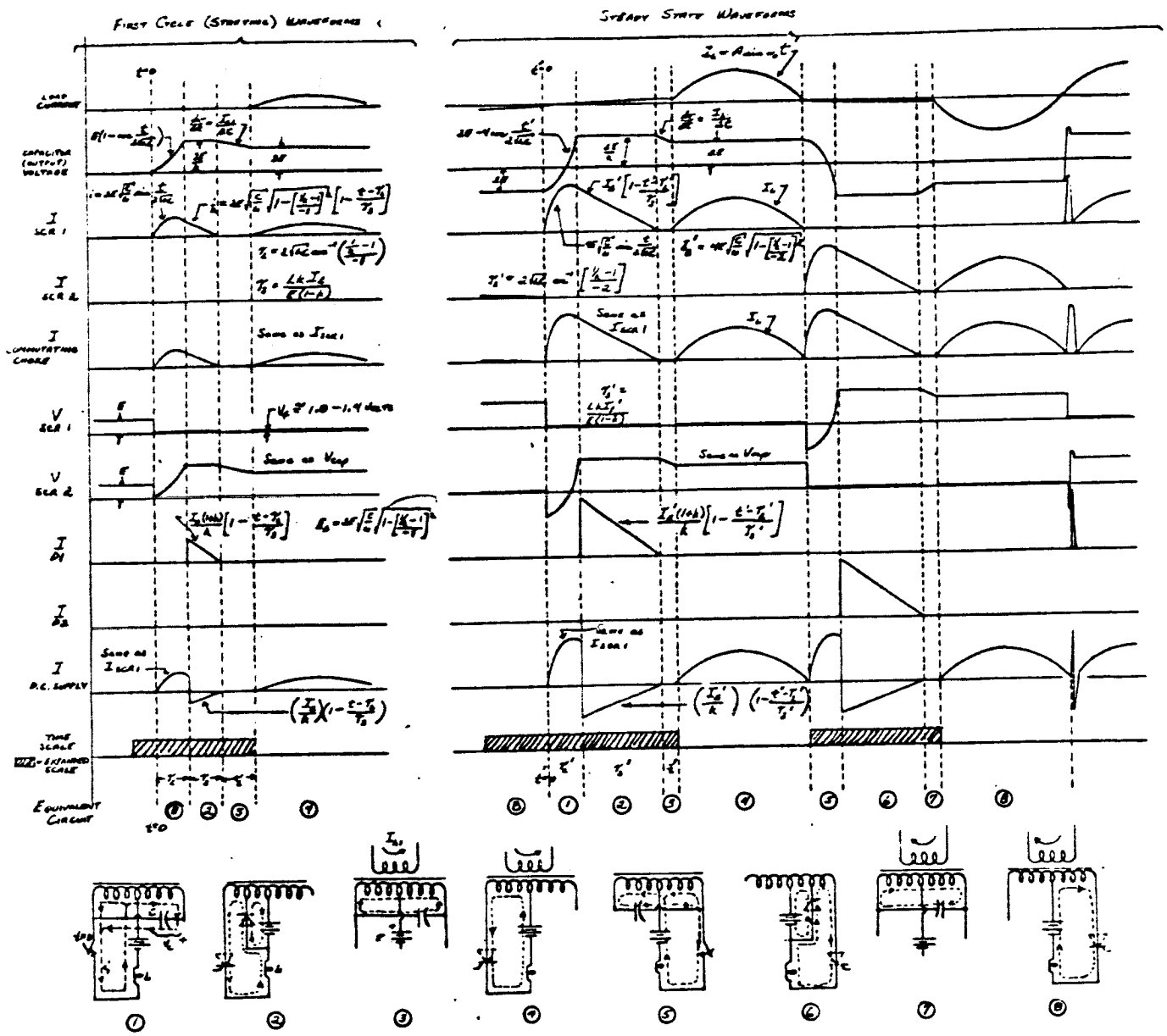
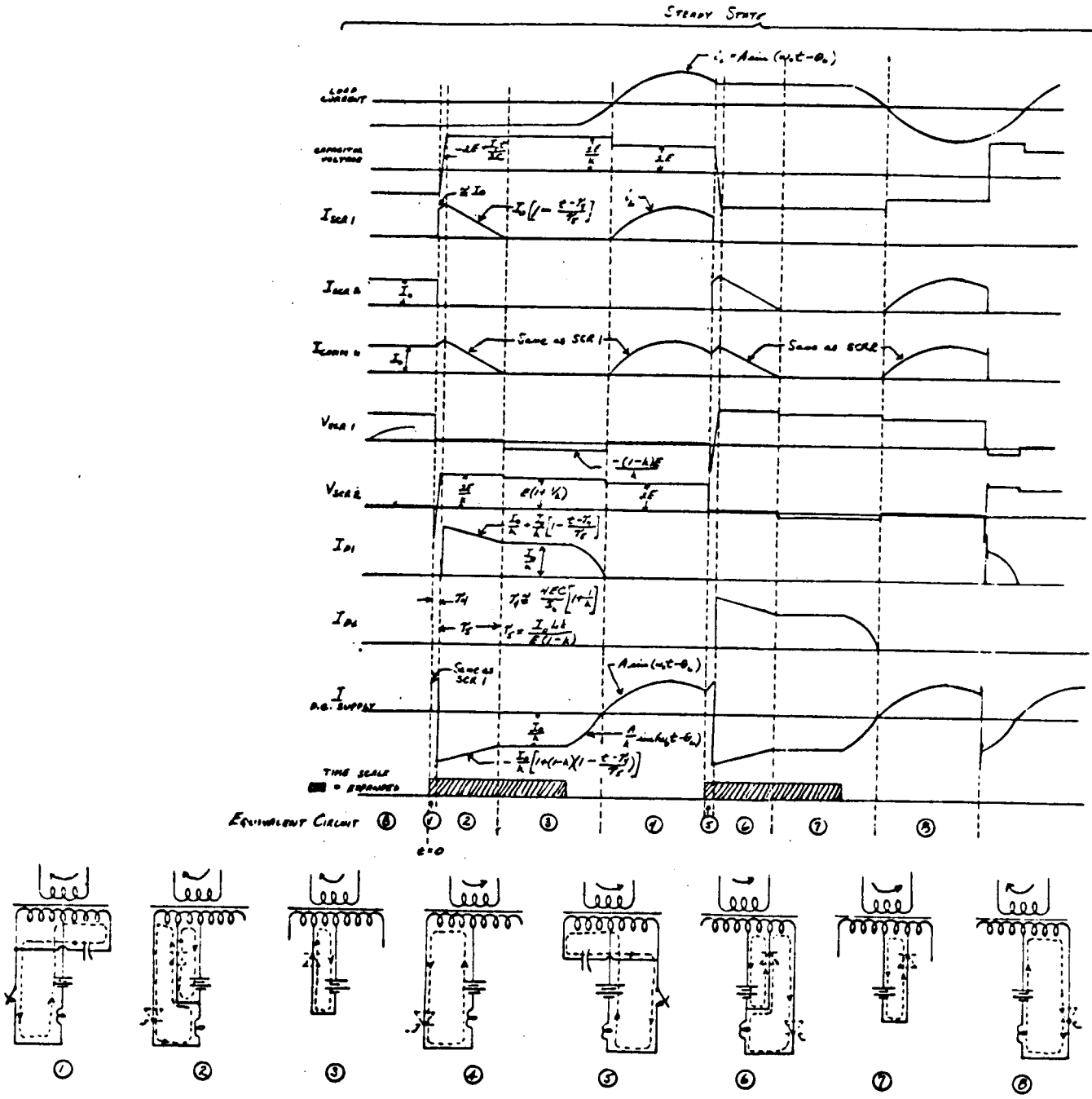


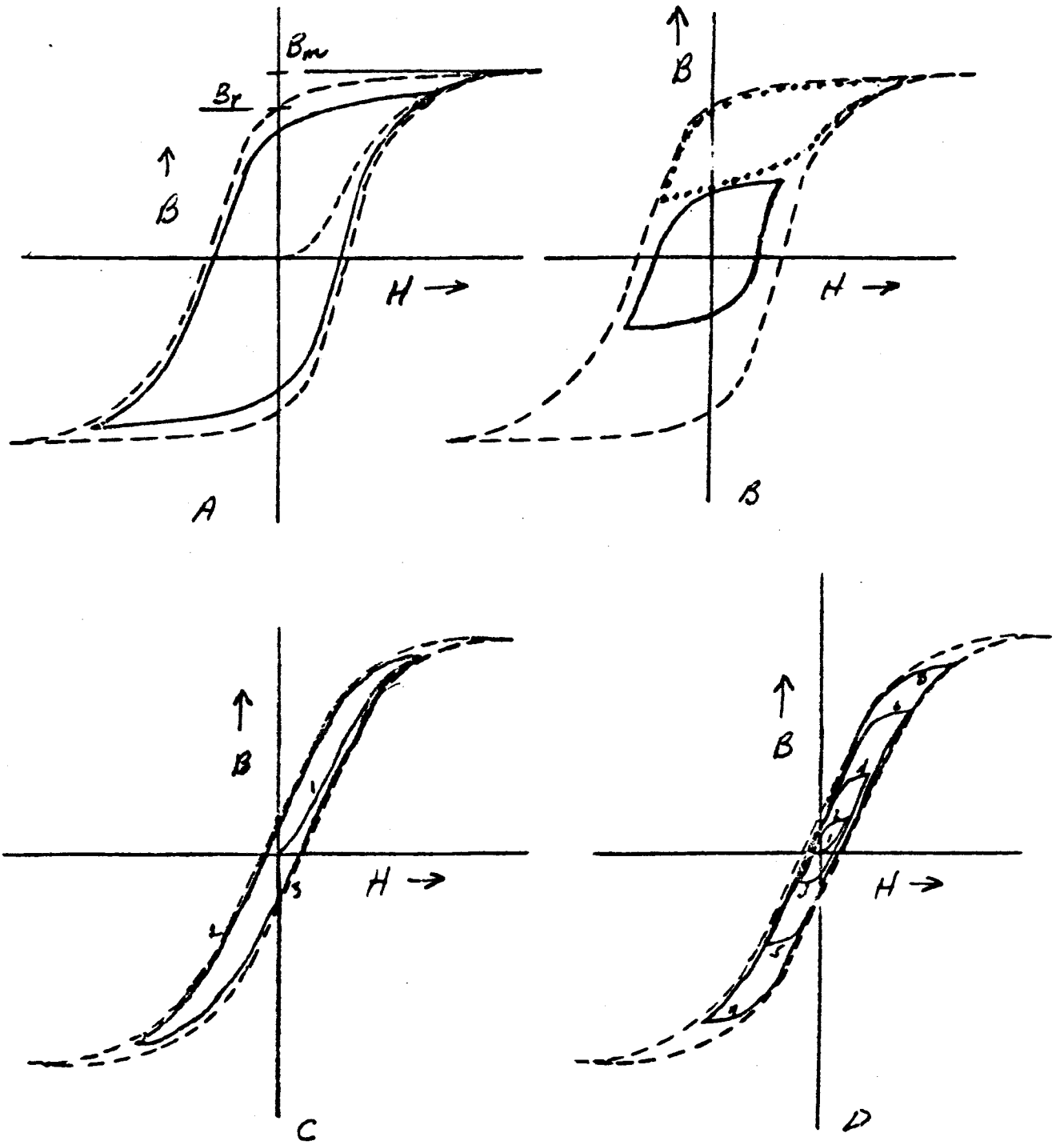
FIGURE 4-I-11

McMURRAY-BEDFORD INVERTER WAVEFORMS INDUCTIVE LOADING



NOTE: STARTING WAVEFORMS FOR THIS CIRCUIT ARE THE SAME AS FOR THE INVERTING LOAD (Fig 4-I-11)

FIGURE 4-I-12



DYNAMIC HYSTERESIS LOOPS – OUTPUT XFMR CORE

FIG. 4-I-13

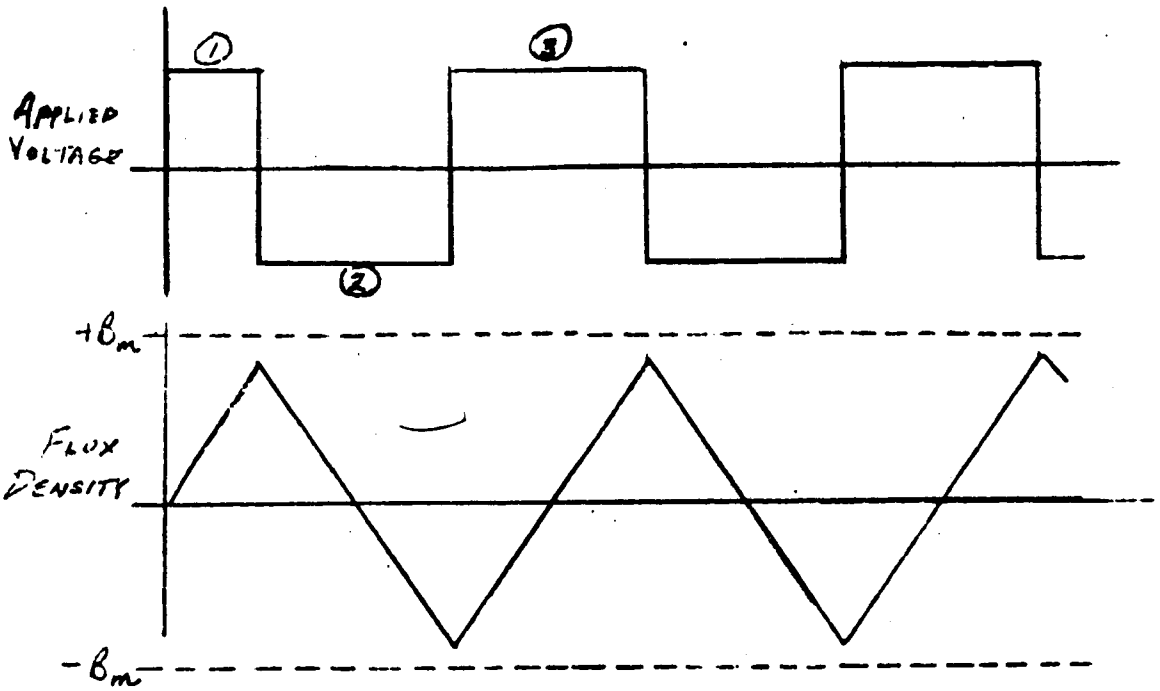


FIG. 4-I-14 QUARTER CYCLE STARTING WAVEFORMS

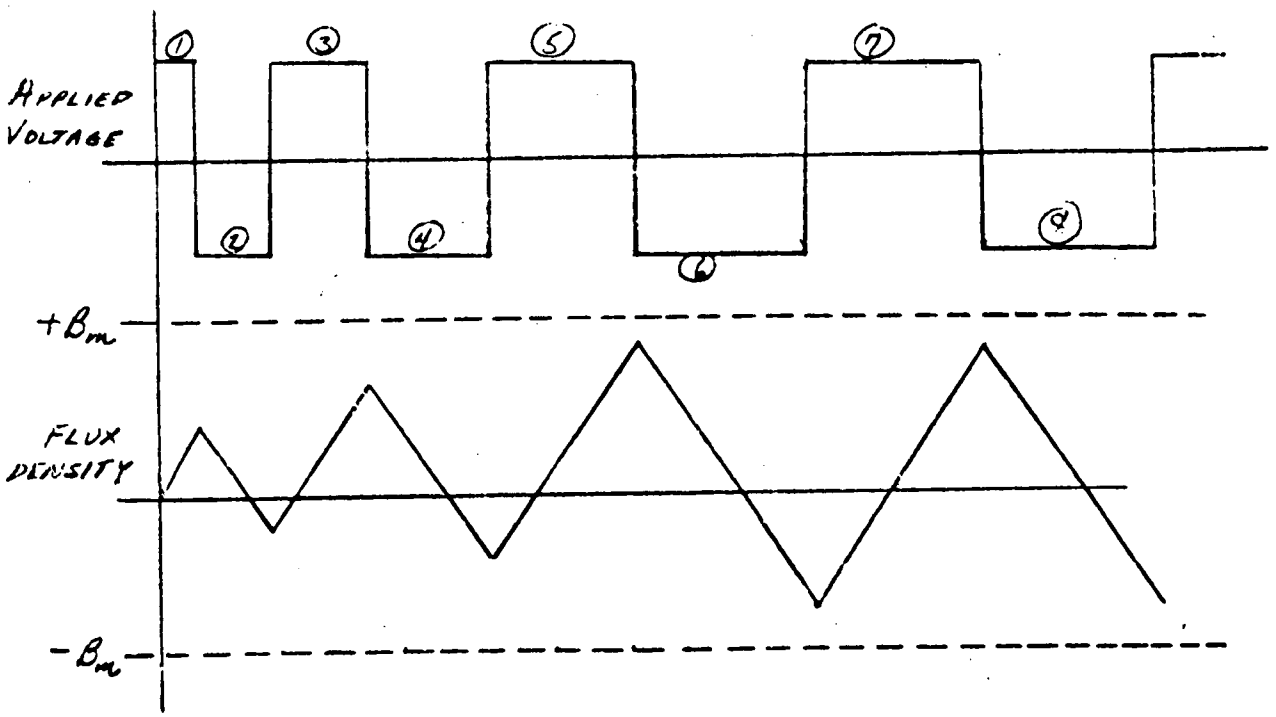


FIG. 4-I-15 HIGH FREQUENCY STARTING WAVEFORMS

Reliability Block Diagram For The 3200 CPS – 10 KW Static Inverter

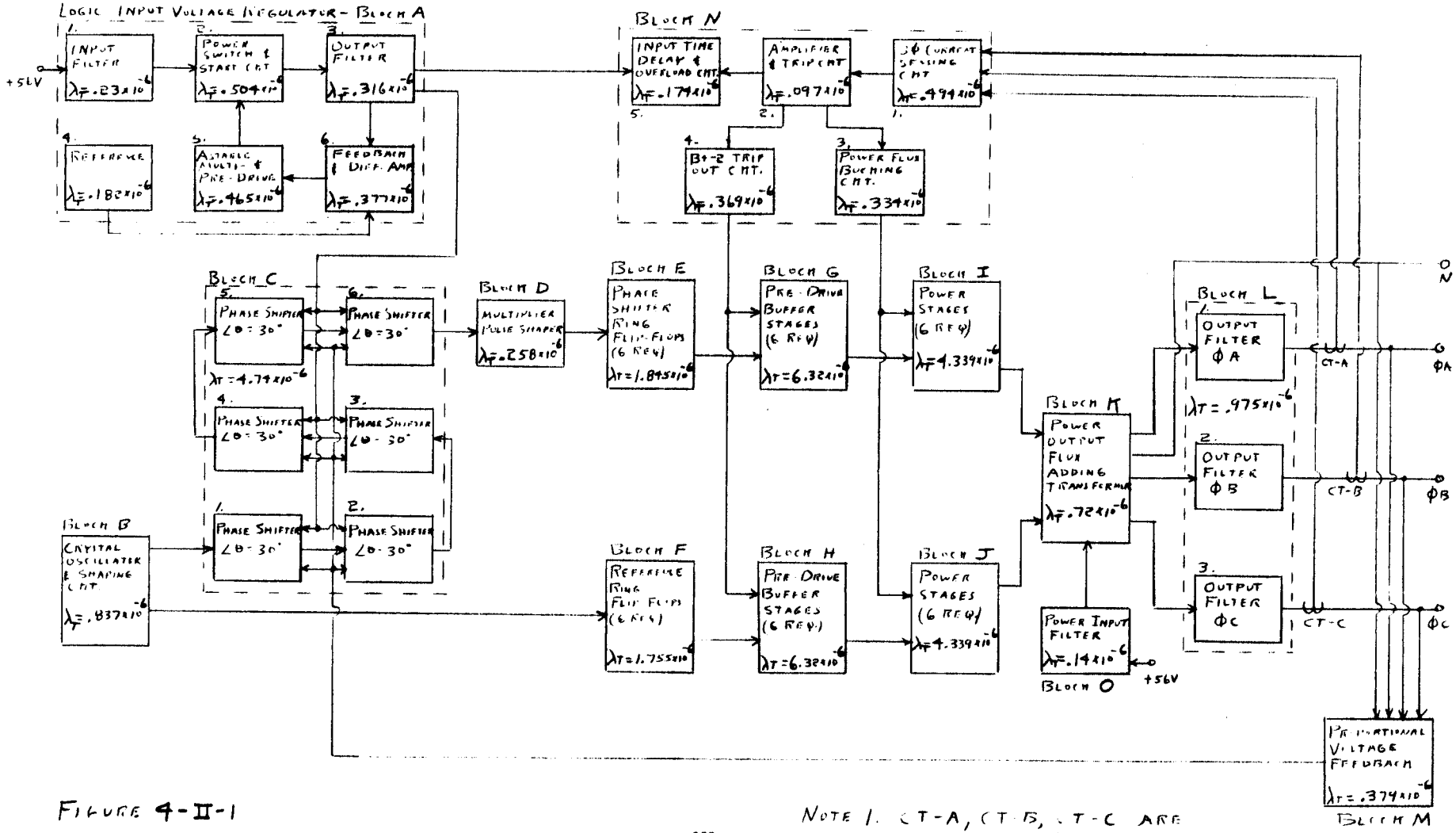


Figure 4-II-1

Note 1. CT-A, CT-B, CT-C are included as part of Block N

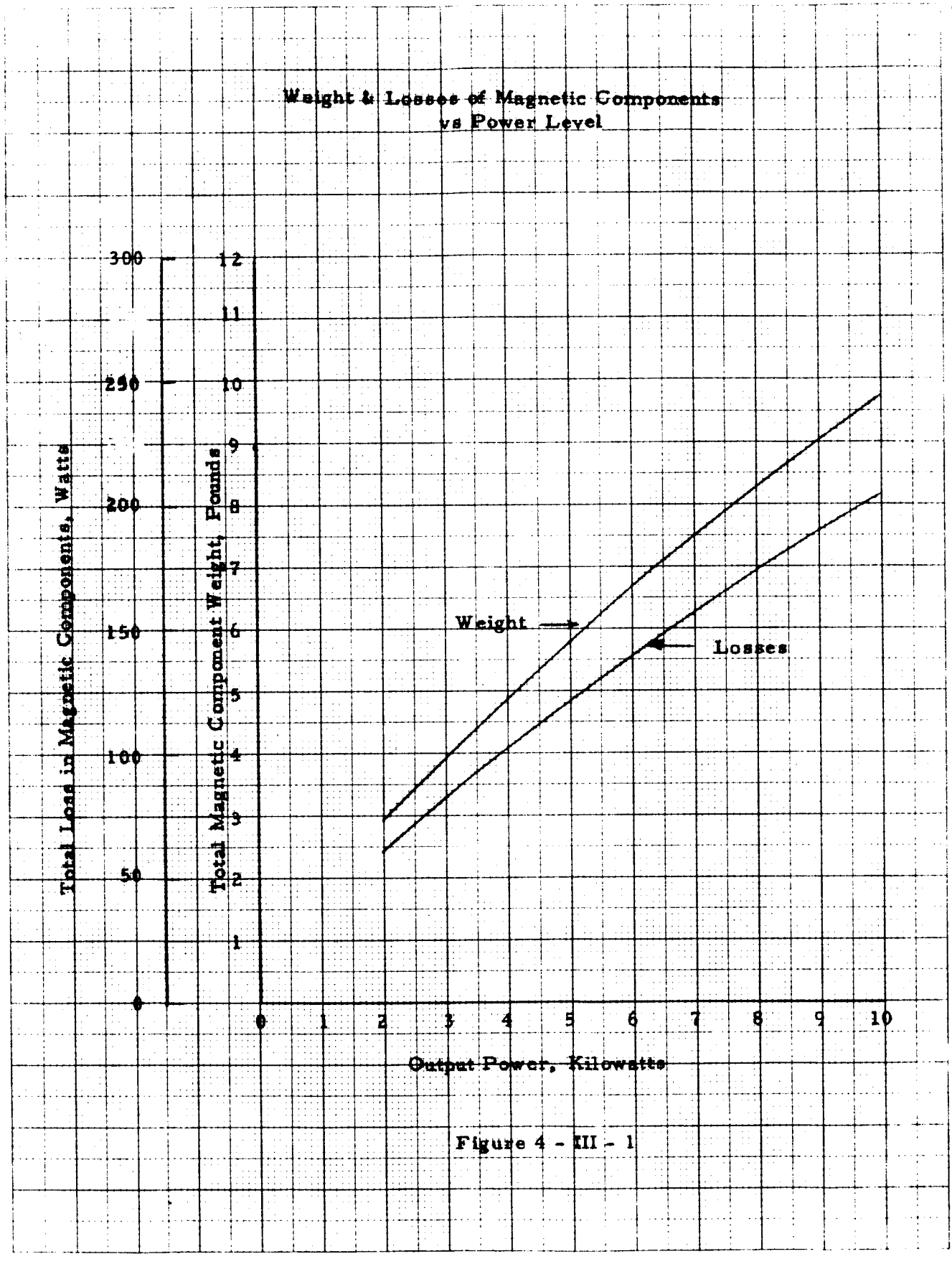
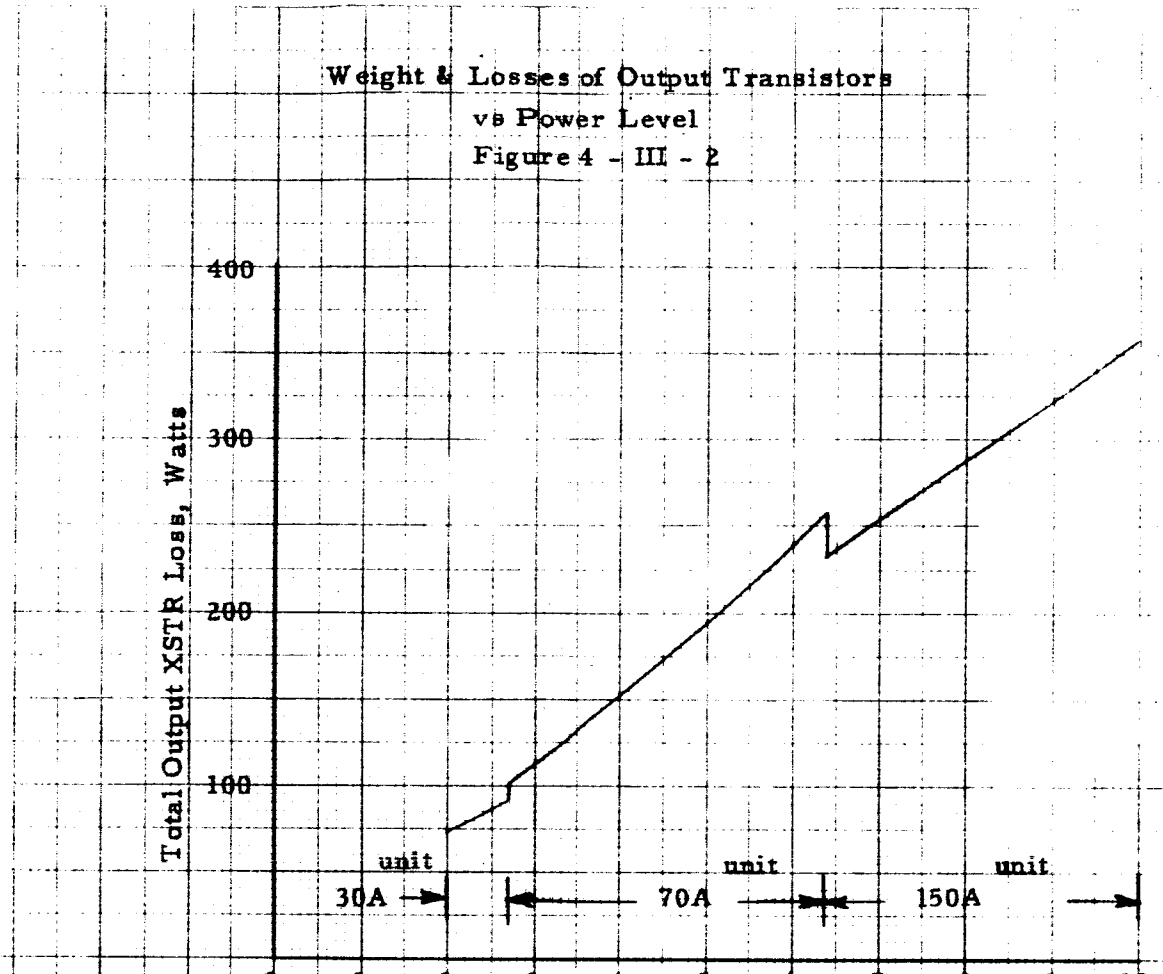


Figure 4 - III - 1

Weight & Losses of Output Transistors
vs Power Level
Figure 4 - III - 2



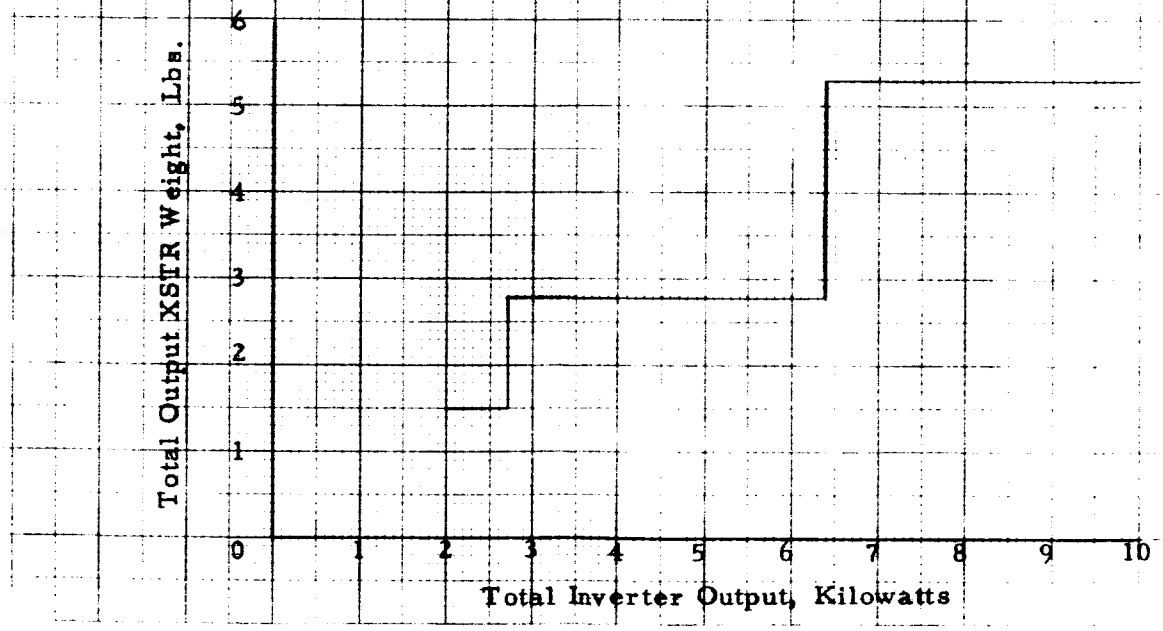
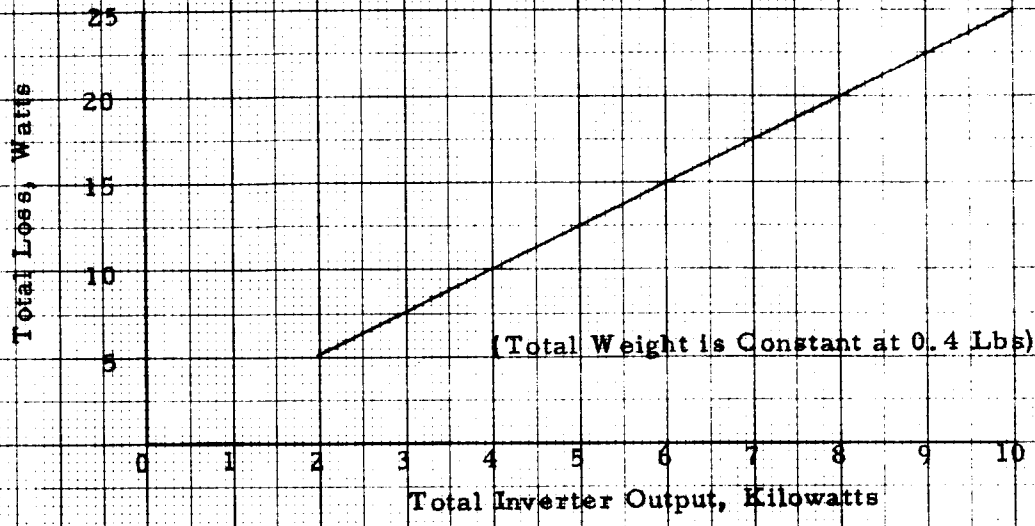


Figure 4 - III - 3

Loss vs. Output Power for Base Limiting Diodes



Loss & Weight vs Output Power for Reactive Diodes

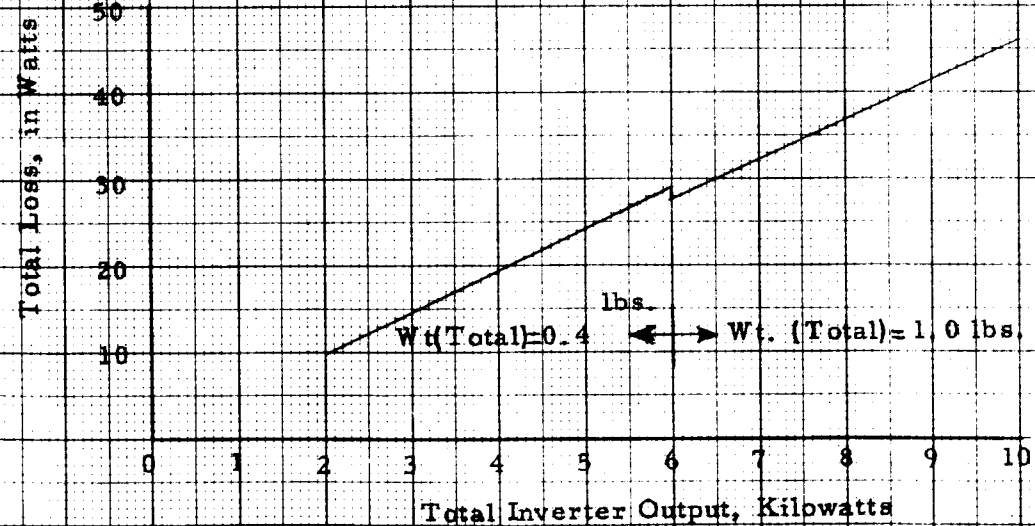
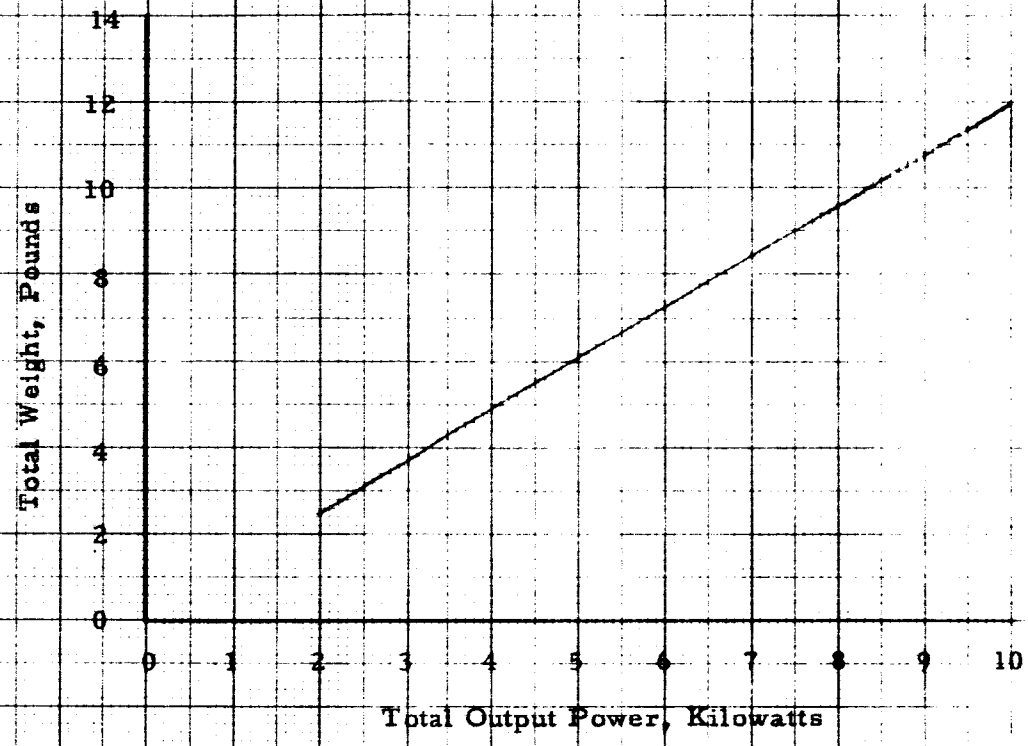
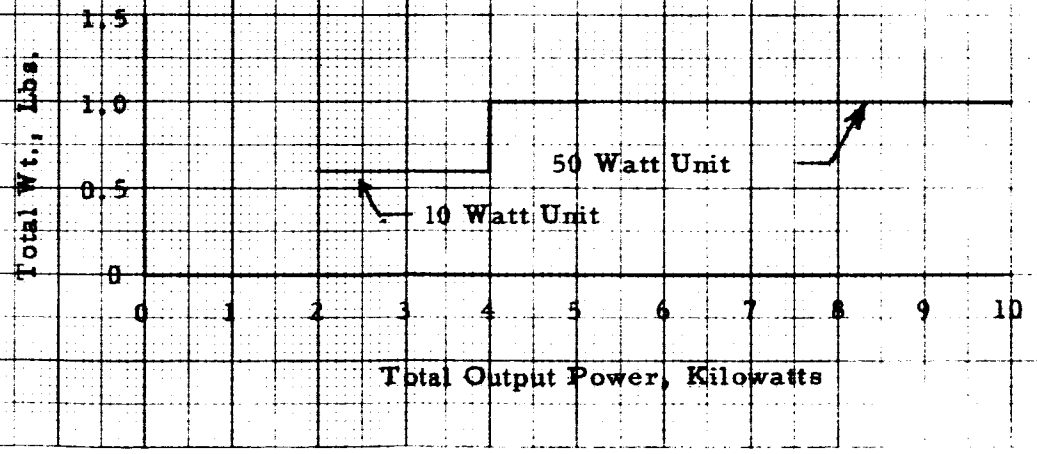


Figure 4 - III - 4

Capacitor Weight vs Inverter Rating

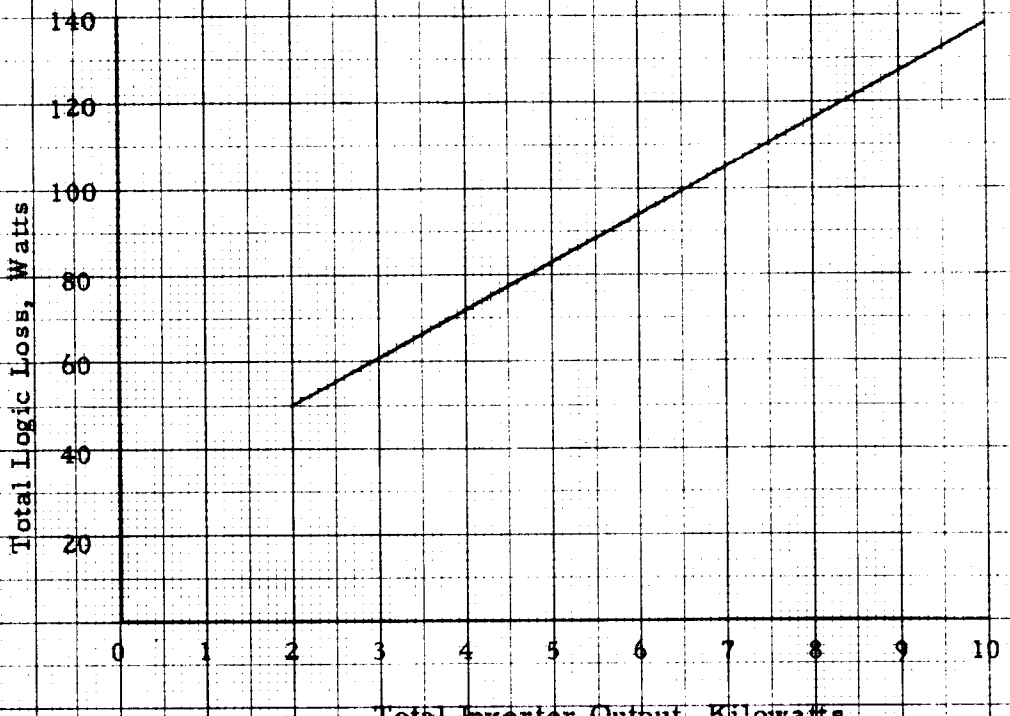


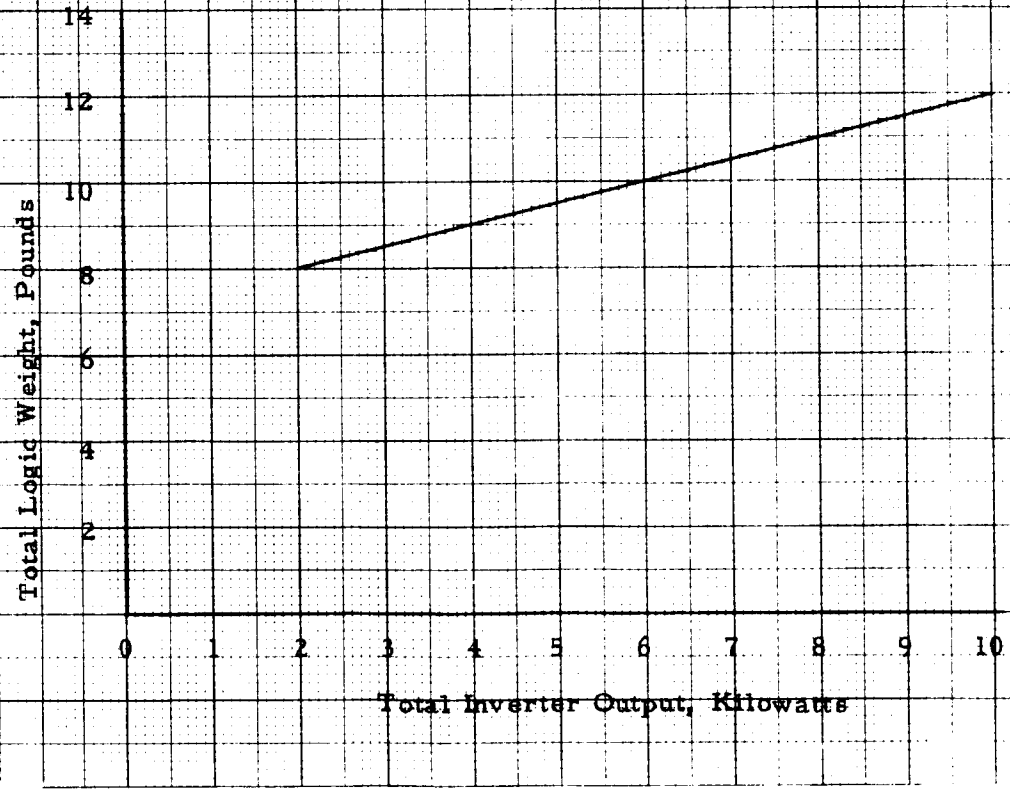
Weight vs Inverter Output Rating for Zener Diodes



Weight & Losses of Logic As a Function of Inverter Power Rating

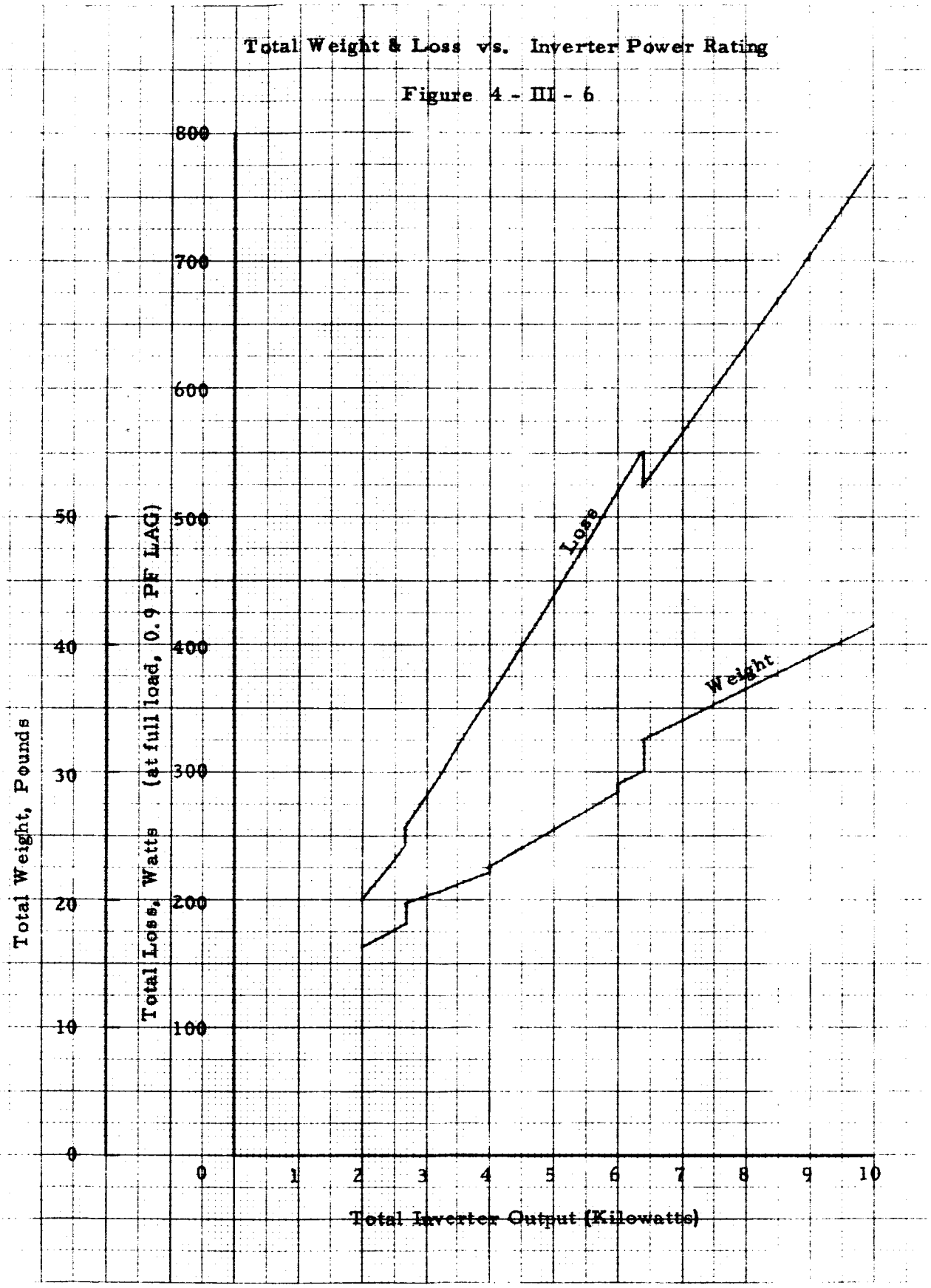
Figure 4 - III - 5



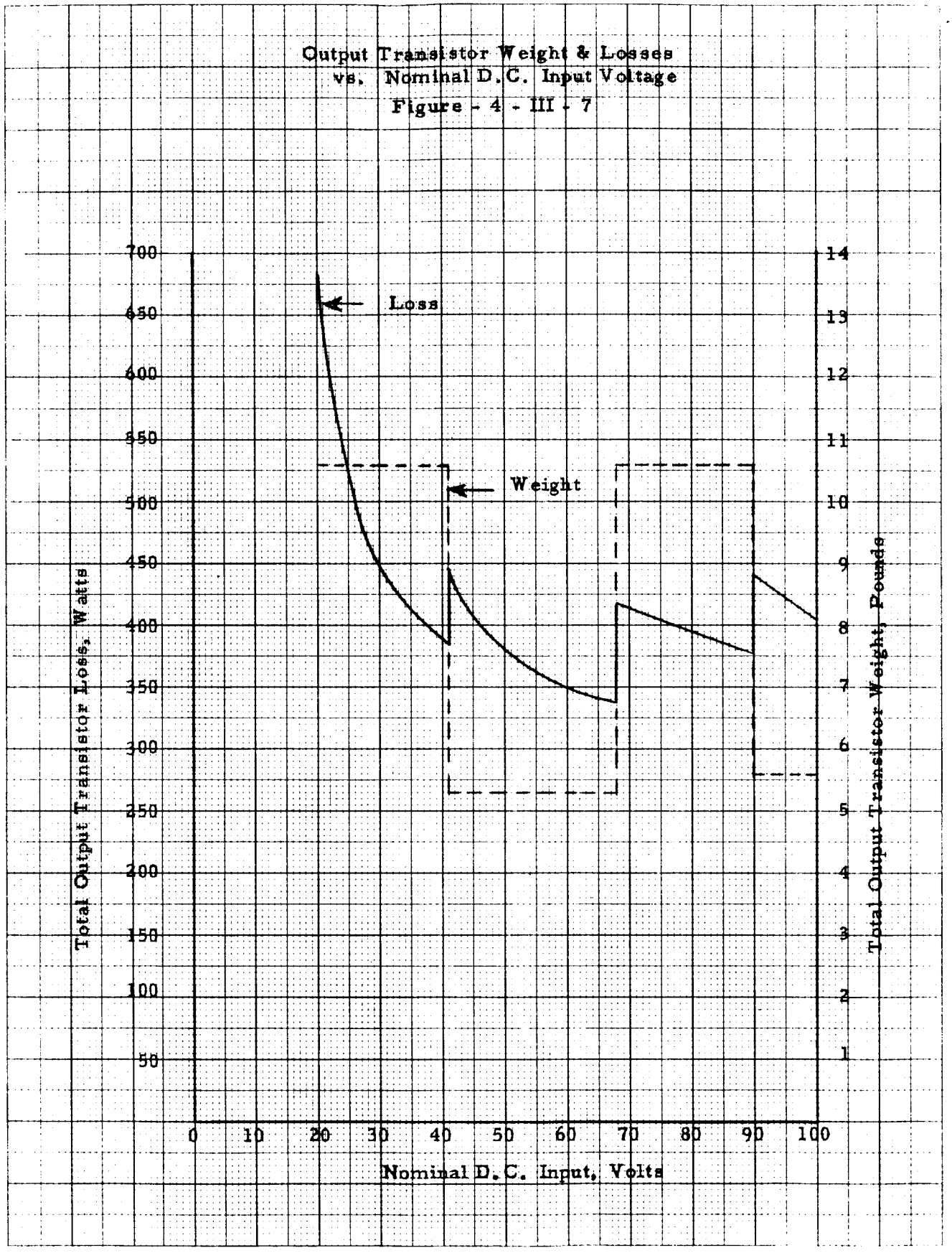


Total Weight & Loss vs. Inverter Power Rating

Figure 4 - III - 6

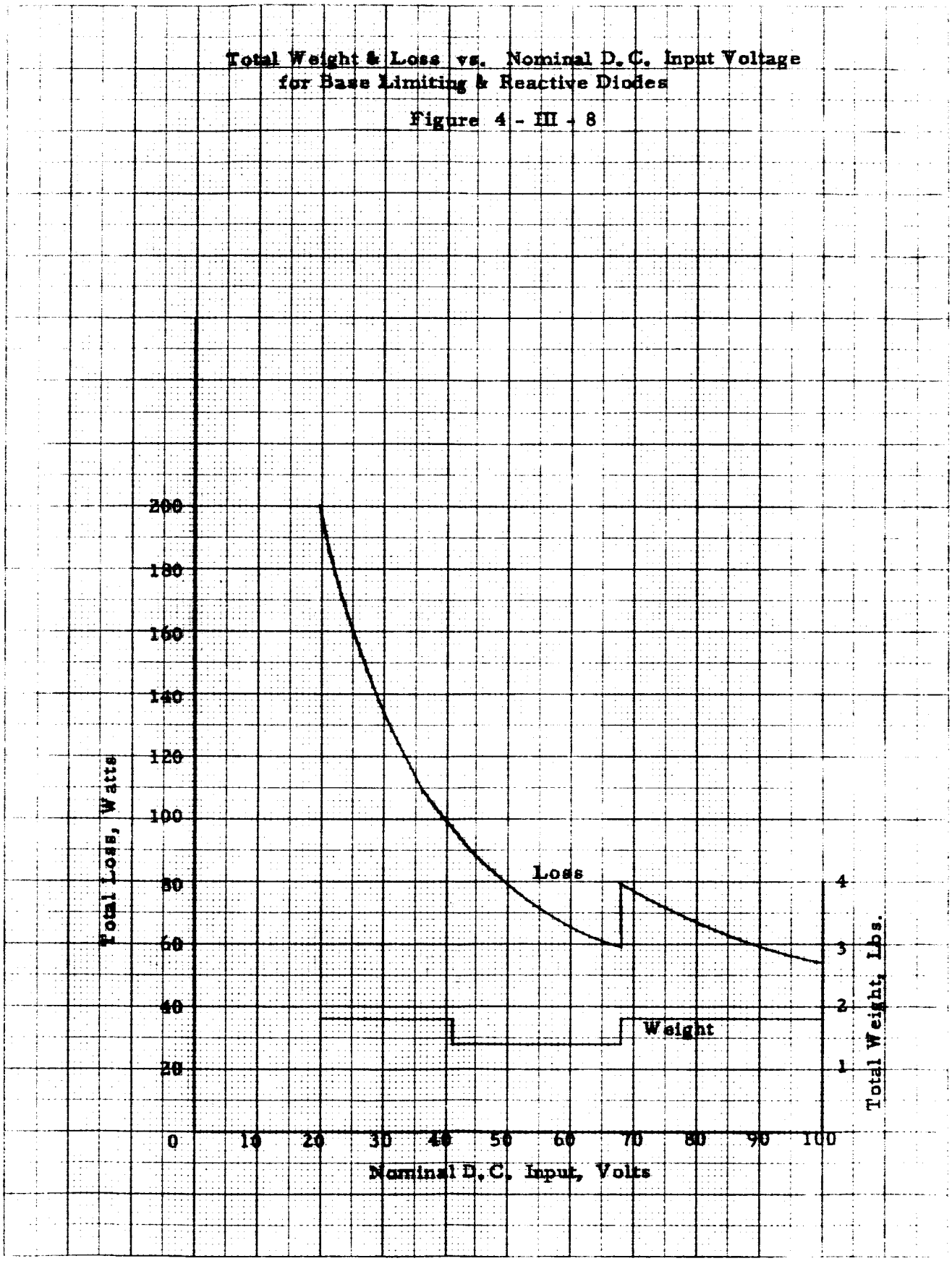


Output Transistor Weight & Losses
vs. Nominal D.C. Input Voltage
Figure - 4 - III - 7



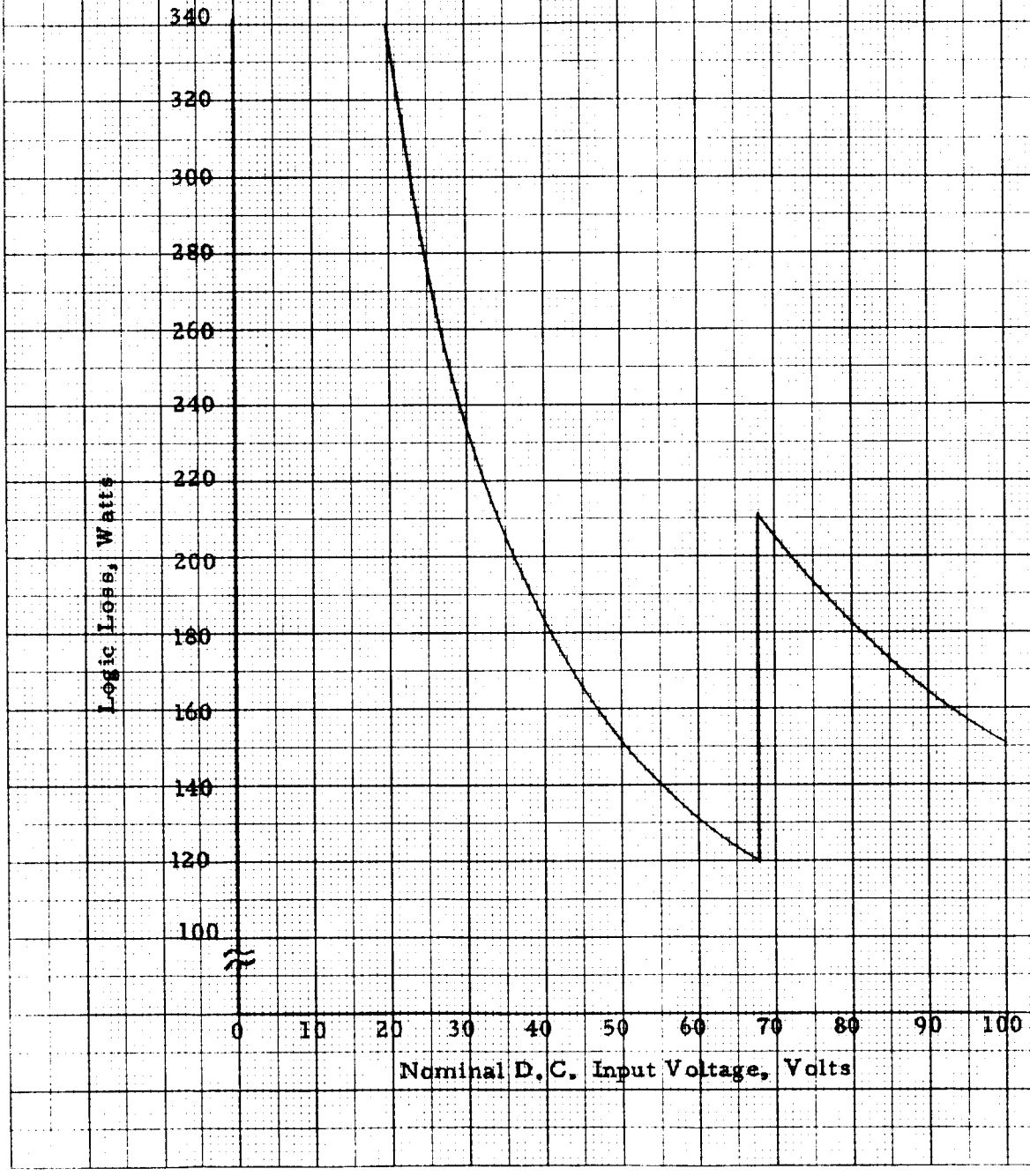
Total Weight & Loss vs. Nominal D.C. Input Voltage
for Base Limiting & Reactive Diodes

Figure 4 - III - 8

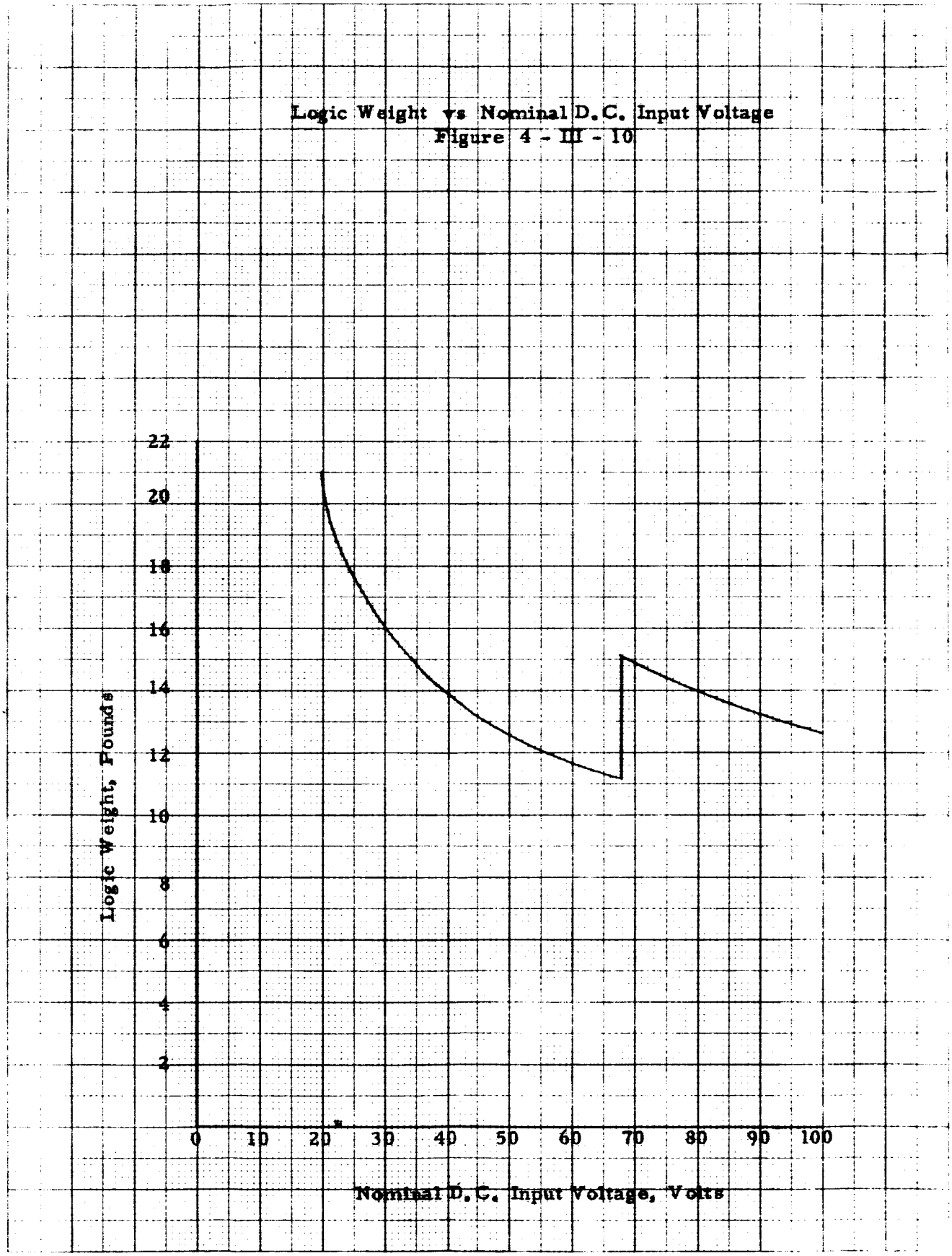


Logic Loss vs. Nominal D.C. Input Voltage

Figure 4 - III - 9

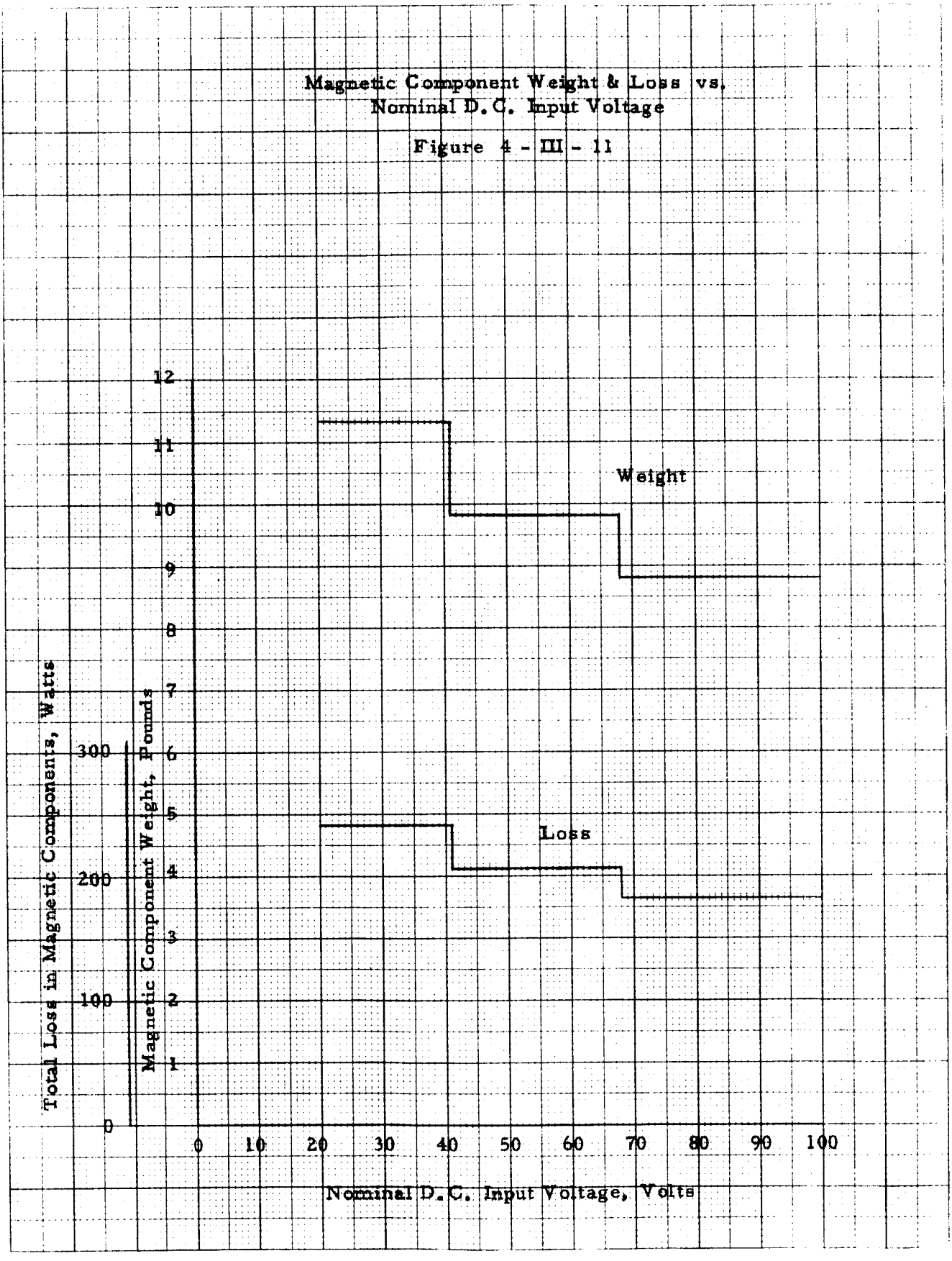


Logic Weight vs Nominal D.C. Input Voltage
Figure 4 - III - 10



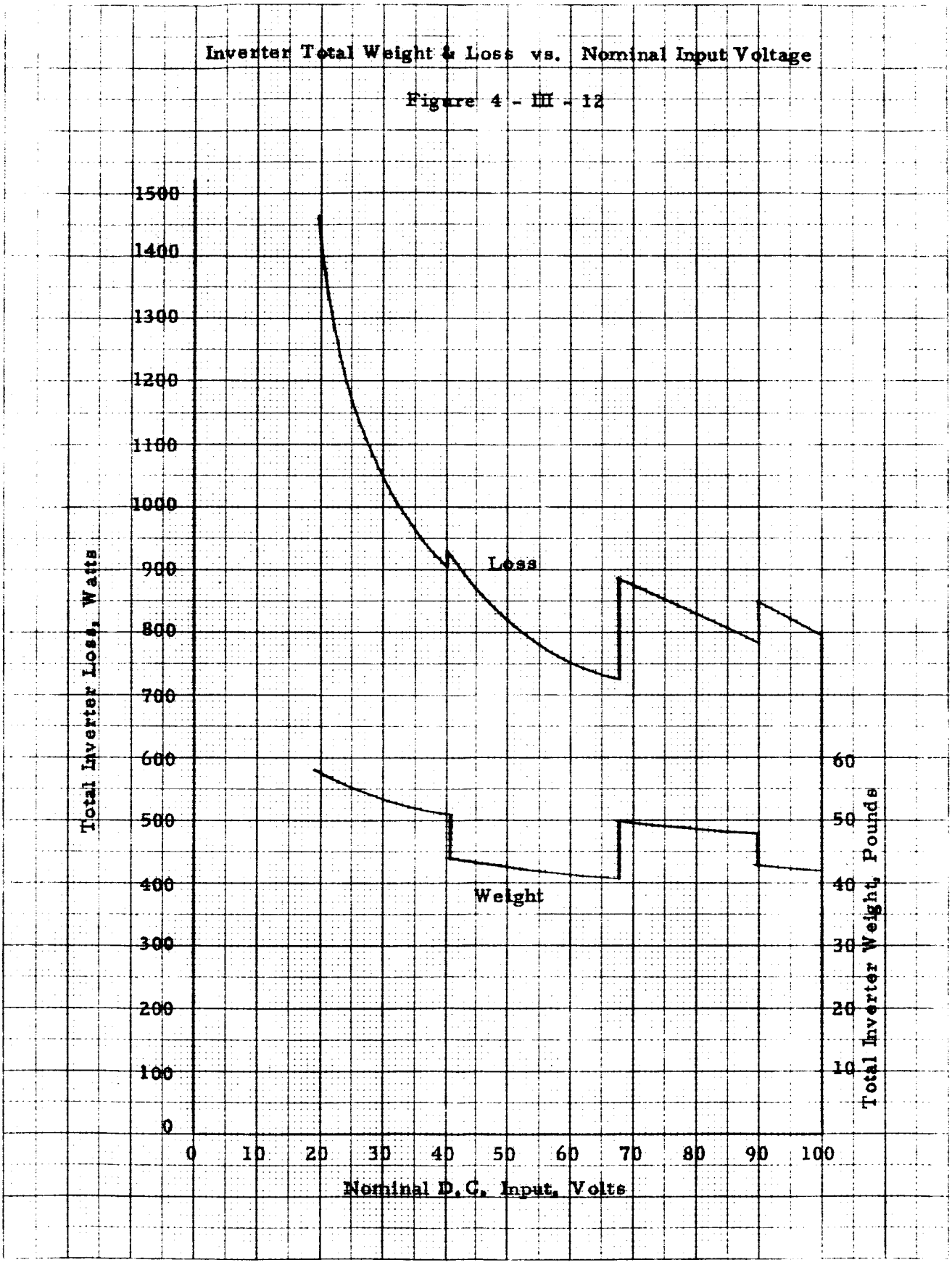
Magnetic Component Weight & Loss vs.
Nominal D.C. Input Voltage

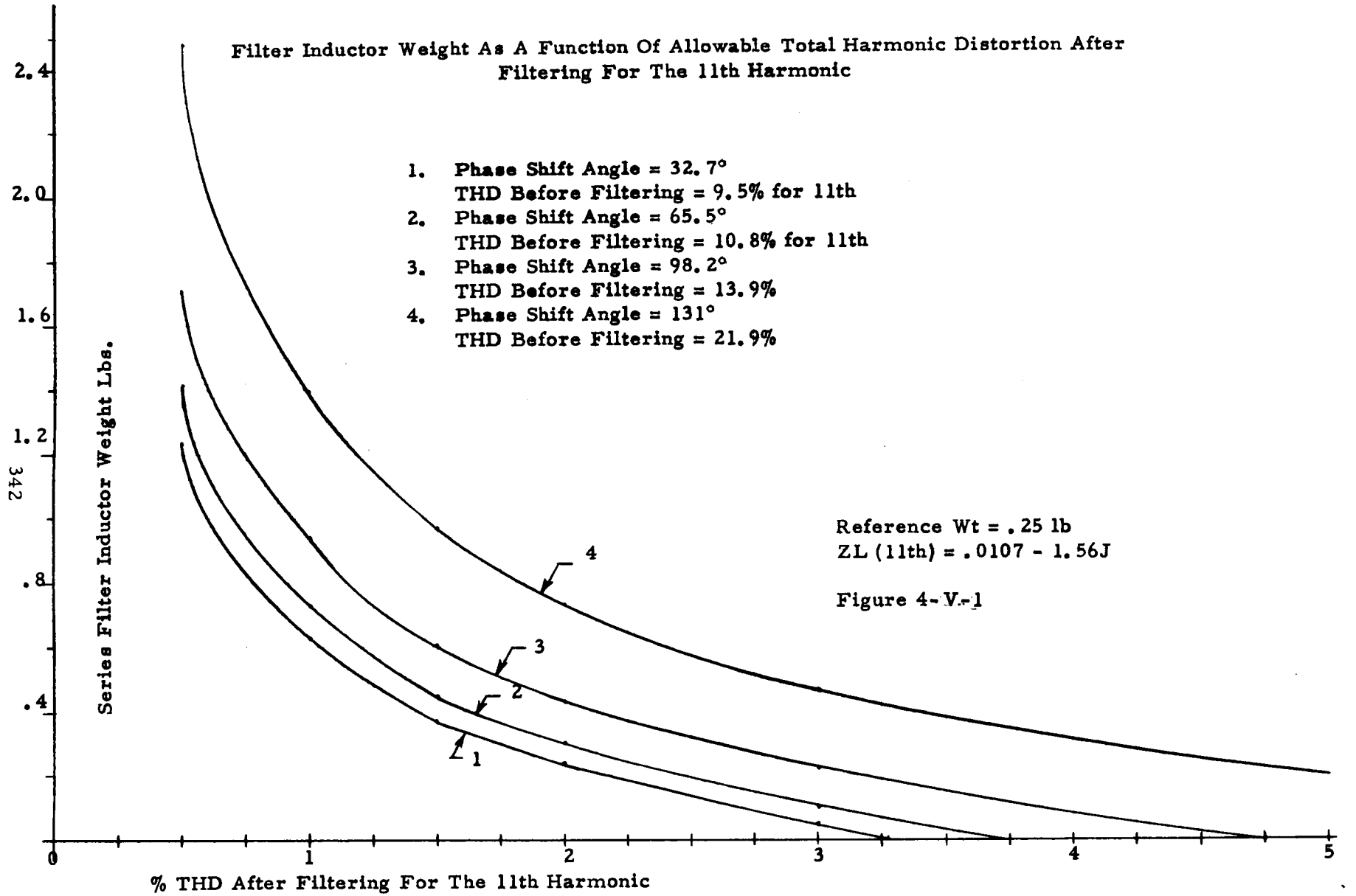
Figure 4 - III - 11

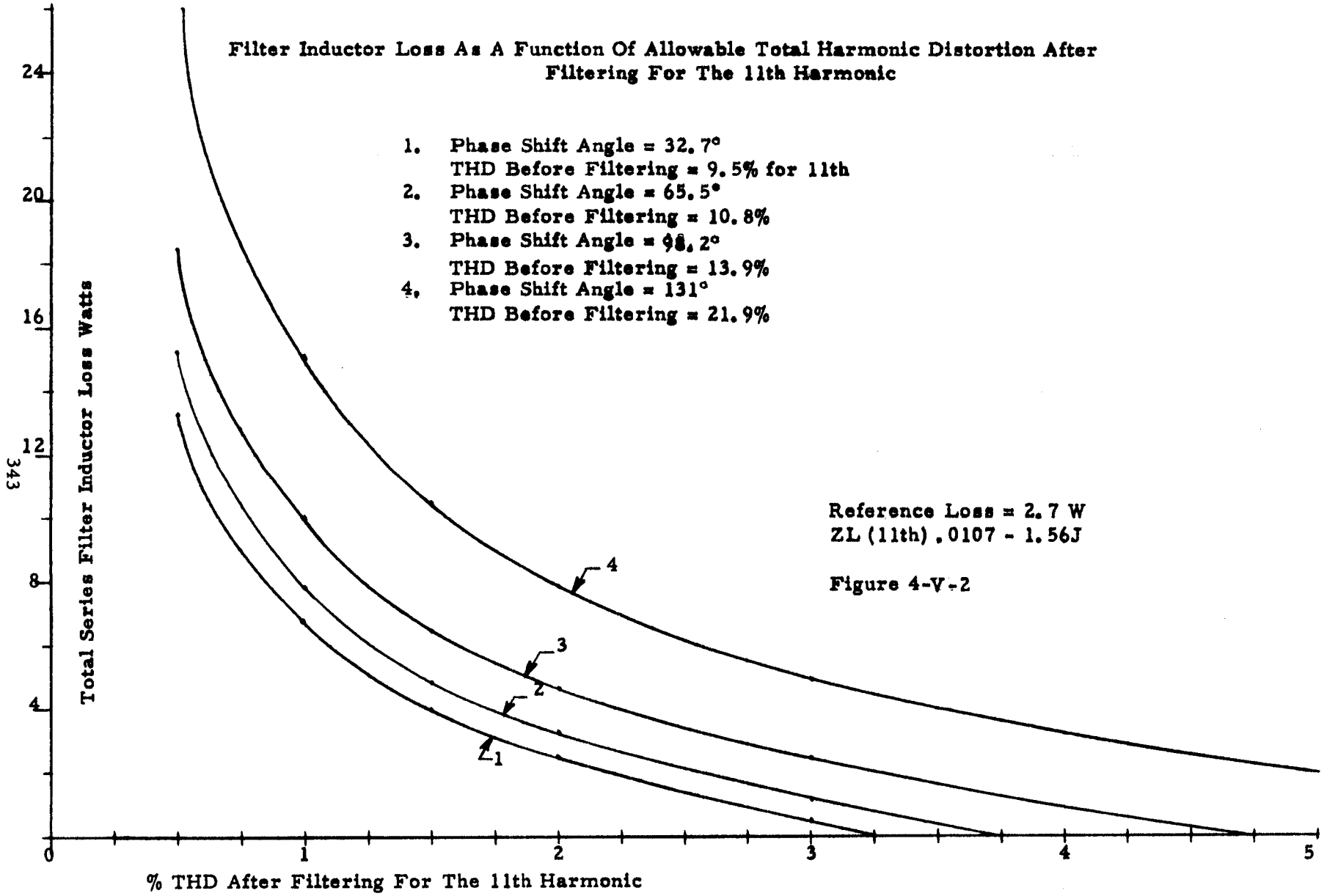


Inverter Total Weight & Loss vs. Nominal Input Voltage

Figure 4 - III - 12

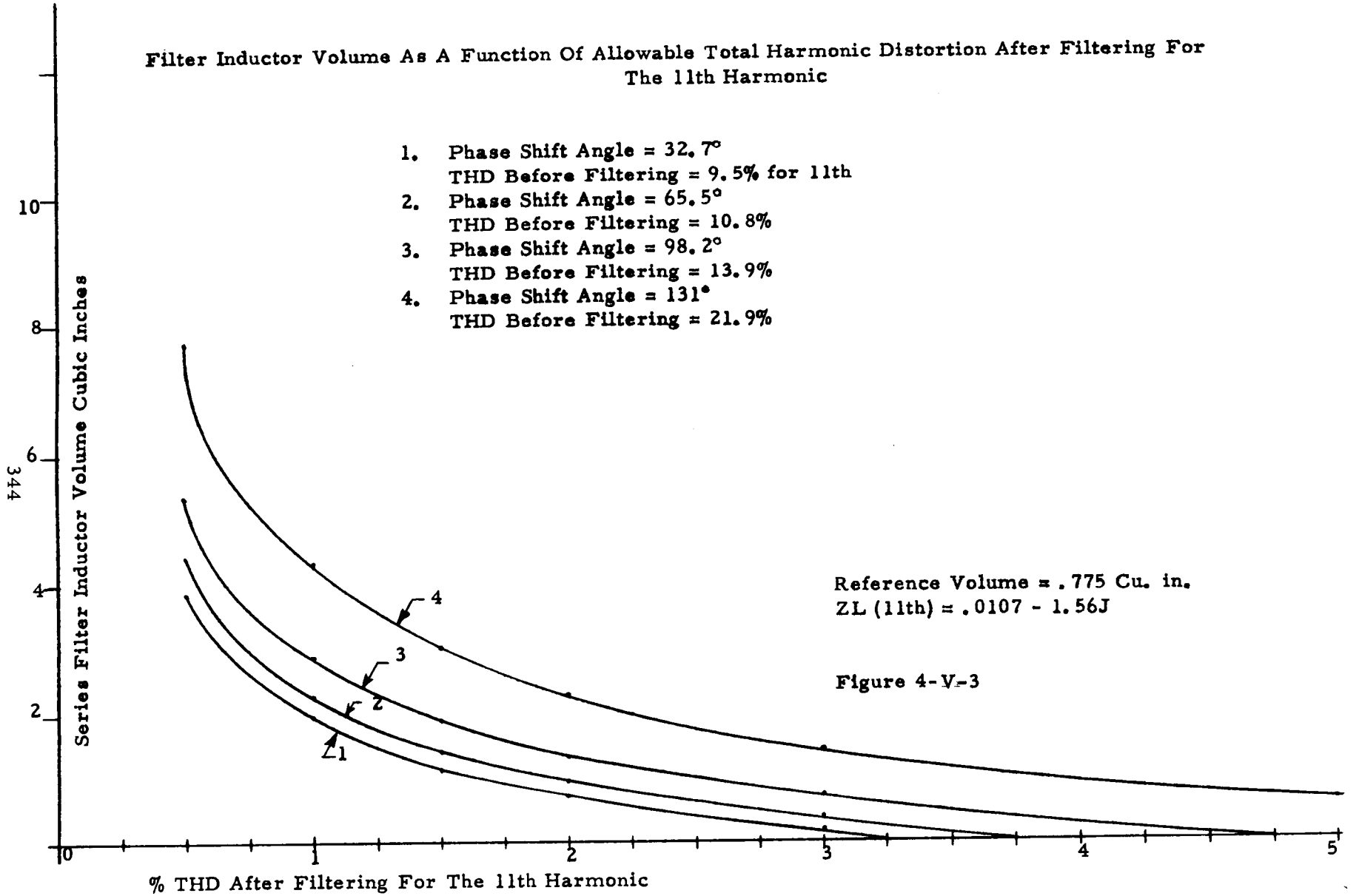



Filter Inductor Weight As A Function Of Allowable Total Harmonic Distortion After Filtering For The 11th Harmonic
1. Phase Shift Angle = 32.7°
THD Before Filtering = 9.5% for 11th
2. Phase Shift Angle = 65.5°
THD Before Filtering = 10.8% for 11th
3. Phase Shift Angle = 98.2°
THD Before Filtering = 13.9%
4. Phase Shift Angle = 131°
THD Before Filtering = 21.9%
Reference Wt = .25 lb
ZL (11th) = .0107 - 1.56J
Figure 4-V-1
Series Filter Inductor Weight Lbs.
2.4
2.0
1.6
1.2
.8
.4
0
1
2
3
4
5
% THD After Filtering For The 11th Harmonic
1
2
3
4


Filter Inductor Loss As A Function Of Allowable Total Harmonic Distortion After Filtering For The 11th Harmonic
1. Phase Shift Angle = 32.7°
THD Before Filtering = 9.5% for 11th
2. Phase Shift Angle = 65.5°
THD Before Filtering = 10.8%
3. Phase Shift Angle = 98.2°
THD Before Filtering = 13.9%
4. Phase Shift Angle = 131°
THD Before Filtering = 21.9%
Reference Loss = 2.7 W
ZL (11th) .0107 - 1.56J
Figure 4-V-2
Total Series Filter Inductor Loss Watts
24
20
16
12
8
4
0
1
2
3
4
5
% THD After Filtering For The 11th Harmonic
4
3
2
1

Filter Inductor Volume As A Function Of Allowable Total Harmonic Distortion After Filtering For The 11th Harmonic

1. Phase Shift Angle = 32.7°
   THD Before Filtering = 9.5% for 11th
2. Phase Shift Angle = 65.5°
   THD Before Filtering = 10.8%
3. Phase Shift Angle = 98.2°
   THD Before Filtering = 13.9%
4. Phase Shift Angle = 131°
   THD Before Filtering = 21.9%



Reference Volume = .775 Cu. in.
ZL (11th) = .0107 - 1.56J

Figure 4-V-3

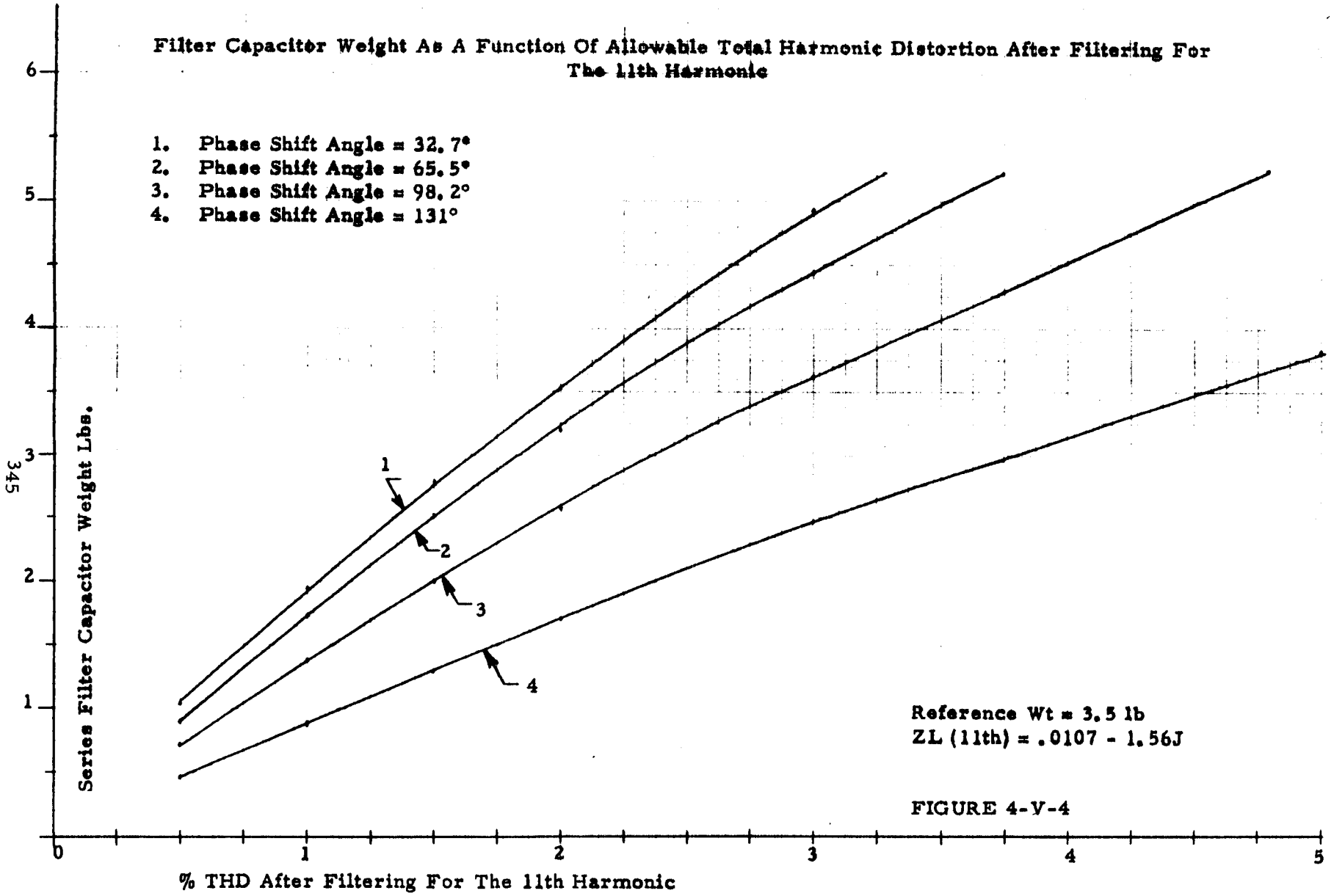

Filter Capacitor Weight As A Function Of Allowable Total Harmonic Distortion After Filtering For The 11th Harmonic
1. Phase Shift Angle = 32.7°
2. Phase Shift Angle = 65.5°
3. Phase Shift Angle = 98.2°
4. Phase Shift Angle = 131°
Series Filter Capacitor Weight Lbs.
% THD After Filtering For The 11th Harmonic
0
1
2
3
4
5
6
1
2
3
4
Reference Wt = 3.5 lb
ZL (11th) = .0107 - 1.56J

FIGURE 4-V-4

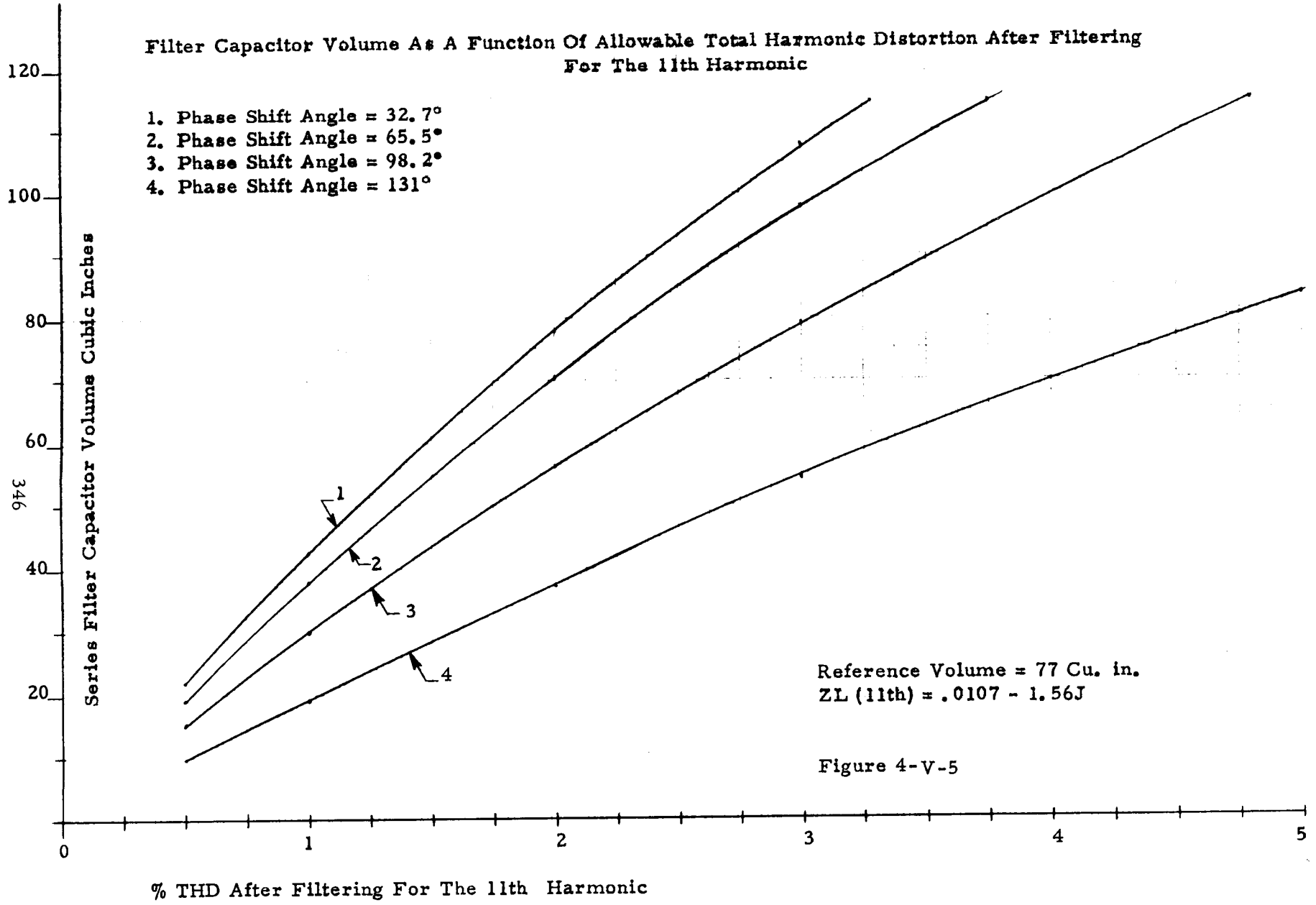
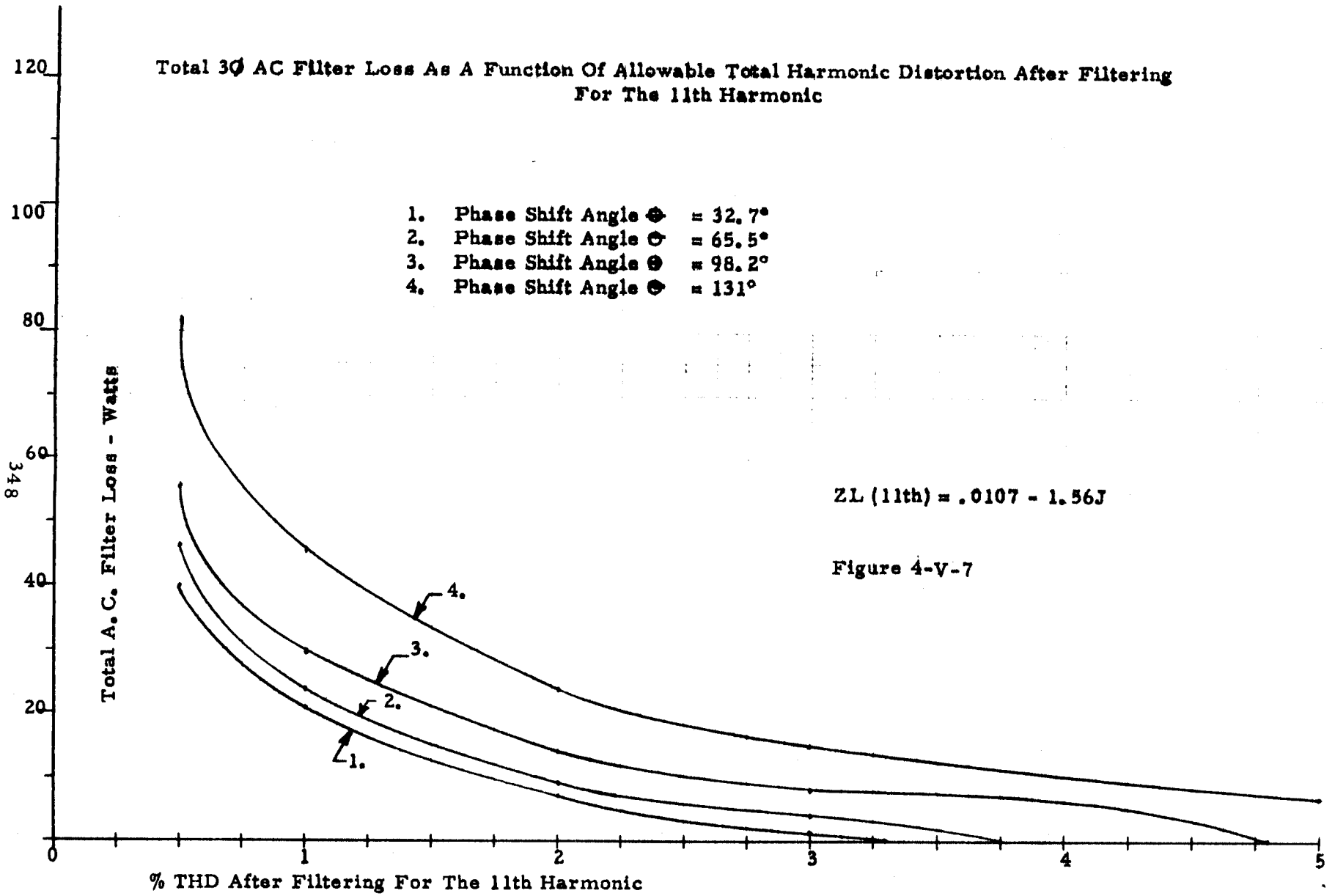

Filter Capacitor Volume As A Function Of Allowable Total Harmonic Distortion After Filtering For The 11th Harmonic
1. Phase Shift Angle = 32.7°
2. Phase Shift Angle = 65.5°
3. Phase Shift Angle = 98.2°
4. Phase Shift Angle = 131°
Series Filter Capacitor Volume Cubic Inches
120
100
80
60
40
20
0
1
2
3
4
5
% THD After Filtering For The 11th Harmonic
Reference Volume = 77 Cu. in.
ZL (11th) = .0107 - 1.56J

Figure 4-V-5

Total 3Ø AC Filter Loss As A Function Of Allowable Total Harmonic Distortion After Filtering For The 11th Harmonic

1. Phase Shift Angle Θ = 32.7°
2. Phase Shift Angle Θ = 65.5°
3. Phase Shift Angle Θ = 98.2°
4. Phase Shift Angle Θ = 131°



ZL (11th) = .0107 - 1.56J

Figure 4-V-7

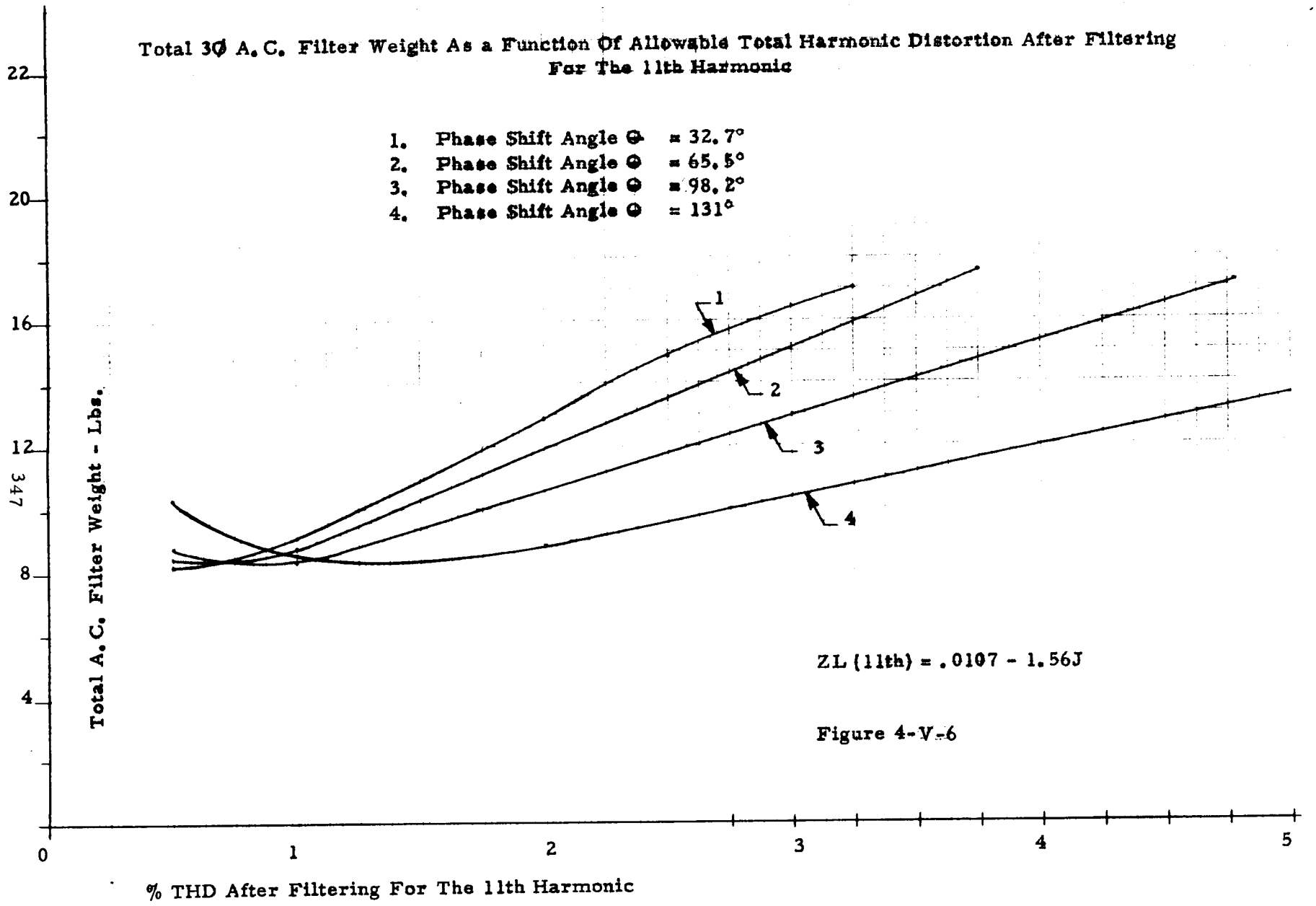
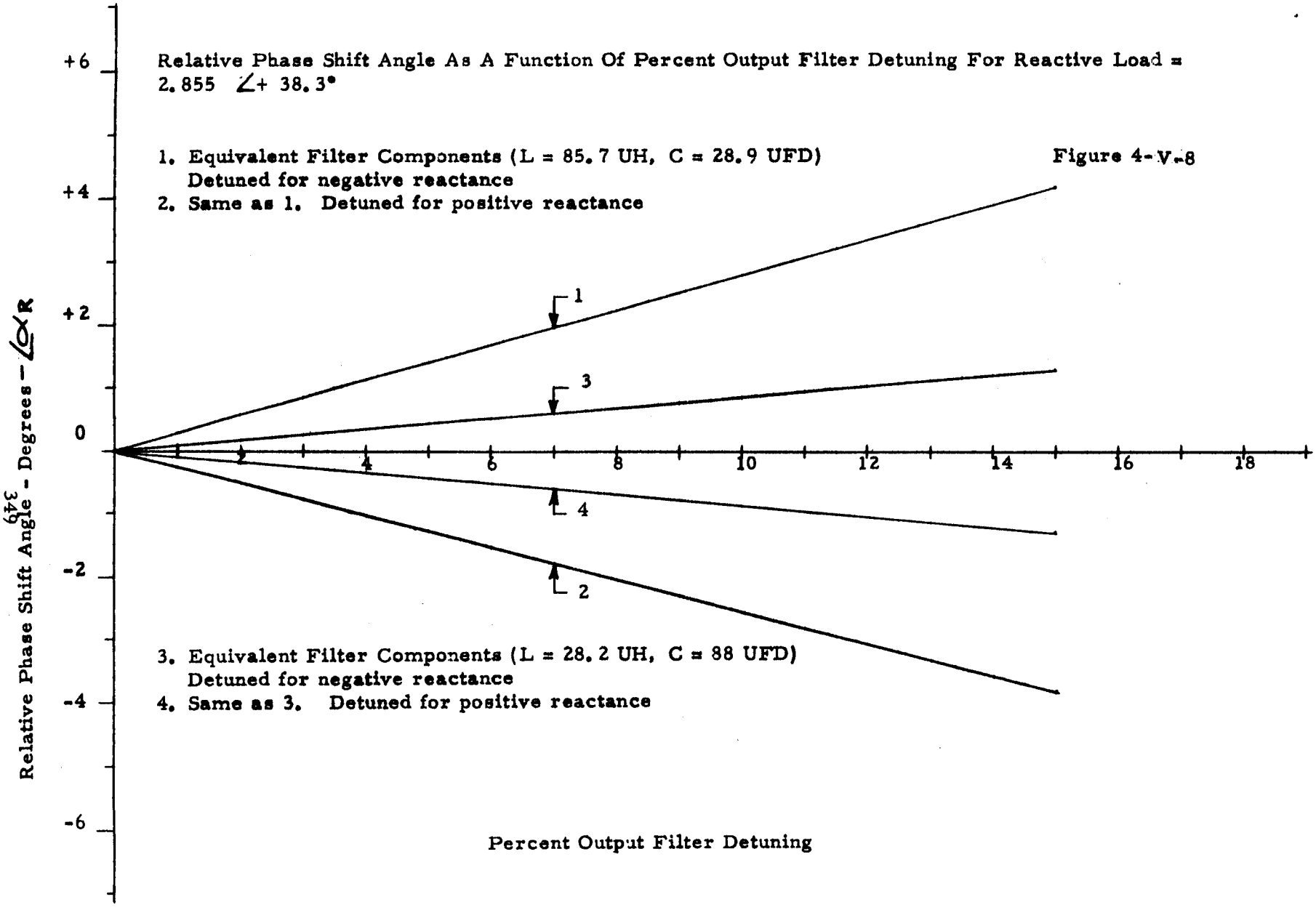

Total 3Ø A. C. Filter Weight As a Function Of Allowable Total Harmonic Distortion After Filtering For The 11th Harmonic
1. Phase Shift Angle Θ = 32.7°
2. Phase Shift Angle Θ = 65.5°
3. Phase Shift Angle Θ = 98.2°
4. Phase Shift Angle Θ = 131°
Total A. C. Filter Weight - Lbs.
22
20
16
12
8
4
0
1
2
3
4
5
% THD After Filtering For The 11th Harmonic
ZL (11th) = .0107 - 1.56J

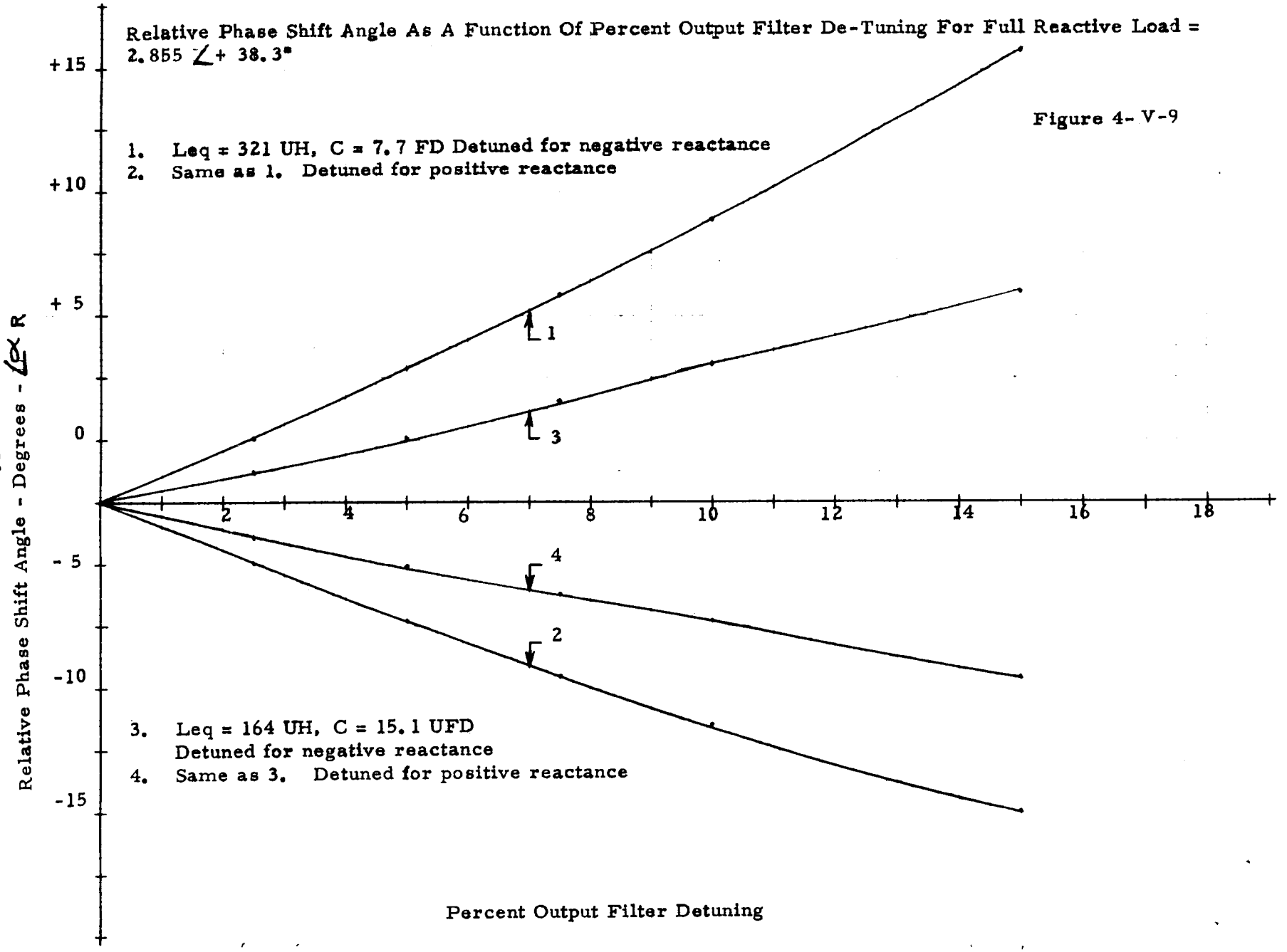
Figure 4-V-6

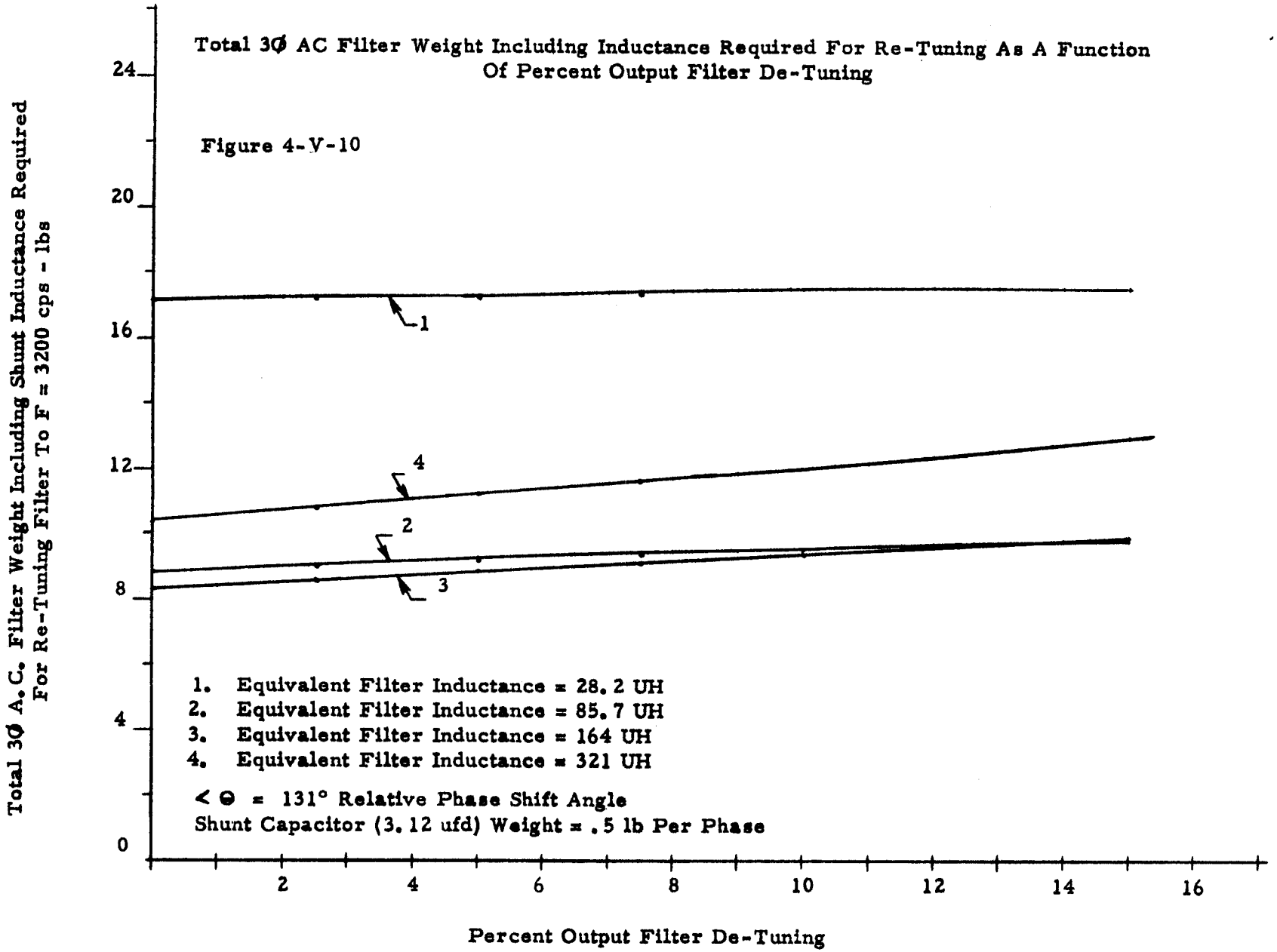

Relative Phase Shift Angle As A Function Of Percent Output Filter Detuning For Reactive Load = 2.855 ∠+ 38.3°
1. Equivalent Filter Components (L = 85.7 UH, C = 28.9 UFD) Detuned for negative reactance
2. Same as 1. Detuned for positive reactance
Figure 4-V-8
3. Equivalent Filter Components (L = 28.2 UH, C = 88 UFD) Detuned for negative reactance
4. Same as 3. Detuned for positive reactance
Relative Phase Shift Angle - Degrees - ∠θR
+6
+4
+2
0
-2
-4
-6
2
4
6
8
10
12
14
16
18
1
2
3
4
Percent Output Filter Detuning

Relative Phase Shift Angle As A Function Of Percent Output Filter De-Tuning For Full Reactive Load = 2.855 ∠+ 38.3°

Figure 4- V-9

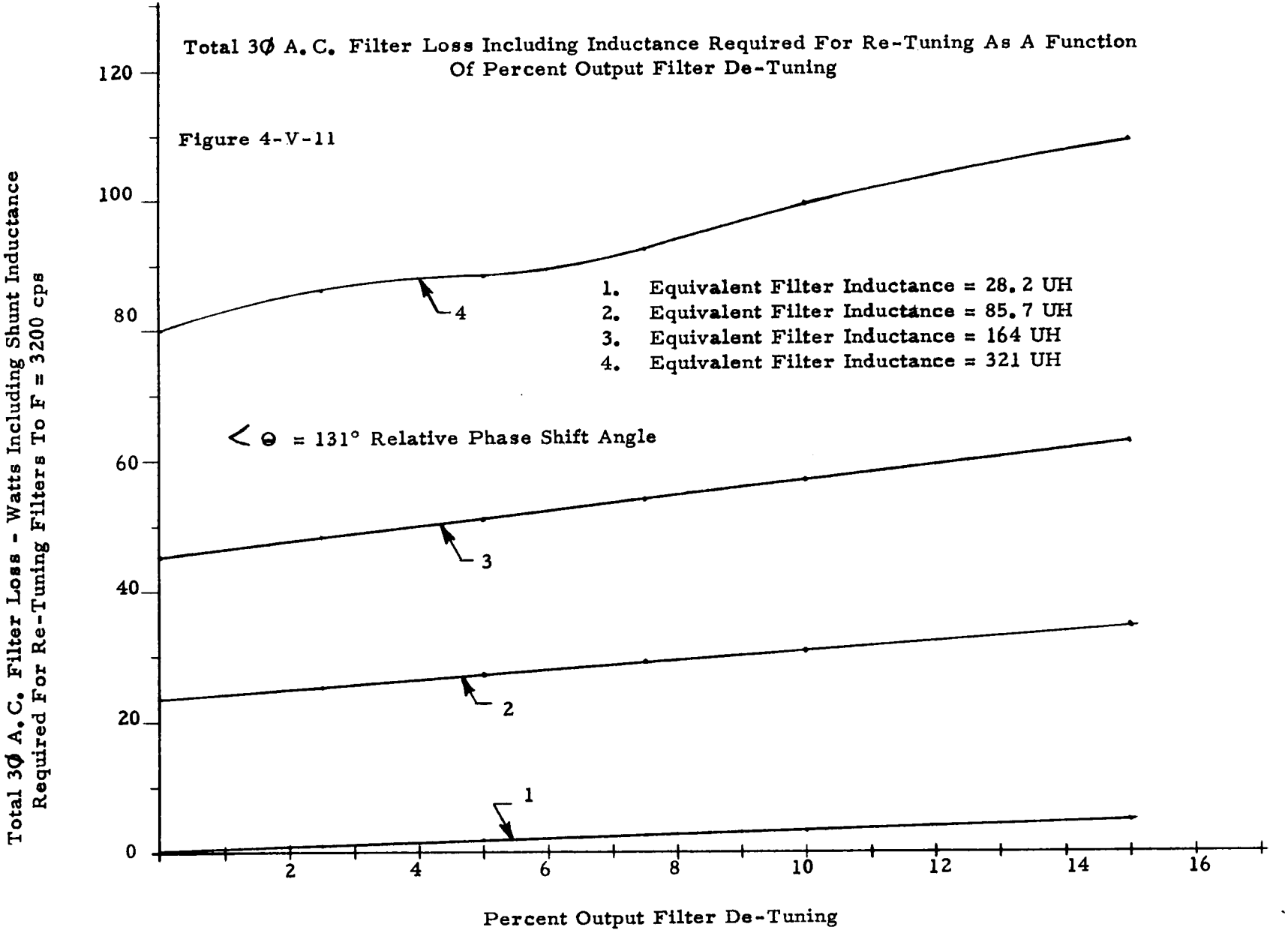
1. Leq = 321 UH, C = 7.7 FD Detuned for negative reactance
2. Same as 1. Detuned for positive reactance
3. Leq = 164 UH, C = 15.1 UFD
   Detuned for negative reactance
4. Same as 3. Detuned for positive reactance

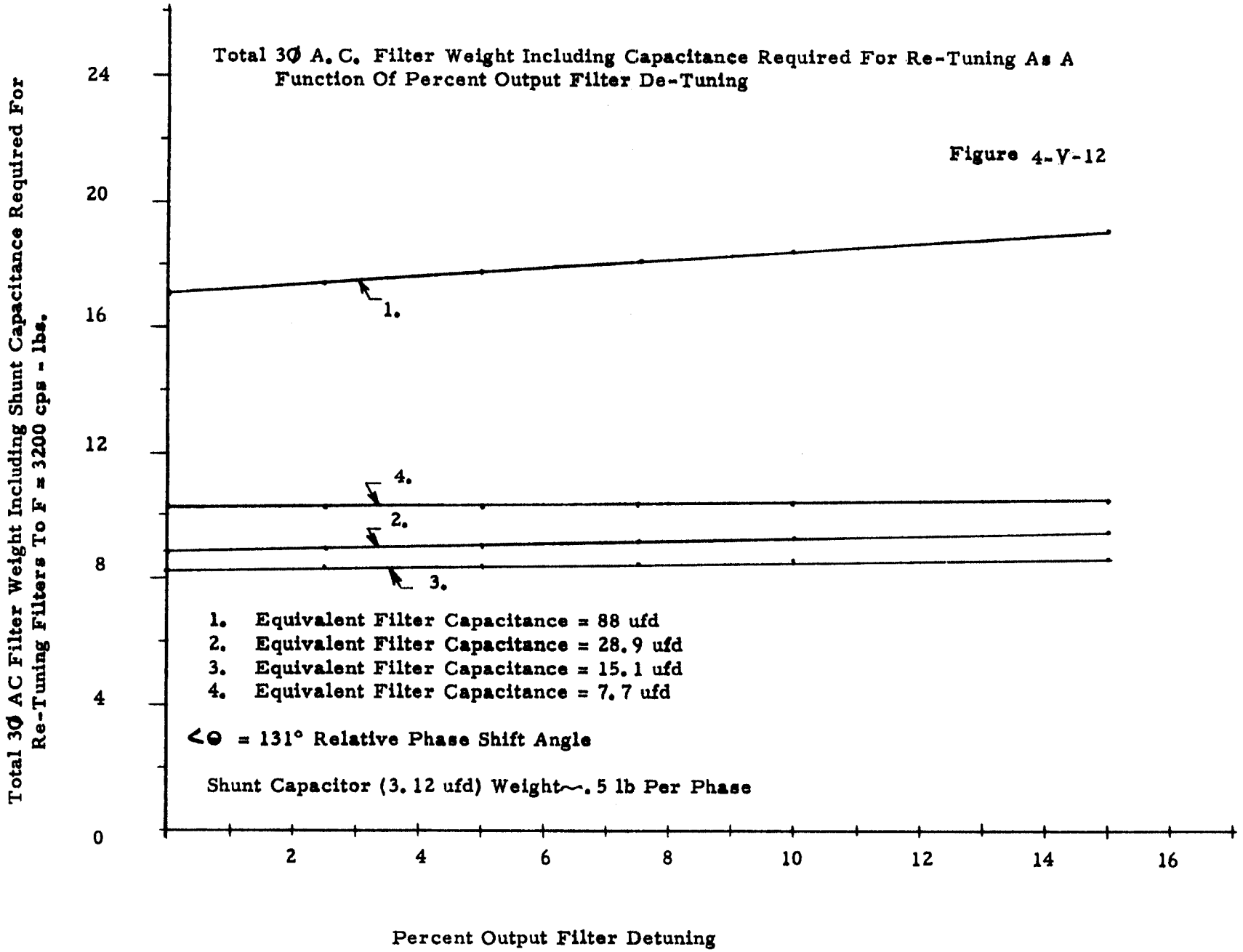



Total 3Ø AC Filter Weight Including Inductance Required For Re-Tuning As A Function Of Percent Output Filter De-Tuning
Figure 4-V-10
Total 3Ø A.C. Filter Weight Including Shunt Inductance Required For Re-Tuning Filter To F = 3200 cps - lbs
24
20
16
12
8
4
0
1
4
2
3
1. Equivalent Filter Inductance = 28.2 UH
2. Equivalent Filter Inductance = 85.7 UH
3. Equivalent Filter Inductance = 164 UH
4. Equivalent Filter Inductance = 321 UH
< Θ = 131° Relative Phase Shift Angle
Shunt Capacitor (3.12 ufd) Weight = .5 lb Per Phase
2
4
6
8
10
12
14
16
Percent Output Filter De-Tuning

Total 3Ø A.C. Filter Loss Including Inductance Required For Re-Tuning As A Function Of Percent Output Filter De-Tuning

Figure 4-V-11




Total 3Ø A. C. Filter Weight Including Capacitance Required For Re-Tuning As A Function Of Percent Output Filter De-Tuning
Figure 4-V-12
Total 3Ø AC Filter Weight Including Shunt Capacitance Required For Re-Tuning Filters To F = 3200 cps - lbs.
24
20
16
12
8
4
0
2
4
6
8
10
12
14
16
1.
2.
3.
4.
1. Equivalent Filter Capacitance = 88 ufd
2. Equivalent Filter Capacitance = 28.9 ufd
3. Equivalent Filter Capacitance = 15.1 ufd
4. Equivalent Filter Capacitance = 7.7 ufd
<Θ = 131° Relative Phase Shift Angle
Shunt Capacitor (3.12 ufd) Weight ~.5 lb Per Phase
Percent Output Filter Detuning

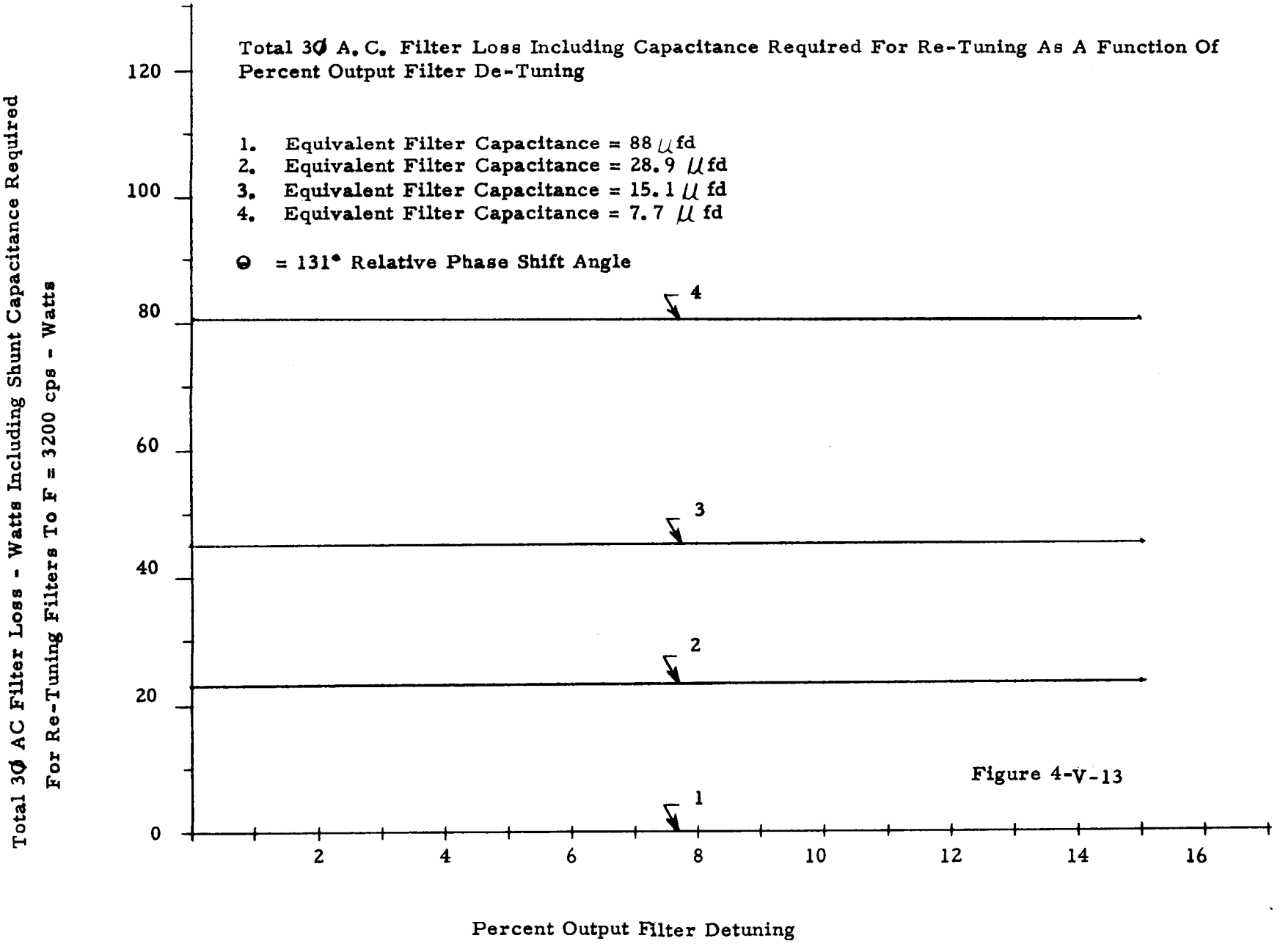

Total 3Ø A. C. Filter Loss Including Capacitance Required For Re-Tuning As A Function Of Percent Output Filter De-Tuning
1. Equivalent Filter Capacitance = 88 μfd
2. Equivalent Filter Capacitance = 28.9 μfd
3. Equivalent Filter Capacitance = 15.1 μ fd
4. Equivalent Filter Capacitance = 7.7 μ fd
Θ = 131° Relative Phase Shift Angle
Total 3Ø AC Filter Loss - Watts Including Shunt Capacitance Required For Re-Tuning Filters To F = 3200 cps - Watts
120
100
80
60
40
20
0
2
4
6
8
10
12
14
16
Percent Output Filter Detuning

Figure 4-V-13

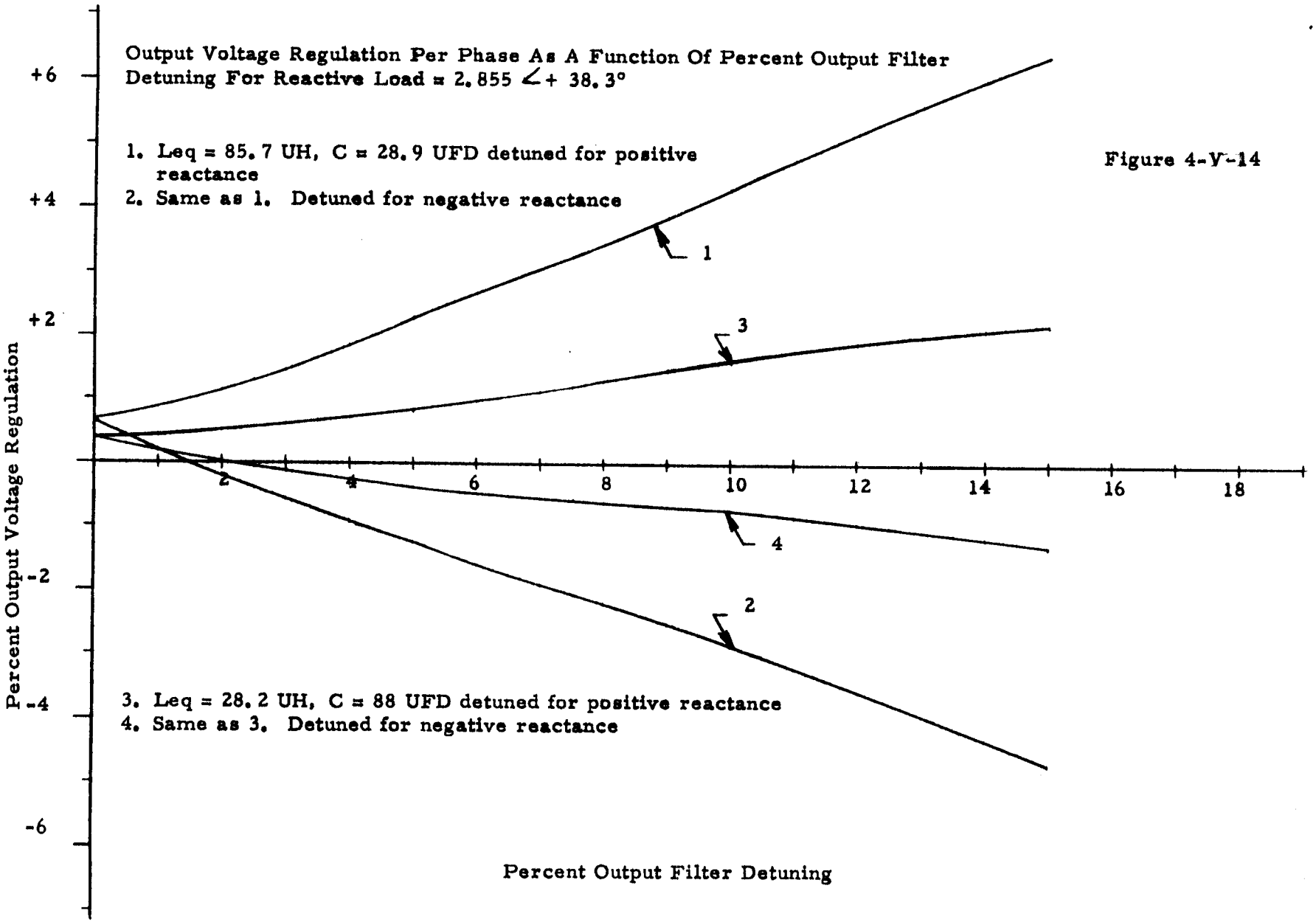

Output Voltage Regulation Per Phase As A Function Of Percent Output Filter Detuning For Reactive Load = 2.855 ∠+ 38.3°
1. Leq = 85.7 UH, C = 28.9 UFD detuned for positive reactance
2. Same as 1. Detuned for negative reactance
3. Leq = 28.2 UH, C = 88 UFD detuned for positive reactance
4. Same as 3. Detuned for negative reactance
+6
+4
+2
-2
-4
-6
2
4
6
8
10
12
14
16
18
1
2
3
4
Percent Output Voltage Regulation
Percent Output Filter Detuning

Figure 4-Y-14

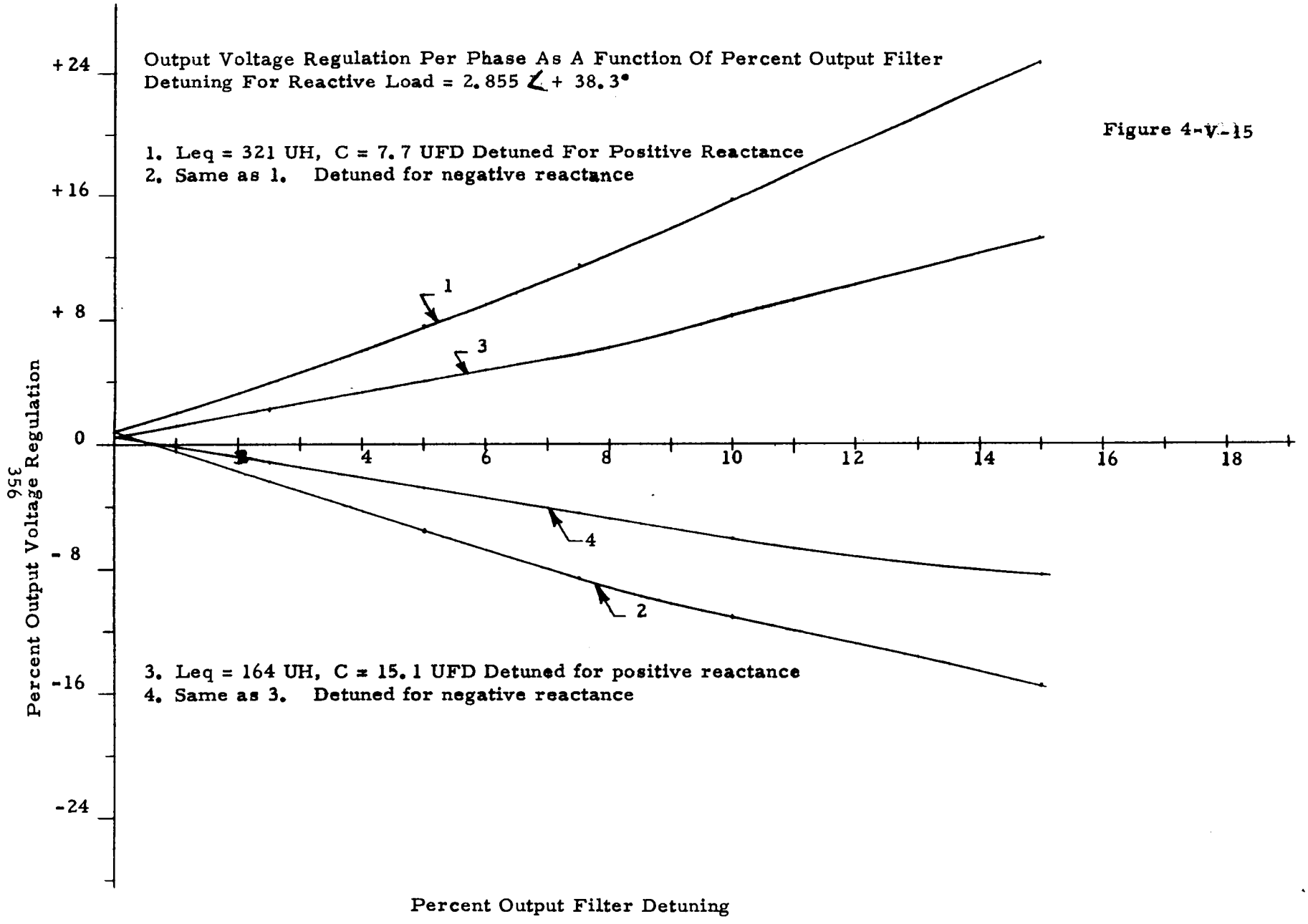
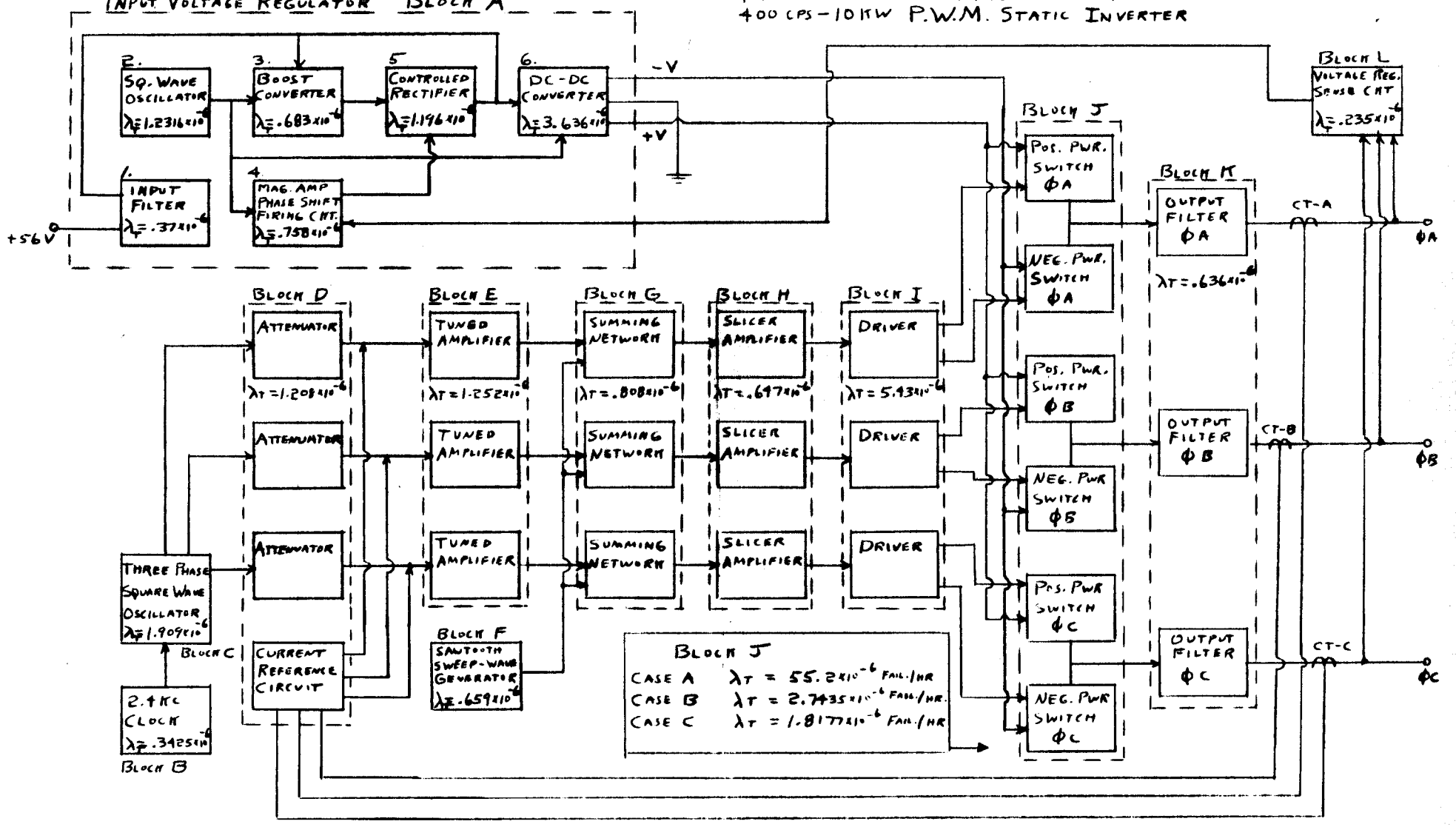

Output Voltage Regulation Per Phase As A Function Of Percent Output Filter Detuning For Reactive Load = 2.855 ∠ + 38.3°
1. Leq = 321 UH, C = 7.7 UFD Detuned For Positive Reactance
2. Same as 1. Detuned for negative reactance
3. Leq = 164 UH, C = 15.1 UFD Detuned for positive reactance
4. Same as 3. Detuned for negative reactance
+24
+16
+ 8
0
- 8
-16
-24
2
4
6
8
10
12
14
16
18
1
3
4
2
Percent Output Voltage Regulation
Percent Output Filter Detuning

Figure 4-V-15

RELIABILITY BLOCK DIAGRAM FOR THE 400 CPS – 10 KW P.W.M. STATIC INVERTER



NOTE 2. CASE A – CATASTROPHIC FAILURE OF TWO POWER TRANS. IN SAME CKT. SEGMENT
CASE B – FAILURE IN SHORTED MODE – 15 TRANS. MAX. PER HALF PHASE
CASE C – FAILURE IN OPEN MODE – 9 CKT. SEGMENTS MAXIMUM PER HALF PHASE

NOTE 1. CT-A, CT-B, CT-C ARE INCLUDED AS PART OF BLOCK D

FIGURE 4-VI-1

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