NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Technical Report No. 32-794

Photon-Actuated Multiplex Switch Development

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ABSTRACT

A photon-actuated electronic switch has been developed for multiplexing low-level analog signals. The development was done by the Components Division of the International Business Machines Corporation under contract to the Jet Propulsion Laboratory. The device represents a significant advance in this type of solid-state switching in terms of miniaturization, speed, simplicity, and potential reliability.

The switch consists of a gallium arsenide diode, as an infrared light source, and a double-emitter silicon transistor that detects the infrared photons and acts as the switch. Efficient coupling between the diode and the transistor has been achieved. Device development, theoretical considerations, problem areas, and test results are covered.

The Report is a condensation of the final IBM report, supplemented by test results and more user-oriented.

I. INTRODUCTION

The multiplexing of low-level analog signals is an important function of many spacecraft telemetry or data-handling systems. This function was originally performed by electromechanical commutators, but these devices were susceptible to high vibration levels and mechanical wear and required periodic maintenance. The advent of transistors and solid-state switching brought considerable improvement in size, weight, speed, and switching power, as well as the elimination of vibration and maintenance problems.

The standard solid-state method of multiplexing or switching low-level analog signals with minimum error is shown in Fig. 1. This circuit was published in 1955 and was subsequently patented by R. L. Bright of Westinghouse Electric Corporation. The offset voltage between the input and output terminals is the difference between the junction potentials of the two transistors and is minimized by operating the transistors in an inverted configuration. The *on* resistance is the sum of the *on* resistances of the two transistors. The switch can handle bipolar signals.

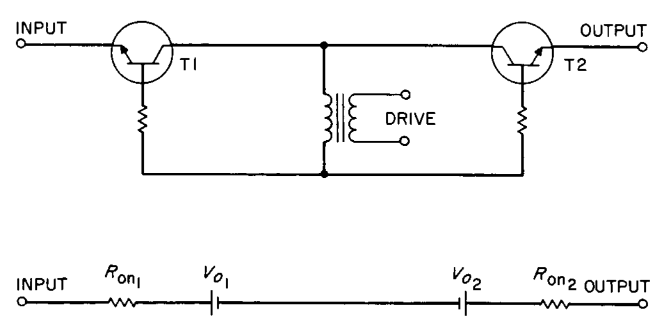

Fig. 1. Matched pair "chopper–multiplex switch" circuit

Direct-current analysis of a solid-state multiplexer is given in the Appendix. It is shown that precision low-level voltage switching requires devices with the following characteristics:

1. Very high open impedance.
2. Very low closed impedance.
3. Low offset voltage.

4. Very high impedance between driving source and signal path.

Other requirements may include high switching speed and the capability of handling signals of either polarity, as well as low size, weight, and power.

A transformer-coupled, solid-state multiplex switch of conventional design (Fig. 2) satisfies these requirements reasonably well and has seen widespread use in recent years. However, the conventional solid-state switch will not be compatible in weight, size, or form factor with microelectronic data-handling systems of the future. The noncompatibility will be particularly noticeable because many multiplex switches are required in a typical telemetry system, the number generally exceeding 100. A microelectronic multiplex switch is therefore desirable as a counterpart to semiconductor integrated and/or thin-film circuits in the next generation of spacecraft telemetry systems.

The phenomenon of infrared emission from the junction of a forward-biased gallium arsenide diode suggested one method of achieving a truly microelectronic and 100% solid-state switch. The GaAs emission spectrum peaks in the wavelength region (9000Å) where silicon junction photon sensitivity is maximum. Therefore, the infrared emission could be used to turn on a phototransistor switch. Such a device would be very small and extremely simple, and very possibly it would offer greater reliability than that presently obtainable in multiplex switches. But could practical coupling efficiencies be achieved?

The Components Division of the International Business Machines Corporation (IBM) was awarded a contract[1] by the Jet Propulsion Laboratory (JPL) to determine whether practical photon-actuated multiplex switches could be made. The principal design and performance criteria for the switch are given in Table 1. The lumped parameters are identified in an equivalent circuit of the switch shown in Fig. 3. Conventional solid-state multiplex switch modules in use at JPL at that time had a volume of 0.6 cubic inch. A goal of 100 times reduction in volume was established for this project.

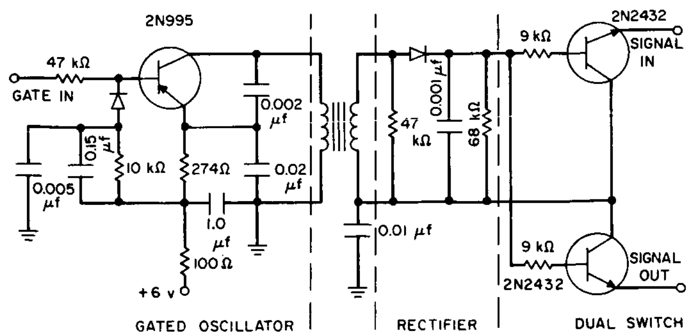

Fig. 2. Transformer-coupled multiplex switch

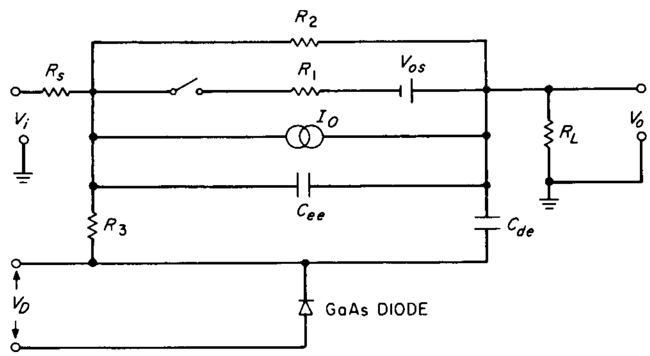

Fig. 3. Photon-actuated switch equivalent circuit

Table 1. Objectives of switch design

Parameter		Value[a]
R_1 or R_{on}	Switch-closed dc resistance	$\leq 20\ \Omega$
R_2	Switch-open dc resistance	$\geq 100\ M\Omega$
R_3	Switch isolation resistance	$\geq 100\ M\Omega$
V_{os}	Switch-closed contact potential	$\leq \pm 50\ \mu v$
I_{EEO} or I_O	Switch-open leakage current	≤ 50 nanoamp
R_S	Source impedance	20 Ω to 10 k Ω
R_L	Load impedance	10 k Ω to 1 M Ω
V_i	Input signal	± 5 v
BV_{ce}	Voltage overload without switch damage, open or closed	$\geq \pm 35$ v
I_m	Current overload without switch damage, open or closed	$\geq \pm 10$ ma
$(t_r + t_f)$	Switch rise and fall time	$< 20\ \mu$sec
P	Total power to close switch	50 mw
Error Band	$\left(\frac{V_i - V_{out}}{V_{FSR}}\right) 100$	$\leq \pm 1\%$
V_{FSR}	Full-scale range voltage	± 5 mv to ± 5 v

[a]For a temperature range of −10 to +85°C.

[1]The final report by IBM on this task, *Integrated Electronic Gating System for Multiplexing Applications,* is available from the National Aeronautics and Space Administration, Scientific and Technical Information Facility, P.O. Box 5700, Bethesda, Maryland, 20014. The NASA document number is N65-19926.

II. PHOTON-ACTUATED SWITCH DEVELOPMENT

The photon-actuated switch consists of four parts: a gallium arsenide diode, a double-emitter transistor, a coupling medium between the diode and transistor, and an enclosing package. The diode and transistor development was conducted by different research physicists working in close proximity and with good coordination. To give an indication of the scope of the effort, 41 GaAs wafers and 189 silicon wafers were processed. Most of these were done one at a time in the trial-and-error fashion.

A. GaAs Diode Development

The mechanism of infrared radiation from a forward-biased GaAs junction diode is not fully understood at this time. It is generally agreed, however, that the radiation is caused by the recombination of injected electrons and holes in the P side of the diode near the junction. The recombination releases energy in the form of phonons (heat) and photons (light). The P side of the diode is not necessarily the one that radiates the most light, however, since the absorption coefficient of P-type GaAs is much higher than that of N-type GaAs at the desired doping levels. It was shown that the light output from the N side of a diode was twice that of the P side, even though the N side is three times thicker than the P side.

The GaAs diode design was based on the results of many experiments correlating efficiency with diode structure, size, starting materials, types of dopant, and doping levels. Diffused planar and mesa diodes were made in sizes varying from 5 by 5 to 40 by 40 mils. With equal junction depths, the planar diode had about the same light output from either surface as the mesa diode did from its N side. The planar diode is harder to make, however, owing to the fact that SiO is not a good mask for zinc, the preferred diffusant, at high temperatures.

The light output is inversely proportional to diode size for a given current level and is therefore directly proportional to current density. For this reason, 5- by 5-mil mesa diodes were used in the switches. The diode configuration is shown in Fig. 4.

A theoretical analysis of the relative efficiencies of a dome-shaped diode and a diode with a flat surface was performed. The dome shape focuses the light, a condition that should result in higher efficiency at the silicon detector. The analysis revealed that a flat diode with a glass or epoxy coupling medium is better than the dome-shaped diode with air coupling.

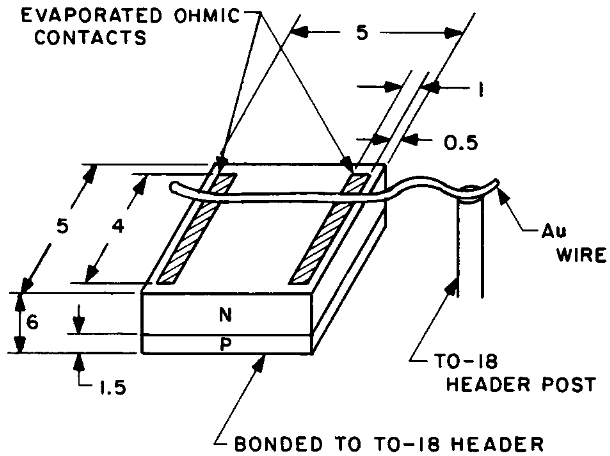

Fig. 4. Diode assembly

Gallium arsenide has an index of refraction of 3.6. The critical angle of reflection at the GaAs–air interface is about 16 deg. The internal reflection losses can be reduced by introducing a light-coupling medium with an index of refraction greater than that of air. The light output was increased by a factor of 2 when an epoxy medium with a refraction index of 1.5 was used. Other coupling materials, including selenium, were considered. Selenium has an index refraction of 2.9 in the amorphous state. The factor-of-2 improvement over epoxy was experimentally demonstrated, but amorphous selenium proved to be unstable and hence was unsuitable for the switch. In the cases where selenium was used on the diode, the light output fell off drastically during prolonged testing. A high-temperature epoxy, which gave a 1.8 improvement over uncoated diodes, was finally chosen. External efficiencies of about 1.4% were achieved for the diode with this epoxy coating.

B. Double-Emitter Transistor Development

The double-emitter transistor (DET) is a logical extension of the Bright configuration in integrated semiconductor technology. It affords the advantages of better matching of individual offset voltages, negligible thermal differences, fewer connections, and more compactness. When photon actuation is considered, the DET offers the optimum configuration for detection.

The operation of the DET under photon drive is explained as follows. Assume the signal polarity shown in Fig. 5. For the opposite polarity, the junction roles are

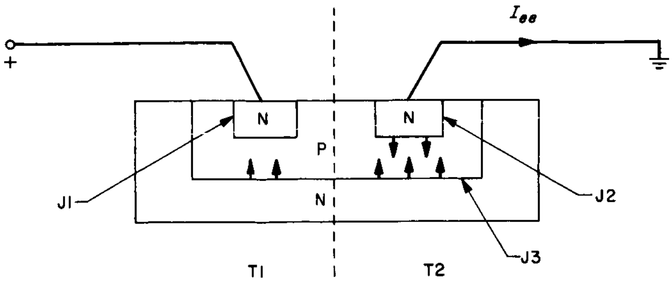

Fig. 5. Mode of operation of double-emitter transistor

reversed. When no light is falling on the DET, junction 1 (J1) is reverse-biased, while J2 and J3 are nearly neutral (slightly forward-biased by the leakage current through J1). The current that flows through the DET is limited to the leakage current in J1.

When the DET is flooded with photons, electron–hole pairs are generated throughout the structure. Diffusion and drift mechanisms cause an accumulation of majority carriers (holes) in the base region, making it positive, and causing J2 to inject. When these injected carriers reach J3, it saturates, becomes forward-biased, and injects throughout. The carriers (electrons) injected by J3 that are within a diffusion length of J1 are collected by J1 and constitute the current flowing in the switch. It can be seen that, for efficient operation, all junctions should be good emitters.

The photon-actuated switch, shown in Fig. 6, is turned on by an effective base current generated through the absorption of photons in the bulk of the silicon detector. This arrangement dictates a certain geometry for the DET. To ensure that J1 and J2 are good emitters, they should be as large as possible. They should also be of equal area for electrical symmetry. Therefore the optimum size for each would be one-half the area of J3. A circular geometry with closely spaced, D-shaped emitters was chosen for the DET.

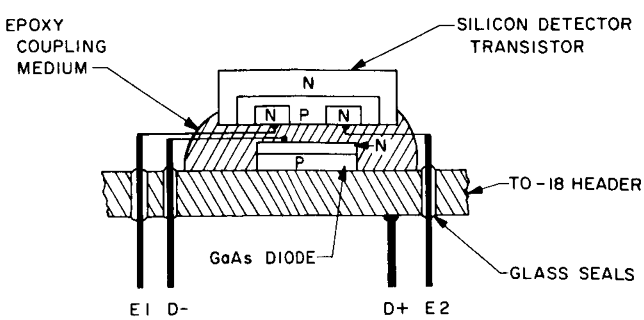

Fig. 6. Structure of photon-actuated switch

Switch parameters having the greatest effect on the DET are the breakdown voltage from emitter to emitter (BV_{EE}), the *on* resistance from emitter to emitter R_{on}, and the voltage from emitter to emitter when no current is flowing (V_{os}). These parameters[2] are defined as follows:

1.

$$BV_{EE} \cong BV_{eb}\left(\frac{1}{\beta_r}\right)^{1/n} \tag{1}$$

where

β_r = the reverse common-emitter current transfer ratio

n = a surface-dependent factor

BV_{eb} = the avalanche breakdown voltage of the emitter junction—an inverse function of the base doping level.

2.

$$R_{on} \cong \frac{2n\,S}{I_b}\left(\frac{1}{\beta_r}\right) + R_i \tag{2}$$

where

I_b = the effective base current, a function of the area exposed to photons

R_i = the intrinsic resistance, typically $< 5\,\Omega$

$S = (kT)/q$, a constant for a given temperature.

Increasing the area of the device in order to decrease R_{on} is not desirable, since speed is an inverse function of area. Therefore, increasing β_i is the prime factor in lowering R_{on}. A trade-off is necessary, however, since increasing β_i would decrease BV_{EE}. This was the main compromise that had to be made in the DET development.

3.

$$V_{os} = n\,S\,ln\left[\frac{\beta_{f_2}(\beta_{f_1}+1)}{\beta_{f_1}(\beta_{f_2}+1)}\right] \tag{3}$$

assuming I_{b_1} (effective) = I_{b_2} (effective). The parameter β_f is the forward common-emitter current transfer ratio.

[2]Subscripts indicating an emitter or diode are in capital letters for direct current ($E,D,$) and lower case for pulsed current (e,d).

From Eq. (3), $V_{os} - 0$, if $\beta_{f_1} = \beta_{f_2}$. Small differences in β_f will not greatly increase V_0 unless β_f is small. Experimental results gave higher values of V_{os} than were indicated by Eq. (3). This indicates nonequal effective base currents, resulting most likely from unequal illumination.

During the DET development, five types of devices were investigated. They are shown in cross section in Fig. 7. Type 1A is a mesa structure, and the others are planar. When a particular type was found to have inherent limitations far short of the design goals, it was abandoned and another type was started. The following is a very brief summary of the progress and findings of the investigations.

1. Type 1A. Single epitaxial, single-diffused NPN mesa. This was the starting point in the DET development. The type 1A had low breakdown voltages (BV_{EE}) and low inverse beta (β_r). Inversion of the P-type base surface was a severe problem.
2. Type 1B. Single epitaxial, double-diffused NPN planar. The value for reverse beta was greatly improved, but BV_{EE} remained low. There appeared to be a practical upper limit on BV_{EE} of about 15 v.
3. Type 2. Single epitaxial, single-diffused NPN planar. A usable range of β_r was achieved. A guard ring of P+ on the surface of the base was used to break the inversion problem. The BV_{EE} was increased to about 20 v. Variation in quality of starting material was thought to be causing considerable spread in final parameters.
4. Type 3. Double epitaxial, single-diffused NPN planar. An attempt to improve uniformity of parameters over type 2 by using epitaxial starting material was not successful. The uniformity was about the same. Values for BV_{EE} and β_r were similar to those for type 2.
5. Type 4. Single epitaxial, single-diffused PNP planar. Surface inversion was a problem in the 1A and 1B NPN devices. A similar PNP type was tried because it would be less susceptible to inversion. This type yielded low but uniform β_r. The BV_{EE} value was improved to 30 or 40 v. Attempts to increase β_r to a useful value brought only limited improvement. *On* resistance was greater than 100 ohms.

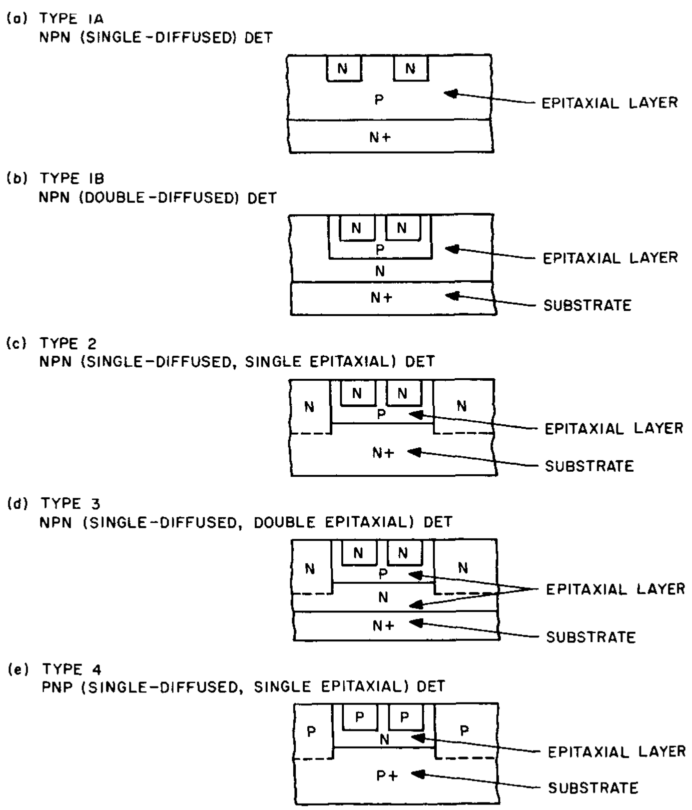

Fig. 7. Cross section of double-emitter transistor structures

Type 2 and type 3 double-emitter transistors came the closest to meeting the JPL requirements, and the work was concentrated on them during the latter part of the project.

An investigation was made of the effect of DET size on the critical parameters. From theory, increasing the DET size should decrease R_{on}, decrease BV_{EE}, increase transfer efficiency, and decrease speed. These factors were all verified experimentally. The trade-off between R_{on} and BV_{EE} again appears, this time as the predominant factor affecting size. The DET size finally chosen was 25 by 25 mils, with a collector area of about 400 square mils.

C. Integrated Switch

The switch was assembled as shown in Fig. 6. Scribe lines on the TO-18 header, Fig. 8, provided alignment points for the diode and the DET. Although the TO-18 package was an expedient choice for the purpose of the development project, it is not the optimum package by any means. A modified flat package could be used that would be compatible with integrated-circuit flat packs.

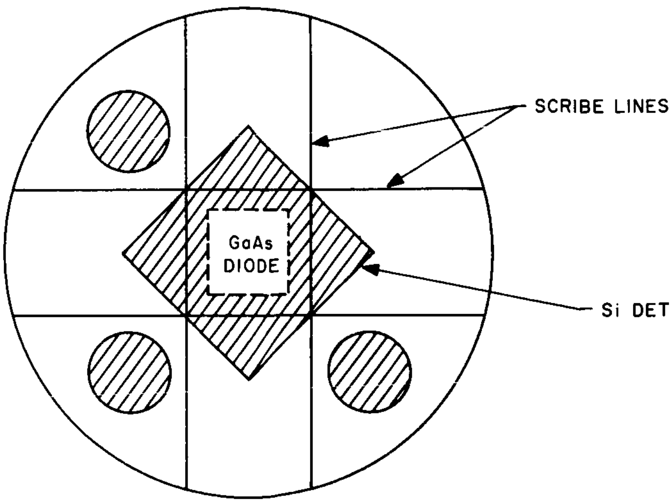

Fig. 8. Alignment lines

Efforts toward improving the photon coupling between source and detector included the investigation of materials with a high index of refraction, previously mentioned, and a unique focusing scheme. A considerable portion of the light emitted by the GaAs source appears at the edge of the chip in the plane of the diode junction. This light is wasted in the conventional assembly. An attempt was made to recover and make use of this light by placing the diode in a parabolic-shaped cavity and suspending the detector over the cavity. In a test made with a silicon solar cell detector 1.12 in. from the diode, the parabolic focusing gave a factor-of-8 improvement in detectable light over the flat-mounted source at an equal distance. However, when epoxy was added to the diode, the improvement factor decreased to about 4:1. In this experiment the detector was not coupled directly to the epoxy as in a photon-actuated switch.

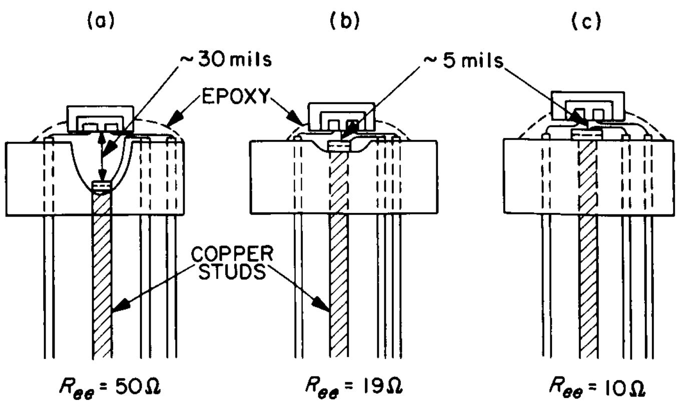

Fig. 9. Focusing experiment on photon-actuated switch

Complete switches were then fabricated in the three configurations shown in Fig. 9. The double-emitter transistors had matched gains. The *on* resistances were (a) 50 ohms, (b) 19 ohms, and (c) 10 ohms. The high R_{on} value of (a) is due to the 30-mil spacing as well as the effects of the epoxy. The fact that the R_{on} value of (b) was higher than that of (c) is in disagreement with the results obtained in the solar cell experiment. This inconsistency was not investigated further, owing to project schedule limitations. It was tentatively concluded that parabolic focusing did not offer a significant advantage.

The coupling efficiency of the switch is of great interest and could be considered a figure of merit. Efficiency is defined as the photon-generated base current divided by the diode current, or

$$\eta = \frac{I_b}{I_D} \tag{4}$$

The photon-generated current was determined by fabricating alternate rows of double-emitter transistors on a wafer, one row having provision for electrical base drive and the next row for photon drive. The efficiency was determined by using R_{on} as a normalizing parameter. A few complete switches were made with provision for electrical as well as photon drive, to verify the procedure. Figure 10 is a plot of I_b vs I_D for the different types of

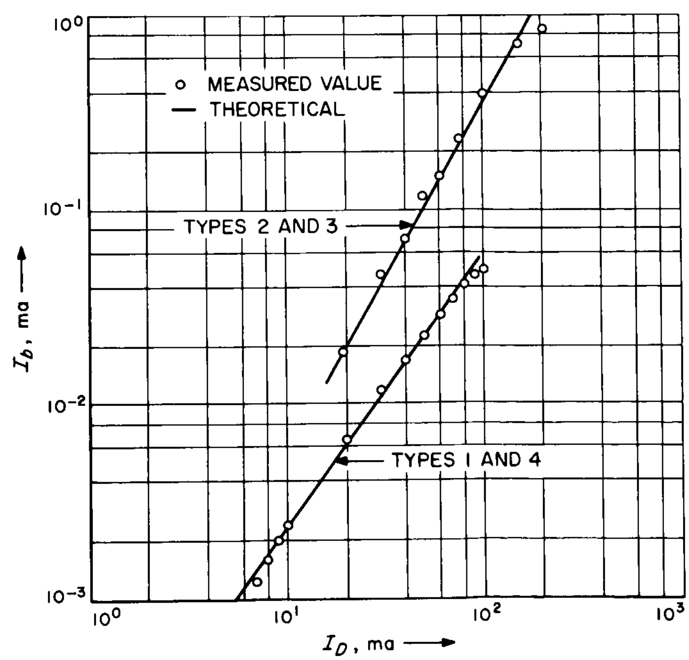

Fig. 10. Effective base current I_b vs diode current I_D for photon-actuated switches

switches. Efficiencies in Table 2 were calculated from Fig. 10. The efficiency varies with diode current and peaks within the range of the graph at 80 ma for types 1 and 4, and at 150 ma for types 2 and 3. The efficiency also increases with DET size, because the detector is able to receive more photons, but not linearly. Figure 11 shows that little increase can be expected with DET sizes larger than 25 by 25 mils, with a 5- by-5 mil diode.

Table 2. Typical efficiencies obtained for double-emitter transistors

Diode current I_D, ma	Efficiency, %	
	Types 2 and 3	Types 1 and 4
20	0.09	0.0325
40	0.175	0.041
60	0.25	0.048
80	0.29	0.0525
100	0.39	0.050
150	0.47	
200	0.425	

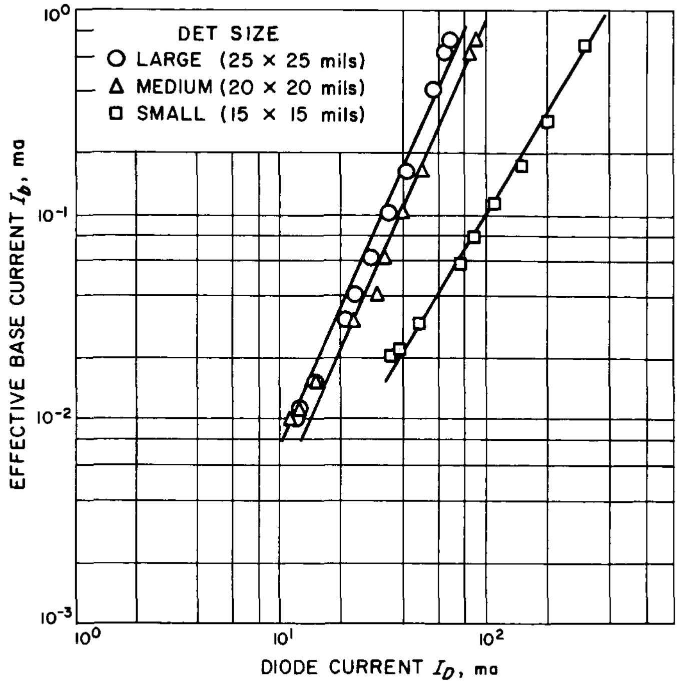

Fig. 11. Transfer efficiency vs size of double-emitter transistor (type 2)

III. TEST RESULTS

Device characterization was a necessary part of the photon-actuated switch development, and a great quantity of data was taken on the many trial runs. The data served to evaluate the success or failure of the run and were generally relegated to the experimenter's notebook. Toward the end of the development period, two DET runs, 168 (type 2) and 173 (type 3), yielded outstanding results. These double-emitter transistors were the peak achievement of the project and were used to assemble the light-actuated switches required for delivery to JPL. Attempts to duplicate these runs during the final months were unsuccessful, owing to processing problems and difficulty in obtaining good epitaxial starting material.

Fifty-one photon-actuated switches were assembled from run 168, and 53 from run 173. The two groups were not tested for all parameters, however, owing to time and manpower limitations. The most thorough testing was done on the run 173 devices, from which 20 were selected for delivery to JPL. This Laboratory also received 10 from run 168 that had received considerable testing.

The test procedures are given in Table 3 and in the associated figures (Figs. 12–18). Pulsed current measurements were substituted for dc measurements whenever possible, to avoid damage from overheating. Parameters investigated are discussed below.

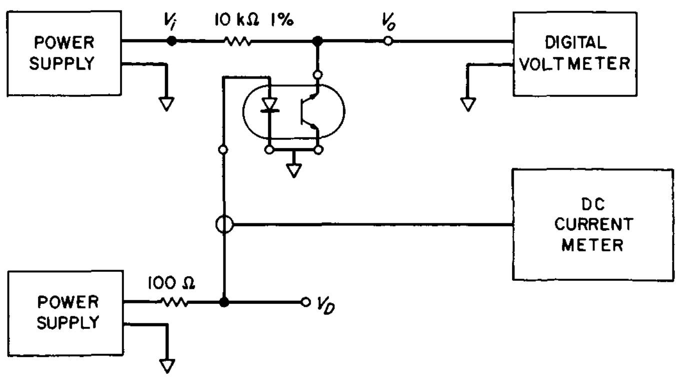

Fig. 12. Setup for tests 1A, 2, and 8 (R_{on}, V_D, and error band)

Table 3. Test procedures

Test	Parameter	Conditions	Procedures
1A	R_1 or R_{on} (dc)	I_D = 20, 30, 40, 50, 60 ma. $V_i = \pm 5$ v. $R_L = 10$ k Ω Temp. = −10°C, +25°C, +85°C.	(Fig. 12) Measure V_o at $V_i = +5$ and -5 v. $R_{on} = V_o \times 2000$. Record R_{on} at $V_i = +5$ and -5 v.
1B	R_1 or R_{on} (pulsed)	I_d (pulsed at 0.25 to 1 kc) = 50 to 100 ma; pulse width = 0.05 to 0.2 msec. V_i = 10 v (p–p) sine wave at 1 kc. Temp. = 25°C.	(Fig. 13) Measure V_o, peak to peak. $R_{on} = V_o \times 1000$. Record R_{on}.
2	V_D	I_D = 20, 30, 40, 50, 60 ma. Temp. = −10°C, +25°C, +85°C.	(Fig. 12) Measure V_D and record.
3	BV_{EE}	$I_D = 0$, $I_{EEO} = 0.1$ ma. Temp. = −10°C, +25°C, +85°C.	(Fig. 14) Measure and record BV_{EE} in both directions.
4	V_{os}	I_D = 20 to 60 ma. Temp. = −10°C, +25°C, +85°C.	(Fig. 15) Measure and record V_{os}. Care must be taken to avoid erroneous readings due to pickup and thermocouple effects.
5	I_{EEO} and R_2	$I_D = 0$, $V_i = \pm 5$ v. Temp. = +25°C, +85°C.	(Fig. 16) Measure and record I_{EEO} at $V_i = +5$ and -5 v. $R_2 = 5/I_{EEO}$. Record R_2.
6	R_3	$I_D = 0$, $V_i = \pm 35$ v. Temp. = +25°C, +85°C.	(Fig. 17) Measure current, $R_3 = 5/I$. Record R_3.
7	t_d, t_r t_s, t_f	I_d (pulsed at 10 kpps) = 40, 50, 60, 75, 100 ma. $V_i = \pm 5$ v. $R_L = 10$ k Ω, Temp. = −10°C, +25°C, +85°C.	(Fig. 18) Measure and record response times. Check for different readings at $V_i = +5$ and -5 v.
8	Error band	I_D = 20, 40, 60, 75, 100 ma. $V_i = \pm 0.1$ mv to ± 5 v. $R_L = 10$ k Ω. Temp. = −10°C, +25°C, +85°C.	(Fig. 12) Measure and record error voltage V_o at many values of V_i.
9	C_{ee}	$I_D = 0$, temp. = +25°C, freq. = 1 kc.	Measure capacitance between emitters on a precision bridge.
10	C_{de}	$I_D = 0$, temp. = +25°C, freq. = 1 kc.	Measure capacitance between diode terminals and emitters on a precision bridge.

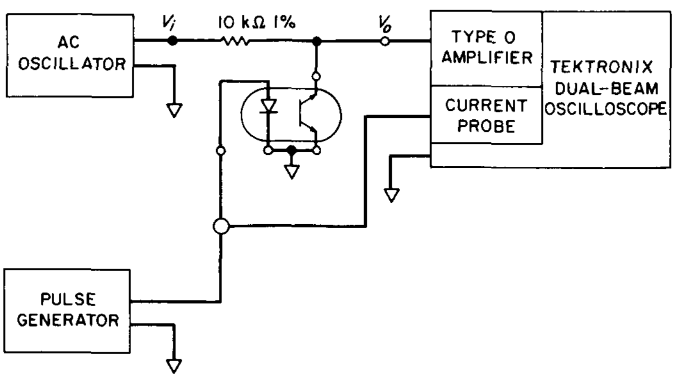

Fig. 13. Setup for test 1B (R_{on}, pulsed)

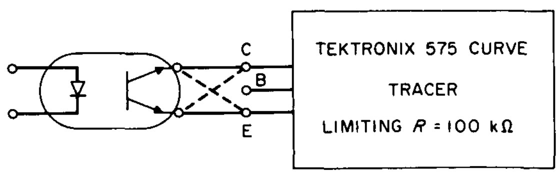

Fig. 14. Setup for test 3 (BV_{EE})

A. Switch-Closed Resistance R_1 or R_{on}

Test 1A gives the static, dc, *on* impedance of the switch. During testing of the first photon-actuated switches, it was found that constant diode currents of 100 ma destroyed some units. Analysis revealed broken wires to the DET that were caused by cracks in the epoxy. It was concluded that the cracks were caused by excessive heat in the diode. To prevent further failures, the diode current was limited to 60 ma dc. When higher current tests were necessary, the current was pulsed as in test 1B.

When current is applied to the diode, R_{on} reacts as shown in Fig. 19. The resistance increase from the initial

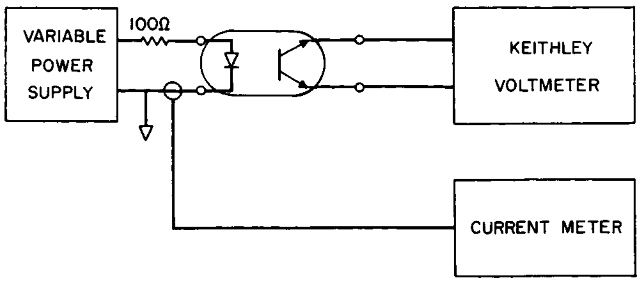

Fig. 15. Setup for test 4 (V_{os})

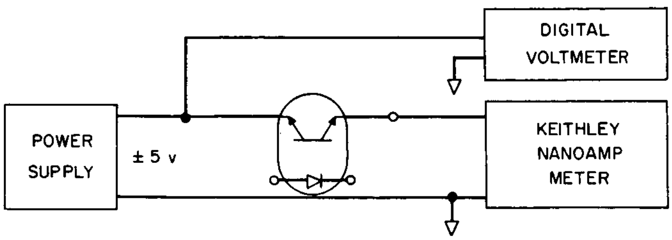

Fig. 16. Setup for test 5 (I_{EEO} and R_{off})

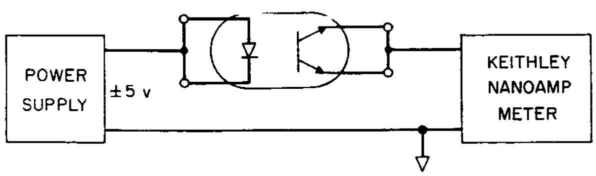

Fig. 17. Setup for test 6 (isolation resistance)

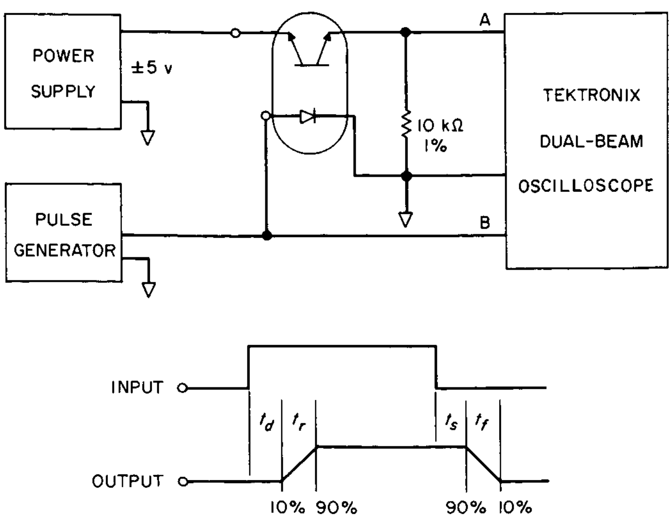

Fig. 18. Setup and measurement points for test 7 (switching times)

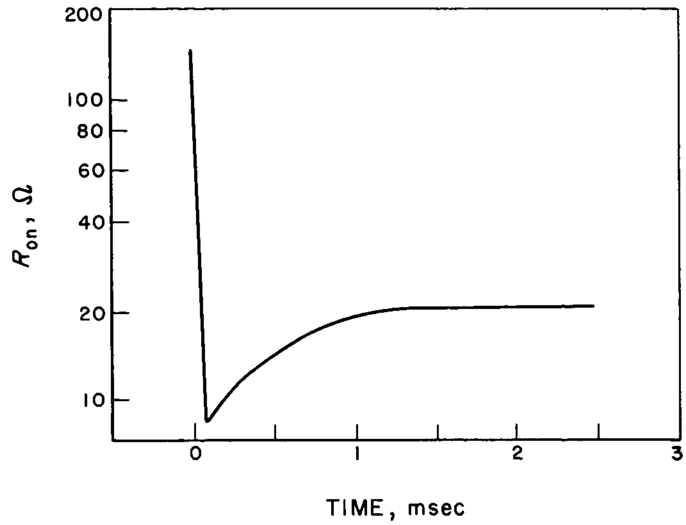

Fig. 19. Typical *on* resistance vs time

low value is due to diminishing light output from the diode, a condition that is caused by heating in the diode. The resistance levels off as the diode temperature stabilizes at some value higher than ambient. If the diode were prevented from heating by reducing the current density or providing a better heat sink than the TO-18 header, the dc (steady state) *on* resistance would approach the instantaneous (pulsed) resistance value. The pulsed R_{on} data in Fig. 20 are therefore representative of

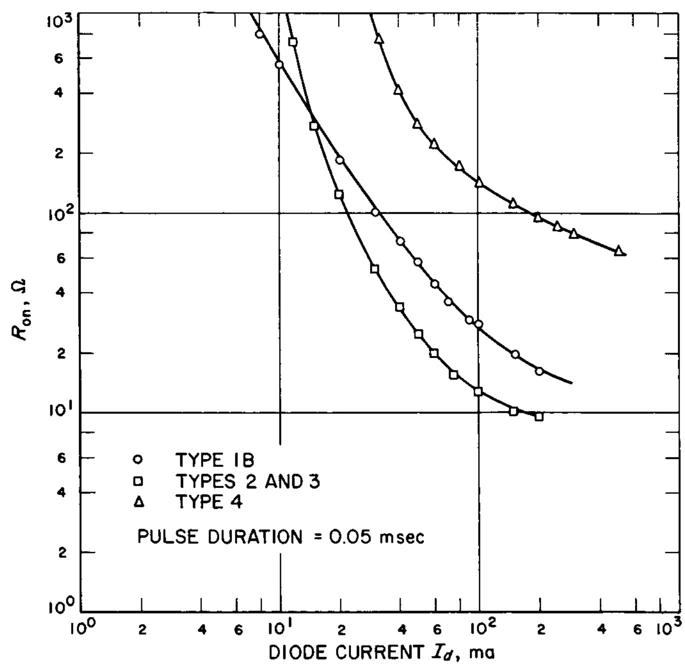

Fig. 20. Plot of R_{on} vs diode current (pulsed), typical for double-emitter transistors of types 1, 2, 3, and 4

the dc *on* resistance that could be achieved with better packaging.

Figures 21 and 22 are R_{on} (pulsed) vs I_d curves from IBM showing distribution of R_{on} and variation with temperature, respectively. The distribution curves represent about 80 switches with type 2 and type 3 double-emitter transistors. The temperature curves are typical. The slope of the type 3 (run 173) curves is less than would be expected from the GaAs diode negative temperature coefficient for efficiency of about 0.05% per degree centigrade.

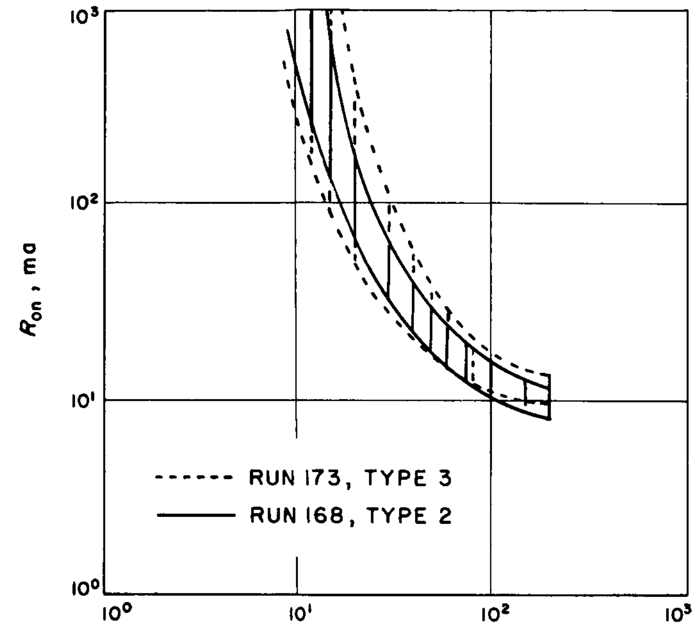

Fig. 21. Spread of R_{on} vs I_d

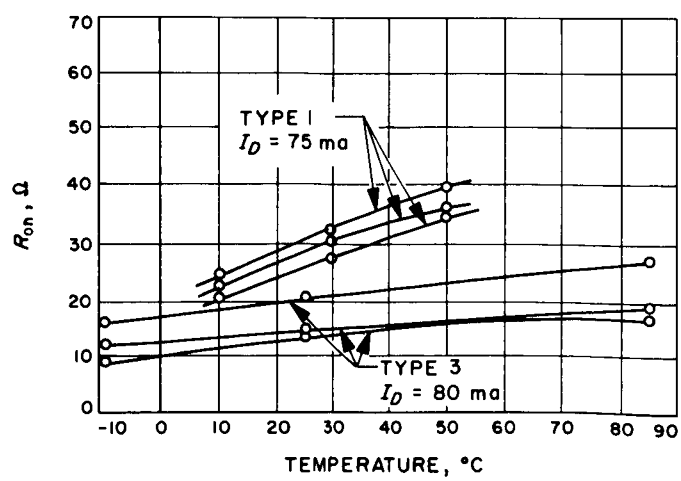

Fig. 22. Variation of R_{on} vs temperature

This is due to the compensating effect of the increase of the DET beta value with temperature.

Table 4 summarizes the R_{on} evaluation of the 20 switches assembled from run 173 double-emitter transistors and delivered to JPL. The number of switches that met the JPL specification requirement of 20 ohms or less at 50-mw drive (I_D = 40 ma) are shown in the first three data columns. Since all of the switches failed to meet the specification, they were evaluated against a relaxed requirement of 30 ohms at 75-mw drive (I_D = 60 ma). The results are shown in the second part of the table.

Table 4. Evaluation of 20 photon-actuated switches from run 173 for R_{on}

Source of data	Number of switches meeting specification					
	With $R_{on} \leqq 20\ \Omega$ at 40 ma			With $R_{on} \leqq 30\ \Omega$ at 60 ma		
	−10°C	+25°C	+85°C	−10°C	+25°C	+85°C
IBM ac	7	2	0	20	20	13
JPL photo	—	—	—	—	9	—
JPL dc	5	0	0	11	10	3
JPL dc	—	0	—	—	8	—
JPL ac				—	10	—
JPL ac after 1000 hr				—	5	—

Table 5. Increase in R_{on}, +25 to +85° C

Switch No.	R_{on}, Ω[a]		Increase, %
	+25°C	+85°C	
7	17	22	29
10	19	40	110
11	21	57	170
12	14	20	43
13	16	24	50
14	23	36	57
15	16	22	38
16	21	26	24
17	28	42	50
18	19	30	58
19	20	26	30
20	14	19	36
21	15	55	267
24	27	40	48
32	16	22	38
33	17	20	18
36	14	15	7
38	20	23	15
39	24	39	62
40	16	16	0

[a]From initial pulsed current data at I_d = 60 ma. Pulse duration = 0.05 ms.

The gradual increase in R_{on} from test to test is a more severe problem than the fact that the switches failed to meet the specification. From careful evaluation of the initial test data, summarized in the boxhead of Table 4, it appears that some of the switches suffered deterioration during the high-temperature test. The R_{on} increase, shown in Table 5, varied from 0% to 267%. (No final data were taken at +25°C to determine how much of this increase was permanent.) The next data were taken on a Tektronix Transistor Curve Tracer. These photographic data, representing a pulsed current test of only moderate accuracy, revealed only nine switches with R_{on} values of 30 ohms or less. From this it is concluded that at least 10 switches had suffered permanent degradation.

Two more switches exceeded 30 ohms during the first dc temperature test at 60 ma. At this point, six of the poorest switches were replaced with other units. Subsequent pulsed current life-testing of the original switches caused further degradation, as noted in Table 4. Figure 23 is a graph of R_{on} vs time for several of these switches. The curves are typical of the different types of performance observed. It is apparent from the different slopes that more than one mode of degradation occurred.

Six switches assembled with double-emitter transistors from run 168 (type 2) were delivered to JPL three months before the end of the development activity. During dc R_{on} testing, three were destroyed by the thermal effect mentioned previously. Four more were received in January 1965. Five of these units were put on the pulsed current life test. The results in Fig. 24 show only slight degradation. Units 8 and 10 had been through a 1000-hr, +85°C temperature test at IBM before delivery to JPL. Units 11, 12, and 19 are from the group of six received

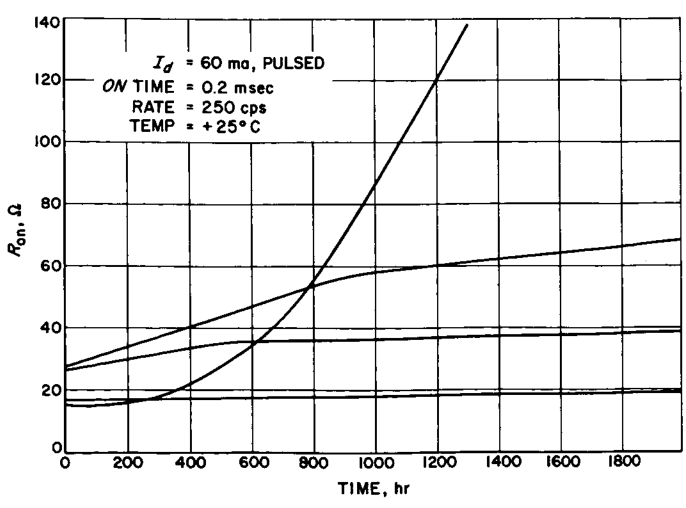

Fig. 23. Typical performance of photon-actuated switch

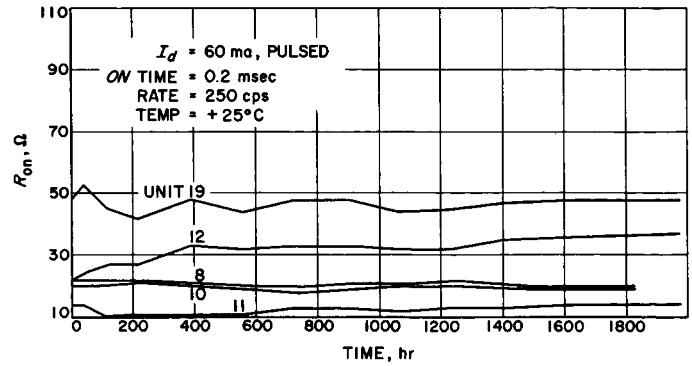

Fig. 24. Pulsed current life test of double-emitter transistor, type 2

originally. Unit 19 held fairly constant even though the data are somewhat erratic; this condition appeared at the time the other three units were damaged.

Two switches from run 168 and two from run 173 were placed on a 50-ma, dc life test. The result is shown in Fig. 25. Units 168-6 and -7 had experienced a previous 1000-hr, +85°C temperature–life test. Unit 6 went through another 1000 hours at +25°C. Taking this accumulated time into account makes the units from run 168 look more stable than those from run 173.

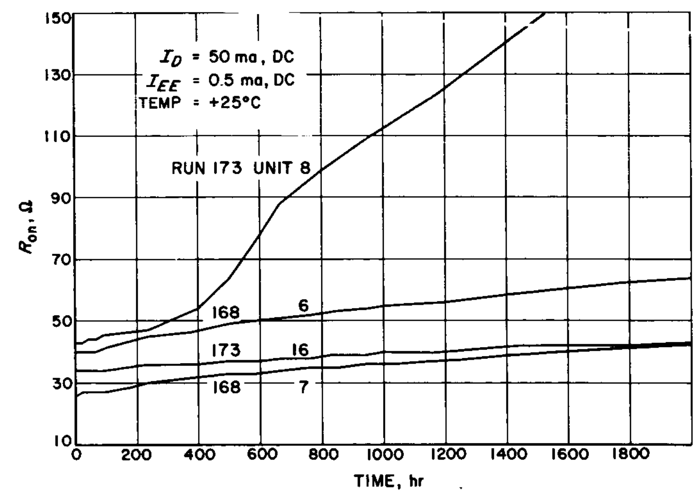

Fig. 25. Direct current life test of double-emitter transistor, types 2 and 3

B. Switch-Open dc Resistance R_2

The parameter R_2, which represents the isolation between the switch contacts (emitter to emitter) in the *off* state, is determined by measuring leakage current I_{EEO} as shown in Table 3. The specification calls for 100 megohms or more at +85°C. Three of the 20 switches from run 173 failed to meet the requirement, but all 20 switches were greater than 5000 megohms at +25°C, equivalent to a leakage current of less than 1 nanoamp.

All of the six original switches from run 168 failed to meet the R_2 requirement at +85°C. The value for one unit was only 57 megohms at +25°C and dropped to 640 kilohms at +85°C.

C. *Isolation Resistance* R_3

This parameter is a measure of the isolation between the diode and the DET. Since the epoxy coupling medium is the only path for conduction, the specification minimum of 100 megohms was exceeded by quite a margin. Measurements taken at 35 v and +85°C show all of the 20 units at values greater than 1×10^{11} ohms.

D. *Switch-Closed Contact Potential (Offset Voltage)* V_{os}

Offset voltage is an indication of (1) asymmetry between the halves of the DET, (2) unequal beta values, or (3) unequal illumination. It induces an error that reaches significant proportions when the switch is handling signals in the low-millivolt range. The specification calls for 50 μv or less over the full temperature range. Difficulty was encountered in measuring offset voltage because of thermocouple effects and the high impedances involved. The data, however, are accurate to approximately 20%.

The distribution of offset voltage in percentages is given in Table 6 for the 20 switches from run 173. Offset voltage varies with drive and temperature. The data in Table 6 were taken with I_D = 60 ma. A definite correlation was noted between high *on* resistance and high offset voltage. The six switches that exceeded 100 μv at +25°C are the same ones that had high values for R_{on}.

Table 6. Percentage distribution of V_{os}

Data source and conditions	% of units with V_{os} as indicated			
	$\leq$ 50 μv	50 to 100 μv	100 to 200 μv	> 200 μv
IBM data on 20 switches (run 173).				
Temp. = −10°C to +85°C.	30	25	30	15
Temp. = +25°C.	65	35	0	0
JPL data, same lot as above. Temp. = +25°C.	60	10	10	20

Offset voltage in type 1 double-emitter transistors is generally less than 50 μv, owing to the higher beta values. Offset in switches with type 2 double-emitter transistors is comparable with that of type 3.

E. *Breakdown Voltage, Emitter to Emitter,* BV_{EE}

The BV_{EE} parameter specifies the maximum voltage-handling capability of the photon-actuated switch. The

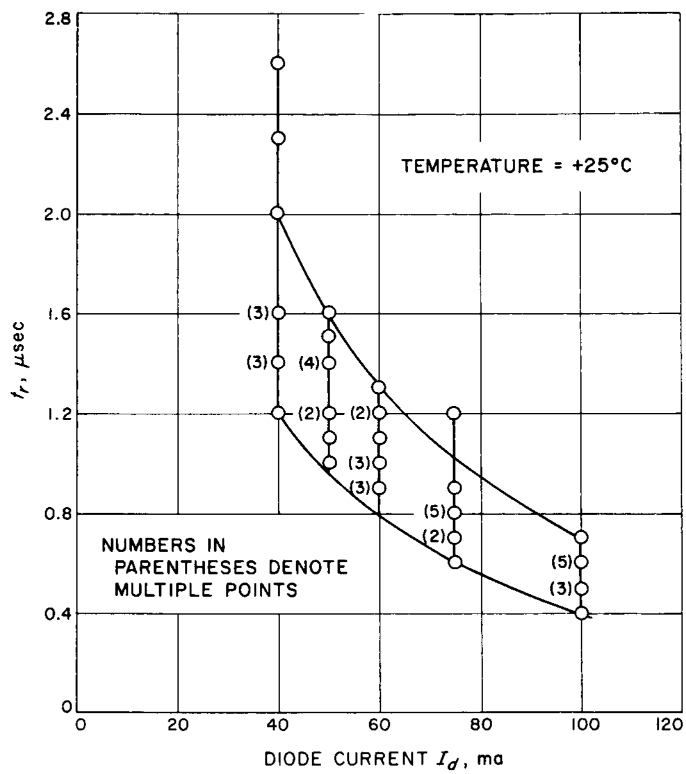

Fig. 26. Rise time vs diode current (pulsed) for 10 photon-actuated switches, type 2

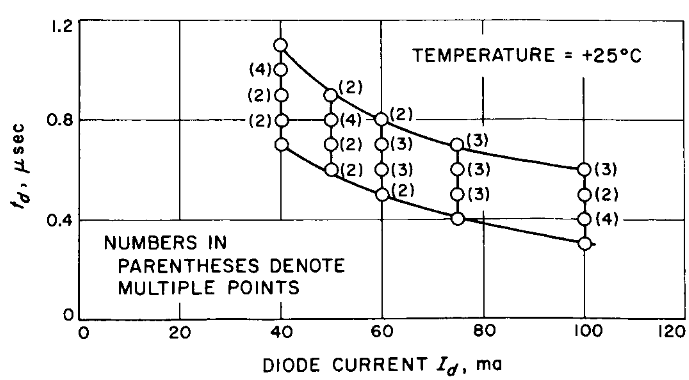

Fig. 27. Delay time vs diode current (pulsed) for 10 photon-actuated switches, type 2

breakdown of both emitter junctions was measured at currents from 100 μa to 10 ma. At +25°C, breakdown in run 173, type 3 double-emitter transistors was 20 to 24 v at 100 μa and 15 to 19 v at 10 ma. A decrease of about a volt occurred at +85°C and an increase of less than a volt at −10°C. The breakdown voltage in type 2 DETs from run 168 was slightly lower. There was virtually no change in the BV_{EE} of five type 2 photon-actuated switches during a 1000-hr, +85°C shelf life test.

F. Switching Times t_d, t_r, t_s, and t_f

Switching time can be divided into four discernible parts: delay, rise, storage, and fall time. These parameters were measured as shown in Table 3 and Fig. 18. The results are given in Figs. 26–29, which show the

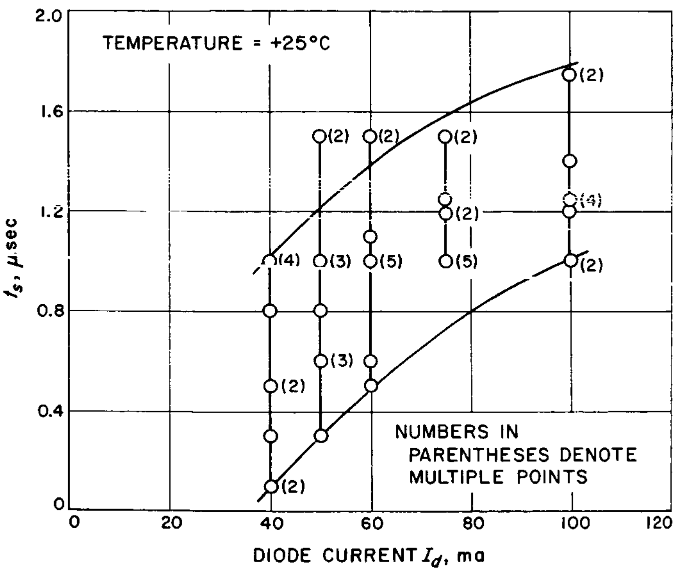

Fig. 28. Storage time vs diode current (pulsed) for 10 photon-actuated switches, type 2

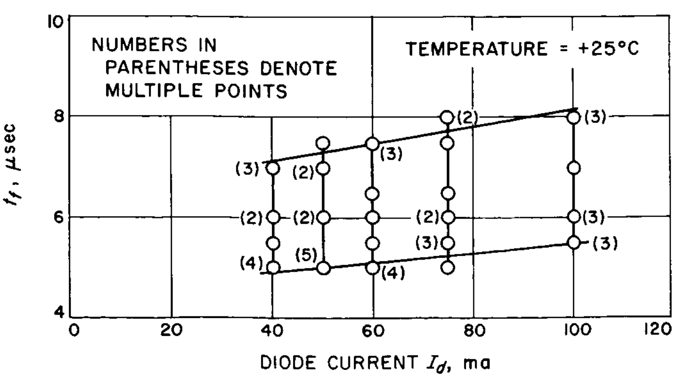

Fig. 29. Fall time vs diode current (pulsed) for 10 photon-actuated switches, type 2

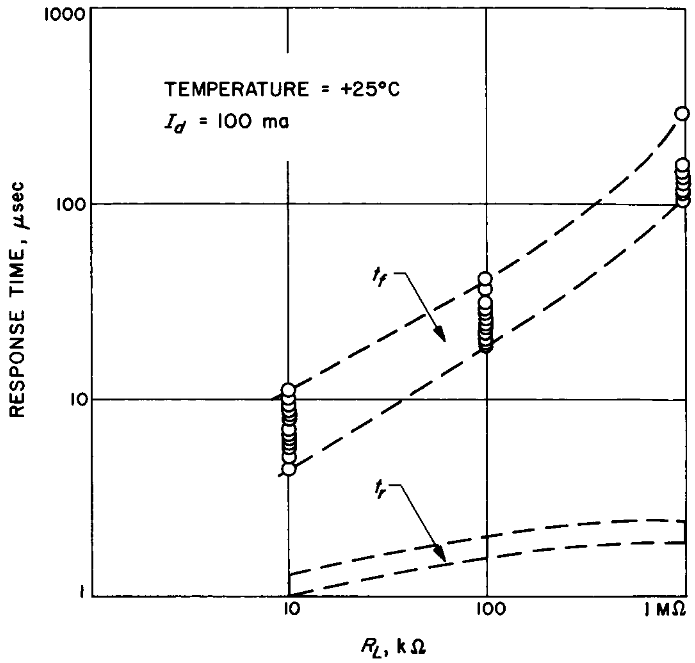

Fig. 30. Dependence of response times on load for double-emitter transistors, type 2

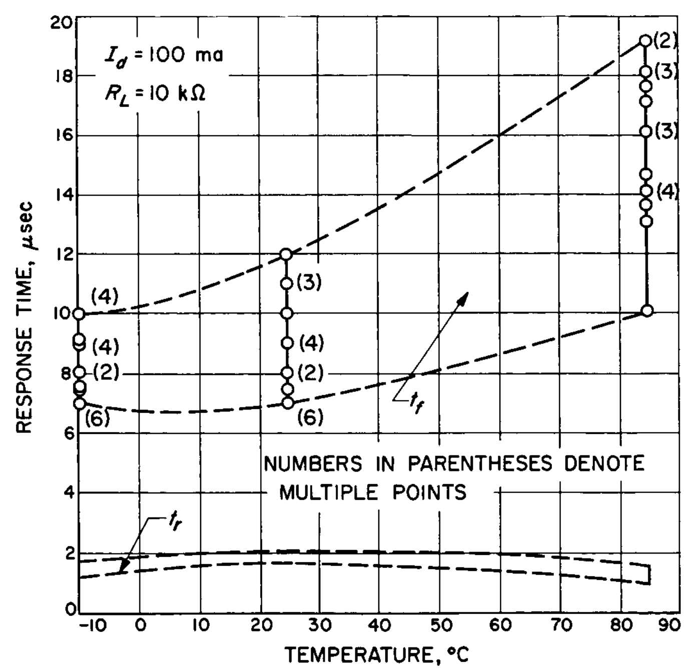

Fig. 31. Dependence of response times on temperature for double-emitter transistors, type 3

variation of these parameters with diode current. The delay and rise times vary inversely with drive current, while storage time increases with drive. The fall time is relatively independent of drive, increasing only slightly, from 40 to 100 ma.

The long fall times are typical of transistors turning off without benefit of reverse (negative) drive. Fall time is a direct function of load resistance, since R_L is the discharge path for the charge within the DET. The switching times given above were measured with a 10-kilohm load resistor according to thc procedure in Table 3.

Dependence of switching time on R_L and temperature is shown in Figs. 30 and 31, respectively.

G. *Error Band*

The purpose of this test was to show the combined effects of all errors between the input and output of the photon-actuated switch. This consisted primarily of the errors contributed by the offset voltage and the *on* resistance, and was specified to be no greater than $\pm 1\%$ of full scale. A plot of V_{in} vs V_{out} does not give an adequate graphical presentation of the error band, because

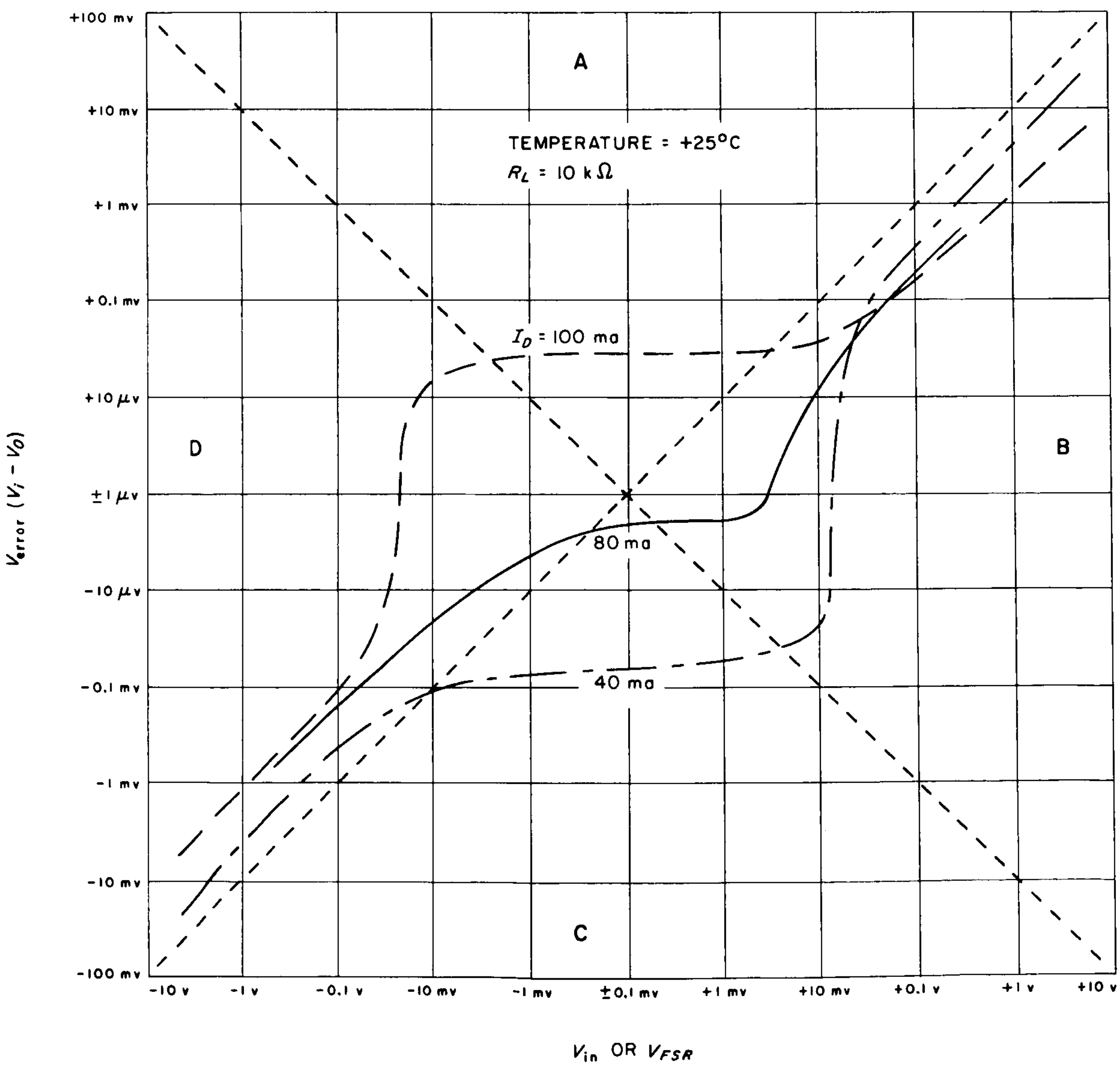

Fig. 32. Effect of diode current (pulsed) on photon-actuated switch error

of the small amount of error in relation to input and output voltages. Plotting V_{in} vs V_{error} on log–log paper gives a much clearer picture of the test results, particularly at low input voltages. Figure 32 shows such a plot of the data from switch 168-9 at three diode currents. This switch is interesting because its offset voltage passes through zero at a drive current near 80 ma.

This graph can also be used to indicate when the switch error exceeds 1% of full scale by relabeling the ordinate (x-axis) V_{FSR} and dividing the graph into four areas, A, B, C, and D, with dotted lines. When the error curves are in areas A or C, the error is greater than 1% of full scale (V_{FSR}). In B or D, the error is less than 1% of full scale. It can be seen from the graph that 10 mv is about the lowest full-scale range that could be used with this switch and retain the 1% accuracy. The position of the error curves change with temperature and load resistance also. The change with temperature was relatively small, the general shape of the curve remaining unchanged. As load resistance is increased, the portion of the error curve that is affected by the ratio of R_1 to R_L changes as shown in Fig. 33, indicating that accuracies considerably greater than 1% can be obtained with higher load resistance.

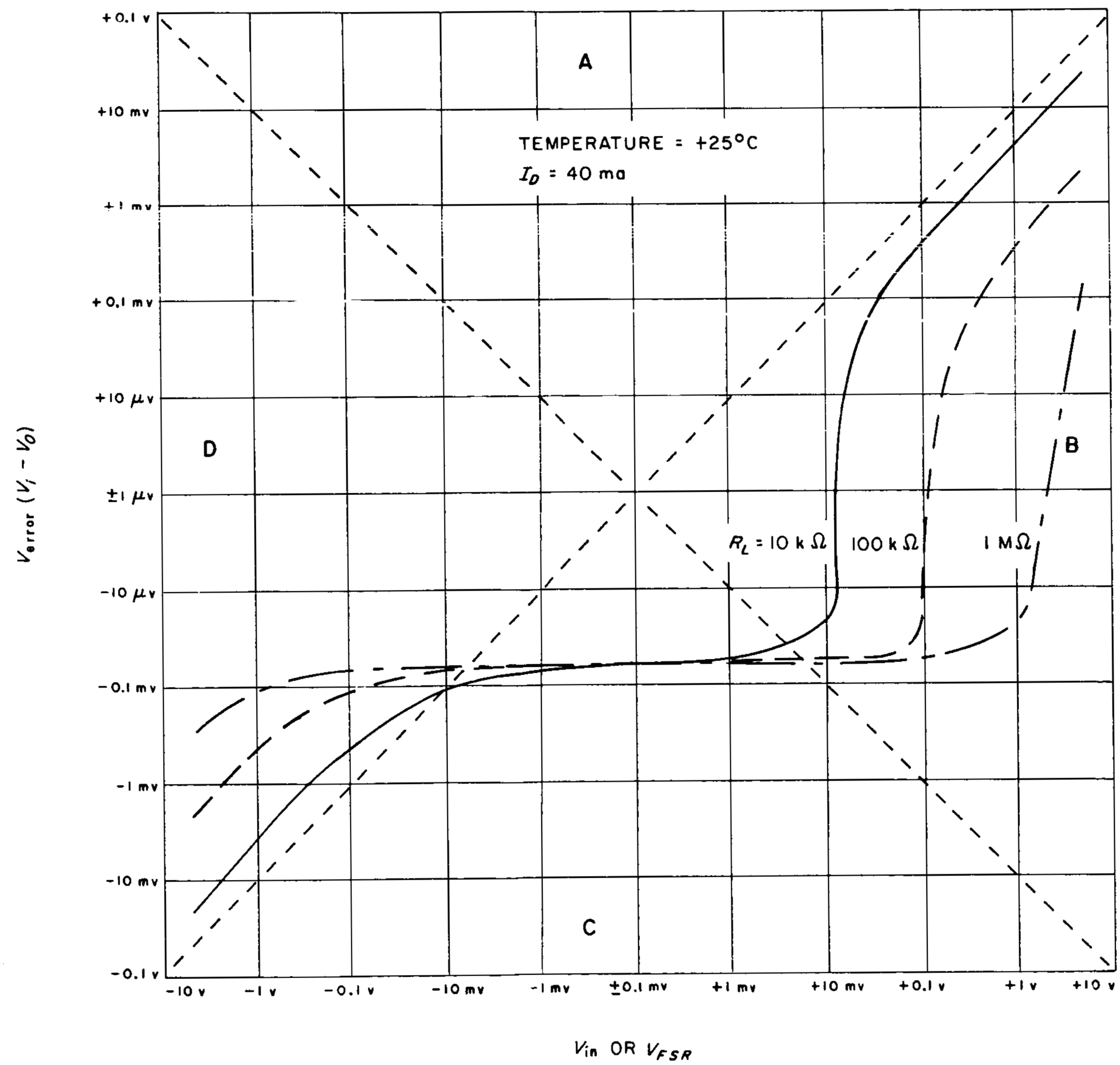

Fig. 33. Effect of load resistance on photon-actuated switch error

H. Feedthrough Capacitance C_{ee}

Although the dc *off* resistance of the photon-actuated switch is 100 megohms, its pulsed current impedance from emitter to emitter is somewhat less owing to the capacitance between emitters (see Fig. 3). This parameter was not covered in the original specification; however, a test was made (Table 3) to determine its value. In type 3 DETs from run 173, the value for feedthrough capacitance C_{ee} was consistently 6.6 pf. In type 2 DETs from run 168, it varied from 6 to 24 pf with most values in the range of 6 to 10 pf.

I. Isolation Capacitance C_{de}

Isolation capacitance (Fig. 3), another parameter not covered by the specification, was measured as shown in Table 3. Its value was consistently 2.4 to 2.6 pf in types 2 and 3 DETs. (The capacitance is determined by the spacing between diode and DET, which is about 5 mils, and the package capacitance.)

J. Diode Voltage V_D

Although the V_D parameter was not covered in the design specification, it is of interest for the purpose of designing drive circuitry. The diode voltages of 26 photon-actuated switch units were measured at various currents over the temperature range. These data have been distilled into the graph of limit curves shown in Fig. 34.

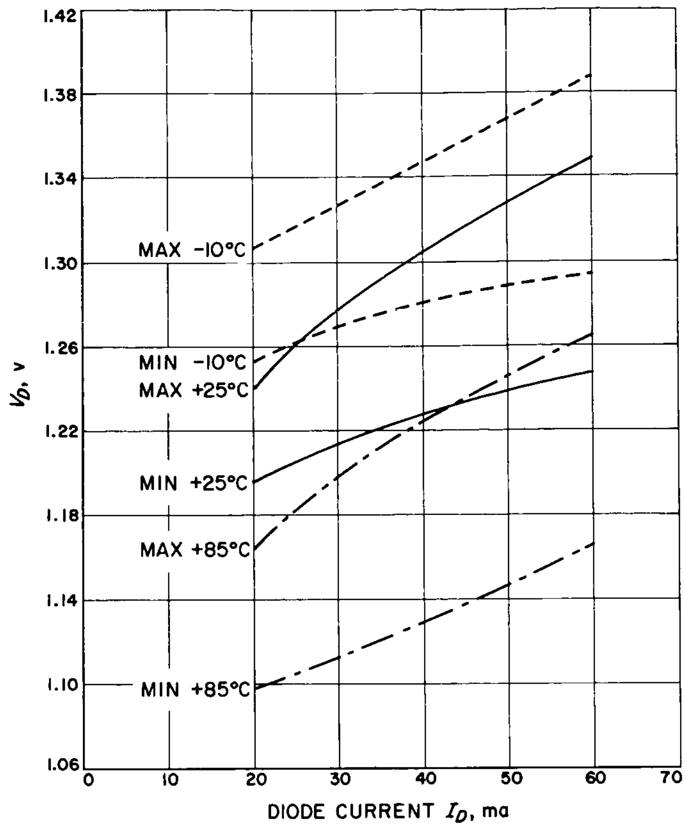

Fig. 34. Diode characteristics

IV. DISCUSSION

The high point of the photon-actuated switch development is represented by units made with DETs from runs 168 (type 2) and 173 (type 3). It is clear from the test results, summarized in Table 7, that some of the specified design objectives were not met, even with these units. This is not a great disappointment, however, since the specified objectives were somewhat arbitrarily chosen. The offset voltage, for example, becomes a problem only when the switch is used for very low level switching.

It is unlikely that the specified goals for R_{on} and BV_{EE} can be met in one device, since the design of the DET requires a compromise between these parameters. The values given for R_{on} and BV_{EE} in Table 7 are usable for many multiplexing applications.

Table 7. Summary of parameter values achieved

Parameter	Value
R_{on}	30 Ω with 60-ma drive (75 mw)
R_2	$> 10^8$ Ω
R_3	$> 10^{11}$ Ω
BV_{EE}	> 20 v at 100 μa
V_{os}	100 μv
C_{ee}	< 6 pf
$t_{on} + t_{off}$	< 20 μs with $R_L = 10$ k Ω

The gradual increase in R_{on} with time indicates an instability that precludes the use of the photon-actuated switch in the near future. This instability is thought to stem mainly from the GaAs diode. One possible mode of degradation is surface leakage current. The forward-bias diode current can be divided into two parts, surface current and bulk current. The bulk current generates heat and light, the surface current heat only. If the surface current increases because of contamination of the junction, a greater percentage of available current will be wasted on non-photon-generating effects. The use of a planar diode with a passivated surface should minimize this failure mode.

It has been shown that there is a direct relationship between current density in the GaAs diode and deterioration of photon output. A possible explanation is that greater current density causes increased heating, which tends to bring the bulk impurities to the surface. If this happens, the surface will be further contaminated, increasing the effect described above.

Attempts to demonstrate the reproducibility of the results obtained in DET runs 168 and 173 were unsuccessful. Poor epitaxial starting material and errors in diffusion were causes of failure in most of the runs. This does not mean the good results are not reproducible, but simply that further work is required.

The TO-18 header used during the course of the contract is by no means optimum packaging. A flat package is preferable for future use. Moreover, a good heat sink will probably be required to optimize R_{on}.

The epoxy coupling medium appears satisfactory, although glasses with higher indices of refraction would improve R_{on} or, conversely, lower drive power.

V. CONCLUDING REMARKS

Considerable progress was made in the development of a new type of multiplex switch that is entirely solid-state. It was demonstrated that useful parameters can be achieved in such a device. Certain problem areas were uncovered, which require further investigation.

Work is being done by Texas Instruments, Inc., the General Electric Company, Westinghouse Electric Corporation, Hewlett-Packard, and others in the areas of photon emission from GaAs and detection in silicon devices, which shows promise of applicability to future spacecraft equipment. In addition to multiplex switching, these techniques may be applied to interface isolation for the elimination of ground loops in large systems, isolated current probes or transducers, and amplifiers requiring extremely high common-mode rejection and/or input isolation. The unilateral properties of photon-coupling can be most useful in applications where isolation from load variations is necessary, in ultra-stable oscillators for example. Photon-coupled devices have unique properties that, when fully developed, will be very useful in future aerospace equipment.

VI. RECOMMENDATIONS

The following courses of action are recommended, in order of priority, in the event that further work is done on photon-coupled multiplex switches:

1. Solve the degradation problem and demonstrate stable performance for a minimum of 10,000 hours.
2. Demonstrate the reproducibility of useful parameters.
3. Optimize the package for future equipment requirements. The possibility of improved photon coupling through the use of reflective and focusing surfaces should be investigated. A thermal study is a prerequisite to the packaging task.
4. Investigate methods of obtaining better optical matching between the diode and the detector.

APPENDIX

Multiplexer DC Analysis

The basic multiplexer for sampling analog signals is shown in Fig. A-1. The switches are closed sequentially by some driving source. When implemented with an electromechanical device with metal-to-metal contacts, the switch-closed impedance is close to zero ohms and the switch-open impedance is infinity. Under these conditions, E_{out} equals E_{in} and the error is zero. However, when the multiplexer is implemented with solid-state (semiconductor) devices, a complex relationship exists between E_{in} and E_{out}.

The schematic of a solid-state switch suitable for multiplexing low-level signals is shown in Fig. A-2a. A single transistor with two emitters (Fig. A-2b) may also be used. The driving source may activate the switch with electrons or photons. In either event the source is isolated from the transistors by a high impedance. A theoretical model of the dc equivalent circuit is shown in Fig. A-3.

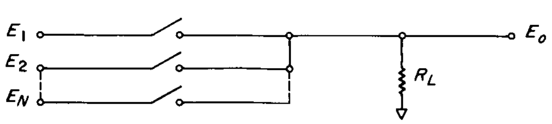

Fig. A-1. Basic multiplexer for sampling analog signals

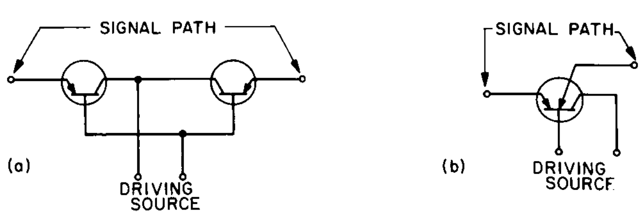

Fig. A-2. Solid-state switches suitable for multiplexing low-level signals

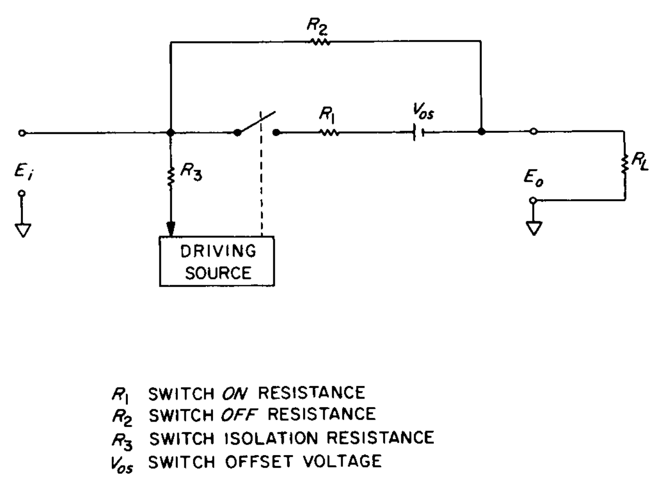

Fig. A-3. DC equivalent circuit

The equivalent circuit of the solid-state multiplexer is given in Fig. A-4. The isolation resistance R_3 is omitted, since it is well over 1000 megohms and has an insignificant effect.

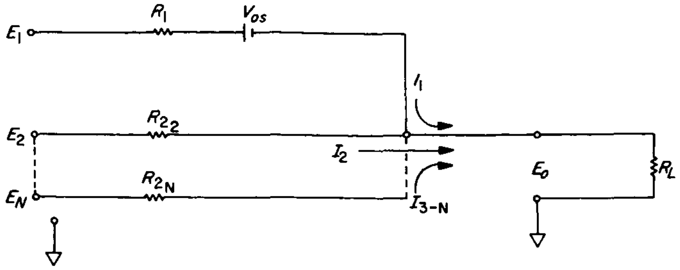

Fig. A-4. Equivalent circuit for solid-state multiplexer

The expression for output voltage is

$$E_o = R_L (I_1 + I_2 + \cdots\cdots + I_N) \qquad \text{(A-1)}$$

This expression expands into a very complex and unwieldy formula because of the parallel effect of the branch circuits. Some simplification is therefore necessary. All R_2 values can be assumed equal, since they are similar and are several orders of magnitude greater than R_1 or R_L. Values for E_2 through E_N are made equal and are assigned a worst-case value. For example, if E_1 is maximum, E_N is assigned a minimum value. Assigning R_2 a minimum worst-case value keeps the following expressions worst-case. The equivalent circuit of the multiplexer then takes the form shown in Fig. A-5.

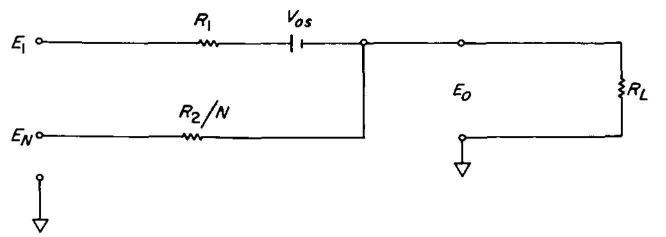

Fig. A-5. Simplified equivalent circuit for the multiplexer

Solving for E_o by summing currents at the output mode,

$$E_o = \frac{R_L [R_2 (E_1 + V_{os}) + E_N R_1 N]}{R_L R_2 + R_1 R_2 + R_1 R_L N} \qquad \text{(A-2)}$$

The switch error in percent is

$$\left(\frac{E_1 - E_o}{E_1}\right) 100 = \left(1 - \frac{E_o}{E_1}\right) 100$$

Substituting Eq. (A-2) for E_o gives

$$\left[1 - \frac{R_L [R_2 (E_1 + V_{os}) + E_N R_1 N]}{E_1 (R_L R_2 + R_1 R_2 + R_1 R_L N)}\right] 100 \qquad \text{(A-3)}$$

A more useful expression is the percent error related to the full-scale range (FSR) of the multiplexer. The percent error of FSR is

$$\left[\frac{E_1 - \dfrac{R_L [R_2 (E_1 + V_{os}) + E_N R_1 N]}{R_L R_2 + R_1 R_2 + R_1 R_L N}}{E_{FSR}}\right] 100 \qquad \text{(A-4)}$$

If $R_2 >> R_L > R_1$, $E_1 >> V_{os}$, and if N and E_N are small,

$$E_o \cong \frac{R_L R_2 E_1}{R_L R_2 + R_1 R_2} = \frac{E_1 R_L}{R_L + R_1} \qquad \text{(A-5)}$$

and the percent error of FSR is approximately equal to

$$\left[\frac{E_1 \left(1 - \dfrac{R_L}{R_L + R_1}\right)}{E_{FSR}}\right] 100 \qquad \text{(A-6)}$$

The error is maximum when $E_1 = E_{FSR}$. Therefore, the maximum percent error is approximately equal to

$$\left[1 - \frac{R_L}{R_L + R_1}\right] 100 \qquad \text{(A-7)}$$

regardless of full-scale range.